Local Interface RF Passivation Layer Based on Helium Ion-Implantation in High-Resistivity Silicon Substrates

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***Abstract*—An original method to locally fabricate interface passivation layers embedded in Silicon-on-Insulator substrates is presented. This method consists in creating defects under the Buried Oxide (BOX) thanks to helium implantation followed by thermal annealing. The performances of the resulting substrates were evaluated through RF characterizations using coplanar waveguide structures to extract effective resistivity and harmonic distortion. Both figures of merit (FoM) are greatly improved by the formation of buried defects layer, reaching 2nd harmonics below -100 dBm and effective resistivities of 4 kΩ.cm. This performance is comparable to commonly used polycrystalline silicon Trap-Rich (TR) layers when measured with similar experimental conditions. Furthermore, we obtained RF performances that were stable with the bias voltage (between – 15 V and + 15 V) and the operating temperature up to 100°C. This approach can efficiently be locally implemented on a wafer to create passivation layer, making it very promising in order to enable co-integration with Fully Depleted-SOI technology requiring back-gate access.**

***Keywords*—RF-SOI, harmonic distortion, effective resistivity, Local passivation layer, helium implantation, FD-SOI co-integration.**

I. Introduction

In the radio frequency (RF) domain, substrates can highly impact devices performance [1]. To make silicon substrates compatible with RF requirements, High Resistivity (HR) silicon base wafers were introduced in the 2000's [2]. However, this solution suffered from the Parasitic Surface Conduction (PSC) effect which seriously degraded RF performances [3]. In order to reduce those losses and mitigate the PSC effect, a so-called Trap-Rich (TR) layer was introduced beneath the buried oxide (BOX) of an HR-SOI substrate. This was achieved using polycrystalline silicon (Poly-Si) deposition [3]. Alternatively, this can be done using porous silicon [4], or double BOX Trap-Rich [5]. Nowadays, Fully Depleted Silicon-on-Insulator (FD-SOI) technology aims to provide a platform for high performance and low power computing specially thanks to its dynamic threshold voltage control by back-gate [6]. In this context, a co-integration of RF devices with FD-SOI logic circuits is desired. Nevertheless, since the TR layer is made of defect-rich Poly-Si, the integration of the back-bias features of FD-SOI is very challenging, making full sheet TR solutions incompatible with FD-SOI [7]. One alternative to preserve the back-bias features of active devices is to locally form TR layers on wafers beneath RF passive devices, leaving conductive crystalline Si below regions where back-biasing is needed. PN junctions [7-8-9], deep level impurities passivation [10] or local Poly-Si fabrication [11] can be used to that end. In this paper, we explore an original approach for local interface passivation layer fabrication. It is based on the generation of buried cavities and crystalline defects in an HR-Si crystal beneath the oxide layer of an HR-SOI substrate. This is achieved using helium (He) ion implantation followed by thermal annealing to form crystalline defects and cavities beneath the BOX [12]. Because ion implantation can easily be performed locally, this technique is compatible with FD-SOI co-integration. Here, we study the impact of cavities and defects size and morphology on RF electrical performances by tuning post-implantation annealing [12-13].

II. Experiments

HR-Si p-type wafers with nominal resistivities between 3 kΩ.cm and 8 kΩ.cm were used as starting materials. The substrates were thermally oxidized (at 900°C during 1 hour and 36 minutes in a dry atmosphere), leading to the formation of a 200 nm-thick SiO_2 layer. Samples were then implanted with He^+ ions at 45 keV with a dose of 3×10^{16} at/cm² at room temperature. A second He^+ implantation was performed at lower energy (17 keV) and higher dose (9×10^{16} at/cm²). Samples were then annealed in a vertical furnace for 2 hours at various temperatures: 400, 600, 800, 900 and 1100°C. In the following, those substrates containing cavities are respectively named B400, B600, B800, B900 and B1100. A non-annealed sample, named B0, is kept as a reference. Two reference samples were also fabricated: (i) un-implanted oxidized HR-Si substrate (labelled HR) and (ii) a sample made of a 100 nm-thick Poly-Si deposited on HR-Si by Low Pressure Chemical Vapor Deposition (LPCVD) followed by a 200 nm oxide deposition by plasma-enhanced (PE)-CVD to get a TR-like reference (labelled TR). Then, Coplanar Waveguides (CPW) were fabricated on all samples for RF characterization. For that, a 200 nm-thick TEOS was first deposited at 260°C. A 100 nm-thick Ti layer and a 1 µm-thick Au layer were then deposited and patterned to define CPW lines. A schematic view of the final stack together with the CPW design is represented in Fig. 1. Then, large- and small-signal RF characterizations were performed to extract RF performances.

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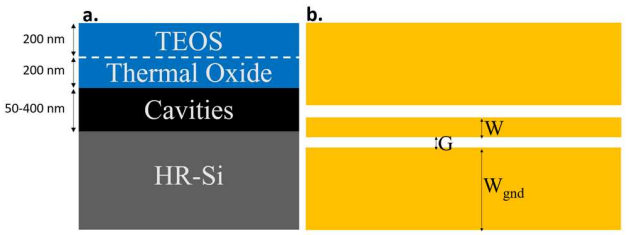

Fig. 1. (a) Representation of the substrates stack. (b) Schematic illustration of the CPW used for RF characterizations with W = 70 µm, G = 42 µm, W_{gnd} = 316 µm and a length of 1.5 mm.

III. Large-Signal Characterization

On silicon-based substrates, passive devices such as CPWs present Harmonic Distortion (HD) between their input and output, which degrades signal integrity. This is due to the semiconductive nature of such substrates, whose electrical properties (conductivity) may be modulated by an applied electric field (field-effect).

When a voltage (or interface fixed charges) is applied to the CPW, substrate-charges will be induced beneath the CPW signal line. Those substrate charges may consist in (i) free carriers (electrons or holes) or (ii) ionized trap states [14]. If substrate charges are free carriers, the substrate's interface conductivity is highly increased (PSC effect), leading to losses and non-linearities. Instead, the substrate engineering methods proposed target charge-compensation schemes -such as deep trap states- that do not involve the generations of large quantities of free interface carriers [14]. Overall, this implies that the interface Fermi-level is strongly pinned by the traps distribution. The energy level E_{pin} of this pinning is determined by the acceptor and donor trap distribution functions in the material. The absolute position of E_{pin} has a strong impact on the absolute value of generated HD components [14].

The HD level is extracted using a large-signal characterization setup made of a Keysight N5173B signal generator associated to a Rohde & Schwarz BBA150 Broadband amplifier with GSG Infinity probes. A fundamental tone at f_0 = 0.9 GHz is injected at the input of the CPW. The 2nd harmonic power (HD2) is extracted at 1.8 GHz as a function of the input power and for different bias voltages ranging from -15 V to +15 V applied to the central conductor of the CPW lines. The chuck temperature is varied from 25°C to 175°C. The setup accuracy was estimated to be +/- 1 dB.

Fig. 2 displays the evolution of HD2, extracted at an input power of 15 dBm as a function of the applied bias on the CPW at room temperature. HD2 data are plotted for all samples and compared with the ones of HR and TR reference substrates.

The HR reference sample presents a typical HR-SOI profile [11, 15]. The HD2 level reaches -73 dBm at -15 V, decreases to -97 dBm at -1 V and increases up to -39 dBm at +15 V. The very low harmonic level of the HR substrate at -1 V can probably be explained by the low interfacial oxide charge density, i.e. the PSC is compensated with bias at -1 V and is weak even at 0 V.

The TR reference substrate presents a flat profile with HD2 values of -100 dBm (corresponding to the noise floor of our characterization setup). This is typically associated to a deep trap density higher than the DC bias induced density of substrate charges [14, 15]. The B0 sample presents a -84 dBm HD2 level which is stable with bias. This feature can be associated to the presence of traps [14] related to post-implantation defects. The B400 sample has a similar profile, with a higher absolute value of -78 dBm. This indicates that the substrate resistivity has likely partially decreased due to a dissolution of post-implantation defects during such an anneal, resulting in a slight HD2 increase. The B600 sample has a much lower HD2 level below -100 dBm.

Large trap densities are associated to the B0, B400 and B600 samples, since one can observe from the bias-independence of the HD2 curves that the interface Fermi level is tightly pinned in those substrates. It appears from absolute HD2 levels that E_{pin} is located deeper in the silicon bandgap for B600 than for B0 and B400 samples (E_{pinB0} being slightly deeper than $E_{pinB400}$). Due to anneals, defects density and morphology (observed by STEM, not showed here) evolve. So that there are less defects in B600 than in B400 and B0. However, those traps are located deeper in the bandgap. This remains compatible with $E_{pinB600}$ being deeper than E_{pinB0} or $E_{pinB400}$, although large amounts of traps are present. The position of E_{pin} is determined by the relative interplay of acceptor and donor traps distribution. This distribution may have been modified during anneals, resulting in a modification of the E_{pin} position, that would be situated at the deepest position for the B600 substrate, leading to the lowest HD2 values.

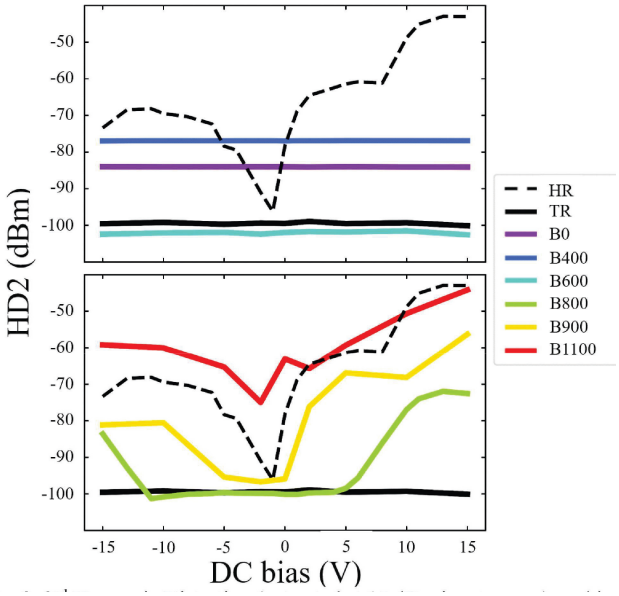

Fig. 2. 2nd Harmonic Distortion (extracted at 15 dBm input power) vs. bias voltage applied on CPW line for all samples.

The B800 sample presents a HD2 level of -101 dBm (noise floor) for biases between -11 V and +5 V, which increases up to -84 and -73 dBm for applied biases of -15 and +15 V, respectively. This indicates that the total traps density is reduced for this anneal compared to that of the B600 sample. Indeed, at high biases, free carriers are induced [14] to compensate the applied voltage, as evidenced by the increased

HD2 level. The trap density is even more reduced in the B900 sample. The latter presents a profile that resembles that of the HR sample [11], suggesting that there is no efficient carrier trapping. After a 1100°C annealing, the HD2 vs. bias profile presents a "V" shape with HD2 levels higher than -70 dBm for the whole bias range, i.e. with absolute performance levels close to that of the HR reference.

To conclude, the HD2 level obtained in the B600 substrate is very low, showing that the approach is promising. To further characterize this substrate, we measured the HD2 evolution vs. chuck temperature from 25°C up to 175°C.

The evolution with the chuck temperature of the HD2 level for the B600 sample is displayed in Fig. 3. The B600 sample presents a stable HD2 level below -90 dBm for chuck temperatures up to 100°C. Then, the HD2 level increases, reaching -75 dBm at 175°C. This behaviour is similar to the one generally observed in TR substrates, making our approach suitable for RF applications [15].

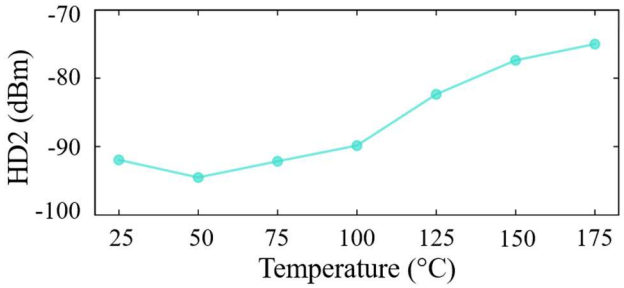

Fig. 3. 2nd Harmonic Distortion (extracted at 15 dBm input power) vs. substrate temperature for B600 sample.

IV. Small-Signal Characterization

The effective resistivity (ρ_{eff}) is a commonly used figure of merit to quantify substrate losses. It is computed from S-parameter data of CPW lines. Small-signal characterization was performed using a PNA-X Vector Network Analyzer with GSG Z-probes. Using two CPWs of different lengths, the access pad parasitic contributions can be removed using the Mangan model [16]. ρ_{eff} is extracted from de-embedded data using the method described in [17].

Fig. 4 displays the ρ_{eff} (extracted at frequencies between 5 GHz and 7 GHz, above the slow-wave mode transition [14]) as a function of DC bias applied to the signal line of CPWs.

The HR reference substrate reaches about 1 kΩ.cm at -15 V and +15 V and 2.2 kΩ.cm around the flatband voltage of -2 V. These ρ_{eff} values are atypically high for an un-passivated HR sample, and are probably due to low fixed charge densities Q_{ox} at the Si/SiO_2 interface. Typical HR samples usually present ρ_{eff} values in the range of 50 to 200 Ω.cm when typical Q_{ox} densities are present [4, 5, 7, 8, 9, 14, 15, 17]. Still, one can observe that the interface Fermi-level is not pinned, as evidenced by the bias dependency of the measured ρ_{eff}. HD2 results presented in Section III clearly revealed a lack of interface Fermi-level pinning, with very high HD2 values when a bias was applied.

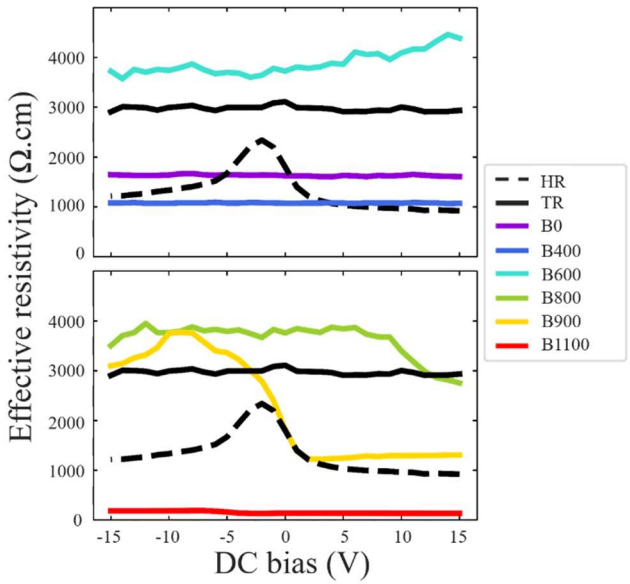

Fig. 4. Effective resistivity (extracted around 6 GHz) vs. bias applied to CPW.

The TR substrate shows effective Fermi-level pinning, demonstrated by the bias-independence of the ρ_{eff}-V_{DC} curve remaining flat at a value of 3 kΩ.cm. There is also Fermi-level pinning in B0 and B400 samples, with flat ρ_{eff} values at 1.7 kΩ.cm and 1 kΩ.cm respectively. The B600 annealed sample reaches a stable ρ_{eff} at a higher value of 4 kΩ.cm, supporting Section II claim of a deeper Fermi-level pinning in this sample. The flat ρ_{eff}-V_{DC} responses of the TR, B0, B400 and B600 samples are in good experimental agreement with their flat HD2-V_{DC} responses in showed Section III. The B800 annealed sample exhibits a stable 4 kΩ.cm value between -15 V and +8 V. The ρ_{eff} value drops above +8 V, reaching 2.6 kΩ.cm at +15 V. Similarly, B900 sample's ρ_{eff} varies between 4 kΩ.cm and 1 kΩ.cm as the bias changes. While ρ_{eff} remains high for B800 and B900 samples, variations with DC bias show that the Fermi-level becomes unpinned at high bias values (onset of trap-state saturation). Their traps densities are lower than that in samples annealed at lower temperatures. Once again, such ρ_{eff}-V_{DC} data are in good agreement with Section III HD2-V_{DC} data. After a 1100°C annealing, ρ_{eff} drops to 100 Ω.cm. Moreover, extracted ρ_{eff} are consistent with Fig. 2 HD2 levels.

V. Discussion

We suppose that RF performances obtained for substrates with cavities are probably associated with the dangling bonds at their internal surfaces. These dangling bonds probably act as a source of charge carrier traps, in a similar fashion to gettering [18-19]. The internal surfaces of cavities are indeed known to be particularly rich in dangling bonds compared to other ion implantation induced crystalline defects [19]. It is likely the main mechanism explaining the modification in traps density and hence RF performances such as HD2 and ρ_{eff}. The morphology of cavities is also known to have a high impact on the trapping efficiency of impurities [20]. Furthermore, another reason of the high RF performance obtained can be the crystalline defects created by the ions implantation, whose are known to be efficient for charge carriers trapping [21]. Thus,

used experimental conditions for He^+ implantation and subsequent anneals have a high impact on obtained RF performances.

Additionally, this method to locally fabricate interface passivation layers can be used at different steps of the integration process. Thus, it could be interesting to assess the thermal stability of the proposed solution at the typical BEOL and FEOL processing thermal budgets. As high RF performances were obtained using our process with thermal budgets of 600°C during 2 hours, the integration to FDSOI BEOL processing, with thermal budgets typically lower than 450°C during few hours, is expected to be supported. Otherwise, the FEOL thermal budget is much higher due to the need to activate dopants. It typically corresponds to spike annealing, which is done at temperatures higher than 1000°C during few seconds. To verify the stability of our process with such an anneal, we performed an He^+ implantation on an HR-Si substrate followed by a 1050°C spike annealing. Actually, stable HD2 and ρ_{eff} values of -85 dBm and 1.5 kΩ.cm, were respectively obtained. These FoMs make this approach suitable for integration during FEOL processing.

VI. Conclusion

In this paper, we assessed the RF performances of HR silicon substrates with buried cavities and defects formed using He^+ ion implantation followed by thermal annealing. This approach can be locally implemented on a wafer. It yields a promising second harmonic level below -100 dBm and high substrate effective resistivity of 4 kΩ.cm after a 600°C 2 h annealing, e.g. values very similar to (even slightly better) than that of our trap-rich reference substrate. Furthermore, RF performances are stable with the DC bias up to +/-15 V and substrate temperature up to 100°C, making this technique compliant with substrate performance requirements for RF applications. Lastly, we checked that this local RF passivation technique is compatible with both FEOL and BEOL thermal budgets. This promising approach enables the co-integration of local interface passivation layers with the FD-SOI technology.

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