A 1.88-NEF 3-kHz Current-Reuse Common-Gate Amplifier Featuring Resistorless High-Pass Filtering

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***Abstract*—Vagus nerve electroneurogram (VENG) signals have recently emerged as markers for the detection of epileptic seizures. However, these signals present a low amplitude and a large bandwidth, making them sensitive to the intrinsic noise of acquisition circuits and to interference from nearby muscles, which must be filtered out before amplification. To properly retrieve the useful signals, both the input filter and the instrumentation amplifier of the acquisition chain require an optimal noise-current trade-off. To tackle these issues, this work presents a common-gate current-reuse amplifier featuring resistorless high-pass filtering, prototyped on a 22-nm fully depleted silicon-on-insulator chip. The measured amplifier consumes 2.38 µA with a 1.7 μV_{RMS} input-referred noise, resulting in a noise efficiency factor (NEF) of 1.88 with a bandwidth from 300 Hz to 3 kHz.**

***Index Terms*—Noise efficiency factor (NEF), high-pass filtering, current reuse, low-power amplifier, biopotential acquisition.**

I. Introduction

Epilepsy is a condition that affects more than 50 million patients worldwide by causing frequent seizures. While drug-based treatments and surgeries exist, one third of the patients need to be treated with other methods such as vagus nerve stimulation (VNS). To avoid side effects of continuous VNS and to improve the patients' response, closed-loop VNS is nowadays under research for adapting the stimulation to the instantaneous physiological state of the patient, especially at seizure onsets. Epileptic seizures are commonly detected from the electroencephalogram but such techniques are subject to technology diversion [1]. Recently, the vagus nerve electroneurogram (VENG) has been shown to contain seizure markers through the identification of compound action potentials [2], offering a less invasive alternative. Fig. 1 shows an implantable system-on-chip (SoC) for VENG-based seizure detection, whose design faces several challenges. First, the SoC has to be supplied by an implantable battery lasting for several years, limiting the power budget to around 10 µW. Second, the analog front-end (AFE) adds noise on top of the low-amplitude (20 µV) useful signal. To keep the seizures detectable and to maintain a sufficiently high signal-to-noise ratio, the intrinsic noise of the AFE in the signal bandwidth (BW) should be kept below 2 μV_{RMS}. Finally, the VENG signal is also polluted by low-frequency interference from the heart and nearby muscles, whose amplitude is several orders of magnitude larger than that of the useful signal. The interference can be attenuated by tripolar sensing [3] but needs to be filtered before amplification to avoid saturating the low-noise amplifier (LNA). The input high-pass filter (HPF) and the LNA are thus bottlenecks for the low-power and low-noise operation of the system. Early designs of LNAs used conventional amplifier topologies with transistors biased in weak inversion [4], [5]. Nowadays, several publications show improvements in the noise-power trade-off of amplifiers, using the noise efficiency factor (NEF) as key performance metric, as discussed in [4]. Major architectural solutions include current-reuse (CR) topologies, amplifier stacking, and switched-capacitor (SC) circuits. CR consists in duplicating the input differential pair to halve the input-referred noise (IRN) power compared to topologies with a single differential pair [6]. In [7], multiple AC-coupled inverter-based CR amplifiers are stacked at the price of reduced output swing. Finally, an SC amplifier is proposed in [8] but suffers from disadvantages of discrete-time capacitor-based structures, including a large area and strict clock requirements. Besides, in any amplifier design, the noise from the HPF in front of the chain might significantly alter the following blocks. For instance, using 50-kΩ resistors in the HPF presented in [3] leads to an IRN of 0.71 μV_{RMS} for the HPF alone, representing 28% of the IRN power. In this work, we propose to broaden the scope of the noise-power trade-off of the LNA to include the contributions of the HPF. To that end, a common-gate (CG) amplifier featuring CR and intrinsic impedance for resistorless high-pass filtering is presented, and implemented on a chip in 22-nm fully depleted silicon-on-insulator (FD-SOI). Measurement results show that this combined filter and amplifier can reach an NEF of 1.88 for a 2.38 µA current, which is the best performance reported for VENG sensing. In this paper, Section II presents the CG topology and its optimization, while Section III discusses the measured performance of the prototype chip.

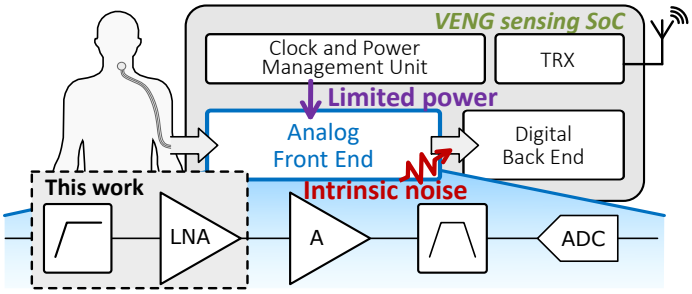

Fig. 1. VENG acquisition system-on-chip with an emphasis on the components of the analog front-end and the blocks considered in this work.

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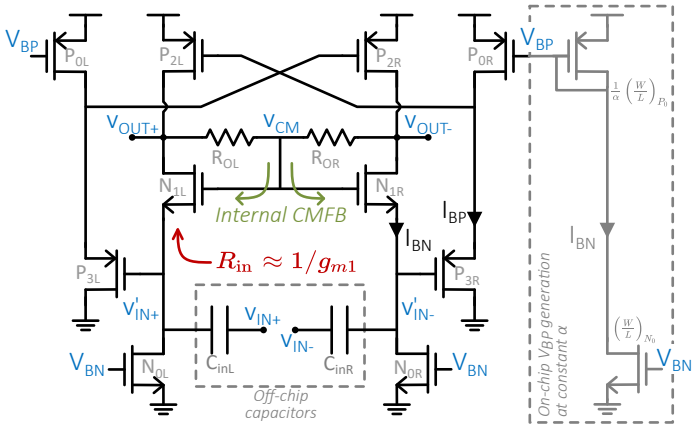

Fig. 2. Schematic of the proposed common-gate amplifier. Biasing circuit shown in grey for V_{BP} generation with constant current ratio $\alpha = I_{\mathrm{BP}}/I_{\mathrm{BN}}$.

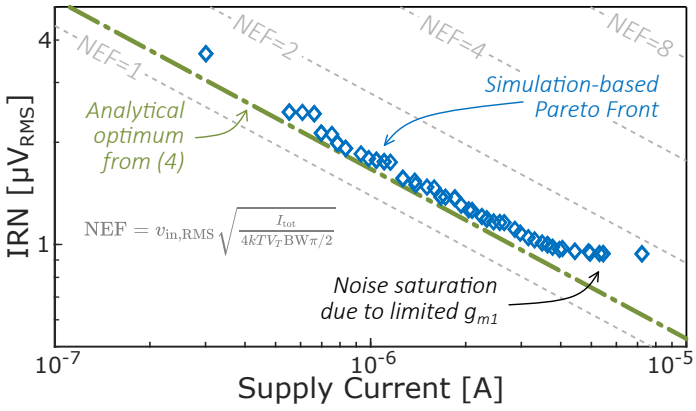

Fig. 3. Analytical (green) and simulation-based (blue) optimization results (input-referred noise in the $\pi/2$-bandwidth as a function of total supply current), with iso-NEF curves indicated in grey dashed lines.

II. Common-Gate Amplifier Design

This section first presents the working principle and analytical modeling of the proposed architecture. Then, analytical and simulation-based optimizations are performed to reach the optimal noise-power trade-off of the whole circuit.

A. Architecture Description

The proposed amplifier is depicted in Fig. 2. $\mathrm{N_{1L}}$ and $\mathrm{N_{1R}}$ form a CG differential pair. The input signal is buffered through $\mathrm{P_3}$ transistors and replicated at the gates of the common-source pair $\mathrm{P_2}$. Output resistors $\mathrm{R_O}$, implemented with high-density polysilicon resistors, set the gain and upper BW limit and improve the linearity of the amplifier. Those also sense the common-mode output voltage, which is then applied on the gates of the CG pair to provide an internal common-mode feedback (CMFB). The body of the NMOS (resp. PMOS) devices is connected to ground (resp. $\mathrm{V_{DD}}$). The input high-pass filter consists of the input impedance of the circuit and off-chip capacitors in the nF range. The use of off-chip components is not critical regarding the total volume as the targeted application employs other external components such as cuff electrodes and a battery. In these conditions, the in-band gain of the amplifier is given by

$$A_{v0} = \frac{g_{m1}+g_{m2}}{g_{d1}+g_{d2}+1/R_O} \approx R_O\left(\left(\frac{g_m}{I_D}\right)_1 + \left(\frac{g_m}{I_D}\right)_2\right) I_{\mathrm{BN}}, \tag{1}$$

where I_{BN} is the bias current in the $\mathrm{N_1}$-$\mathrm{P_2}$ branch, controlled by the bias voltage V_{BN}. The proposed approximation holds with $\mathrm{R_O}$ in the MΩ range. Then, the lower and upper BW limits are respectively given by

$$f_{\mathrm{low}} \approx \frac{(g_m/I_D)_1}{2\pi C_{\mathrm{in}}} I_{\mathrm{BN}}, \qquad f_{\mathrm{high}} \approx \frac{1}{2\pi R_O C_L}, \tag{2}$$

where C_L is the load capacitance. The thermal noise power spectral density (PSD) from MOS transistors is modeled as

$$S_{i_d} = 4kT\gamma g_m, \tag{3}$$

where k is the Boltzmann constant, T is the absolute temperature (body temperature), and γ is a bias-dependent parameter obtained from simulations of a single transistor. The total thermal IRN PSD can then be expressed as

$$S_{\mathrm{in}} = \frac{8kT/I_{\mathrm{BN}}}{\left(\left(\frac{g_m}{I_D}\right)_1 + \left(\frac{g_m}{I_D}\right)_2\right)^2}\left[\gamma_1\left(\frac{g_m}{I_D}\right)_1 + \gamma_2\left(\frac{g_m}{I_D}\right)_2 + \left(\frac{(g_m/I_D)_2}{(g_m/I_D)_3}\right)^2\left(\gamma_0\left(\frac{g_m}{I_D}\right)_0 + \gamma_3\left(\frac{g_m}{I_D}\right)_3\right)\frac{I_{\mathrm{BN}}}{I_{\mathrm{BP}}}\right], \tag{4}$$

where I_{BP} is the bias current in the $\mathrm{P_0}$-$\mathrm{P_3}$ branch. We neglect the noise from $\mathrm{R_O}$ due to the large resistance value. As shown in (4), CR allows to sum the transconductances of both differential pairs to strongly decrease the IRN. The flicker noise is minimized thanks to large gate areas.

B. Circuit Design and Sizing

The IRN is modeled in (4), highlighting its dependence on the bias currents and the levels of inversion of the transistors through their g_m/I_D ratios. An analytical optimization can be made from (4) to minimize the noise by choosing optimal g_m/I_D ratios and currents. Regarding the g_m/I_D ratios, $\mathrm{N_1}$ and $\mathrm{P_3}$ must be biased in weak inversion and $\mathrm{P_0}$ is optimally set in strong inversion. While the choice of $(g_m/I_D)_2$ is less obvious, the optimum is to keep it in strong inversion to minimize the noise from the secondary branch containing $\mathrm{P_0}$ and $\mathrm{P_3}$. The optimal current ratio is given by

$$\alpha = \left(\frac{I_{\mathrm{BP}}}{I_{\mathrm{BN}}}\right)_{\mathrm{opt}} = \frac{\left(\frac{g_m}{I_D}\right)_2}{\left(\frac{g_m}{I_D}\right)_3}\sqrt{\frac{\gamma_0\left(\frac{g_m}{I_D}\right)_0 + \gamma_3\left(\frac{g_m}{I_D}\right)_3}{\gamma_1\left(\frac{g_m}{I_D}\right)_1 + \gamma_2\left(\frac{g_m}{I_D}\right)_2}}, \tag{5}$$

which is close to 0.1 in the bias conditions stated above. The values for the γ coefficients and the minimum/maximum g_m/I_D values were extracted from simulations of I/O MOSFETs in 22-nm FD-SOI and injected into the analytical noise model, as described in [9]. The resulting theoretical minimum NEF is 1.20.

The sizing of the devices is performed by a genetic optimization algorithm based on simulations as in [10]. In

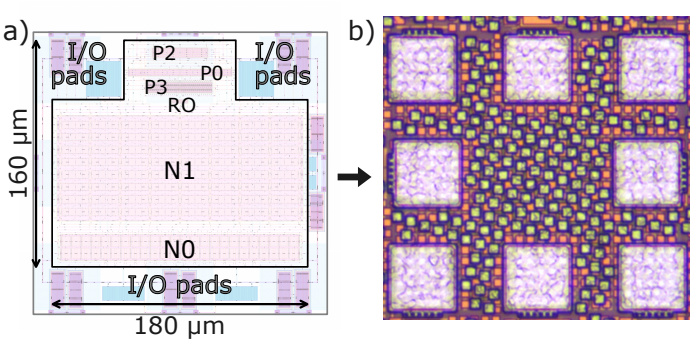

Fig. 4. Amplifier layout (a) and microphotograph of the amplifier on the prototype chip (b). Pads are included for stand-alone circuit measurements.

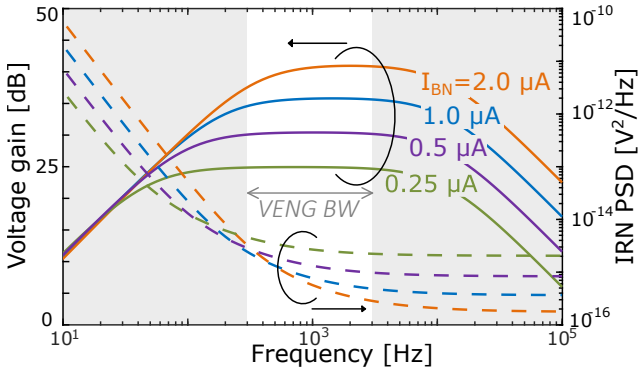

Fig. 5. Post-layout frequency-dependent results from a sweep on I_{BN} with constant $I_{\mathrm{BP}}/I_{\mathrm{BN}}$. The bias current tuning allows to set the high-pass filter pole and the gain value (left), as well as the thermal noise PSD level (right).

addition to minimizing the IRN and the current consumption, the algorithm also constrains the voltage gain to be higher than 35 V/V, f_{low} below 300 Hz with C_{in} = 30 nF, and f_{high} above 3 kHz with a 10-pF load. With these BW specifications, the useful signal can be recovered for seizure detection [11]. The optimization results are presented in Fig. 3, showing good agreement between the analytical developments and the simulation-based optimization. At high currents, the simulation-based results saturate at a constant noise value. This is due to the constraint on f_{low}, which imposes a maximum g_{m1}. Thus, at constant levels of inversion, the total supply current is limited to 3.9 µA. For individuals in the Pareto front exceeding that current limit, N_1 pulls away from weak inversion, increasing the NEF. As a result, the IRN cannot be pushed lower than 0.85 $\mu\mathrm{V}_{\mathrm{RMS}}$. Flicker noise is also relatively more significant in the high-current individuals, as that type of noise is not reduced by an increase in the supply current.

After the optimization process and a sensitivity analysis, a design sizing was selected for implementation in layout, as shown in Fig. 4(a). The transistor sizes are summarized in Table I. The post-layout performance indicates an NEF of 1.63, higher than the theoretical minimum due to the parasitic resistances in the layout and to a reduction in the device dimensions to fit in a limited area. Thanks to the simplicity of the topology and the straightforward control via V_{BN}, the noise and current performance can be adapted following an iso-NEF curve. Fig. 5 shows the adaptation of the gain and

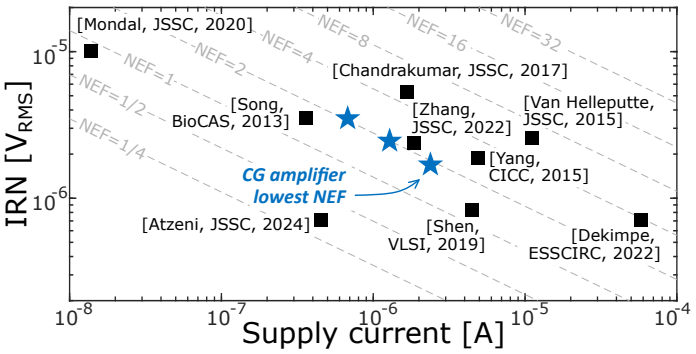

Fig. 6. Measured noise - current trade-off of the CG amplifier for three different operating conditions (blue stars) and state-of-the-art reference designs (black squares). All noise results were rescaled to a [0.3 - 3] kHz bandwidth.

noise performance in post-layout simulations by a sweep on the bias current I_{BN}, with a constant ratio $I_{\mathrm{BP}}/I_{\mathrm{BN}}$. First, it can be seen that the thermal noise PSD level decreases as the bias currents increase, as expected from Fig. 3. Second, the lower BW limit f_{low} increases with I_{BN}, as expressed in (2). Finally, the in-band gain given by (1) is also proportional to the bias current. These variations hold at constant device dimensions given that, in weak inversion, a small variation in the drain current at constant dimensions only has a negligible impact on the g_m/I_D ratio of the transistor [12]. The in-band gain and the upper BW limit can similarly be adapted with variations in the value of resistors R_{O}.

TABLE I
TRANSISTOR SIZES

Device	N_0	N_1	P_0	P_2	P_3
W/L [µm]	112/6.0	640/4.5	1.0/8.0	2.0/16	150/0.15

III. Measurement Results

The proposed topology was prototyped as a stand-alone block on a chip in 22-nm FD-SOI from GlobalFoundries. The microphotograph of the amplifier on the die is shown in Fig. 4(b). The amplifier occupies an area of 0.030 mm^2. Transistors N_1, biased in very weak inversion, are the largest components, taking 63% of the total area.

As explained in Section II-B, V_{BN} is swept to change the operating point with almost constant NEF. Fig. 6 shows three measurement results for our design, with additional references. The lowest NEF measured is 1.88 with a total supply current of 2.38 µA. The differences with the simulated NEF of 1.63 are due to parasitic resistances on the test board, process variations, as well as non-ideal supply and measurement equipment. Fig. 7 presents the frequency response and the IRN PSD for this lowest-NEF operating point. Table II presents a detailed comparison of the proposed CG amplifier with several low-NEF designs. Up to the authors' best knowledge, [3] is the only previous publication presenting an AFE for VENG sensing, and [8] reports the lowest NEF ever achieved for a low-power amplifier. Table II shows that, beyond the competitive noise performance of the CG amplifier, the proposed topology also reaches good performance in terms of harmonic distortion,

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART OF BIOMEDICAL AMPLIFIERS

	This work	Atzeni [8]	Dekimpe [3]	Mondal [7]	Shen [13]	Song [6]
Application	**VENG**	-	**VENG**	ECG	-	EEG
Technology	22 nm	22 nm	22 nm	0.18 µm	0.18 µm	0.18 µm
Area [mm^2]	**0.03**	0.21	**0.03**	0.24	0.14	0.16
Supply [V]	1.8	Dual	1.8	1.35	0.6	1.2
Power [µW]	4.29	0.37	104	**0.0187**	2.7	0.43
Gain [dB]	35.8	26-85	91.5	36	46	26
BW [kHz]	[0.3-3.0]	10	[0.5-16]	0.24	8	[0.08-15]
IRN [µV$_{RMS}$]	1.70	1.36	1.4	-	1.4	8.1
NEF	1.88	**0.34**	3.87	0.86	1.26	1.52
Z_{in} [MΩ]	0.028	389	-	93	-	-
THD [%]	0.13 (1 mV$_{PP}$)	0.2 (10 mV$_{PP}$)	-	0.16 (75% out)	0.4 (3 mV)	0.05 (10 mV$_{PP}$)
CMRR [dB]	>60 (in BW)	70	-	>95 (in BW)	84	>60
PSRR [dB]	>81 (in BW)	78	-	>68 (in BW)	78	>80
Output swing [V]	1.21 (-3 dB)	-	-	-	-	-
Techniques	**CG**, CR	SC	Cascode	Stacking, chopping	Stacking, chopping	CR, cascode
Considered blocks	**HPF**+LNA	AFE	AFE	AC-coupled LNA	3-stage LNA	Closed-loop LNA
Required clock(s)	**None**	Multiple	32 kHz	1.5 kHz	10 kHz	**None**

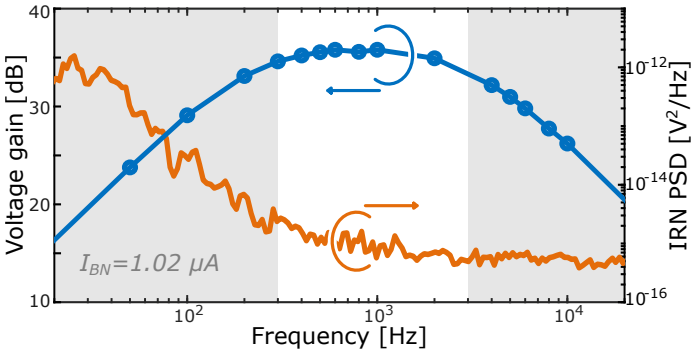

Fig. 7. Measured frequency response and input-referred noise PSD for a total current consumption of 2.38 µA.

common mode and power supply rejection, and output swing. To accurately reject interference, it is necessary to control the input impedance, which is lower in this topology than in many other amplifiers. Other works that implement chopping [13] or a resistor-based HPF [3] also present a low input impedance. The need for a high input impedance must be assessed based on the electrode impedance value. The large output impedance of this CG LNA is not an issue if the subsequent circuit in the AFE has a common-source input with a large input impedance.

IV. CONCLUSION

The combined high-pass filter and amplifier proposed in this work provides a solution for resistorless high-pass filtering and low-NEF amplification thanks to a common-gate input and current reuse. The measurement results on the prototype chip in 22-nm FD-SOI show a current consumption of 2.38 µA for an IRN of 1.7 µV$_{RMS}$, giving an NEF of 1.88. Besides, a gain of 35.8 dB is attained in the 0.3-3 kHz bandwidth. Finally, we demonstrate that the filter cut-off frequency, the gain and the noise-current trade-off can be calibrated thanks to the adaptation of the bias current.

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