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Towards Porous Si THz Planar Waveguides in Ultra-Low-Resistivity Substrates

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***Abstract*— This paper presents an innovative approach to integrate a high-quality porous silicon (PSi) waveguide on ultra-low-resistivity (ULR) substrates for terahertz (THz) applications. Eliminating the need for deep etching and multiple wafer bonding, the proposed technique leverages the low resistivity of ULR substrate and the high resistivity of PSi to create an efficient waveguide. Simulations and preliminary experiments validate the concept.**

Keywords—waveguide (WG), effective dielectric permittivity, effective resistivity, microwave losses, porous silicon (PSi), ultra-low-resistivity (ULR) substrate, trap-rich (TR), high-resistivity (HR) silicon, THz waveguide

I. INTRODUCTION

Nowadays, the THz frequency range (0.1-10 THz) is the focus of intense investigation for communication, sensing, spectroscopy and imaging. Indeed, going to THz provides huge benefits in terms of bandwidth, data rate, and resolution and opens door to new applications [1]. However, the large-scale deployment of THz systems is currently hindered by current limitations of packaging and semiconductor technologies.

Traditional packaging approaches for THz devices rely on split-block systems and WG made by bulk metal machining [2][3]. This ensures a proper quality of interconnection between devices, and provides the required mechanical stability. It also features very low loss. However, using machined WG at THz frequencies also has severe limitation in terms of bulkiness and cost. At those frequencies, WG losses become also more sensitive to the CNC machining tolerance and achieved, surface roughness. While the number of THz devices and application fields are growing, their integration into compact systems therefore remains a challenge. In terms of semiconductors, advanced CMOS platforms (22FDx [4]) now offer transit frequencies and maximum oscillation frequencies in the range of 400 GHz and are promising contenders for the development of highly integrated, low cost systems in the low THz range. However, as CMOS nodes have scaled down, the cross dimensions of their metal stacks also have shrunk vertically. As explained in [5] a clear trend of increased transmission lines (TL) losses can be observed at those nodes, which is further exacerbated at THz frequencies due to the skin effect.

To improve the integration of THz systems while reducing TL losses, researchers are currently investigating the integration of waveguides (WG) on silicon. Two main categories of Si-integrated WGs have been demonstrated, i.e. air-filled WG [6] and Si-filled WG [7][8]. For a given frequency band, the air-filled WG exhibits lower losses but the Si-filled WG features considerably smaller dimensions thanks to the high permittivity of silicon and is therefore the focus of this paper.

Typically, the Si-filled WG fabrication process deploys deep reactive ion etching (DRIE) of a high resistivity silicon wafer and bonding. However, DRIE is a slow process and is highly pattern-dependent, necessitating meticulous optimization of the recipe to attain vertical sidewalls. The overall etching process is therefore intricate and comes with a substantial cost. In an alternative perspective, porous silicon (PSi) has stood out as a promising choice for radio frequency (RF) substrates [9]. The creation of PSi involves the electrochemical anodization of bulk silicon [10], resulting in numerous favourable characteristics such as high resistivity, low permittivity, low losses, low crosstalk levels, and strong linearity. In most cases, PSi is therefore predominantly employed as a substrate to realize high-quality planar transmission lines and passive devices on silicon.

In this paper, we introduce an innovative technique for integrating a waveguide within a silicon wafer, using high-quality high-resistivity (HR) porous silicon (PSi) on an ultra-low-resistivity (ULR) substrate. The WG is fabricated using a process that eliminates the need for (1) time-consuming deep etching of the silicon wafer; (2) multiple wafers and bonding between them. In Section II, we describe the concept and advantages of the new PSi WG fabrication approach, along with simulated performance of a H-band Psi WG. In Section III, we present the fabrication methodology and introduce preliminary experimental characterization data of the PSi substrate, which are required for proper WG performance modelling. In Section IV, a brief conclusion is given.

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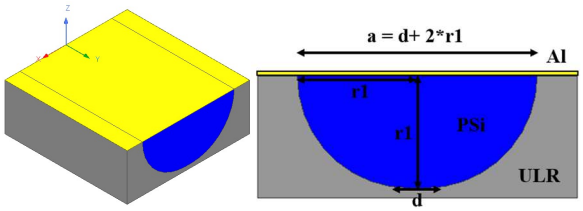
II. Concept of PSi WG in ULR Substrate

The newly proposed integrated WG concept is illustrated in Fig. 1. The integrated WG is filled with HR PSi, embedded in a ULR (ρ_{Si}~0.5 mΩ·cm) substrate and its top surface is covered by a metal layer. In this concept, the substrate is akin to the 'metal' component of traditional WG owing to its very low value of resistivity. The porous area, characterized by a resistivity (ρ_{PSi}) on the order of a few kΩ·cm or higher, aligns with the 'silicon core' concept as proposed in [5][7][8]. The proposed concept offers flexibility in terms of achievable cross-section geometry, enabling the fabrication of waveguides with various dimensions and shapes. The shape can be optimized to some extent for a given application. The waveguide is "embedded" at the top of the substrate, ensuring that the top surface remains flat. This characteristic facilitates subsequent wafer processing for the integration of active circuits onto a planar substrate. Consequently, a complete THz system, comprising both active circuits and waveguide-based passive circuits, can be more readily fabricated compared to conventional silicon-integrated waveguide fabrication techniques.



(a) (b)

Fig. 1. (a) 3D view of the proposed PSi WG in ULR substrate (b) cross-section shape variation.

The PSi WG embedded on an ULR substrate shown in Fig. 1 is modelled and simulated using the HFSS software, for a constant length of 1 mm, surface roughness of 200 nm, and a constant width 'a' of 600 µm (for a targeted H-band operation). The effective permittivity values for the ULR substrate and PSi area are 11.7 and 3, respectively.

Fig. 2a reports the impact of the WG height (r1) on the WG losses across the entire H band. For those simulations, nominal ρ_{Si} and ρ_{PSi} values of 0.6 mΩ·cm and 10 kΩ·cm were chosen, respectively. r1 is seen to slightly impact the WG cut-off frequency as it affects the rounding of the WG lower corner due to the fabrication process (Section III). Fig. 2a also shows that as the height is reduced (and so is the corner rounding) the WG losses are increased which we attribute to higher current densities in those regions.

Fig. 2b shows the losses at the higher H band edge (i.e., 325 GHz) as a function of ρ_{PSi} and for varying values of ρ_{Si}. Both parameters affect the losses as a lower ρ_{PSi} means higher conduction within the WG core (core losses) and a higher ρ_{Si} means higher field densities (and hence currents) inside the ULR substrate (substrate losses). For a given ρ_{Si} value the figure shows that losses reach a plateau level where they become dominated by substrate losses. The plateau value therefore depends solely on ρ_{Si} and increases (ie, total losses are reduced) for lower ρ_{Si} values.

The figure shows that for a nominal ρ_{Si} value of 0.6 mΩ·cm and a PSi resistivity higher than a few kΩ·cm, the proposed device exhibits insertion losses close to its optimum value (~0.47 dB/mm), which is close to the value of 0.43 dB/mm as reported in [8] for conventional Si-filled WG at a similar frequency.

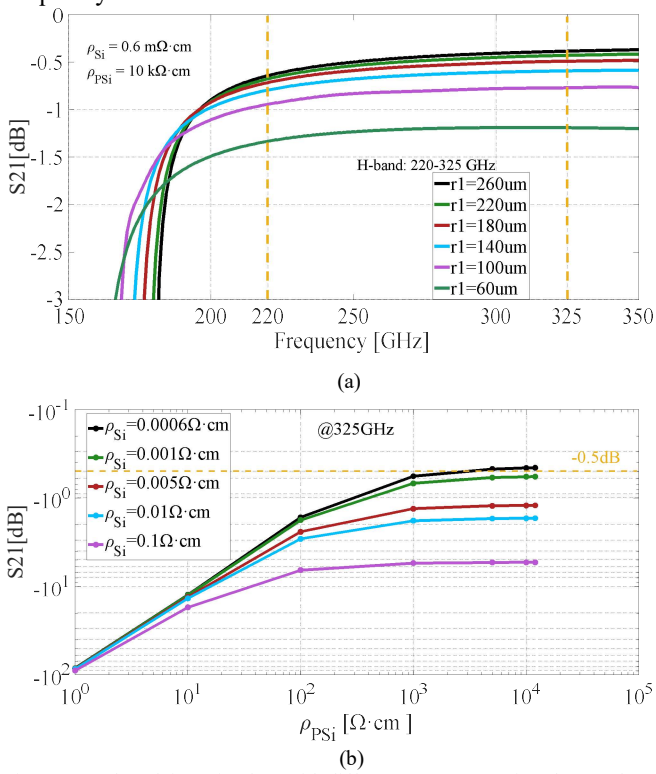


Fig. 2. 1 mm length insertion loss with different (a) cross-section shapes, (b) resistivity sweep at 325 GHz.

III. Substrate Fabrication and Description

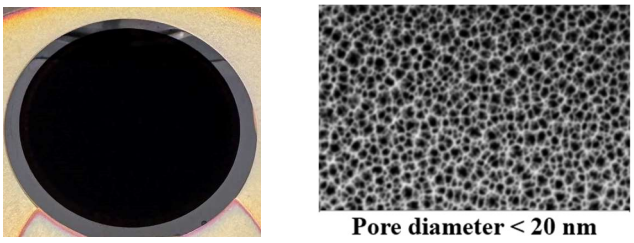
As explained in the previous section the performance of the proposed WG largely depends on the electrical characteristics of the achieved PSi. In this section we perform an extensive characterization of the PSi layer built with a dedicated porosification process and using coplanar waveguides (CPW).

A. PSi substrate fabrication

A 380 µm-thick heavily doped p-type silicon 3-inch wafer from SIL'TRONIX with a resistivity ranging from 0.6 to 0.8 mΩ·cm, serves as the initial substrate . Prior to processing, the wafer undergoes a cleaning procedure using nitrogen gas flow, and a thin layer of sacrificial material is removed. Similar to [10], PSi is then prepared through anodization in a solution with a 3:1 volume ratio of HF (49%): ethanol. The etch cell has a radius of 3 cm, and the growth of porous silicon is isotropic.

The applied total current is adjusted to maintain an etching current density of approximately 20 mA/cm². Each etching cycle consists of 10s of etching followed by a 2s pause, allowing the recovery of HF concentration. After 700 cycles, the estimated depth of the porous region exceeds 80 µm. The fabricated sample is shown in Fig. 3a, the average

pore diameter is measured to be below 20 nm under Scanning Electron Microscope (SEM).



(a) (b)

Fig. 3. (a) PSi area on ULR substrate, (b) surface pore morphological using SEM.

B. CPW sets to characterize the substrate

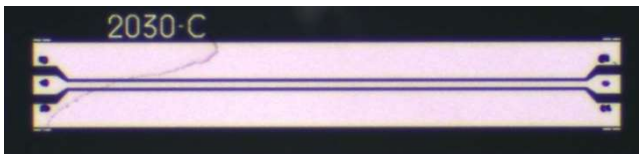
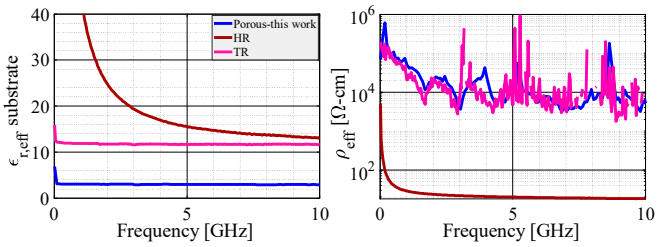


Fig. 4. CPW lines for proposed PSi characterization (signal width, ground spacing and ground width of 26, 40 and 155 µm respectively).

A 500 nm-thick silicon oxide (SiO2) layer is then deposited on top of the porousified area to safeguard the fragile PSi region. This deposition occurs at 250°C using plasma-enhanced chemical vapor deposition (PECVD). Subsequently, a 1 µm-thick layer of aluminium is deposited via physical vapor deposition (PVD) to define CPW lines with signal width, ground spacing and ground width of 26, 40 and 155 µm respectively (in Fig. 4). Identical CPW lines are also built on HR (>3 kΩ·cm) and Trap-Rich (TR, >3 kΩ·cm) substrates in our lab for further benchmarking.

C. Small signal characterization

On-wafer small signal measurements of the CPW lines up to 10 GHz were conducted utilizing an Agilent 2-port performance network analyzer (PNA)-X vector network analyzer, along with a pair of ground-signal-ground (GSG) |Z| probes from Cascade Microtech. From the measured S parameters, the effective permittivity and effective resistivity [11] of the proposed PSi substrate are extracted up to 10 GHz using an mTRL-based calibration method [12]. The data are presented in Fig. 5a and b, respectively, where they are also compared with the results obtained on the HR and TR Si substrates. The HR and TR show an effective permittivity around 11, while the PSi shows a low value of around 2.9 as it is partially filled with air. The effective resistivity (Fig. 5b) of the HR is only of 30 Ω·cm at 10 GHz because parasitic surface conduction effects increase substrate losses [11]. The TR substrate shows a value of 8 kΩ·cm at 10 GHz as the 300 nm thin layer of polysilicon between the SiO_2 and silicon bulk is able to trap the electrons attracted near the substrate surface by the fixed positive oxide charges. The PSi shows almost the same effective resistivity as the TR substrate due to its high density of traps [10]. Those results, coupled with the simulation data provided in Section II, indicate that THz WG with acceptable loss levels can be obtained using a simple porosification of an ULR Si substrate.



(a) (b)

Fig. 5. Effective electrical substrate parameters extracted from wideband S-parameter measurements of RF CPW lines (a) permittivity, (b) resistivity.

IV. Conlucion

In this paper, a novel concept of a PSi WG in a ULR substrate has been proposed, based on a fabrication process that is simplified compared to standard DRIE-and-bonding-based WG integration techniques. Its working principle, advantages and future applications have been discussed in details. We modelled the PSi WG in HFSS and studied the influence of cross-section shape, PSi resistivity and resistivity of the ULR substrate on the novel WG insertion loss. Preliminary fabrication and characterization of the PSi layer has been done. An extremely high value of PSi resistivity (~11 kΩ·cm at 10 GHz) has been extracted. The results prove the feasibility of the proposed concept and indicate that it should lead to WG with performances comparable to those obtained using conventional integration techniques, thereby presenting itself as a promising solution for the integration of THz WG on silicon.

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