Development of High Resistivity FD-SOI Substrates For mmWave Applications

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FD-SOI CMOS technology is entering the mmWave realm, providing undeniable benefits in terms of data-rates, bandwidth, latency and power consumption improvements. The high resistivity substrate option is seen as a major booster to reach ultimate mmWave performances. The engineering challenges related to this new wafer generation are addressed in this paper. We will review benefits and drawbacks of each possible high resistivity material, and discuss process options to enhance performances on resistivity stability and mechanical robustness to deformation through fabrication processes. Specific measurements are presented to show that going from standard to high resistivity substrates did not impact the behaviour of logic devices. Those substrates being destined to RF and mmWave applications, their performance was also measured in terms of small signal response using coplanar waveguides.

Introduction, Context and Targeted Application

The mmWave era opens up the door to revolutionary applications in the fields of communication, radar, imager, security, etc. FD-SOI CMOS technology is entering the mmW realm as a versatile and flexible solution. The technology provides the benefits in terms of data-rates, bandwidth, latency and power consumption required by high growth markets such as mobile & infrastructure for 5G mm-Wave implementations, consumer & industrial edge devices for AI & ML and consumer wearables for ultra-low power connectivity capabilities and automotive ADAS applications. However, future RF markets will impose new levels of performance for both RF and logic devices. To fulfil all the requirements, additional improvements at substrate level are mandatory. The high resistivity option on FD-SOI is seen as a major booster to reach ultimate mmW performance, enabling a higher level of SoC integration with unrivalled PA, LNA, ADC/DAC or Switch characteristics.

High Resistivity FD-SOI substrate design will share the same SOI and BOX layer attributes with respect to standard FD-SOI: ultra-thin (~10 nm), highly uniform (±5 Å, all points, all wafers) and very low roughness (<1 Å RMS) top Silicon, ultra-thin buried oxide (15-30 nm) with back-biasing capability. The handle wafer resistivity will be raised from standard 10-15 Ω.cm to a wide range of HR specification (from 250 to 10000 Ω.cm)

to assess material robustness to FD-SOI process, design constraint and performance. The engineering challenges related to this new wafer generation are discussed in this paper.

Experimental Preliminary Results on Standard HR Materials

Different options exist for high resistivity (HR) silicon handle substrates, mainly driven by oxygen content. Indeed, oxygen inside silicon is known to generate thermal donors at quite low temperature range, between 375 to 500°C approximately, maximum generation rate being estimated at 450°C (1). Those thermal donors will affect resistivity stability, especially at typical back end of line passivation anneals, close to this temperature range.

In this work, we will present resistivity profiling in depth measured with SRP (Spreading Resistance Profile), on final SOI samples with different material options, the SRP profiles can be either before or after an additional thermal budget generating oxygen thermal donors. This thermal budget will be described as a DGA for Donor Generation Anneal, and is chosen to be at 450°C during 1 hour, which would be the worst scenario, as 450°C is the temperature with the maximum thermal donor generation rate. We also tried to simulate a softer test, assumed to be closer to real devices maker's back end of line conditions. This test will be referenced as soft-DGA, it is made at 425°C during 30 minutes, and is roughly equivalent to 400°C 1h. Some SRP profiles will also be presented with this soft-DGA test, to illustrate the potential for each material on resistivity stability with a more realistic case compared to 450°C DGA.

The overall process used to fabricate FD-SOI wafers is quite extensive in terms of substrate mechanical robustness, as it implies several anneals at high temperature, and specifically one very high temperature anneal, above 1100°C, for several hours, to get very thin and homogeneous FD-SOI layers. We will need to make a specific focus on slip-line generations at the end of the SOI process, pending material options. This slip-line impact will be characterised by defectivity in-line inspections, such as KLA-Tencor Surfscan SP5 tools on unpatterned wafers, and we will show some defect maps obtained from different materials.

We can distinguish two most widespread families for HR substrates. All oxygen concentration [Oi] will be reported in old ppma (ASTM79) in this work.

Low Oi Substrates

The first option is low Oi material, containing [Oi] below 12 old ppma approximately. The main advantage of this kind of material will be the stability of the resistivity, due to the low interstitial oxygen amount, leading to low thermal donor generation rate. We will then reach a very good resistivity predictability and stability, at a resistivity range from several hundreds to several kΩ.cm. Figure 1 below represents the SRP profiling in depth on a final SOI wafer, before and after the DGA tests, and shows the good stability of low Oi substrates towards thermal donor generation for a 2000 Ω.cm substrate.

The main drawback for this material range will be the mechanical robustness to harsh thermal treatments, and the impact on slip-line generation. The lower the [Oi] is, the

higher the slip-line rate will be. For oxygen content being below 12 old ppma, the slip-line amount can be really huge with our typical thermal budget needed to produce appropriate FD-SOI substrates. An example of defectivity maps is shown in figure 2 below, showing both slip-lines at the edges of the wafers and also pin-marks, generated at boat or pins contacts during anneals. Hence, the low Oi material robustness to plastic deformation is not appropriate to produce that kind of HR FD-SOI substrates.

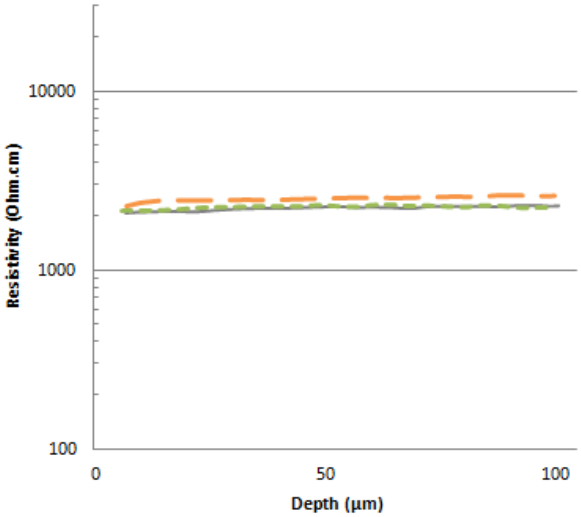


Figure 1. SRP profiles at final SOI, for 7-8 old ppma material initially around 2000 Ω.cm. Plain line is final SOI, short-dash line is final SOI and soft-DGA, long-dash line is final SOI and DGA.

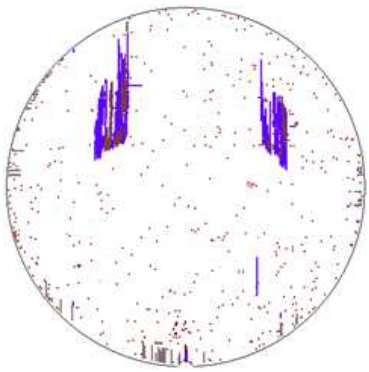


Figure 2. Final SOI defectivity SP5 maps in oblique mode, on 23 wafers stacked for Low Oi material around 7-8 old ppma.

High Oi Substrates

The second option is high Oi material, containing [Oi] between 26 to 32 old ppma approximately. That kind of substrate will need a good oxygen precipitation level to reach acceptable resistivity stability. Indeed, if all oxygen content in HighOi material is left at interstitial stage, the amount of thermal donors generated at back end of line will exceed the amount of initial P-type doping left inside the material, even for substrates with resistivity range around 500 - 1000 Ω.cm. The way to guarantee acceptable

resistivity is to perform adequate thermal treatment to create Bulk Micro Defects (BMD) by oxygen precipitation.

The precipitation will appear in 2 phases (2), a nucleation that will create small SiO_x precipitates acting as embryos that will aggregate more oxygen, and a growth leading to bigger precipitates that will be more stable and won't be dissolved after subsequent annealings.

The nucleation can be homogeneous (some interstitial oxygen atoms close enough to nucleate, without other defects assistance) or heterogeneous (based on material point defects, such as vacancies for example), and generally will appear in the range of 650°C to 900°C. We generally apply a nucleation at 650°C and 800°C during 2 to 4 hours.

The growth is realised at 1000°C for several hours, at least long enough to decrease residual interstitial oxygen left inside the material roughly below 14-15 old ppma. The BMD size after full thermal anneal is found to be greater than 70nm, and the density will be above 1e10 def/cm3.

The resistivity stability is globally ensured such that high Oi material will remain in the high resistivity range. But depending on initial point defects concentration which can vary with pulling conditions, [Oi] range, and initial resistivity (or P-type doping quantity), the resistivity range at final SOI and thermal donors generation tests, can be wide, from several hundreds, to 10.000 Ω.cm. Then a precise resistivity range can be difficult to contain.

The BMD created will bring a good robustness to slip-lines, as they will act as traps to slip-lines propagation, thus decreasing the amount of emerging slip-lines and defectivity. But BMD themselves can generate local strain in the material, the BMD growth leads to dislocations generation that can move after subsequent annealing (3), leading to wafer warpage and potential overlay issues at devices makers' line. Based on literature and internal tests summarised in part 5 of this work, the harmful BMD density to overlay is estimated to be above 1e10 def/cm3, and the beneficial BMD density to block slip-lines propagation is estimated at minimum 1e9 def/cm3, with a good centre to edge uniformity, to get rid of fragile area in the wafer.

Last but not least, will be the high Oi material pulling, that generates a lot of Crystal Originated Particles (COPs) inside the handle wafer. Those COPs will induce wafers inspectability issues, as the SOI and buried oxide layers are thin, the defectivity metrologies are impacted by those handle defects. In addition, those COPs make co-integration in the base wafer impossible due to the amount of defects visible in the map shown in figure 3.

Considering overlay potential risk and COPs inspectability and co-integration limitations, it is barely possible to use that high Oi material to process HR FD-SOI wafers. For the targeted technologies with FD-SOI, equal or below 28 nm, those handle properties will be even more critical than usual.

Then, none of the conventional high resistivity materials are compatible with FD-SOI process and customers requirements.

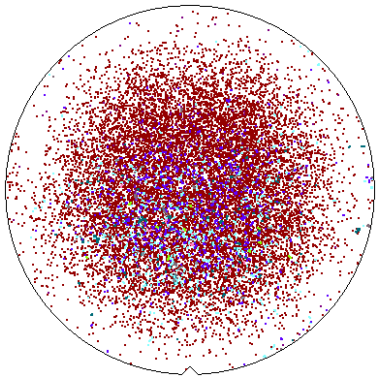


Figure 3. Final SOI defectivity SP5 maps in oblique mode, on 22 wafers stacked for High Oi material at 30 old ppma - defectivity maps show impact of COPs central pattern.

Experimental Procedure and Results on New Substrates

It is generally difficult to work with middle [Oi] materials, between 15 to 25 old ppma, to get good resistivity stability. Indeed, precipitation rate is globally worse than high Oi material as the oxygen level is lower, and then thermal donors can severely affect resistivity as the level of residual interstitial oxygen is significantly higher than low Oi materials. Besides, the lack of precipitation can be an issue also for slip-lines robustness.

But the fabrication process used to generate those FD-SOI wafers with thin and uniform layers implies some specific very high temperature thermal treatments above 1100°C, for several hours, then helping to strengthen the oxygen precipitation rate. Besides, we know we have some options to increase this precipitation further, such as conventional nucleation and stabilisation of BMD already described, and also increasing the initial point defects such as vacancies to enhance heterogeneous nucleation. And finally, this middle Oi material range is compatible with low COPs pulling, contrarily to high Oi options.

As briefly presented above, our targets will be to reach a BMD range between 1e9 to 1e10 def/cm3 to be compatible with both slip-lines and overlay requirements, and a high and stable resistivity after thermal donor generation, between 500 to 1500 Ω.cm.

Tests and Samples Description

The precipitation enhancement options, separately or combined together, have been evaluated on the middle Oi range, approximately between 16 to 21 old ppma, on 300mm wafers. The incoming material resistivity range on the test samples was from 500 to 1000 Ω.cm. The precipitation tests were composed of 2 different treatments, one working on standard nucleation process as already described, based on a long thermal treatment, and one working on adding heterogeneous sites for nucleation, based on a rapid thermal annealing on the initial material before all thermal stages.

The thermal treatment for conventional precipitation is made of one double nucleation between 650°C to 800°C for 2 to 4 hours, and one growth stage at 1000°C for

several hours, at least 5 hours. The effect of that kind of precipitation has already been described above and is coherent with former extensive literature on this topic (2).

The rapid thermal treatment, for nucleation site strengthening, is composed of an RTP (rapid thermal processing) stage, at very high temperature above 1250°C, for approximately 30 seconds, under nitride gas ambient. A nitride ambient will inject vacancies inside silicon handle material from the surface, in addition to in-depth vacancy generation due to high temperature treatment and rapid cool down freezing vacancies in depth. Those vacancies will help the heterogeneous nucleation, and lead to a higher precipitation rate, then compensating for the initial lack of precipitation for middle [Oi] (from 16 to 23 old ppma). Vacancy injection and strengthening of nucleation by this way is documented in literature (4; 5; 6; 7). This process configuration, done on the initial material before any thermal treatment, will also help to prevent a depleted BMD zone at the handle wafer surface, increasing the in-depth resistivity stability up to at least 50 to 100µm depth below the buried oxide.

Effects of Preliminary RTP Addition

We tested similar substrates, one set with [Oi] 16-17 old ppma, and another set with [Oi] 20-21 old ppma, with and without the preliminary RTP treatment injecting vacancies. The BMD density, measured at final SOI with laser scattering tomography (LST), is drastically increased when we apply the preliminary RTP, as shown in figure 4, for both sets of samples, at 16-17 or 20-21 old ppma. Besides, the BMD radial density is clearly more homogeneous if we apply the RTP step due to vacancy injection through the whole surface of the wafer. Then the radial homogeneity is not dependent on the initial pulling conditions leading to centre to edge variations, and we can have a better stability through the wafer radius. We managed to reach the good BMD range between 1e9 to 1e10 def/cm3 by applying this preliminary RTP on material, on the middle Oi range, even if we are really close to the 1e9 def/cm3 minimum target on the lowest Oi range 16-17 old ppma.

The injection of vacancies from the wafer surface, leading to more robust precipitation, is also visible on the LST pictures in figure 5. Those pictures are taken at the wafer centre, where we measure the maximum BMD density on wafer without preliminary RTP, anyway, we still can see the huge difference in precipitation regime at both the 50µm surface, and also in depth, on those 20-21 old ppma substrates.

The effect of this better precipitation rate is already visible in defectivity maps on slip-lines, as shown in figure 6, suppressing both boat marks and slip-lines at wafer edges. However, as BMD density on 16-17 old ppma is close to the 1e9 def/cm3 minimum BMD density, statistically we could find very low residual small slip-lines on few wafers. Then, we would need to go slightly further for this precipitation enhancement on this lower [Oi] materials.

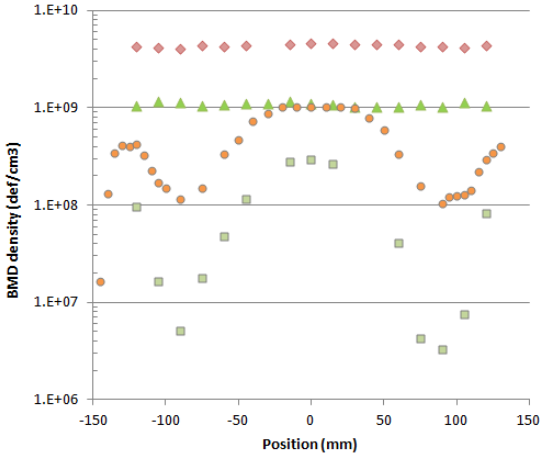
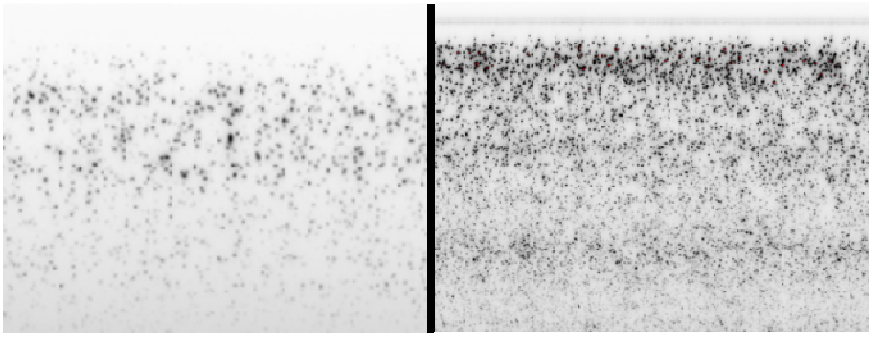


Figure 4. BMD density on wafer diameter, measured with LST, at final SOI. Diamond shape is 20-21 old ppma with RTP, circular shape is 20-21 old ppma without any RTP, triangular shape is 16-17 old ppma with RTP, square shape is 16-17 old ppma without any RTP.



a b

Figure 5. LST pictures at final SOI, at wafer centre, for 20-21 old ppma ; a) without any preliminary RTP on initial material, b) with additional preliminary RTP on bulk. Picture size is 400µm in depth and images are cut at approximately 500µm large.

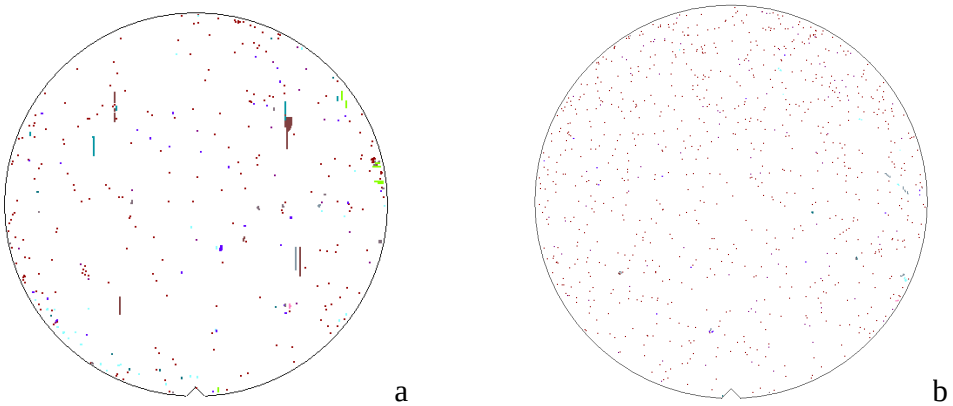


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Figure 6. Final SOI defectivity SP5 maps in oblique mode, on 25 wafers stacked, middle Oi 16-17 old ppma, a) without RTP, and b) with RTP.

For the resistivity stability in depth, figure 7 shows the different behaviour, with and without the preliminary RTP. Wafers with preliminary RTP can be quite stable at 500 Ω.cm after soft-DGA, whereas the resistivity increases dramatically after the initial worst case DGA. In comparison, resistivity stability is not guaranteed on wafers without RTP, even with the soft-DGA, the thermal donors generated increase resistivity from 500 Ω.cm to roughly 800 Ω.cm. And after the worst case DGA, there are so many thermal donors generated that we measure in-depth type flipping. Clearly the RTP addition will help to maintain some stable resistivity with the soft-DGA.

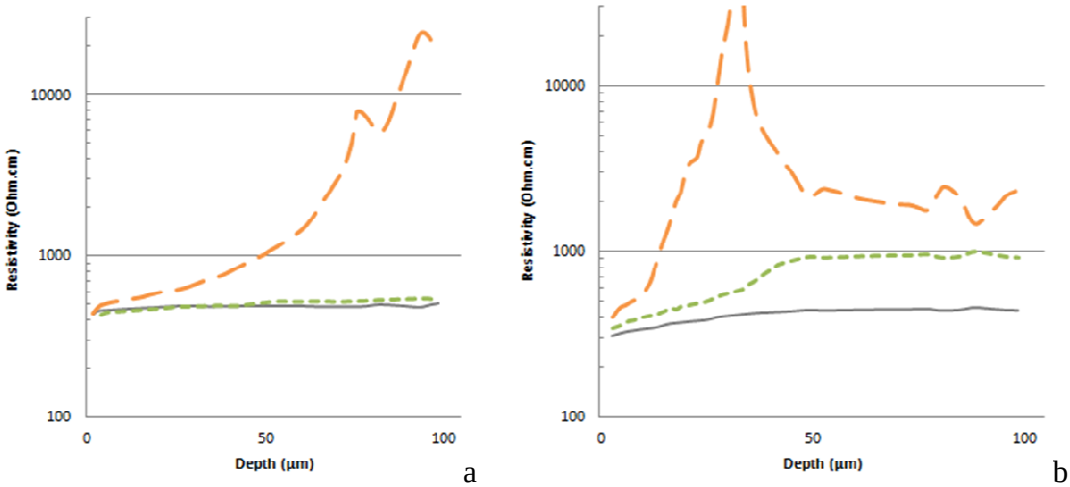


Figure 7. SRP profiles at final SOI, for 20 old ppma material initially around 500 Ω.cm, a) with preliminary RTP, b) without preliminary RTP. Plain lines are at final SOI, short-dash lines are at final SOI and soft-DGA, long-dash lines are at final SOI and DGA.

Considering the effect on BMD density and on resistivity stability even for the lowest range of resistivity, the pre-processing with an RTP step injecting vacancies, before performing the SOI process, is a key step to have a robust HR FD-SOI product.

Effects of Preliminary Precipitation Addition

Same as for the preliminary RTP tests, we evaluated the effect of the additional specific precipitation treatment on 2 sample sets, one with [Oi] 16-17 old ppma substrates, and the other one with [Oi] 20-21 old ppma substrates. Those substrates were both preliminary treated with an RTP step injecting vacancies, to help for further precipitation. By adding this specific precipitation treatment, we also demonstrated a further improvement on the BMD density on both kinds of materials, leading to a safer BMD range around 6 to 7 e9 def/cm3, even for the lowest [Oi] substrates at 16-17 old ppma, as shown in figure 8. The density homogeneity is still guaranteed as we have performed the preliminary RTP, and the additional specific precipitation treatment doesn't affect this homogeneity. The BMD size is also increased on the 2 material sets, due to an enhanced growth time by adding specific treatment in addition to the long thermal SOI process at high temperature above 1100°C. This BMD size above 50 to 60 nm is believed to be big enough to have a beneficial effect on slip-lines trapping, and indeed we don't detect any slip-line even for the lowest [Oi] material around 16 old ppma after this cumulative RTP and specific precipitation tests, at final SOI. The in-depth BMD density homogeneity is also reinforced by the specific precipitation treatment as shown by LST pictures in figure

9. We are also safe towards overlay risks as the BMD density is still below 1e10 def/cm3, and as shown in part 5 of this work.

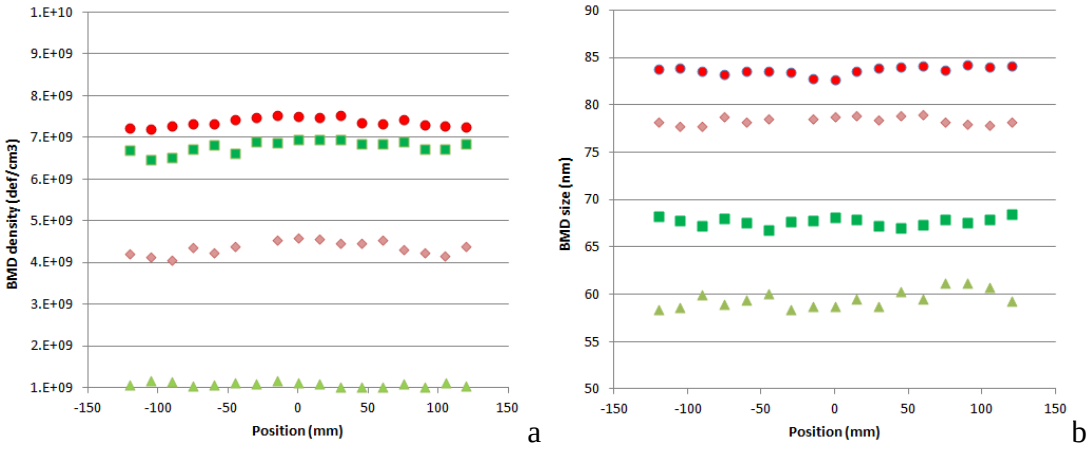
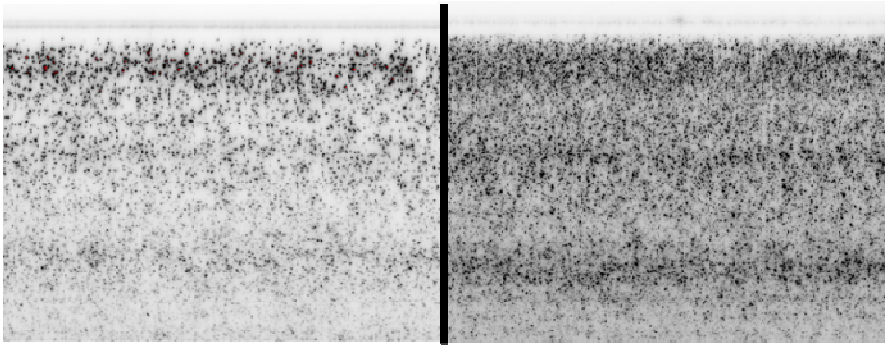


Figure 8. BMD density (a) and size (b) on wafer diameter at final SOI. Preliminary RTP was applied on material. For [Oi] 20-21 old ppma, diamond shape is without specific precipitation, circular shape is with specific precipitation. For [Oi] 16-17 old ppma, triangular shape is without specific precipitation, and square shape is with specific precipitation.



a b

Figure 9. LST pictures at final SOI, at wafer centre, for [Oi] 20-21 old ppma with preliminary RTP ; a) without specific precipitation, b) with specific precipitation. Picture size is 400µm in depth and images are cut at approximately 500µm large.

The in-depth resistivity stability is represented in figure 10 which illustrates the benefit of the specific precipitation anneal addition. The wafers without specific anneal will show huge variations after DGA, and a quite stable resistivity after soft-DGA, whereas the wafers with the specific anneal show a very good stability within a range 1000-2000 Ω.cm, whatever the DGA conditions applied. The precipitation is clearly enhanced, and then the amount of thermal donors is reduced, and compensated by initial P-type doping level for the targeted resistivity range.

This way to process the substrate gives good results in terms of resistivity stability in the middle to high resistivity range, from few hundreds Ω.cm to few kΩ.cm, BMD density and size, and protects from defectivity such as slip-lines propagation. The specific precipitation anneal, cumulated with vacancies injecting RTP and conventional FD-SOI process, is an important step to be compatible with HR FD-SOI product requirements.

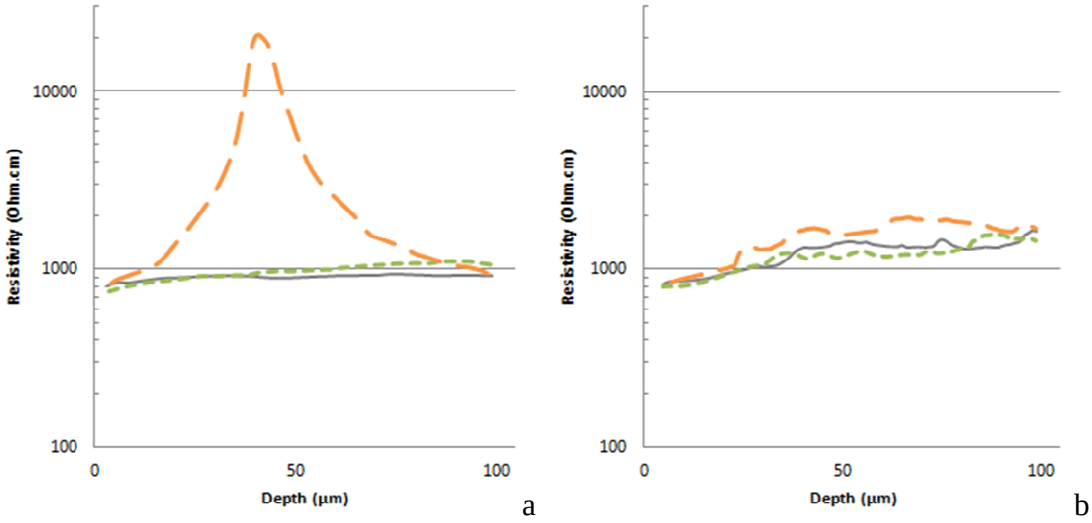


Figure 10. SRP profiles at final SOI, for 16-17 old ppma material initially around 1000 Ω.cm, a) no specific precipitation, b) with specific precipitation. Plain lines are at final SOI, short-dash lines are at final SOI and soft-DGA, long-dash lines are at final SOI and DGA.

Material Results Discussion

With some other experimental points on the middle Oi range, with resistivity from 500 to 1500 Ω.cm, we were able to estimate the residual [Oi] left inside the material on each 2 configurations : with RTP and no specific precipitation, with RTP and with specific precipitation. This is based on raw SRP data comparison, before and after DGA, and conversion of added donors within residual [Oi] quantity, with a home-made thermal donor generation model. This residual [Oi] estimation is plotted in figure 11. A rough estimation was added for wafers without preliminary RTP treatment, as we had few data, only for comparison with the other processes.

Based on this estimation, we were able to simulate the resistivity stability towards soft-DGA and DGA, within a larger scale of incoming oxygen and resistivity. This is summarised in Table 1, for the RTP + precipitation case. We can confirm that with a targeted resistivity around 250 to 1500 Ω.cm we can accept middle Oi material if the back end conditions are similar to soft-DGA conditions, around 425°C 30 minutes (or equivalent to 400°C 1 hour). This material range is reduced to 250 to 750 Ω.cm maximum if back end conditions are closer to DGA 450°C 1 hour which is the worst case scenario.

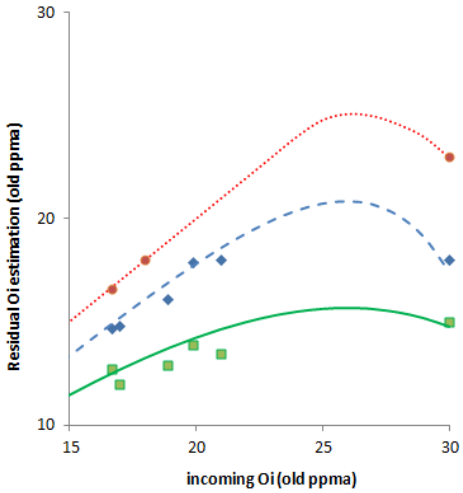


Figure 11. Residual [Oi] calculation as a function of incoming [Oi], for the 3 different processes. Points are experimental data, lines are the worst case projection. Plain line is with preliminary RTP and specific precipitation, dashed-line is with preliminary RTP but without specific precipitation, dotted-line is rough estimation on wafers without any RTP nor specific precipitation, only FD-SOI process.

TABLE I. Resistivity variations after soft-DGA or DGA, for RTP + specific precipitation process at final SOI (Resistivity is in Ω.cm) - calculations are done for [Oi] range from 17 old ppma to 22 old ppma

Incoming	Final + soft-DGA	Final + DGA
250	255 to 260	280 to 300
500	530 to 570	650 to 900
750	850 to 920	1150 to ~2000
1000	1150 to 1350	~2000 to >5000*
1250	1500 to 1800	~3000 to type flipping*
1500	1900 to 2400	>5000 to type flipping*

* Resistivity is very high and unstable, up to type flipping and further resistivity loss due to excessive thermal donor generation

Within this material range, we also confirmed that the BMD density and size were comfortable enough to block slip-lines propagation, without having excessive BMD density that could lead to plastic deformation at customer's processing.

Substrate Validation for RF Applications

As explained above, the optimization of the substrates leads to a base wafer resistivity in the 250~1500 Ω.cm range. Said substrates being destined to RF and mmWave applications, it is essential to ensure they induce low insertion loss in the devices built upon them. Contribution of the substrate to the insertion loss is driven by the effective resistivity (8). Figure 12 shows the values extracted at 6GHz as a function of base wafer resistivity for simulated coplanar waveguides (CPW) placed directly above a 20nm-thick BOX or on top of an 8µm-thick back end of line dielectric. The CPW transmission lines are 2 mm long, the width of the signal electrode is W= 26 µm, the spacing between the ground and signal electrodes is S= 12 µm and the width of the ground electrode is 208 µm. The same geometry is used for simulations and measurements.

For both dielectric thicknesses, a tenfold improvement is seen when going from a standard 10-15 Ω.cm wafer to about 300 Ω.cm. For higher resistivities, the effective resistivity remains mostly constant as it is primarily driven by the parasitic surface conduction (PSC) (9;10), thus negating the need to resorting to higher resistivities. This conclusion would be different in a substrate integrating a Trap-Rich solution to suppress the PSC (11). A steady improvement of the RF performance with the base wafer resistivity would then be seen.

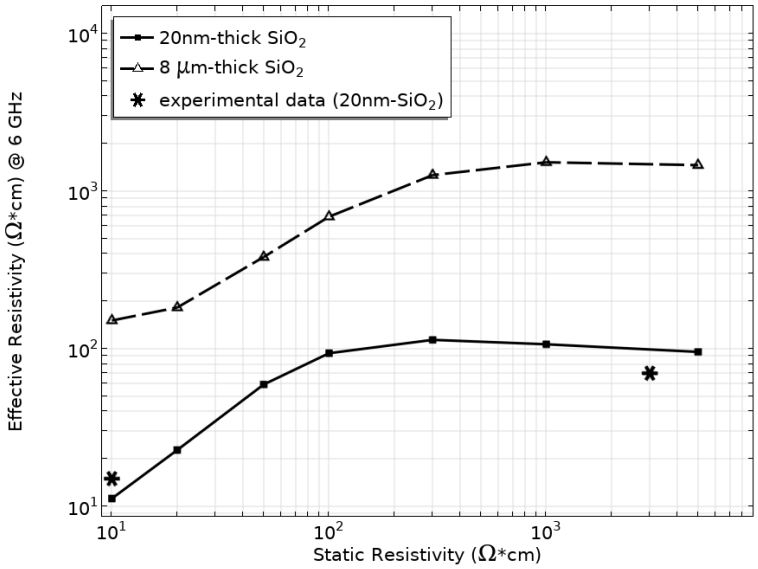


Figure 12. Effective resistivity as a function of the base wafer resistivity extracted at 6GHz from simulated CPWs for 20nm or 8µm-thick SiO_2 between the CPWs and silicon wafer. Dark stars denote measurements on fabricated structures.

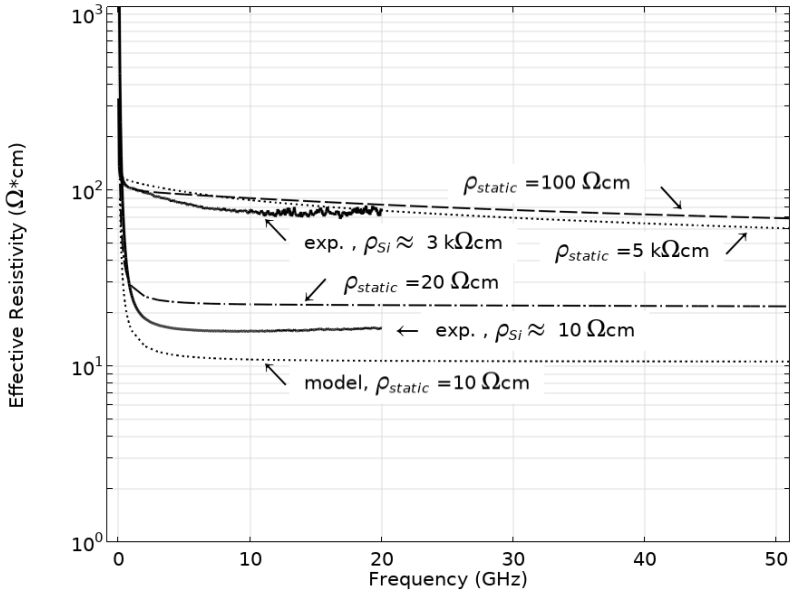


Figure 13. Effective resistivity as a function of frequency extracted (12) from measured (solid lines) and simulated (dashed lines) CPWs deposited on a 20nm-thick BOX on substrates with various base wafer resistivity.

On figure 13 are represented both experimental and simulated data of effective resistivity as a function of frequency for a standard and high resistivity substrate. The advantage of the HR wafer remains throughout the frequency range.

Validation on Device

Specific experiments were carried out to ensure that going from standard to high resistivity substrates did not adversely impact the CMOS fabrication process, nor the behaviour of logic devices. The samples have been fabricated with a 28FDSOI single gate oxide process flow, using HfO2 as high-k dielectric and TiN as metal gate. The gate length and BOX thickness are respectively 28 and 25 nanometers. Two threshold voltage flavours are obtained by playing with the wells doping type. To speed up the study, the devices have been probed at M1. Parametric test structures were implemented on SOI substrates with handle resistivity ranging from 10 Ω.cm to 5 kΩ.cm and channel orientation <100>. The only adaptation brought to the process was a tuning of the electrostatic chuck current limit at the implantation steps in order to avoid false alarms, as the high resistivity affects the clamping current stability. Other than this, all wafers successfully went through all the standard 28nm process steps up to M1.

As explained above, the main concern when processing high resistivity substrates is the impact of the change in interstitial oxygen concentration [Oi] on the mechanical properties of the substrates, which can, in turn, generate overlay issues. We compared the overlay maps obtained from 4 flavours of wafers: Standard resistivity, with a middle [Oi] as well as HR wafers with either low, middle or high [Oi]. The maps are shown in Figure 14 along with the overlay value at gate level.

While for high and low [Oi] the overlay is degraded, it is not impacted by the use of the middle [Oi] HR substrate, thus validating our optimization choices.

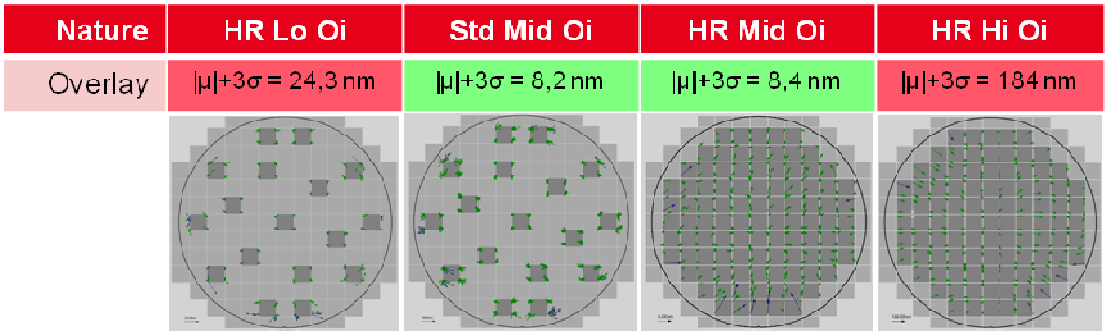


Figure 14. Overlay maps between active and gate levels (courtesy of STM) of 4 different flavors of wafers.

Figure 15 represents the VTH distributions for low VTH (LVT) and regular VTH (RVT) devices on both standard and HR wafers. Comparison is performed in the linear regime on devices with L=W=1µm to limit geometrical variation impact. Neither centering nor spread of the distributions are affected by the substrate resistivity. This can be easily understood by considering that the devices are sitting on type of either N or P wells with a dopant concentration of the order of $10^{18}cm^{-3}$, so 3 to 6 orders of magnitude

higher than the substrates' doping. These results demonstrate that the implanted dopant profiles were not affected by the high resistivity.

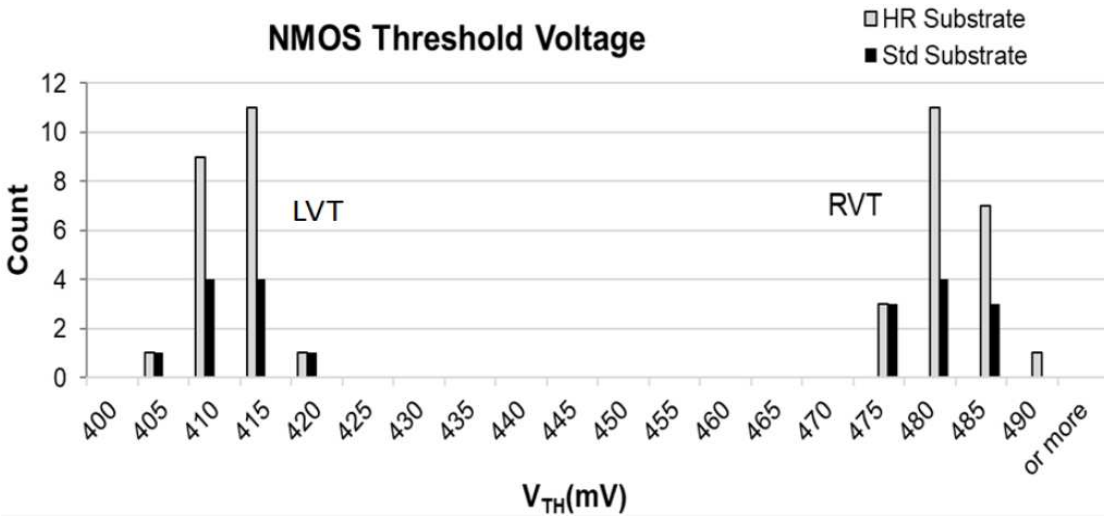


Figure 15. Linear V_{TH} Distribution of Regular and Low V_{TH} NMOSFETs, with W=L=1µm on both standard (black) and HR (grey) substrates.

The performance of the fabricated devices was at the expected level for a 28nm technology, with on-currents well above 1mA/µm. Figure 16 illustrates the I_{ON}/I_{OFF} tradeoff of the nominal devices, with drawn gate length L ranging from 30 to 36nm and gate width of 210nm. Once again, the results show that the resistivity of the substrate does not affect the devices' characteristics, even for high performance transistors.

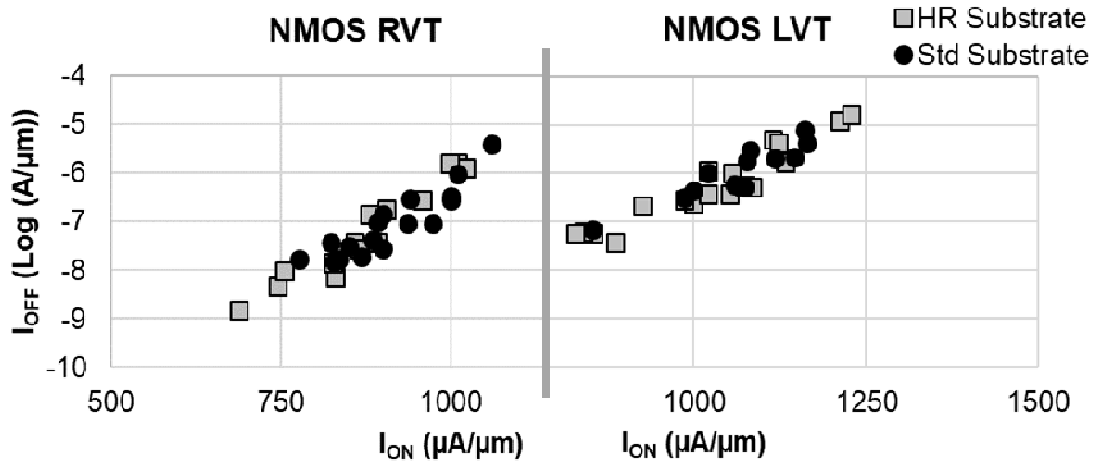


Figure 16. I_{ON}/I_{OFF} plots of Regular and Low V_{TH} NMOSFETs on both standard (black) and HR (grey) substrates. L ranging from 30 to 36nm. W=210nm.

Conclusion

In conclusion, we have developed a process to obtain High Resistivity FD-SOI substrates, based on middle Oi materials, with a good robustness towards slip-lines and overlay potentiel issues, and with a final resistivity which is stable versus back end of line

treatments and compatible with the application needs. Through simulation, RF measurements as well as fabrication of logic devices using 28nm design rules, we have demonstrated that the selected [Oi] and resistivity range enables improving the RF parameters of passive devices without any negative impact on the CMOS fabrication process, nor the logic devices performance.

The HR option for FD-SOI product portfolio is seen as a new leveller to further enhanced performance while enabling more and better RF IP implementation on a same die. In order to have a seamless transition from standard to HR FD-SOI, SOITEC aims to design a substrate that will avoid device integration changes for existing 28nm, 22nm and future 18nm, 12nm technology nodes. Hence, HR FD-SOI substrates will benefit from any CIP updates to match standard FD-SOI manufacturing capability and get flexible Fab capacity.

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