# Mixed-Signal Compensation of Tripolar Cuff Electrode Imbalance in a Low-Noise ENG Analog Front-End

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***Abstract*—Due to their low amplitude, electroneurogram (ENG) signals are particularly subject to external muscle artefacts and intrinsic electronic noise. However, achieving a high signal-to-noise ratio is a challenge for implanted systems that have a limited power budget. This work presents a low-power analog front-end which features low intrinsic noise and high interference rejection. The proposed mixed-signal feedback loop for tripolar cuff electrode imbalance compensation provides an interference rejection of 56 dB with a negligible power overhead. The instrumentation amplifier achieves a gain of 91.5 dB, an input-referred noise of 1.35 µV, an input offset voltage below 1 µV, and digitally-tunable imbalance compensation with 7 bits of resolution over a ±20% range. The results are validated on the ICare microcontroller system-on-chip, a 22-nm fully-depleted silicon-on-insulator prototype.**

***Index Terms*—Biomedical electronics, CMOS integrated circuits, analog front-end, electroneurogram, low noise, imbalance.**

## I. Introduction

The vagus nerve is a cranial nerve which plays a key role in the autonomic nervous system. It carries bidirectional information between the medulla oblongata in the brainstem and multiple organs such as the heart, the lungs, the liver, and many others. Vagus nerve stimulation has already proven useful for the treatment of epilepsy and depression, and has demonstrated promising results for other disorders [1]. The interest around vagus nerve sensing, i.e., vagus nerve electroneurogram (VENG), has also been growing for diagnostic purposes. It has been used previously for epileptic seizures detection [2] or the extraction of respiratory markers [3].

However, the design of VENG acquisition systems, as the one represented in Fig. 1, encounters several challenges. Firstly, compared to other electrical biosignals, neural signals have a very low amplitude below 20 µV and a high bandwidth up to 20 kHz [2]. The input instrumentation amplifier (IA) thus requires a high gain above 90 dB and a very low input-referred noise below 2 µV RMS. A low DC offset voltage is also necessary to avoid saturation with the high gain. Secondly, the VENG signal is subject to interferences from surrounding electrical biosignals from the heart and muscles. Due to their high amplitude, these artefacts can saturate the amplifier if they are not properly rejected. Tripolar cuff electrodes can be used to linearize the external artefact and reject it using a true tripole or quasi-tripole amplifier configuration. Unfortunately, this linearization may not be ideal due to electrode imbalance, which requires additional compensation techniques [4]. Finally, in the case of long-term implantable devices, the limited battery capacity, usually in the order of 1 Ah, imposes a power consumption around 100 µW to last several years.

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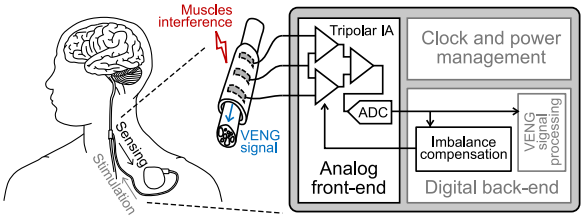


Fig. 1. VENG acquisition system with tripolar cuff electrode input. The analog front-end interfaces the cuff electrode and compensates the imbalance. The digital back-end (DBE) estimates the imbalance to control the compensation feedback loop and can perform additional VENG signal processing to infer clinical information. The clock and power management unit generates all clocks and voltage references used in the system.

In this work, we propose an analog front-end (AFE) for VENG signal acquisition with a new mixed-signal imbalance compensation method. The AFE features a low input-referred noise of 1.35 µV RMS and a power consumption of 104 µW. Section II presents the mixed-signal imbalance compensation scheme which provides high signal-to-interference ratio and allows duty-cycled operation for reduced power overhead. In Section III, the IA with gain balancing is described and optimized for low-noise, high-gain and low-offset performance. Section IV finally details the AFE prototype embedded in a 22-nm fully-depleted silicon-on-insulator (FD-SOI) microcontroller SoC codenamed ICare, with its measurement results.

## II. Imbalance Estimation and Compensation

The linearization effect inside the tripolar cuff electrode enables the rejection of external artefacts. Indeed, as the resistivity inside the cuff is assumed constant and as A, B, and C electrodes are equally spaced, $V_{AB}$ and $V_{CB}$ voltages have opposite values as shown in Fig. 2(a). By adding those voltages, the artefact current $I_{art}$ is cancelled and only the ENG signal ($V_{ENG}$) remains. The most common amplifier configurations for instrumentation amplifiers to perform this cancellation are the true tripole and quasi-tripole architectures

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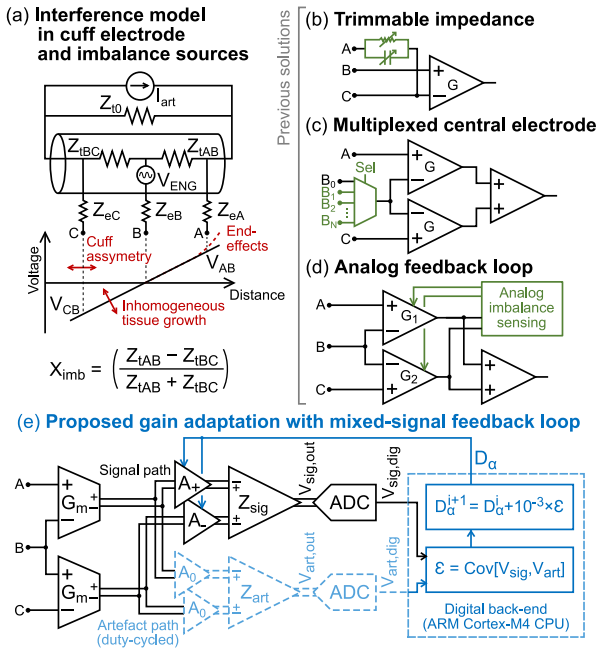


Fig. 2. Tripolar cuff electrode imbalance model and compensation methods. In the lumped-element model (a), $V_{ENG}$ and $I_{art}$ are the sources of ENG signal and external muscle artefacts. The impedances model the tissue resistance outside ($Z_{t0}$) and inside ($Z_{tAB}$, $Z_{tBC}$) the cuff electrode. Trimmable impedance (b), multiplexed central electrodes (c) and analog feedback loop (c) techniques have been proposed in the literature. This work proposes a mixed-signal compensation scheme (e) with duty-cycled artefact sensing path.

[4]. Unfortunately, the linearization assumption is not always verified due to cuff non-idealities such as inhomogeneous scar tissue growth, cuff asymmetry, and non-linearity of the electric field close to the cuff extremities. These effects lead to an imbalance $X_{imb}$ between the $Z_{tAB}$ and $Z_{tBC}$ impedances which induces an imperfect cancellation of the artefact.

Modifications to the tripole amplifier configurations have been proposed to enable the compensation of electrode imbalance. Demosthenous et al. [5] added a trimming impedance network in series with one of the electrodes in the quasi-tripole configuration (Fig. 2(b)). This solution however requires large off-chip capacitors up to 500 nF. ElAnsary et al. [6] used a multiplexer with multiple selectable electrodes to modify the sensing location inside the cuff (Fig. 2(c)). The resolution of this solution is limited by the number of electrodes and the minimal manufacturing dimensions. The previous solutions do not discuss how the estimation of the imbalance is performed prior to setting the actual compensation. Demosthenous and Triantis [7] proposed an analog adaptive tripole (AAT) configuration in which the individual amplifier gains can be tuned (Fig. 2(d)). The gain control is performed by a bias voltage generated from an analog imbalance sensing module. This solution however requires the imbalance sensing to remain active, which consumes 1.4 mW (20% of the total power).

In this work, we propose a new imbalance compensation scheme based on a mixed-signal artefact estimation and compensation loop (Fig. 2(e)). In the signal path, two transconductance stages ($G_m$) followed by current amplifiers ($A_\pm$) and a transimpedance stage ($Z_{sig}$) amplify the signal. All blocks are fully-differential to improve the common-mode rejection. Similarly to the AAT [7], the imbalance compensation is performed by symmetrically tunable gains. However, digital control signals $D_\alpha$ are used here to enable robust and duty-cycled artefact estimation. The gain adaptation is performed at the current amplification stage by two complementary gains $A_\pm = A_0(1 \pm \alpha)$. When the imbalance remains small, the resulting signal obtained along the ENG signal sensing path before digitization is approximately equal to

$$V_{sig,out} \approx 2G_m A_0 Z_{sig} \left[V_{ENG} - V_{art,res}\right], \\ V_{art,res} = \frac{I_{art} Z_{t0}}{2}(X_{imb} + \alpha), \tag{1}$$

where it can be seen that the ENG signal $V_{ENG}$ can be properly recovered, i.e. the residual artefact interference $V_{art,res}$ is zero, if the gain adaptation $\alpha$ matches the imbalance $X_{imb}$.

In order to properly set the gain control $D_\alpha$, the artefact is measured through a separate artefact sensing path using fixed-gain current amplifiers ($A_0$) and a second transimpedance ($Z_{art}$). Reusing the same $G_m$ stages allows to save power and additionally compensate mismatch between the transconductances. Note that as $V_{AB}$ is subtracted from $V_{CB}$ instead of added, by inverting the wires compared to the signal sensing path, the output signal of the artefact path is equal to

$$V_{art,out} = G_m A_0 Z_{art} I_{art} Z_{t0}. \tag{2}$$

The covariance between the outputs of the signal and artefact paths is computed in the digital back-end (DBE) by an ARM Cortex-M4 CPU over a 200-sample window and is used as an error signal $\varepsilon$, as shown in Fig. 2(e). When the $A_\pm$ gains are correctly adapted and the artefact is effectively removed from the signal, the covariance is close to zero. When the gain adaptation does not match the imbalance, the artefact is mixed with the signal and the covariance increases in absolute value. The sign of the covariance provides information on the direction of the imbalance. The gain control is performed iteratively by a first-order infinite-impulse-response (IIR) filter integrating the error until it reaches zero.

Thanks to the separate sensing paths, the gain in the signal path can be set higher as the feedback loop is robust to artefact-related saturation. Assuming maximum amplitudes of 20 µV and 500 µV for the ENG signal and the artefact [7], the gains are set as follows: $G_m = 4.2$ mS, $A = 0.25$, $Z_{sig} = 18$ MΩ, and $Z_{art} = 590$ kΩ. The analog-to-digital conversion is implemented with time-based ADCs using voltage-controlled oscillators. They have a resolution of 10 bits with a power consumption of 0.8 µW per ADC at a 32-kHz sampling rate.

The main limitation of the mixed-signal imbalance compensation is the resolution of the gain control, which limits the worst-case artefact attenuation, i.e., when the imbalance $X_{imb}$ sits between two successive codes. From Eq. (1), it can be seen that the worst-case signal-to-interference ratio (SIR) is equal to

$$SIR_{out} = \frac{V_{ENG}}{V_{art,res}} = \frac{4V_{ENG}}{I_{art} Z_0 \alpha_{LSB}}, \tag{3}$$

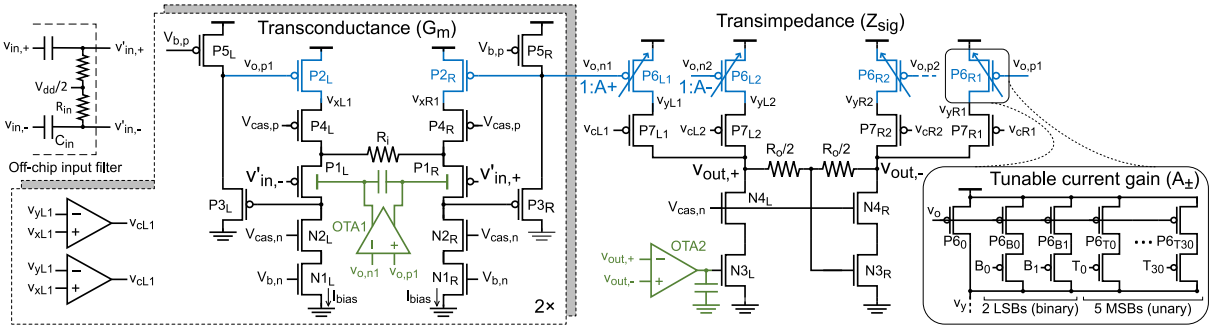


Fig. 3. Instrumentation amplifier circuit. The blue color highlights the current mirrors with tunable gain $A_{\pm}$ for the imbalance compensation. The green color shows the offset correction feedback loops with $OTA_1$ and $OTA_2$.

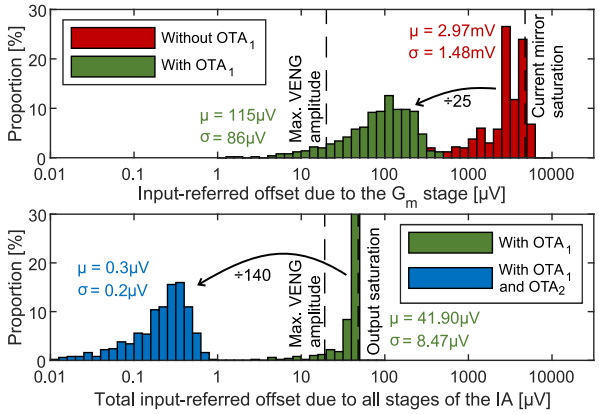


Fig. 4. Monte-carlo offset simulation results before and after correction. $OTA_1$ and $OTA_2$ avoid saturation in the $G_m$ and $Z_{sig}$ respectively. The resulting offset is lower than 1 μV, which is well below the signal level.

with $\alpha_{LSB}$ the gain control step size. In order to reach a minimum signal-to-interference ratio (SIR) of 20 V/V, a gain resolution $\alpha_{LSB}$ of 0.35% is required. This corresponds to an artefact rejection of 56 dB. With a nominal gain of 91.5 dB (37.5 kV/V), this corresponds to a resolution of 130 V/V, with 128 steps (7 bits) over a ±20% imbalance range.

## III. Low-Noise Instrumentation Amplifier

A current-balancing topology is used for the IA as shown in Fig. 3 [8]. The input differential voltage $v'_{in}$ after the external high-pass filter is copied to the terminals of resistor $R_i$ by transistors $P_1$ in flipped voltage-follower structures, which generates a current variation between the branches. The $G_m$ transconductance is equal to $(R_i + g_{d,P1}/(g_{m,P1}g_{m,P2}))^{-1}$. The current variation is copied from transistors $P_2$ to $P_6$ with a current gain $A = (W/L)_{P6}/(W/L)_{P2}$. The tunable current gain is implemented by digitally controlling PMOS switches ($B_{0-1}$, $T_{0-30}$) to modify the width of transistors $P_6$. The current from the two $G_m$ blocks is summed at the nodes $v_{out}$ and the impedance $R_o$ generates the output differential voltage.

Given the low amplitude of the VENG signal, the instrumentation amplifier in the AFE must achieve high noise efficiency in order to reach a sufficient signal-to-noise ratio. A genetic optimization algorithm similar to [8] performs the sizing of the devices in the signal sensing path to reach the optimal

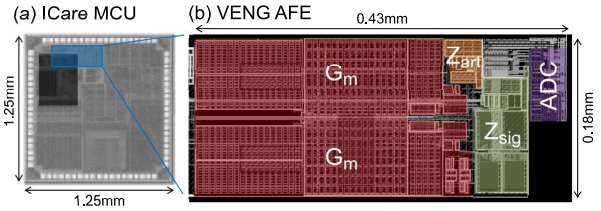


Fig. 5. ICare chip (a) and AFE (b) layouts. The $G_m$ stages take up 65% of the space due to the noise requirement on the input stage of the IA. Time-based ADCs occupy only 3500 μm$^2$ thanks to their digital-only implementation.

noise-power trade-off. The resulting design achieves an input-referred noise (IRN) of 1.3 μV RMS and consumes an average power of 102 μW when the artefact path is disabled.

Due to the large gain of 91.5 dB, the input-referred offset voltage of the amplifier needs to remain in the μV range. In the considered topology, the offset arises mainly from the mismatch between the input pair $P_1$, the current sources $N_1$ and the current mirrors $P_2$-$P_6$. Without an appropriate solution, this mismatch leads to a large DC current being amplified and results in the saturation of the amplifier. As the VENG signal bandwidth starts at 500 Hz, the offset can be filtered out by introducing two DC feedback loops in the $G_m$ and $Z_{sig}$ stages. Those feedback loops work by matching the DC levels of the output signals ($v_{o,p}$ and $v_{o,n}$ in $G_m$, and $v_{out,+}$ and $v_{out,-}$ in $Z_{sig}$). The first feedback loop ($OTA_1$) acts on the back-gate of the input transistor pair $P_1$, which modulates their respective threshold voltage $V_{th}$. The second feedback loop ($OTA_2$) directly controls the front-gate of the bottom left NMOS $N_3$ to regulate the bias current. The low-frequency pole at 500 Hz in the feedback loop is set by the amplifiers with low conductance and on-chip capacitors. Simulation results show that the offset is effectively reduced below 1 μV as shown in Fig. 4.

## IV. Measurement Results

The AFE along with the proposed compensation scheme have been prototyped in a 1.6 mm$^2$ chip in 22-nm FD-SOI technology from GlobalFoundries. As shown in Fig. 5, the VENG AFE only takes up 0.077 mm$^2$ while the rest of the chip is occupied by the DBE and the clock and power management unit which are not discussed in this paper. Measurements of the AFE show a good matching with expected performance, with a gain of 91.5 dB and a bandwidth up to 16 kHz. The

TABLE I
ENG AFE COMPARISON

| | This work | ElAnsary [6] JSSC 2021 | Demosthenous [5] Sensors 2013 | Demosthenous [7] JSSC 2005 | Ng [9] JSSC 2019 | Schönle [10] JSSC 2018 | Lee [11] TCAS-II 2018 |
|---|---|---|---|---|---|---|---|
| Technology | 22nm FD-SOI | 0.13µm CMOS | 0.35µm CMOS | 0.8µm BiCMOS | 0.18µm CMOS | 0.13µm CMOS | 0.13µm CMOS |
| Electrode configuration | Tripole | Quasi-tripole | Quasi-tripole | Tripole | Bipole | Bipole | Quasi-tripole |
| Compensation resolution | 7 bits | 3 bits | 7 bits | Continuous | - | - | - |
| Compensation range | ±20% | ±45% | ±80% | ±40% | - | - | - |
| Artefact rejection [dB] | **56** | 25 | 44 | **60** | - | - | - |
| Power (/channel) [µW] | **104** | **0.14** | **27** / 930 | 7200 | **34** | 285 | **11** / 176 |
| Gain [dB] | **91.5** | N/A | 6 - 47 | **87** | 55 / 75 | 18 / 66 | 44 |
| IRN [µV RMS] | **1.4** | 24.7 | 2.95 / **0.7** | **0.29** | **1.9** | **1.2** | 3 / **1** |
| Power efficiency factor | 27 | 13 | 24 / 43 | 60 | 33 | 4100 | 9 / 15 |
| ADC | 10b time-based | 8b ΣΔ | - | - | 10b SAR | 14b SAR | - |

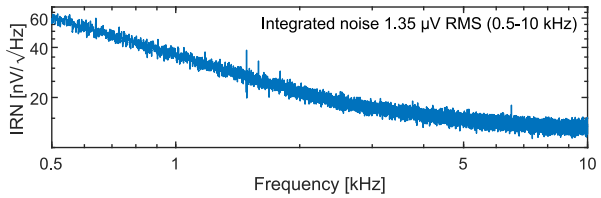


Fig. 6. Measured noise power spectrum density for the signal sensing path.

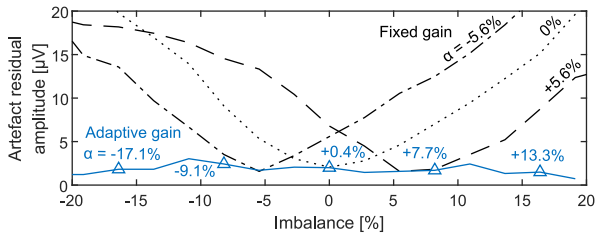


Fig. 7. Artefact interference and imbalance compensation. The gain compensation $\alpha$ in blue shows the inferred imbalance estimated and corrected by the feedback loop.

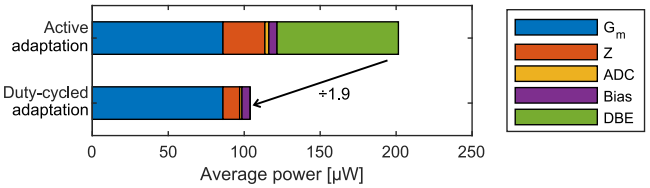


Fig. 8. Power breakdown of the VENG sensing SoC with active and duty-cycled compensation. The $G_m$ stages dominate the power consumption for noise requirements.

measured noise distribution shown in Fig. 6 corresponds to an IRN of 1.35 µV. Compared to the state of the are (Table I), the proposed AFE provides excellent resolution for imbalance compensation, while having a low power consumption, a high gain, and a competitive noise efficiency.

With fixed gains at different $D_\alpha$ configurations, Fig. 7 shows that the artefact only cancels at specific imbalance values. When enabling the gain adaptation with the proposed mixed-signal feedback loop, the system is able to accurately estimate the imbalance and compensate it with the appropriate setting to keep the residual amplitude close to the measurement noise level. The response to a change in imbalance takes less than 250 ms to settle, thus allowing very low duty-cycle ($< 1\%$). As shown in Fig. 8, while the feedback loop increases the power consumption by 93%, it can be disabled after estimation, thus making its impact on average power consumption negligible. The average power consumption with duty-cycled gain adaptation is 104 µW.

## V. Conclusion

The mixed-signal scheme proposed in this work provides a solution to tripolar cuff electrode imbalance with low power and area overhead, which achieves high compensation resolution and robust imbalance estimation. A high artefact rejection of 56 dB reduces the residual artefact interference below noise level. The prototyped AFE achieves high gain and noise efficiency which is of the utmost importance for sensing low-amplitude ENG signals. The proposed AFE was successfully validated on a 22-nm FD-SOI prototype chip.

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