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SURVEY

AI-Driven Integrated Circuit Design: A Survey of Techniques, Challenges, and Opportunities

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ABSTRACT Analog and radio-frequency integrated circuit (RFIC) design has traditionally been defined by inherent complexity, reliance on manual iterations, and dependence on domain-specific heuristics. Recently, however, this landscape has undergone a transformative shift driven by advances in Artificial Intelligence (AI) and Machine Learning (ML). This survey provides a systematic and forward-looking review of AI-enabled methodologies—including evolutionary algorithms, Bayesian optimization, reinforcement learning, deep learning, and large language models—applied to key design and measurement stages: circuit topology and structure synthesis, circuit optimization, layout automation, and post-silicon calibration and fault diagnosis. By mapping these techniques to each phase of the analog and RFIC development pipeline, we identify emerging trends, persistent challenges such as generalization and data efficiency, and the trajectory toward fully autonomous, scalable, and innovation-driven analog/RFIC design. Beyond circuit design, this evolving ecosystem is also expected to reshape the broader Electronic Design Automation (EDA) landscape. This article serves as a comprehensive reference for academic researchers and industry practitioners seeking to leverage AI in next-generation circuit and system design.

INDEX TERMS Analog circuit design, radio frequency integrated circuits (RFIC), millimeter-wave (mmWave) circuits, machine learning (ML), reinforcement learning, electronic design automation.

I. INTRODUCTION

Historically, the design of analog and Radio Frequency Integrated Circuits (RFIC) has relied on expert intuition and a labor-intensive iterative refinement process [1]. Unlike digital circuits, which benefit from extensive automation, analog designs face greater challenges due to their continuous-signal nature and the sensitive trade-offs among multiple performance metrics [2]. Conventionally, this involves manual parameter tuning based on established methodologies, such as the g_m/I_D approach [3], followed by validation through computationally intensive SPICE and Electromagnetic (EM) simulations. This challenge is particularly severe for RF and mmWave circuits, where layout-dependent parasitic effects dominate performance and demand costly and time-consuming analysis [4], [5].

To address these challenges, Electronic Design Automation (EDA) has increasingly incorporated Artificial Intelligence (AI), following an evolutionary trajectory that is evident in publication trends over time (Fig. 1). Early efforts, prior to 2018, concentrated on foundational machine learning and optimization methods, such as evolutionary algorithms (EA) and Bayesian Optimization (BO), which improved efficiency in core tasks like circuit sizing [6], [7]. A major inflection point occurred around 2018 with the introduction of Deep Learning (DL) and Reinforcement Learning (RL). DL architectures, including Convolutional Neural Networks (CNNs) and Graph Neural Networks (GNNs), offer the ability to capture the highly complex, nonlinear relationships governing circuit behavior [8]. This capability has enabled automation of challenging RFIC designs, with recent studies successfully modeling high-frequency components that exhibit layout-dependent effects—previously considered intractable without expert intervention [9], [10]. Since 2023,

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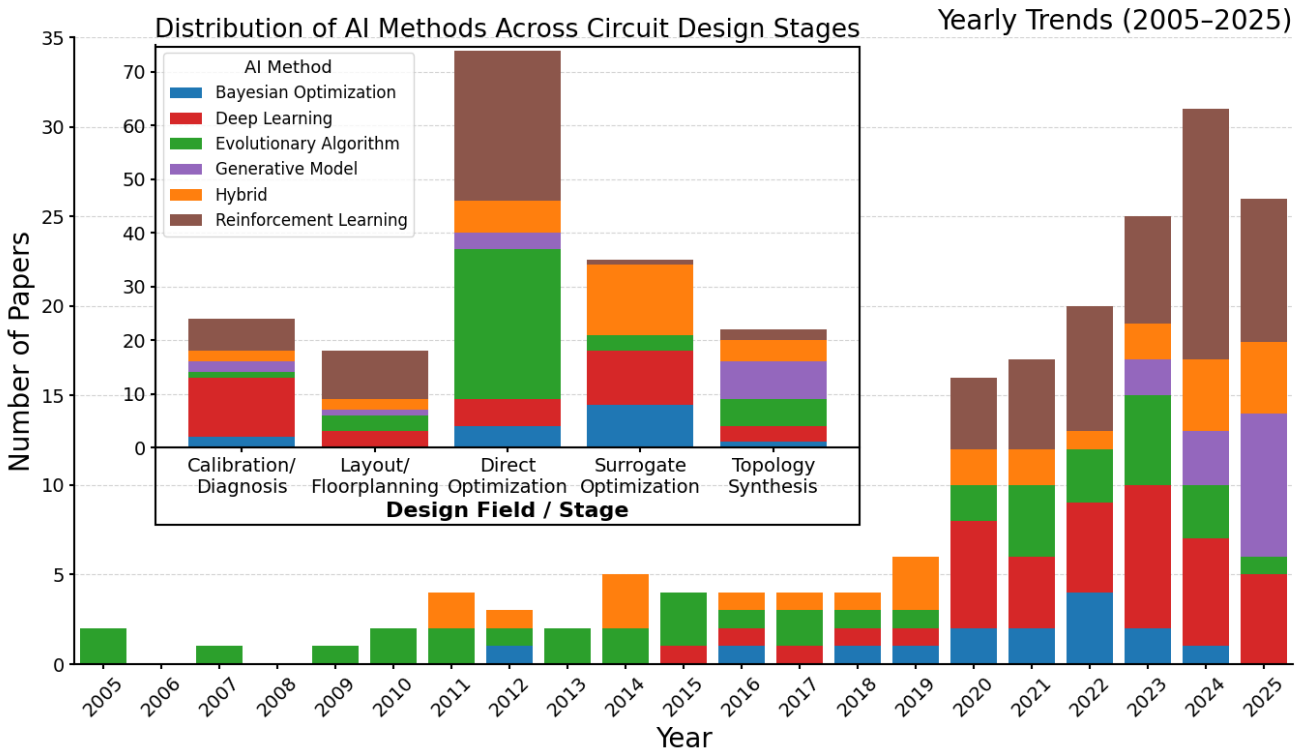

FIGURE 1. Evolution of AI methodologies across different stages of analog and RF circuit design, along with the overall publication trends over time.

this trend has accelerated further with a surge in publications driven by Generative AI, particularly large language models (LLMs).

With the capability of advanced AI models to manage such complexity, the vision for AI in EDA has expanded considerably. The objective has shifted from automating isolated tasks to developing intelligent systems that provide end-to-end design support. This new generation of AI-powered tools seeks to manage the entire workflow, functioning either as an AI co-pilot assisting human engineers or, ultimately, as an autonomous AI designer. The scope spans topology synthesis, initial sizing, and layout generation, extending through post-silicon stages such as automated testing and performance tuning [11], [12], [13], [14] (Fig. 1).

This survey provides a comprehensive overview of the ongoing transformation of circuit design enabled by AI. We trace the evolution of AI methodologies and their applications across the entire design pipeline, from core tasks such as optimization and layout to advanced topology synthesis. In addition, we assess the current state of the field by reviewing key datasets and outline future directions toward intelligent, end-to-end circuit design. The remainder of this survey is organized as follows and illustrated in Fig.2. Section II provides a comprehensive comparison with prior surveys in the field of AI and ML applications in analog and RF circuit design. Section III presents a concise overview of relevant AI methodologies applied in circuit design. Section IV presents AI-enhanced stages of the design workflow. Sections IV-A, IV-B, IV-C, and IV-D review AI applications in topology and structure synthesis, parameter optimization, layout automation, and testing/adaptation, respectively. Section V introduces an

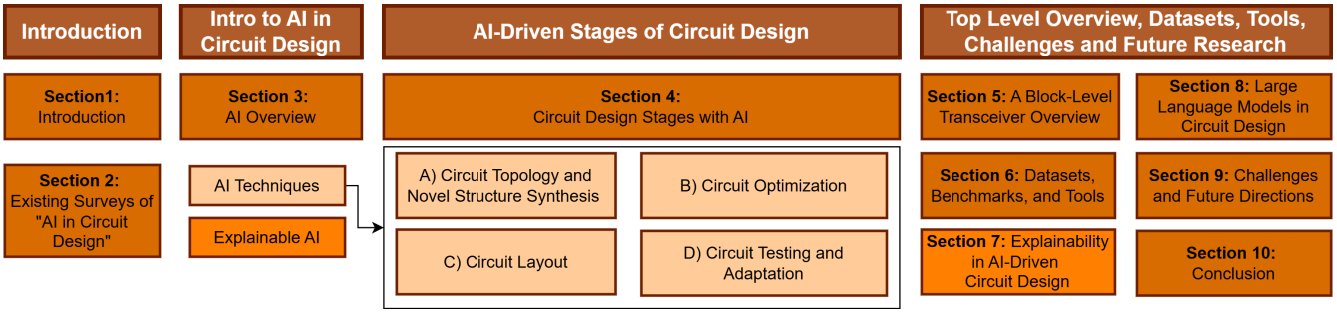

FIGURE 2. Overview of the survey.

RF/mmWave transceiver architecture annotated with AI-synthesized blocks, highlighting the potential for end-to-end AI-driven design. Section VI surveys open-source datasets, benchmarks, and tools supporting this domain. Section VII discusses explainability of AI models, while Section VIII explores the integration of large language models (LLMs) and conversational AI into the workflow. Section IX outlines key challenges and future research directions, and Section X concludes the paper.

II. SURVEYS OF AI APPLICATIONS IN CIRCUIT DESIGN

The rapid integration of AI into electronic design automation has prompted a growing body of literature aimed at surveying this dynamic field. Existing reviews provide valuable, though often specialized, perspectives on this evolution [14], [15], [16], [17], [18], [19], [20], [21], [22]. Some surveys focus on the application of a particular AI paradigm across the broader EDA landscape, such as those dedicated to reinforcement learning [18], graph neural networks [19], or the broader category of machine learning for EDA and FPGAs [21]. Afacan et al. [15] provide a broader overview that includes synthesis, layout, and test. Other works take an application-centric approach, reviewing various AI techniques within a specific domain, such as AMS design [16], general VLSI design [17], or antenna design [20].

More recently, with the increasing utilization of advanced generative techniques, researchers have delivered a systematic review of generative AI, including LLMs and GNNs, for analog IC design [14]. While these surveys are essential, they tend to either concentrate on a specific AI methodology or a subset of the design pipeline. Some surveys highlight innovations in physical design but do not offer a comprehensive, pipeline-wide analysis [22].

As detailed in Table 1, our work distinguishes itself by offering a structured analysis that connects algorithmic paradigms to specific engineering challenges. By synthesizing these diverse threads, we aim to provide not just a review of the state-of-the-art but also a clear roadmap toward the future of fully autonomous, AI-driven circuit design. The survey provides a holistic and forward-looking perspective, mapping the full spectrum of AI methodologies to each stage of the analog and RFIC design flow. Our key contributions are as follows:

- **Comprehensive Pipeline Analysis:** We provide an in-depth analysis of each stage in the analog and RFIC design pipeline, starting from topology synthesis and parameter optimization to layout and post-silicon tuning.
- **Focus on Emerging AI Paradigms:** We uniquely highlight the impact of LLMs and explainability, critical emerging technologies whose applications in circuit design have not been systematically reviewed before.
- **Design-Centric Organization:** Unlike prior surveys that are method-centric or limited in scope, our work organizes AI techniques around a practical and modular design flow. This design-stage-centric mapping enables circuit designers to identify the most relevant AI strategies for their current workflow.
- **Broad Comparative Analysis:** We compare a wide spectrum of AI techniques (evolutionary algorithms, deep learning, LLMs, etc.) to provide an actionable guide for practitioners.
- **Emphasis on Industry Adoption:** We address critical, yet underexplored, challenges to industry adoption, including the generalization of models across different process technologies and the explainability (XAI) of AI-driven design decisions.
- **Roadmap Toward Autonomy:** We synthesize the survey's findings into a high-level roadmap, outlining a tangible trajectory and key research opportunities for achieving fully autonomous, innovation-driven design.

TABLE 1. Comparison of our survey with selected prior review papers.

Feature/Scope	This	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]
Full analog/RFIC design pipeline coverage	✓	✓	✓	Partial	✗	Partial	Partial	✗	✗	Partial
AI technique comparison across paradigms (EA, BO, RL, DL, LLM)	✓	Partial	✓	Partial	✓	✗	✗	Partial	✓	✗
Inclusion of LLMs and generative AI	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗
Focus on analog-specific challenges (PDK, layout, post-silicon)	✓	✓	✓	✓	✗	Partial	Partial	✗	✗	✗
Discussion on generalization and data efficiency	✓	✓	Partial	Partial	Partial	✓	✓	✓	Partial	✗
Emphasis on explainability (XAI) in circuit design	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗
Coverage of layout automation and DRC-aware generation	✓	✓	✓	✗	✓	Partial	✓	✗	✓	✓
Coverage of fully autonomous design workflows	✓	✓	Partial	Partial	✓	✓	✓	Partial	Partial	✓
Special focus on RFIC or highfrequency design challenges	✓	Partial	✓	✓	✗	Partial	Partial	✗	✗	✗
Specific survey focus (e.g., RL, GNNs, antennas)	General	GenAI	Analog /RF	AMS	VLSI	RL	GNNs	Antennas	EDA	Phys. Dsgn.

III. AI OVERVIEW

AI encompasses a diverse range of methodologies that vary in how they search, learn, and reason from data. These techniques can be systematically classified along multiple dimensions: learning paradigm (e.g., deterministic algorithms, metaheuristic optimization, supervised, unsupervised, and reinforcement learning); data representation (e.g., scalar parameters, structured graphs, images); and architectural strategy (e.g., single-agent models, multi-agent systems, and meta-adaptive frameworks). A clear understanding of these categories is essential for mapping AI capabilities to the distinct challenges posed by analog and RFIC design, where design spaces are often non-convex, data is scarce or costly, and domain knowledge is deeply embedded in expert heuristics.

Table 2 categorizes the major AI techniques commonly applied in analog and RF circuit design based on their optimization paradigms and operational characteristics. Each method is evaluated along four key attributes: whether it is gradient-free, stochastic in nature, capable of model-based reasoning, and able to support sequential decision-making. These attributes influence the suitability of each method for specific circuit design tasks, such as parameter tuning, topology exploration, or layout synthesis. For example, gradient-free metaheuristic algorithms like Genetic Algorithm (GA) and Particle Swarm Optimization (PSO) are widely used for sizing due to their robustness to non-differentiable objectives. Surrogate-based methods, such as BO, offer strong performance in low-data regimes through model-based reasoning. RL stands out for its ability to handle sequential decisions, making it well-suited for layout routing or multi-step synthesis. This classification provides a conceptual map to guide practitioners in selecting appropriate AI strategies for different stages of the analog/RFIC design flow.

A. INTRO TO AI TECHNIQUES IN CIRCUIT DESIGN

1) DETERMINISTIC AND META-HEURISTIC OPTIMIZATION

Early efforts in circuit design automation primarily employed deterministic optimization techniques, such as geometric programming and constraint-based solvers. These methods are well-suited to problems that exhibit convexity and possess continuous, differentiable analytical models. However, analog and RF circuits typically involve high-dimensional, non-convex design spaces, often governed by complex device interactions and implicit constraints that violate these assumptions. In such settings, exhaustive parameter sweeps are computationally infeasible and rarely yield globally optimal solutions. To overcome these limitations, metaheuristic approaches—particularly GA [23] and multi-objective evolutionary algorithms (MOEAs) such as NSGA-II [24]—have gained widespread adoption. These techniques perform population-based, stochastic search and treat circuit simulators as closed box functions, relying solely on input–output evaluations without requiring analytical gradients or explicit internal models.

A typical GA begins by sampling an initial population of candidate solutions from the design space—such as circuit parameter vectors—and iteratively refines this population through evolutionary operators, primarily crossover and mutation. These operators facilitate exploration and exploitation by recombining and perturbing solutions across generations. In multi-objective optimization settings, GAs such as NSGA-II generate an approximated Pareto front of non-dominated solutions, where each solution represents a different trade-off among conflicting objectives (e.g., gain vs. power, linearity vs. area). Since these solutions form a set rather than a single optimum, researchers often apply multi-criteria decision-making (MCDM) techniques—such as weighted sum or analytic hierarchy process (AHP)—to select the most suitable design based on domain-specific priorities.

BO [25] is a sample-efficient global optimization framework that constructs probabilistic surrogate models—commonly Gaussian Process (GP), though neural networks or random forests may also be used to approximate the behavior of expensive closed box functions, such as circuit simulators. These surrogate models estimate both the expected performance and the uncertainty across the design space, enabling the use of acquisition functions

TABLE 2. Taxonomy of AI methods evaluated across key properties.

Category	Gradient-Free	Stochastic	Model-Based	Sequential Decisions	Example Methods
Deterministic Optimization	✗	✗	✗	✗	GP, SQP
Metaheuristic Optimization	✓	✓	✗	✗	GAs, NSGA-II, PSO
Surrogate-Based Optimization	✓	✓	✓	✗	GP, BNN, EI, UCB
Supervised Learning	✗	✗	✓	✗	MLPs, CNNs, GNNs
Unsupervised Learning	✗	✗	✓	✗	k-Means, VAEs, LLM Embeddings
Reinforcement Learning	Optional	✓	Optional	✓	DQN, PPO, TRPO, DDPG, SAC, QMIX, VDN

(e.g., Expected Improvement, Upper Confidence Bound) to balance exploration and exploitation during search. BO is effective when function evaluations are costly or limited, as is often the case in analog and RF circuit sizing. Due to its simplicity, data efficiency, and minimal reliance on gradient information, BO has become one of the most widely adopted techniques for performance-driven parameter optimization in this domain.

2) SUPERVISED LEARNING AND SURROGATE MODELING

Supervised learning is a subset of AI methods in which models are trained using labeled datasets. These models learn to approximate the output (label) of a new input by leveraging patterns extracted from existing data. Through backpropagation, supervised learning algorithms compute gradients across network layers to iteratively update model parameters, thereby capturing complex relationships within non-convex design spaces. High-capacity architectures—such as multi-layer perceptrons (MLPs) and CNNs—are particularly well-suited for processing high-dimensional inputs. These models are commonly trained to regress performance metrics (e.g., gain, power-added efficiency (PAE), and S-parameters) directly from circuit design variables.

CNNs are typically employed in scenarios where circuit design data exhibits spatial structure, such as layout images or metal–dielectric patterns in EM simulations. More recently, GNNs have been applied to circuit design problems involving high-dimensional data, such as netlists, where nodes correspond to components and edges represent electrical connectivity. GNNs learn message-passing functions across circuit topologies, enabling context-aware inference and improved generalization to unseen designs [26].

3) UNSUPERVISED LEARNING

Unsupervised learning models are employed to discover inherent structures and patterns within large-scale circuit datasets without reliance on pre-labeled examples. These methods are primarily used for design classification and dimensionality reduction. For instance, clustering algorithms can automatically group designs with similar performance characteristics or identify distinct fault signatures in post-silicon test data [27], as discussed in Section IV-D. This helps categorize failure modes or architectural families from raw data. Similarly, dimensionality reduction techniques can simplify the high-dimensional design spaces common in circuit sizing, as detailed in Section IV-B, making optimization tasks more computationally tractable. The insights and simplified representations derived from unsupervised methods often serve as an effective initialization mechanism for the supervised or reinforcement learning models [28] used in the subsequent stages of the design flow.

4) GENERATIVE MODELS AND REPRESENTATION LEARNING

Generative AI introduces a paradigm for creating novel data artifacts by learning the underlying distribution of a training dataset. This category includes Variational Autoencoders (VAEs), Generative Adversarial Networks (GANs), and Large Language Models (LLMs). VAEs create a compressed, continuous latent space that enables efficient design exploration and generation of new, valid circuit parameter sets [11]. GANs use adversarial training to produce highly realistic data and have been applied to tasks such as inverse design of passive components [29] and data augmentation to reduce simulation costs, as noted in Section IX. More recently, LLMs have proven powerful tools for representation learning, as discussed in Section VIII. By training on technical documents and code, LLMs build semantic embeddings that capture complex design knowledge [14]. This allows them to guide optimization algorithms, making the design search more efficient and intelligent [11]. The representations learned by generative models are increasingly used to initialize and guide other AI systems, such as reinforcement learning agents for sizing and layout automation.

5) REINFORCEMENT LEARNING

RL formulates the circuit design process as a sequential decision-making problem under uncertainty, typically represented as a Markov Decision Process (MDP). An RL agent learns a policy that maximizes cumulative reward by interacting with an environment, which is often defined by a circuit simulator or a surrogate model. Canonical algorithms in this domain include Deep Q-Networks (DQN) [30], Trust Region Policy Optimization (TRPO) [31], and Proximal Policy Optimization (PPO) [32]. For continuous action spaces—common in analog parameter tuning—actor–critic methods such as Deep Deterministic Policy Gradient (DDPG) [33] and Soft Actor–Critic (SAC) [34] have demonstrated effectiveness.

Deep reinforcement learning (DRL) algorithms leverage Deep Neural Networks (DNNs) to approximate policy or value functions, enabling learning in complex, high-dimensional design environments. These models are particularly effective when explicit modeling of system dynamics is infeasible or when search spaces are too large for tabular methods. DRL pipelines incorporate supervised pretraining to accelerate convergence and stabilize early-stage learning. In scenarios where the reward function is sparse or difficult to define, imitation learning [35] offers an alternative by learning policies directly from expert demonstrations.

Multi-agent reinforcement learning (MARL) extends the RL framework by decomposing design problems into subtasks handled by individual agents. MARL enables scalable coordination in complex circuit co-optimization or layout

planning scenarios. Cooperative algorithms—such as Value Decomposition Networks (VDN) [36] and QMIX [37]—facilitate decentralized learning by allowing agents to learn local policies while pursuing shared goals.

B. EXPLAINABLE AI

As AI models continue to grow in complexity, their interpretability diminishes, raising concerns about transparency and trustworthiness. To address this, Explainable AI (XAI) techniques have been developed to provide insights into the decision-making processes of these "closed box" systems [38]. Various XAI methods have emerged to interpret model outputs, each with differing applicability depending on the nature of the data and the AI architecture. The adopted approaches: SHapley Additive exPlanations (SHAP) [39], Local Interpretable Model-Agnostic Explanations (LIME) [40], Gradient-weighted Class Activation Mapping (Grad-CAM) [41] will be further discussed in Section VII.

IV. AI-DRIVEN STAGES OF CIRCUIT DESIGN AND MEASUREMENT

This section, along with Table 3, outlines AI integration across key phases of the circuit design pipeline, showing how AI techniques are progressively replacing traditional EDA methods. By leveraging AI across topology synthesis, parameter optimization, physical layout, and post-silicon operations, designers are increasingly empowered to overcome the inherent complexities of analog and RFIC development.

Circuit topology and structure synthesis involves the generation or selection of circuit architectures that satisfy specific functional requirements. Traditional methodologies often rely on the expertise of the designer and domain-specific heuristics. In contrast, AI-driven approaches have demonstrated the ability to uncover non-intuitive yet high-performing topologies that may surpass human-designed counterparts in terms of efficiency, compactness, and performance trade-offs [42], [49].

Circuit optimization involves fine-tuning transistor-level parameters, such as channel dimensions, bias currents, and passive element values, to meet performance specifications such as gain, bandwidth, noise figure, and power efficiency. In AI-assisted design flows, this stage is significantly enhanced through the use of surrogate modeling, which approximates complex device behavior to reduce simulation costs [166]. Moreover, inverse design methodologies, where AI maps high-level specifications directly to design parameters, have emerged as a powerful paradigm [9].

TABLE 3. AI/ML Techniques and applications in analog/RF circuit design and measurement.

Task Category	Conv. EDA Method	AI Methodologies	Citations
Circuit Topology and Novel Structure Synthesis	Schematic design, design-space exploration	Evolutionary Algorithms	[42]–[48]
		Reinforcement Learning	[49]–[53]
		Neural Networks (GNN, DNN)	[54]–[58]
		Framework based	[59]
Circuit Optimization	Constraint-driven design with manual / heuristic design space exploration, circuit sizing tools,	Evolutionary Algorithms (EA)	[6], [43], [45]–[47], [60]–[88]
		Reinforcement Learning (RL / DRL)	[26], [50], [89]–[114]
		Bayesian Optimization (BO)	[3], [7], [11], [115]–[128]
		Other Optimization Methods	[4], [46], [129]–[137]
Surrogate Modeling	Simulation	Neural Networks (ANN/DNN/CNN)	[5], [123], [138]–[161]
		Gaussian Processes (GP)	[121], [162]–[164]
		Space Mapping, Multi-Fidelity	[122], [165]–[169]
Inverse Design	EM simulations	Neural Networks (CNN, DNN, INN, GAN)	[9], [28], [29], [157], [170]–[175]
		Machine Learning (General)	[10], [176]–[178]
Symbolic Analysis	Network modeling	Symbolic Methods	[2], [179]–[181]
Circuit Layout	Layout generation, Floorplanning, DRC, LVS	Reinforcement Learning	[88], [182]–[189]
		Neural Networks (CNN, GNN, HyperGCN)	[8], [190]–[196]
Circuit Testing and Adaptation	Verification and measurement	Classification / Detection / Regression	[197]–[204]
		RL for Calibration / Self-healing	[13], [27], [205]–[208]
		XAI for fault segmentation	[209], [210]
Generative Design /Automation Frameworks	Interactive schematic design	Generative AI / LLMs	[11], [12], [14], [211]–[218]
		Integrated Systems / Benchmarks	[1], [10], [139], [219]–[232]

Circuit layout: Placement, and routing (P&R) constitutes the physical realization of a circuit schematic on silicon, where design decisions must account for parasitics, signal integrity, and compliance with design rules. Traditionally a bottleneck due to its complexity and interdependence with earlier design stages, AI has begun to revolutionize this domain by automating layout generation using graph-based models and reinforcement learning agents that learn from previous layouts and design patterns [191], [193].

Circuit testing and adaptation: Calibration, fault diagnosis, self-healing, and reliability assessment are crucial for ensuring post-fabrication correctness, yield optimization, and long-term robustness. AI models have been increasingly adopted to predict fault classification and localization, and to facilitate real-time calibration of process-sensitive blocks [13], [206].

These advancements represent a transformative shift from isolated optimizations to an integrated, intelligent design ecosystem. The following sections will delve into each of these AI-enhanced stages, providing a comprehensive analysis of the methodologies, applications, and challenges.

A. AI FOR CIRCUIT TOPOLOGY AND NOVEL STRUCTURE SYNTHESIS

AI is increasingly being applied to the ambitious task of topology synthesis, the automatic generation of novel circuit architectures from a set of basic components and design rules. This direction marks a significant advance toward end-to-end design automation, with the potential to discover circuit topologies that outperform human-designed counterparts in terms of performance, efficiency, or compactness.

Traditional analog circuit design is heavily based on established topologies that have been refined over decades. While template-based generators [219], [222] and procedural generators such as Berkeley Analog Generator (BAG) [139] automate the initialization and sizing of these known topologies, AI-driven topology synthesis aims to explore a much broader design space.

1) EVOLUTIONARY ALGORITHMS FOR TOPOLOGY GENERATION

Early approaches often utilized EA for topology generation. GA, a subset of EAs, is suitable, as it can evolve tree-like structures that represent circuits [42], [45]. In these systems, the ''genes'' can represent basic components (transistors, resistors, capacitors) and connections, and evolutionary operators (crossover, mutation) combine and modify these elements to create new circuit topologies. The fitness of each generated topology is typically evaluated through simulation against desired performance specifications.

McConaghy et al. [42] presented MOJITO, a GP-based system using hierarchical domain-specific building blocks to synthesize trustworthy analog topologies. Wu et al. [44] proposed an automated method for CMOS LNA topology generation and optimization using EAs. Zhou et al. [43] developed a system with a rule-guided GA for analog circuit design and optimization, which includes topological considerations. Muttoni and Veiga [46] introduced SANN-GCE, combining simulated annealing with geometric circuit evolution for both topology and sizing. Dastidar et al. [48] also explored evolutionary search with topological reuse.

2) REINFORCEMENT LEARNING FOR TOPOLOGY GENERATION

More recently, reinforcement learning has been applied to topology synthesis. The design process can be modeled as a sequential decision-making task where an RL agent learns to add components and connections to build a circuit. Zhao and Zhang [49], [50] demonstrated that a deep RL agent could learn to synthesize analog integrated circuit topologies, such as operational amplifiers, by sequentially selecting and connecting components. Their subsequent work also explored signal-division-aware topology synthesis aided by transfer learning [51], highlighting efforts to make these AI systems more generalizable. Hsu and Lin [52] used RL combined with building block classification for automatic analog schematic diagram generation.

GNNs are also playing a role, often in conjunction with RL or other generative models. Since circuits are naturally represented as graphs, GNNs can learn to understand, manipulate, and generate circuit graph structures. Dong et al. introduced CktGNN [54], a two-level GNN framework for simultaneous topology generation and device sizing, experimented on the Open Circuit Benchmark (OCB).

3) GENERATIVE MODELS FOR TOPOLOGY GENERATION

Generative Models, such as Generative Adversarial Networks (GANs) and diffusion models, are emerging as powerful tools. While their application to complex analog topology synthesis is still nascent, they hold promise for generating novel and diverse circuit structures. Zhang et al. [29] used GANs for the inverse design of impedance matching circuits, which involves generating component values that implicitly define a topology. Zadeh and Elamien [14] provide a review of generative AI methodologies, including diffusion models, for analog IC design, suggesting their potential for topology exploration.

4) DISCUSSION

The challenge in AI-driven topology synthesis is defining a suitable representation for circuits that allows for effective exploration and manipulation by AI algorithms. Managing the high-dimensional search space and ensuring that generated topologies are physically realizable and meet performance constraints are also significant hurdles. Furthermore, evaluating the novelty and practicality of AI-generated topologies requires rigorous simulation and comparison against established human designs.

The ultimate goal is to develop AI systems that can not only optimize existing designs but also discover entirely new circuit architectures that might offer superior performance, lower power consumption, or smaller area than currently known solutions, potentially leading to breakthroughs in analog and RFIC design [9], [42], [55].

B. AI FOR CIRCUIT OPTIMIZATION

One of the primary applications of AI in analog and RF design is the automation of circuit sizing—selecting component values such as transistor widths and lengths, bias currents, resistor and capacitor values, and inductor geometries to satisfy specified performance targets (e.g., gain, bandwidth, noise, linearity, power consumption, and efficiency) [15]. Traditionally, designers estimate initial values based on analytical calculations, heuristics, or prior designs, followed by iterative fine-tuning through simulation-based parameter sweeps. This process can be formulated as an optimization problem, as outlined in (1), and is typically characterized by a high-dimensional, non-convex design space, conflicting objectives, and computationally expensive function evaluations—often requiring SPICE-level circuit simulations or EM analysis [166]. AI techniques have been increasingly employed to improve the efficiency and robustness of this process, while reducing reliance on human intuition and manual design effort.

Circuit-sizing is especially critical and challenging in the RF and mmWave domains. At these high frequencies, performance is no longer solely dictated by transistor sizing but is dominated by a complex interplay of layout-dependent parasitics, electromagnetic (EM) coupling, and impedance matching [2]. For instance, in a mmWave transceiver, sizing the components of the Low-Noise Amplifier (LNA) [44], [65], Power Amplifier (PA) [89], [153], Voltage-Controlled Oscillator (VCO) [136] or mixer involves tuning potentially dozens of interacting parameters. AI-driven sizing aims to automate this search, often treating the circuit simulator (e.g., SPICE, Spectre) or EM simulator (e.g., HFSS, Momentum) as a closed box or an environment to be explored [63], [165].

Finding a solution that satisfies all design specifications is essentially an optimization problem, often multi-objective, which can be generally formulated as:

$$\begin{aligned} \underset{\mathbf{x}}{\text{maximize}} \quad & \text{FoM}(\mathbf{x}) = \mathbf{W}\mathbf{F}(\mathbf{x}) \\ \text{subject to} \quad & \mathbf{x}_{\min} \le \mathbf{x} \le \mathbf{x}_{\max} \\ & \text{Spec}_i^{\min} \le f_i(\mathbf{x}) \le \text{Spec}_i^{\max}, \quad \forall i \end{aligned} \tag{1}$$

Here, $\mathbf{x}$ denotes the vector of design variables (e.g., transistor width/length ratios, bias currents, and passive component dimensions). The vector $\mathbf{F}(\mathbf{x}) = [f_1(\mathbf{x}), \ldots, f_k(\mathbf{x})]$ represents the k objective functions to be optimized, such as maximizing gain or minimizing power consumption and noise figure. The multiplying vector $\mathbf{W} = [w_1, \ldots, w_k]$ represents the weight of each objective. These objective functions $f_i(\mathbf{x})$ are typically evaluated using circuit or EM simulators. The vectors $\mathbf{x}_{\min}$ and $\mathbf{x}_{\max}$ define the lower and upper bounds on the design variables, respectively. The objective is often to identify the Pareto-optimal front, which captures the best trade-offs among competing objectives [72], [84], [119]. In RFIC design, this front might represent the compromises between power-added efficiency (PAE) and linearity in a PA [89], [153], or phase noise and tuning range in a VCO [136]. In some cases, a scalar figure-of-merit (FoM) [26] is defined by applying weights to individual objectives, thereby converting the problem into a single-objective optimization formulation.

This optimization formulation serves as the foundation for many of the works reviewed in this survey [94], [100], [166], although the specific objectives, constraints, and optimization algorithms vary considerably. A representative optimization flow is illustrated in Figure 3. This section discusses both direct optimization approaches—which operate without surrogate models—and the role of surrogate-assisted optimization, highlighting their importance in reducing computational cost and improving sample efficiency across various baseline AI techniques.

The automation of analog circuit sizing and optimization has progressed significantly over the past few decades. Early efforts relied on symbolic analysis techniques to derive analytical expressions and gain design insight [179], [180], [181]. Prior to the widespread adoption of DL and RL, analog designers frequently employed EAs and BO to automate the sizing process. These approaches remain relevant and are often integrated with contemporary AI models. BO, in particular, is commonly used to construct surrogate models of circuit simulators, typically modeled as Gaussian processes. The overarching objective is to efficiently sample a set of design points that guide the optimization algorithm through the high-dimensional, non-convex design space.

1) EVOLUTIONARY AND BAYESIAN OPTIMIZATION

The 2010s witnessed a notable rise in the application of EAs and Swarm Intelligence (SI) techniques for analog circuit optimization. Prominent examples include GAs [6], [47], [60], PSO [62], [65], [66], [67], and Differential Evolution (DE) [68], [69]. Additionally, alternative meta-heuristic approaches—such as Firefly algorithms [73] and chaotic optimization methods [74]—were explored to address complex, non-convex design landscapes.

A significant body of work in this field focuses on improving sample efficiency to reduce the number of expensive simulations, particularly the full-wave EM simulations required for accurately modeling on-chip inductors, transformers, and matching networks at RF frequencies [5]. Liu et al. have proposed various surrogate modeling techniques that are both sample-efficient and adaptable to new circuit design problems [85], [145], [166]. Their recent work extends this line of research by incorporating Bayesian Neural Network (BNN)-based surrogate models into hybrid optimization algorithms, further improving adaptability and performance [153].

These works provide a foundation for ongoing developments aimed at improving optimization speed and accuracy. However, a common limitation is the lack of adaptability to other circuit types or process technologies. Surrogate models are typically constructed with a fixed input–output mapping, making them incompatible with varying topologies or device models; in many cases, the trained parameters do not generalize well across different design scenarios. This challenge has motivated researchers to explore more flexible AI techniques that enhance exploration and training efficiency. Recent advances—including in-context learning with LLMs and BNN-based surrogates—demonstrate improved adaptability to new specifications and enhanced performance on emerging technologies [11], [153].

2) REINFORCEMENT LEARNING BASED OPTIMIZERS

RL offers an alternative paradigm, framing circuit sizing as a sequential decision-making policy [107]. In this framework, an RL agent interacts with a circuit simulator—treated as the environment—by iteratively adjusting design parameters (actions) based on the current circuit state and observed performance feedback (rewards). The agent aims to learn a policy that maximizes the cumulative reward, typically aligned with meeting or exceeding design specifications [91], [94].

Two primary advantages of RL in circuit design are its ability to learn generalizable strategies and its flexibility to incorporate domain knowledge through reward shaping and state encoding. AutoCkt is a DRL framework that introduces a subsampling technique to efficiently explore large design spaces [94]. Building on this work, Wang et al. integrated GNNs with RL in the GCN-RL framework [26]. By representing the circuit as a graph, the GNN enables the RL agent to extract structural features that are transferable across different circuit topologies and technology nodes. This capability significantly improves design porting and reduces the need for retraining from scratch. Such transfer learning approaches are increasingly important for enhancing computational efficiency and design reusability [51], [221].

Recent advances in RL for circuit design have focused on improving sample efficiency and robustness. One commonly encountered challenge is model initialization, as poorly initialized weights can delay learning and lead the RL agent to waste computational resources discovering basic patterns that traditional optimizers can identify more directly. To address this, Gao et al. proposed RoSE [101] and its extension RoSE-Opt [100], which integrate BO for efficient initial exploration with RL for fine-tuning. This hybrid approach achieves more robust optimization with fewer simulation evaluations. Their results demonstrate that combining the strengths of multiple algorithms yields advantages. In parallel, Shi et al. introduced RobustAnalog [102], which employs multi-task RL to design circuits resilient to process, voltage, and temperature (PVT) variations. Additionally, curiosity-driven RL has been proposed to improve exploration in sparse-reward environments, as demonstrated by Yamamoto and Takai in GNN-Curio [95].

MARL is an emerging approach for tackling complex system-level design tasks in analog and RF circuits. Bao et al. [97] and Zhang et al. [96] developed MARL frameworks in which multiple agents concurrently optimize different sub-blocks—such as the LNA, PA or VCO within a Phase-Locked Loop (PLL)—thereby reducing design complexity

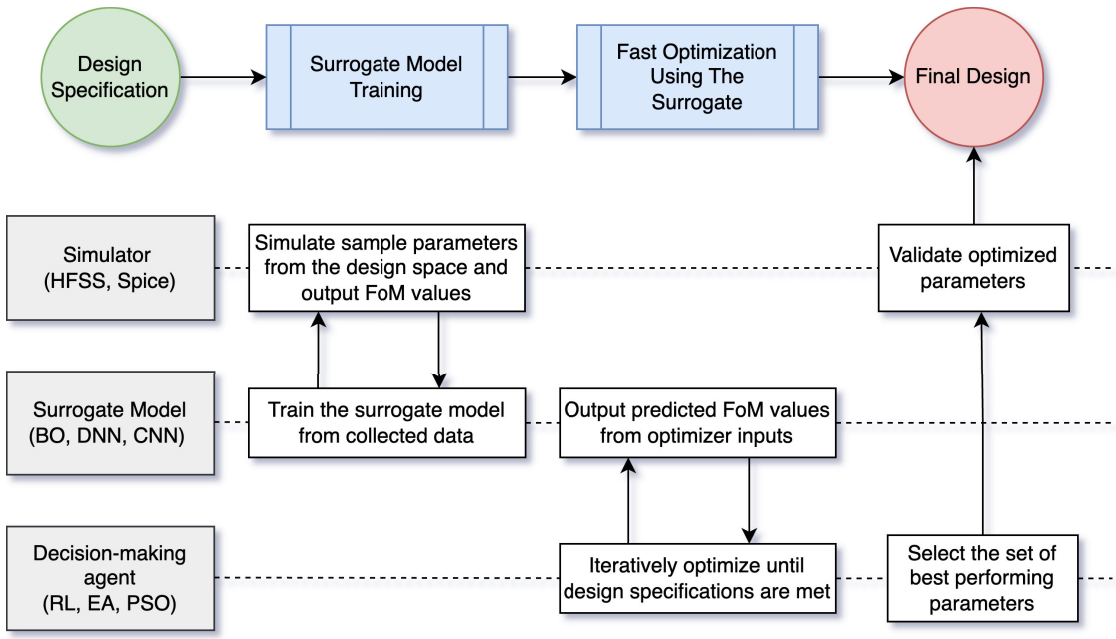

FIGURE 3. General optimization flow of a surrogation process.

through task decomposition. MA-Opt [98] extends this concept by deploying multiple actors to explore the same optimization problem in parallel, accelerating convergence through diverse policy exploration. This design philosophy resembles a mixture-of-experts (MoE) architecture, where a generalized model is composed of specialized sub-models, each responsible for a specific part of the system.

3) DEEP LEARNING SURROGATES AND GRADIENT-BASED OPTIMIZATION

While BO typically relies on surrogate models such as GP [121], [162], [164], an alternative strategy leverages DL techniques for surrogate modeling. Instead of probabilistic GPs, high-capacity neural architectures such as Artificial Neural Networks (ANNs), DNNs, CNNs, and GNNs are trained to act as fast, deterministic emulators of complex circuit simulators (e.g., SPICE) or EM solvers [142], [143], [220]. The core idea, illustrated in the workflow diagram in Figure 3, involves an upfront computational investment to train an accurate surrogate model using data generated from a limited number of high-fidelity simulations.

Once trained, this DL surrogate can predict performance metrics (e.g., gain, bandwidth, S-parameters, PAE) based on input design parameters significantly faster than the original simulator [138], [140], [170]. This acceleration is crucial for design space exploration, especially when the surrogate is integrated with optimization algorithms such as EAs [140], [141], BO [123], [153], or RL [143]. Solutions identified as promising by the surrogate are then validated using the original simulator to confirm performance and potentially refine the surrogate model. Researchers apply this concept as offline and online surrogates, depending on whether the model is pre-trained or trained in-the-loop [144], [145], [150].

An important potential benefit of neural network surrogates over treating original simulators as closed boxes is their differentiability. If the neural network surrogate accurately models the input-output relationship, its gradients with respect to the design parameters can often be computed efficiently using backpropagation. This characteristic allows for the application of efficient gradient-based optimization methods [129], which might not be feasible with the original non-differentiable simulator environment.

4) INVERSE DESIGN OF RF PASSIVES AND COMPONENTS

Distinct from the forward modeling approach where performance is predicted based on a given structure, AI techniques facilitate effective *inverse design* methodologies. This is particularly relevant for the synthesis of passive RF and microwave components where performance is dictated by their passive components—matching networks, filters, and baluns—whose optimal geometries are often non-intuitive and difficult to derive analytically [15], [16]. Instead of optimizing the parameters of a predefined geometry (e.g., width and spacing of a inductor), inverse design aims to determine the necessary physical structure or component values required to achieve a specific set of desired performance characteristics (e.g., target S-parameters, impedance, or radiation patterns) [173]. This approach reframes the design challenge, moving directly from functional requirements to physical implementation.

This methodology is highly applicable to components where electromagnetic performance is strongly dictated by physical geometry, including antennas [20], [157], filters [174], [175], matching networks [29], couplers [177], transformers [172], and various other passive EM structures [9]. Traditional design methods for these components often depend on analytical models for standard shapes or involve labor-intensive iterative optimization using EM simulators over a restricted parameter set. AI-based inverse design seeks to automate much of this iterative process by learning a direct mapping from the performance domain back to the design domain (geometry or parameters).

Significant work in this area has been conducted [9], [28], [170], [171]. They utilize deep learning techniques, primarily CNNs, often integrated with generative models or optimization algorithms (such as GAs or PSO), to enable the inverse design of complex, often arbitrary-shaped, high-frequency passive structures, including their co-design with active circuitry like PAs. Their typical workflow involves training a fast CNN surrogate model capable of accurately predicting EM performance from a geometric representation (e.g., a pixel map indicating metallization). This forward surrogate model is then embedded within an optimization framework. The optimizer searches the space of possible geometries, using the surrogate for rapid evaluation, to identify a structure whose predicted performance closely matches the target specifications. The speed of the CNN surrogate allows the exploration of a very large design space, potentially discovering unconventional yet high-performing geometries within practical timeframes [9]. They also leverage transfer learning effectively to adapt pre-trained models to new design contexts (e.g., different substrates or frequency bands) with minimal additional simulation data.

Generating sufficient training data is often a challenge; domain-specific data augmentation strategies, such as the physical multi-port decomposition are methodologies for data augmentation for maximizing the information extracted from limited simulation runs [9]. A multi-port decomposition process computes S-matrices for a large circuit and decomposes the resulting S-parameters into two-port matrices. This approach substancially reduces the simulation times required for simulating equivalent amount of two-port circuits.

Other AI methodologies have also been explored for inverse design tasks. Invertible Neural Networks (INNs) provide a structure capable of learning both forward and inverse mappings within a single model [174]. Inverse ANNs [157] and GANs [29] have been employed to directly generate design parameters or geometric descriptions from target performance specifications. General ML models have also been specifically trained to automate the synthesis of components such as baluns [176] and couplers [177]. Toolboxes designed for component synthesis, such as PACOSYT [10], often

encapsulate ML surrogate models coupled with optimization algorithms to provide users with component geometries based on desired electrical characteristics.

5) DISCUSSION

Despite significant progress, challenges remain. While BO and DL surrogates aim to reduce simulation calls, their effectiveness can vary. Robustness across PVT variations is another concern, addressed by works like RobustAnalog [102]. The generalization of learned policies or models to new circuit topologies or technologies without extensive retraining is also a problem, though transfer learning approaches show promise [26]. Effectively handling multiple conflicting objectives (e.g., gain vs. power vs. noise) within AI frameworks continues to be an active research area as RL models are not directly designed for multi-objective problems.

A significant limitation of many current AI sizing tools is their focus on schematic-level optimization. For RFICs, this ''layout-unaware'' approach is particularly problematic. Performance metrics such as gain, impedance matching, and stability are critically dependent on layout parasitics, which can completely invalidate a seemingly optimal schematic design [170].

Future work must therefore focus on AI frameworks that tightly couple schematic sizing with physical layout generation. This could involve RL agents that learn to co-optimize transistor dimensions and placement simultaneously, or the integration of fast, GNN-based parasitic predictors [190] directly into the optimization loop to provide layout-aware feedback at design time. Hybrid approaches combining the strengths of different AI paradigms, such as BO with RL [100], [101], or LLMs with BO [11] can lead to more stable and reproducible solutions.

C. AI FOR CIRCUIT LAYOUT

Automated circuit layout, consisting of floorplanning, placement, and routing, is another critical area where AI is demonstrating significant potential. The physical arrangement of components in an analog or RFIC influences its performance, primarily due to parasitic effects, signal coupling, and thermal considerations [4]. Efficient arrangement requires considerations such as symmetry constraints, minimizing offsets, and managing signal path integrity to avoid crosstalk [2]. Furthermore, any AI-generated layout must adhere to manufacturability requirements, ensuring they are DRC (Design Rule Check) clean and LVS (Layout Versus Schematic) correct.

Traditionally, this has been a labor-intensive process, heavily reliant on designer expertise (as shown in Table 4), particularly for sensitive analog circuits where symmetry, matching, and signal path integrity have a greater impact on performance. AI-driven approaches aim to automate this complex, high-dimensional search problem. Similarly to digital place-and-route, the problem can be framed as finding an optimal arrangement of circuit blocks (macros) and individual devices (standard cells or transistors) that minimizes a cost function, which includes wirelength, area, and performance metrics derived from post-layout parasitic estimations [188], [189].

1) REINFORCEMENT LEARNING FOR LAYOUT AUTOMATION

Following its successful application in circuit optimization, reinforcement learning has been applied to placement tasks. Mirhoseini et al. demonstrated a GNN-based RL agent for macro placement in digital designs, outperforming humans [193]. Transferring this to analog layout presents challenges —such as complex constraints and continuous variables—but models are adapting. Recent work explores RL for analog and mixed-signal placement, focusing on optimizing symmetry, routability, and performance metrics [182], [183], [185]. An RL agent can learn to sequentially place components, receiving rewards based on layout quality or simulation feedback. He et al. explored Monte Carlo Tree Search with deep RL for circuit routing, relevant to analog routing [184]. Wang et al. proposed RTplace, an RL-based macro placement method using ResNet and Transformer architectures, showcasing advanced neural networks for spatial optimization [195].

2) GRAPH NEURAL NETWORKS FOR LAYOUT AUTOMATION

GNNs are well-suited for layout problems, as circuits naturally lend themselves to graph representations (components

TABLE 4. Traditional vs. AI-driven layout to GDSII.

Layout Stage & I/O	Traditional Flow (Process)	AI-Driven Flow (Process & Refs)
Floorplanning *I: Netlist, Rules* *O: Initial Placed Layout*	Manual block setup; iterative refinement.	Automated global placement via RL/GNNs. [183], [186], [193]–[195]
Detailed Placement *I: Initial Place* *O: Optimized Placed Layout*	Manual/scripted cell adjustments	RL/DL/Meta-heuristics for precise positioning and constraint handling. [185], [192], [225]
Routing (Global/Detail) *I: Placed Layout, Nets* *O: Routed Layout*	Algorithmic; manual and iterative.	DRL for smart pathfinding; ML predicts congestion; GNNs for routing-aware placement. [88], [182], [184], [189], [225]
Post-Route Opt. *I: Routed Layout* *O: Final Layout*	Manual fixes (timing, noise); rule-based detailing.	ML predicts parasitic impacts for optimization; RL for post-layout tuning. [8], [104], [139], [188]
Verification (DRC/LVS) & GDSII Gen. *I: Final Layout, Rules, Schematic* *O: GDSII / Errors*	Tool-run checks; manual error debug; GDSII export.	ML aids error analysis/prediction; AI-guided debug; automated GDSII from high-level specs. [88], [185], [191], [211], [213]

as nodes, connections as edges). GNNs can learn to extract features from the circuit netlist and current placement state to guide the optimization process. For example, GNNs can predict post-layout parasitics from a pre-layout netlist and initial placement, providing rapid feedback to an optimizer [8], [190]. Chen et al. developed MAGICAL, an open-source, fully automated analog IC layout system that incorporates GNNs [191]. Guan et al. proposed a Transformer-characterized approach using HyperGCN and Deep Transformer Q-Networks (DTQN) for chip floorplanning [194], indicating a trend towards more sophisticated GNN architectures. Li et al. customized a GNN model specifically for guiding analog IC placement, demonstrating superior accuracy and knowledge transfer compared to CNN-based methods and standard GNNs [192]. Basso et al. have explored relational GNNs combined with RL for effective analog IC floorplanning [186] and further enhanced RL floorplanning with beam search techniques [187].

A general workflow for a GNN-assisted layout predictor is illustrated in Figure 4. In this framework, the message parsers—responsible for learning spatial and topological dependencies—can range from DNNs to more advanced GNNs and transformer-based architectures tailored for graph-structured data. These models capture intricate relationships between layout components (e.g., transistors, wires, and parasitics) and enable efficient feature propagation across the circuit graph. The integration of such parsers enhances the model's capacity to infer layout constraints, predict design rule violations, or estimate parasitic effects, all of which are critical for layout optimization in modern analog and mixed-signal design flows.

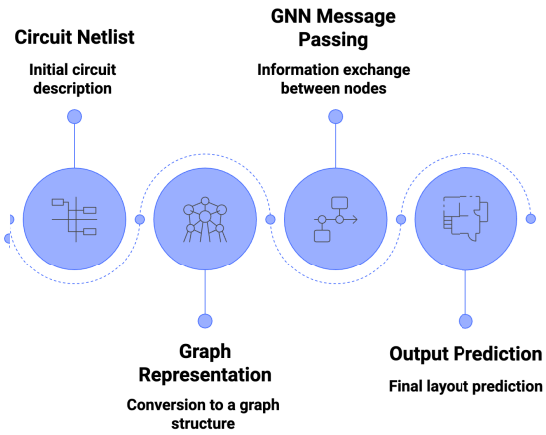

FIGURE 4. A sample workflow for a GNN-assisted layout generator.

3) DISCUSSION

A significant challenge in AI-driven analog layout is the tight coupling between placement, routing, and performance. Unlike digital design, where wirelength is a primary proxy for timing, analog performance is a complex function of many layout-dependent effects. Future AI methodologies will need to integrate these considerations more deeply, potentially through AI agents that simultaneously consider schematic parameters and physical layout and generative models (e.g., GANs, diffusion models) capable of producing complete, high-quality layouts from specifications or schematics.

The MAGICAL framework [191] and the open-source AMS circuit optimization framework by Li and Chan Carusone [104] are steps towards more integrated solutions that bridge the gap from specifications to GDSII. As AI techniques for layout mature, they promise to significantly reduce the manual effort involved in this critical design stage, particularly for complex analog and RFICs where achieving optimal performance is highly dependent on the physical implementation.

D. AI FOR CIRCUIT TESTING AND ADAPTATION

The integration of AI in the lifecycle of integrated circuits extends significantly beyond the pre-silicon design phases. Post-silicon activities, including performance calibration, fault diagnosis, and the implementation of self-healing mechanisms, are increasingly benefiting from AI methodologies. These applications are critical to improving manufacturing yield, ensuring operational reliability, and reducing the long-term maintenance costs of complex analog and RFICs.

Modern analog/RF SoCs seldom meet data-sheet limits at first power-up: Process spread, supply noise and temperature drift translate into gain/offset shifts, timing skew or outright functional failures. AI calibration replaces time-consuming trim loops and rule-based look-up tables with on-chip learning engines that (i) sense deviations, (ii) infer optimal correction vectors and (iii) apply trims continuously or on demand.

1) AI-DRIVEN CIRCUIT CALIBRATION AND TUNING

Fabricated integrated circuits exhibit deviations from their nominal design specifications due to inherent process variations, as well as fluctuations in operating PVT. Component mismatches further contribute to this performance spread. Circuit calibration aims to compensate for these variations by adjusting configurable on-chip parameters post-fabrication. AI techniques, primarily deep learning and reinforcement learning, are effective in automating this tuning process.

2) REINFORCEMENT LEARNING FOR CALIBRATION

Reinforcement learning agents can be trained to learn optimal calibration policies by interacting with the physical chip or a digital twin. These agents adjust tunable elements, such as bias currents, capacitor banks, or phase shifters, to steer circuit performance metrics into desired operational ranges [13]. For example, RL has been applied to generate optimal stimuli for IC design verification, which can be extended to characterization and calibration tasks [27], [205]. On-chip learning for self-correcting systems, such as ADCs, has been demonstrated using RL principles [206]. Supervised machine learning models, trained on pre-silicon simulation data (incorporating detailed variation models)

or on characterization data from initial silicon wafers, can predict optimal calibration settings for new, uncalibrated chips, ensuring robust performance [208]. These AI-driven calibration approaches can lead to substantial reductions in production test time.

3) MACHINE LEARNING IN FAULT DIAGNOSIS AND DEFECT LOCALIZATION

Machine learning models, including Support Vector Machines (SVMs), decision trees, and diverse neural network architectures (e.g., ANNs, CNNs), can be trained on datasets comprising test responses from both faulty and fault-free circuit instances. These models learn to classify different types of faults such as stuck-at faults, open or short circuits, and subtle parametric deviations or to identify anomalous electrical behavior. For example, 1-D CNNs have been utilized for data-driven feature extraction in analog circuit fault diagnosis [198]. Other approaches include statistical property feature extraction using techniques like the Fractional Fourier Transform (FRFT) [197], and methods based on Support Vector Data Description (SVDD) combined with Dempster-Shafer evidence theory for modular analog circuits [199]. Dynamic Bayesian networks have also been explored for circuit fault localization [204]. More recent advancements feature methods using relevance vector machines [202] and neural network architectures, such as LightGBM with Boruta feature selection, for diagnosing soft faults in analog circuits [200], [201].

4) ADVANCEMENTS TOWARDS SELF-HEALING CIRCUITS WITH AI

The concept of self-healing or self-repairing circuits, in which a system can autonomously detect, diagnose, and recover from internal faults or significant performance degradation, represents a frontier application of AI in hardware systems. Although this field is still maturing, AI provides the core intelligence required for such adaptive systems. A self-healing circuit architecture would need to integrate several key components:

- On-chip sensors for continuous monitoring of critical performance parameters and health indicators.
- AI-based fault detection and diagnosis units to promptly identify the occurrence and nature of a fault [198], [199].
- An AI decision-making engine, potentially an RL agent or a sophisticated rule-based system, to determine the most appropriate corrective action [206].
- Reconfigurable hardware elements that can be dynamically adjusted, or signal paths that can be rerouted, to compensate for the fault or bypass the compromised section of the circuit.

Frameworks incorporating robust calibration and supervised machine learning serve as foundational elements for digitally-assisted self-healing functionalities in RFICs [208]. Such frameworks are summarized in Figure 5. Although achieving fully autonomous self-healing across a comprehensive range of fault types remains a long-term objective, AI techniques are enabling substantial progress in constructing circuits with enhanced resilience and adaptive capabilities, thereby contributing to overall system reliability and extended operational longevity [206].

5) DISCUSSION

The integration of AI into the post-silicon lifecycle of integrated circuits represents a significant paradigm shift. AI-driven calibration is already revolutionizing performance tuning [13], [27], [205], [206], [208], and machine learning models are utilized for fault diagnosis and defect localization [197], [198], [199], [200], [201], [202], [204]. While fully autonomous self-healing circuits remain a long-term goal, AI provides the core intelligence for systems to detect, diagnose, and initiate recovery from performance degradation or faults [206].

Future research must focus on delivering a complete self-healing pipeline with a focus on data efficiency and privacy. Furthermore, integrating on-chip AI accelerators could enable faster, more localized, and more energy-efficient self-correction capabilities. As chip designs grow in complexity, especially with multi-die assemblies, AI will be essential for developing system-level diagnostic and self-healing strategies across heterogeneous components. These advancements are vital for boosting manufacturing yield, ensuring operational reliability, and significantly reducing maintenance costs in future IC systems.

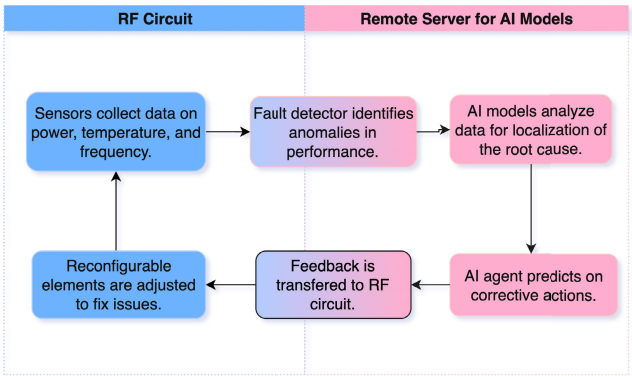

FIGURE 5. AI-driven self-healing RFIC cycle.

V. A BLOCK-LEVEL OVERVIEW

To contextualize the surveyed AI methodologies within a practical system framework, Figure 4 illustrates a representative RF/mmWave transceiver architecture annotated with circuit blocks that have been synthesized or optimized using AI techniques. Each active block—such as the PA, LNA, PLL, mixer, variable gain amplifier (VGA), analog-to-digital converter (ADC), digital-to-analog converter (DAC), low-dropout regulator (LDO), current conveyor (CC)—as well as each passive block—such as the antenna, filter, inductor, matching network (MN), and directional coupler (DC)—is linked to relevant literature in Table 5, where AI has been

successfully applied to the corresponding design task. This figure serves as a unifying visual summary, highlighting the extent to which AI has penetrated the analog/RF design pipeline at the block level. It also underscores the growing potential for end-to-end AI-driven transceiver design, where individual block-level innovations may be composed into fully synthesized system architectures.

This system-level perspective helps identify not only the maturity of AI techniques across blocks but also critical integration challenges. For example, while AI-driven optimization has shown promise in LNA and PA design, automated co-design of blocks with cross-domain constraints (e.g., linearity, noise figure, power consumption) remains largely unexplored. Addressing these integration-level issues will be essential for scalable, holistic design methodologies.

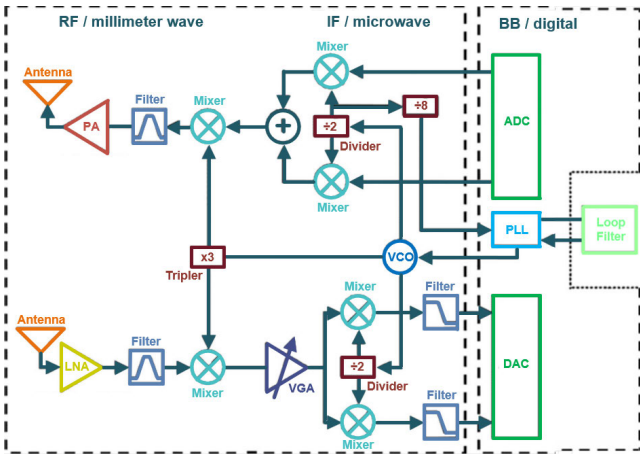

FIGURE 6. A mmWave Transceiver with annotated RF, IF, BB circuit blocks.

TABLE 5. Classification of papers by RF transceiver component.

LNA	[44], [65], [88], [168]
PA	[28], [89], [151], [153], [166], [170], [171], [228]
PLL	[4], [43], [48], [70], [136], [137], [164], [190], [223]
Filter	[60], [174], [175]
Antenna	[150], [154]–[157]
MNs	[9], [29], [170], [171]
Inductor	[5], [10], [165], [168], [169], [172], [178]
DACs	[61], [86], [112], [230]
ADCs	[97], [104], [230]
VGA	[118], [207]
Coupl.	[113], [177]
LDO	[3], [117]
CC	[63], [78]
Comp.	[47], [142]

VI. DATASETS, BENCHMARKS, AND TOOLS

The progress of AI-based methods in analog and RFIC design depend significantly on the availability of high-quality datasets, standardized benchmarks, and accessible software tools. These elements are fundamental for training models, comparing different algorithms, and supporting reproducible research.

A. DATA COLLECTION METHODOLOGIES

One of the fundamental challenges in applying AI to analog and mixed-signal circuit design lies in data acquisition, as generating high-quality, simulation-based datasets often demands significant computational resources [26], [139]. Historically, such datasets have been created in a problem-specific manner and rarely shared publicly, restricting reproducibility and slowing community-wide progress. However, a recent shift toward open-source datasets aims to overcome this limitation. Notable contributions include the OCB, which provides diverse operational amplifier designs [54], as well as datasets focused on specialized domains, such as antenna design via deep learning techniques [20]. The CIRCUIT benchmark was recently introduced to assess LLM reasoning in analog design tasks [229]. Nevertheless, the generation of datasets with broad topological and technological coverage remains constrained by high simulation costs. AICircuit [230] has addressed this partially by releasing reusable circuit templates—such as for LNAs and PAs—intended to support downstream design tasks.

In parallel, researchers benchmark their AI models against prior literature or expert-designed circuits on a per-case basis [26], [94]. While some efforts have introduced standardized evaluation protocols for specific algorithm classes—such as test suites for multi-objective evolutionary algorithms (MOEAs) [72] or supervised learning benchmarks for analog/RF regression tasks [231]—there remains no universally adopted benchmarking standard for analog AI design. To address this, Figure 7 presents a comparative analysis of eleven representative AI-based circuit design methodologies that leverage foundry-grade tool Cadence [232].

This binary heatmap provides a structured overview across seven key capability dimensions: topology selection, parameter inference, performance prediction, layout awareness, RF/mm-Wave applicability, and the availability of public datasets and codebases. The selected databases include GCN-RL [26], domain knowledge-based dataset [87], BO-SPGP [7], ESSAB [142], AICircuit [230], ALIGN [189], LayoutCopilot [214], AutoCKT [94], L2DC [107], CAN-RL [114], and FALCON [232].

Each cell denotes whether a method incorporates a specific feature (✓ = 1, ✗ = 0). Among the surveyed approaches, the FALCON framework and dataset stands out for fully supporting all seven dimensions, reflecting its comprehensiveness and practical utility. In contrast, most other methods remain specialized; for instance, BO-SPGP and ESSAB focus on sizing and performance estimation but lack layout integration and open-source dissemination. Layout-aware tools such as ALIGN and CAN-RL incorporate foundry-compatible design flows but differ in their public accessibility. This comparison underscores the broader challenges in the field, particularly the scarcity of open data/code resources and the limited support for topology generation and performance prediction across many state-of-the-art methods.

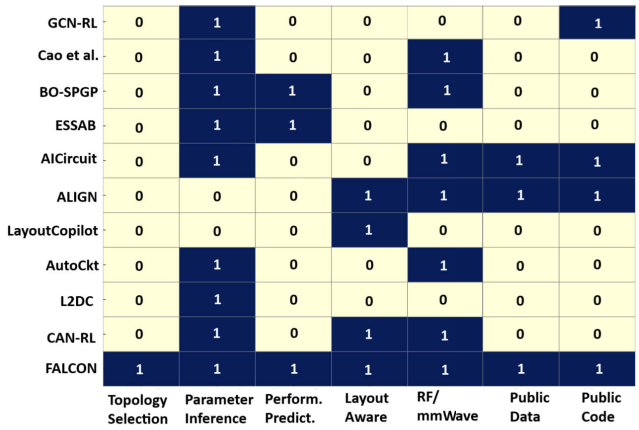

FIGURE 7. A qualitative comparison and capabilities of the datasets.

B. TOOLS AND FRAMEWORKS

The application of AI in circuit design is supported by various tools and frameworks. General-purpose AI/ML libraries such as TensorFlow [233] and PyTorch [234] are at the core of most development. Circuit simulators such as SPICE-like programs (e.g., HSPICE, Spectre, Ngspice) and EM simulators (e.g., HFSS, ADS Momentum) are commonly used for data generation and design validation.

Optimization frameworks that combine AI algorithms with circuit simulators: RL-based AMS circuit optimization framework [104], AutoCkt [94], and GCN-RL [26] are commonly referenced by recent publications and provide a baseline for development. Layout automation systems such as MAGICAL offer netlist-to-GDSII generation using AI techniques [191]. Tools such as PACOSYT [10] and SIDe-O [178] focus on synthesizing passive components with ML models. Generative design platforms such as the BAG [139] are being augmented with AI/ML, alongside other specialized synthesis tools [59], [146], [220].

C. DISCUSSION

The availability of open-source datasets and benchmarks is crucial for the evolution of AI in analog/RF design. While there are valuable contributions, the field still awaits more comprehensive and widely adopted benchmark suites to allow for consistent comparison of emerging AI techniques. As for AI-driven tools, many presented in academic literature are often tailored to solve specific problems or optimize particular circuit topologies and device types. This specialization can make it difficult to establish broad citation trends or direct applicability across the wide spectrum of analog design challenges.

VII. EXPLAINABILITY IN AI-DRIVEN CIRCUIT DESIGN

As AI models are used for increasingly complex tasks in circuit design, the evolution towards sophisticated, non-interpretable ‘‘closed box’’ methodologies presents a significant problem. XAI has emerged as a critical field, providing the tools necessary to improve the interpretability and tunability of these advanced models, transforming them from inscrutable models into transparent design partners.

Several XAI techniques have been adapted for use in circuit-related applications. One widely adopted approach is SHAP, which offers a game-theoretic framework for assigning importance scores to input features based on their contribution to a specific prediction [39]. LIME is another prominent technique that approximates the behavior of a complex model locally around a specific prediction using a simpler surrogate model, such as a linear regressor [40]. For CNNs, which are often employed in tasks such as layout analysis and inverse design, Grad-CAM is a powerful XAI method that produces class-specific localization maps [41]. Grad-CAM leverages the gradients of a target concept flowing into the final convolutional layer to generate heatmaps that highlight the most influential regions of the input image.

A. XAI-BASED CIRCUIT ANALYSIS

The main application of these XAI methods in circuit design today is to validate the decision-making process of AI models used for analysis and verification. A recent example is in the domain of semiconductor fault detection, where AI is used to identify microscopic defects on wafer maps [209]. By applying Grad-CAM and LIME, researchers were able to generate heatmaps over wafer images, visually confirming that the AI correctly focused on the physical regions of a defect when making a classification. Another application focused on classifying reasons of failure in microwave networks [210] that also uses Grad-CAM. This usability is a step towards industry adoption, as it allows domain experts to audit the AI’s reasoning, build confidence in the system, and ensure that the model has learned genuine fault characteristics rather than non-interpretable weights from the data.

B. DISCUSSION

The integration of XAI into IC design automation marks a pivotal shift from simply achieving results to understanding the reasoning behind them. This transition is not only an academic exercise; it is increasingly driven by the need for trust, validation, and regulatory compliance, particularly in safety-critical domains such as automotive and medical electronics. As highlighted by Kelly et al. [235], emerging regulations such as the EU AI Act [236]impose more constrained requirements on high-risk AI systems, mandating attributes such as transparency, accountability, and human oversight. XAI provides a direct technical pathway to meet these requirements. For instance, explaining why an RL agent chose a specific circuit topology or why a DL model flagged a potential fault allows designers and auditors to verify that the system’s decisions align with sound engineering principles and safety standards.

However, the adoption of XAI is not without significant challenges. An analysis by Panigutti et al. [237], cautions that the EU AI Act itself does not explicitly mandate specific XAI tools and emphasizes that transparency can

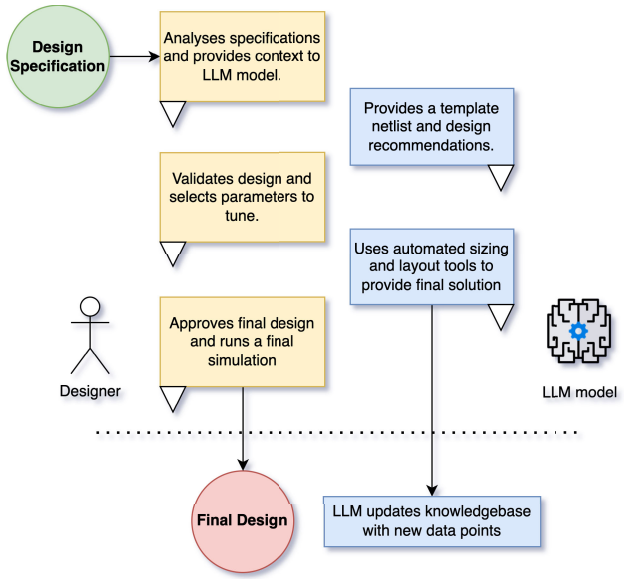

FIGURE 8. General LLM-designer conversation based on [11] and [213].

also be achieved through comprehensive documentation and user training. This is partly due to the recognized limitations of current XAI methodologies. Many techniques, while promising, can produce explanations that are fragile, inconsistent, or even susceptible to manipulation. An explanation might appear plausible but fails to capture the true reasoning of the model, a phenomenon that could lead to a false sense of security or "automation bias," where a human designer over-trusts a flawed, AI-generated solution because it is accompanied by a convincing but misleading explanation [237].

In addition, these challenges are particularly important in the context of RFIC design. The continuous nature of design parameters, the complex, non-linear correlation of physical effects, and the high-dimensional trade-offs mean that a simple feature-importance score from SHAP or a LIME approximation may be insufficient. The goal is to move towards domain-aware XAI that can ground its explanations in the language of circuit theory by linking a model's focus to concepts such as impedance matching, linearity, or noise figure. Future research must therefore focus on developing new techniques that are directly relevant to the physical constraints of circuit design. Such advancements will be crucial for transforming AI from a "closed box" optimization engine into a truly collaborative and trustworthy design partner.

VIII. LARGE LANGUAGE MODELS IN CIRCUIT DESIGN

The recent and rapid advancements in LLMs and other generative AI paradigms have catalyzed exploration of their potential across EDA [14]. LLMs, characterized by their sophisticated capabilities in understanding, generating, and reasoning with human language and structured code, present a novel interface and a powerful assistive technology for circuit designers. Early applications focused on knowledge management and design assistance, but the field is quickly evolving toward more integrated and autonomous systems. We provide a general conversation between an LLM model and a designer in Figure 8.

1) LLM-BASED AGENTS AND AUTOMATED WORKFLOWS

A significant new direction is the development of LLM-based AI agents that can interact with EDA tools to automate complex design tasks. Rather than simply providing information, these agents actively participate in the design loop. For example, Liu et al. proposed an AI agent for analog circuit sizing that integrates an LLM with simulation tools, successfully optimizing multiple circuits to meet performance targets [216]. Other agent-based systems optimize different parts of the design flow, such as AnalogTester, which automates the generation of testbenches by extracting information from academic papers [217], or LIMCA, which uses an LLM to automate the design space exploration of in-memory computing architectures [57].

More sophisticated frameworks employ multiple specialized agents that collaborate to manage the entire design process. Atelier introduces a multi-agent system based on a graph-of-thoughts architecture, where each agent handles a specific task like topology selection or parameter tuning, guided by a curated knowledge base to avoid extensive fine-tuning [12]. Similarly, MenTeR presents a fully-automated multi-agent workflow for end-to-end RF/analog netlist design, envisioning a future of "RF/Analog Copilots" that work alongside human designers [58]. The ChipMnd framework also utilizes specialized agents for both digital and analog design, aiming to enhance efficiency and accelerate prototyping [218]. These multi-agent systems represent a significant step towards fully autonomous design workflows.

2) GENERATIVE AI FOR SYNTHESIS AND EXPLORATION

Beyond workflow automation, generative models are being used for creative design tasks like topology synthesis. AUTOCIRCUIT-RL is a novel framework that uses an LLM, further refined with reinforcement learning, to automatically generate valid and efficient circuit topologies from high-level constraints [53]. This approach moves beyond optimizing fixed topologies to exploring novel circuit structures.

Other generative techniques, like the Denoising Diffusion Probabilistic Models (DDPMs) explored by de Azevedo et al., are being applied to the inverse sizing problem. These models can generate promising sizing solutions from random noise, significantly reducing the number of simulations required for optimization [158]. This highlights a broader trend where generative AI, including VAEs and GANs, is being used to explore the design space more effectively [14].

3) INTERACTIVE DESIGN AND KNOWLEDGE MANAGEMENT

The initial application of LLMs as conversational partners and knowledge managers remains highly relevant. They can quickly search and synthesize information from vast libraries of technical documents, helping designers find solutions and stay up-to-date [212], [213]. This capability is now being integrated with optimization tools. The ADO-LLM framework, for instance, combines an LLM with Bayesian Optimization, where the LLM provides contextually relevant guidance to make the optimization process more intelligent and efficient [11]. LLMs are also being used for more focused tasks, such as generating Verilog code [211] or assisting with layout through ''copilot'' systems [214], [215].

4) DISCUSSION

Current demonstrations increasingly show LLMs as active participants in the design flow, not just passive tools. However, challenges remain. A primary concern is the potential for LLMs to generate plausible but technically incorrect information (''hallucinations''). Frameworks such as Atelier address this by training the LLMs in a curated, high-quality knowledge base [12].

The trajectory of this field is moving from single-purpose LLM applications toward integrated multi-agent ''copilots'' that can manage end-to-end design tasks [58], [218]. As LLM technology continues its rapid evolution, its role in analog and RFIC design is anticipated to become more deeply integrated, shifting from assistive functions to collaborative, and even autonomous participation in both creative and analytical design stages.

IX. CHALLENGES AND FUTURE DIRECTIONS

Despite the significant progress and promising results demonstrated by AI in automating various stages of analog and RFIC design, several challenges remain. Future research directions will focus on overcoming these limitations and exploring new frontiers in AI-assisted circuit development. This section will give an overview of the approaches that can be used to solve the remaining problems and advance the field.

A. SCALABLE AND EXPLAINABLE AI ADAPTATION

A key area for future development lies in creating more generalizable and interpretable AI models. The objective is to develop systems that can adapt to new design problems without requiring complete retraining, as current models often struggle to generalize beyond their original training domains [94]. Promising directions include meta-learning approaches [238], in which models ''learn to learn'' and advanced transfer learning techniques. These can build upon the demonstrated success of frameworks such as GCN-RL in transferring knowledge across different circuit technologies [26], ultimately enabling more flexible and reusable AI tools for a wide range of analog and RF design tasks.

Another important area for advancement is improving the interpretability of AI models. As explained in Section VII, XAI has potential to be applied for simulation-based design stages such as sizing or layout. Many sophisticated AI systems function as ''closed boxes'' [9], making it difficult for designers to understand the underlying decision-making processes. This lack of transparency can reduce trust in AI-generated recommendations. For example, as discussed in Section VIII, LLMs could be leveraged to translate complex outputs or reasoning paths of AI-based optimization tools into human-readable explanations. Such capabilities would enable designers to better interpret, verify, and trust the AI's suggestions, ultimately facilitating more effective human-AI collaboration in the circuit design process.

Current XAI applications can be extended to other stages of the IC design flow. For instance, after an optimizer finds a promising set of parameters, LIME could be used to explain the AI's performance prediction by identifying which specific transistor dimensions or bias currents were most critical to achieving a high figure-of-merit. This would provide designers with immediate insight into performance sensitivities for a given design point. Other research fields have expanded upon such explainable feature selection frameworks that uses SHAP and LIME with increased efficiency [239].

Similarly, XAI can bring transparency to RL for inverse design or topology synthesis. The policy of an RL agent is often a complex neural network that is difficult to interpret. XAI techniques could be applied to explain why an agent made a particular decision at a certain step, such as choosing to add a specific component or make a certain connection. By highlighting the features of the circuit's current state that most influenced the agent's action, designers could better understand, debug, and refine the agent's learned design strategy.

B. SMARTER LAYOUT-AWARE DESIGN

In analog and RF circuits, physical layout has a substantial impact on performance, primarily due to parasitic effects and layout-dependent variations [2]. A persistent challenge is that many existing AI-based design tools focus exclusively on schematic-level optimization, without accounting for layout implications early in the design flow. As a result, circuits that initially meet performance targets in pre-layout simulations may exhibit significant degradation after layout, requiring additional manual iteration and tuning.

Future research could focus on developing AI methodologies that incorporate layout considerations earlier and more deeply into the design process. This includes creating models capable of predicting potential layout-induced issues in the early stages of schematic design [190], or frameworks that co-optimize both schematic and layout concurrently. For instance, RL agents could be trained to place components while simultaneously tuning their electrical parameters,

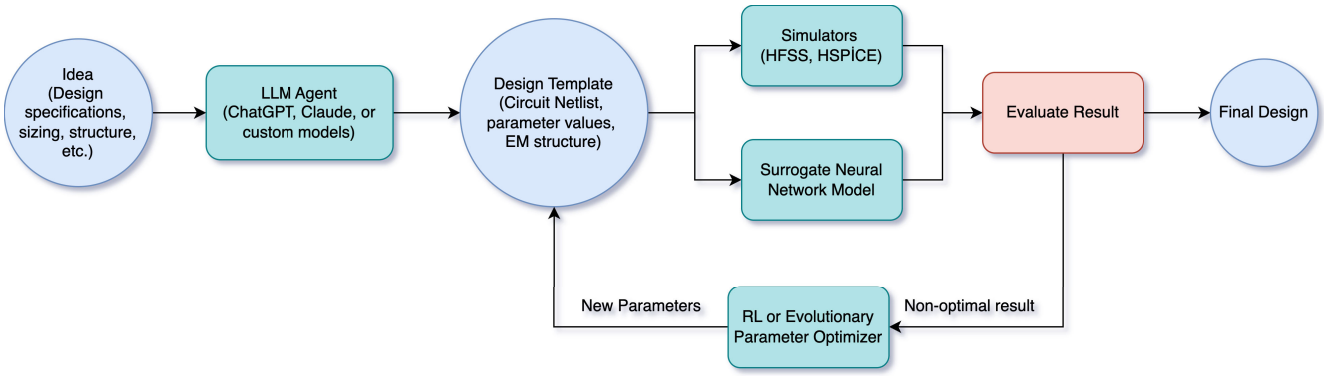

FIGURE 9. Combination of various design flows proposed by recent publications [9], [11], [88].

extending recent work in layout-aware RL for placement and routing [185], [193]. Generative models also hold promise for directly synthesizing complete, optimized layouts from high-level specifications. In the context of high-frequency RF design, integrating EM-aware learning into these systems would enable improved handling of layout-dependent parasitics and signal integrity challenges [9].

C. DATASET AVAILABILITY AND REPRODUCIBILITY

Another obstacle to the broad application of AI in circuit design is collecting and efficiently using datasets. High-quality circuit data is both expensive to generate and highly restricted. Acquiring it requires vast numbers of computationally intensive simulations with SPICE or full-wave EM solvers, creating a significant resource bottleneck [9], [138]. This problem is compounded by confidentiality issues, as most designs are intrinsically tied to proprietary PKDs from foundries, which are protected by strict non-disclosure agreements. This legal constraint makes it nearly impossible for academic researchers to share datasets or reproduce results, stifling collaboration and progress.

This scarcity and inaccessibility have profound consequences. It leads to a lack of standardized benchmarks, making it difficult to compare different AI methodologies fairly. Furthermore, the data itself is not static; an AI model trained on an early version of a PDK may become inaccurate when the foundry releases an update, leading to model drift [2]. This requires that AI systems possess lifelong learning capabilities to adapt to such changes without requiring a complete and costly retraining from scratch.

To overcome these problems, future research must prioritize data-efficient learning. One powerful strategy is transfer learning, which maximizes the value of every simulated data point [26]. A model pre-trained on a large dataset from one process node or circuit family can capture fundamental circuit behaviors. This ‘‘knowledge’’ can then be transferred and fine-tuned for a new design task using a much smaller dataset, drastically reducing the required simulation budget.

A more transformative approach that targets the root of the problem is the use of Physics-Informed Neural Networks (PINNs). Conventional surrogate models are purely data-driven, learning to mimic the output of a PDK-based simulator without any intrinsic understanding of the underlying physics. PINNs, however, operate on a different principle by embedding the governing equations of circuit theory and semiconductor physics directly into the neural network’s loss function [240]. This approach fundamentally shifts the burden of learning from data to physics. Because the PINN is constrained to obey these universal physical laws, it no longer needs to learn device behavior from scratch. It only requires a sparse set of simulation or measurement data to calibrate its physics-based model to a specific manufacturing process.

The implications of this are significant. A PINN could potentially construct a high-fidelity model of a transistor using only a handful of publicly available data points (e.g., from IV curves in a research paper), dramatically reducing the reliance on confidential PDKs. This capability, complemented by the continued development of open-source datasets [54], is vital for democratizing research and fostering a more open, collaborative, and reproducible design ecosystem.

D. ADVANCING TOWARDS FULL DESIGN AUTOMATION

A long-term goal is the development of AI systems that can manage the entire circuit design process more autonomously, from understanding initial specifications to delivering a verified design. AI is generally applied to specific segments of the design flow, we discussed various methods for specific stages of design, and integrating these into a seamless, fully automated pipeline is an ongoing effort [88]. Analog circuit design also frequently requires balancing multiple, often conflicting, performance objectives (such as gain, power consumption, and noise levels).

Inverse design [9] as mentioned in Section IV-B, offers a potentially more direct route from specification to physical realization for essential RF and microwave building blocks, aligning with the goal of increased automation in the circuit

design process. As represented in Figure 9, we designed a general design flow that are based on future works mentioned in various publications [9], [11], [88].

Future work can involve hierarchical AI systems where different AI agents collaborate, each specializing in different tasks. For example, emerging capabilities in LLMs that allow them to process and understand information from various formats including textual specifications, circuit diagrams (represented as graphs or images), simulation waveforms, and layout images could lead to a more complete understanding of the design context. Such multi-modal LLMs could improve the interaction between designers and AI tools and help link different design stages more effectively.

E. EFFICIENT AND COLLABORATIVE AI

Beyond improving algorithms, the success of AI in circuit design depends on addressing the efficiency of the AI models themselves and building a collaborative ecosystem. As AI models for RFIC design grow in complexity, the computational cost of training and running them creates a new bottleneck. The future requires hardware-aware AI model co-design, a meta-level challenge where the AI algorithms are optimized in tandem with the hardware that executes them. This could lead to specialized hardware accelerators for RFIC-specific AI tasks, drastically speeding up design space exploration. As mentioned in Section IV-D, self-healing aims to provide immediate reconfiguration of components. An on-chip AI processor can enhance this process and provide a global data collection mechanism where future generations of circuits can benefit from post-silicon failures. This enables on-chip AI co-processors that perform real-time, post-silicon optimization and calibration of the circuits.

Upon this foundation, the field can advance along two complementary paths. One path aims for fully autonomous synthesis, where an AI can take system-level specifications and independently navigate the complex, multi-physics design space to produce an EM-verified GDSII file [88]. The other path focuses on creating interactive AI co-pilots [214], where the tool acts as a powerful assistant. Both the autonomous and collaborative approaches are vital for the future of RFIC design.

X. CONCLUSION

This survey has investigated the expanding role of AI in analog and RFIC design, from optimizing parameters and generating novel topologies to automating layout and enhancing post-silicon processes. AI techniques such as RL, GNNs, and surrogate modeling significantly accelerate design cycles and uncover innovative solutions. Although challenges in generalization, layout-aware synthesis, and data requirements persist, the progress promises a transformative shift toward more autonomous and intelligent circuit design. Future work will focus on integrated AI frameworks, advanced multi-objective optimization, and leveraging emerging AI paradigms such as LLMs to further revolutionize the field.

APPENDIX
ABBREVIATIONS

TABLE 6. List of acronyms used throughout this survey.

Acronym	Definition
ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
AMS	Analog/Mixed-Signal
ANNs	Artificial Neural Networks
BB	Baseband
BNNs	Bayesian Neural Networks
BO	Bayesian Optimization
CC	Current Conveyor
CNNs	Convolutional Neural Networks
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DDPG	Deep Deterministic Policy Gradient
DE	Differential Evolution
DL	Deep Learning
DNNs	Deep Neural Networks
DQN	Deep Q-Network
DRC	Design Rule Check
DRL	Deep Reinforcement Learning
DTQN	Deep Transformer Q-Network
EA	Evolutionary Algorithms
EDA	Electronic Design Automation
EM	Electromagnetic
FoM	Figure-of-Merit
GA	Genetic Algorithm
GANs	Generative Adversarial Networks
GCN	Graph Convolutional Network
GDSII	Graphic Design System II
GNNs	Graph Neural Networks
GP	Gaussian Process
IC	Integrated Circuit
INN	Invertible Neural Network
LDO	Low-Dropout Regulator
LLMs	Large Language Models
LNA	Low-Noise Amplifier
LVS	Layout Versus Schematic
MARL	Multi-Agent Reinforcement Learning
MCDM	Multi-Criteria Decision-Making
MDP	Markov Decision Process
ML	Machine Learning
MLP	Multi-Layer Perceptron
mmWave	Millimeter-Wave
MN	Matching Network
MOEA	Multi-Objective Evolutionary Algorithm
MoE	Mixture-of-Experts
OCB	Open Circuit Benchmark
PA	Power Amplifier
PAE	Power-Added Efficiency
PINN	Physics-Informed Neural Network
PLL	Phase-Locked Loop
PPO	Proximal Policy Optimization
PSO	Particle Swarm Optimization
PVT	Process, Voltage and Temperature
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuits
RL	Reinforcement Learning
SAC	Soft Actor-Critic
SI	Swarm Intelligence
SoC	System-on-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SVDD	Support Vector Data Description
SVM	Support Vector Machine
VAE	Variational Autoencoders
VCO	Voltage-Controlled Oscillator
VDN	Value Decomposition Network
VGA	Variable-Gain Amplifier
XAI	Explainable Artificial Intelligence

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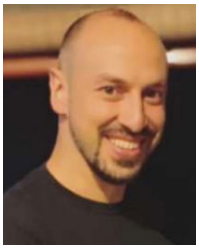

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