Experimental study of thermal coupling effects in FD-SOI MOSFET

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***Abstract*— This work studies the thermal cross-coupling between two side-by-side FD-SOI MOSFETs separated by two different spacings. Through DC measurements, the temperature increase experienced by a device due to the self-heating of a neighbor one is estimated by making a comparison with hot chuck measurements. The degradation of electrical parameters caused by the operation (i.e. heating) of the neighbor device is also analyzed as a function of the bias applied to (i.e. power dissipated by) the neighbor device.**

Keywords- FD-SOI; UTBB; thermal-coupling; self-heating.

I. INTRODUCTION

UTBB (ultra-thin body and ultra-thin BOX…) fully-depleted (FD) Silicon-on-Insulator (SOI) technology is widely considered as one of the main contenders for the technology downscaling to 20 nm and beyond [1]. However, in spite of its numerous advantages such as outstanding electrostatic control, very low mismatch, high performance in terms of low-power, high-speed, as well as attractive analog and RF figures of merit (FoMs) [2], the lower thermal conductivity of the buried oxide w.r.t silicon makes it more subject to self-heating than their bulk counterparts [3]. Some applications such as quantum computing require tight temperature control [4] and can be greatly impacted by these unwanted heating sources. Therefore, studying thermal cross-coupling is crucial to guarantee the proper functioning of such circuits.

In this paper, the impact of a heat originated from the device operation on the characteristics of a neighbor device is studied through DC measurements. The corresponding temperature rise is estimated by using the comparison with hot chuck measurements.

II. EXPERIMENTAL DETAILS

The devices used in this study are FD-SOI nMOSFETs featuring a gate length below 30 nm, a single finger of 10 µm-wide, a buried oxide (BOX) thickness in the order of 20-25 nm and a SOI film thickness of around 6-7 nm. Devices were voluntarily designed very wide in order to better demonstrate the thermal cross-coupling effect between neighbor devices representative of analog / RF circuits. Fig. 1 shows a schematic cross-section of two transistors placed side-by-side spaced by distances $L_{G\text{-}G}$ from gate-to-gate and $L_{D\text{-}S}$ from drain-to-source. Two configurations will be studied: (i) $L_{G\text{-}G}$ = 312 nm and $L_{D\text{-}S}$ = 164 nm; (ii) $L_{G\text{-}G}$ = 1204 nm and $L_{D\text{-}S}$ = 1056 nm.

In order to calibrate our feature assessment of temperature rise in the neighbor device, we first realize I_d-V_g measurements at different temperatures ranging from 298 K to 373 K (with a step of 20 K) by using a thermo-chuck from Temptronic that allows heating up the devices to the desired temperature with accurate and stable temperature control. The system was kept steady for 10 minutes on reaching each temperature point to aid in stabilizing temperature of the devices.

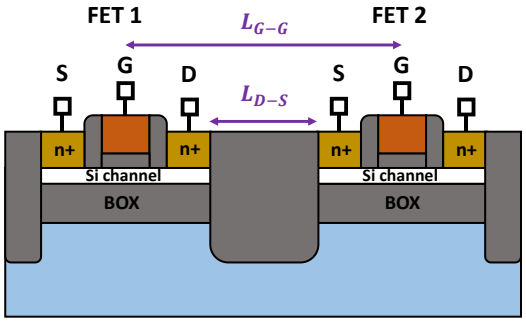

Fig. 1. Schematic cross-section of two side-by-side FD-SOI nMOSFETs spaced by distances $L_{G\text{-}G}$ from gate-to-gate and $L_{D\text{-}S}$ from drain-to-source (not to scale).

III. RESULTS AND DISCUSSION

Measurements were done in two phases. First, electrical characteristics of device 1 were measured at different temperatures using the heating chuck. During this step device 2 terminals were left floating/unbiased. Secondly, device 1 was measured again but this time with the heating chuck disabled (i.e. keeping it at a room temperature) and device 2 biased at different usual operation conditions.

A. Hot chuck measurements

Figs. 2a and 2b show, respectively, I_d-V_{GS} and subthreshold swing (SS) characteristics of device 1 biased at V_{DS} = 50 mV for temperature (T) ranging from 298 K to 373 K. One can observe that the off-state current defined at V_{GS} = -0.3 V increases by two orders of magnitude while SS increases from 78 mV/dec to 95 mV/dec with temperature rise from 298 K to 373 K. The threshold voltage V_{Th} shown in Fig. 2c is computed using

the second derivative method [5] and reduces with temperature by 0.68 mV/K which is close to 0.6 mV/K slope typically observed in advanced technologies with ultra-thin bodies like FD-SOI and FinFETs [6].

As shown in Fig. 3a, g_m/I_d curves are also strongly dependent on temperature. Indeed, by looking at Fig. 3b, one notes a reduction of almost 20% in g_m/I_d in weak inversion regime, at $I_d = 10^{-7}$ A, when T rising from 298 K to 373 K. g_m/I_d vs T plot (Fig. 3b) (as the most reliable, due to strongest variation with T), will be used here to provide an estimate of the temperature rise in the next section studying side-by-side devices.

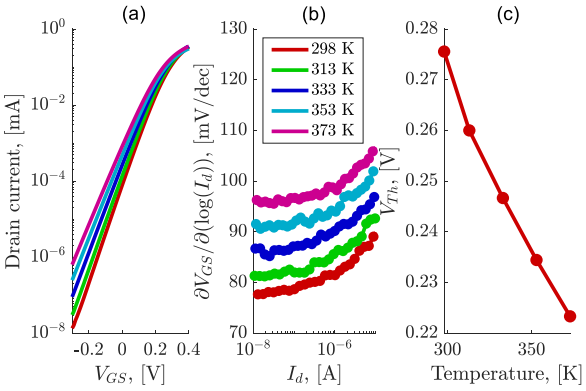

Fig. 2. (a) Drain current I_d of FET 1 vs gate voltage V_{GS} at V_{DS} = 50 mV at different temperatures, (b) $\partial V_{GS}/\partial(\log(I_d))$ vs I_d at V_{DS} = 50 mV and (c) V_{Th} vs temperature at V_D = 50 mV.

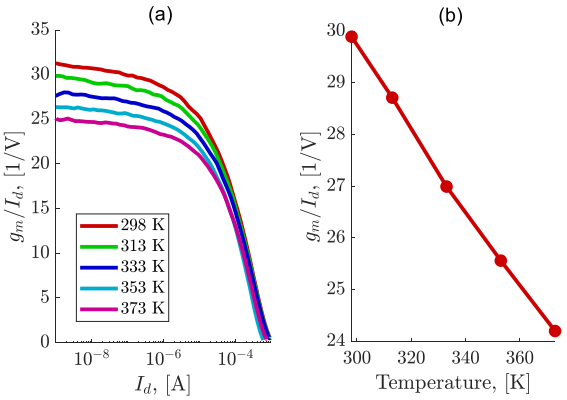

Fig. 3. (a) g_m/I_d of FET 1 vs I_d plot at V_{DS} = 50 mV at different temperatures, and (b) g_m/I_d of FET 1 vs temperature plot at V_{DS} = 50 mV and $I_d = 10^{-7}$ A.

B. Thermal coupling

Fig. 4a shows g_m/I_d characteristics of device 1 when device 2 is biased in cold FET (V_2=V_{GS2}=V_{DS2} = 0 V) and in different operation conditions in saturation and strong inversion regimes (V_2 = 0.6, 0.8 and 1 V) for Config. (i). Hold time for the device 1 was set to 30 s to assure sufficient heating of device 2 prior measurements of device 1. In strong inversion and saturation regime, the channel temperature of device 2 is expected to rise due to self-heating [3] and therefore, device 2 acts as a heater for its environment (i.e. device 1). Increasing the bias applied to device 2 (V_{GS2} and V_{DS2}) results in a temperature rise of overall structure and g_m/I_d characteristic of device 1 (Fig. 4a) thus follows the same decreasing trend with temperature as in Fig. 2. From Fig. 4b, the same observation is made for Config. (ii) although g_m/I_d reduction is smaller due to the larger distance between devices.

Fig. 5 plots g_m/I_d of device 1 measured with simultaneously operated device 2 as a function of bias applied to (power dissipated by) the device 2 for both configurations. It can be seen that the g_m/I_d of device 1 is, respectively, reduced by around 4% and 1.3% for Configs. (i) and (ii) when device 2 dissipating 9 mW (corresponding to V_2 = 1 V). By comparing g_m/I_d of Fig. 3b to Fig. 5, the relative temperature rise is estimated to 14 K (Config. (i)) and 5 K (Config. (ii)) under these conditions.

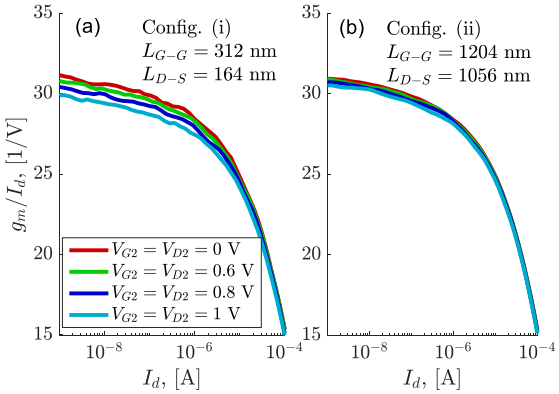

Fig. 4. g_m/I_d vs I_d plot of FET 1 at V_{DS1} = 50 mV when FET 2 is under different bias conditions for (a) Config. (i) and (b) Config. (ii).

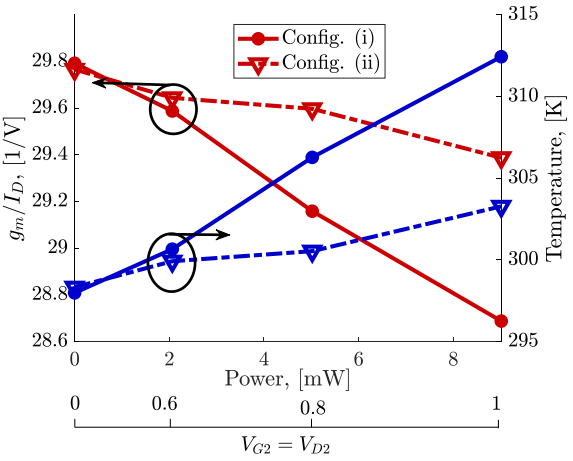

Fig. 5. g_m/I_d of FET 1 at $I_d = 10^{-7}$ A and V_{DS} = 50 mV vs dissipated power of FET 2 and its corresponding temperature for both configurations.

IV. CONCLUSION

In this work, we studied the degradation of the device characteristics caused by the heat originated from a neighbor device operation . In addition to the degradation of SS, V_{Th} and g_m/I_d with temperature, it was shown that a neighbor device in strong inversion and saturation at a

distance $L_{D\text{-}S}$ = 164 nm and $L_{D\text{-}S}$ = 1056 nm can result in a temperature rise up to 14 K and 5 K, respectively. It is essential to assess these temperature variations in order to further incorporate them in the predictive models. This is particularly important for for cryogenic applications.

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