Methodology for Performance Optimization in Noise- and Distortion-Canceling LNA

Antonio D. Martínez-Pérez
Group of Electronic Design (GDE)
Universidad de Zaragoza
Zaragoza, Spain
adimar@unizar.es

Cecilia Gimeno
ICTEAM Institute,
Université Catholique de Louvain
Louvain-la-Neuve, Belgium
cecilia.gimenogasca@uclouvain.be

Denis Flandre
ICTEAM Institute,
Université Catholique de Louvain
Louvain-la-Neuve, Belgium
denis.flandre@uclouvain.be

Francisco Aznar
Group of Electronic Design (GDE)
Centro Universitario de la Defensa
Zaragoza, Spain
faznar@unizar.es

Guillermo Royo
Group of Electronic Design (GDE)
Universidad de Zaragoza
Zaragoza, Spain
royo@unizar.es

Carlos Sánchez-Azqueta
Group of Electronic Design (GDE),
Universidad de Zaragoza
Zaragoza, Spain
csanaz@unizar.es

***Abstract*— This paper proposes a general methodology for designing noise-canceling low noise amplifiers (LNA). The procedure provides designers a more accurate information of the topology trade-offs in the technology and which restrictions must be imposed to design variables to attain target specifications. Thus, it is especially desirable when opposite specification, such as cut-off frequency, linearity, noise figure or power consumption are required. A CG-CS LNA in a 45 nm SOI CMOS technology is presented, although authors give guidelines to extrapolate the method to other topologies and technologies.**

Keywords*— *low-noise-amplifier, design methodology, wideband receiver, CMOS, noise-canceling, distortion-canceling, optimization

I. INTRODUCTION

The number of wireless connections has been increasing over the years. Moreover, new communication systems are required to be smaller, with lower power consumption and able to transmit a huge quantity of data [1]. As consequence, low noise amplifiers (LNAs) have been integrated inside the chipset and must target more restrictive specifications to allow the receiver to achieve the required performance [2].

Although some LNA topologies include inductors to improve noise figure, in most nanometer technologies the available inductors attain a low quality factor. Consequently, in the state of the art, inductorless topologies are more desirable. Among these, CS-CG (Common Source-Common Gate) LNA and its variants are widely employed [3].

This work proposes a systematic methodology for designing noise and distortion canceling LNA, applying it to a CS-CG topology in a 45 nm SOI CMOS technology. However, the methodology can easily be extrapolated to other noise canceling topologies. Linearity (IIP3) and Noise Figure (NF) are optimized simultaneously, while reflection coefficient (S_{11}), gain (G), power consumption (P) and cut-off frequency (f_C) are also evaluated. This methodology focuses on solving the problem that each design variable (transistors sizes, values of resistors and reference voltages) can affect several specifications, especially when parasitic effects of transistors cannot be neglected.

MINECO –FEDER: TEC2014-52840-R and TEC2017-85867-R

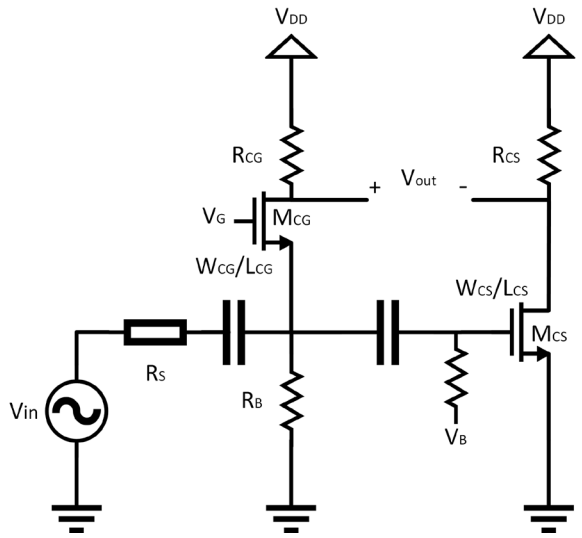


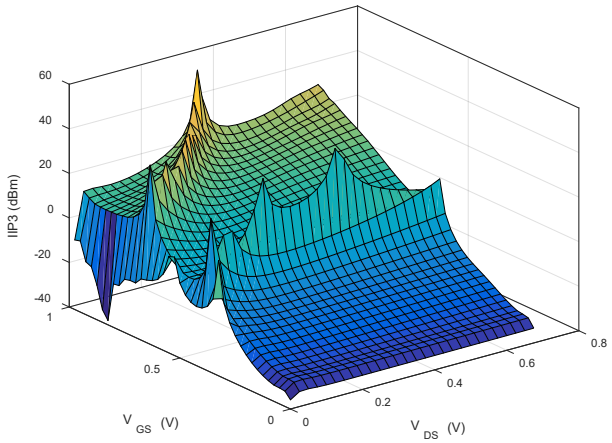
Fig. 1 Topology of basic CS-CG LNA with polarization voltages.

This paper is organized as follows. Section II describes the topology of noise canceling LNA and its specifications selected as an example for the methodology. Section III provides a deeper analysis about trade-offs between variables and restrictions for the selected topology that, afterward, are used for the component sizing. Section IV details the process of the methodology and presents the results of the designed LNA. Finally, in Section V, conclusions are drawn.

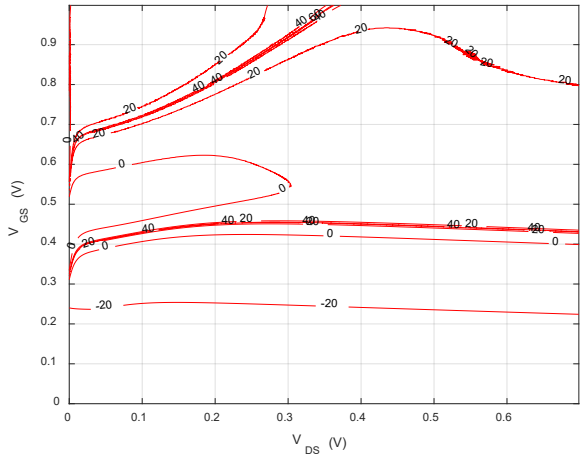
TABLE I. TARGET SPECIFICATIONS

Specification	*Value*
Noise Figure (NF)	< 2.5 dB
Linearity (IIP3)	> 0 dBm
Reflection Coefficient (S_{11})	< -10 dB
Cut-off frequency (f_C)	> 5 GHz
Gain (G)	> 15 dB
Power Consumption (P)	< 15 mW

978-1-7281-1201-5/19/$31.00 ©2019 IEEE



(a)



(b)

Fig. 2 IIP3 from combinations of V_{GS} and V_{DS} in a 100 µm width transistor in the selected technology: (a) 3-D representation (b) 2-D plot with isovalue IIP3 curves. Due to the expected voltage of V_{DS} (from 0.1 V to 0.4 V), V_{GS} should be around 0.4 V or above 0.6 V to avoid a minimum.

II. CS-CG LNA Topology

The CS-CG LNA topology (Fig. 1) amplifies the input simultaneously by a CG stage and a CS stage. On the one hand, the CG stage is required to achieve the 50 Ω input impedance adaptation and on the other hand, the CS stage to cancel output distortion and noise from CG. Ideally, obtaining a balanced output (equal gain in CS and CG stages) is the condition to cancel noise and distortion from CG. Thus, CG is calculated for input adaptation and, then, CS is designed to achieve the same gain while reducing noise and distortion [4]. This implies that:

$$g_{m\text{-}CS} \cdot R_{CS} = g_{m\text{-}CG} \cdot R_{CG} \quad (1)$$

where $g_{m\text{-}CS}$ and $g_{m\text{-}CG}$ are the transconductance of the transistors of CS and CG respectively, and R_{CS} and R_{CG} the resistor values for each stage.

However, in a higher-order evaluation, other factors, such as parasitic effects at high frequencies, can cause the CS stage to also alter the input impedance and new order terms to appear in linearity and noise calculations. Besides, most specifications become non-linearly dependent on diverse

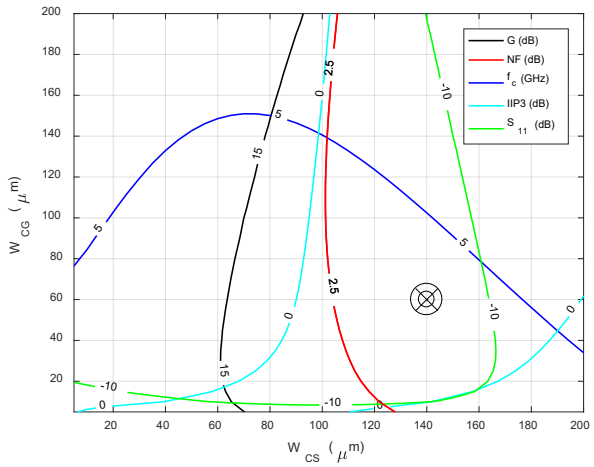


Fig. 3 Restrictions imposed by specifications depending on M_{CS} and M_{CG} widths. Analysis carried out with R_B = 1 kΩ; R_{CG} = 400 Ω; and R_{CS} = 100 Ω. Design window arround W_{CG} = 60 µm and W_{CS} = 140 µm.

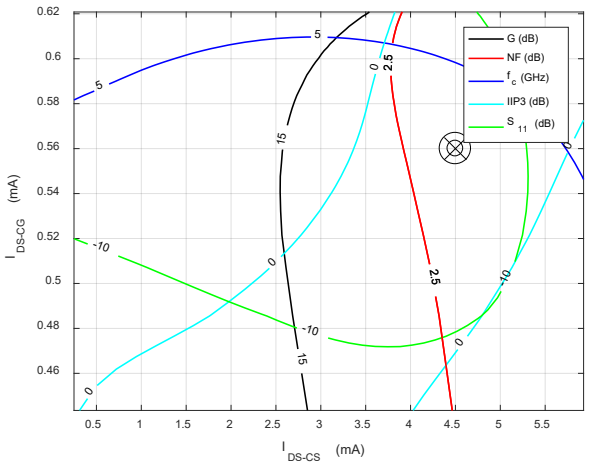


Fig. 4 Restrictions imposed by specifications depending on M_{CS} and M_{CG} currents. Analysis carried out with R_B = 1 kΩ; R_{CG} = 400 Ω; and R_{CS} = 100 Ω. Design window around $I_{DS\text{-}CG}$ = 0.56 mA and $I_{DS\text{-}CS}$ = 4.5 mA.

combinations of the same factors. In conclusion, to improve optimization several variables must be evaluated at the same time. Target specifications for a state-of-the-art receiver are shown in Table I.

In the basic topology, there are two load resistors, R_{CG} and R_{CS}. A large R_{CG} provides high gain, although bandwidth and linearity will decrease. Also, a too high R_{CG} might affect input impedance. In the case of R_{CS}, its value should be reduced to improve NF, but too much reduction would prevent the CS stage gain. It should be remarked that, in order to implement the cancellation, equation (1) must be fulfilled.

In addition, another resistor R_B is used instead of the DC current source for CG biasing. In order to avoid a resistor divider with source impedance, R_S must be negligible in comparison with R_B.

As a first approach for sizing resistor values, R_B should be at least one order of magnitude larger than the source impedance (R_S), and R_{CG} and R_{CS} values between R_B and R_S, with R_{CG} larger than R_{CS}. Otherwise, the stage will not present gain and/or linearity. The gain of the amplifier in first order is proportional to R_{CG}/R_S and R_{CS}/R_S, thus, those resistors should be larger than R_S. However, if R_{CG} is close to

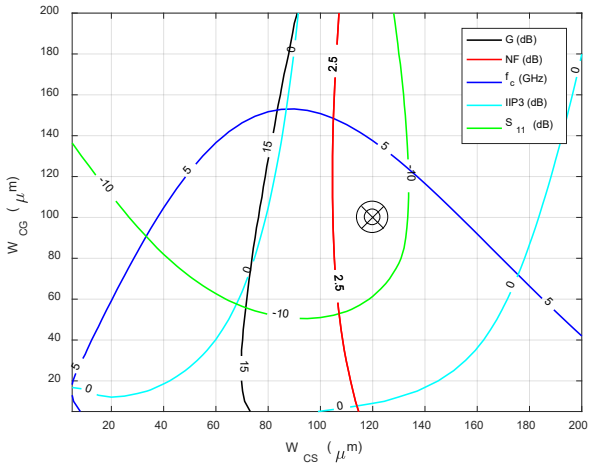


Fig. 5 Restrictions imposed by specifications depending on M_{CS} and M_{CG} widths. Analysis carried out with R_B = 1.5 kΩ; R_{CG} = 400 Ω; and R_{CS} = 100 Ω. Design window around W_{CG} = 100 µm and W_{CS} = 120 µm.

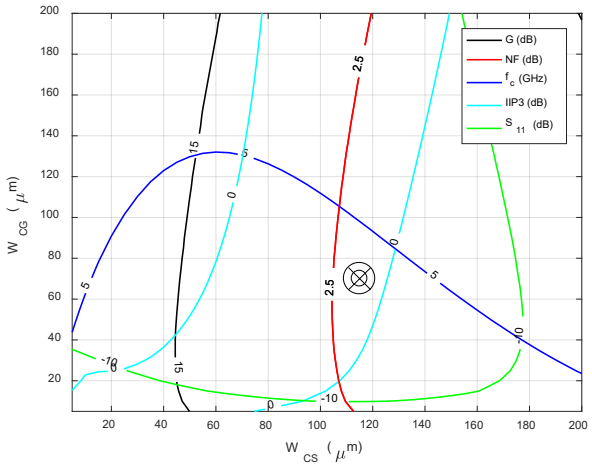


Fig. 6 Restrictions imposed by specifications depending on M_{CS} and M_{CG} currents. Analysis carried out with R_B = 1 kΩ; R_{CG} = 400 Ω; and R_{CS} = 150 Ω. Design window around W_{CG} = 70 µm and W_{CS} = 115 µm.

R_B, a constrained dynamic range will reduce linearity. Moreover, [4] recommends an R_{CS} smaller than R_{CG} for reducing non-cancelable thermal noise, and, as consequence, improving NF.

III. Transistor Sizing and Biasing

Typically, transistor length will be the minimum available of the used technology to achieve high frequency, although increasing the area could help reduce some noise; and V_G will approach V_{DD} to bias M_{CG} in saturation. Consequently, the width of both transistors (W_{CG} and W_{CS}) and V_B are the main variables to control.

As distortion of M_{CG} will be canceled by topology, the linearity of the LNA will strongly depend on M_{CS}. According to [3], knowing the value of I_{DS} of the M_{CS} transistor in function of V_{GS} and V_{DS}, it is possible to calculate coefficients proportional to signal and harmonic power by derivation. In consequence, IIP3 can be estimated as Fig. 2 represents. Considering the 1-V V_{DD} supply voltage, a V_{DS} from 0.1 to 0.4 V is expected in this design. Thus, according to Fig. 2b, V_{GS} should be about 0.4 V (weak inversion) or above 0.6 V (limit between saturation and triode region) to attain good linearity. However, due to gain restrictions, weak inversion is preferred for M_{CS} [5], so 0.4 V is selected for V_B.

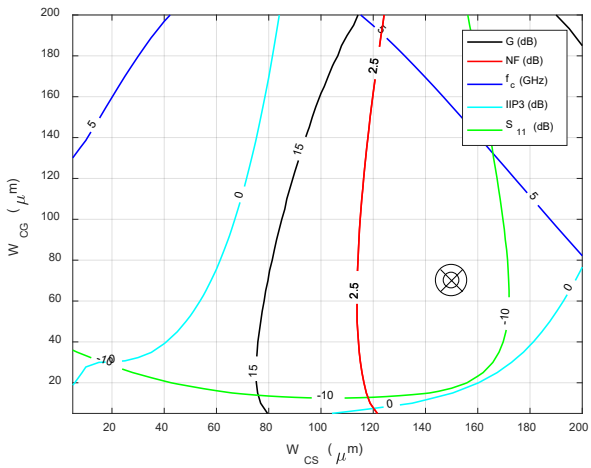


Fig. 7 Restrictions imposed by specifications depending on M_{CS} and M_{CG} widths. Analysis carried out with R_B = 1 kΩ; R_{CG} = 300 Ω; and R_{CS} = 100 Ω. Design window around W_{CG} = 70 µm and W_{CS} = 150 µm.

In a similar way, the noise has also a great dependency on M_{CS}. It will decrease with M_{CS} area, but also f_C will do. Normally, the different specifications will create diverse restrictions with several terms. These equations result too complex for an easily-understandable analytical approach but can be represented from detailed model simulation results as Fig 3. This figure shows the achieved specifications versus the width of the transistors.

This representation allows to visualize dependencies and optimize specifications trade-off. Increasing W_{CS} and W_{CG}, as expected, improves Gain and NF, but S_{11} and f_C reach a limit. In terms of linearity, the possible area is between the two light-blue lines. Besides, it should be considered that fabrication inaccuracies, temperature or other non-predictable effects can shift the lines, thus certain margins are desirable. In Fig. 3, an advisable selection is around W_{CG} = 60 µm and W_{CS} = 140 µm.

Fig. 4 represents the same data as Fig. 3, but the axes are the currents of the stages instead of the transistor size. It can be observed that power consumption is far below our maximum, so it is excluded from the figures. From the comparison between Fig. 3 and Fig. 4, it can be deduced that $I_{DS\text{-}CG}$ has little variation on the W_{CG} while the MOSFET is in the saturation region (since the current is controlled mainly by R_B).

If R_B is increased (see Fig. 5), noise and bandwidth are improved, although S_{11} becomes much more restrictive because it modifies $I_{DS\text{-}CG}$, and, thus, M_{CG} transconductance. Also, the area of interest for linearity in Fig 5 is narrower than in Fig. 3 and requires lower values of W_{CS}.

On the other hand, a higher value of R_{CS} causes to shift linearity to lower W_{CS} as it is shown in Fig 6. This is expected due to (1). The minimum NF is increased because topology does not cancel CS noise and noise is well known to be proportional to resistance. However, gain and input impedance are improved while the cut-off frequency is reduced.

Decreasing R_{CG} can improve bandwidth, at the cost of restricting gain and noise figure. It also makes S_{11} and linearity less restrictive for certain combinations. Fig 7 presents the impact of an R_{CG} variation.

TABLE II. VALUES OF THE DESIGNED LNA

Variable	*Optimized Value*	*Initial Value*
R_{CG}	400 Ω	400 Ω
R_{CS}	150 Ω	100 Ω
R_B	1.2 kΩ	1 kΩ
V_G	0.8 V	1 V
V_B	0.4 V	0.4 V
W_{CG}	40 µm	60 µm
W_{CS}	100 µm	140 µm

TABLE III. COMPARISON WITH THE STATE OF THE ART

Specification	*This work*	[1]	[3]	[4]	[6]
CMOS Technology	45 nm SOI	28nm FDSOI	28 nm FDSOI	65 nm	65 nm
NF	2.5 dB	4.5 dB	3.1 dB	3.5 dB	5 dB
IIP3	1 dBm	3 dBm	4.2 dBm	0 dBm	2 dBm
S_{11}	-12 dB	-	-	-10 dB	-6 dB
f_C	6.2 GHz	3.5 GHz	11 GHz	5.2 GHz	7 GHz
G	16.8 dB	15 dB	15 dB	15.6 dB	20 dB
P	3.75 mW	0.8 mW	1.8 mW	14 mW	3.84 mW

IV. PROPOSED METHODOLOGY

A methodology for optimal selection of component values in noise/distortion canceling LNA is proposed by induction from the analysis of CS-CG LNA. The method is flexible enough to be adapted to different technologies, but, as example, authors present a design of a CS-CG LNA in 45 nm SOI CMOS technology.

Its main principle is to select an initial operating point, and then, for that point, plotting the design restriction versus the two main variables that must be balanced. Later, it will be possible to displace the operating point to a more adequate position and by iteration, optimize the multivariable system.

Because of the standard CS-CG topology, resistors and bias voltages define the operating point and transistors are sized to guarantee the balance. As transconductance is related to W/L and the length is minimum for frequency optimization, W_{CG} and W_{CS} become the two main variables.

Thus, as a starting point, resistor values should be selected to be R_B (1 kΩ) much larger than R_S (50 Ω); R_{CG} (400 Ω), between R_B and R_S; and R_{CS} (100 Ω), between R_{CG} and R_S (see Section II for more details). Also, V_B and V_G can be set to 0.4 V and 1 V, respectively. All these initially selected values will hardly be the optimal ones, but they will allow to observe the main restrictions in terms of W_{CS} and W_{CG}.

Then, the designer can optimize transistor sizes by the representation of restrictions due to target specifications. The area where all the conditions are achieved is the design window. Modifying the operation point will open or close this window thus, by iteration, optimization can be carried out for all variables according to all the others.

Table II shows the final values of the variables. From the initial ones, R_{CS} and V_G have been decreased while R_B has been increased. Also, W_{CG} and W_{CS} have changed to smaller sizes. Obtained specifications are presented in Table III. This table also shows a comparison with other similar LNAs in the literature, which were designed following other methods.

V. CONCLUSIONS

In this paper, a design methodology for a noise- and distortion- canceling LNA is proposed. The main target of this methodology is not only to optimize a certain parameter but to obtain several parameters optimized at the same time according to the best trade-off for the applications. To enable this, a graphical global vision of the trade-offs is provided to designers.

Main specifications, such as noise, linearity or frequency, tend to imply opposite requirements. However, the design window represents the viability to obtain all desired specifications. Thus, the methodology can greatly benefit designers working with high restrictive specifications.

Moreover, in contrast to a pure simulation methodology, this method favors the comprehension of the circuit, which can lead to determinate if a modification of the topology can be of interest or otherwise it will not improve the performance.

The paper also presents a design obtained by this method in a 45 nm SOI CMOS technology. Results, competitive compared with other similar LNAs, and sizing for those results are shown.

REFERENCES

[1] G. de Streel, D. Flandre, C. Dehollain and D. Bol, “Towards ultra-low-voltage wideband noise-cancelling LNAs in 28nm FDSOI”, 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2015, pp-1-2

[2] H. Zang and E. Sanchez-Sinencio, “Linearization techniques for CMOS low noise amplifiers: A tutorial.”, IEEE Trans. Circuits Syst.-I: Reg. Pap., vol. 58, no 1, pp. 22-36, Jan. 2011

[3] C. Gimeno, F. Stas, G. de Steel, D. Bol and D. Flandre, “Improving Noise and Linearity of CMOS Wideband Inductorless Balun LNAs for 10-GHz Software-Defined Radios in 28nm FDSOI”, 2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2017, pp-1-2

[4] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts and B. Nauta, “Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling”, IEEE Journal of Solid-State Circuits, vol. 43, no. 6, June 2008, pp. 1341-1350.

[5] R. Fiorelli, F. Silveira and E. Peralias, “MOST Moderate-Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs”, IEEE Transactions on Microwave Theory and Techniques, vol.62, no.3, March 2014.

[6] T. Chen, S. Rodriguez, J. Akerman and A. Rusu, “An inductorless wideband Balun-LNA for spin torque oscillator-based field sensing”, 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2014, pp. 36