Quantum capacitance impact on low-frequency noise in MoS_2 transistors

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Low-frequency noise (LFN) is a critical figure of merit for characterizing the performance and application limits of electronic devices and circuits. In two-dimensional (2D) material-based transistors, their higher amplitudes of LFN than those of silicon counterparts are generally attributed to the atomically thin body, which is more susceptible to interfacial scattering. However, with advancing miniaturization of 2D transistors, the quantum capacitance (C_q) arising from the confined density of states of the ultrathin channel can impose limitations on electrical performance and inevitably influence the LFN behavior. Herein, to elucidate the fundamental physics of how quantum capacitance impacts LFN, we present a comprehensive study of the LFN characteristics in MoS_2 field-effect transistors (FETs). It is found that C_q significantly limits transconductance and carrier density, thereby affecting the LFN performance. For monolayer devices, the drain current fluctuations can be explained by the carrier number fluctuation featuring correlated surface mobility fluctuation, and the normalized noise amplitude (S_I/I_{ds}^2) becomes effectively suppressed in the subthreshold region while enhanced in accumulation because of the influence of C_q on transconductance efficiency. On the other hand, the LFN characteristics inside multilayer transistors follow Hooge's mobility fluctuation model and are impacted by C_q mainly in strong accumulation. In this regime, C_q leads to an increment of S_I/I_{ds}^2 due to the restrained carrier density in semiconductor channels. Our findings provide unique insight into quantum capacitance effects on LFN characteristics in 2D FETs, and can facilitate their device design, performance optimization, and electronic applications.

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I. INTRODUCTION

Two-dimensional (2D) semiconductors, such as the transition metal dichalcogenides (TMDs), have been extensively developed for future electronic device and circuit technologies [1–5]. Field-effect transistors (FETs) fabricated from MoS_2 and related TMD layers can achieve excellent on:off current ratio and carrier mobility and exhibit advantages of channel scalability and short-channel-effect immunity [6–10]. However, low-frequency noise (LFN), usually manifesting as drain-current or flat-band voltage fluctuations, has become a crucial metric and adversely impacts the operation of 2D transistors and circuits [11,12]. Specifically, the amplitude of LFN is significantly important for radio-frequency circuit design, because it is the major contributor to phase noise of oscillating systems [13,14]. Numerous studies have identified physical mechanisms of LFN characteristics for TMD-based FETs [15–19]. Among them, drain-current fluctuations arise from carrier number fluctuation (CNF) due to carrier trapping and releasing by interface defects, or Hooge's mobility fluctuation (HMF) caused by a fluctuation of the mean free path of carriers, with relevance to operation regime and channel thickness [15,16]. Furthermore, to attain ideal LFN characteristics, the metal contact, subgap density of states, and aging issues are addressed by forming a van der Waals junction, inserting a Fermi-level depinning layer, implementing dual-gate modulation, annealing, etc. [20–23].

In ultrathin 2D transistors, it is imperative to take into account the quantum capacitance effect induced by the movement of the Fermi level relative to the energy bands in 2D semiconductors with low density of states [24]. Especially for FETs characterized by aggressively scaled effective oxide thicknesses (EOTs) or nondegenerate carrier statistics, the quantum capacitance (C_q) plays

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a significant role in influencing their electrostatic field-effect control capability and thereby limits transconductance, maximum carrier density, field-effect mobility, etc. [24,25]. In such cases, previous reports may be inadequate for comprehensively understanding the LFN mechanisms of 2D FETs and optimizing the noise performance thereafter. Generally, the fluctuations and noise in a FET can be elucidated by the CNF model, which comes from the charge fluctuations at the semiconductor-oxide interface and evolves from transfer via transconductance [26–30], or by the HMF model, which is induced by the fluctuations of the transport coefficients like conductivity, mobility, and velocity [31–36]. With respect to this issue, how quantum capacitance impacts LFN performance of 2D transistors has not yet been explored when miniaturizing electronic devices.

In this Paper, we address these gaps in knowledge by systematically investigating LFN characteristics of MoS_2-based transistors with nanometer-scale EOTs, based on experimental observations and analytical simulations. The measurements suggest that LFN in monolayer and multilayer MoS_2 transistors follows CNF featuring correlated surface mobility fluctuation and the HMF model, respectively. Concerning the underlying physics of LFN, we accurately quantify the impact of quantum capacitance on LFN performance in these 2D devices, which evolves from the variation of transconductance and carrier density induced by C_q. These results can offer valuable physical insights into noise behavior for these 2D transistors with scaling dimensions, and improve the reliability of LFN as a means of evaluating device performance and applications.

II. RESULTS AND DISCUSSION

A. Device fabrication and dc measurements

Figure 1(a) shows a schematic of the back-gated MoS_2 transistor used in our investigation. For fabrication, firstly, Cr(30 nm)/Au(20 nm) metal stacks are evaporated on a sapphire wafer as the back-gate electrode, then the HfO_2 gate dielectric is grown by atomic layer deposition. Next, mechanically exfoliated MoS_2 is transferred to the gate insulator, followed by physically laminated drain-source contact electrodes (20-nm Au). See Fig. S1 within the Supplemental Material for the process details [37]. Finally, the resulting configuration consists of two transistors in series, as depicted in Fig. 1(b), where the red dashed area defines the exfoliated MoS_2 sheet. Raman and photoluminescence (PL) spectra are implemented to confirm the film thickness. As shown in Figs. S2(a) and S2(b) within the Supplemental Material [37], the Raman shift between E^1_{2g} and A_{1g} modes is approximately 18.95 cm^{-1} and the PL peak is located at 1.87 eV, which are typical for monolayer MoS_2 [38–40]. The dc characteristics of the fabricated MoS_2 transistors are determined in vacuum (1.2×10^{-5} Torr) at room temperature. Figures 1(c) and 1(d) depict the representative transfer and output characteristics of the fabricated monolayer device, respectively. The on:off current ratio $I_{on}/I_{off} > 10^7$ is measured for a back-gated voltage V_{bg} ranging from -1 to 1 V at drain-source bias $V_{ds} = 0.1$ V, with a negligible gate-leakage current I_{bg} of 0.01 pA/μm. Subthreshold swing (SS) is estimated for the drain-current I_{ds} range of 10^{-12}–10^{-11} A/μm to be 103.72 mV/dec. The linear relationship between I_{ds} and V_{ds} indicates a high-quality metal-semiconductor contact.

B. Quantum capacitance

Before investigating the noise characteristics, primarily we consider the quantum capacitance properties in MoS_2 transistors. Figure 2(a) shows the equivalent circuits of monolayer (top) and multilayer (bottom) MoS_2 transistors for capacitance versus back-gate voltage (C-V_{bg}) measurements. For monolayer devices, the total gate capacitance C_g can be given by $1/C_g = 1/C_{ox} + 1/(C_q + C_{it})$ [41], where C_{ox} represents gate oxide capacitance, C_q is quantum capacitance, and $C_{it} = q^2 D_{it}$ (q and D_{it} are the elementary charge and interface state density, respectively) is the interface trap capacitance, which can be neglected in high-frequency measurements [42]. The measured C-V_{bg} curves for monolayer MoS_2 transistors with different EOTs are shown in Figs. 2(b) and 2(c), where frequency dispersion can be clearly observed in both samples. In general, a smaller frequency dispersion indicates a higher interface quality, that is, a lower interface state density D_{it}. Here, the values of D_{it} extracted from SS in transfer characteristics of sample 1 [EOT = 6.11 nm; see Fig. S3(a) within the Supplemental Material [37]] and sample 2 [EOT = 4.54 nm; see Fig. 1(c)] are 5.92×10^{12} and 3.46×10^{12} cm^{-2} eV^{-1}, respectively [42,43]. The corresponding metal-insulator-metal structures are constructed to obtain C_{ox}, as shown in Figs. S4(a)–S4(c) within the Supplemental Material [37], with the values of 0.565 and 0.76 μF/cm^2, respectively. The variable-frequency C-V characteristics show that C_{ox} is almost independent of frequency, which confirms the high quality of gate stacks.

Ideally, the total gate capacitance C_g should be zero in the deep depletion region (off state) and saturate to C_{ox} in the strong accumulation region (on state). In our practical measurements, the discrepancy of C_g at off state can be attributed to the parasitic capacitance C_{para}, which is generated in the spatial region without MoS_2 underneath top electrodes [see Fig. 1(b)]. In the accumulation region, quantum capacitance C_q becomes pronounced upon interface trap capacitance C_{it} and significantly restricts the saturation capacitance. For monolayer MoS_2 transistors, C_q can be evaluated as [24]

$$C_q = q^2 g_{2D}\left[1 + \frac{\exp(E_g/2kT)}{2\cosh(qV_{ch}/kT)}\right]^{-1}, \qquad (1)$$

where g_{2D} is the 2D density of states [24,44], E_g is the band gap, V_{ch} is the channel potential, k is the Boltzmann

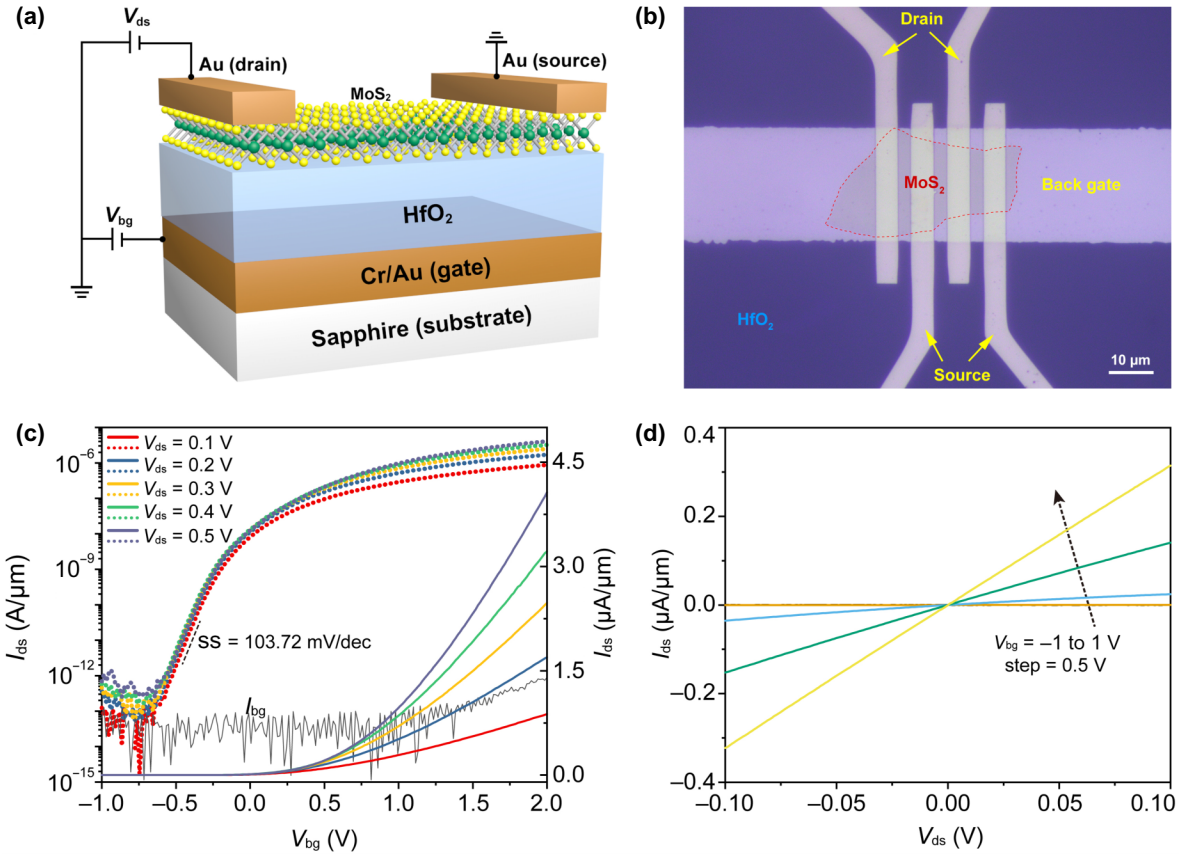

FIG. 1. (a) Schematic of our back-gated monolayer MoS_2 transistor with electrical connections. (b) Optical micrograph of the MoS_2 transistor fabricated on a sapphire substrate. The red dashed region marks the mechanically exfoliated MoS_2. The scale bar is 10 μm. (c) Transfer (I_{ds}-V_{bg}) and (d) output (I_{ds}-V_{ds}) curves of the monolayer MoS_2 transistor with EOT = 4.54 nm. The gate-leakage current (I_{bg}) is about 0.01 pA/μm at $V_{ds} = 0.1$ V.

constant, and T is ambient temperature. Taking the terms of C_{it} and C_q, the relationship between V_{bg} and V_{ch} can be expressed as [41,42,45]

$$V_{bg} = V_{bg,midgap} + \int_0^{V_{ch}} \frac{C_{ox} + C_q + C_{it}}{C_{ox}} dV_{ch}, \quad (2)$$

where $V_{bg,midgap}$ is a fitting parameter to compensate for the n-doping effect for MoS_2. Herein, based on Eqs. (1) and (2), we calculate the dependence of C_g and C_q on V_{bg}, as depicted by the black dashed lines and red solid lines in Figs. 2(b) and 2(c) and the corresponding insets, respectively, which are in good accordance with the experimental C-V curves. Therefore, we confirm that C_q in the MoS_2 transistors increases with V_{bg} while the device regime goes from depletion (off state) to weak and strong accumulation regimes (on state).

Scaling EOT in the MoS_2 FETs, the impact of quantum capacitance C_q on the device's total gate capacitance C_g is further analyzed. C_g-V_{bg} curves for the monolayer MoS_2 device are obtained from the Technology Computer Aided Design (TCAD) platform, as illustrated in Fig. 2(d), in which the interface trap capacitance C_{it} is excluded with an ideal interfacial condition. For such a case, C_q can be directly calculated by $\partial Q/\partial V_{ch}$ (Q is the channel charge density), and the relationship between C_g and C_q is recast as: $1/C_g = 1/C_{ox} + 1/C_q$. Obviously, as EOT decreases from 3.85 to 1.54 nm, C_q turns out to noticeably limit the total capacitance C_g and leads to an incremental loss of C_g (from 6.1% to 9.4%). This trend is consistent with similar observations in previous reports [44], with sample-to-sample variability. Further, for multilayer configurations (approximately 10 nm), the depletion capacitance C_{dep} (defined as ε_s/W_D, where ε_s and W_D are dielectric constant and depletion width of MoS_2, respectively) should be included. As a result, the extracted $\partial Q/\partial V_{ch}$ as a function of V_{bg} is plotted in Fig. 2(e) for monolayer and multilayer MoS_2 transistors. It is clearly seen that $\partial Q/\partial V_{ch}$ of the multilayer devices is much lower than that of the monolayer cases, due to the non-negligible C_{dep} in series [see Fig. 2(a)]. Thus, it is worth noting that

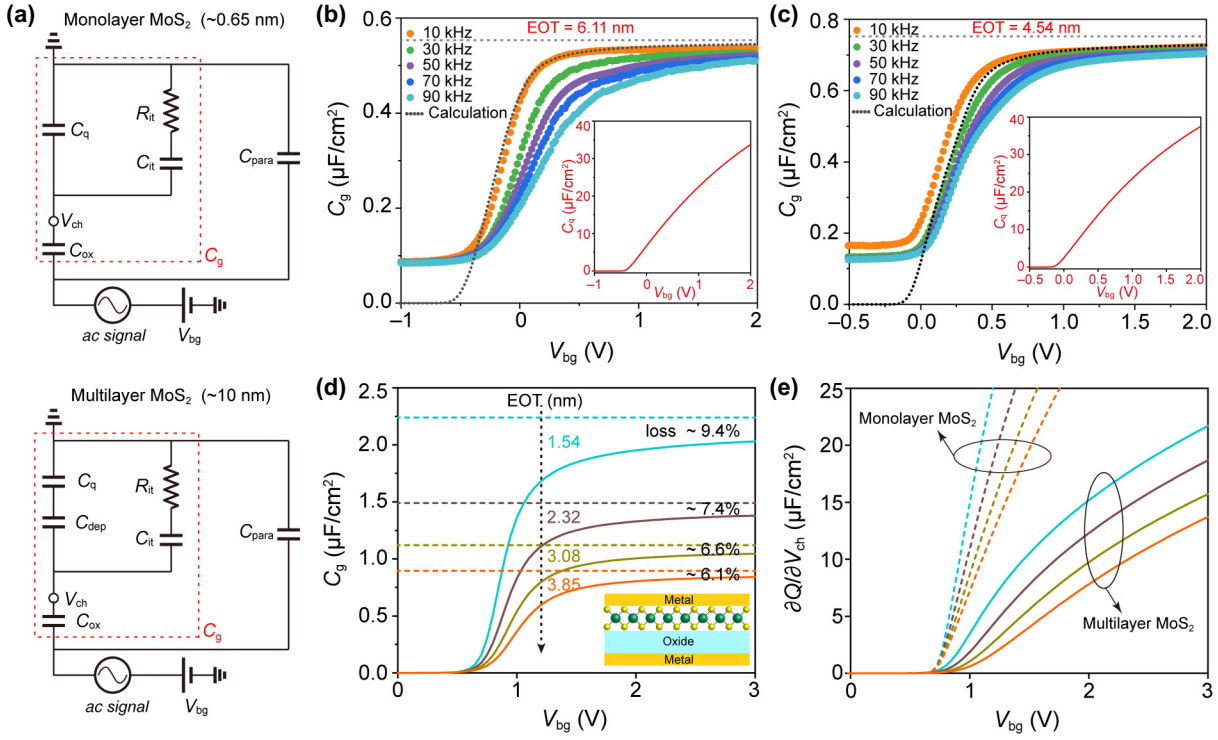

FIG. 2. (a) Equivalent circuits of monolayer and multilayer MoS_2 transistors for C-V measurement. Measured C_g-V_{bg} characteristics of the monolayer transistors with EOT = 6.11 nm for sample 1 (b) and EOT = 4.54 nm for sample 2 (c). The gray and black dashed lines are C_{ox} and calculated C_g, respectively. Correspondingly, the insets show C_q as a function of V_{bg}. (d) Simulated C-V characteristics for the monolayer MoS_2 capacitor with different EOTs. The inset shows a schematic of the capacitor. (e) Simulated $\partial Q/\partial V_{ch}$ as a function of V_{bg} for monolayer and multilayer MoS_2 devices.

C_q cannot be derived from $\partial Q/\partial V_{ch}$ for multilayer MoS_2 devices because of the extra depletion capacitance C_{dep}.

C. LFN in monolayer MoS_2 transistors

Subsequently, LFN measurements are conducted for the fabricated monolayer devices. Figures 3(a) and 3(b) illustrate the normalized drain-current power spectral density (S_I/I_{ds}^2) versus frequency (f) at different back-gate voltages V_{bg} but the same $V_{ds} = 0.1$ V. The amplitude of S_I/I_{ds}^2 decreases with increasing V_{bg} in both samples. And the typical $1/f$ noise behavior can be clearly observed, indicating the uniform trap distributions in the gate insulator [46]. In order to verify the physical origin of LFN fluctuations, the relationships between S_I/I_{ds}^2 and I_{ds} are plotted on a log-log scale [see Figs. 3(c) and 3(d)]. Typically, the current or voltage fluctuation in 2D field-effect transistors can be attributed to the HMF and CNF models. If S_I/I_{ds}^2 is proportional to $1/I_{ds}$, the HMF model is suitable for interpreting LFN, while S_I/I_{ds}^2 changes with I_{ds} as $(g_m/I_{ds})^2$, demonstrating that the CNF model is appropriate. See Note S1 within the Supplemental Material for the detailed theoretical derivations and physical explanations [37] (including Refs. [47–50]). At frequency $f = 100$ Hz, the same trends appear for the experimental S_I/I_{ds}^2 (left axis) and $(g_m/I_{ds})^2$ (right axis) versus I_{ds} in Figs. 3(c) and 3(d), indicating that the CNF model is appropriate for the monolayer MoS_2 transistors, where the normalized drain-current power spectral density $S_I/I_{ds}^2 = (g_m/I_{ds})^2 \times S_{Vfb}$, and the input back-gated voltage noise power spectrum density S_{Vbg} is simply equal to the flat-band voltage spectral density S_{Vfb} [47], which is independent of back-gated voltage. However, in our experiments, the measured S_{Vbg} of both samples exhibits a correlation with back-gate voltage V_{bg} (see Fig. S5 within the Supplemental Material [37]), which suggests that the classical CNF model seems to be insufficient to elucidate the measured LFN in our devices.

In fact, for such ultrathin channels, the carrier fluctuation scheme should consider that the interface defects could induce a fluctuation of the scattering rate and, therefore, of the effective mobility. The dependence of the effective mobility on the interfacial defects gives an extra drain-current fluctuation. Therefore, the CNF model with correlated surface mobility fluctuation (corrected CNF model) is employed, which can be expressed as [51,52]

$$\frac{S_I}{I_{ds}^2} = \left(1 + \alpha\mu_{eff}C_{ox}\frac{I_{ds}}{g_m}\right)^2 \times \left(\frac{g_m}{I_{ds}}\right)^2 \times S_{Vfb}, \quad (3)$$

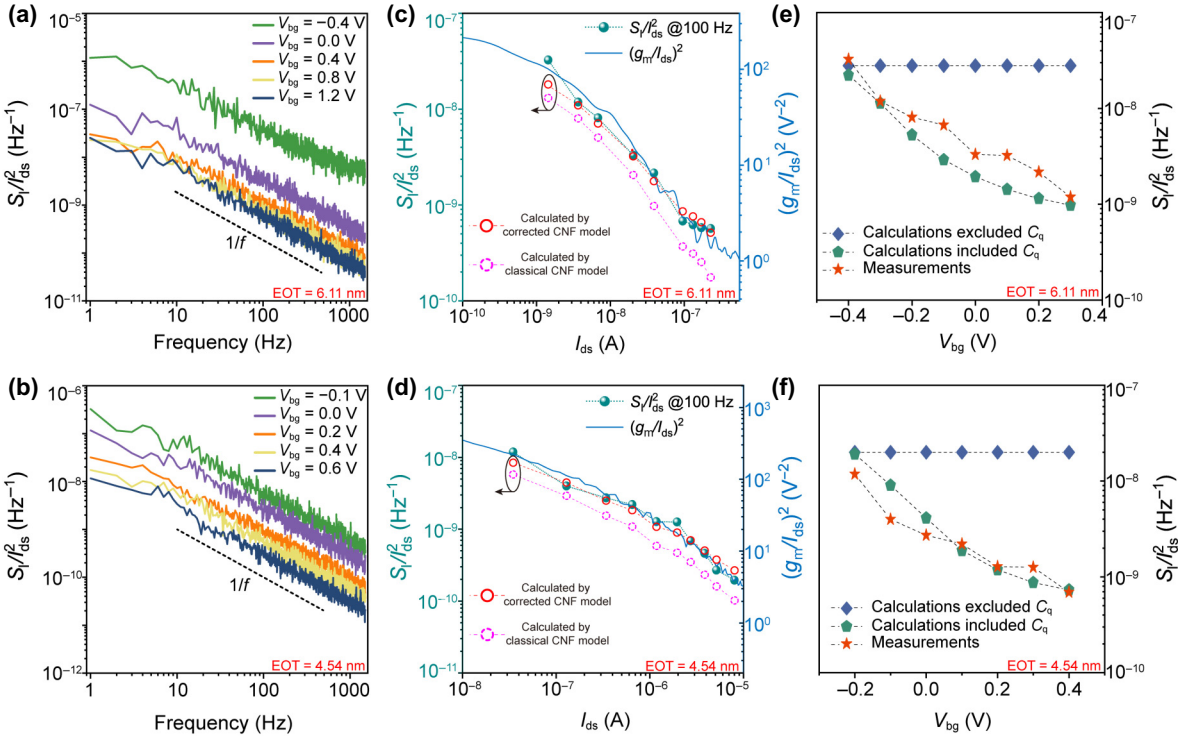

FIG. 3. Normalized current power spectral density S_I/I_{ds}^2 as a function of frequency for (a) sample 1 (EOT = 6.11 nm) and (b) sample 2 (EOT = 4.54 nm) under different back-gate voltages at $V_{ds} = 0.1$ V. (c),(d) Plots of measured and calculated S_I/I_{ds}^2 versus I_{ds} at $f = 100$ Hz, respectively. The solid lines represent $(g_m/I_{ds})^2$ versus I_{ds}. (e),(f) Comparison of S_I/I_{ds}^2 between experimental measurement and analytical calculation for monolayer MoS_2 transistors by incorporating the C_q effects.

where μ_{eff} is the effective mobility and α is the Coulomb scattering coefficient representing the sensitivity of carrier mobility to the interfacial charge. If the sensitivity is weak enough ($\alpha \approx 0$), Eq. (3) is then simplified to the classical CNF model where S_{Vbg} is constant with V_{bg}. Then we calculate the LFN amplitude by employing the classical and corrected CNF models with numerical results shown in Figs. 3(c) and 3(d). It is clearly seen that the measured noise amplitudes S_I/I_{ds}^2 are better matched by the corrected CNF model than by the classical model. In addition, the relationship between S_{Vbg} and S_{Vfb} can be rewritten as: $\sqrt{S_{Vbg}/S_{Vfb}} = 1 + \alpha\mu_{eff}C_{ox}I_{ds}/g_m$. Thus the Coulomb scattering coefficient α can be extracted from plots of $(S_{Vbg}/S_{Vfb})^{0.5}$ versus $(g_m/I_{ds})^{-1}$ (see Fig. S6 within the Supplemental Material [37]), with values of 1.27×10^5 and 1.09×10^5 V s/C for sample 1 (EOT = 6.11 nm) and sample 2 (EOT = 4.54 nm), respectively, which are comparable with the values reported for MoS_2 transistors [52].

To explore how quantum capacitance impacts the LFN characteristics, the transconductance efficiency g_m/I_{ds} for the monolayer MoS_2 transistor can be represented as $(q/kT)[C_{ox}/(C_{ox} + C_{it} + C_q)]$ in the weak accumulation regime [47]. By utilizing C_q [see insets of Figs. 2(b) and 2(c)], C_{ox}, and C_{it}, we plot S_I/I_{ds}^2 versus V_{bg} at $f = 100$ Hz in accordance with analytical calculation and experimental data in Figs. 3(e) and 3(f). It can be clearly seen that the experimental S_I/I_{ds}^2 versus V_{bg} is in good agreement with the calculations after incorporating the C_q effect. In contrast, S_I/I_{ds}^2 is independent of V_{bg} when excluding C_q and only matches the experimental data in the deep subthreshold region ($V_{bg} = -0.4$ V for sample 1 and -0.2 V for sample 2), where C_q is very small and negligible. Apparently, the gate-controlled quantum capacitance C_q determines the transconductance efficiency g_m/I_{ds} of the monolayer MoS_2 transistors, and g_m/I_{ds} significantly affects the amplitude of LFN derived from Eq. (3). Based on this correlation, we conclude that C_q significantly reduces the normalized noise amplitude (S_I/I_{ds}^2) in the subthreshold region, where C_q increases with gate voltage V_{bg} and leads to a decreased transconductance efficiency g_m/I_{ds} thereafter. For strong accumulation, g_m/I_{ds} is plotted in Fig. S7 within the Supplemental Material [37], obtained from the TCAD platform and with the quantum capacitance model under consideration. See Note S2 within the Supplemental Material for the detailed TCAD model [37]. It can be inferred that the noise amplitude gets enhanced since C_q increases g_m/I_{ds} in this regime.

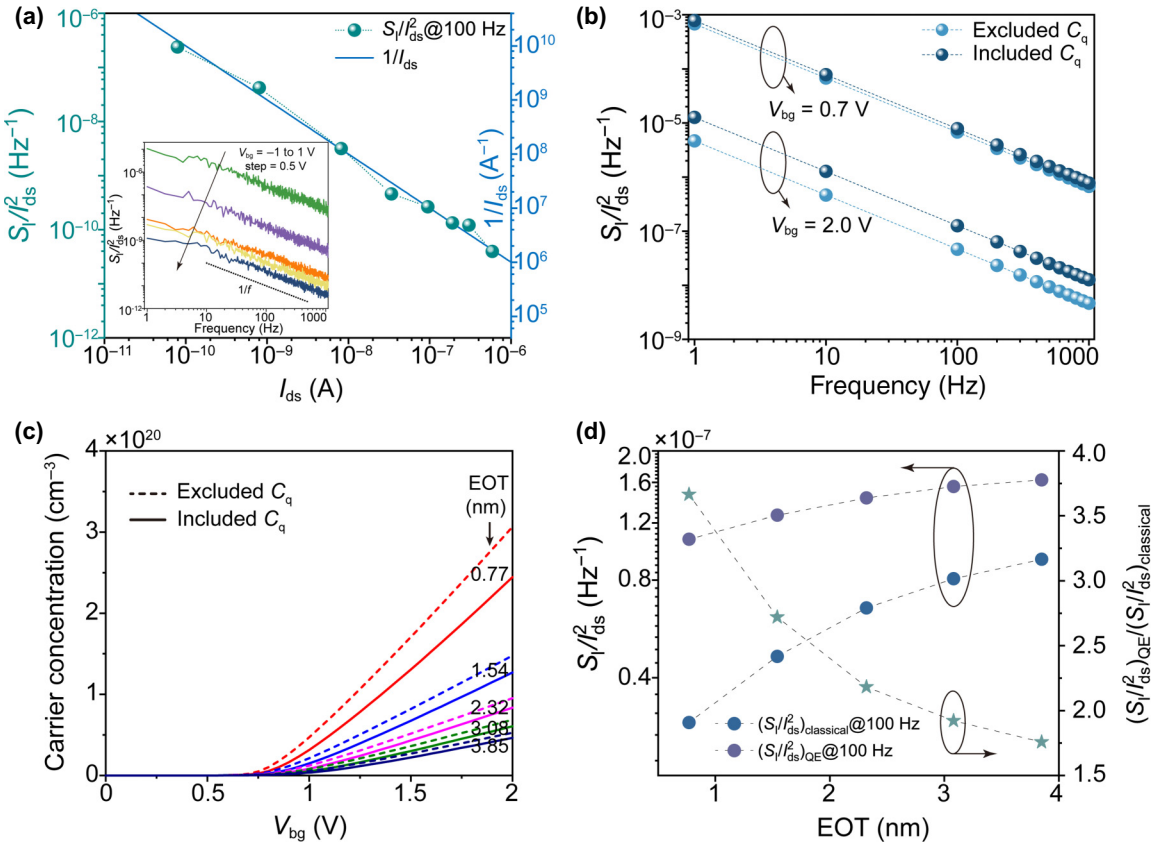

FIG. 4. (a) Normalized current power spectral density S_I/I_{ds}^2 as a function of I_{ds} for a multilayer MoS_2 transistor at $f = 100$ Hz. The inset shows S_I/I_{ds}^2 versus f at different gate voltages. (b) Simulated LFN characteristics (S_I/I_{ds}^2 versus f) of a 10-nm-thick MoS_2 FET with EOT = 1.54 nm, in subthreshold region (V_{bg} = 0.7 V) and strong accumulation (V_{bg} = 2.0 V). (c) Channel carrier concentration as a function of V_{bg} with various EOTs. (d) Noise amplitude S_I/I_{ds}^2 calculated with quantum effect $(S_I/I_{ds}^2)_{QE}$ and without quantum effect $(S_I/I_{ds}^2)_{classical}$ and the ratio between $(S_I/I_{ds}^2)_{QE}$ and $(S_I/I_{ds}^2)_{classical}$ as a function of EOT at V_{bg} = 2.0 V.

D. LFN in multilayer MoS_2 transistors

For the multilayer transistors, to further understand the impact of quantum capacitance on LFN, experimental characterizations are conducted with an approximately 10-nm-thick MoS_2 transistor. Figure 4(a) shows the measured S_I/I_{ds}^2 varies with I_{ds} as $1/I_{ds}$ on a log-log scale suggesting the LFN behavior tends to follow the HMF model closely. Here, the HMF model is associated with channel carrier concentration and can be given by [50]

$$\frac{S_I}{I_{ds}^2} = \frac{q\alpha_H}{fWLQ}, \tag{4}$$

with α_H representing the Hooge parameter and W and L denoting the width and length of the channel, respectively. Since C_q cannot be strictly extracted from $\partial Q/\partial V_{ch}$ in multilayer cases (C_{dep} has to be included), we construct a 10-nm-thick back-gated MoS_2 transistor with EOT = 1.54 nm in the TCAD platform to analyze the LFN behavior, with the HMF model and quantum effect (i.e., quantum capacitance C_q) included. See Note S2 within the Supplemental Material for the detailed TCAD model [37] (including Refs. [53,54]). The results are shown in Figs. 4(b)–4(d). We note that the LFN amplitude S_I/I_{ds}^2 in weak accumulation (V_{bg} = 0.7 V) remains approximately unchanged, whereas C_q causes an increment of S_I/I_{ds}^2 in strong accumulation (V_{bg} = 2.0 V). More details about the channel carrier concentration are presented in Fig. 4(c), in which C_q conspicuously limits the channel carrier densities in strong accumulation and thereby degrades the LFN performance. Scaling EOT from 3.85 to 0.77 nm, the channel charges get substantially reduced, and thus the noise amplitude calculated with quantum effect $[(S_I/I_{ds}^2)_{QE}]$ is significantly larger than that without quantum effect $[(S_I/I_{ds}^2)_{classical}]$, with an increasing ratio between $(S_I/I_{ds}^2)_{QE}$ and $(S_I/I_{ds}^2)_{classical}$ as depicted in Fig. 4(d). That means that deterioration of the noise performance is further enhanced by quantum capacitance C_q, while implementing high-κ or

scaled gate dielectrics in the multilayer MoS_2 transistor.

III. CONCLUSION

In this study, we comprehensively investigate the quantum capacitance (C_q) and LFN for monolayer and multilayer MoS_2 transistors, as well as the impact of C_q on LFN. For an atomically thin channel, C_q leads to an incremental loss of the total gate capacitance C_g while scaling the EOT, thus inevitably impacting other electrical parameters like transconductance, channel carrier density, and LFN. In these MoS_2 transistors, we clarify the origins of their LFN behaviors and determine theoretical models of the drain-current fluctuations. It is found that LFN in monolayer devices follows the CNF model featuring correlated surface mobility fluctuation, and their amplitude gets effectively suppressed in the subthreshold region but enhanced in accumulation because of the transconductance efficiency modulated by C_q. In contrast, the HMF model dominates the LFN mechanism for multilayer cases. And C_q mainly impacts LFN in strong accumulation, in which the channel carrier density is restrained and resulting in an enhancement of S_I/I_{ds}^2. This limitation is increasingly pronounced when EOT is scaled. We expect that this work can provide a more accurate analysis of noise characteristics in nanoscale 2D transistors, and help in improving the performance and reliability of 2D electronic devices and circuits.

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DATA AVAILABILITY

The data that support the findings of this article are not publicly available upon publication because it is not technically feasible and/or the cost of preparing, depositing, and hosting the data would be prohibitive within the terms of this research project. The data are available from the authors upon reasonable request.

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