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Characterization and Modeling of SOI RF integrated components

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Introduction

The boom of mobile communications leads to an increasing request of low cost and low power mixed mode integrated circuits. A very high degree of integration, a lower power consumption and the use of a lower supply voltage are the goals set for new developments in wireless transceiver design. Present-day transceivers often consist of a three or four chip-set solution combined with several external components. The required number of external components is linked to the physical limitations of the analog front-end topology. A further reduction of the number of external components is essential to obtain lower cost, power consumption and weight. The evolution of wireless transceiver design will be the realization of the complete transceiver (analog and digital processing) on one chip. Submicron CMOS technology appears to be a feasible and cost-effective integration solution for mobile communication systems. Effectively, the maturity of silicon-based CMOS technology for small device feature size and low voltage digital circuits and also the recent progresses of MOSFETs microwave performances explain the silicon success compared to III-V technologies.

Since the gate length of MOSFETs transistor has become in the sub-micron range, cut-off frequencies above tens of GHz are observed for sub-micron MOSFETs. As they exhibit gain up to several GHz, circuits operating at microwave frequencies, such as low noise amplifiers (LNA) or oscillators can be realized. But high quality passive elements, such as inductors, capacitors or transmission lines are needed to obtain high performances circuits.

Unfortunately, the fabrication of high quality passive elements is quite difficult due to two major limitations of silicon-based technologies which are the relatively high losses linked to the silicon substrate itself and the relatively thin metal layers used for interconnections. The main proposed solutions to overcome the parasitic substrate effects are the use of high resistivity silicon substrates, a very thick isolating oxide layer between passive components and the substrate, the silicon substrate removal below the passive components by micromachining techniques and the use of a patterned ground shield that avoid the electric fields to penetrate into the substrate. Thicker metallization and

stacking of multiple metal layers are used to reduce the conductor dissipation.

In order to develop low power, high performance circuits, a good characterization and modeling of all passive and active components are required over the whole frequency band.

The present work concentrates on the study of integrated components that are fundamental in the design of microwave circuits. Along the different chapters, various topics covering the measurement, the characterization and the modeling of integrated MOSFETs, inductors and transmission lines are presented. The content of each chapter is briefly described hereafter:

In order to model and characterize accurately various electronic components, a good understanding of the substrate used is required; this is the goal of the first chapter. The technological aspects of the various SOI materials that have been used in this work are presented. The influence of the thickness of the active silicon film on the electrical properties of MOSFETs is given allowing the definition of the Partially and Fully depleted SOI MOSFETs. The influence of various mechanical substrates on the RF performances of integrated components is discussed. Their advantages and drawbacks for RF analog applications are presented.

The concepts that are involved in the RF measurement methods are presented in the second chapter. Based on the power- and pseudo-waves definition, the scattering parameters are defined. They are measured using a Vector Network Analyzer (VNA). This equipment allows us to determine both the amplitude and the phase of the measured parameters. In order to make accurate measurement, the VNA must be calibrated. The general Thru-Attenuation-Network (TAN) calibration algorithms are detailed.

Usually, the measurement of integrated components directly on the silicon wafer, or on-wafer measurement, is performed in two steps. First a rigorous calibration using commercial and certified standards is performed, then a second one, using standards fabricated on the wafer. This second calibration is usually the Thru-reflect-Line algorithm, which suffers from few limitations. To reduce one of them, the determination of the characteristic impedance of the line standard, a new method has been developed.

The MOSFET transistors are the active devices used by the engineers to design SOI circuits operating at microwave frequencies. MOSFETs must then be accurately characterized to design efficient circuits. In the third chapter, answers are given to the following questions:

"What is equivalent circuit of a MOSFET transistor?"

"How to determine the equivalent circuit of a MOSFET?"

Starting from the physical properties of the field effect transistors, the equivalent circuit of the SOI MOSFET is built. All parasitic effects, which influence the RF behavior of the transistors, are modeled using discrete electrical elements, like resistances, inductances and capacitances. The equivalent circuit is defined to correspond to the RF properties of the integrated device. An extraction procedure of the equivalent circuit is proposed, including an original method to determine parasitic capacitances. Deep-submicron Partially, Fully Depleted SOI MOSFETs are used to illustrate the proposed procedure.

The aim of the fourth chapter is to study alternative structures of transistors, which can exhibit better performances than MOSFET in the field of low power, low voltage RF applications. Two alternative structures are studied, the Dynamic Threshold MOSFET (DTMOS) and the Graded Channel MOSFET (GCMOS).

The DTMOS is a MOSFET transistor having its body connected to the gate. It is fabricated in Partially Depleted technology. The body contact brings numerous advantages in DC operations compared to classical MOSFETs, like a reduction of the threshold voltage and a higher current drive capability. The AC behavior of this transistor is studied into details, covering low and high frequency operation.

The GCMOS is an asymmetric doped channel MOSFETs, which exhibits several benefits compared to a classical, uniformly doped, MOSFET. Higher current drive, transconductance and lower output conductance are some of its properties that can be deduced from DC analysis. The properties of GCMOS structure are investigated in order to determine its limits, for both low and high frequency applications.

Passive elements are one of the major limiting factors to realize high performances and low power system-on-chip microwave circuits. It is then necessary

to understand the mechanism affecting the performances of passive elements, and to optimize their structure in order to increase the circuit performances.

In the fifth chapter, a brief analysis of transmission line topology is presented. Then, we show a complete analysis of square spiral inductors made on SOI technology. An original model of integrated inductor is given. By using a coupled lines approach, the model developed allows us to study the influence of the topology of inductors, and also the influence of the underlaying substrate on the properties of the inductor. Furthermore, some design rules of integrated inductors are provided.

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