

Université catholique de Louvain

EPL - École Polytechnique de Louvain
ICTEAM - Information and Communication Technologies,
Electronics and Applied Mathematics

Routes Towards Novel Active Pressure Sensors in Thin Film SOI Technology

Dissertation présentée en vue de l'obtention du grade de
Docteur en Sciences de l'Ingénieur
par

Benoit Olbrechts

Promoteur:
Prof. Jean-Pierre Raskin

December 15, 2011



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To my parents
Pierre and Alice Olbrechts,
Bernard and Jacqueline Golard,
my wife Lara,
and my daughter Hermione

Abstract

The present work is subdivided in two parts. Both parts are in line with the 'More than Moore' ITRS roadmap as they serve either application driven CMOS-based components or tri-dimensional (3D) integration.

The first part deals specifically with the association of very thin dielectric membranes with FD SOI CMOS devices directly integrated on them. The combination of these two elements is as much an opportunity as it is a challenge.

Indeed, it is an opportunity because it opens the way for making innovative pressure sensing structures, beneficing of the inherent characteristics of SOI technology, being mainly (ultra-) low power capabilities, high temperature operation and radiations hardening. These qualities are utmost valuable for integrated pressure sensors. Moreover, the technology offers the possibility of developing simple and novel active sensing architectures, comprising current-to-frequency conversion solutions. This feature brings about intrinsically digital properties to the sensors through a noise sensitivity reduction and an interfacing ease. The thin membrane with CMOS devices association is all the more an opportunity as making very thin dielectric membranes is eased from a process point-of view, taking advantage of the SOI buried oxide (BOX) that acts as a natural etch-stop layer. The thickness of the membrane can then be very well controlled and uniform. Besides, it offers an important scientific interest because this association of MOS devices with very thin membranes is completely unedited about its mechanical aspect as it is about the electro-mechanical point-of-view. Furthermore, due to the integration of the MOS devices onto the membranes, thin films stacks and theirs respective patterning shapes are particularly complex. This complexity, added to unusual dimensional ratios between horizontal and vertical axes, makes the handling such systems a challenge, materially and under numerical simulations.

By means of fabrication, material characterization, electrical characterization and numerical simulations, the present work traces significant advances in the study of such systems and pushes towards their validation as functional sensors, in particular by the successful realization of demonstrators.

The second part, while being connected to the first part, does not restrict to pressure sensing applications. In fact, it explores wafers assembly in the frame of Direct Wafer Bonding (DWB) experiments, pursuing an overcome on the third dimension of integrated circuits.

DWB is a technique particularly attractive because it is fully CMOS-compatible, provided that the thermal budget is respected. The absence of intermediate layer of heterogeneous material bring unique properties such as high temperature withstanding and limited

stress generation at the bonded interface. Low temperature or even room temperature process is possible with the help of surface activation treatments. For these reasons, DWB can be implemented as a front-end process step as well as a back-end process step. In front-end, advanced substrates preparation is its main application. In back-end, MEMS packaging and CMOS 3D-integration are usually targeted. Nevertheless, as this bonding process has to occur directly between brittle materials (typically Si and/or SiO_2), the technique is very sensitive to surface contamination as well as to surface roughness. These are the two main process limiting parameters. Besides, the chemical and physical mechanisms involved in DWB are still topics under investigations.

In this work, general case-studies are conducted bringing valuable scientific contributions concerning its fundamental mechanisms as well as contributions in the frame of precise applicative contexts like the fabrication of planar double gate transistors. These investigations are all made with the CMOS process compatibility as a requirement.

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Awards

Best Student Paper Award - International IEEE Silicon-on-Insulator (SOI) Conference, Tempe, Arizona, October, 3-6 2011.

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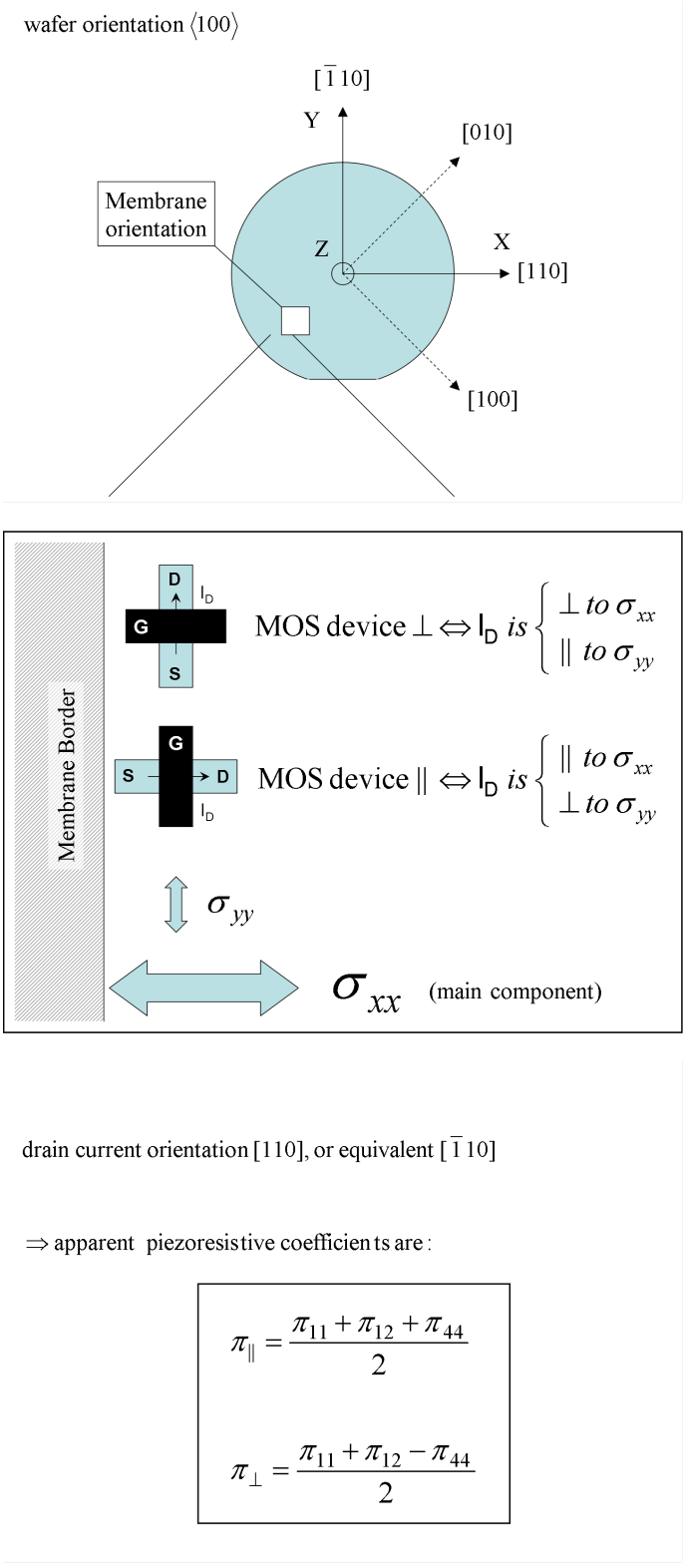


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Part I

Introduction

Chapter 1

Context and Motivations

1.1 Introduction

The present thesis is constituted of two parts. In the first part, the potentialities of a novel active pressure sensing concept are explored, while in the second moves on contributions based on direct wafer bonding technological step.

In this chapter, the scientific context is presented and the specific questions, addressed in this work, are highlighted sequentially for each part.

1.2 Technologies of MEMS Pressure Sensors

Pressure sensors constituted the earliest volume application of Micro-Electro-Mechanical Systems (MEMS), being mass produced since mid-1970s. Nowadays, they still represent one of the largest MEMS markets [26]. IHS iSuppli announces that the pressure sensors generated a revenue of USD 1.22 billion during year 2010 and forecasts that, by 2014, it will grow up to USD 1.85 billion, making of them the top MEMS devices market [50].

Their application domains shifted from high cost, low volume, niche military and industrial use towards automotive sector when appeared electronic engine regulation, first with the air/fuel ratio control by the manifold air pressure (MAP) and later with fuel rail and tire pressure [26]. In 2011, the automotive sector remains the widest area for MEMS pressure sensors, comprising 72 percent of the revenue, followed by medical electronics at 11 percent and the industrial segment at 10 percent. The remaining 6 percent of the market is split between consumer electronics on the one hand, and military-aerospace on the other [50].

A wide variety of pressure sensing technologies is available. Most of them rely on the deflection of a diaphragm, transducing its displacement into an electrical signal. They are described here after, mainly from Beeby [18], Eaton [55] and Yurish [183].

1.2.1 Piezoresistive - Bulk Micromachined Sensors

The most widely spread architecture of pressure sensors takes advantage of the piezoresistive nature of silicon, which modulates its resistivity according to an applied mechanical stress. Its consists in the diffusion or implantation of resistors located at the borders of a silicon diaphragm (Figure 1.1). These resistors are classicaly oriented by pairs in opposite crystalline orientations and connected in Wheatstone bridge configuration (Figure 1.2).

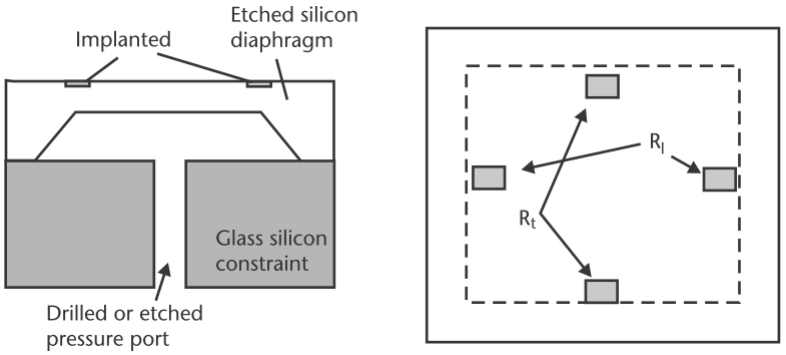


Figure 1.1: Sectional-view and top-view of typical piezoresistive bulk-micromachined pressure sensor; [18].

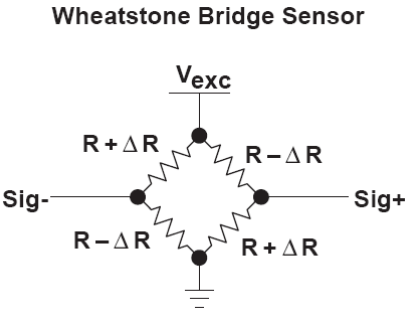


Figure 1.2: Schematics of Wheatstone bridge generally involved in piezoresistive pressure sensors; [18].

Membranes are generally released by a back-side etching in KOH, an anisotropic Si etching solution. Three methods may be used to stop the etching and, hence, control the membrane thickness: (i) time control, (ii) diffusion of a p+ doped etch-stop layer combined with the growth of an epitaxial layer, (iii) electrochemical etch-stop at a reverse-biased p-n junction. The technique of an electrochemical etch-stop on an epitaxial layer offers a precision of 0.2 μm [93].

An important limitation of diffused or implanted resistors transducers is the maximum operating temperature which cannot rise above 120 °C, due to the p-n junctions leakage

current in the resistors. If higher temperature operation is requested, polysilicon [153], silicon islands on SOI substrates [86] or SiC [178] are available technological solutions.

It is worth to note that, instead of increasing the diaphragm dimensions, a way to improve the pressure sensitivity may consist in the insertion of a boss at the central region of the diaphragm. Indeed, the stress is then concentrated near the edges of the boss, where the resistors have to be located. Such configuration is illustrated in Figure 1.3.

Besides, compact configurations, e.g. for medical use, may be achieved by fabricating the diaphragm in Front-End-Of-Line (FEOL), implementing a fusion wafer bonding step and transferring a silicon film over a pre-etched cavity [134], as illustrated in Figure 1.4.

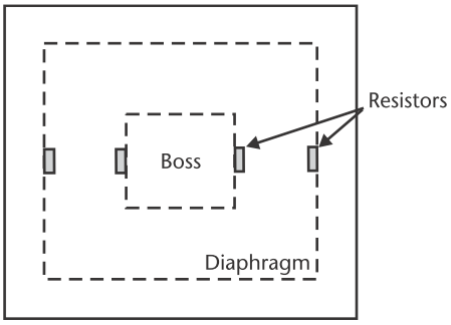


Figure 1.3: Top-view of piezoresistive bulk-micromachined pressure sensor with bossed diaphragm; [18].

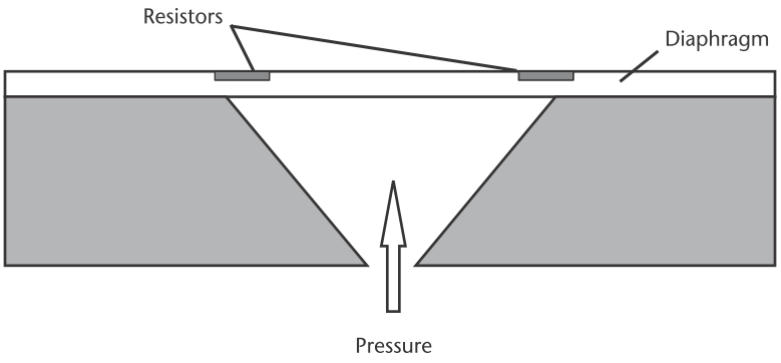


Figure 1.4: Sectional-view of piezoresistive bulk-micromachined pressure sensor with a diaphragm formed by a transferred layer by fusion direct wafer bonding in front-end-of-line; [18].

1.2.2 Piezoresistive - Surface Micromachined Sensors

As an alternative to volume machining, mobile diaphragms may be released by a front-side attack of a sacrificial layer i.e. by surface micromachining. Such topology is illustrated

at Figure 1.5. The diaphragms are made of deposited materials which are typically either polysilicon, with an SiO_2 sacrificial layer, or Si_3N_4, with a polysilicon as sacrificial layer. The volume underneath the diaphragm may be vacuum sealed by the use of a Chemical-Vapor-Deposition (CVD) process. The piezoresistors are of polysilicon.

The main advantages of surface-micromachined architectures compared to bulk-micromachined are their reduced size and, by the way, their lower cost. They offer furthermore simplified integration with electronics, easing the co-integration of a temperature sensor for compensating the temperature dependency of the sensor. Nevertheless, piezoresistive surface-micromachined pressure sensors generally suffer of a limited measurable pressure range, a limited sensitivity with pressure augmented by reproducibility limitations [55].

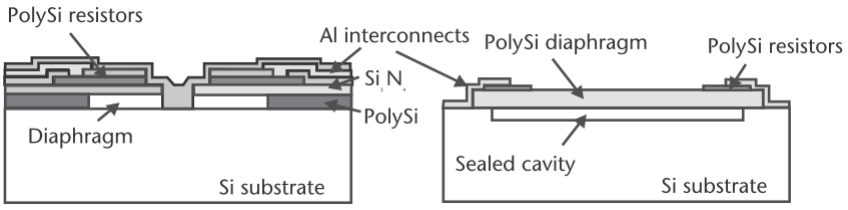


Figure 1.5: Piezoresistive surface-micromachined pressure sensor with a nitride (left) or polysilicon (right) diaphragm; [18].

1.2.3 Capacitive Pressure Sensors

Capacitance variation is also a widely used sensing principle. Based upon parallel plates pairs structures, MEMS capacitive pressure sensors are classically fabricated with the assembly of a bulk-micromachined wafer onto a metalized glass wafer by anodic bonding, as illustrated in Figure 1.6.

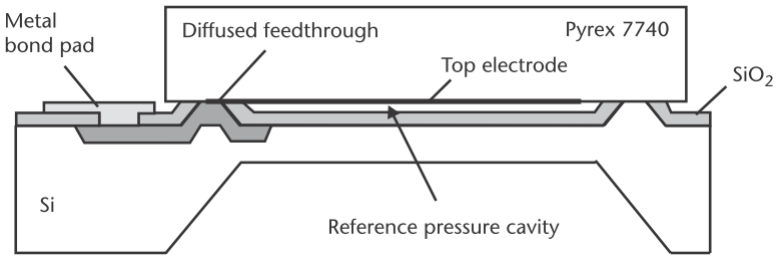


Figure 1.6: Capacitive bulk-micromachined pressure sensor; [18].

When starting from a SOI Wafer, a surface-micromachined capacitive pressure sensor may be easily fabricated by using the buried oxide film as sacrificial layer (Figure 1.7). The SiO_2 etching is performed isotropically from a patterned hole in the top silicon thin

film, yielding a circular-shape diaphragm. The central hole is later vacuum sealed by a silicon nitride deposition. Surface-micromachined architectures are more common nowadays. Typical applications are in the medical sector: intravascular blood pressure and intracranial pressure (coated with a silicon elastomer).

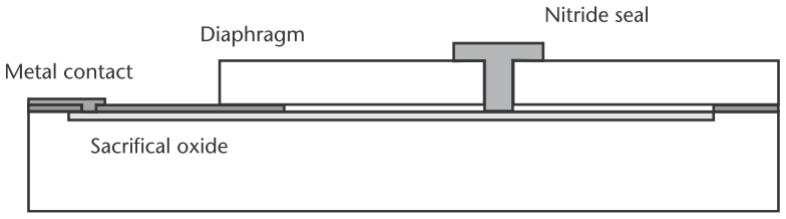


Figure 1.7: Capacitive surface-micromachined pressure sensor on SOI wafer; [18].

The main advantages of capacitive pressure sensors are (i) a high sensitivity, (ii) a low-power consumption and (iii) a low temperature cross-sensitivity. Their main drawbacks are (i) their non linear output, (ii) the complexity of the associated electronics and (iii) their sensitivity to parasitic capacitances that require, ideally, a co-integration of the electronics. The non linearity of the output is above all due to the relative movement of the electrodes which do not remain parallel under high pressure values. Solutions are the implementation of bossed diaphragm, the clamping of the diaphragm at its center or the use of the sensor at higher pressure, in touch mode (Figure 1.8). Besides, in order to increase the measured capacitance signal, sensing diaphragms may be connected in arrays, eventually with various pressure sensitivities.

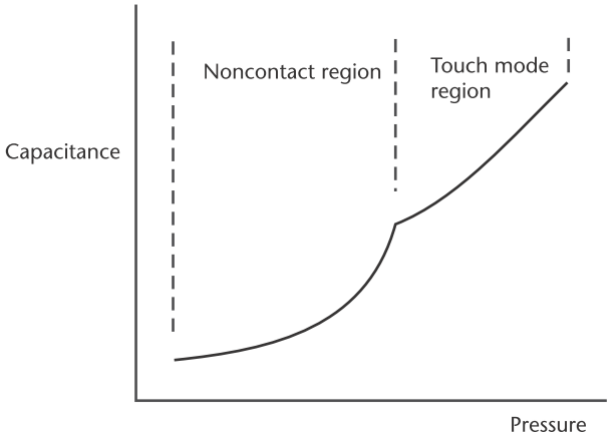


Figure 1.8: Typical capacitance curve as a function of the pressure when the diaphragm is in touch-mode or not; [18].

1.2.4 Resonant Pressure Sensors

Last sensing method consists in a mechanically resonating structure which is strained by a pressure-deflected diaphragm. The resonance frequency is hence modulated by the applied pressure. A typical block diagram of resonant pressure sensors is printed in Figure 1.9.

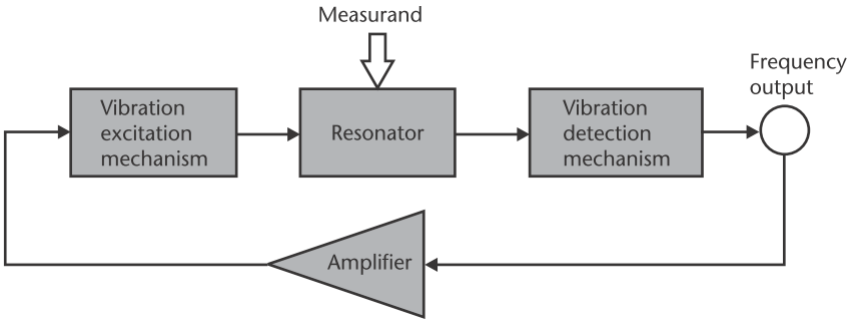


Figure 1.9: Block diagram of a resonant sensor. [18].

Such pressure sensor architectures are usually implemented either in quartz or in silicon technology (Figure 1.10). The main interest of quartz material is its piezoelectric properties, easing the sensor excitation as well as the oscillation signal detection. However, the quartz option suffers from limitations in micromachining options. Silicon technology resonant sensors offer the opposite characteristics: various manufacturing options and the necessity to incorporate excitation and detection mechanisms.

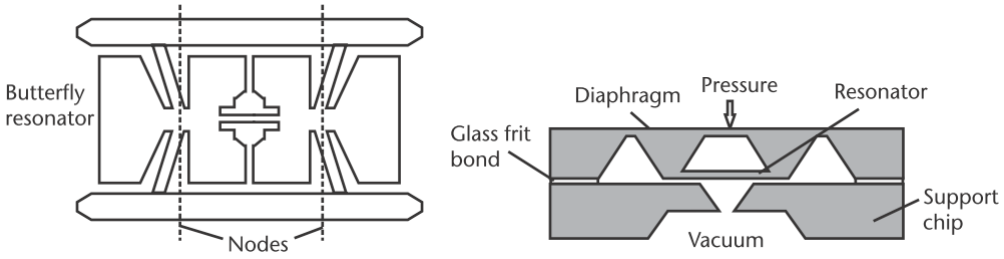


Figure 1.10: Structures of resonant pressure sensors in (a) quartz and (b) silicon materials. [18].

The advantages of resonant pressure sensors are their stability and their accuracy. They have been developed in particular for high pressure applications in oil and gas industry. Their main drawbacks are a challenging fabrication and their price.

1.2.5 This Work - A Novel Concept of Pressure Sensor

In the present work, a novel concept of pressure sensor is presented. This concept is based on the combination of three main characteristics:

1. Thin Dielectric Membranes,
2. Fully-Depleted (FD) Silicon-on-Insulator (SOI) CMOS (Complementary Metal-Oxide-Semiconductor) Technology,
3. Active Transducers.

This work follows up the remarkable PhD thesis of Dr. Jean Laconte, book edited by Springer [100]. Under the title "Micromachined Thin-Film Sensors for SOI-CMOS Co-Integration", the concepts of flow and gas sensors using materials and films directly available from the standard SOI process are developed. The active part or the sensors were implemented on very thin dielectric membranes for their unique thermal insulation properties, lowering the power consumption of the sensors. The present thesis exploits such thin membranes as a mechanical support where to locate pressure transducers. The motivations underlying the three basic principles of the presented concept are expressed here below.

Thin Dielectric Membranes

First, the opening part of this work is based on the use of multilayered thin film membranes. Their interest comes from their flat aspect ensured by a selected films stack in terms of materials and thicknesses. Most of the films constituting the membrane are directly available from the FD SOI CMOS process. The use of such membranes is particularly encouraged by the technological opportunity that they represent. Indeed, their release may be achieved easily thanks to a silicon oxide film as bottom layer. This layer stands as a very effective etch stop during a TMAH wet back-etching.

FD SOI CMOS Technology

Second, SOI wafers are ideal substrates for providing the needed SiO_2 etch-stop layer for the thin membranes release, yielding very uniformly thin membranes. Moreover, beyond easing the membranes fabrication, a FD SOI technology offers advantageous electrical qualities which are mainly (ultra-) low power and high temperature operation capabilities as well as a radiations hardened behavior. These qualities are utmost appreciated, particularly in portable/autonomous and harsh environment applications.

Active Transducers

Third, in this work, active CMOS transistors play the role of transducers converting mechanical stress variations to electrical signals. Compared to classical diffused resistors, the use of MOS devices allow to reduce considerably the size of the transducers, involving by the way a possibility for reducing membranes sizes. In addition, active character of the transducers enables their direct integration into oscillating circuits. This fact offers a direct and intrinsic digital behavior to the system. Indeed, three approaches may be

figured out for smart sensors with digital output (Figure 1.11): (i) the sensing part delivers an analog voltage or current which is connected to an Analog-to-Digital Converter (ADC), (ii) the sensing part of the system delivers directly a frequency output which is connected to a Frequency-to-Digital Converter (FDC), (iii) the analog signal of the sensing part is converted into a frequency signal which in turn is connected to a FDC. The conversion from analog to frequency signals may be as simple as a ring oscillator, while the simplest form of FDC is a counter. Rising edges of frequency signals may be either counted over a determined period of time or the signal be sampled at a determined rate. Mr. Sergey Yurish summarizes the advantages of sensors with frequency output in [183]. Main of them are high noise immunity thanks to the frequency modulation, a wide dynamic range and a simple interfacing. Moreover, by the fact that the complete electronic circuitry may be directly co-integrated with the sensing part of the sensor, a finalized sensor architecture may result in a System-on-a-Chip (SoC) rather than a System-in-a-Package (SiP) requiring additional packaging operations and costs.

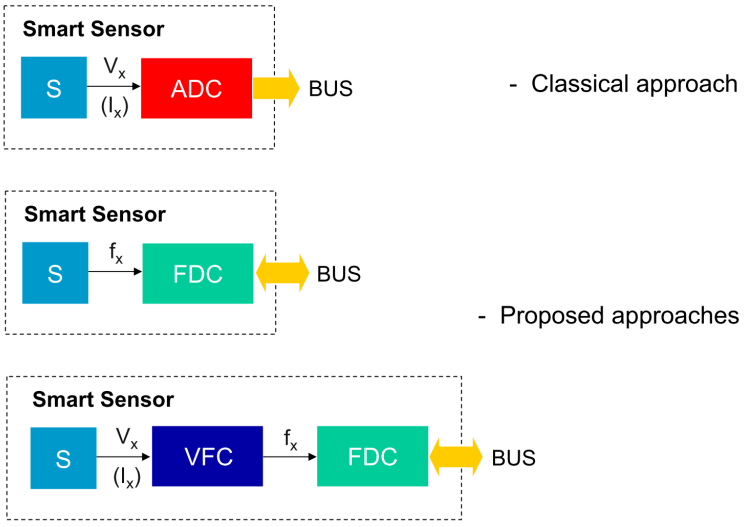


Figure 1.11: Block diagrams of three possible approaches for digital output sensors. [8].

Bringing together these three basic elements opens a way for making innovative pressure sensors featured with all electrical and topological qualities cited here above. Compared to classical piezoresistors on silicon membranes configuration, the presented concept enters a new paradigm (Figure 1.12). Indeed, thick and monolithic diaphragms are replaced by thin and multilayered structures. Surface diffused resistors are substituted by middle-fiber MOS devices involving the presence of various materials with vertical and lateral patterning. Such pressure sensor configuration has not been reported yet and do present very specific outcomes.

Mr. Felix Mayer, CEO of Sensirion AG, has entitled his invited talk at EuroSensors 2010 Conference: "From stepping into an opportunity Gap to continuous Innovation",

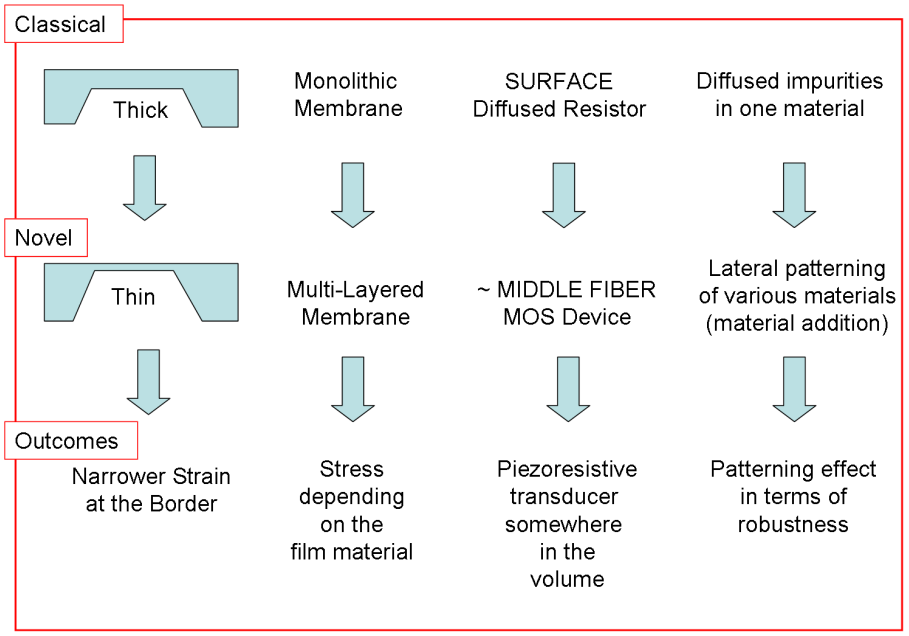


Figure 1.12: Diagram summarizing the paradigm changes bewteen a pressure sensor based on a classical piezoresisitive bridge on Si monolithic membrane architecture and the approach proposed in this work.

mentioning thereby that his company was founded on a technology gap in the humidity sensors field. The following question then arises. Does such technology gap exist concerning pressure sensors that could be filled with our proposed concept? This work tries to give substantial elements to answer that question and, incidentally, the driving questions that are thoroughly developed in the present work are: "Can we really make functional pressures sensors with this concept as postulate?", "How do such structures behave mechanically?", "What could be their operating pressure range?", "What sensitivities to the pressure may we expect?"

In a parallel way, recent research results show that there exists a giant piezoresistive effect in silicon nanowires [74]. It is worth to investigate whether thin dielectric membranes are suitable devices supports to study electronic transport at high stress levels. Then the question is: "Is there a way to model robustly the stress/strain in suspended silicon structures on such thin dielectric membranes?"

By means of fabrication, material characterization, electrical characterization and numerical simulations, the present work traces significant advances in the study of such novel pressure sensors and pushes towards their validation as functional sensors, in particular by the successful realization of demonstrators.

Outline of Pressure Sensing Systems Part - II

Chapter 2 further introduces the concept of "Novel Active Pressure Sensors in Thin Film SOI Technology" with first experimental demonstrations and characterization of MOS devices as well as complete ring oscillators suspended on thin dielectric membranes. The systems behavior at high temperature is also investigated, up to 200 °C.

Chapter 3 deals with mechanical properties of thin multilayered membranes. Deflection and burst pressure measurements are presented, evidencing the fragility of functionalized membranes. Finite Element Modeling (FEM) is performed in order to establish the stress/strain distribution in thin and blanket or patterned plates. Mechanical experiments show the role of subtractive as well as additive patterning.

In Chapter 4, several novel configurations, based on the design recommendation established in Chapter 3, are electromechanically characterized. It offers an exploration of some possible designs and transducers positions on the membrane. The sensitivities to the pressure as well as the burst pressures are reported. Besides, a drift effect is newly observed and assessed.

In Chapter 5, a particular pressure sensing configuration is further investigated attempting to address the stress/strain value in the silicon channel of suspended devices. In that frame, transistor current variations under pressure, technology-specific piezoresistive coefficients and numerical simulations are confronted trough the prism of the piezoresistive theory.

1.3 Wafer Bonding for Packaging and Special Substrates Preparation

Besides pressure sensing systems, wafer bonding technology is investigated in this work. Both axes of work of this thesis are in line with the "More than Moore" development direction in the International Technology Roadmap for Semiconductors (ITRS), as illustrated in Figure 1.13. Indeed, this direction notably aims to the emergence of novel applications bringing new functionalities and portability. The new functionalities are, for instance, met by the development of multi-sensors systems with embedded advanced intelligence. The portability is ensured by a limited power consumption and/or power scavenging and a reduced form factor. One technique used for incorporating such new functionalities is wafer bonding.

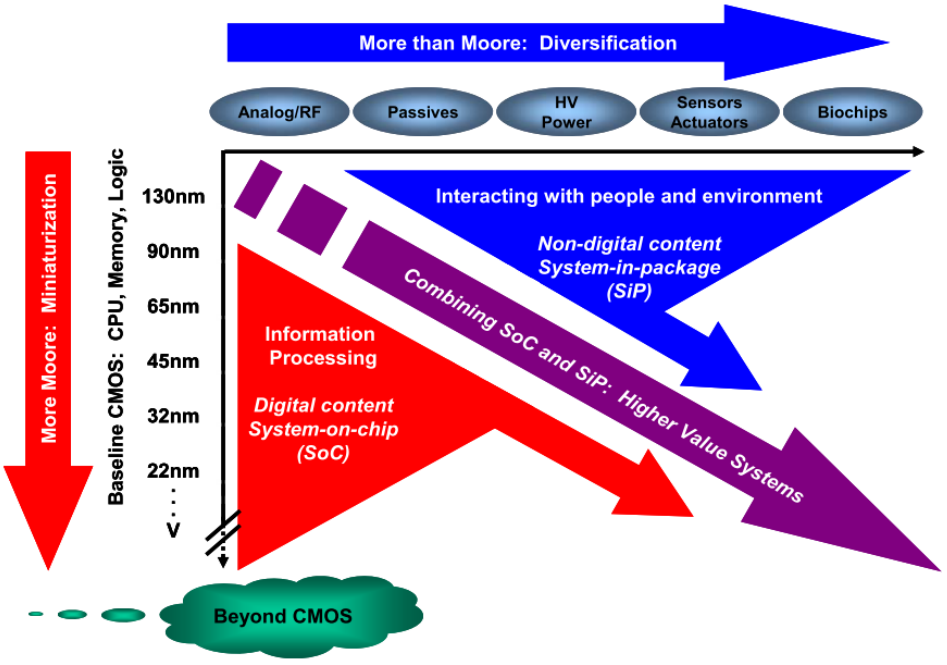


Figure 1.13: The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions (More Moore) and functional diversification (More-than-Moore); [1].

1.3.1 Wafer Bonding - Technologies and Applications

Wafer bonding technology concerns directly pressure sensing systems but is certainly not restricted to them. Indeed, its applicability has become almost as wide as the microfabrication sector itself. According to Mr. Roy Knechtel, nearly 70% of wafers processed at X-Fab require wafer bonding, sometimes even twice [94]. Looking at Figure 1.14 gives

an overview on the final products or intermediate processing stages that make use of wafer bonding, ranging from all kinds of MEMS, CMOS image sensors, LEDs or power electronic devices to advanced substrates and advanced packaging.

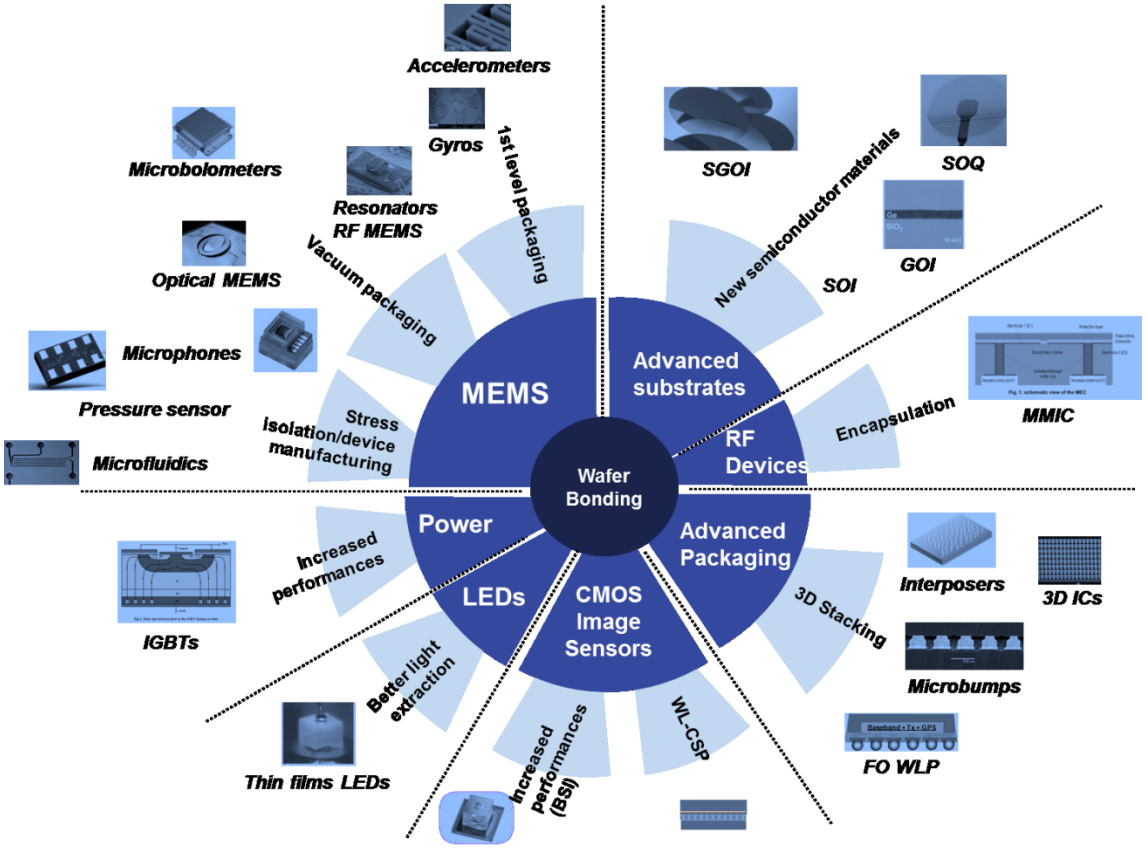


Figure 1.14: Overview of wafer bonding applications; [17].

Wafer bonding consists in the assembly of wafers to other wafers or of chips to wafers and encompasses diversified technologies involving different materials, operating conditions (force, electric field, temperature, etc.) and the presence or not of an intermediate layer.

Available bonding technologies are graphically classified in Figure 1.15 and briefly described here after.

- *Anodic Bonding* - This technique allows to bond Na-containing glass wafers to silicon wafers. The wafers pair is heated up to 300-500°C, giving a slight conductivity to both substrates, and a voltage is applied (typically 500-1000 V). This voltage involves a strong electrostatic force at the bonding interface, bringing them into intimate contact while the temperature increases locally, fusing materials at the interface. Anodic Bonding is a widely used technique for MEMS and microfluidic devices. Due to the presence of Na as well as the applied voltage, it is generally admitted that

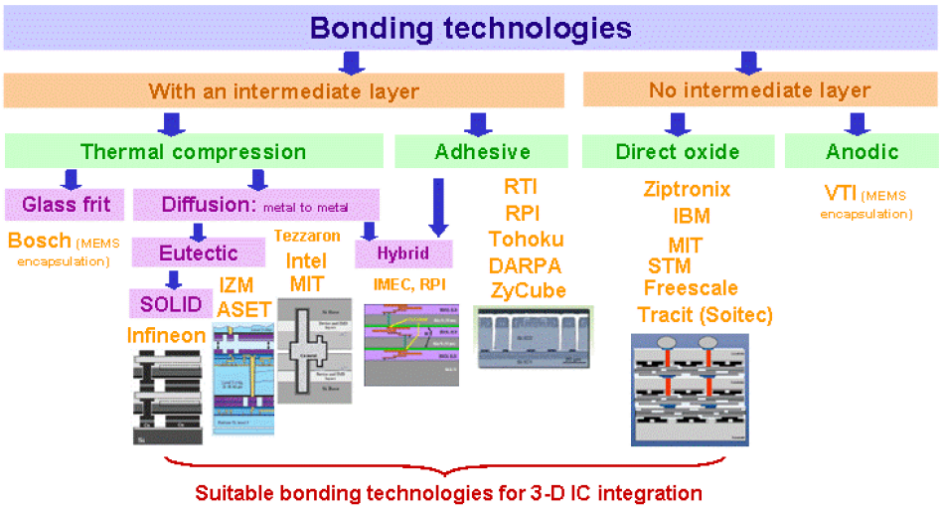


Figure 1.15: Overview of the different bonding technologies and their relative major actors; [49].

this method is not compatible with CMOS processed wafers. Nevertheless, Dr. Roy Knechtel has reported successful cavity sealing with co-integrated MOS devices [95].

- *Direct Wafer Bonding* - It is also named molecular or fusion bonding if high temperature are reached during a subsequent annealing. It designates a bonding process spontaneously occurring between sufficiently clean, flat and smooth surfaces of any material. Depending on the surface chemistry, three types of interactions may take place: Van der Waals forces, hydrogen bonds and stronger covalent bonds. In silicon wafer bonding, one distinguishes hydrophilic and hydrophobic processes.

  – The *hydrophilic process* concerns the bonding of Si surfaces with a native oxide and/or SiO_2 films. It relies on water adsorption on the surfaces to be bonded which enables hydrogen bonds to take place immediately at the contact. Covalent bonds are formed by polymerization of silanol groups and water removal from the interface [162], as formulated in the following reaction:

$$\equiv Si - OH + HO - Si \equiv \rightarrow \equiv Si - O - Si \equiv + H_2O \tag{1.1}$$

This mechanism is promoted by subsequent thermal treatments and/or surface activation prior to bonding. The yielded water may either diffuse along the bonding interface or oxidize Si, producing hydrogen atoms which diffuse easier:

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{1.2}$$

In order to favor silanol groups formation on hydrophilic surfaces, surface activation are performed before contacting the wafers. Most widely used methods

are warm nitric acid dipping and oxygen plasma. The effects of the plasma treatments are complex and were reviewed by Dr. Hubert Moriceau [119].

  - In the *hydrophobic process*, the native oxide is removed form the Si surfaces, yielding hydrogen- and/or fluoride-terminated silicon surfaces, according to the removal and cleaning procedures. A bonding surface energy enhancement by the formation of Si-Si covalent bonds can be obtained with thermal treatments above 600°C. Nevertheless, under the naming of Surface Activated Bonding (SAB), Prof. Tadatomo Suga has developped an original method yielding high surface energies at room temperature or low temperature annealing. It relies on an argon Fast Atom Beam (Ar-FAB) surface activation and a bonding performed in Ultra High Vacuum (UHV). Besides heterogeneous bonding in optoelectronic applications, this low temperature method is also effectively implemented for vacuum sealing cavities [80, 124].

- *Adhesive Bonding* - The bonded surfaces are "glued" together by the insertion of an adhesive polymer, typically SU-8 (epoxy-type) or BenzoCycloButene (BCB). This technique offers the following advantages: less sensitive to surface topography, low thermal budget is required, CMOS compatible, ability to join various dissimilar materials, robust and low-cost. Its drawbacks are: permeability to gas and moisture, temperature stability and long-term stability [54]. This technique is mainly used for the packaging of MEMS on the wafer level (WLP).

- *Hybride Bonding* - This configuration combines two (or more) bonding techniques on a patterned surface. It is for instance implemented for simultaneously establishing electrical contacts and mechanical bond. Such works are notably reported by Dr. Léa Di Cioccio [40] and Dr. Pierric Gueguen [69], for 3D integration applications, or by Stéphane Kuhne [99], for vertical interconnection of 3D MEMS.

- *Metal Bonding* - Metal bonding is the technique ensuring the highest vacuum levels in cavity sealing, thanks to the absence of bonding reaction outgassing and the perfect hermeticity of the bond [54]. Moreover, in 3D integration applications, this technique allows the mechanical and electrical connections to be made between two wafers in one step [3]. It is worth to note that direct bonding may also occur between metallic surfaces, as of any other material, at room temperature or low temperature annealing. Such experiments are notably reported by Dr. Tadatomo Suga [146, 173].

  - *Diffusion* - Metal diffusion bonding is based on the thermocompression of identical metal surfaces to be bonded, typically Cu-Cu, Al-Al or Au-Au. Metal diffusion also enables superior post bond alignment accuracy over glass frit bonding. It is worth to note that aluminum metallization is used frequently in MEMS device structures and offers the potential to serve as a sealing metallurgy during device packaging steps via a diffusion reaction. Advances in CMP techniques and deposition methods contribute to promote metal diffusion bonding instead of anodic or glass frit [3].
  - *Eutectic* - Metal eutectic bonding of wafers is based on the melting of solder-like alloys, typically Au-Sn or Au-Si, at relatively low temperatures comprised

between 200 and 500°C. It is used in advanced MEMS packaging and 3D integration technologies. A unique feature of eutectic metals is the melting of the solder-like alloys that facilitate surface planarization and provides a good tolerance on surface topography and particles. Eutectic bonding requires precise force delivery and controlled uniform temperature to control reflow of the eutectic material [4].

– *SLID* or *SOLID* (Solid-Liquid InterDiffusion) - This technique relies on a binary system of metals, typically Cu-Sn, where the first metal has a higher melting point than he second one. In practice, the second metal (Sn) is molten while the first one (Cu) diffuses in the solution. Once the solution saturates, a solid intermetallic compound (IMC) grows up until both wafers are solidly joined. The advantages of this method are a very high temperature resistance of the formed joins, very fine pitch and relatively low cost. A major drawback is a risk of overflow leading to short-circuits [108]

- *Glass Frit Bonding* - Glass Frit wafer bonding has been the traditional wafer bonding technique used in MEMS production and based on the use of low melting point glass. Glass frit applications include three axis accelerometers, gyroscopes and pressure sensors used in automotive, gaming and cellular phone technology [5].

Typical parameters values of wafer bonding processes and their figures of merit are summarized in Figures 1.16 and 1.17.

	No Intermediate Layer			Intermediate Layer					
	Anodic Bonding (Electric Field)	Direct Bonding	Plasma Activated Direct Bonding	Glass Frit	Thermo Compression	Solder / Eutectic / TLP	Adhesive	Epoxy (thermally cured)	Epoxy (UV cured)
Surface Roughness	< 20 nm	< 0.5 nm	< 1.5 nm	< 1000 nm	< 20 nm	< 1000 nm	< 1000 nm	< 1000 nm	< 1000 nm
Layer Thickness	NA	NA	NA	Typically 10 - 40 µm	Min. 300nm each side	Min. 500nm each side	Polymer dependent (from <1µm to few 100µm)	Polymer dependent (from <1µm to few 10µm)	Application dependent
Process Temperature	350 - 450°C	>1000°C (anneal)	100-400°C anneal	350 - 450°C	200 - 500°C depending on metal	200 - 500°C depending on metal	< 300°C depending on adhesive	< 300°C depending on adhesive	~ Room Temperature
Cleanroom Environment (FS209E)	100 to 1000	10 or 1	10 or 1	1000	10	100	100	1000	1000
Sensitivity to Particles	High	High	High	Low	High	Medium	Low	Low	Low
Sensitivity to Surface Contamination	High	High	High	Medium	High	High	Low	Low	Low
Na present	Yes	No	No	No	No	No	No	No	No
Cycle Time (minutes)	45 - 90	Bond ~ 1 Anneal - hrs	Bond ~ 1 Anneal 15min to 1-2 hours	45 - 90	30 - 90	30 - 60	5 - 45	15-30	5 -15

Figure 1.16: Summary of the main features of wafer bonding processes, [54].

	No Intermediate Layer			Intermediate Layer					
	Anodic Bonding (Electric Field)	Direct Bonding	Plasma Activated Direct Bonding	Glass Frit	Thermo Compression	Solder / Eutectic / TLP	Adhesive	Epoxy (thermally cured)	Epoxy (UV cured)
CMOS Compatible	No	No	Yes	No	Yes	Some	Some	Yes	Yes
Electrically Conductive	No	No	No	No	Yes	Yes	No	No	No
Hermeticity (vacuum sealing)	Medium to High	Medium to High	Medium to High	Medium	High	High	Low	Low	Low
Current Manufacturing Volume	High	High	High	High	Medium to High	High	High	High	High
Bonding Strength*	High	High	High	High	High	High	High	High	High
Max. Temperature Bond Can Withstand	> 1000 C	> 1000 C	> 1000 C	Lower than melting point of glass frit (<350°C)	Limited by melting point of metal	Limited by melting point of solder/ eutectic except for TLP is higher	Low, limited by adhesive (<150°C)	Low, limited by adhesive (<150°C)	Low, limited by adhesive

* For wafer bonding processes based on the use of intermediate layers the maximum bond strength may be limited by intermediate layer fracture strength.

Figure 1.17: Wafer bonding processes figures of merit, [54].

1.3.2 The case of 3D Integration

This Section is mainly based on [109].

The major drivers pushing towards the development of 3D integration are: (i) the form factor by reduced volume and weight as well as reduced footprint, (ii) the performance through improved integration density, reduced interconnect length, improved transmission speed, reduced power consumption and (iii) the heterogeneous integration in order to boost the functionalities (e.g. co-integration of RF, logic, memory and sensors) in a reduced space [82, 48].

Referring to Figure 1.18, three categories of 3D integration schemes are distinguished: (i) 3D packaging technology, (ii) transistor build-up and (iii) monolithic wafer-level back-end-of-line (BEOL) compatible.

- *3D packaging based technologies* offer a yield advantage, a short time-to-market thanks to less design effort but have a high cost in high volume production because an extensive testing is needed for extracting the known good dies (KGD). Moreover they have a low throughput due to the pick-and-place method used for the assembly. Typical technologies and applications are (a) System-in-Package (SiP) or Package-on-Package (PoP) for portable devices (cell-phones), (b) dies-stack with trough-silicon-vias (TSVs) for memories and (c) die-to-wafer assembly for 3D Systems-on-Chips (SoCs).

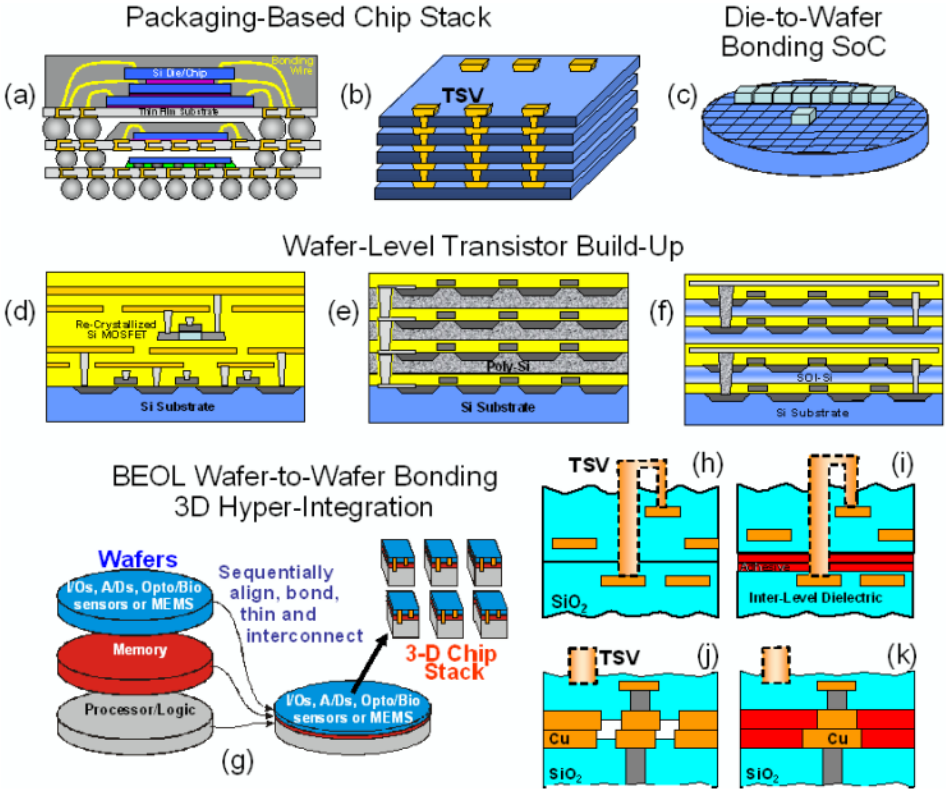


Figure 1.18: Schematic representations of major 3D integration approaches: (a-c) 3D Packaging technology, (d-f) Wafer-level transistors build-up 3D technology and (g-k) Wafer-level BEOL-compatible 3D technology; (h) SiO_2- SiO_2 bonding, (i) adhesive bonding, (j) Cu-Cu bonding, (k) hybrid metal/adhesive bonding. [109].

- The *transistor build-up approach* consists in the sequential fabrication of device layers either by deposition of amorphous silicon films (to be re-crystallized) or by fusion bonding of single-crystal silicon films. The thermal budget is related to the interconnect material which is usually of polysilicon or tungsten. Tungsten tolerates temperatures up to 600°C. This approach offers the highest density and is performed at a wafer-level which induces reduced costs for high volume production. Typical applications are repeaters, low performance memory or, for single crystal Si technologies, NAND flash memory.

- The *Monolithic Wafer-Level BEOL-compatible approach* is based on the assembly of fully processed wafers by aligned wafer bonding and substrate thinning. Inter-wafer interconnections are made either before ('via-first') or after wafer bonding ('via-last'). Typically the bottom wafer retains its full thickness and serves as a mechanical support for the stack. Each subsequent wafer is then thinned to micron scale after stacking (bonding), resulting in a stack with an overall thickness close to that of a single wafer. Hence, current packaging methods are applicable in this configuration.

The BEOL-compatible approach, also named 3D hyper-integration, is perhaps the most attractive 3D technology due to its flexibility for heterogeneous integration of different materials, processing technologies and functional components with additional benefits in cost and performance. Indeed, one can perform separately the choice on the electrical, RF, optical, thermal and mechanical behavior for each component. Furthermore, the starting yield can be improved by fabricating the logic and memory components on separate wafers with optimized materials and process technologies. The separate wafers are then stacked using a monolithic wafer-level BEOL-compatible process for all components, potentially improving the cost and overall system yield at high-volume production. Finally, massive (millions), short (micronscale) inter-wafer interconnects (vias) provide extremely high data bandwidth and dramatically decrease interconnect delay and power consumption.

The wafer bonding technologies associated with the BEOL-compatible approach are: (i) direct wafer bonding, (ii) adhesive wafer bonding and (iii) metal bonding. Yole Development has quantified the trends of bonding scenarios developed in the 3D integration context, as illustrated in Figure 1.19, ranking the direct bonding as the third major techniques adopted. Representative actors implementing each of these bonding categories are mentioned in Figure 1.15.

The main interests for using direct wafer bonding as wafer assembly technique in 3D integration are the following. This process is fully CMOS compatible, provided that the thermal budget is respected. By making use of surface activation methods, such as oxygen plasma, the surface energy may be enhanced at low or even at room temperature. Besides, the absence of intermediate layer of heterogeneous material brings about unique properties such as high temperature withstanding and limited stress generation at the bonded interface. Furthermore, high temperatures tend to strengthen the interface. These properties are well in scale with typical operating conditions of SOI technology: harsh environments.

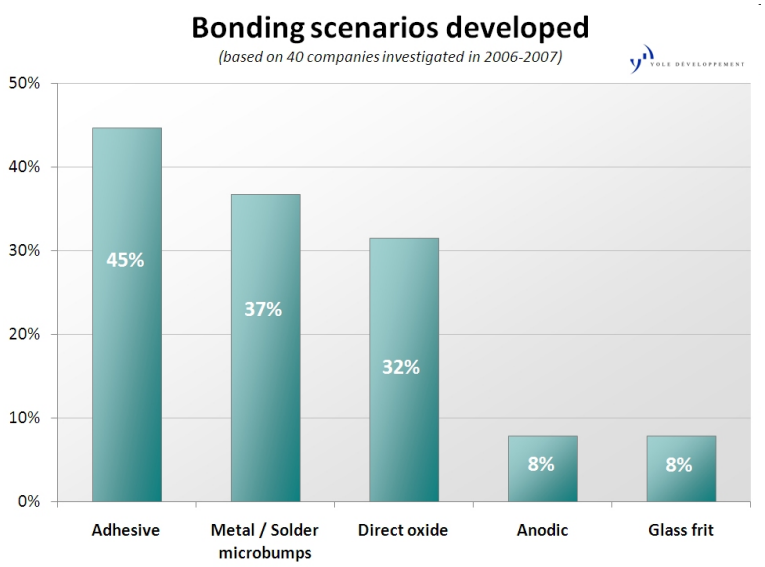


Figure 1.19: 3D integration scenarios developed, [49].

Nevertheless, in order to achieve good quality bonding with direct wafer bonding method, one must take great care about the roughness of the surfaces and their cleanliness. In particular, 3D integration relies on the bonding of deposited oxide films which, contrarily to thermal SiO_2, require a Chemo-Mechanical-Polishing (CMP) in order to reduce the surface roughness.

1.3.3 This Work - Wafer Bonding Research Axis

In the present thesis, we report on the resolution of four case-studies of Direct Wafer Bonding which are related either to a better understanding of the fundamental bonding mechanisms or to applicative contexts: 3D-IC integration and special substrates fabrication. Each case-study is directly related to a chapter and for all of them the motivations are expressed here below.

Case Study 1 - *In the literature, we can read that Si/SiO_2 bonding strength is higher than SiO_2/SiO_2* [161, 98, 151]. But in hydrophilic bonding, both surfaces are in Si/SiO_2 bonding configuration are virtually of SiO_2. Then the driving question developed in Chapter 6 is: "From which SiO_2 thickness is SiO_2/SiO_2 bonding configuration weaker than Si/SiO_2?" The following question is: "How could we optimize the bonding of thick SiO_2 films?" In this chapter, fundamental mechanisms of direct wafer bonding are investigated. It is observed that, when the interfacial SiO_2 thickness is increased, the resulting surface energy is drastically reduced for a given plasma surface activation and annealing conditions. The effect of O_2 plasma and warm HNO_3 surface activation techniques are investigated as well as the surfaces roughness.

CASE STUDY 2 - In the context of 3D-IC integration, we have read that *the wafer bow is a problem (i) for making accurate bonding alignment* [28, 149]*, (ii) for achieving the direct bonding itself* [107, 156]. Then in Chapter 7, the following question is addressed: "Is it possible to reduce the impact of a deposited PECVD oxide film on the wafer bow?" Furthermore, "Can we do that by tuning the recipe? Or by thermal treatments?" Wafer bonding experiments are conducted with Plasma-Enhanced Chemical-Vapour Deposited (PECVD) SiO_2. In that frame, a complete study on stress reduction is performed in order to be able to reduce the impact of the SiO_2 film on the resulting wafer bow. Deposition parameters are investigated as well as subsequent thermal treatments. A Chemo-Mechanical-Polishing (CMP) procedure is set up in order to obtain a suitable surface roughness allowing direct bonding to occur and check experimentally the assumptions of bow-prevented wafer bonding.

CASE STUDY 3 - Some 3D-IC integration developments imply the *coexistence of metal layers with direct bonding interfaces of PECVD oxide films* [40, 69]. In Chapter 8, the driving questions are then: "What are the outcomes of such neighboring?", "Would it be possible to enhance the bonded interface toughness by inserting a ductile layer near the interface?" Such ductile layer is expected to dissipate a part of the debonding energy by a plastic deformation. Multi-scale numerical simulations based on J2 flow theory are discussed and the concept with embedded dissipative layers is experimented.

CASE STUDY 4 - In Chapter 9, a special substrate preparation case is addressed by the proposal of *an original planar double-gate (DG) SOI CMOS process flow.* This process flow implies the transfer of a thin SOI film onto an oxidized wafer with pre-patterned cavities, by direct wafer bonding. And the questions become: "How could we optimize that transfer?", "What is the best surface activation configuration?", "What are the best annealing parameters?" The quality of the transfer is evaluated by optical observation globally and locally. The transferred areas are quantified at each step and the wafers are locally inspected. Fully processed DG SOI MOS devices are electrically characterized. This latter case is actually closely related to the concept of active pressure sensor thoroughly developed in Part II, as DG MOS is expected to constitute an architecture that will improve the electrical behavior of the suspended devices (see Chapter 4).

Part II

Pressure Sensing Systems

Chapter 2

Devices and Ring Oscillators on Very Thin Dielectric Membranes - A Proof of Concept

2.1 Introduction

In this chapter, we introduce the concept of "Novel Active Pressure Sensors in Thin Film SOI Technology" with first experimental demonstrations and characterization of MOS devices as well as complete ring oscillators suspended on thin dielectric membranes. Thermal aspects are also investigated.

2.2 An Augmented SOI CMOS Process Flow

The fabrication of suspended MOS devices on very thin dielectric membranes is based on a standard SOI CMOS process supplemented with two main steps. The first one is a front-end nitride layer deposition and its patterning for the membrane setting up, while the second one is a post-process TMAH back-etching for its release. This process flow was demonstrated by Dr. Jean Laconte in [100].

The complete fabrication process is illustrated in Figure 2.1. Following it step-by-step, the process starts with a (100) UNIBOND SOI wafer for which the top thin silicon film is 100 nm-thick and its buried oxide 400 nm-thick. The wafer is 25 nm oxidized to bring a protection to the Si film during the first steps of the process. A photolithography is performed and the active film is removed from the future membrane areas with a $SiCl_4$ based RIE etching (Figure 2.1(a)). It is worth to note that, in this step, the silicon film is preserved at the transistors areas even if these ones are on future membranes. Next, the active zones are defined by a patterned LPCVD nitride film which acts as a mask for locally wet thinning the top silicon film and for the LOCOS oxidation (Figure 2.1(b-c)). This mask is removed by wet etching. Following that, another LPCVD nitride layer is deposited and patterned, which constitutes the second layer of the membrane stack and covers all membrane areas except active devices locations. The etching of this latter film is performed by a combination of SF_6 and CHF_3 based plasmas. Although SF_6 provides an

interesting 2.5:1 selectivity between nitride and oxide as well as a end-of-attack detection, CHF_3 is adopted to terminate the nitride film etching for precaution reasons: in case of oxide over-etch the silicon film would be very rapidly etched with SF_6. From this point, wafers follow a standard SOI CMOS process with gate oxidation, channel implantation, polysilicon gate deposition and patterning, source and drain implantation, interconnect oxide deposition, metal layer evaporation and passivation oxide deposition (Figure 2.1(e-g)). Finally, at the back end of the process, the wafers are thinned by grinding from 725 μm down to 200 μm and the membranes are released by back-etching (Figure 2.1(g)). This release is performed in TMAH (Tetramethyl Ammonium Hydroxide) 10% solution at 90°C with addition of 35 g/l of dissolved silicon powder and 15 g/l of APS (Ammonium Persulfate), ensuring a nearly infinite selectivity to aluminum used as back mask.

The resulting membrane is constituted by, starting from the bottom: (1) the 400 nm buried oxide of the SOI substrate, (2) a 300 nm LPCVD silicon nitride layer, (3) the 300 nm densified PECVD oxide interconnection film, and finally (4) a 500 nm-thick APCVD oxide passivation layer. The lateral dimensions of the membranes are varied from 250 μm to 800 μm-side. The mechanical aspects of this membrane are the subject of Chapter 3.

2.3 Piezoresistivity theory applied to MOS Devices

While many research groups are reporting [35, 91, 123, 169] and taking benefit [64, 125, 155] of the enhancement of carriers mobility in strained-silicon inversion layers, the mechanisms involved in this phenomenon are not completely understood [58]. Nevertheless, the MOSFETs drain current variation can be related to the mechanical stress applied on the membrane by a simple phenomenological model. From the physics of semiconductor we have:

$$\rho = \frac{1}{q \cdot (\mu_n \cdot n + \mu_p \cdot p)} \tag{2.1}$$

where ρ is the silicon resistivity; q is the electronic charge; μ_n and μ_p are the mobility of electron and hole; n and p are electron and hole densities, respectively. Hence, the relative resistivity change of the devices channel is equal and opposite in sign to the carrier mobility variation, as expressed by:

$$\frac{\Delta\rho_{channel}}{\rho_{channel}} \cong -\frac{\Delta\mu}{\mu}. \tag{2.2}$$

According to the piezoresistivity theory, the relative variation of resistivity can be written, at the first order of approximation, as the stress tensor multiplied by the matrix of piezoresistive coefficients, which gives for in-plane stress:

$$\frac{\Delta\rho}{\rho} = \pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp} + \pi_s\sigma_s \tag{2.3}$$

where $\sigma_{\parallel}$ and $\sigma_{\perp}$ are the stress magnitude, respectively, parallel and perpendicular to the channel current; $\pi_{\parallel}$ and $\pi_{\perp}$ are the corresponding piezoresistive coefficients. s is the shear stress while the shear coefficient π_s is null in the [110] direction on a (100) wafer. Table 2 gives typical values of piezo-coefficients for a SOI technology. Besides, in linear and

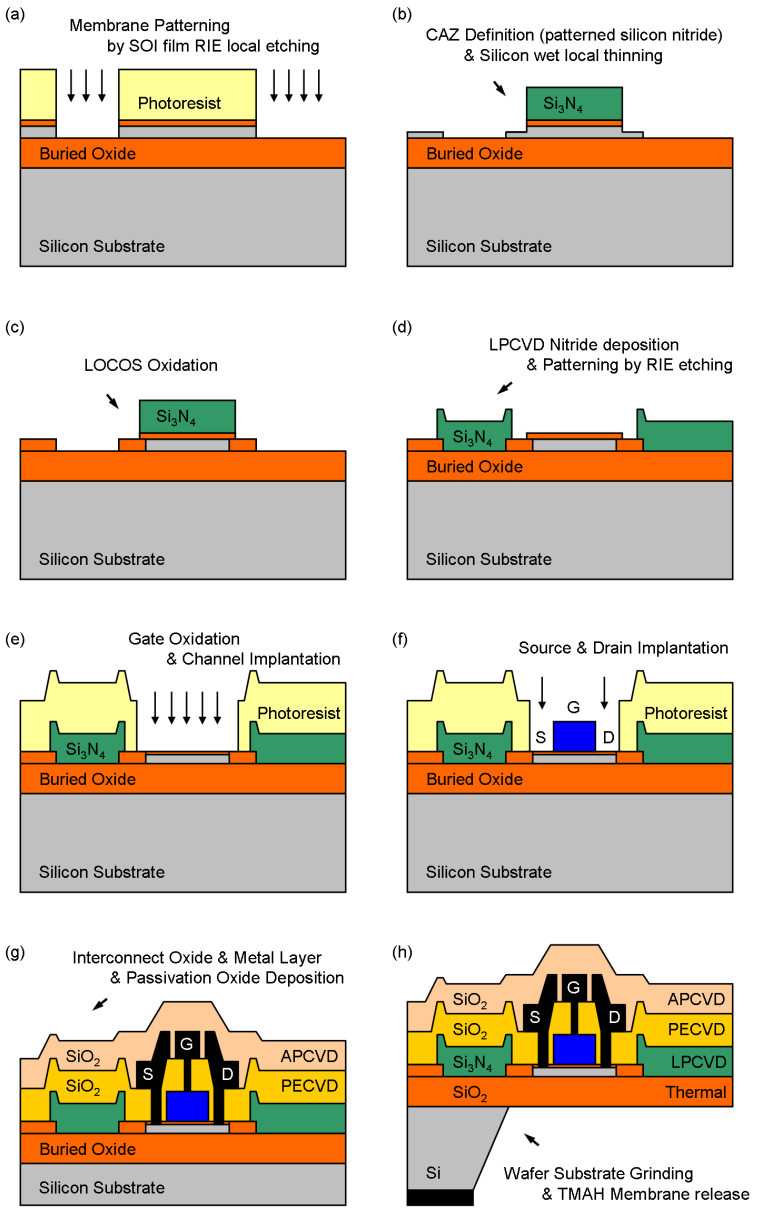


Figure 2.1: Schematic illustration of the process flow of the multilayered membrane with integrated MOS device: (a) SOI thin film locally removed from oxidized starting SOI wafer on future membrane areas, (b) LPCVD silicon nitride film deposition and patterning according to the active zones, Si local wet thinning (c) LOCOS oxidation, (d) membrane's nitride film deposition and RIE patterning, (e) gate oxidation and channel implantation, (f) source and drain implantation, (g) deposition of interconnect oxide, aluminum s-gun evaporation and passivation layer deposition, (h) wafer's substrate grinding, metal layer evaporation and patterning, TMAH membrane release; the final system configuration.

saturation regimes the drain current is proportional to the carrier mobility. Hence, their relative variation is equivalent:

$$\frac{\Delta I_D}{I_{D_0}} = \frac{\Delta \mu}{\mu} \tag{2.4}$$

From Equations (2.2), (2.3) and (2.4), we have finally:

$$-\frac{\Delta I_D}{I_{D_0}} \cong \frac{\Delta \rho_{channel}}{\rho_{channel}} = \pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp} \tag{2.5}$$

The piezoresistive coefficients measured on devices issued from the technology under study are given in Table 2.1.

Source	Technology	$\pi_{NMOS,\parallel}$	$\pi_{NMOS,\perp}$	$\pi_{PMOS,\parallel}$	$\pi_{PMOS,\perp}$
UCL	*SOI MOS*	*-1.97*	*-1.23*	*+2.58*	*-2.43*

Table 2.1: Piezoresistive coefficients measured for the available technology; for further details see Chapter 5.

2.4 Active suspended MOS Devices

Although mechanical stress considerations are specifically addressed in Chapter 3, one knows from the classical solid-state pressure sensors implementations with resistive Wheatstone bridges that the highest strained areas are located at the middle points of membranes borders. It is also at these points that the strain components are the most directional with the perpendicular strain component relatively to the membrane's border being dominating. Therefore, looking for evaluating the impact of a longitudinal or transversal stress on the drain current of MOS devices, transistors are placed at the border of membranes, in both parallel and perpendicular orientations relatively to the edges (Figure 2.2).

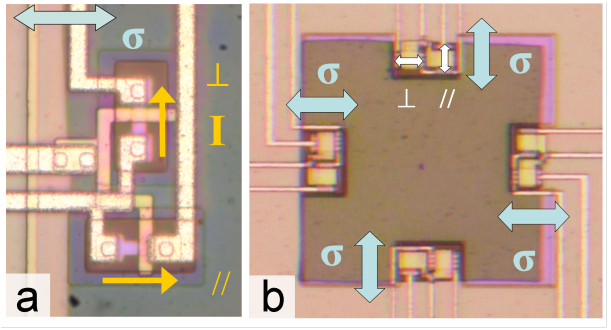


Figure 2.2: Description of the measured structures and their devices configuration: (a) local view of 3 x 3 μm^2 MOSFETs, the stress is mainly uniaxial, perpendicular to the drain current, (up device) or parallel to it (bottom device), (b) layout of a 250 μm side membrane with 20 x 20 μm^2 devices located at its edges (anchors).

2.4.1 Measurement setup

Active suspended structures are characterized when applying a mechanical force at the center of each membrane. A smoothly profiled microprobe is carefully directed to apply this constraint (Figure 2.3). Although we could not measure the value of the applied force in the present setup, electrical results give a demonstrator and an estimation of the piezoresistive effects magnitude involved in these systems.

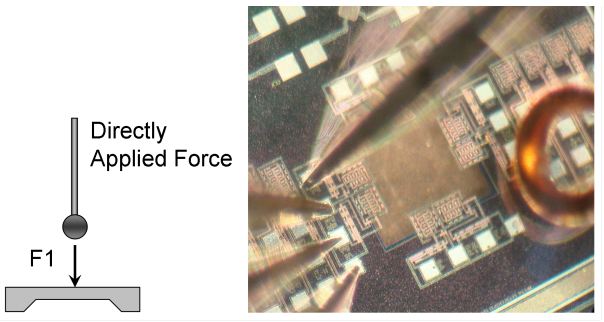
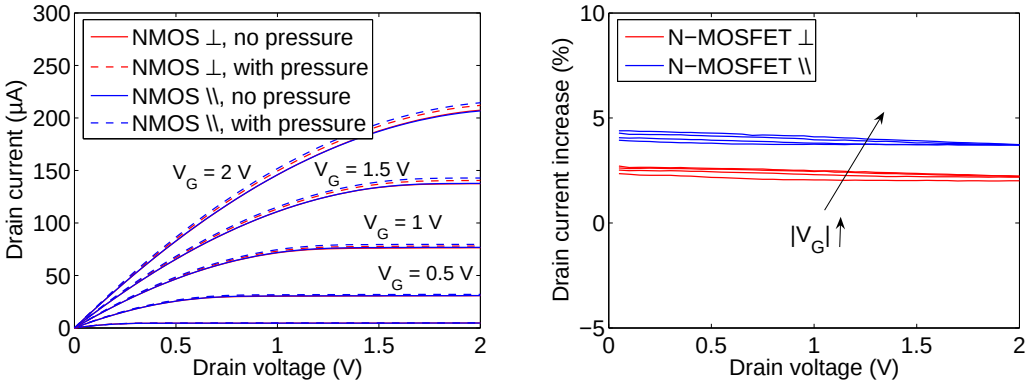


Figure 2.3: Description of the setup used for characterizing the devices and circuits on membranes when applying a force at the center of the membranes; probe needles are disposed on contact plots of a VCOs' pair; the transparent membrane is 800 μm-side the smoothly profiled microprobe is visible on the right side of the photograph.

2.4.2 Devices characterization under static force

Figures 2.4 and 2.5 show I_D-V_D characteristics with and without applied force on the membrane, respectively, for a N-MOSFET and a P-MOSFET with identical dimensions: $Lp = Ln = 20$ μm (channel length), $Wp = Wn = 20$ μm (channel width). It is worth to note that, in both cases, the drain current change is very steady with respect to the drain voltage. Moreover, this variation is also only barely sensitive to the gate voltage. These measurements are in good agreement with piezoresistive coefficients values given in Table 2.1. The sign of sensitivities and their order of magnitude are respected for both devices types and orientations. Based on the value of these piezoresistive coefficients and the fact that the drain current of a parallel N-MOSFET increases by 4% when the force is applied on the membrane and provided that at the border of the membrane $\sigma_{yy} = \nu_{Si} \cdot \sigma_{xx}$, we estimate from Equation (2.5) that this force induces a local stress of around 170 MPa perpendicular to the membrane border and 50 MPa parallel. For resolution details, please see Appendix A. Besides, when the gate voltage is close or lower than the threshold voltage, the steady character of the drain current change is lost and the piezoresistive coefficients are not valid in this regime of operation. Figure 2.6 illustrate the relative drain variation as a function of the gate voltage for the two same n- and p-type devices. These curves are reported in linear as well as in saturation regime for device channels placed in perpendicular and in parallel orientation with respect to the stress direction. In order to have a comparison with the I_D-V_G characteristics of the device, a typical drain current is given on the left-axis.

The drastic increase of I_D variation when approaching the threshold voltage (V_{Th}) could be due to a slight shift of this threshold. The threshold voltage has been extracted with and without applied force on the membrane (Tables 2.2 and 2.3). V_{Th} was evaluated at the inflexion point of the transconductance which is at the maximum of d^2I_D/dV_G^2. No variation has been observed in our experiments. Nevertheless, according to C. Gallon et al. in [62], the change of threshold voltage is negligible with a theoretical variation less than 3 mV for 130 MPa applied stress.

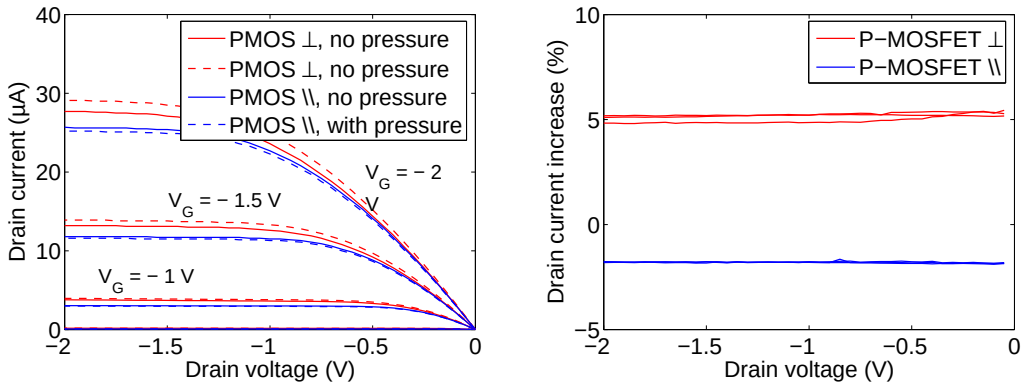


(a) (b)

Figure 2.4: Output characteristics of perpendicularly oriented (red lines) and parallel (blue lines) intrinsic N-MOSFETs at various gate biases: (a) I_D-V_D curves with (dashed lines) and without (solid lines) applied stress on the membrane, (b) the corresponding I_D increase as a function of the drain voltage. $L = W = 20$ μm.

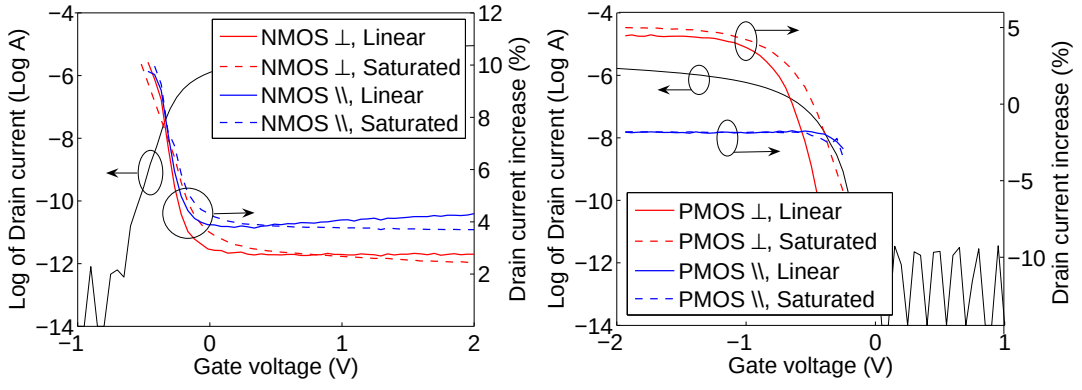
Extracted Threshold Voltage (V_T), ± 25 mV		
Applied Stress	Without	With
Perpendicular	-0.3	-0.3
Parallel	-0.3	-0.3
Idrain increase (%) when $V_G = V_T + 1$ V		
Regime	Linear ($V_D = 50$ mV)	Saturated ($V_D = 2$ V)
Perpendicular	+2.69	+2.60
Parallel	+4.07	+3.70

Table 2.2: Extracted threshold voltage with and without applied stress and drain current increase under stress of an n-type MOSFET on membrane; the device dimensions are $L = 20$ μm, $W = 20$ μm.



(a) (b)

Figure 2.5: Output characteristics of perpendicularly oriented (red lines) and parallel (blue lines) P-MOSFETs at various gate biases: (a) I_D-V_D curves with (dashed lines) and without (solid lines) applied stress on the membrane, (b) the corresponding I_D increase as a function of the drain voltage. $L = W = 20$ μm.



(a) (b)

Figure 2.6: Transfer characteristics of a (a) N-MOSFET and (b) P-MOSFET; Right axis - I_D increase of perpendicularly oriented (red lines) and parallel (blue lines) transistor channel as a function of the gate voltage, in linear ($V_D = \pm$ 50 mV, dashed lines) and saturation ($V_D = \pm$ 2 V, solid lines) regimes when a mechanical stress is applied on the membrane. $L = W = 20$ μm. Left axis - The corresponding I_D-V_G characteristics of perpendicularly oriented device in linear regime.

Extracted Threshold Voltage (V_T), ± 25 mV		
Applied Stress	Without	With
Perpendicular	-0.5	-0.5
Parallel	-0.5	-0.5
Idrain increase (%) when $V_G = V_T$ - 1 V		
Regime	Linear (V_D = -50 mV)	Saturated (V_D = -2 V)
Perpendicular	+4.44	+4.880
Parallel	-1.85	-1.84

Table 2.3: Extracted threshold voltage with and without applied stress and drain current increase under stress of a p-type MOSFET on membrane; the device dimensions are L = 20 μm, W = 20 μm.

2.4.3 Devices response under a Dynamic Pressure

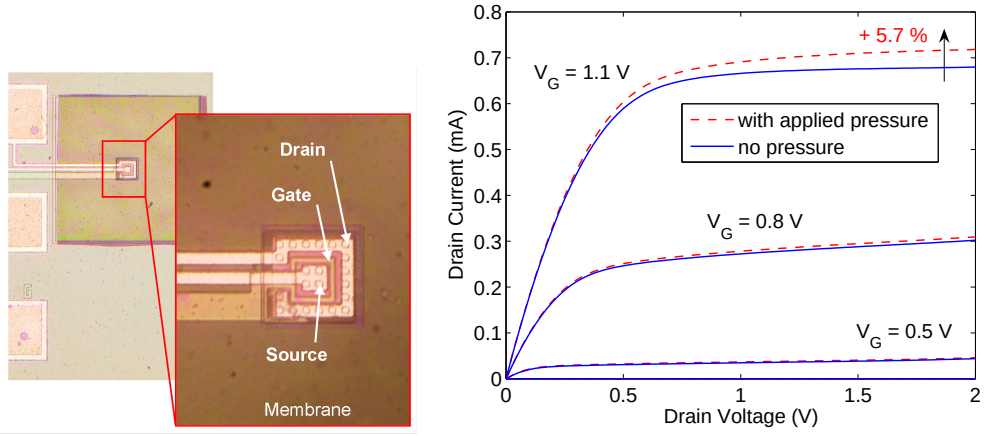
The dynamic pressure applied by a fan, a turbine or a propeller can be measured with a simple MOS device integrated on a thin membrane, allowing rotational speed measurements. Indeed, each passage of a rotating blade near the suspended device involves a pressure peak inducing short drain current variation.

This was experimented with a sensitive edgeless transistor located at the center of a 250 μm side membrane. The static characteristics of the device are given in Figure 2.7, with a physical description of the system. When a static pressure is applied, I_D increases by 5.7%. For dynamic measurements, the devices are mounted in series with a resistor and placed on the edge of a bladed rotor, which can speed up to 135 rpm. The full set-up is graphically described in Figure 2.8. The spectral response of the system is given in Figure 2.9 at various blade rotation frequencies, from 830 to 1215 Hz. It is worth to note that the output signal is clear and accurate with respect to the rotor speed on all this range of speeds, revealing a real opportunity of application of this kind of active element sensors. Some low amplitude noisy peaks are distinguishable on the graph, which can be attributed the basic character of the packaging technology in use in these first experiments.

2.5 Complete suspended Voltage Controlled Oscillators

From the technology available, a smart pressure sensor can be obtained by integrating CMOS ring oscillators on a membrane. This configuration gives a direct digital output, avoiding external analog circuitry and, thus, is less sensitive to noise compared to the conventional Wheatstone bridge. A pressure change on the membrane induces a variation of the oscillator frequency. This variation is related to the delay variation of each inverter due to the piezoresistive effect induced by the stress in the channel resistivity of the MOSFETs:

$$-\frac{\Delta F}{F_0} \approx \frac{\Delta \tau_{inverter}}{\tau_{inverter}} \approx \frac{1}{2}\left(\left(\frac{\Delta R}{R_0}\right)_{NMOS} + \left(\frac{\Delta R}{R_0}\right)_{PMOS}\right) \tag{2.6}$$



(a) (b)

Figure 2.7: Edgeless 72 x 2 μm^2 N-MOSFET: (a) layout of the device on a square 250 μm-side membrane and (b) I_D-V_D curve showing the influence of a pressure applied on the membrane.

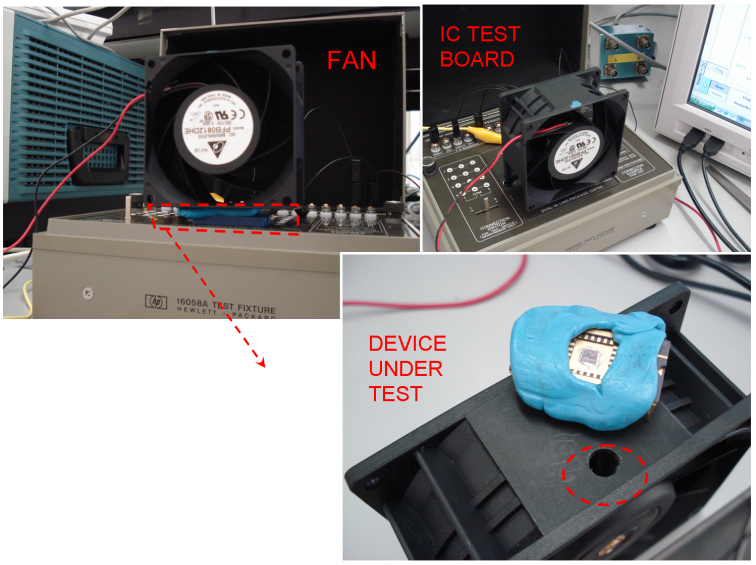
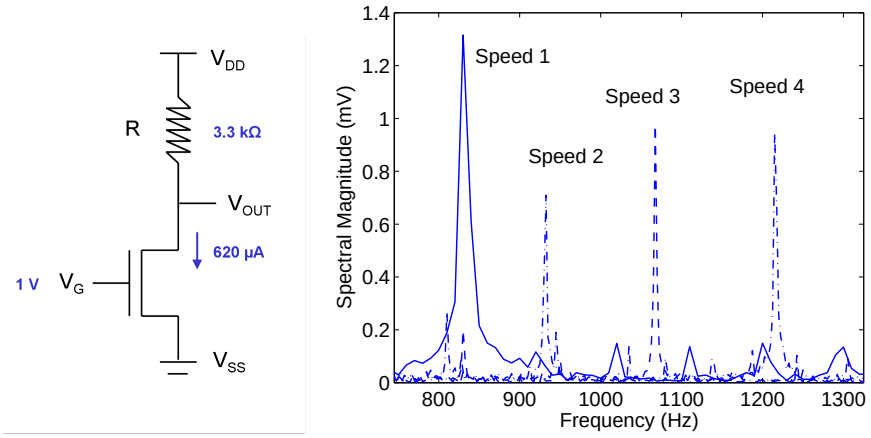


Figure 2.8: Composite view of the dynamic pressure measurement set-up; the dynamic pressure is applied to the MOS device through a hole on the edge of a fan; the device is packaged in a dual-in-line (DIL) package which is placed on an IC test board.



(a) (b)

Figure 2.9: Dynamic pressure measurement: (a) inverter device mounting and bias conditions, (b) spectral dynamic response of a 72 x 2 μm^2 N-MOS edgeless transistor excited at various rotor blade speeds: 830, 921, 1067 and 1215 Hz, respectively.

Referring to Table 2.1, designing inverters with N-MOSFET and P-MOSFET channels, respectively, parallel and perpendicular to the strain will increase the VCO output frequency. Choosing the opposite configuration (N-MOSFET $\parallel$ and P-MOSFET $\perp$) should lead to a decrease of this frequency. Figure 2.10 illustrates the implementation of such suspended oscillators pair architecture.

By considering the frequency ratio of these two oscillators, the pressure sensitivity of the system is then amplified. Besides, ring oscillators are very sensitive to temperature because of the dependence of the carrier mobility, the threshold voltage (first order effects) and the piezoresistive coefficients (second order effect). Hence more importantly, the consideration of the frequency ratio of the oscillators pair is expected also to suppress first order effects due to temperature as well as eventual supply voltage variations. Section 2.6 investigates the temperature self-compensation capability of such architecture. Each ring oscillator is made of seven CMOS inverters. Channel dimensions are $Lp = Ln = 12$ μm, $Wp = Wn = 24$ μm and the ring oscillator is 150 μm x 150 μm in size. The VCO's are located at the border of the membrane where the stress is the highest. When $V_{DD} = 2$ V, the oscillators frequencies are respectively 5.55 and 4.96 MHz for the configurations with N-MOSFET$_\perp$ and N-MOSFET$_\parallel$. Measurements under pressure are presented in Figure 2.11. As predicted, we have a positive and negative shift of the VCOs' oscillation frequencies according to their orientation. The positive shift is more important due to the higher piezoresistive coefficients sum for this configuration. Eventually, the difference of resonance frequency without applied pressure can be attributed to the internal residual stress of the membrane.

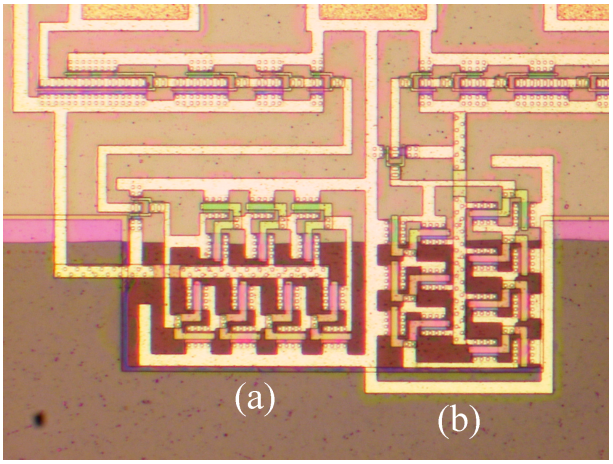


Figure 2.10: Microphotograph of an oscillator pair at the border of a membrane. (a) left oscillator, the N-MOS devices are parallel to the stress and P-MOS are perpendicular, denoted shortly oscillator ∥, (b) right oscillator, the devices are inversely oriented, denoted shortly oscillator ⊥.

2.6 Temperature Self-Compensation Performances

Oscillators do present a Zero Temperature Coefficient voltage (V_{ZTC}), as illustrated in Figure 2.12 for on- and off-membrane oscillators. At such an operating point, the output frequency is insensitive to the temperature. It originates from the mutual compensation of the threshold voltage and the carriers mobility dependencies with temperature [31], which modify the channel resistivity and hence the output frequency.

From Figure 2.12, oscillation frequencies differ whether the circuit is implemented on or off a membrane: this frequency is 13% higher for the oscillator ⊥ (i.e. with the N-MOSFETs ⊥, as indicated in Figure 2.10) than one out off membrane, at room temperature and 2 V supply voltage. This variation is mainly attributed to the substrate contribution to the parasitic capacitances. Besides, the residual membrane stress is assumed being responsible of a 12% frequency difference between oscillator ∥ and oscillator ⊥, under the same conditions (Figure 2.13).

From Figure 2.13, operating a couple of oscillators at one V_{ZTC} does not provide a temperature independent output because of a slight V_{ZTC} mismatch. As suggested in Section 2.5, by considering the output frequency dependency with the membrane stress and the temperature, we have for both orientations oscillators:

$$F_{\parallel} \approx F_0 \left(1 + \pi_{\parallel}\sigma\right)\left(1 + \alpha T\right), \tag{2.7}$$

$$F_{\perp} \approx F_0 \left(1 + \pi_{\perp}\sigma\right)\left(1 + \alpha T\right), \tag{2.8}$$

where $\pi_{\parallel}$ and $\pi_{\perp}$ are the piezoresistive coefficients, σ is the stress, α is the temperature coefficient and T is the temperature. Neglecting the second order terms, the frequency ratio between both oscillators can be expressed as:

$$F_{\parallel}/F_{\perp} \approx 1 + \left(\pi_{\parallel} - \pi_{\perp}\right)\sigma \tag{2.9}$$

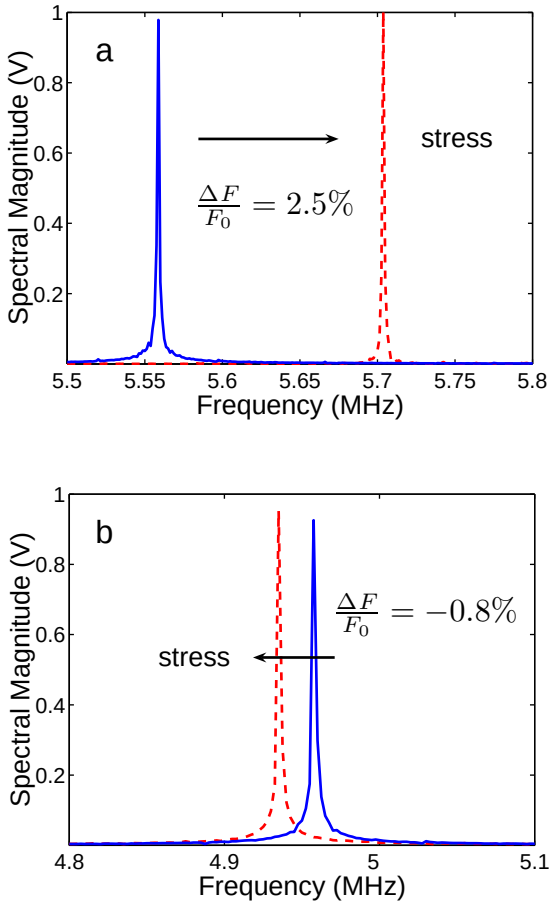
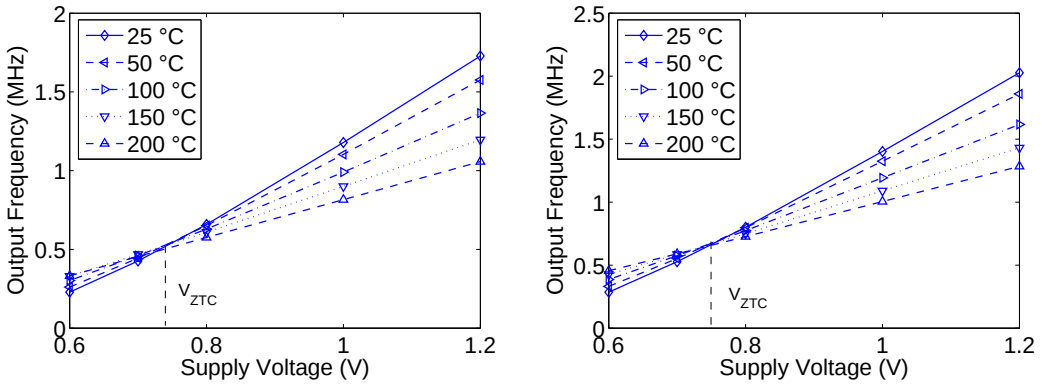


Figure 2.11: VCOs resonance frequency shift according to their orientation when a force is applied at the center of the membrane: (a) the channel of N-MOS devices are parallel to the stress while the P-MOS are perpendicular, (b) the channel of N-MOS devices are perpendicular to the stress while the P-MOS are parallel.

a temperature independent expression. In practice, this statement was verified only at higher supply voltages (i.e. 2 V). In this latter case a steady output frequency ratio of 1.13 is observed with only 1.4% variation between 25°C and 200°C. Stress sensitivity experiments were conducted at room and high temperature as a function of the supply voltage ($V_{DD} - V_{SS}$) and lead to, respectively, an increase of the output frequency of 5% and 8% for oscillator $\parallel$ (-1% and +1% for oscillator $\perp$). The output frequency increase is weakly dependent on the supply voltage at room temperature while it increases with the voltage at 200°C.

The supply voltage plays then a determinant role in terms of sensitivity to the temperature. Nevertheless, the use of oscillator frequencies ratio provides a stable sensor output for sufficient supply voltages (from 2 V). Finally, these first cross-sensitivities experiments let us figure out the applicability of this system in high temperature environments (Figure 2.14). Hence, a possible self-heating due to the high thermal insulation character of the membranes does not appear being detrimental to the sensitivity of the sensor.



(a) Off-membrane RO

(b) On-membrane RO

Figure 2.12: Output frequency for off- and on-membrane ring oscillators (RO's) as a function of the supply voltage ($V_{DD} - V_{SS}$) for various temperature values.

2.7 Conclusions

Preliminary experimental results presented in this chapter demonstrate the real interest of implementing SOI MOS devices as well as complete circuits on suspended thin dielectric membranes. Indeed, such systems are easily fabricated and provide a highly flexible sensing platform. The piezoresistive effect was shown to have an order of magnitude of few percents for devices as well as for circuits implemented on thin membranes. The opportunity for making dynamic pressure sensors was identified. Besides, the interest of considering the output frequency ratio of inversely pressure-sensitive oscillators was demonstrated as an effective mean for reducing the temperature dependence on the output signal, provided that the supply voltage is sufficient (typically 2 V or above). Finally, measurements at 200°C, have evidenced the fact that sensitivities are, at high temperature, in the same

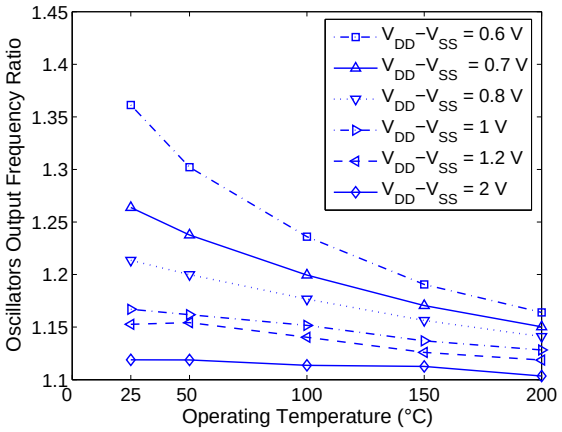


Figure 2.13: Output frequency ratio of two on-membrane ring oscillators (one $\parallel$ and one $\perp$) as a function of the temperature for various supply voltages.

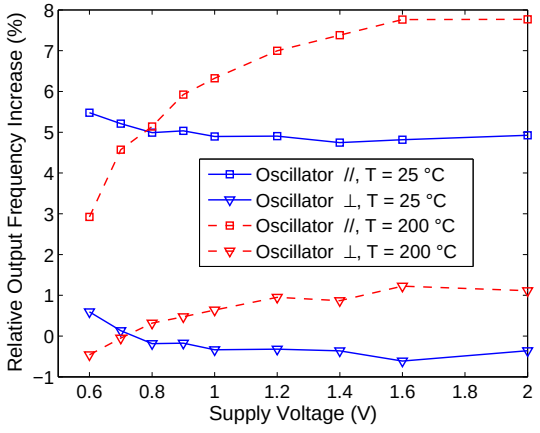


Figure 2.14: Output frequency sensitivity of two on-membrane ring oscillators (differing in their orientation), as a function of the supply voltage at 25°C and 200°C. The stress applied at both temperatures is not supposed being the same.

order of magnitude as room temperature sensitivities. However it is not known, from the measurements, how much these sensitivities are affected by a piezoresistive coefficients shift with the temperature.

Chapter 3

Mechanical Characterization of Thin Dielectric Membranes - A Study on Patterning Effect

3.1 Introduction

The main motivation of the present chapter originates from the first characterization under calibrated pressure of complete ring oscillators integrated on large and thin membranes (i.e. 800 μm-side and 1.5 μm thick). Indeed, these measurements have shown early fracture of the membranes, much earlier than observed with similar size blanket membranes. In fact, the maximal admissible pressure before burst is almost divided by a 10 factor, dropping from a value superior to 5 bars down to a value comprised between 0.5 and 1 bar, whether the membrane is functionalized with Voltage Controlled Oscillators (VCOs) or not. To the best of our knowledge, mechanical considerations of such thin and patterned multilayered membranes are not reported yet in the literature. Therefore, it was necessary to address the question. In particular, in this chapter, finite element modeling (FEM) is conducted in order to understand the reasons of the early fracture observed and find appropriate solutions. These simulations are complemented by mechanical measurements to further complete the study.

In addition, beyond membranes robustness considerations, one can wonder how the strain is distributed in these membranes, talking into account internal stresses of the various materials constituting them. Where are defined the tensile or compressive areas? How is the strain gradient? These are essential issues in order to determine the most appropriate areas where locating the pressure transducers. This is the second main purpose of the chapter.

3.2 Problem Description

This section objectively sets forth the problem as a basis for the next developments.

3.2.1 Membrane Structure

The membrane structure with an integrated device at its border is described in Figure 3.1. Its stack is formed by four thin films which are respectively from the bottom to the top: (1) the 400 nm buried oxide of the SOI substrate, (2) a 300 nm LPCVD silicon nitride layer, (3) a 300 nm interconnection PECVD oxide film, and (4) a 500 nm-thick APCVD oxide layer for the passivation of the electronics. All these films are opportunely directly involved with the standard SOI process, with the exception of the nitride layer. Indeed, the silicon nitride film is an additional layer contributing to a globally resulting tensile stress in the films stack.

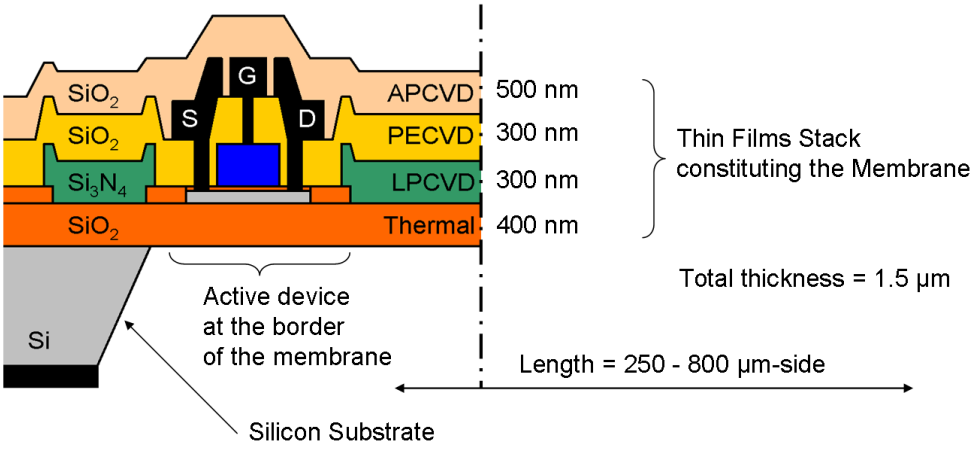


Figure 3.1: Physical description of the complete structure under study.

3.2.2 Deflections Measurements

Membranes are mechanically characterized under pressure by use of a Pressure Module mounted on a PM6 prober, both from Süss MicroTec. Compressed nitrogen passes through the Pressure Module at a controlled flow in order to yield a calibrated pressure at the surface of the membrane. The prober is equipped with a Polytec MSA-500 configured in white-light interferometer. A dedicated lens comprising a Michelson interferometer allows for measuring membranes topographies through an optical window in the Pressure Module (Figure 3.2).

Figure 3.3 clearly sets-up how functionalized membranes with VCOs have very different mechanical resistance than equivalent size blanket membranes. Indeed, a 850 μm-wide membrane bursts at around 600 mbar while for a 780 μm-wide membrane with no pattern the burst exceeds 5 bars. There is thus almost one order of pressure magnitude separating both membranes types.

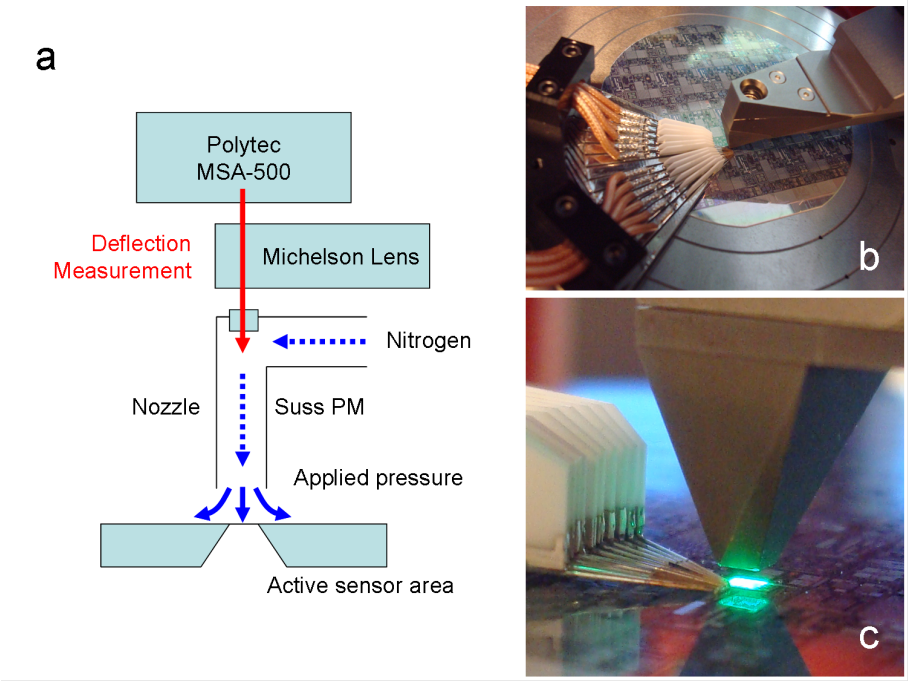
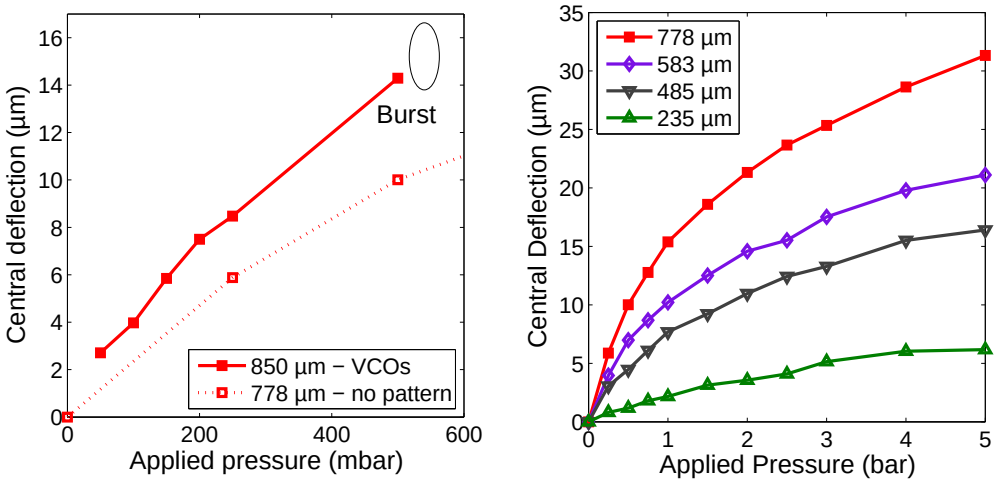


Figure 3.2: General description of the electro-mechanical characterization set-up: (a) sketch of the pressure application system, (b) general view of pressure nozzle, including a transparent window for in-situ deflection measurements, with additional card probes on the wafer, (c) area under study close-up.



(a) (b)

Figure 3.3: Membranes deflection measurements as a function of the applied pressure: (a) deflection curve of 850 μm-wide membrane functionalized with VCOs, (b) deflection curves of blanket membranes.

3.2.3 Topography of Complete VCOs on Membrane

Furthermore, topography images, issued from white-light interferometer, do evidence a waviness shape in the area of the large oscillators implemented on the membrane. The amplitude of the wave is tiny with 2.5 μm for a 400 μm-length scan but, nevertheless, translating a residual compressive stress (Figure 3.4).

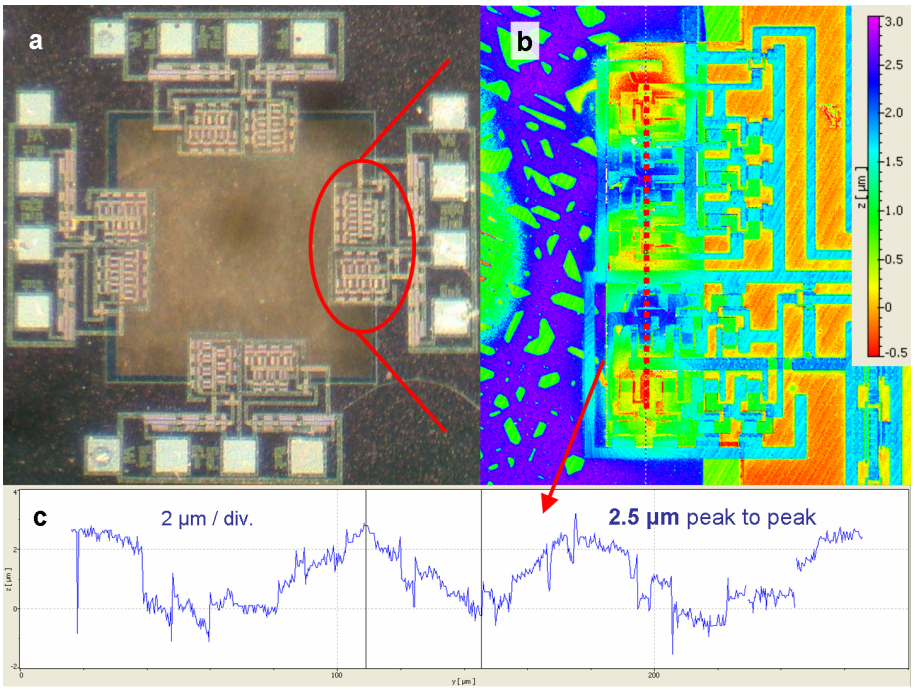


Figure 3.4: Composite view showing: (a) a 800 μm-side membrane with complete ring oscillators integrated at its borders, (b) a topographical close-up on one pair of oscillators, (c) the profile extracted along the axis crossing the oscillators pair; on the left side of (b) remaining silicon fragments on the membrane back-side are visible.

3.3 Finite Element Modeling

The first mean deployed to study the exposed problem is numerical simulations by finite elements analysis.

3.3.1 Framework

COMSOL simulations are performed with tri-dimensional modeling with Lagrange-Quadratic element type. Due to the membranes deflection amplitude, regarding to their thickness, the large deformation option was enabled. Besides, the symmetry of the studied problem is also considered by implementing quarters of membranes models, reducing computation complexity and thus time. The complete information about the simulator settings is reported in Appendix D.

3.3.1.1 Material Physical Constants

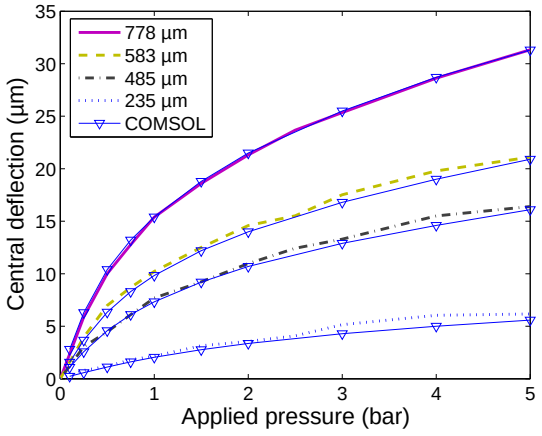
Numerical simulations and material properties extraction were performed on the same period of time. Therefore, the constants values adopted in COMSOL models are partly issued from earlier measurements in our laboratory and from literature (Table 3.1). They were slightly adjusted in order to fit the first mechanical measurements of membranes (Figure 3.5(a)). By the way, the influence of films residual stresses and their Young's Modulus (E) is highlighted in Figure 3.5(b). In this figure, it is shown that the thermal stresses act mainly upon the deflection at the lowest pressure values (i.e. below 1 bar). In particular, they define the elbow position in the curve, while the Young's Modulus characterize the slope of the deflection curve at the highest pressure values (i.e. beyond 2 bars). In order to compare, on a limited number of degrees of freedom, the results obtained from both parameters sets, a single film nitride is released. Figure 3.6 exposes the deflection measurements of such membrane and computed data. The error brought about by both parameters sets is less than 10%. Besides, considering the uncertainty on the physical characteristics of the measured membrane (Table 3.2), let us draw a tolerance corridor in Figure 3.6, which embraces the measured deflection curve. Globally, simulations performed with precise and process extracted values lead to under-estimated deflection of the membrane. It is envisioned that the reduced model considering perfect and complete clamping of the membranes edges partly explains this difference. In their reports on boundary effects in micromachined beams, de Boer [16, 84] and Senturia [96] invite to consider the clamping as not perfect to gain accuracy.

Material	Stress (MPa)	Young Mod. (GPa)	Poisson Coefficient
SiO_2 Thermal	-313∗, *-225*	70∗∗, *50*	0.17∗∗
Si_3N_4 LPCVD	1050∗, *770*	225∗, *210*	0.23∗∗
SiO_2 PECVD densified	-70∗, *-172*	72∗, *17*	0.25∗∗∗
SiO_2 APCVD annealed	130∗, *0*	67∗, *45*	0.17∗∗∗

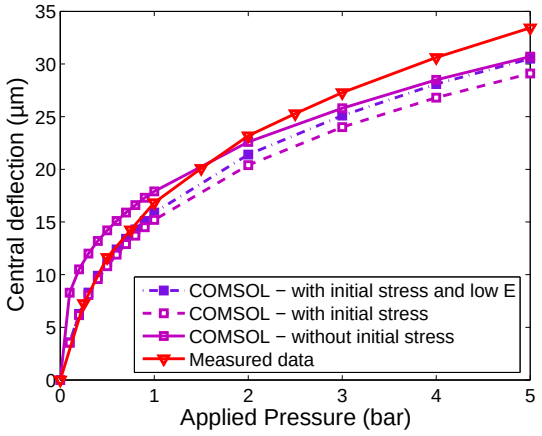
Table 3.1: Material constants ∗extracted from UCL process data, ∗∗from MEMSNET material database, ∗∗∗from MIT material database, in *italic*, adjusted values according to simulation results.

Physical parameters and their tolerence:
Membrane side length = 645 ± 5 μm
Film thickness = 285 ± 10 nm
E = 225 ± 26 GPa
σ = 1050 MPa ± 50 MPa

Table 3.2: List of measured physical characteristics of a Si_3N_4 monolayer membrane and their uncertainty.



(a)



(b)

Figure 3.5: Deflection curves as a function of applied pressure for OONO membranes, (a) measured data and simulation results with adjusted material constants are compared, (b) the influence of films residual stresses and thier Young's Modulus (E) is evidenced.

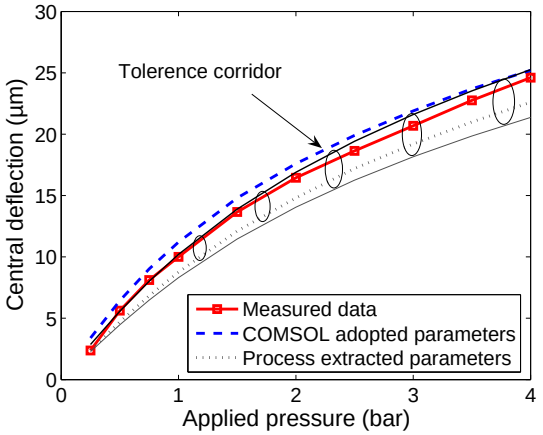


Figure 3.6: Deflection curves of 645 μm wide Si_3N_4 monolayer membrane, comparing measured data with COMSOL simulation results.

3.3.1.2 Implementation

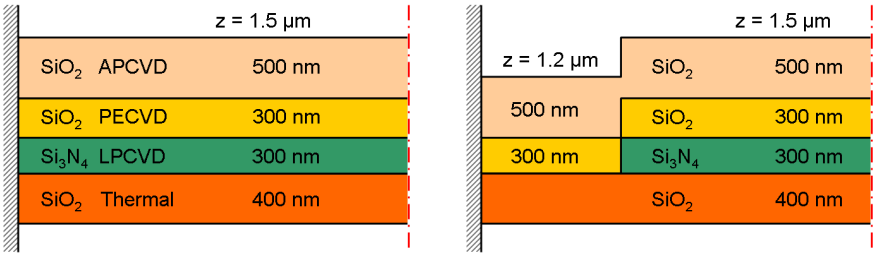
800 μm-wide membranes are simulated in three different configurations: (a) blanket, (b) globally patterned and (c) locally patterned. The global patterning case corresponds to the VCOs implementation situation, while the local patterning case draws a hypothetical configuration of six devices disposed directly near the border, each measuring 20 μm parallel to the border and 10 μm perpendicularly. Figure 3.7 illustrates the thin films stack of the simulated models. Patterned areas are areas where the nitride film was etched away during the process. These regions, where only a silicon oxide films stack remains, have a compressive resulting stress. Therefore, the simulation attempts

Therefore, simulations have the limitation that no residual stress was considered in oxide films of the patterned areas.

Membranes edges are considered as perfectly clamped. The position of the simulated quarter of membrane and the corresponding coordinates are given in Figure 3.8. The meshes are manually implemented, refining them particularly around discontinuities, notably at the borders and the patterned areas, as shown in Figure 3.9. The locally patterned configuration is implemented under two different meshes for an identical geometry.

3.3.2 Volume Analysis

With this first approach, it is intended to be systematic in order to locate the highest strained areas. This method is a kind of brute-force extraction and consists in considering the points population belonging to a set of 13 horizontal planes which are indicated in Figure 3.10(a). This set of planes is considered to be a good representative of the membranes volume. This population is composed of over 3×10^5 points (161 points/side/plane) which are interpolated from the model mesh. From this population, the 99-percentile is extracted as described in Figure 3.10(b). These points correspond to the 1% of the most strained population. The 99-percentile are plotted in Figures 3.11 and 3.12, respectively for the Y-axis strain (ε_{YY}) and X-axis strain (ε_{XX}). It very clearly highlights the most



(a) No patterning (b) Global patterning

Figure 3.7: Membrane's models description, perfect clamping, symmetry axis and thin films stacks.

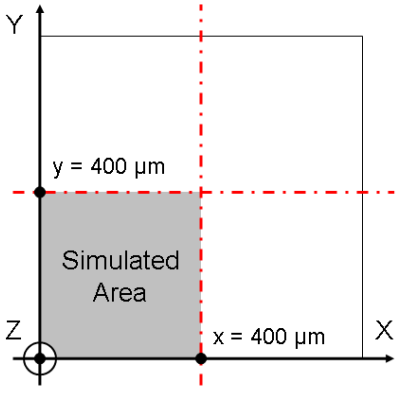
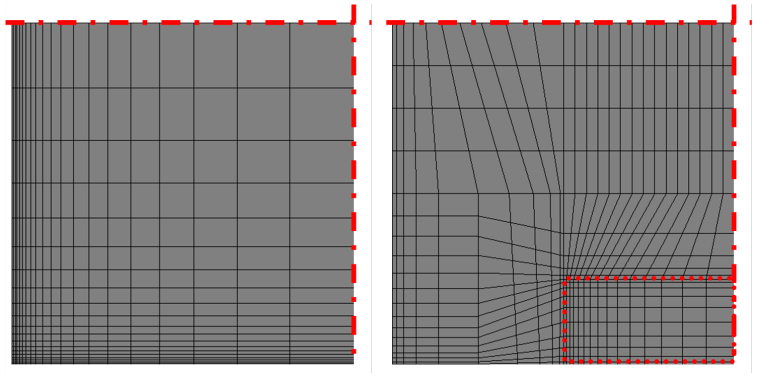
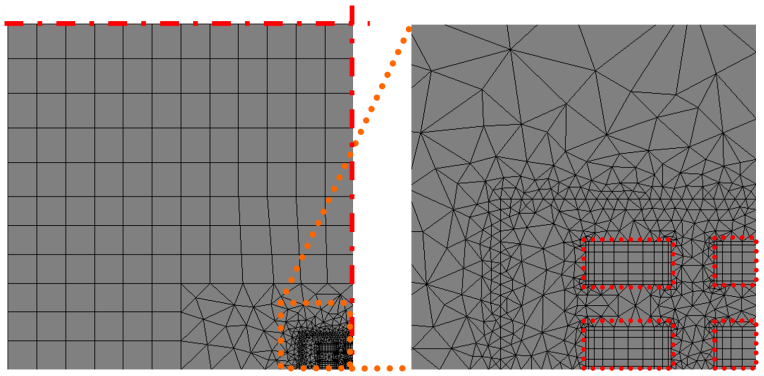


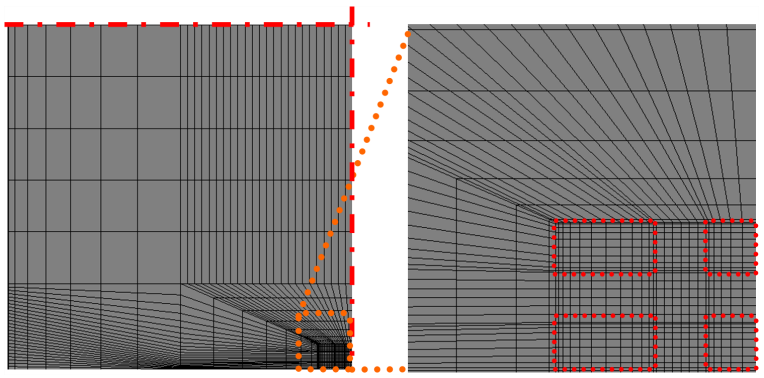
Figure 3.8: Simulated quart of membrane and coordinates.



(a) No patterning (b) Global patterning



(c) Local patterning, mesh1



(d) Local patterning, mesh2

Figure 3.9: Meshes' top view of the four configurations simulated in COMSOL; patterned areas are surrounded.

strained regions in the different configurations. For the blanket membrane case, it essentially concerns the top fibers of the anchored face. For the globally patterned case, the most strained region is similar but more centered on the patterned area along X-axis (for ε_{YY}). For the local patterning case, the patterned zones are identified as highly strained zones.

Besides, it is clear that this approach is not suitable in order to get a strain quantification. Indeed, the strain thresholds, noted $\varepsilon_{1\%}$ and being the base value defining the 1% most strained population, are not mesh insensitive. Focusing on the highest level strain component ε_{YY} (Figure 3.11), they consitute rather an index of dangerosity than a reliable information on the strain applied locally.

In the following section, local pattern case results are only given for mesh2, preserving clarity in the figures. Both meshes give very similar results.

3.3.3 Medial Axis Analysis

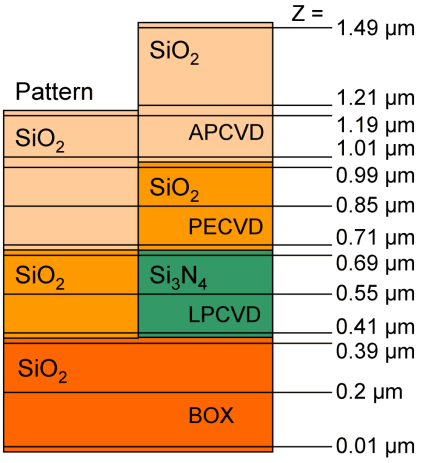
According to volume analysis results, the highest strained points are identified being near the edges. They are also centered on the medial point of these edges. Therefore, the following analysis explores particularly a median plane of the membranes, i.e. in this case X = 400 μm in Figure 3.8.

For blanket membranes, one distinguishes two regions (Figure 3.13(a)). The first one is characterized by a high strain gradient along Y-axis as well as Z-axis. It has a clamped beam behavior with flexure effort. The second region is almost a strain plateau with pure tensile effort and low strain vertical gradient (Figure 3.13(b)). The separation of these two regions is marked by a strain curve order inversion with respect to the Z-level. In the illustrated case (Figure 3.13(a)), it occurs at 28 μm, but generally it varies according to the applied pressure (from 35 to 19 μm, when the pressure ranges from 0.1 to 5 bars).

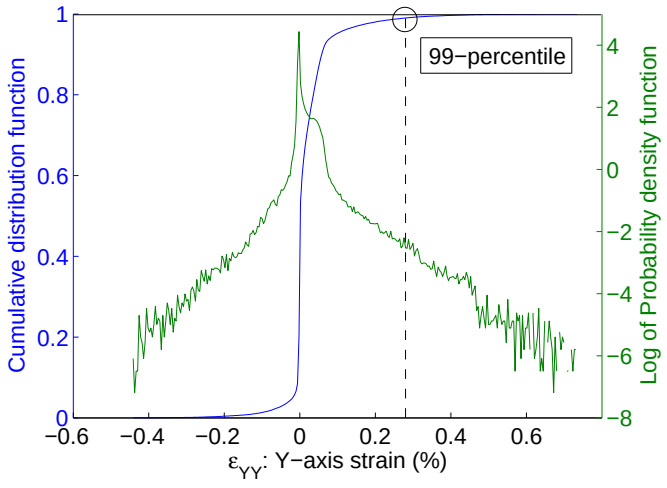
For patterned cases, the same both regions can also be distinguished (Figure 3.14). This involves that, in the first region, the strain in the electrically sensitive silicon film is largely dependent on its level in the multilayers stack. Secondly, as announced by the volume analysis, it appears clearly that, in global and local cases, patterned areas are much higher strained than others.

While this simulation work gives precious informations about the stress/strain distribution, it is not relevant for addressing the reliability issue involved with patterned and functionalized membranes. Indeed, for instance, one could extract the values at the anchoring point which look graphically the most strained (Table 3.3), but these values are mesh dependent, due to the purely elastic character of the model.

In Figure 3.14, strain peaks are present at film discontinuities. Such numerical simulation is again not relevant to estimate the height of these peaks. They are located at singularities were the stress is highly concentrated. Therefore, the membranes reliability issue should be solved by fracture mechanics tools as presented in the next section.



(a)

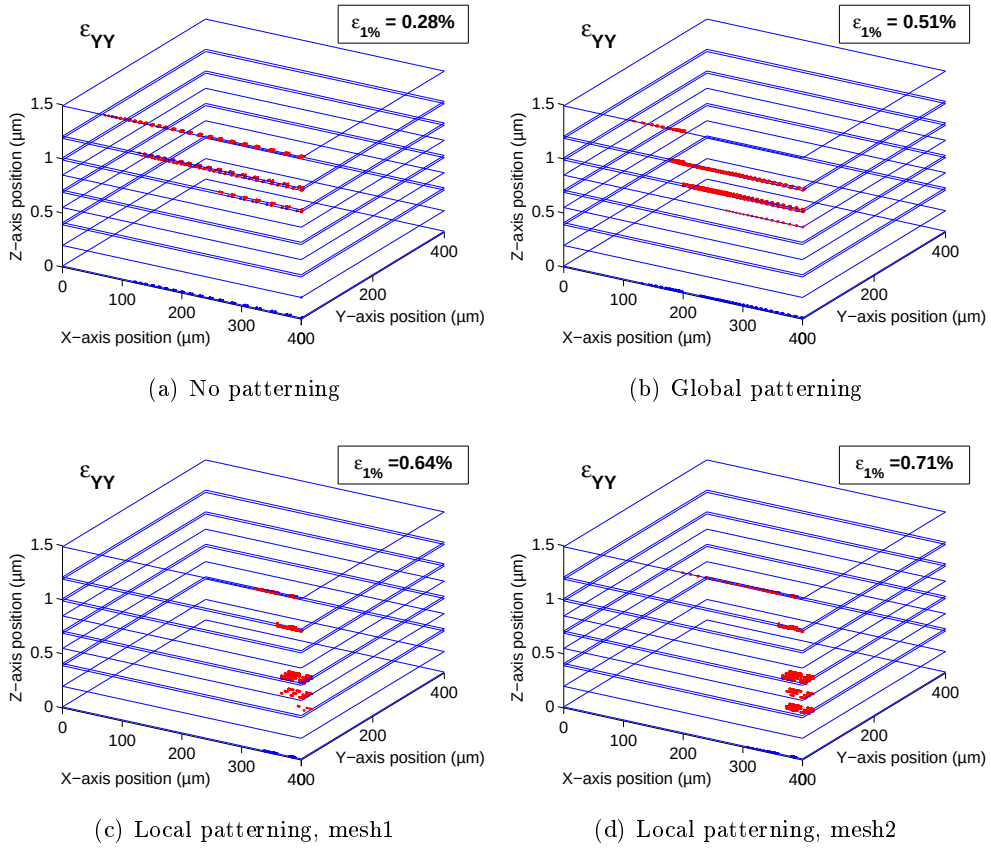


(b)

Figure 3.10: Description elements of volume analysis methodology: (a) Z-level of the 13 planes from where the points are considered, (b) Distribution functions of ε_{YY} for the blanket membrane case; the 99-percentile is identified.

ε_{YY} (%); pressure = 0.5 bar	No patterning	Global patterning	Local patterning
Bottom-layer (z = 0.0 μm)	-0.450	-0.414	-0.368
Top-layer-1 (z = 1.2 μm)	0.466	*1.00*	*0.937*
Top-layer-2 (z = 1.5 μm)	0.745	Not applicable	Not applicable

Table 3.3: Y-axis strain values at anchoring point X = 400 μm, Y = 0 μm.



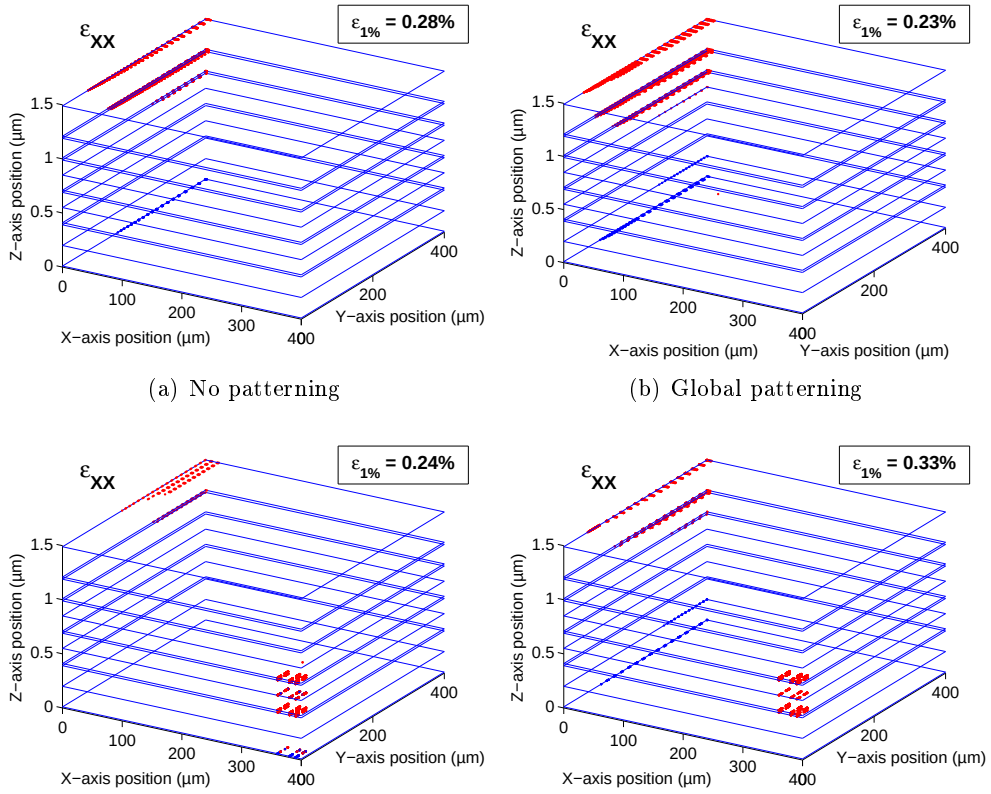
(a) No patterning

(b) Global patterning

(c) Local patterning, mesh1

(d) Local patterning, mesh2

Figure 3.11: Volume extraction of the points belonging to the 1% part of the population having the highest strain ε_{YY}; from a 800 μm-side membrane under 0.5 bar pressure; the 1% threshold ε_{YY} level is indicated.



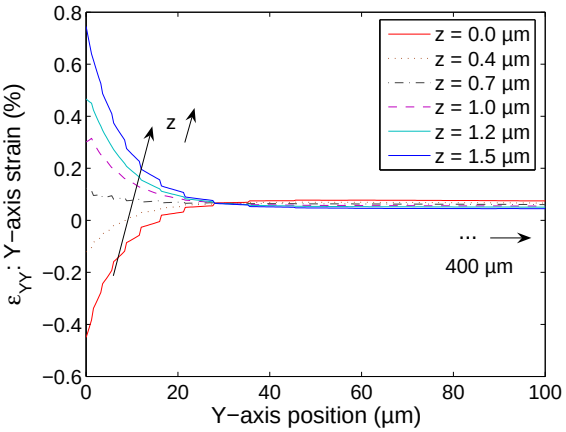
(a) No patterning

(b) Global patterning

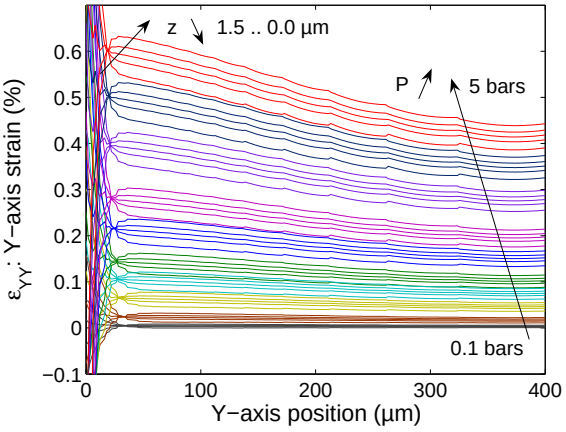
(c) Local patterning, mesh1

(d) Local patterning, mesh2

Figure 3.12: Volume extraction of the points belonging to the 1% part of the population having the highest strain ε_{XX}; from a 800 μm-side membrane under 0.5 bar pressure; the 1% threshold ε_{XX} level is indicated.

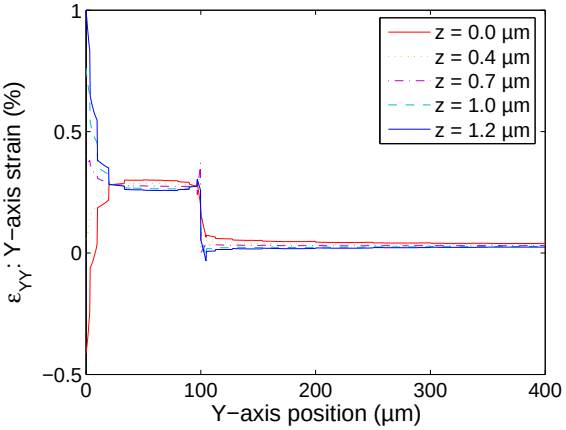


(a)

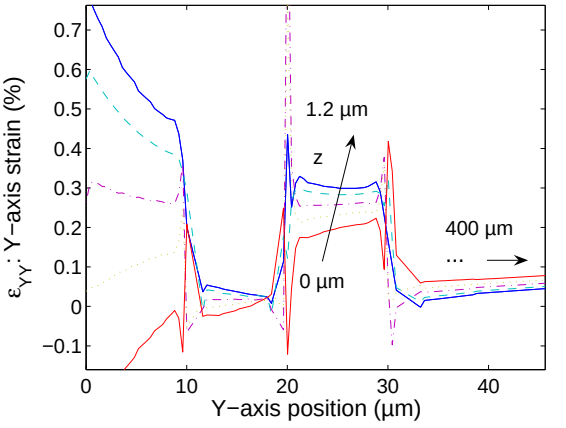


(b)

Figure 3.13: Y-axis strain of a blanket membrane along X = 400 μm symmetry axis, (a) anchor close-up (p = 0.5 bar), (b) full length view (p = 0.1... 5 bars).



(a)

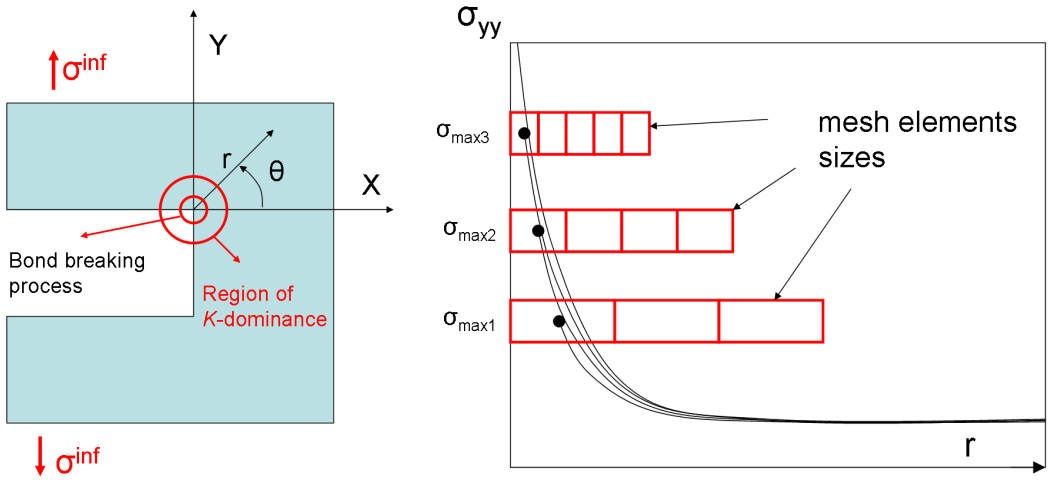


(b)

Figure 3.14: Y-axis strain of a membranes along X = 400 μm symetry axis, p = 0.5 bar, (a) globally patterned membrane, full length view, (b) locally patterned membrane, anchor close-up.

3.4 A Note About Fracture Mechanics

In the membrane structures, there exist stress concentration zones. In Figure 3.14, we have seen that at film discontinuities strain peaks are present. Moreover, the membranes edges are also zones where the stress is highly concentrated. At these points or lines, in a pure elastic material model, the stress field is defined as mathematical singularities. Therefore, the maximum stress or strain values estimated at these stress peaks depend on the thinness of the model mesh, as illustrated in Figure 3.15 for a simple example. Refining the mesh indefinitely will always bring higher stress values, simply reflecting the size of the last mesh element, because the mathematical solution in the model is infinite. In practice, the stress at the singularity is naturally finite. A notch is never perfectly sharp as well as, for instance, some plasticity may occur very locally. Hence, as a fracture criterion, a relation of the form $\sigma_{yy} = \sigma_c$ is not relevant.



(a) (b)

Figure 3.15: Simple example of a structure including singularities: (a) a notch is considered as the zone of interest, (b) illustration of the mesh dependency on the stress evaluation at the singularity.

In order to assess in a quantified way the question about the membranes reliability, this typical fracture mechanics problem should be solved with the approach of Linear Elastic Fracture Mechanics (LEFM). This phenomenological theory concerns reasonably brittle, isotropic materials experiencing cracks [6]. We would expect to find an asymptotic solution becoming progressively more accurate as we approach the crack tip. Nevertheless, at the crack tip itself, non-linear effects occur so that the LEFM is not applicable. But a second region may be considered, surrounding the non-linear zone, as the "region of K-dominance" where K is the *stress intensity factor*. Away from these regions, the fields are influenced by the solid and boundary conditions. Hence, three regions are distinguished [6] (Figure 3.15(a)):

1. Close to the crack tip, there will be a process zone, where the material

suffers irreversible damage.

2. A bit further from the crack tip, there will be a region where the linear elastic field asymptotic crack tip field might be expected to be accurate. This is known as the "region of K-dominance". The existance of this region requires the size of the plastic zone to be small with respect to the size of the structure [129]. This condition is called *Small Scale Yielding*.
3. Far from the crack tip the stress field depends on the geometry of the solid and boundary conditions.

Linear elastic fracture mechanics postulates that it is not necessary to understand in detail the complex mechanisms that take place in the process zone, since the fields in the process zone are likely to be controlled mainly by the fields in the region of K-dominance. The fields in this region depend only on the stress intensity factor K which can phenomenologically characterize the process zone. In tri-dimensional problems three opening modes can be considered (Figure 3.16), involving the determination of three factors (K_I, K_{II} and K_{III}). In linear elasticity, more complex loading configurations may be expressed as a linear combination of these three modes [129].

Expressions for K have been determined by the resolution of elasticity equations for a large number of geometries and loading configurations (e.g. Lawn [103]) while for complex cases only numerical methods can be employed [129].

In plain strain and mode I, the failure criterion writes

$$K_I \geq K_{Ic}, \tag{3.1}$$

where K_{Ic} is the critical value of K_I and is called the *fracture toughness* of the material. It is an "intrinsic" property of a material [129] but can vary with the temperature, velocity of crack and environmental conditions.

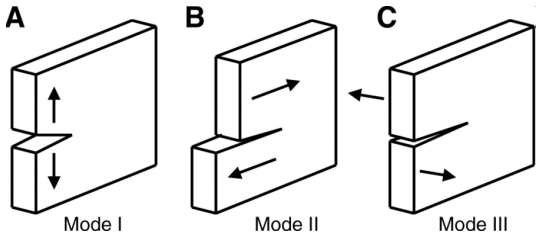


Figure 3.16: Three modes of opening: (A) mode I: tensile opening (cleavage); (B) mode II: in-plane shearing; and (C) mode III: anti-plane shearing (tearing) [2].

A practical case of patterned membranes is illustrated in Figure 3.17. It concerns the patterning around small devices. The problem resolution passes by the sequential consideration of all singularities present on the membrane and by the evaluation of their stress intensity factors K_i. These factors have to be compared with the fracture toughness of the relative materials.

In a two-dimensional (2D) problem, Luo [110] has applied the method to the study of an integrated circuit interconnection stack. He distinguishes three main categories of stress singularities arising in microelectronics:

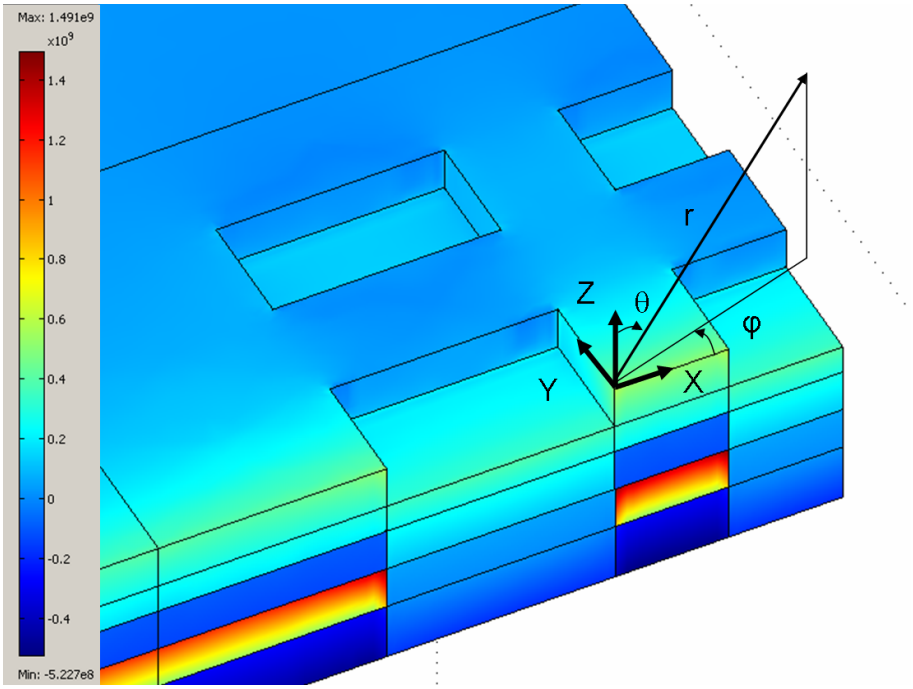


Figure 3.17: Tri-dimensional problem of locally patterned membranes (close-up on the border devices patterns); σ_{yy} is plotted on the apparent surfaces (Pa), the membrane is 800 μm-wide, under a pressure of 0.5 bar.

1. Angular corner of homogeneous material (Figure 3.18(a)),
2. Angular corner of a bi-material wedge (Figure 3.18(b)),
3. Multi-material wedge with adhesion at all interfaces (Figure 3.18(c) and (d)).

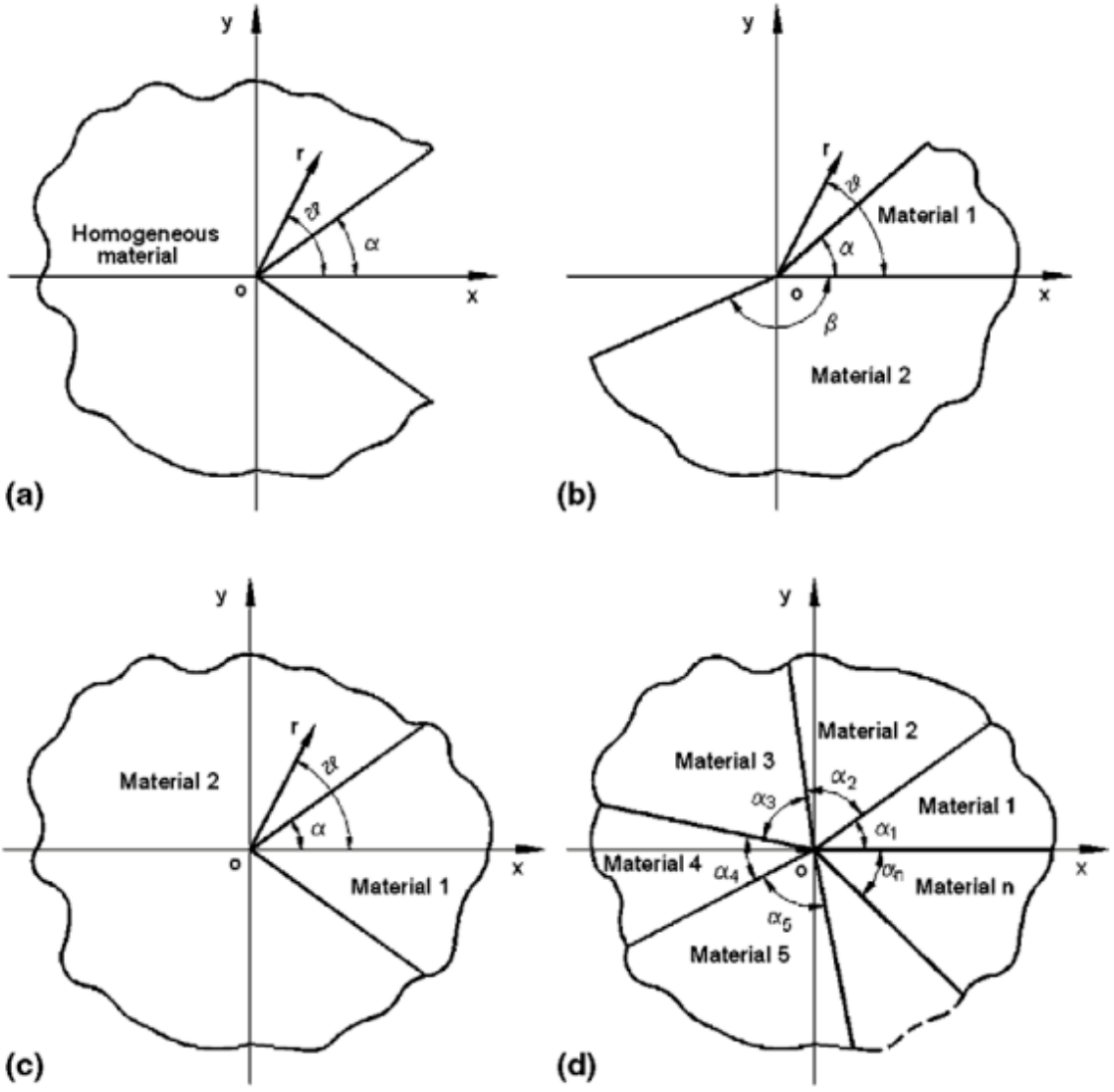


Figure 3.18: Classification of multi-material wedges: (a) angular corner of a homogeneous material, (b) angular corner of a bi-material wedge, (c) bi-material wedge with adhesion at both interfaces, (d) multi-material wedge with adhesion at all interfaces.

In a tri-dimensional (3D) case, the singularities inventory will then include all edges as well as all material discontinuities and interfaces. To our knowledge, very few authors have assessed the resolution of a 3D problem involving multiple singularities and multi-materials was never reported in the literature. One can point out the paper of Koguchi [97] who has

solved the problem of the order of stress singularity near the vertex in in 3D joints . In our case, extending the formulation of Luo [110], the stresses near the edge of an interface can be described asymptotically as:

$$\sigma_{ij} = \sum_{n=1}^{N} K_n r^{-\lambda_n} f_{ijn}(\phi, \theta) + \sigma_{ij0}(\phi, \theta) \tag{3.2}$$

where r, ϕ and θ are the polar coordinates, N the total number of singularities. λ_n is the order of singularities. The angular function $f_{ijn}(\phi, \theta)$ can be completely determined by an asymptotic analysis; it is dependent on the geometry as well as the mechanical and thermal properties of the composite structure. Nevertheless, the complete resolution of this problem is beyond the scope of the present thesis.

3.5 A Comment about Thin Films Robustness

Membranes are stress platforms. Films and devices experience stress at various levels according to the applied pressure but also to their location laterally or vertically in the thin films stack. From previous section we have seen that, in 800 μm-side patterned membranes, the areas where the silicon nitride is removed are under a strain approaching 0.3–1% when the pressure is 0.5 bar. The thickness of the films ranges from 300 to 500 nm for the films deposited on large areas. Films involved in device fabrication are thinner: 100 nm for the silicon channel and 27 nm for the gate oxide. It is therfore interesting to examine the influence of the films thicknesses on their mechanical properties from published papers. The results presented here concern silicon and polysilicon studies. *The elements on Weibull theory given this section come essentially from Borrero [25].*

First, it is worth to note that fracture of brittle materials (like Si, SiO_2 and Si_3N_4) initiates from randomly distributed flaws. Hence, a statistical treatment is very well suited for its study. In that frame, the most used theory is based on Weibull's works which relies on the hypothesis of the weakest link. Indeed, the strength of a body is ensured by the survival probabilities of smaller individual elements that constitute the body. Therefore, the body subsistence is evaluated by multiplying the survival probabilities of the smaller elements. It is worth to note that this theory assumes the absence of interaction between the flaws. For a uniaxial stress, we have:

$$P_f = 1 - \exp\left[-\int_V \left(\frac{\sigma - \sigma_u}{\sigma_0}\right)^m \mathrm{d}V\right], \tag{3.3}$$

where P_f is the fracture probability of an object at a given stress σ. σ_0 is the characteristic strength i.e. the strength for which 63% of failure is obtained. σ_u is the 0%-failure strength, usually 0 GPa. m is the Wiebull modulus depending on the shape of the sample. For a given geometry, the integration of Equation (3.3) writes:

$$P_f = 1 - \exp\left(\frac{\sigma}{\sigma_\theta}\right)^m, \tag{3.4}$$

where σ_θ is the characteristic strength for a given geometry, related to σ_0 through:

$$\sigma_0 = \sigma_\theta V_{eff}^{1/m} \tag{3.5}$$

The effective volume of the component, V_{eff}, is defined as the volume of an equivalent sample — having the same probability of failure — subjected to uniform stress. Equation (3.5) can be used to convert strength values obtained in different test geometries, thereby permitting comparison.

The most important consequence of Weibull theory is the existence of a size effect in strength. Indeed, considering Equation (3.5) for two specimens of volumes V_1 and V_2 results in:

$$\frac{\sigma_{\theta_1}}{\sigma_{\theta_2}} = \left(\frac{V_{eff,2}}{V_{eff,1}}\right)^{1/m} \tag{3.6}$$

Equation (3.6) expresses that a decrease of the specimen size results in an increase of the characteristic strength. The strength size effect arises from the observation that it is more likely to find a major flaw in a large than in a small specimen, provided that flaws do not interact.

Practically, many groups have successfully experimented such property on thin films or nanowires. As a first example, Tsuchiya [165] has studied the size effect of polysilicon (P-Si) samples by performing tensile tests with an electrostatic actuating system build inside a scanning electron microscope (SEM). The P-Si samples were varied with the following ranges of dimensions: 30–300 μm-long, 2–5 μm-wide and 2 μm-thick. An increase by 40% of the tensile strength was measured, moving from 2.0 to 2.8 GPa (2.7 GPa for doped P-Si).

In a second example, Zhu [190] worked on much smaller structures i.e. silicon nanowires with diameters of 15–60 nm and length between 1.5 and 4.3 μm. These structures were actuated by a nanomanipulator as the actuator and an atomic force microscope (AFM) cantilever as the load sensor inside a SEM. Zhu evidenced a decrease of the Young's Modulus for nanowires smaller than 30 nm diameter, while the fracture strength of the nanowires was measured at a maximum value of 12 GPa. Zhu also compares nanowires with thin films properties change has a function of the surface area, showing how faster small volumes reach high behavior modification compared to large but thin films (Figure 3.19).

Very recently Dr. Vikram Passi [132] and Umesh Bhaskar [22] have published succesfull experiments with on-chip actuated single cristal silicon nanowires and nanoribbons. They measured strain values up to 5% for nanowires with a cross-section of 50×50 nm^2 and 25 μm-long. Strains of 3% were reproducible. In [22], a drop of the Young's Modulus was also measured from 160 GPa down to 108 GPa when the thickness was varied from 200 nm to 50 nm. Besides, the authors have shown very promosing first results on electronic transport study on such structures.

Finally, one can mention that the size effect leading to high fracture strain for small samples is not always verified. Borrero [25] has experimented a "reverse size effect" involving an early fracture strength for thinner deposited films. The material under investigation

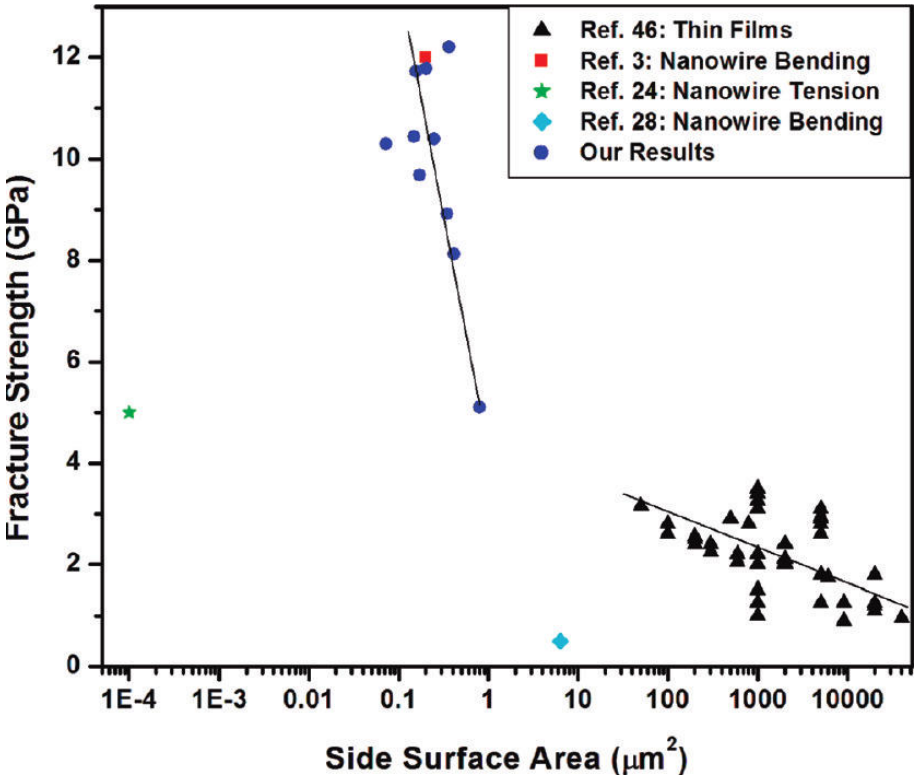


Figure 3.19: Plot of fracture strength versus the side surface area of the Si nanowires and thin films. References 3, 24, 28 and 46 are respectively [75], [92], [154] and [164] in this work, *reproduced from Zhu [190].*

was brittle Tantalum Carbide. This effect was attribued to the presence of critical defects of comparable size in all films, leading to higher stress intensity factors with decreasing thickness. In a general way, such effect is applicable to any thin film where the size of the defects are on the order of the specimen size.

3.6 Mechanical Experiments and Measurements

In addition to numerical modeling, experimental demonstration is achieved.

3.6.1 Smaller Patterned Membranes - Patterning Method

Complementary experiments are performed on smaller membranes, with various patterning designs, not functionalized with devices but having a films stack comparative to simulations case (i.e. with a Si_3N_4 film discontinuity). The stack is illustrated in Figure 3.20, while the membranes are inventoried in Figure 3.21. Deflection and burst pressure measurements are reported in the same figure. In these experiments, the influence of the patterning design on the membranes robustness was not evidenced. But thanks to their smaller size (ranging from 200 to 240 μm), the structures withstood pressure values up to 4 bars. The smallest membrane did not break at the maximum pressure of 5 bars. These high pressure values are appreciable for the application in pressure sensing systems.

Besides, one can also wonder if the patterning method has a potential influence on the robustness of the membrane. Indeed, the nitride film, as well as any other thin layer, may be etched-away by humid or dry process. A humid method has in general the advantage of having a very good selectivity on other materials but usually be an isotropic process. The process has generally the inverse characteristics, being less selective but more anisotropic. Beyond the risk of over-etch, a plasma process might also damage the surface of the underlying layer and weaken it.

In the present case, Si_3N_4 is wet etched in a bath of hot H_3PO_4 at 145°C. The nitride etching rate is 2 nm/min. It has a selectivity of 140 with respect to thermal SiO_2 and of 17 to Si. When etched with a dry method, as it is the case in the full process, a combination of SF_6 and CHF_3 plasmas is used. Figure 3.21(e) reports measurements under pressure either for dry and wet patterned membranes. No drop of mechanical withstanding is noticed with the dry etched ones, although the plasma etching has involved an over-etch of 40 nm from the 365 nm ab initio of the underlying SiO_2 film.

3.6.2 Additive Patterning Effect

So far in the development the sole case of SiN film patterning was treated. However, on a functionalized membrane, with the exception of the buried oxide, all present films are patterned. In this section, we selected two significant materials present on membranes when devices are concomitantly integrated: aluminum and polysilicon (P-Si).

These materials are placed with their respective thickness and at their respective level in the stack as proposed in the full process (cf. Chapter 2). It is illustrated in Figure 3.22, the Al is 800 nm-thick and the P-Si is 320 nm-thick. The layers patterning was made by wet etching for the Al layer, in H_3PO_4:IPA (5:2), and $SiCl_4$ plasma for the P-Si. No significant

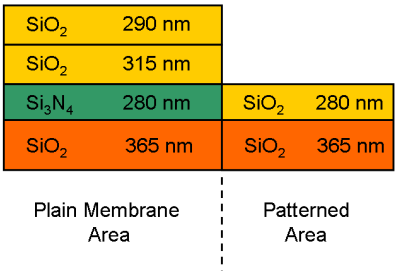


Figure 3.20: Layers stack of small Si_3N_4 patterned membranes.

over-etch of the underlying nitride film was noticed. The pattern design is composed of 25 μm-width strips, regularly spaced also by 25 μm, as it is photographed in Figure3.23.

Characterization under pressure are reported in Figure 3.24(a), evidencing that a mechanical weakening of the membrane is involved by the addition of strips. Patterned membranes of ~600 μm-side do burst at the early pressure value of 4 bars, either with supplemental strips of Al or P-Si. Additionally, a ~800 μm-side membrane do burst at 2 bars. Figure 3.24(b) illustrates measurements made on similar 3-layers O-N-O membrane with no burst occurring up to the maximal pressure of 5 bars.

Besides, topographical measurements are performed on an Al-patterned membrane, examining a potential hysteresis originating from a permanent plastic deformation of the metallic layer. Form the present experiment, it appears that no such hysteresis occurs after a 0-4.5 bar pressure cycle (Figure 3.25).

3.7 Conclusions and perspectives for improved designs

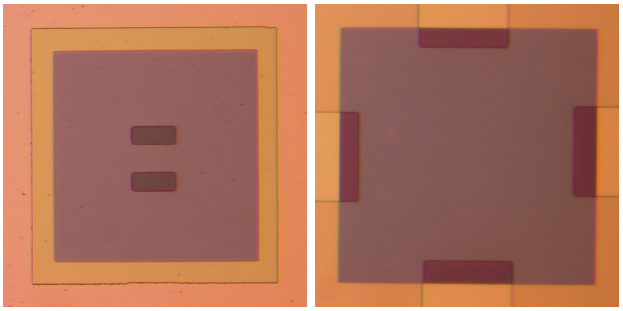
In the problem description, introducing the chapter, the problem of functionalized membrane robustness was clearly enounced. It was also pointed out elements indicating that the patterning of the nitride film in the membranes stack had to be considered.

By analyzing the problem through the scope of FEM simulations, precious information about strain distribution in the membranes was provided. It was shown that, near the borders, the strain is higher but accompanied with a high strain gradient. In these regions, there is also flexure strain implying a high fiber dependence on the strain. At the opposite, in the central region (i.e. from 30 μm away from the borders), there is an almost steady tensile strain lowly dependent laterally as well as along the vertical axis.

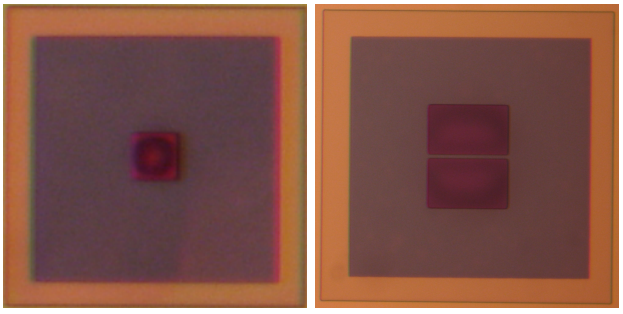
Moreover, the FEM simulations have shown that (i) the mean stress is higher in patterned areas and (ii) there exist strain peaks at film discontinuities. Reformulated we have that, with film patterning, there is more surface exposed to high strain and there are more points where the strain is concentrated.

Weibull theory was shortly presented. As a consequence of theory, exposing larger surfaces to a higher stress will inevitably rise the fracture probability.

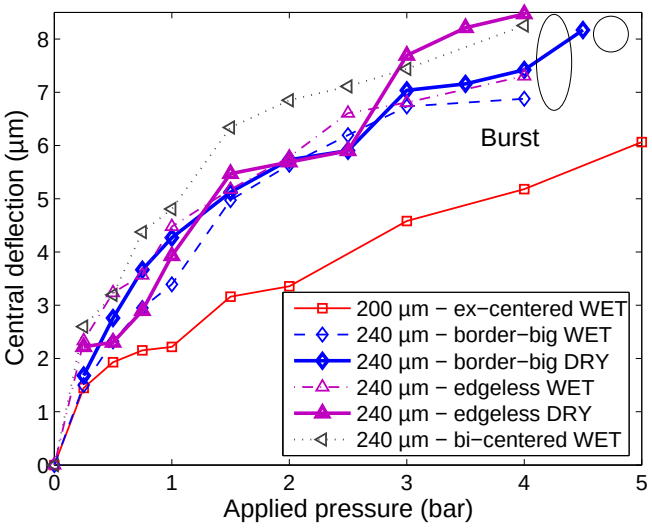
Besides, it was evidenced that a simple strain extraction at a point graphically ap-



(a) 200 μm, 'ex-centered' (b) 240 μm, 'border-big'

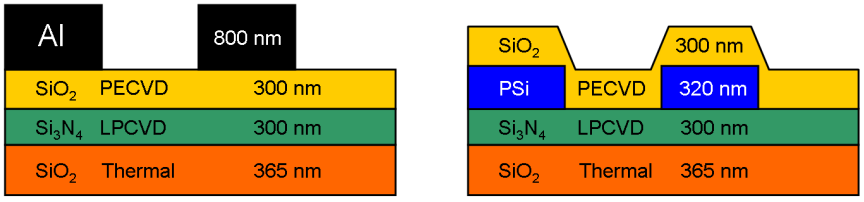


(c) 240 μm, 'edgeless' (d) 240 μm, 'bi-centered'



(e)

Figure 3.21: Small Si_3N_4 patterned membranes of 200-240 μm-side, (a-d) photographs of four patterned designs, (e) corresponding deflection measurements and burst pressure evaluation.



(a) Aluminium layer added on top (b) Polysilicon film inserted

Figure 3.22: Membrane stack description with additional patterned layers to blanket 3-layered O-N-O stack.

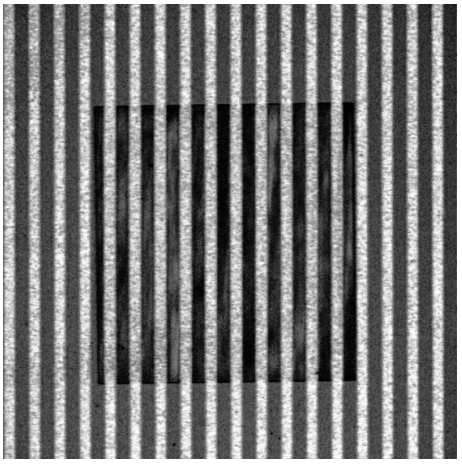
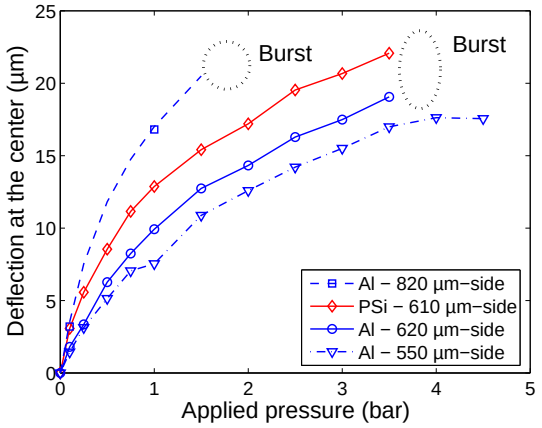
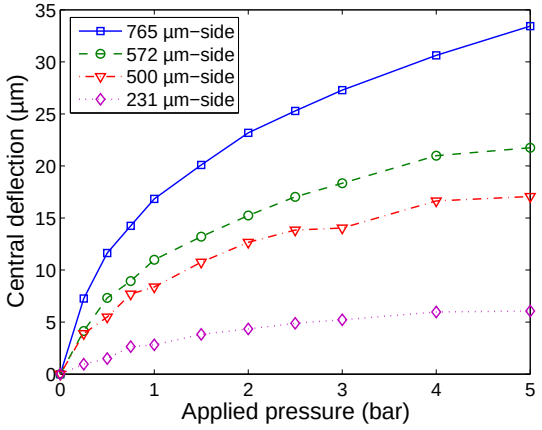


Figure 3.23: Photograph of a 550 μm-width membrane with an additional 800 nm-thick patterned aluminium layer over a blanket 3-layered O-N-O stack; the Al strips are 25 μm-width and distant of 25 μm.

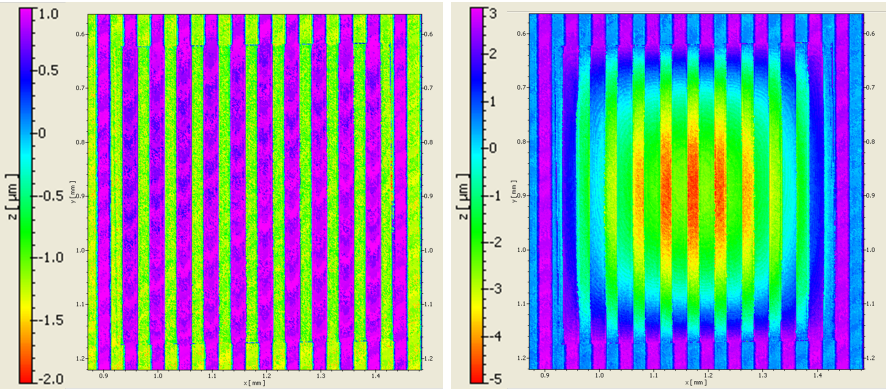


(a) 3-layered O-N-O membranes with additional patterned layers

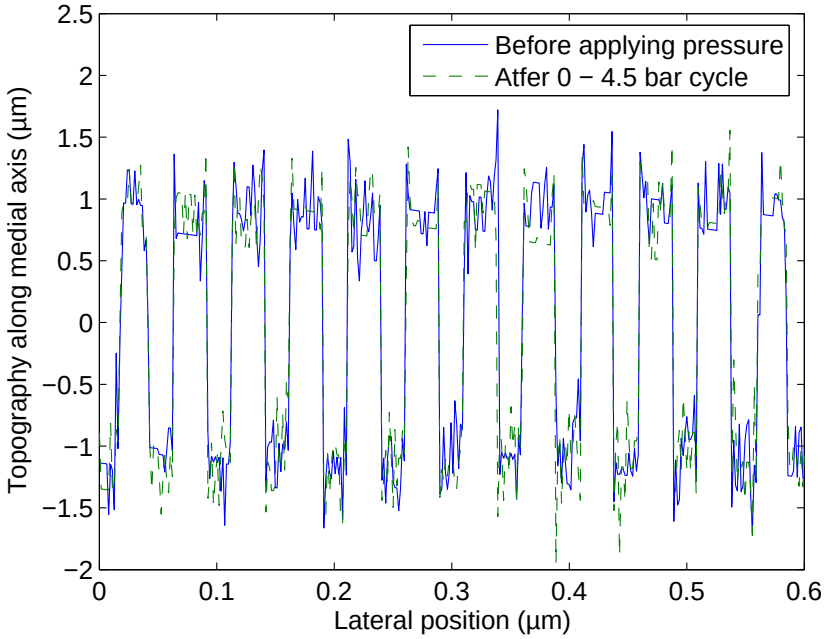


(b) Blanket 3-layered O-N-O membranes

Figure 3.24: Membrane deflections as a function of the pressure and burst pressure values estimation for (a) various 3-layered membranes sizes and additional patterned layers, (b) blanket 3-layered membranes as a comparison.



(a) Topography at p = 0.0 bar (b) Topography at p = 0.5 bar



(c) Topography hysteresis

Figure 3.25: Membrane topography examination under pressure; the membrane is 550 μm-side with a 800 nm-thick Al layer added on simple 3-layers O-N-O stack. Images height full-scale ranges are (a) 2 μ and (b) 8 μm. The membrane is at the center of the profile given in (c)

pearing as the most strained point is not a relevant way for solving the reliability issue. This is a limitation of the isotropic elastic model. Therefore, the strain peaks as all other singularities must be addressed by the linear elastic fracture mechanics. With this method a stress intensity factor can be calculated, giving a precise quantification of the local stress and, hence, allowing to draw solid conclusions.

Complementary experiments have proved that, obviously, the robustness is greatly enhanced by combining reduced membranes size with reduced patterned areas and, furthermore, that additional patterned layers do also, paradoxally, weaken the thin membranes.

On the basis of these conclusions, an ideal active pressure sensor design will then:

a. Implement reduced membranes sizes with reduced patterned structures (transducers) footprint, in order to ensure sufficient robustness;

b. Position the active devices at the central region of the membrane for enlarging the process window (i.e. the lateral definition of the membranes).

Chapter 4

Novel Pressure Sensor Architectures - Towards A Concept Validation

4.1 Introduction

On the basis of the mechanical analysis of patterned membranes exposed in Chapter 3, this chapter explores solutions and presents novel pressure sensor architectures which are figured out and experimented with the target of reducing the transducers footprint on the membranes. All of them are measured under calibrated pressure with the set-up described in Section 3.2.2. Besides a drift effect is newly observed and assessed in the present chapter.

4.2 Single N-MOSFET Suspended Transducer

A first solution consists in suspending a single MOS transistor used as a current source varying with the pressure applied on the membrane and controlling a current-starved out-of-membrane ring oscillator. The schematics of a such architecture is illustrated in Figure 4.1.

With the complete suspended ring oscillators pair architecture presented in Chapter 2, it is necessary to consider the ratio of both oscillators output frequencies for defining a temperature independent signal. In the present case, the use of a current-starved ring oscillator topology controlled by the MOS current source allows a current to frequency conversion with controlled frequency and consumption. Biasing the gate of the source device at its Zero Temperature Coefficient (ZTC) voltage may provide a temperature independent behavior to the system. Moreover, targeting a limited current consumption, the intrinsic suspended device is designed with a very long channel (i.e. $L = 120$ μm, $W = 6$ μm).

4.2.1 Influence of the Geometrical Parameters

In order to investigate the sensitivity to the pressure as well as having sensor pressure-range estimations, N-source devices are implemented in various configurations in terms of membrane size and position on the membrane, with or without connected oscillator. The devices themselves are declined in two configurations. The first device design features a classical monolithic channel, as illustrated in Figure 4.2, in order to locate the device near membranes borders. The second design intends to give a robust behavior to the system

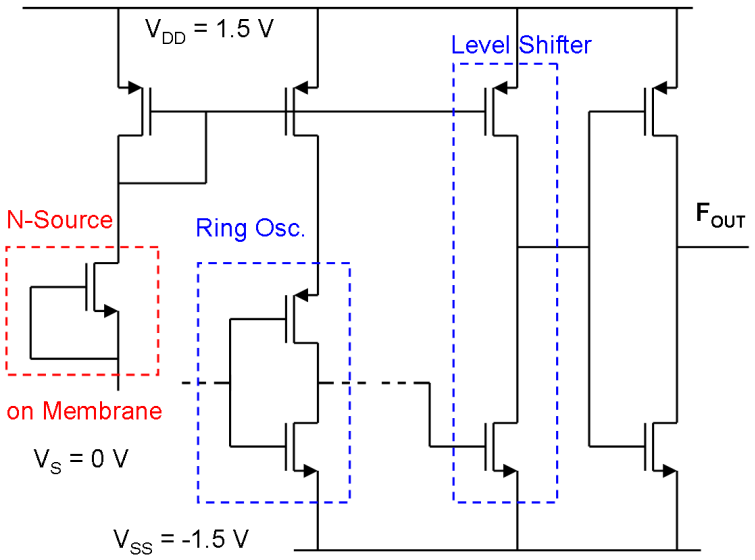


Figure 4.1: Smart pressure sensor schematics of a single intrinsic N-Source suspended pressure transducer, commanding an out-of-membrane oscillator (Circuit design: Bertrand Rue).

when the device is located at the center of a membrane. Figure 4.3 gives a complete view of a rectangular membrane hosting a N-source device with its channel divided in four parallel segments. This original design justifies its geometry from Chapter's 3 conclusions in terms of reduced footprint on the membrane, but also by integrating the transducer at the center of the membrane. Thanks to its identically signed piezoresistive coefficients, a N-MOSFET takes advantage being located at the center of a membrane with the weighted sum of the strain components contribution to the drain current variation.

Figures 4.4 and 4.5 give the I_D curves as a function of the time, while the pressure was increased by 100 mbar per step, and the corresponding I_D-pressure curves. Figure 4.4 concerns monolithic devices implemented at the border of square membranes. On the 600 μm-side membrane the current was drifted. A correction was therefore applied to establish the true pressure sensitivity. This correction consists in evaluating the slope at each pressure plateau (from 35 to 82 nA/s), where the current is supposed to be steady, and the mean value of these slopes (56 nA/s) was added to I_D. The drift issue is addressed in Section 4.4. Figure 4.5 concerns the current sensitivity to the pressure of the 4-segmented device located at the center of a 250 x 400 μm^2 rectangular membrane. The corresponding sensitivities are summarized in Table 4.1.

4.2.2 Influence of Bias Point

Pushing towards lowering power requirements, it is of first interest to look at the pressure sensitivity in lower current operating regions. Figure 4.6 gives the results at four bias points embracing the threshold voltage. Being its usual operating regime in the complete system, the device is kept in saturation in all measured cases.

When decreasing the gate voltage, the sensitivity on the full scale is maintained (18-

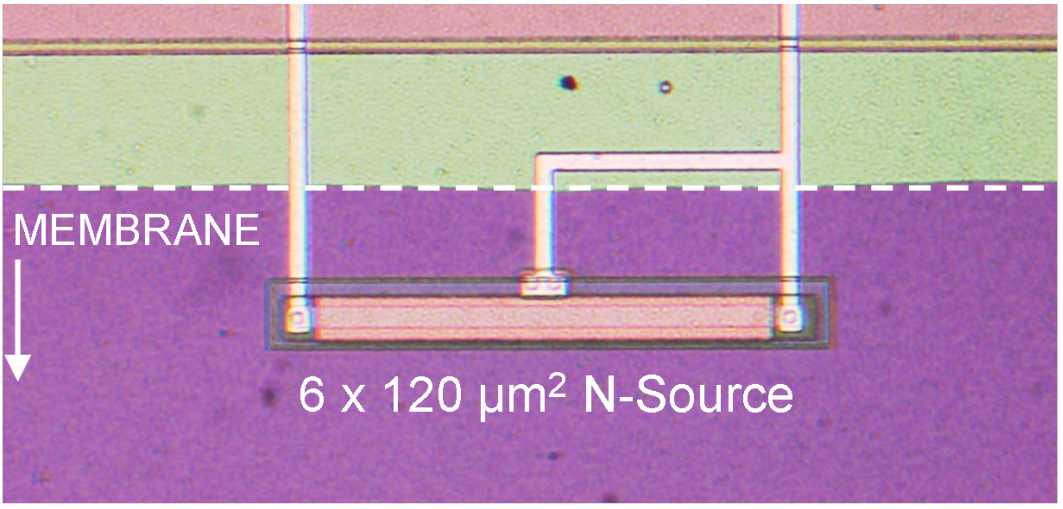


Figure 4.2: Photograph of a single intrinsic N-Source pressure transducer; the device is $L = 120$ μm, $W = 6$ μm; the device implemented at the border of square membranes of 340, 600 and 800 μm-side.

Configuration	Sensitivity (%/bar)*	FS Variation (%)**	Measured range		Burst Pres. (bar)
			Min (bar)	Max (bar)	
Mb: 250 x 400 μm^2 at the center	**4.59**	**19.58**	**0.1**	**4.8**	$\geq$ **4.8**
Mb: 340 x 340 μm^2 60 μm from border	2.56	7.20	0.5	3.5	4
Mb: 340 x 340 μm^2 27 μm from border	1.79	5.21	0.5	3.5	4
Mb: 600 x 600 μm^2 35 μm from border	3.23	3.73	0.1	1.4	1.4
Mb: 800 x 800 μm^2 35 μm from border	3.09	3.39	0.1	1.3	1.3

Table 4.1: Electrical and mechanical figures of merit of the N-Source transducers and their associated membranes for all fabricated configurations, *the reference value is linearly extrapolated at 0 bar, **on measured range.

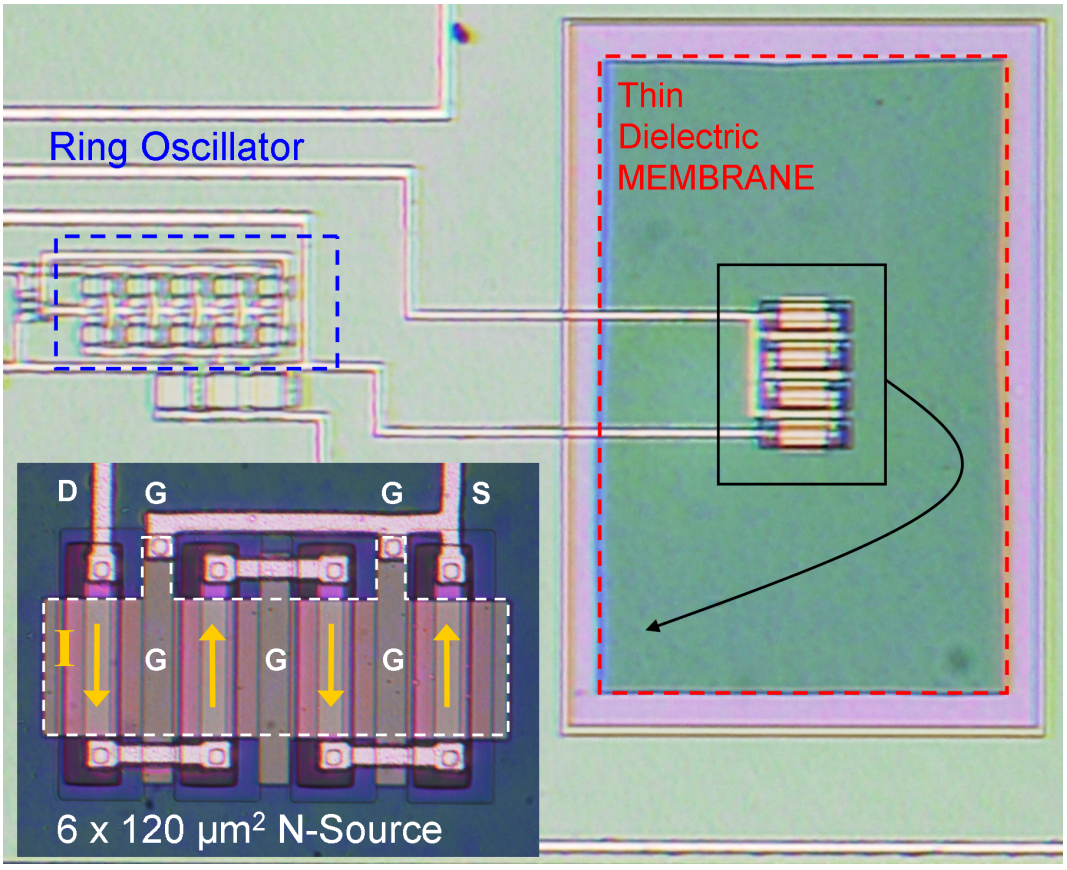


Figure 4.3: Photograph of a single intrinsic N-Source pressure transducer, commanding an out-of-membrane 5 steps oscillator; the membrane is 250 x 400 μm^2; the multi-segmented device is L = 120 μm, w = 6 μm; the current passes along 4 segments of L = 30 μm, W = 6 μm; the terminals are identified; the polysilicon gate (G) is surrounded by a white dashed line; the gate is connected to the source (S).

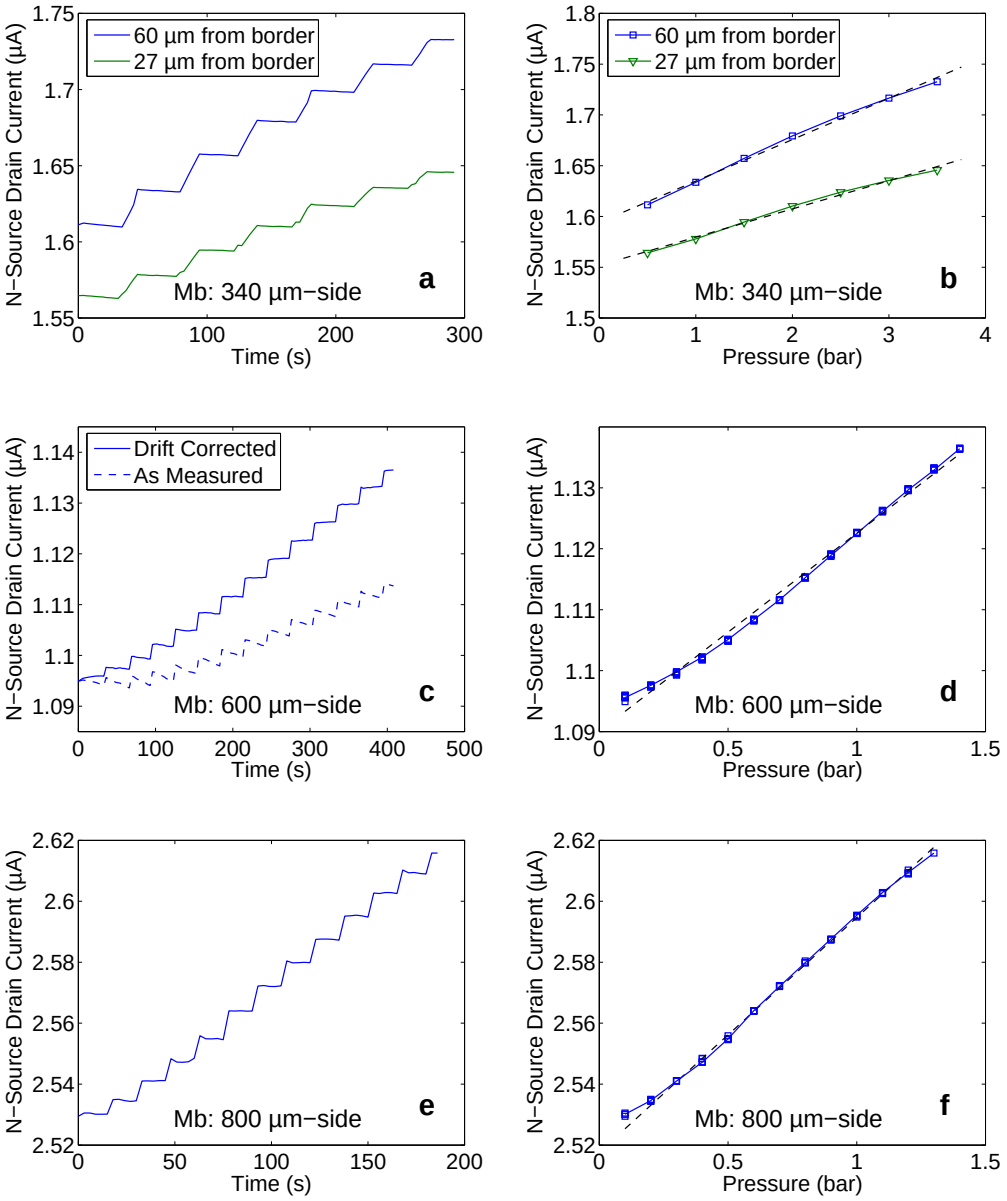


Figure 4.4: Drain current of N-Source devices as a function of the time (under pressure ramp with 100 mbar steps) and converted to the pressure, for various membrane sizes and positions: **(a-b)** 340 μm-side, independent devices, $V_S = V_G = 0$ V, $V_D = 1.5$ V, **(c-d)** 600 μm-side, 27 μm from border, device connected to an oscillator, $V_S = V_G = 0$ V, **(e-f)** 800 μm-side, 35 μm from border, device connected to an oscillator $V_S = V_G = 0$ V; *the corresponding sensitivities are reported in Table 4.1*; the devices have one monolithic silicon channel $L = 120$ μm, $W = 6$ μm, as illustrated in Figure 4.2.

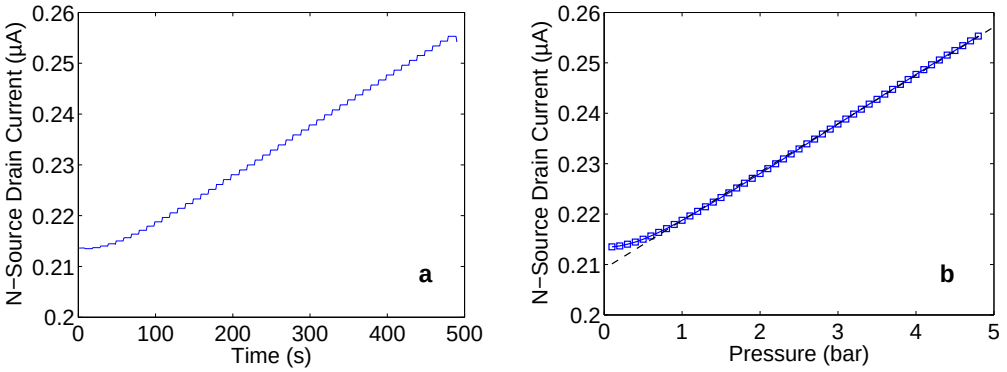


Figure 4.5: Drain current of a 4-segments channel N-Source device as a function of (a) the time (under pressure ramp with 100 mbar steps) and (b) converted to the pressure; the membrane is 250 x 400 μm^2; the device has its drain connected to an out-of-membrane oscillator, $V_S = V_G = 0$ V.

20%) but the drain current linearity drops drastically, in particular at lower pressure values. From this observation, it is preferred to operate the device over the threshold voltage.

4.2.3 Systems Performances

Finally, the output frequencies of two configurations are reported as a function of the pressure.

The first configuration concerns a system with a monolithic channel device located at 27 μm from the border of a 600 μm-side membrane and is given in Figure 4.7. Due to a noticeable drift on the measurement, the procedure adopted to evaluate the output frequency includes F to be noted twice at each pressure step (Figure 4.8). A drift corrected value[1] is obtained by cumulating the difference observed between the two readouts and gives a full-scale frequency variation of 2.8%, rising the frequency value from 885 kHz at 100 mbar to 908 kHz at 1.4 bar. This brings the output frequency sensitivity to the pressure at 2%/bar. The membrane bursted at 1.4 bar preventing a second frequency readout at that pressure value.

The second configuration concerns a system with a 4-segmented channel source-device located at the center of a 250 $\times$ 400 μm^2 rectangular membrane. In this case, a current drift is observed when no pressure is applied on the membrane, in the order of 3.3 pA/s or 1.3e-3%/s (Figure 4.9). When 0.5 bar pressure are applied, the drift falls to 0.3 pA/s or 1e-4%/s and a current value that seems stabilized, is reached after 400 s. As illustrated in Figure 4.10, the output frequency varies from 344 to 384 kHz (12%) and the transducer current from 213 to 255 nA (20%) when the pressure is increased from 0.1 to 4.8 bar. This brings the output frequency sensitivity at 2.6%/bar. It is worth to note that at the maximum pressure value of 4.8, the membrane has not broken, making this configuration the most robust of all tested. Additionally, the current-starved ring oscillator topology

[1]formally: $F_{\mathrm{COR}}(p_i) = F_1(p_i) + 2\sum_{j=1}^{i-1}(F_1(p_j) - F_2(p_j))$

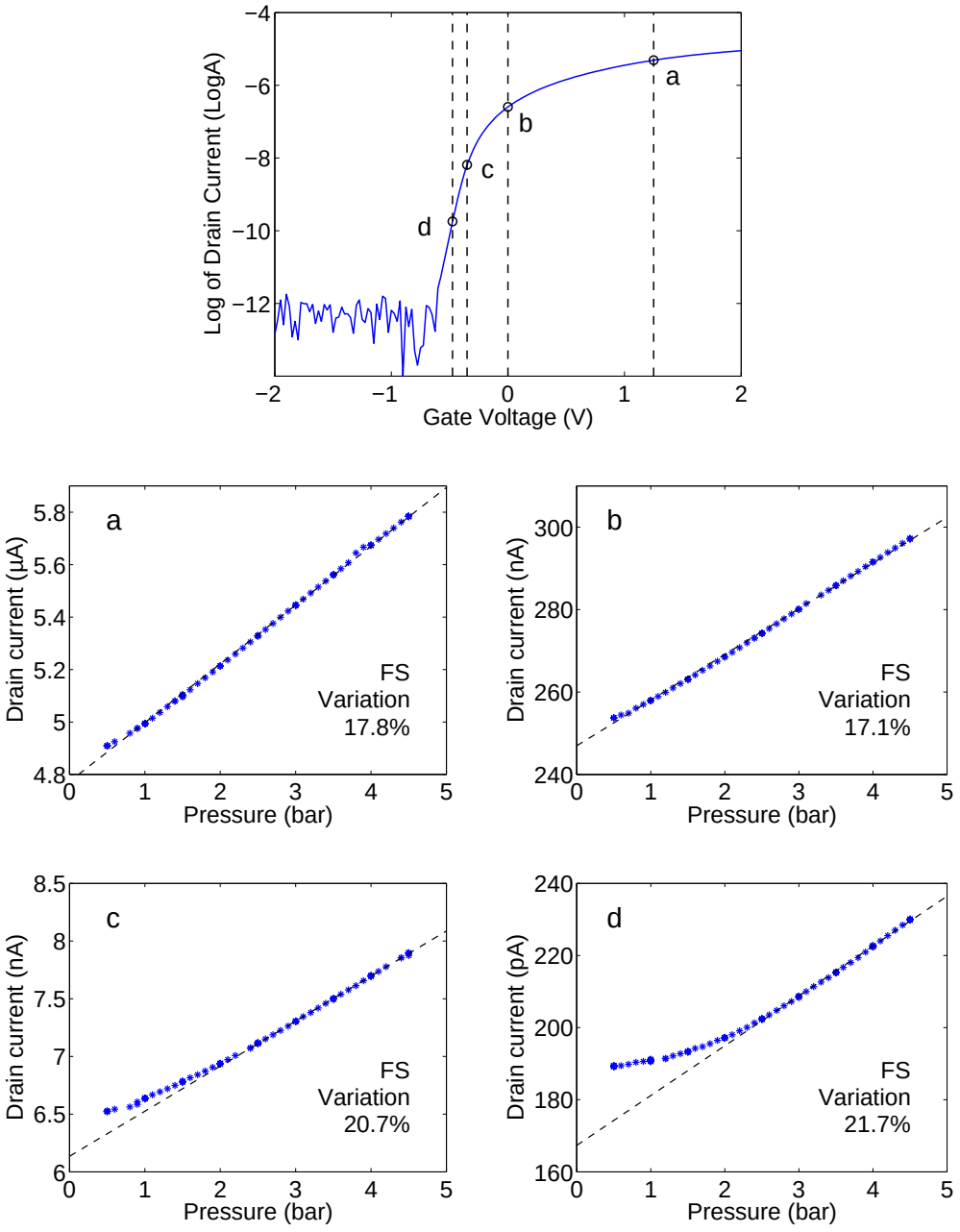


Figure 4.6: Drain current of the N-Source device as a function of the pressure (V_S = 0 V, V_D = 1.5 V), at 4 gate voltage bias points: (a) V_G = 1.25 V, (b) V_G = 0 V, (c) V_G = -0.35 V, (d) V_G = -0.475 V; in each case the full-scale variation is indicated; this variation is strictly evaluated from the points measured; the top figure shows the position of the bias points on I_D-V_G reference curve.

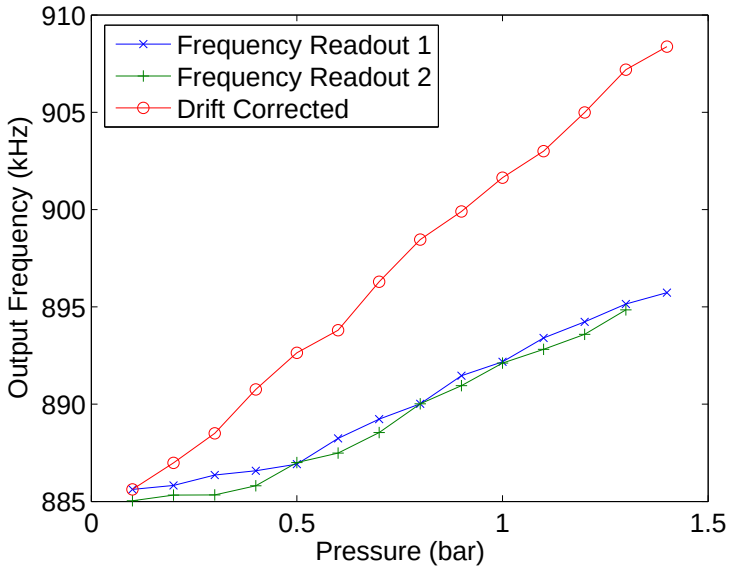


Figure 4.7: Output frequency as a function of the pressure for a device at 27 μm from the border of a 600 x 600 μm^2 membrane; the frequency measurement procedure is described in Figure 4.8; the drift correction consists in the cumulative compensation of $F_{\text{READOUT2}} - F_{\text{READOUT1}}$.

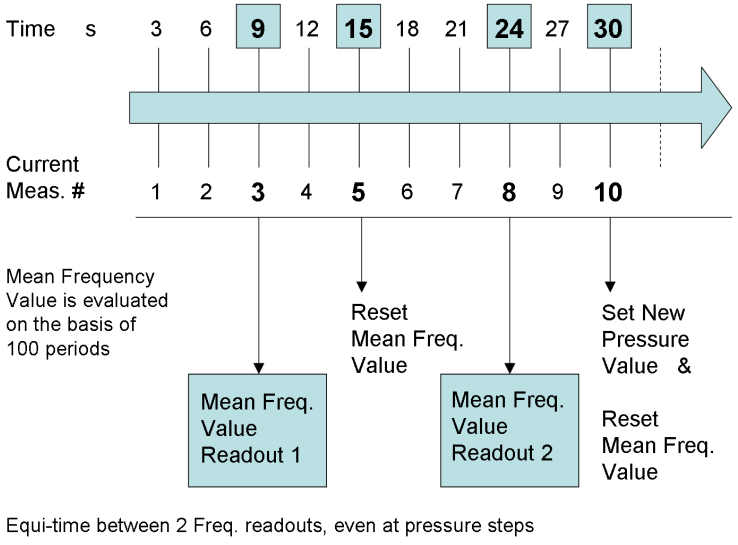


Figure 4.8: Description of the procedure adopted for the frequency measurement; each pressure step lasts 30 s and the current is measured every 3 s; at each pressure step the frequency is read twice; all frequency readouts are equi-distant in time (15 s); the frequencies are computed as the mean value of the last 100 periods of the output signal on an Agilent MSO8104A oscilloscope.

controlled by the MOS current source features to the system a very advantageously low sensitivity to the suplly voltage, as illustrated in Figure 4.11. The output frequency, as well as the N-Source current, varies of less than 1% when the supply voltage is decreased from 3 to 1.25 V. Besides, the consumption of the full circuit, including the output buffers loaded with 200 pF cables, is 50 μA $*$ 3 V = 150 μW. The power consumption of the sole sensing circuit (i.e. the ring oscillator) is as low as 700 nA $*$ 3 V = 2.1 μW.

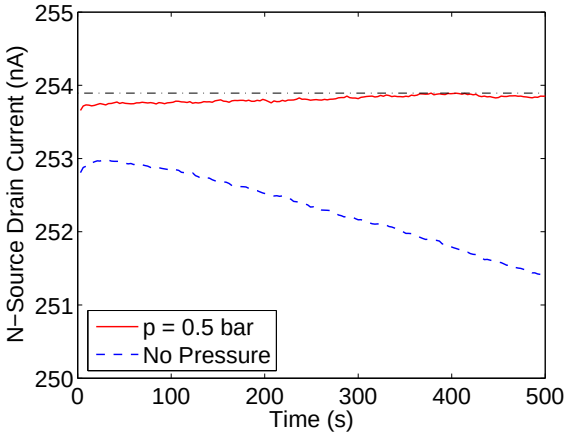


Figure 4.9: N-Source Drain Current Drift with and without applied pressure; the device is located at the center of a 250 x 400 μm^2 membrane and connected to an oscillator; with 0.5 pressure, the current stabilizes after 400 s.

4.3 PMOS-based Transducer's Architectures

Alternatively, P-MOSFETs offer also potentialities as reduced footprint pressure transducers, talking advantage of their high value and opposite in sign piezoresistive coefficients.

4.3.1 Suspended Devices Pair - PMOS-Mirror

A first PMOS-based option is the PMOS current mirror with transistors oriented perpendicularly to each other, as illustrated in Figure 4.12(a). When the transistors are oriented orthogonally, the current mirror ratio changes with the stress. Assuming that the transistors work in saturation, the drain current of the device M1 is provided by the reference current:

$$I_{ref} = \frac{K_1}{2}(V_G - V_{T1})^2 \quad \text{with} \quad K_1 = \frac{\mu_1 C_{ox} W_1}{L_1}, \tag{4.1}$$

where V_{T1} is the threshold voltage of M1, μ_1 is its carrier mobility, C_{ox} is the gate capacitance per unity of area, W_1 and L_1 are the channel width and length, respectively.

The gate voltage and the output current are thus:

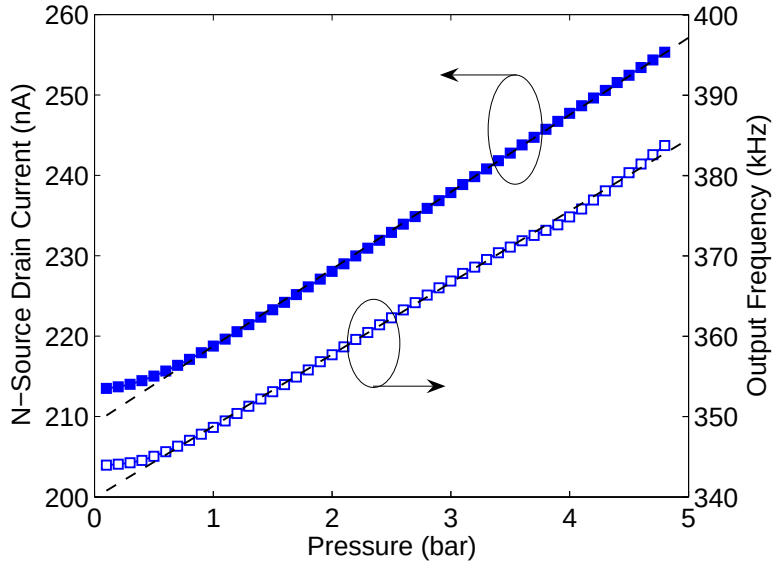


Figure 4.10: N-Source drain current and output frequency as a function of the pressure for a device at the center of a 250 x 400 μm^2 membrane, commanding an out-of-membrane oscillator; no significant drift was observed under pressure.

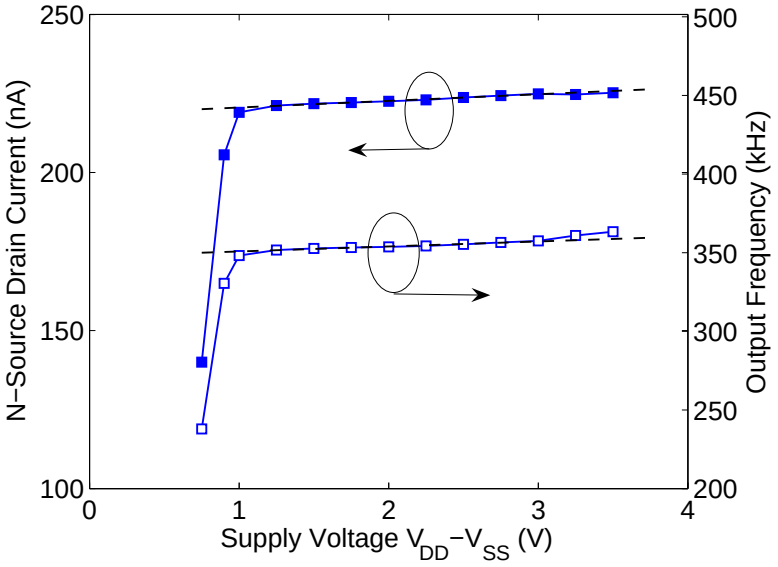


Figure 4.11: N-Source Drain Current and Output Frequency sensitivity to the supply voltage; the device is located at the center of a 250 x 400 μm^2 membrane.

$$V_G = \sqrt{\frac{2I_{ref}}{K_1}} + V_{T1} \quad \text{and} \quad I_{out} = \frac{K_2}{2}\left(\sqrt{\frac{2I_1}{K_1}} - V_{T2} + V_{T1}\right)^2. \tag{4.2}$$

Assuming that the effect of the threshold voltage, the dimensions or the gate oxide changes are much smaller than the change in mobility due to the stress, the variation of the output current, for MOS devices of identical sizes with no mismatches, can be approximated by:

$$\frac{\Delta I_{out}}{I_{ref}} \cong \frac{\Delta\mu_2}{\mu_2} - \frac{\Delta\mu_1}{\mu_1} = \pm\left(\pi_{PMOS,\perp} - \pi_{PMOS,\parallel}\right)\cdot\sigma, \tag{4.3}$$

under uniaxial stress. As the PMOS piezoresistive coefficients are opposite in signs, the output current increases or decreases depending on the orientation and the sign of the stress. Figure 4.12(b) shows the measurements under stress of the mirror structure sketched in Figure 4.12(a), for various current values. The uniaxial tensile stress is applied using a four-point bending setup.

This configuration is not experimented on a membrane but introduces very well the following solution. It is, nevertheless, worth to note that on a membrane, where a biaxial stress is present, the mirror output current (I_{out}) is sensitive to the difference of both components of stress. Such architecture may therefore not be implemented at the center of a square membrane.

4.3.2 Cascaded PMOS-Mirrors

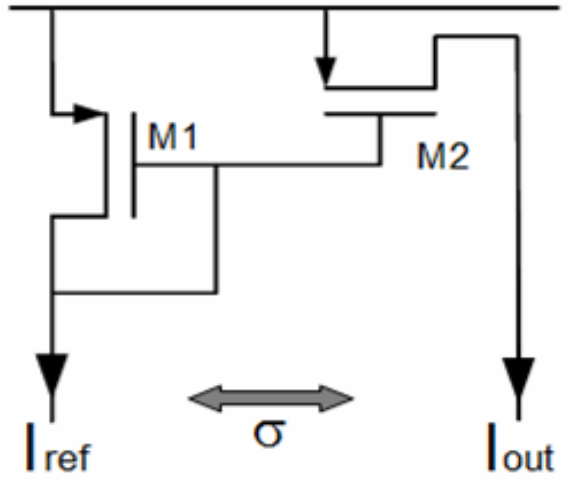
As a second PMOS-based design solution, PMOS mirror cells may be cascaded increasing the sensitivity to the membrane strain induced by a pressure application. Figure 4.13 presents the cascade of two cells and the frequency variation of a current-starved ring oscillator controlled by the resulting output current. The output frequency, varying up to 20%, are obtained under uniaxial stress applied on a four-point bending set-up.

This latter configuration is implemented on a 500 μm-side square membrane, locating the devices at 50 μm from the border in opposite directions, as illustrated in Figures 4.14 and 4.15 respectively for the circuit schematics and the photograph of such system.

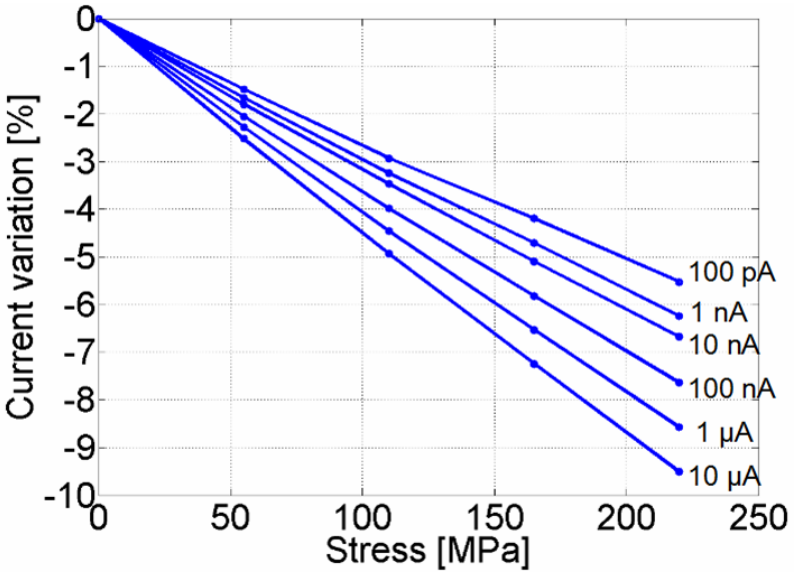
Figure 4.16 gives its output frequency and the corresponding relative frequency variation as a function of the pressure. The mirror devices are oppositely orientated compared to the measurements made under bending, involving a rising output frequency with the pressure. The full-scale frequency variation amounts to an outstanding value of 140.5%, while the output frequency sensitivity is not less outstanding with 46.8%/bar, opening the way for a wide range of applications, including high precision pressure measurements.

The frequency evaluation procedure includes two readouts of the frequency for each pressure step and is described in Figure 4.8. The membrane bursted at 3.1 bar, preventing a second readout of the frequency at the highest pressure value. It is very worth to note that, as illustrated in Figure 4.16, except for few pressure steps, both frequency readouts give very close values, mixing-up both curves in the graph. Hence, it is clear that no drift is biasing the measurement.

No measurement of the current passing through the mirror branches is possible with a complete circuit. The measured complete system consumption, including the 200 pF

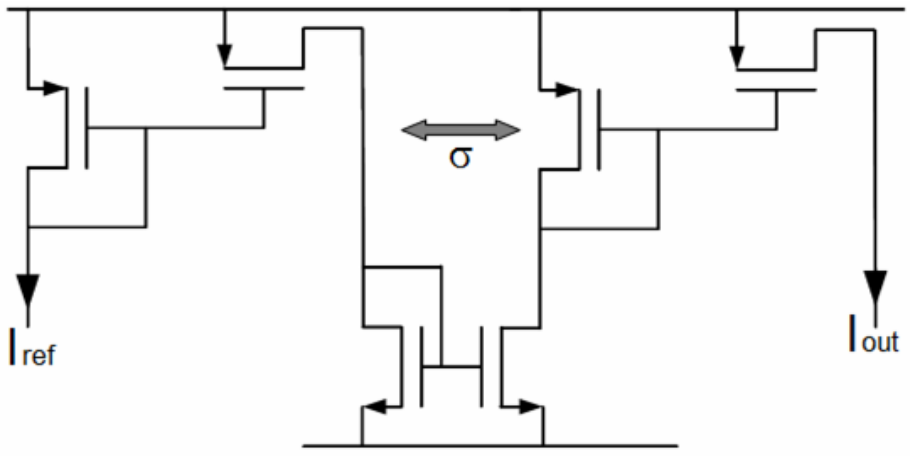


(a)

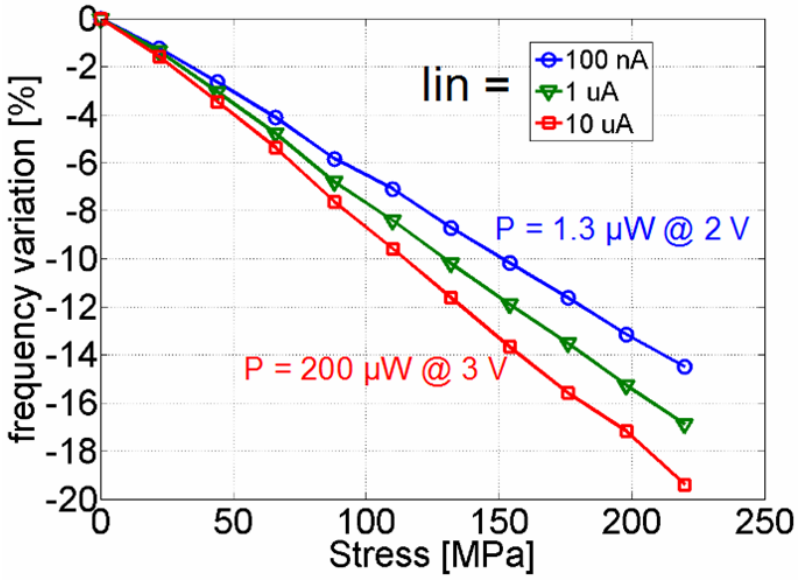


(b)

Figure 4.12: Orthogonal PMOS current mirror (a) schematics, (b) output current variation measurements under tensile stress for different reference currents; Bertrand Rue.



(a)



(b)

Figure 4.13: Two cascaded orthogonal PMOS current mirror: (a) schematics, (b) measurements of the frequency variations of a current-starved ring oscillator controlled by the stress sensitive output current I_{out}, the applied stress is tensile; Bertrand Rue.

loaded output buffers, is around 150 μW. According to ELDO simulations, the sensing part of the system does not consume more than 2-3 μW with a supply voltage (V_{DD}-V_{SS}) of 3 V.

Besides, it can be noted that two current mirrors may be designed in opposite orientations, one case giving a rising frequency shift and the second case having a descending frequency when the pressure increases. Considering the ratio of both signals frequencies would still improve the sensitity and, by the same way, offering a temperature independent output.

Finally, according to Jaeger [83], the cascaded PMOS-mirror configuration has a sensitivity to the strain which can be formulated as follows (the axes are indicated in Figure 4.15):

$$\frac{\Delta I_{out}}{I_{ref}} \cong 2 \cdot \left(\pi_{PMOS,\parallel} - \pi_{PMOS,\perp}\right) \cdot (\sigma_{xx} - \sigma_{yy}) \tag{4.4}$$

Considering that for this architecture the current variation $\Delta I_{out}/I_{ref}$ is directly proportional to the output frequency variation, a 140% current variation combined with the π coefficients given in Table 2.1 lead to an estimated $(\sigma_{xx} - \sigma_{yy})$ of 1.4 GPa. In order to very roughly evaluate both strain components, we make use of the relation $\sigma_{yy} = \nu_{Si} \cdot \sigma_{xx}$ which is formally correct only at the border (Appendix A) and the present devices are 50 μm away from the border on a 500 mum-side square membrane. This approximation gives 1.94 GPa and 0.54 GPa respectively for σ_{xx} and σ_{yy}.

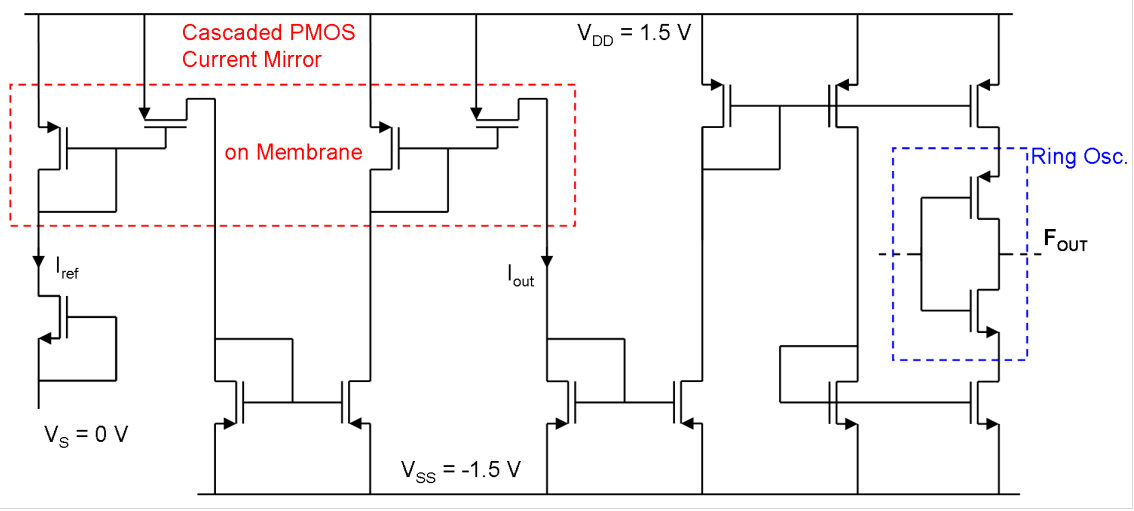


Figure 4.14: Smart pressure sensor schematics of a cascaded PMOS mirror suspended pressure transducer, commanding an out-of-membrane oscillator (Circuit design: Bertrand Rue).

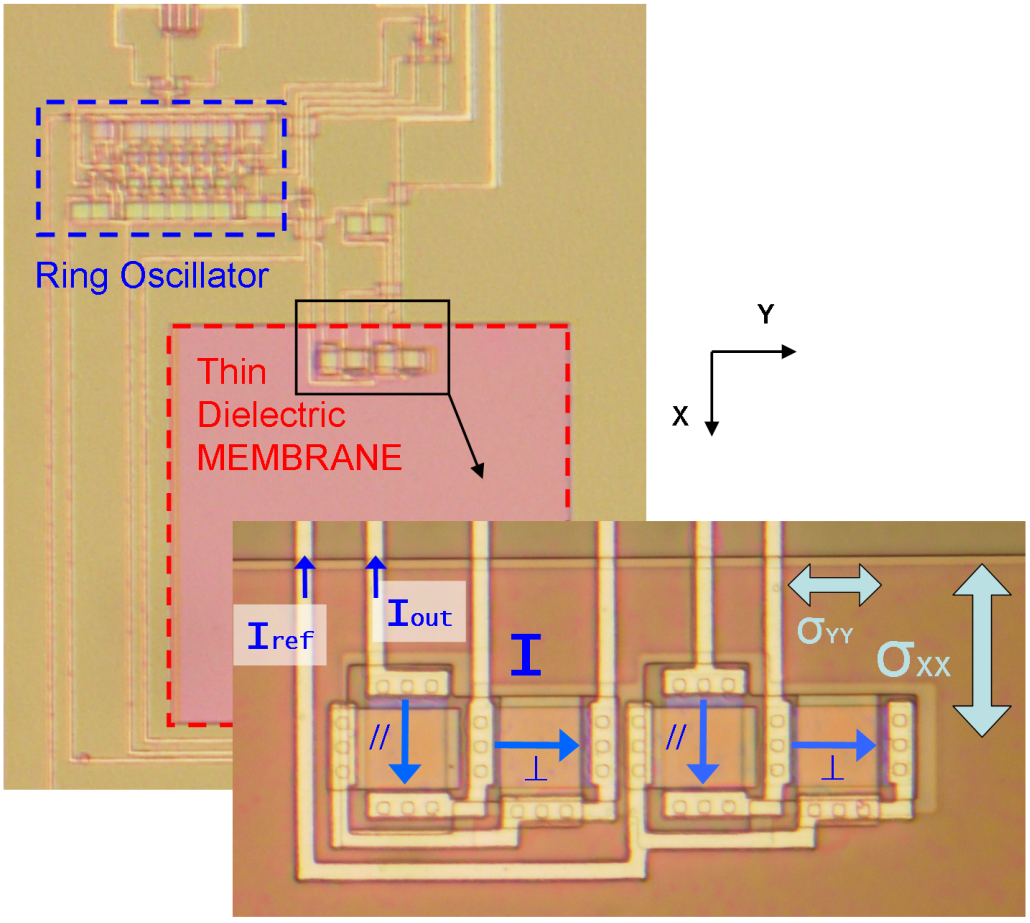


Figure 4.15: Photograph of a cascaded PMOS mirror-based smart pressure sensor, implemented on a 500 μm-side square membrane; the transducer devices are located at 50 μm from the border; the main component of stress is perpendicular to the membrane border; the devices current orientations are related to this main component of stress (Figure 1).

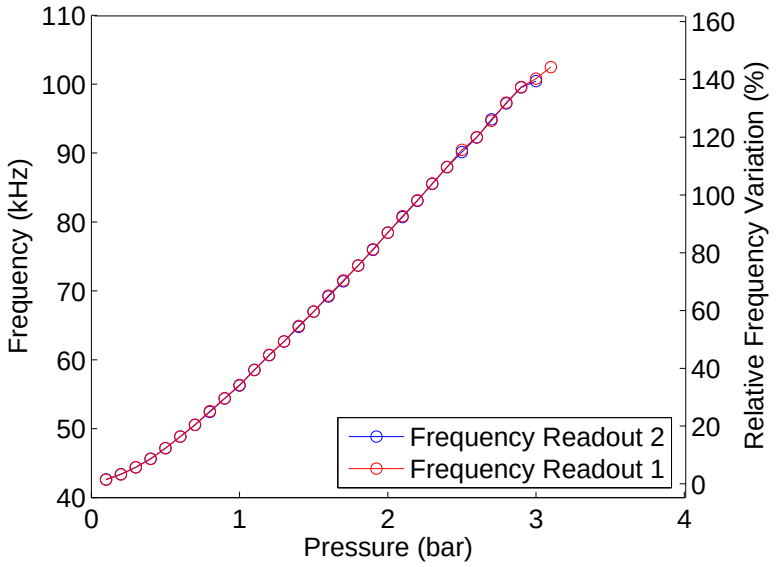


Figure 4.16: Ouput frequency and corresponding relative frequency variation as a function of the applied pressure for a cascaded PMOS mirror-based smart pressure sensor, implemented on a 500 μm-side square membrane; the transducer devices are located at 50 μm from the border.

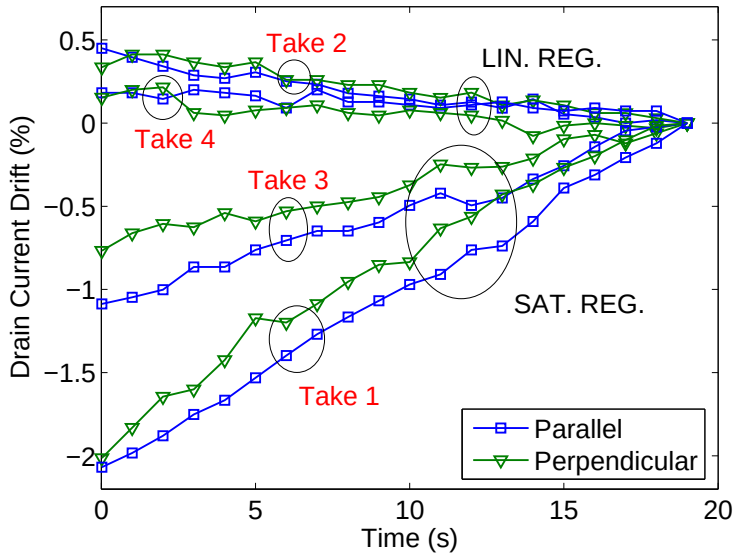
4.4 Drift Effect on Very Thin Dielectric Membranes

The drift phenomenon, observed during electrical characterization under pressure, is particularly embarrassing for the applicability of such systems as pressure sensors as well the potential use of thin dielectric membranes as a characterization platform for devices under very high stress. Therefore, complementary experiments are conducted.

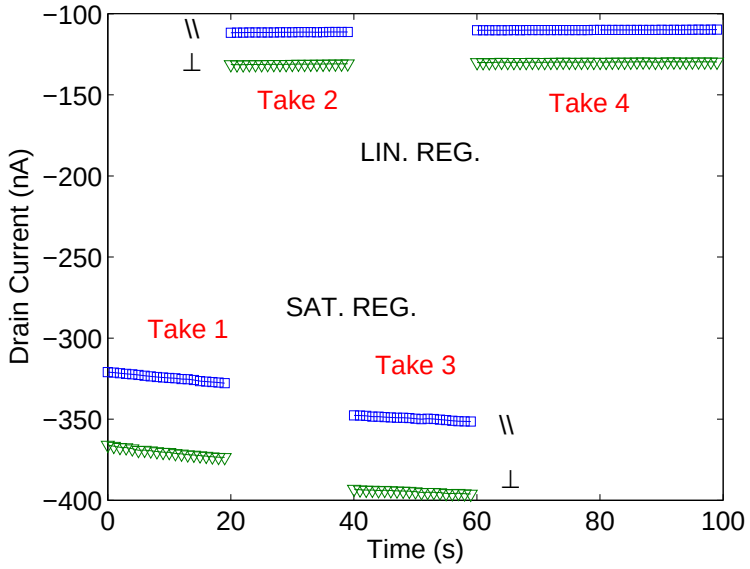
4.4.1 Influence of Bias Conditions

First, PMOS devices parallel and perpendicular to the border of a 340 μm-side thin dielectric membrane are measured with respect to the time in both linear and saturated regimes. These measurements are compared in Figure 4.17. For a better readability among the different measured cases the last current point is considered as the reference and the drift is expressed in percentage regarding to this last value in Figure 4.17(a). Two main observations may be set forth:

1. The history plays a role. Indeed, in linear regime, as well as in saturation regime, the last take of measurement as decreased slope (from Take 1 to Take 3 and from Take 2 to Take 4 in the Figure). This history effect evokes then a charging effect.
2. The operating regime or V_{DS} do play also a role, changing importantly the dynamics of this charging effect and also it sign.



(a)

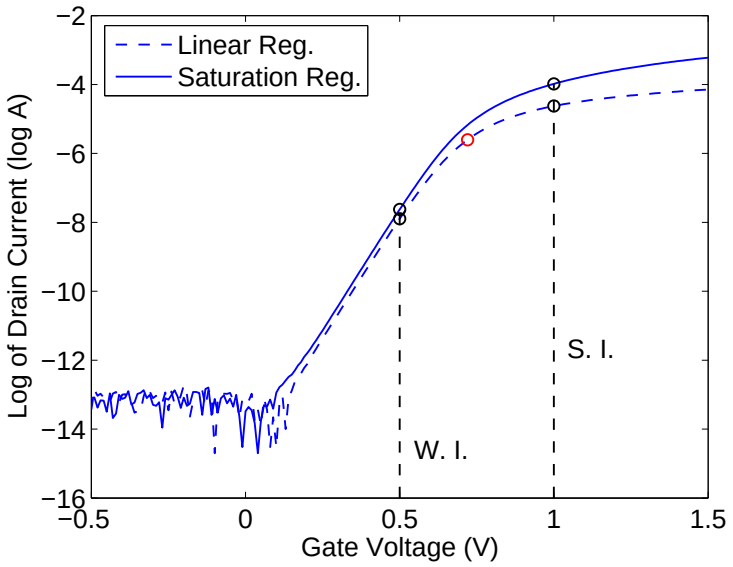


(b)

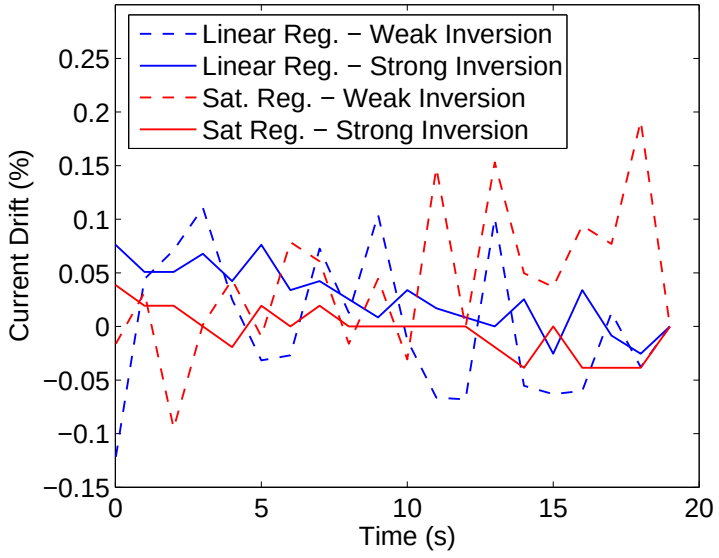
Figure 4.17: Drain current drift study on PMOS devices L = 3 μm, W = 3 μm parallel and perpendicular to the border of a 340 μm-side thin dielectric membrane: (a) drain current drift as a function of the time, taking the last measured point as the drift reference, each configuration is sampled twice, V_G = -0.4 V, V_{Th} = -0.27 V, in linear regime V_{DS} = 50 mV, in saturation regime V_{DS} = -1.5 V, (b) corresponding drain current absolute values with respect to the time chronology.

4.4.2 Influence of Back Potential

The removal of the silicon substrate during the membrane release suppresses, by the way, the control on the back gate potential of the integrated devices. It is then figured out that this open access to the back side of the membrane may alter the electrical characteristics of the suspended devices. To verify that hypothesis, an aluminum layer is conformally deposited on the back side of a functionalized membrane and the corresponding current drift is measured. Figure 4.18 reports these results with a back-gate voltage of 0 V. No significant drift is observed in this configuration, evidencing the role of the back gate potential.



(a)



(b)

Figure 4.18: Electrical characteristics of an edgeless NMOS device $L = 2$ μm, $W = 72$ μm on a thin 240 μm-side membrane with an additional 1 μm-thick Al layer on its back side: (a) I_D-V_G curve showing the four bias points where the current is sampled, in linear regime $V_{DS} = 50$ mV, in saturation regime $V_{DS} = 1.5$ V, (b) drain current drift in the four bias conditions; $V_{BG} = 0$ V.

4.5 Conclusions

In this chapter innovative designs were experimented. These designs reflected the will of reducing the transducers footprint on the thin membranes, in order to assure a good mechanical robustness.

Three main architectures were fully experimentally demonstrated with a reporting of their output frequency as a function of the pressure and a burst pressure estimation. Their performances are summarized in Table 4.2. The power consumption of the sensing stages of the circuits was measured or simulated, according to the cases, at a level as low as 2-3 μW.

Configuration	Sensitivity (%/bar)*	FS Variation (%)*	Measured range		Burst Pres. (bar)
			Min (bar)	Max (bar)	
Intrinsic N-Source Mb: 600 x 600 μm^2 60 μm from border	1.98	2.57	0.1	1.4	1.4
Intrinsic N-Source Mb: 250 x 400 μm^2 at the center	2.47	11.63	0.1	4.8	$\geq$ 4.8
Casc. PMOS Mirror Mb: 500 x 500 μm^2 50 μm from border	46.83	140.48	0.1	3.1	3.1

Table 4.2: Summary of the performances of the fabricated pressure sensing systems; *on the measured range.

Two architectures are particularly convincing in terms of robustness and sensitivity, opening largely a way towards pressure sensing applications. The first architecture is a NMOS-based with a single suspended device acting as a current source which controls a current-starved ring oscillator. This structure is further studied in Chapter 5 to attempt to relate the electrical performances with mechanical strain in the membrane. The second architecture is based on a cascaded PMOS mirror. Its location is kept quite close to a membrane border in order to feature an asymmetric stress to the transducers. An alternative way to bring devices in asymmetrically stressed areas could consist in implementing them at the center of a rectangular membrane. Simulations made on thin dielectric blanket membranes do show an interesting evolution of the strain components difference as soon as the ratio Length/width worths 2 (Figure 4.19).

A newly observed drift issue was addressed in this chapter, showing that the back gate potential is a critical parameter for ensuring the electrical stability of suspended devices. The application of a pressure appeared to play also a role, involving a drift amplitude reduction. It is believed that the nitrogen flowing from the pressure nozzle may keep away external charges that could affect the electrical behavior of the devices.

In practice, a classical metal layer may probably not be used, due to high strain values at the bottom fiber of the membranes. Nevertheless, there exist alternatives. The first consists

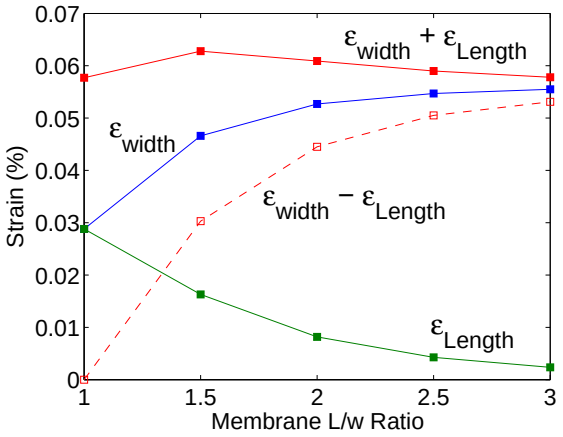


Figure 4.19: Simulated strain components at the center of a 4-layers thin membrane, with their corresponding sum and difference, as a function of the membrane Length/width ratio; z-level = 0.4 μm; p = 1 bar; the width is 200 μm; for details concerning the membrane layers see Chapter 3.

in the back-side deposition of a mineral conductive layer. A doped amorphous silicon deposited at low or even room temperature in a PECVD chamber could be convenient. Such material is documented by Oxford Instrument [7]. Secondly, one can think about starting with a special substrate including a buried conductive layer in a SOI stack. Third, the back gate control can be assured by suspending double gate transistors on thin dielectric membrane. In that latter configuration, all the tools are available as an original SOI double-gate devices process is experimentally demonstrated in Chapter 9. Finally, looking at pressure sensing applications, absolute pressure sensors have a vacuum sealed cavity, preventing any potential approach of external charges.

Chapter 5

Single MOSFET suspended on Rectangular Membrane - A case study for Coupled Electro-Mechanical Characterization

5.1 Introduction

As a functional pressure sensor, a single NMOSFET suspended on membrane architecture, commanding an out-of-membrane oscillator, was presented and validated in Chapter 4. This design integrates the main design rules issued from the concept developed in the first part of the thesis which are (i) the pressure transducer area has to be minimized and (ii) being positioned at the center of the membrane. Its performances were demonstrated with an increase of the N-source current of 20% and the output frequency rises of 12% when the pressure is varied from 0.1 bar to 4.8 bar.

Beyond the operating character of this system, setting up the relationship of its electrical performances with internal mechanical stresses appears to be of prime interest.

Firstly, for nourishing a material science point of view. Applying a mechanical stress on electronic devices arises the curiosity of many research groups [19, 105, 139, 159, 158] and companies [24, 115, 140, 172], mainly towards a performances boost but also for a better understanding of electron transport in strained semiconductors. In that context, reaching very high levels of stress is particularly requested and, therefore, the stress values applied to the present suspended device has to be quantified.

Secondly, from the application point of view, developing a numerical model able to describe accurately the mechanical and, incidentally, electrical behaviors of a transistor implemented on a very thin dielectric membrane is also highly desirable for the designer. In that frame, confronting electrical measurements and mechanical simulated data through the piezoresistive theory reveals being a severe prism in a numerical models validation process. Developing these points is the objective of the present chapter.

5.2 System Description

The transducer system is graphically described in Figure 5.1 and is composed of a single transistor implemented at the center of a rectangular membrane. This membrane has 250 x 400 μm^2 lateral dimensions. The device is 6 μm-width and 120 μm-length. Acting as an intrinsic current-source, this transistor has its large length tailored in order to limit the power consumption which is typically in the order of 230 nA. In addition, its Early voltage is also improved by the same way, stabilizing the current value. For giving a rather compact shape to such long device, the conductive channel is divided in four segments of 30 μm-length each. These segments are orientated so that the drain current is parallel to the supposed main component of stress, i.e. along the width axis (σ_{yy}). Indeed, this configuration optimizes the sensitivity as $\pi_{NMOS,\parallel} \geq \pi_{NMOS,\perp}$. A second reason for orientating the channel segments along the Y-axis is that the mechanical strength is intuitively enhanced when placing patterned fins parallel to the supposed main component of stress. In practice, this structure appears indeed to be very robust, withstanding pressures over 4.8 bars which is the highest value reachable by the pressure testing set-up. Being one of the most successfully completed designs of this work, it is also one of the most interesting structures to be analyzed further numerically.

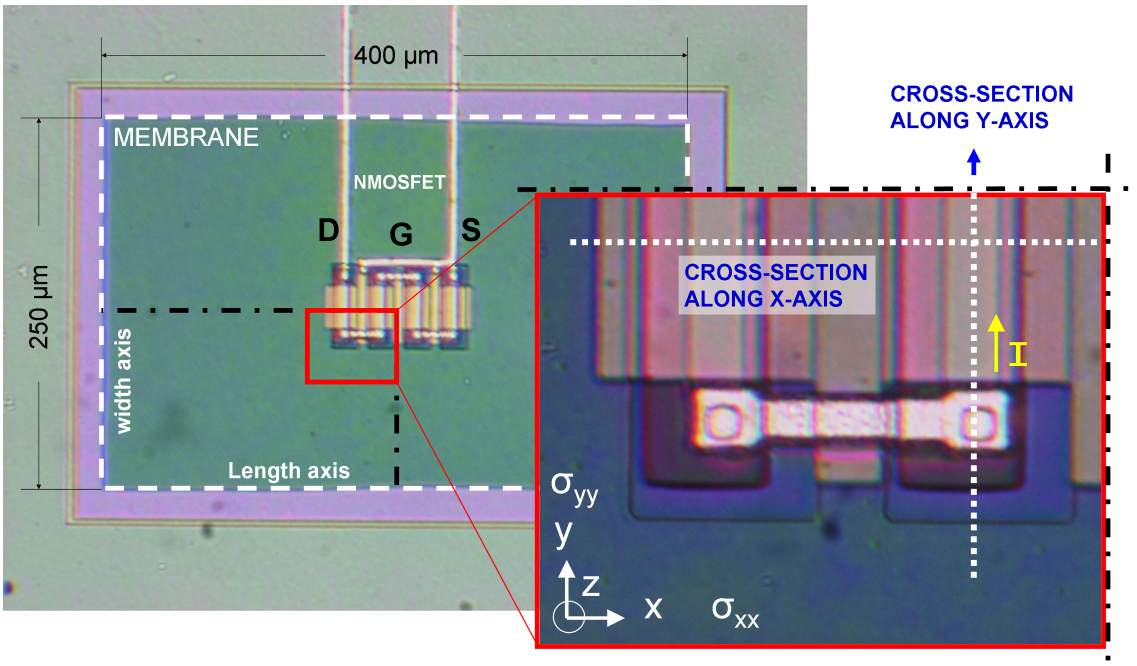


Figure 5.1: Detailed top view of single NMOSFET pressure sensor architecture. In numerical models, only the quart of the membrane indicated by the symmetry axes is considered; focusing on the device area, two cross-sections are extracted and reported in Figures 5.6 and 5.7

5.3 Methodology

The methodology is based on the bridge equation linking electrical measurements and mechanical simulations. Several numerical models implemented in Comsol are presented and confronted.

5.3.1 A Bridge Equation

The relationship between the mechanical stress and the relative drain current variation which can be generally expressed as [83]:

$$\frac{\Delta I_D}{I_{D_0}} = -\boldsymbol{\pi} \cdot \boldsymbol{\sigma}, \tag{5.1}$$

where $\Delta I_D/I_{D_0} = (I_D - I_{D_0})/I_{D_0}$ is the relative current variation, $\boldsymbol{\pi}$ a piezoresistive coefficients vector and $\boldsymbol{\sigma}$ the stress vector in the conductive channel of silicon. The relative current variation is directly measured; the stress is delivered by finite elements analysis. On the basis of this equation, we set forth the three possible axes of view, each reflecting a same reality:

1. Estimating piezoresistive coefficients from the measured current variations and simulated stresses; the values obtained are to be compared with the ones obtained under four-point bending set-up;

2. Computing the current variation from simulated stress and piezoresistive coefficients, to be compared to measured electrical currents;

3. Calculating local stress from measured coefficients and measured current variations and compare it with stress computed by FEM analysis.

Equation (5.1) underlies on three basis elements that are introduced here after.

5.3.2 Electrical Measurements

Being the first element, Figure 5.2 illustrates the drain current variation for an independent NMOS device as well as for a second item which is connected to an associated out-of-membrane oscillator. The devices are operated over the threshold voltage, in saturation regime. In the three measured cases, the current response is linear with the pressure except for values below 0.5 bar. As the following developments are based on, the reliability and reproducibility characters of the drain current variation have to be highlighted. It is all the more remarkable that the current levels differ among the measurements, ranging from 215 nA for the oscillator-connected device up to 5 μA for the independent device biased at $V_G = 1.25$ V.

In Chapter 4 extensive electrical characterization of the concerned device is presented for different points of bias (Figure 4.6). It is there proved that, while keeping a good sensitivity to the pressure, applying a gate voltage under the threshold voltage induces a drastic linearity loss of the current variation.

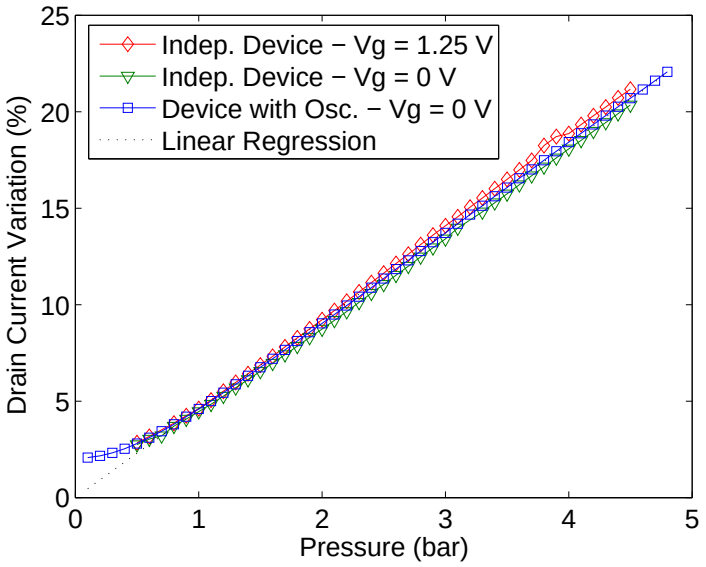


Figure 5.2: Drain current variation of intrinsic NMOSFETs located at the center of a 250 x 400 μm^2 rectangular membrane, as a function of the pressure; when biased at V_{DS} = 1.5 V and V_G = 1.25 V, the independent device has $V_{Goverdrive}$ = 1.45 V and $I_D \approx 5$ μA under a low pressure; when biased at V_G = 0 V, it corresponds to $V_{Goverdrive}$ = 0.35 V and $I_D \approx 250$ nA under a low pressure. The device connected to the ring oscillator has $I_D \approx 215$ nA at low pressure.

The pressure applied is comprised between 0.1 and 4.8 bar. One can note that the zero pressure point was not measured because of the possible current instability when stopping the nitrogen flow of the pressure nozzle. The drift effect on the drain current of transistors on very thin dielectric membranes is addressed in Section 4.4.

The relative current variation calculation supposes the use of a reference current, i.e. I_{D_0} in Equation (5.1). A choice on this value has to be made. Indeed, in Equation (5.1) the left member of the equation is relative to I_{D_0}, while its right member deals with the absolute value of stress. The output of the simulations is the absolute value of the stress, but we have no knowledge about the current corresponding to zero σ. The current response being very linear, the reference is taken as the linear regression value at zero pressure. Nevertheless, this choice does not condition the validity of the results discussion.

Being a perfect clone of the two first devices, a third device is under study. An intrinsic PMOSFET is implemented on a membrane with the same design. As illustrated in Figure 5.3, its current response with the pressure has a low amplitude (max. -2.5% at 3 bar) and is bell-shaped. The reference current to calculate the relative variation is extrapolated at null pressure.

5.3.3 Piezoresistive Coefficients

The second element is the knowledge of the piezoresistive coefficients. Equation (5.1) may be re-written more precisely as follows:

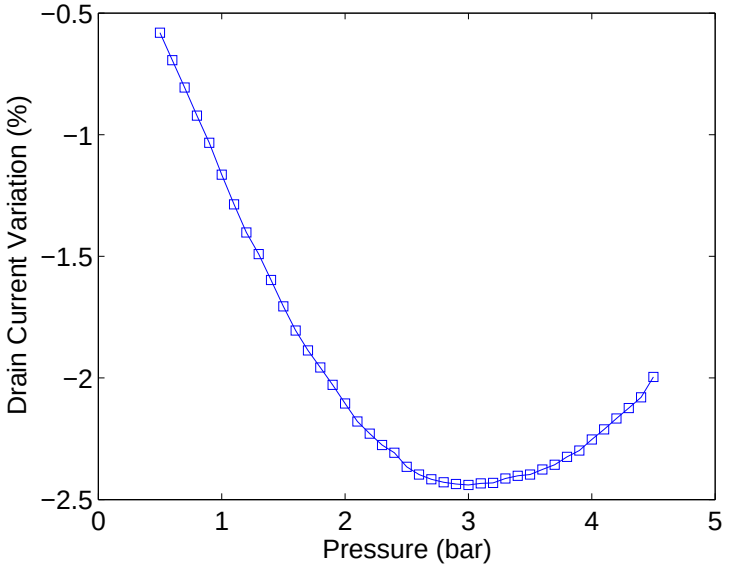


Figure 5.3: Drain current variation of an intrinsic PMOSFET located at the center of a 250 x 400 μm^2 rectangular membrane as a function of the pressure, V_{DS} = -1.5 V; V_G = -2.475 V which corresponds to $V_{Goverdrive}$ = 1.3 V and $I_D \approx 1$ μA.

$$\frac{\Delta I_D}{I_{D_0}} = -\pi_{MOS,\parallel} \cdot \sigma_{\parallel} - \pi_{MOS,\perp} \cdot \sigma_{\perp}, \tag{5.2}$$

where $\pi_{MOS,\parallel}$ and $\pi_{MOS,\perp}$ are respectively the piezoresistive coefficients for MOS devices along parallel and perpendicular directions with respect to the current direction. $\sigma_{\parallel}$ and $\sigma_{\perp}$ are the corresponding stress component. As a side note, one can notice that in the [110] directions on a (100) wafer, the frame of this work, the current is not sensitive to the shear stress [83].

π coefficients are channel doping type dependent. They are also technology dependent, as illustrated by the variety of values reported in the literature. Representative values are given in Table 5.1. A specific knowledge of the piezoresistive coefficients relative to the technology under study is then essential. The scatter among π coefficients reported by the various authors is commented in Appendix C.

Figure 5.4 illustrates the linear dependence between the stress and the current for the present UCL technology. The methodology employed for the UCL technology π extraction is described in Appendix B. In short, a linear regression is performed and its slope gives the coefficients values, expressed here in %/100 MPa. In these measurements, the stress is applied uniaxially on a four-point bending set-up. Extracting systematically these coefficients for all applied gate voltage values brings into light their respective dependencies with the bias conditions, for both N- and P-channel types as well as both parallel and perpendicular orientations. In Table 5.2, this dependency is completely described for devices in saturation regime, which is usually the case when devices are biased in operational circuits. Relating the piezoresistive coefficients as a function of the gate overdrive

Source	Technology	$\pi_{NMOS,\parallel}$	$\pi_{NMOS,\perp}$	$\pi_{PMOS,\parallel}$	$\pi_{PMOS,\perp}$
Smith [147]	Bulk Si	-3.10	-1.74	+7.19	-6.62
Thompson [159]	MOS	-3.55	-1.45	+7.17	-3.38
Bradley [27]	MOS IBM	-4.50	-3.50	+5.00	-4.50
	MOS TI	-3.20	-2.50	+4.15	-3.85
	MOS Lucent	-5.00	-3.50	+6.00	-4.00
Chang [33]	SOI MOS	-4.78	-3.01	+7.69	-5.63
Gallon [62]	SOI MOS	-4.97	-2.30	+6.48	-4.66
UCL	*SOI MOS*	*-1.97*	*-1.23*	*+2.58*	*-2.43*

Table 5.1: Piezoresistive coefficients reported in the literature for lightly doped bulk and SOI MOS technologies (1∼10 μm); units are %/100 MPa.

(V_{GO}), this figure of merit is rendered more generally interpretable. On the right side axes, the linear regression residues[1] are reported, giving information on the linear character of the measurements. One can formulate the following observations. When biased over the threshold, the N-MOSFETs exhibit a slight dependency with V_{GO} for both stress orientations, progressing of 10% when V_{GO} rises from 0 to 1.5 V. The P-MOSFETs have different behaviours according to the stress orientation. $\pi_{PMOS,\perp}$ is very steady beyond V_{GO} = 0.8 V, while $\pi_{PMOS,\parallel}$ ramps slightly and continuously down with V_{GO}, varying of 20% when V_{GO} rises from 0 to 1.5 V. Under the threshold voltage, the linear relation between the stress and the current is lost. This non-linear character is confirmed by sub-threshold measurements of devices on membrane under pressure, in Section 4.2.2.

These piezoresistive coefficients are extracted from lightly doped devices. As shown in Figure 5.5, light doping levels of the conductive channels have no significant influence on the value of the piezoresistive coefficients. Channels are boron doped approximately with 7×10^{16}/cm^2 for the N-MOSFETs and 4×10^{16}/cm^2 for the P-MOSFET concentrations. As a comparison, source and drain regions are doped with 5×10^{20}/cm^3 volume doses of boron (p-type) and arsenic (n-type), where the coefficients are highly reduced as well as their temperature dependency.

5.3.4 Numerical Models

Extensive simulations of multilayered membranes are presented in Chapter 3, including the effect of patterning. In this chapter, it is intended to go further in the stress quantification, trying to make echo to electrical measurements by interpreting data through the piezoresistive theory. The structure to be simulated is too complex to be fully introduced in a tri-dimensional (3D) model and solved with finite elements analysis (FEA). Indeed, there is a multi-layered membrane which is patterned by the integration of a MOS device. From the top view of the system given in Figure 5.1, two cross-sections are extracted focusing on the device area and describing the structure of the actual system (Figures 5.6 and 5.7). Therefore, three computing routes of gradual complexity are set up and compared.

[1] $R(V_G) = \left[\sum_{i=1}^{n} \left\{ \left(I_D(V_G, \sigma_i) - I_D(V_G, \sigma_0) \right) / I_D(V_G, \sigma_0) - \pi(V_G)\sigma_i \right\}^2 \right]^{1/2}$

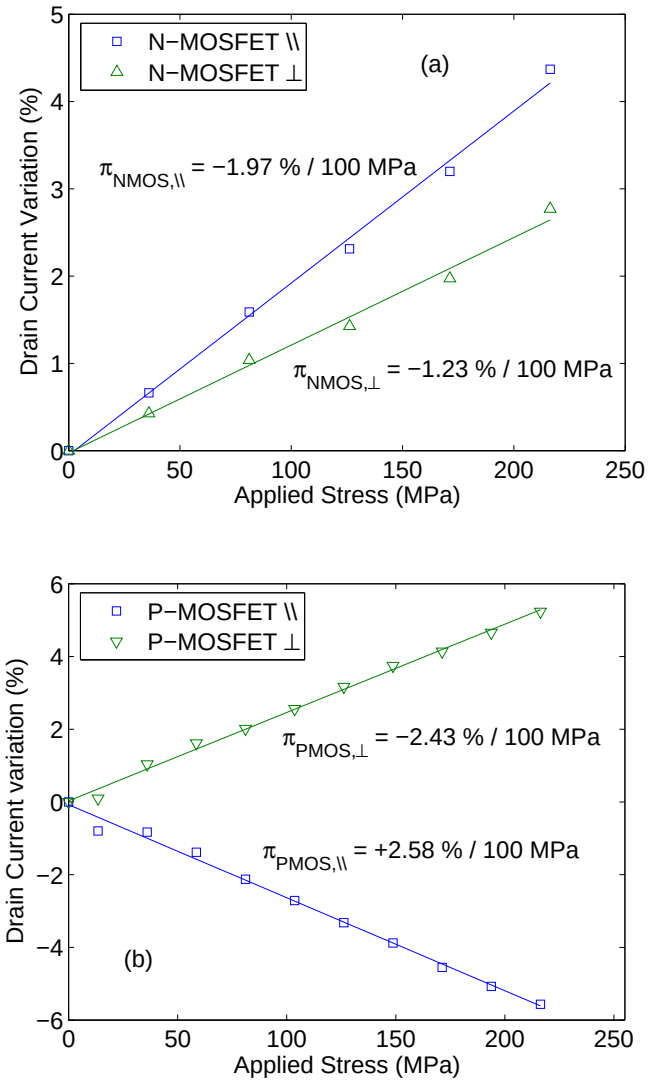


Figure 5.4: π piezoresistive coefficients extraction for (a) N-MOSFET and (b) P-MOSFET from four-point bending set-up measurements; the device dimensions are 20 x 20 μm^2; the transistors are biased in saturation regime ($V_{DS} = V_G = \pm 2V$, giving respectively $V_{GO,NMOS} = 1.5$ V and $V_{GO,PMOS} = 1.35$ V). Redrawed from Rue [142]

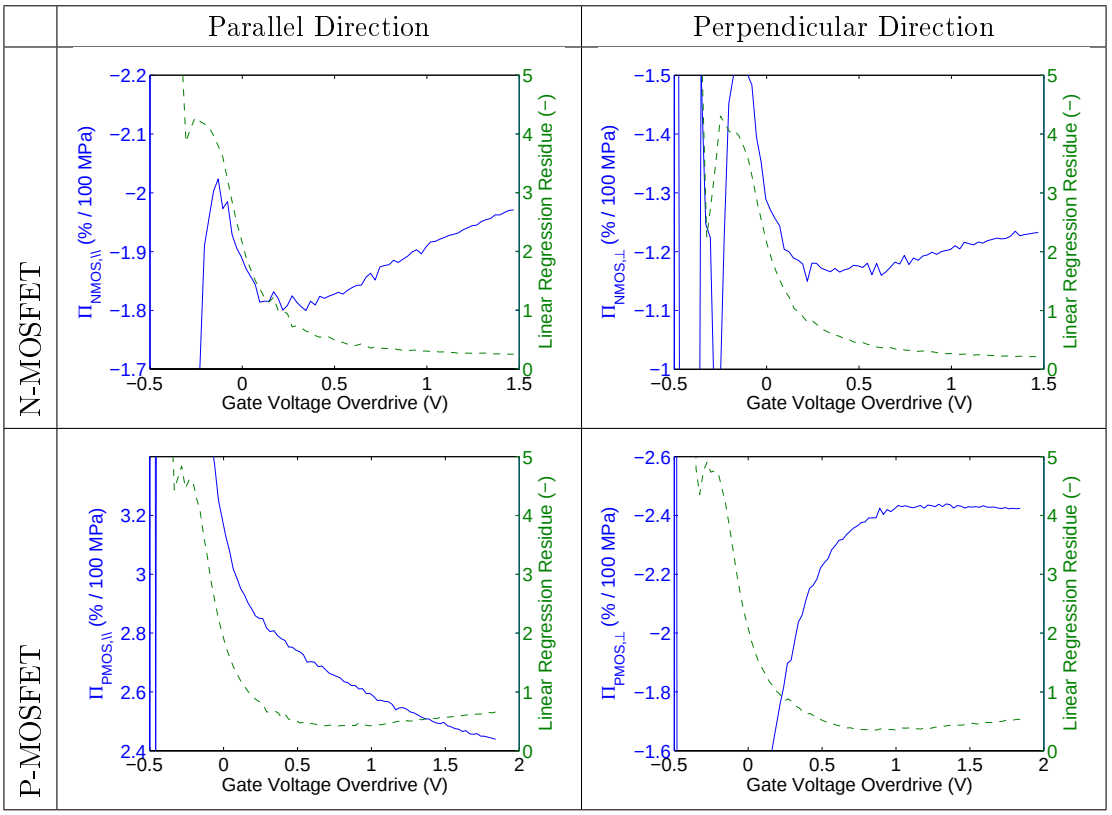


Table 5.2: Systematically extracted piezoresistive coefficients as a function of the gate voltage overdrive ($V_{GO} = |V_G - V_{Th}|$), $V_{DS} = \pm 2V$, for both current-stress orientations and both devices types.

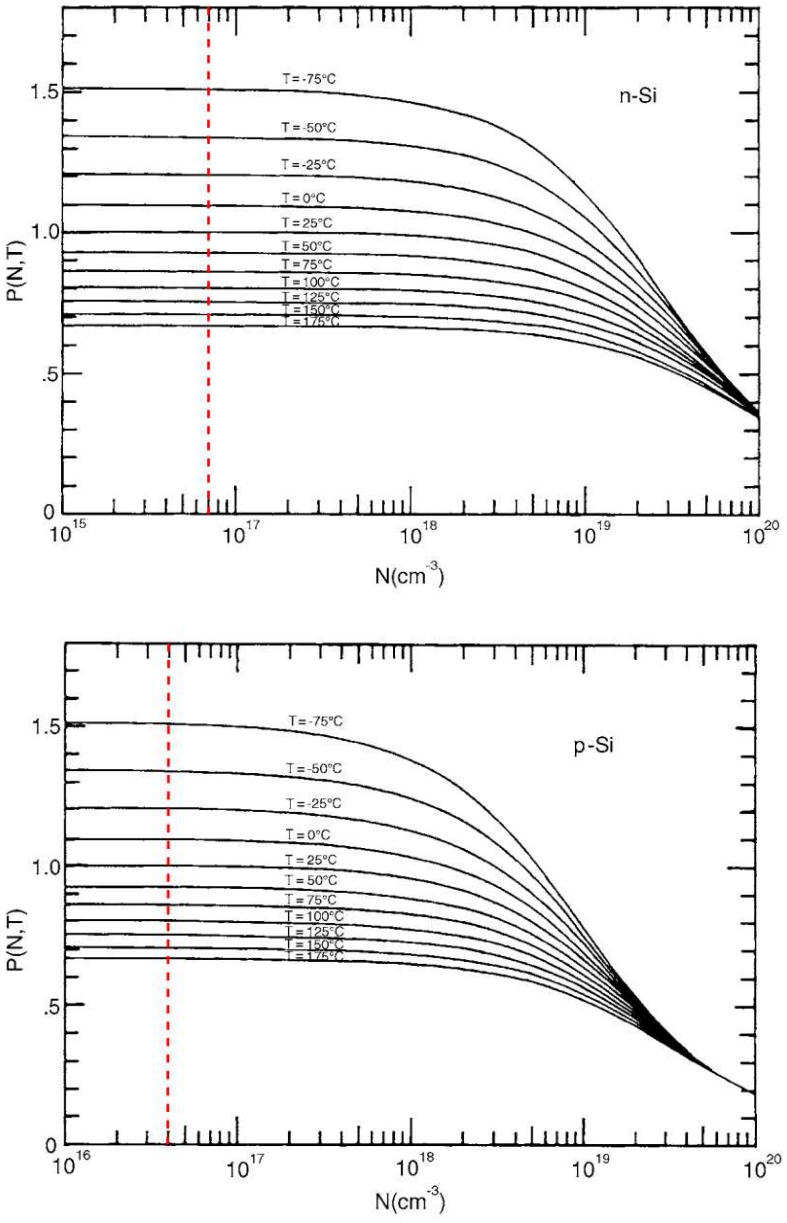


Figure 5.5: Variation of piezoresistive coefficients for (a) n-type and (b) p-type Si as a function of doping level and temperature. Reproduced from Kanda [87]. Typical channel doping levels are marked with dashed lines.

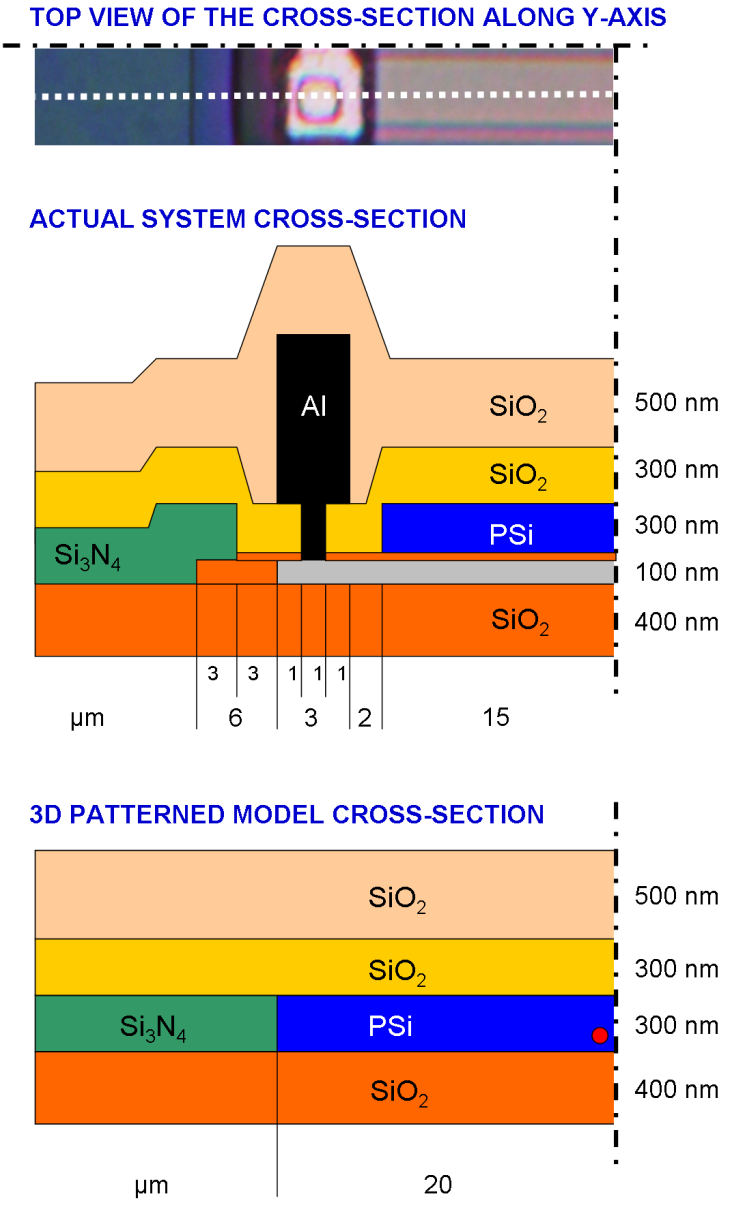


Figure 5.6: Sketch focused on the device area, comparing the structure of the actual system and the 3D patterned membrane model (model3), along the Y-axis as defined in Figure 5.1.

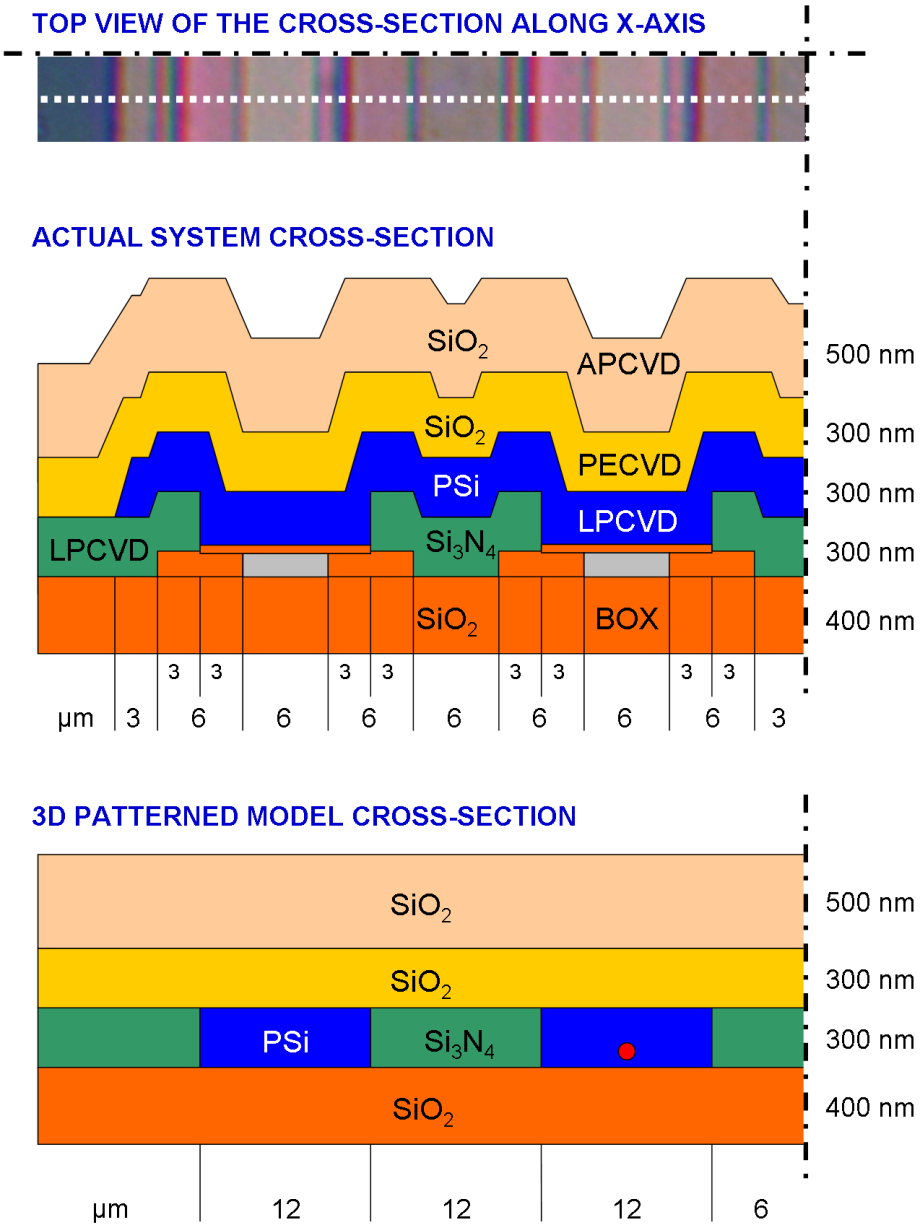


Figure 5.7: Sketch focused on the device area, comparing the structure of the actual system and the 3D patterned membrane model (model3), along the X-axis as defined in Figure 5.1.

5.3.4.1 3D Model of Blanket Membrane

The first computing route starts from the observations issued from Chapter 3 stating that two regions can be distinguished in membranes mechanical behaviour. These are (i) the borders area, extending up to around 30 μm from the edges, exhibiting a high strain gradient hugely dependent on the fibre level, and (ii) the central region where there are low vertical and horizontal stress gradients. In addition, thanks to the low complexity of a blanket membrane model, it is possible to attribute most computing resources to regions where the strain gradient is the highest i.e. at the anchors, by applying a very high mesh density at these areas. This constitutes a first reference model.

5.3.4.2 Additional Correction with 2D Model

The devices on membranes are singularities inserted in a planar continuous multi-layered film. They present a complex design with short-range lateral patterning and local films stack modifications with respect to the rest of the membrane areas. Looking at the cross-section figures (5.6 and 5.7), the Si_3N_4 film is interrupted while the thin silicon film is added along with the gate oxide and the polysilicon gate. In addition, metal lines are present for electrical contacts at the devices fins extremities. The metal layer is much thicker compared with the rest: 1 μm-thick for the aluminum film with respect to 300-500 nm for Si_3N_4, PSi and SiO_2 films and 100 nm for the Si film.

It is then advantageous to implement complementary 2D models along the X- and Y-axis directions, as defined in Figure 5.1, that include all these local topological changes with a high fidelity.

The methodology is graphically illustrated in Figure 5.8. At the center of the membrane the efforts are mainly aligned with the membrane plane. It is then possible to establish a bijective conversion function between the strain in the homogeneous part of the membrane (i.e. the output of the 3D blanket membrane model, $\varepsilon_{Si_3N_4}$) and its value at the center of the semi-conducting silicon film (ε_{Si}). In that way, Figures 5.9 and 5.10 illustrate simulation results of these complete 2D profiles, respectively along the X- and Y-axis directions, when a lateral stretching is applied to them. The displacements of 20 μm and 10 μm in the respective directions induce strain values close to what is obtained at the maximum studied pressure of 4.8 bar. Figures 5.11 and 5.12 present the same respective results but do integrate initial stresses in all films in the calculation. The model based on 3D blanket membrane completed by 2D detailed profiles corrections is the second model.

The 2D conversion functions are plotted in Table 5.3 for profiles along the X- and Y-axis, including or not initial stresses. The configuration that do not take into account initial stresses reveals mainly the strain conversion relationship of the materials stack with their respective Young's Moduli.

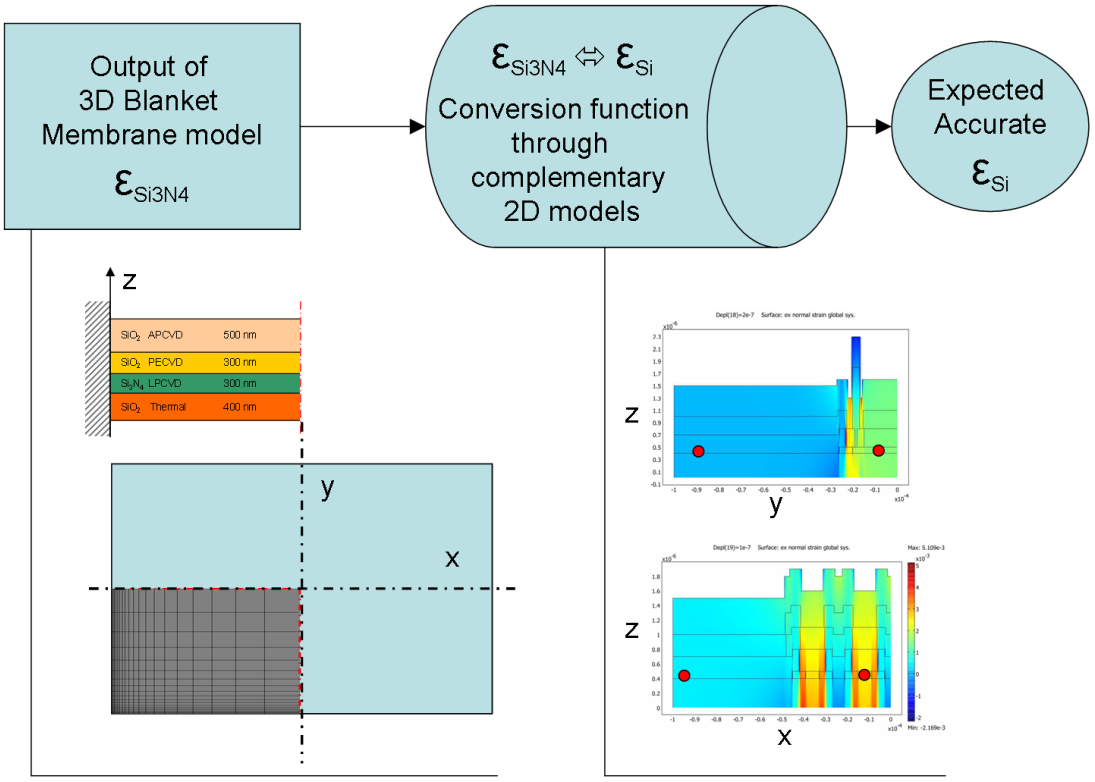


Figure 5.8: Graphical description of the methodology implemented under the naming "Additional Correction with 2D Model".

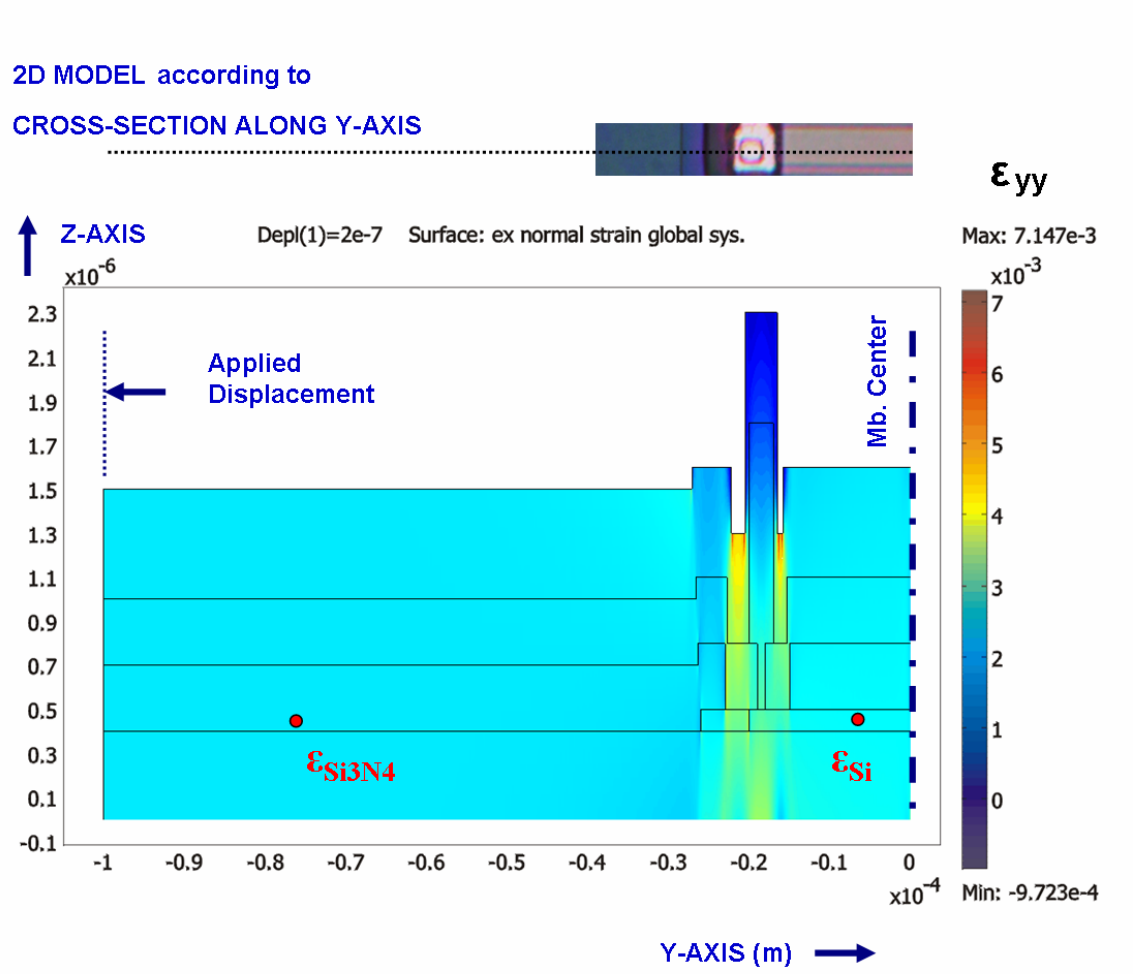


Figure 5.9: 2D model, drawn in Comsol, with all layers and corresponding patterning present on the membrane at the device area; this profile is oriented *along the Y-axis*, as defined in Figure 5.1; a perfect clamping is applied at $y = 0$ (central symmetry axis of the membrane) while a displacement of -0.2 μm is applied at $y = -100$ μm, *no starting internal stresses are considered.*

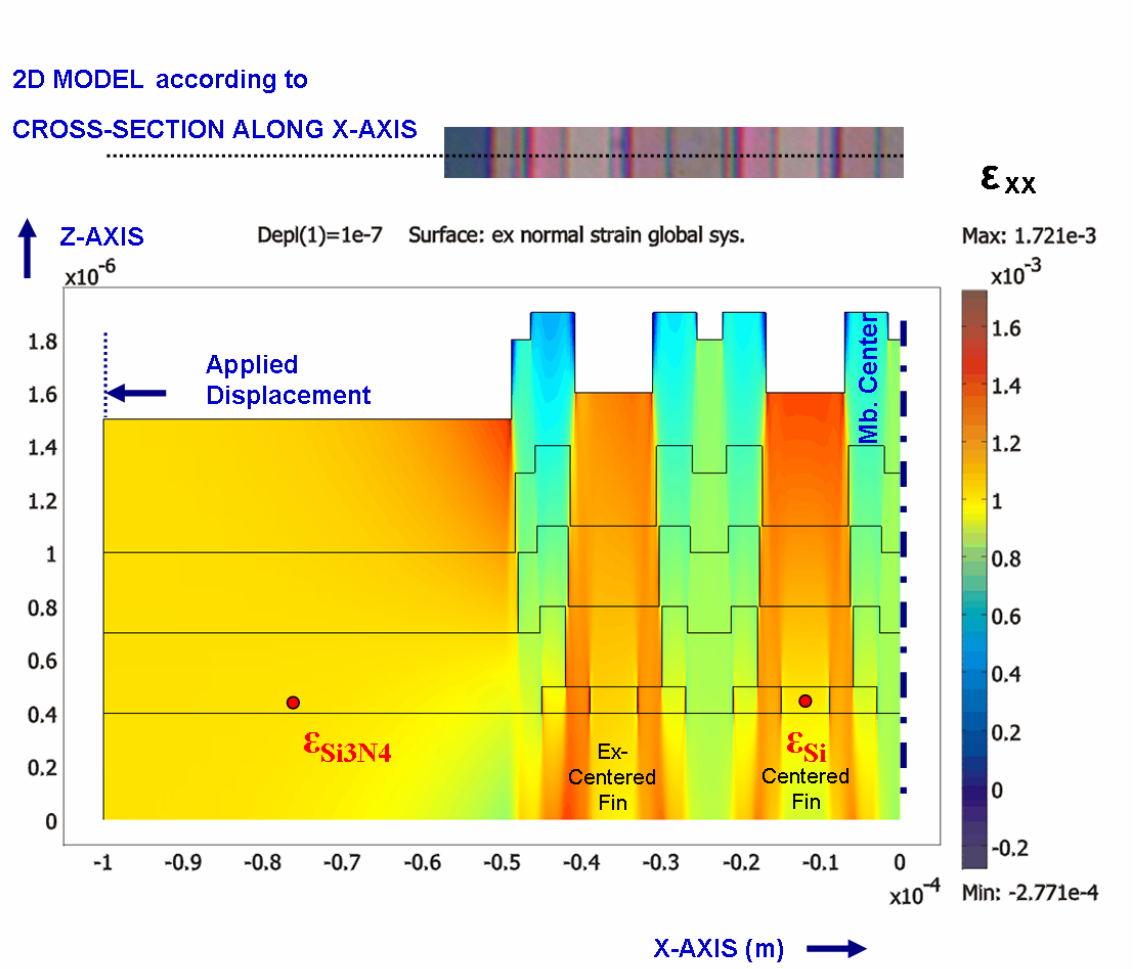


Figure 5.10: 2D model, drawn in Comsol, with all layers and corresponding patterning present on the membrane at the device area; this profile is oriented *along the X-axis*, as defined in Figure 5.1; a perfect clamping is applied at $x = 0$ (central symmetry axis of the membrane) while a displacement of -0.1 μm is applied at $x = -100$ μm, *no starting internal stresses are considered.*

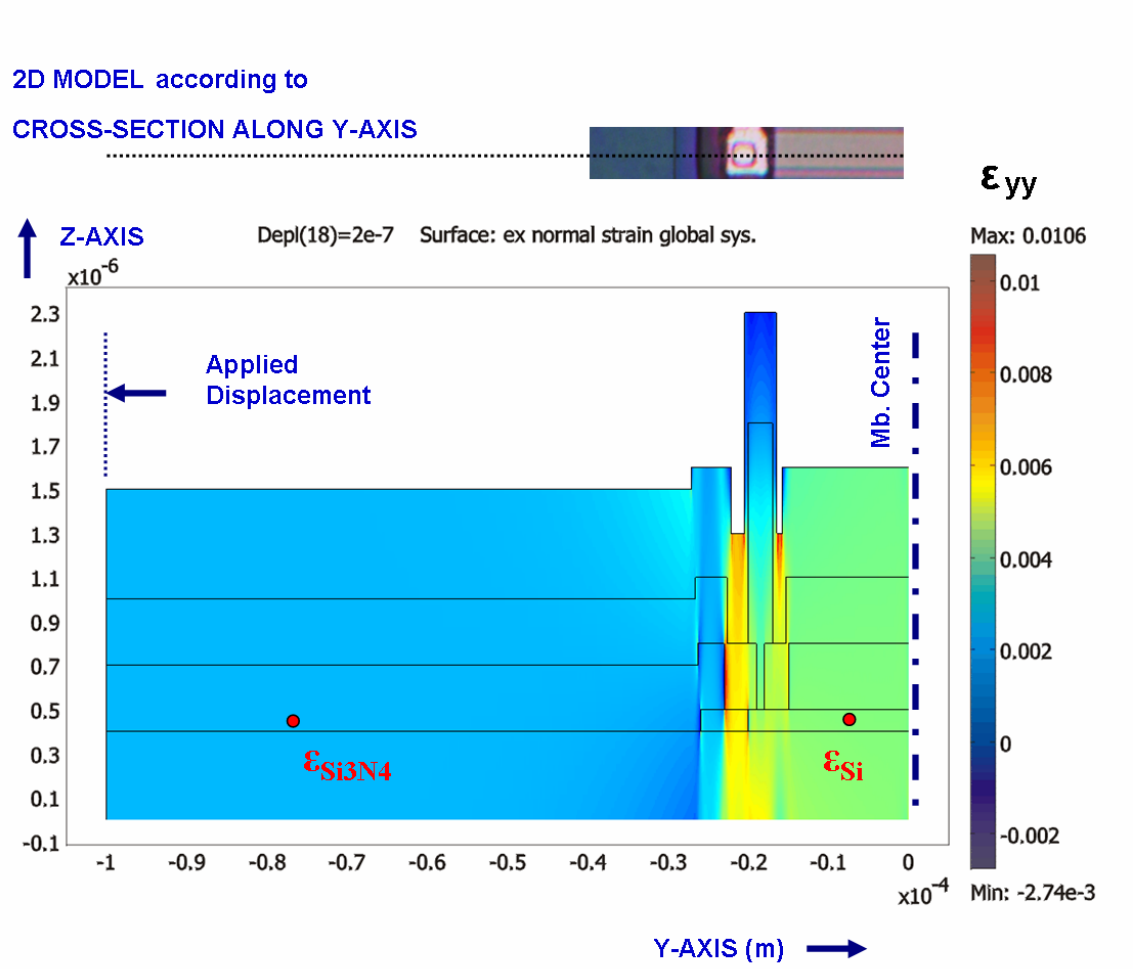


Figure 5.11: 2D model, drawn in Comsol, with all layers and corresponding patterning present on the membrane at the device area; this profile is oriented *along the Y-axis*, as defined in Figure 5.1; a perfect clamping is applied at $y = 0$ (central symmetry axis of the membrane) while a displacement of -0.2 μm is applied at $y = -100$ μm, *material thermal stresses are taken into account.*

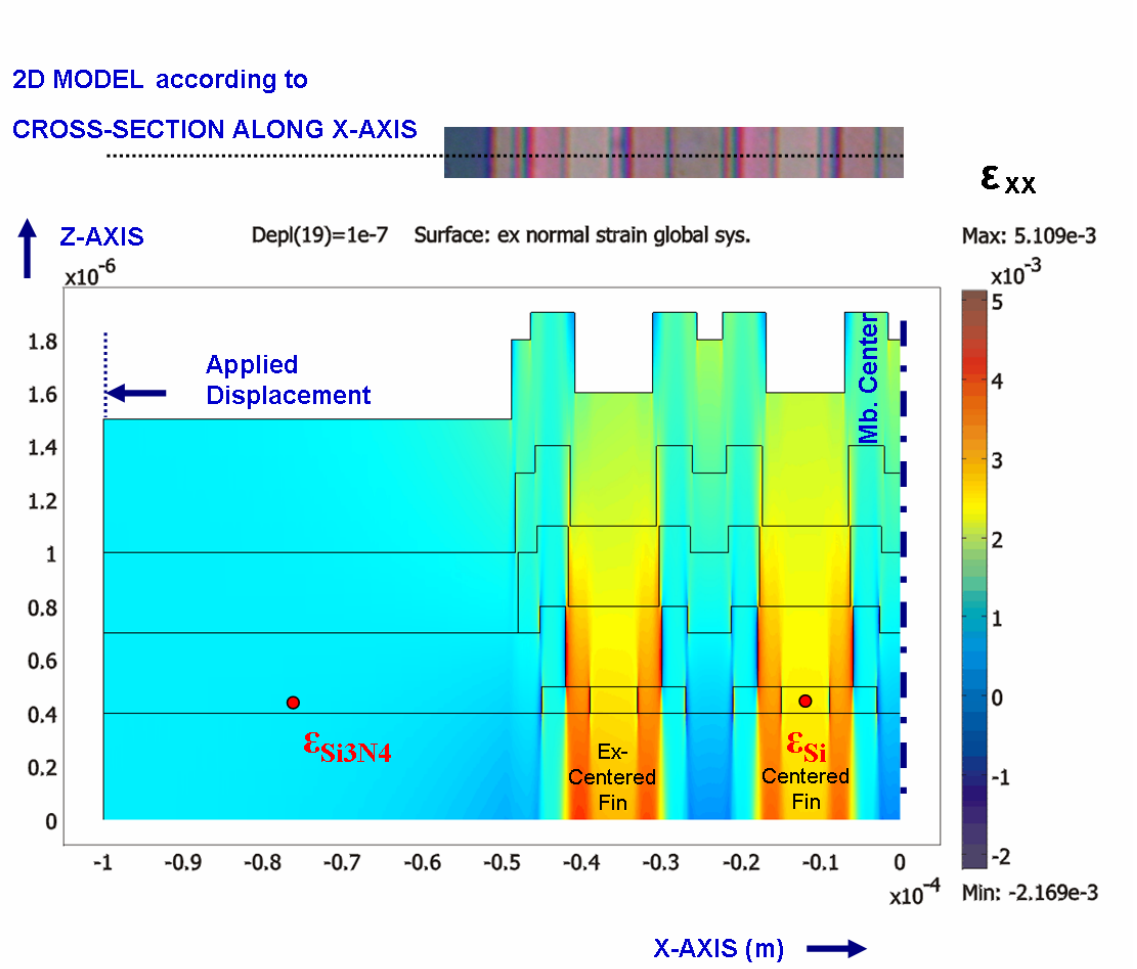


Figure 5.12: 2D model, drawn in Comsol, with all layers and corresponding patterning present on the membrane at the device area; this profile is oriented *along the X-axis*, as defined in Figure 5.1; a perfect clamping is applied at $x = 0$ (central symmetry axis of the membrane) while a displacement of -0.1 μm is applied at $x = -100$ μm, *material thermal stresses are taken into account.*

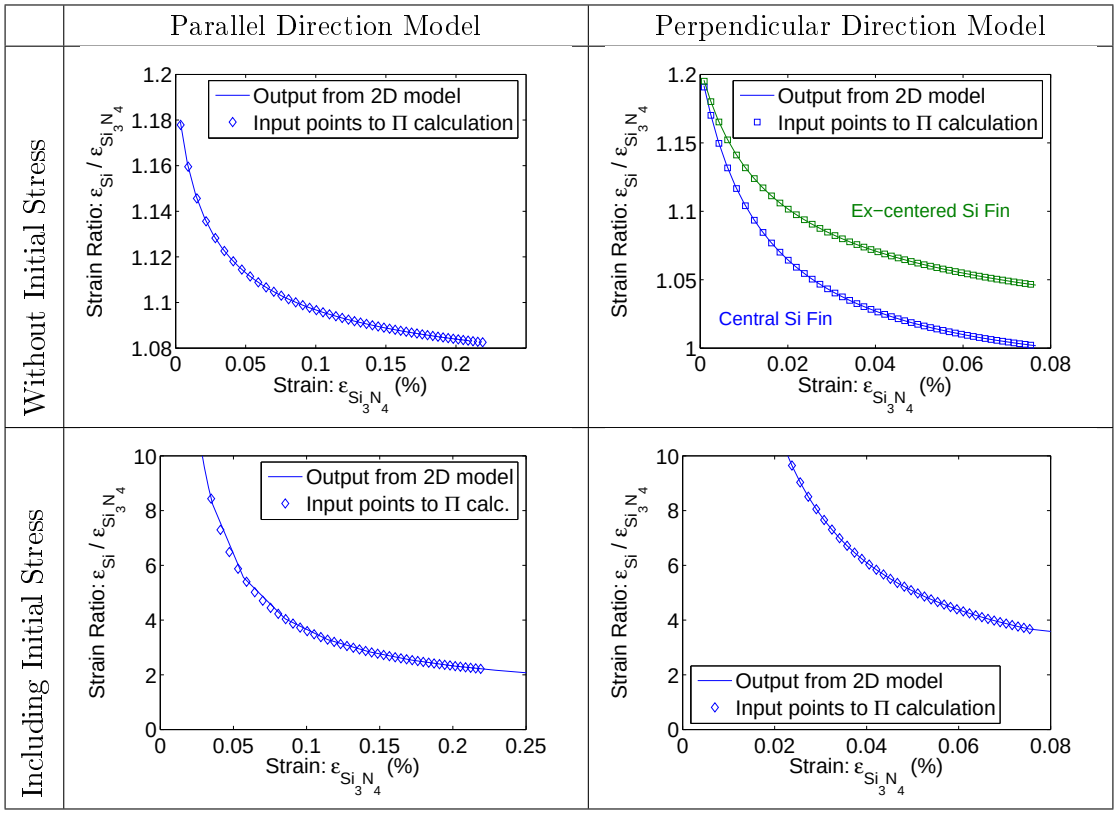


Table 5.3: Graphs illustrating the correction functions applied on the 3D blanket membrane model, by the mean of the 2D models; ε_{Si} and $\varepsilon_{Si_3N_4}$ are identified in Figures 5.9, 5.10, 5.11 and 5.12; the references about π coefficients calculation do refer to subsequent Section 5.4.2.

5.3.4.3 3D Model of Patterned Membrane

As an alternative to the two first routes for computing most precisely the strain present in the transistors channel, a 3D model including device patterning is implemented. This model is nevertheless a simplified implementation of the system. Figures 5.6 and 5.7 put in exact correspondence the actual devices structure with the present 3D model. One can mention the three main following points:

1. As it is capped by polysilicon with close Young modulus and significantly higher thickness, the Si channel is considered to be one of the lowest fibers of the polysilicon film;
2. In the parallel direction, the lateral limit of the polysilicon are extended to the limits of the silicon channel;
3. In the perpendicular direction, the polysilicon gate capping of the nitride is neglected; the PSi remains inserted into nitride gaps, planarizing the model.

Besides, it is particularly worth to note that initial stresses may be taken into account also at the locally patterned regions and even if the resulting stress of the stacked films is compressive. The necessary conditions to get convergence during the system resolution are (i) starting the solving process with the highest pressure value where all films are tensile before decreasing the pressure set-point step-by-step and (ii) the compressive zone must not be placed near a clamped zone. These conditions can be fulfilled in the present case. This constitutes the third model under study.

5.4 Results

All models are solved with the material constants given in Table 5.4. The question of the choice of material constants is addressed in Chapter 3. These models are first compared through the following figures of merit: membrane deflection, strain progression with the pressure and fiber level scan of the strain components. The three axes of the piezoresistive equation are then analyzed. Each of them gives an original point of view on the measurements and simulations combination. All of these are established for the NMOS and the PMOS devices.

Material	Stress (MPa)	Young's Mod. (GPa)	Poisson Ratio
SiO_2 (Thermal)	-225	50	0.17
Si_3N_4 LPCVD	770	210	0.23
SiO_2 PECVD	-172	17	0.25
SiO_2 APCVD	0	45	0.17
Si (Crystal)	0	170	0.28
PSi LPCVD	-223	160	0.22
Al	0	70	0.35

Table 5.4: Summary of the material constants implemented in all Comsol simulations.

5.4.1 Figures of Merit

Figures of merit are a first element of comparison among the different elaborated models.

5.4.1.1 Membrane Deflection

The membrane deflection is the most immediate mean for comparing models as a direct measurement with white light interferometer may serve as reference. Being 3D models, the blanket and patterned membrane models yield deflection curves as a function of the applied pressure which are illustrated in Figure 5.13. The measured curve is embraced between both simulated curves. The computed curves are distant of the measured one of less than 1 μm. One can mention that the patterned membrane model issues a larger deflection

than which of blanket membrane. This may be due to the compressive character of the patterned zones.

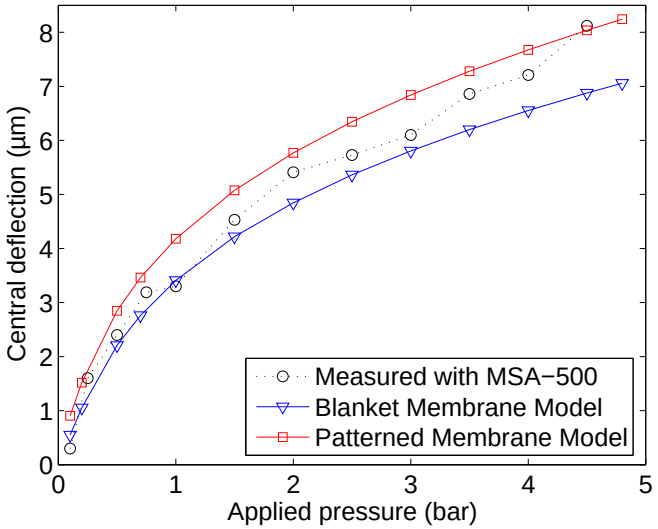


Figure 5.13: Deflection curves of a functionalized 250x400 μm^2 membrane; measured and simulated curves are compared.

5.4.1.2 Strain vs. Pressure

The pressure-strain curve permits to compare with more details the considered models. The data are extracted at the central point of the device channel segment, identified ε_{Si} in Figure. The fiber level is z=0.41 μm.

From Figure 5.14, one may formulate the following observations. Most of the curves have similar slopes, they differ mainly by vertical offsets. The 3D patterned model (model3) and the 2D corrected model (model2) that include initial stresses give higher strains in all cases. The 2D correction without considering the initial stresses appears to be almost without effect.

5.4.1.3 Strain vs. Fiber-Level

Due to its very small volume, the semiconducting Si channel is explicitly implemented only the 2D models. Indeed, in other cases (i.e. models 1 and 3), the strain values are extracted at its approximated location in the stack: its X-Y coordinates and z=0.41 μm. This corresponds in the blanket membrane model to the nitride layer, as it was illustrated in Figure 3.7. In the case of the patterned model, it corresponds to the polysilicon volume, as indicated by a red point in Figures 5.6 and 5.7. Therefore, plotting the strain components (ε_{xx} and ε_{yy}) at the lateral X-Y coordinates of the fin for various Z-levels gives a clear overview of the vertical strain gradient. This is illustrated in Figure 5.15 for both 3D models, i.e. blanket and patterned membrane models.

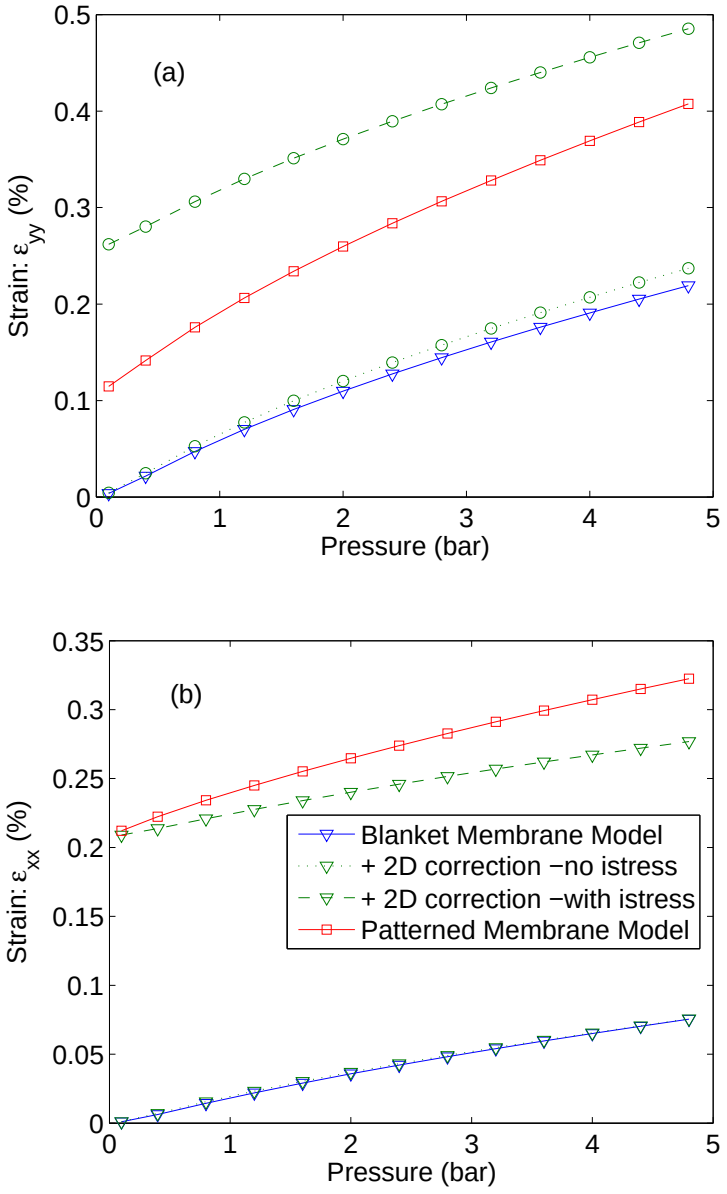


Figure 5.14: Strain as a function of the pressure, for all simulated models, at the central point of the device conductive channel ($z = 0.41$ μm) along (a) the Y- and (b) the X-axis of the membrane, respectively the parallel and perpendicular directions of the current, as defined in Figure 5.1.

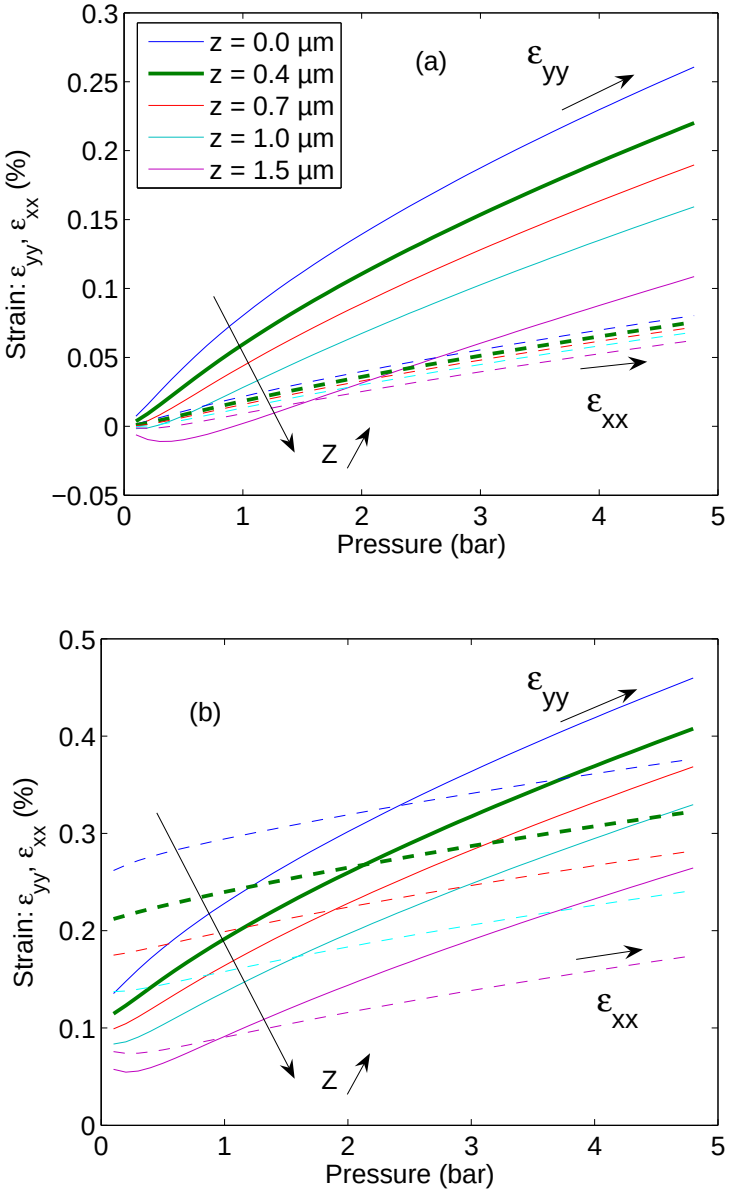


Figure 5.15: Fiber level scan of simulated strain components (ε_{yy} and ε_{xx}), as defined in Figure 5.1) for (a) Blanket and (b) Patterned Membrane Models.

5.4.2 First Axis: $\Delta I_D/I_{D_0}$, $\sigma \rightarrow \pi$

Electrical current variation as a function of the pressure is the most immediate available data. In the same way, the direct output of the simulation tool is the strain. It is then natural to combine them, expecting getting a steady piezoresistive coefficient as the result. This combination can be expressed as:

$$\pi_{MOS,\parallel} = -\frac{\Delta I_D}{I_{D_0}} \cdot \frac{1}{\sigma_\parallel + \alpha\sigma_\perp},$$

where $\alpha = \pi_{MOS,\parallel}/\pi_{MOS,\perp}$. For the NMOS, the calculated α value from extracted UCL π coefficients is 0.62, coinciding with the literature values mean (Table 5.1). For the PMOS, the ratio α issued from the literature has more variation ranging from 1.1 to 2.1. According to our measurements, it equals to 1.06. The results of these combinations are plotted in Figures 5.16 and 5.17.

For NMOS, with the identical negative signs of π_{NMOS} coefficients, the output curves translate the accuracy on the weighted sum of the stress components. The slopes are similar for all models. The blanket membrane and the 2D corrected without initial stress models give closer value to the expected coefficient at lower pressure while the patterned membrane and the 2D corrected with initial stress models are in the opposite situation.

For PMOS, with similar value and opposite sign of π_{PMOS} coefficients, the calculated curves express in some way the accuracy on the stress components difference. The patterned membrane model is particularly out of the scope because both components of stress cross their values, giving a mathematical pole. Besides, the blanket membrane and the 2D corrected without initial stress models give fair π approximation and almost steady value.

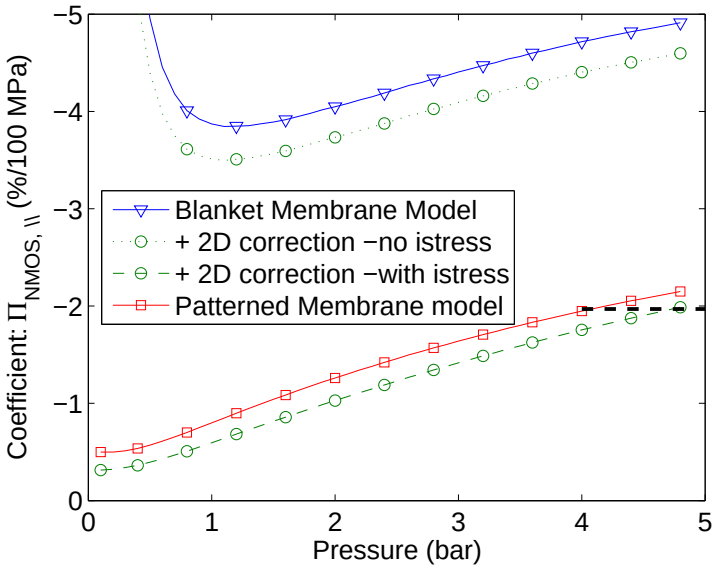


Figure 5.16: Piezoresistive coefficient $\Pi_{NMOS,\parallel}$ calculation as a function of the pressure from electrical measurements and simulated stresses, for various simulation models.

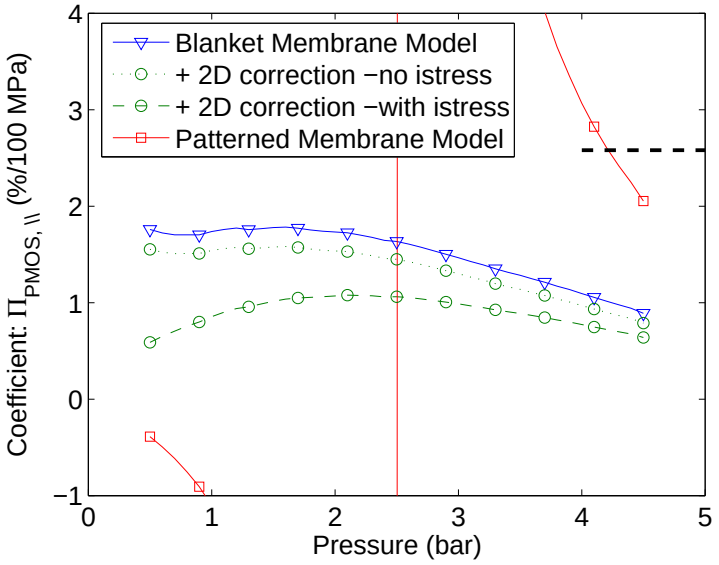


Figure 5.17: Piezoresistive coefficient $\Pi_{PMOS,\parallel}$ calculation as a function of the pressure from electrical measurements and simulated stresses, for various simulation models.

5.4.3 Second Axis: σ, $\pi \rightarrow \Delta I_D/I_{D_0}$

The computed current variations from simulated stresses and measured piezoresistive coefficients are given in Figure 5.18. They derive directly from the formulation of Equation (5.2), given that $\sigma_{\parallel} = \sigma_{yy}$ and $\sigma_{\perp} = \sigma_{xx}$.

5.4.4 Third Axis: $\Delta I_D/I_{D_0}$, $\pi \rightarrow \sigma$

As being implemented on the same design, it is a very good opportunity considering that the stress applied on the NMOSFET and the PMOSFET under pressure is the same in both cases. Their current variations may then be combined in order to determine both components of stress, as formulated in the following system:

$$\begin{cases} \left(\frac{\Delta I_D}{I_{D_0}}\right)_{NMOS} &= -\pi_{NMOS,\parallel} \cdot \sigma_{yy} - \pi_{NMOS,\perp} \cdot \sigma_{xx} \\ \left(\frac{\Delta I_D}{I_{D_0}}\right)_{PMOS} &= -\pi_{PMOS,\parallel} \cdot \sigma_{yy} - \pi_{PMOS,\perp} \cdot \sigma_{xx}, \end{cases} \tag{5.3}$$

which can be re-written under a matricial shape expliciting the piezoresistive coefficients values:

$$\begin{pmatrix} (\Delta I_D/I_{D_0})_{NMOS} \\ (\Delta I_D/I_{D_0})_{PMOS} \end{pmatrix} = \begin{pmatrix} +1.97 & +1.23 \\ -2.58 & +2.43 \end{pmatrix} \cdot \begin{pmatrix} \sigma_{yy} \\ \sigma_{xx} \end{pmatrix}. \tag{5.4}$$

The solutions of this system for each pressure value are plotted in Figure 5.19 and superimposed with stress components calculated by numerical models.

The maximum stress values of the resolved system are 663 MPa and 621 MPa, respectively for σ_{yy} and σ_{xx} under a pressure of 4.5 bar. The respective stress values at 4.8 bar,

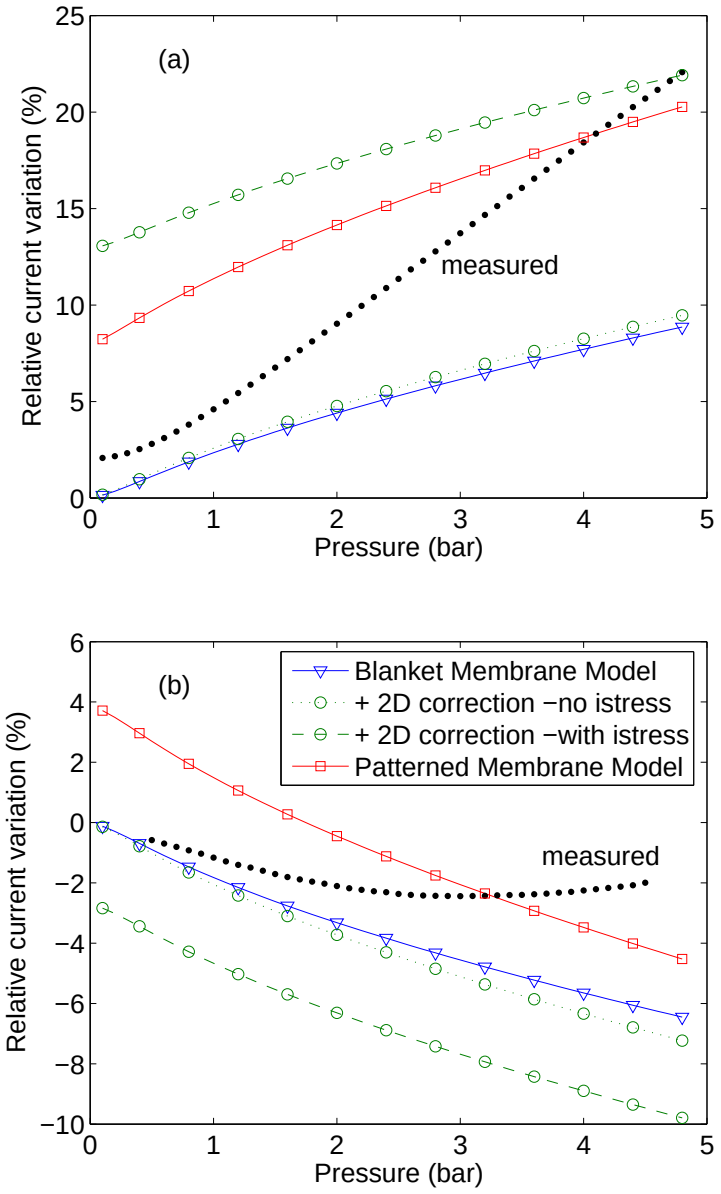


Figure 5.18: Simulated relative current variations of (a) the NMOSFET and (b) the PMOSFET as a function of the pressure, for various numerical models, compared with electrical measurements.

the highest pressure applied to the NMOS device, are extrapolated at 690 MPa and 672 MPa.

This calculation relies on the zero stress current reference (I_{D_0}). A change of this current value shifts vertically the output stress curve, without modifying nor the shape, nor the slope. The resolution accuracy relies also on adequate piezoresistive coefficients determination. However, it is also worth to note that thanks to the absolute values and signs of the π_{MOS} coefficients, the problem is well conditioned and the solution is robust to minor uncertainty on coefficients.

5.5 A Note about Rectangular Membranes

In the conclusions of Chapter 4, p. 90, the placement of a PMOS mirror architecture at the center of a membrane was evoked for robustness and process window reasons. As this architecture is sensitive to $\sigma_{yy} - \sigma_{xx}$, an asymmetrically stressed area is needed at the center of the membrane. Numerical simulations of blanket membranes have then shown that rectangular membranes would be convenient for that application (Figure 4.19). On the basis of the present mathematical resolution of both components of strain, we observe that the design under study in this chapter and based on a 250 × 400 μm^2 would not be convenient. Indeed, the ratio $\varepsilon_{width}/\varepsilon_{Length} = \varepsilon_{yy}/\varepsilon_{xx}$ remains close to unity, as illustrated in Figure 5.20. One can nevertheless envision that the this ratio might be device shape specific.

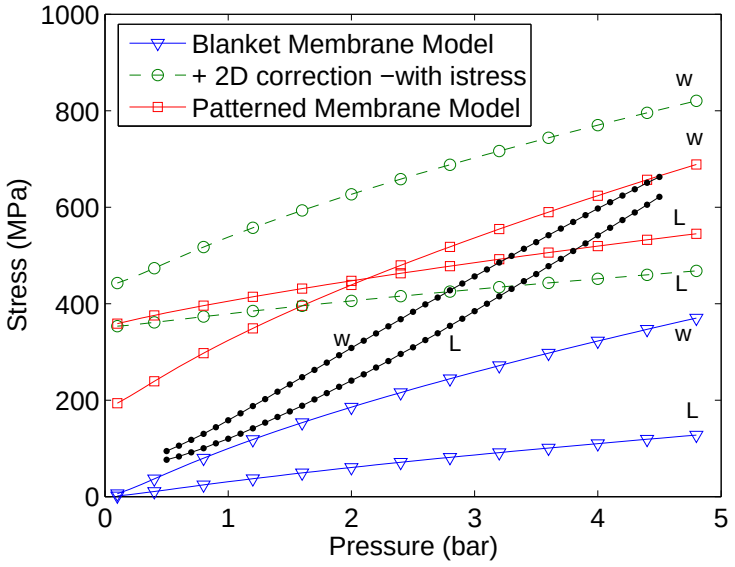


Figure 5.19: Calculated stress components (black knobbed line) as a function of the pressure, compared with the values yielded by various numerical models; the components are noted w and L respectively for σ_{yy} and σ_{xx}, which are oriented along the width and the length axes of the membrane.

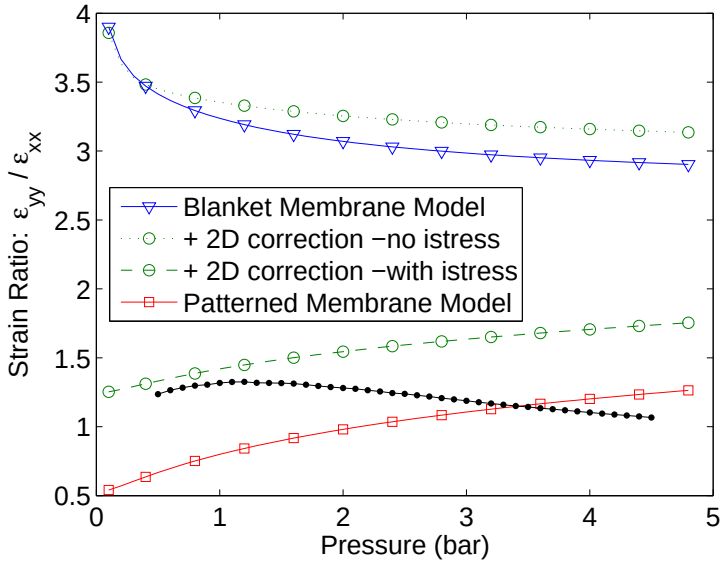


Figure 5.20: Calculated σ_{yy}/σ_{xx} stress components ratio (black knobbed line) as a function of the pressure, compared with the strain ratio values yielded by various numerical models; $\varepsilon_{width} = \varepsilon_{yy}$ and $\varepsilon_{Length} = \varepsilon_{xx}$.

5.6 Conclusions

The following conclusions may be formulated.

1. The combination on the same design of N- and P-MOSFETs is proven to open a very simple and effective way for resolving both stress components, on the basis of the piezoresistive theory. This resolution scheme spares advantageously the need for external numerical simulations. This method is, to our knowledge, not reported in the literature and is very promising for achieving, for example, mappings of stress distribution on any membrane design.

2. Stress values are estimated at 690 MPa and 672 MPa respectively for σ_{yy} and σ_{xx} at the maximum pressure of 4.8 bar. These values are clearly not reachable by a conventional bending set-up. Besides, the stress applied is biaxial, contrary to which is applied on bending set-ups. This gives then a suitable environment for complete electrical devices characterization under tunable strain.

3. From these simple calculations, it comes out that the strain components ratio $\varepsilon_{width}/\varepsilon_{Length}$ is close to unity. Expectations for using rectangular membranes as non-symmetric central stress supports for P-MOSFETs mirrors are then uncertain. Nevertheless, this ratio $\varepsilon_{width}/\varepsilon_{Length}$ is perhaps device shape specific. It is clear that, so far, only experimental proofs can be relied on.

4. Finally, one of the objectives of this chapter was defining the degree of complexity necessary to describe adequately the stress distribution and progression inside the sensitive

silicon, by comparing the outputs of various models issued from different routes. It was shown that all models give results on the order of the calculated stress values. But it has to be concluded also that none of the numerical models proposed in this chapter predicts sufficiently accurately to satisfy a sensor designer.

5. Beyond proving that dealing with such mechanical structures is a real challenge, potential ways of modeling improvement are listed here after.

   a. Utmost precise material constants have to be used.

   b. The stress evaluations from mechanical data are global, while simulations outputs are extracted in single central point of the channel. Extracting data as the mean value of surfaces or volumes corresponding to the device channel could help.

   c. A more complex and accurate model may need to be implemented. It is figured out building a 3D submodel.

   d. It is possible that the system under study outmatches the piezoresistive equation as it is formulated. Indeed, it is made implicitly the approximation $\Delta\mu/\mu \approx -\Delta\rho/\rho$, where μ and ρ are respectively the electron mobility and the channel resistivity. Tsang [163] proposes an alternative expression of the piezoresistive equation, declared as more accurate at higher stress values. That new formulation could be applied.

Part III

Direct Wafer Bonding

Chapter 6

Effect of interfacial SiO_2 thickness for low temperature direct wafer bonding

6.1 Introduction

In wafer bonding processes involving an interfacial silicon oxide film, Si/SiO_2 or SiO_2/SiO_2 bonding configuration are often two possible options during device manufacturing. However, it can also happen that the choice of bonding interfaces or even their dimensions (thickness) would be imposed by the final physical structure of devices or MEMS. So far, in the literature dealing with Si/SiO_2 and SiO_2/SiO_2 wafer bonding it was commonly accepted that Si/SiO_2 bonding strength was higher than SiO_2/SiO_2 [161, 98, 151]. Therefore, it resulted as a common option to use Si/SiO_2 as bonding interface. Today, we know that O_2 plasma activated wafer bonding enables stronger Si/SiO_2 and SiO_2/SiO_2 bonding at low temperature. But, beyond these considerations, a new request for efficient development is: how to use it routinely? In [188], Dr. Zhang has reported that annealing bubbles (appearing during the annealing step subsequent to O_2 plasma activated wafer bonding) were avoided by an adequate plasma exposure in Si/Si and SiO_2 (1000 Å)/SiO_2 (1000 Å) bonding. Maximum bonding strength was reached. High surface energy (2.3 J/m^2) and void-free wafer bonding was obtained after only 5 s O_2 plasma exposure on both thermally oxidized wafers. This can arise the question to know whether so high surface energy can be reached for SiO_2/SiO_2 wafer bonding with any interfacial oxide thickness by exposing wafers to 5 s plasma pretreatment. How this exposure could be optimized for low temperature wafer bonding of any configuration (Si/SiO_2 and SiO_2/SiO_2)? It is obvious that the answers to these questions will be helpful for generalizing the use of low temperature wafer bonding processes. In this chapter, we present the correlation between bonding strength and SiO_2 thickness at the bonding interface, and propose optimal oxygen plasma conditions to reach maximum surface bonding strength and void-free bonded surfaces.

6.2 Samples Preparation and Experimental Set-up

For this study, 3 inch, p-type, <100> one side polished commercially available silicon wafers were used. Some of the wafers to be bonded were oxidized at 1000 °C for obtaining oxide thicknesses from 500 Å, to 9000 Å after standard cleaning. Wet oxidation was adopted for all samples except for 500 Å oxidation, to get consistent roughness.

Before bonding, wafers were cleaned twice in a RCA-like solution (H_2SO_4:H_2O_2 = 5:2) at 110 °C during 10 minutes, each time was followed by 10 minutes rinsing in DI (de-ionized) water. All wafers were surface activated immediately after cleaning.

Most of the wafers used in Si/SiO_2 or SiO_2/SiO_2 bonding were pretreated by oxygen plasma under the same conditions (except exposure time) for comparison reason, in an Oxford PlasmaLab System 100. The surface activation parameters in the RIE (Reactive Ion Etching) chamber were 100 sccm O_2 flow, 90 mTorr chamber pressure, about 300 V DC bias, 100 W RF power and the plasma exposure time was varied from 5 to 120 s. O_2 plasma surface activation was followed by 10 minutes rinsing in DI water (except subsequently degassed wafers). Few other wafers were activated by warm HNO_3 (70%) at 70 °C during 30 minutes and rinsed (10 minutes). Some wafers were degassed during 1 hour at 400 °C under N_2 atmosphere after surface activation.

One part of the wafers was bonded manually: using tweezers, by applying pressure from the center towards the edge of the wafers to avoid trapped air at the bonding interface. Other wafers have been bonded with a K&W mask aligner using a special bonding kit. A force of 730 N was applied during 30 seconds at the center, initiating a bonding front also moving to the wafers edge avoiding bubbles formation. According to Yun et al. in [182], applied force during wafer bonding has no influence on resulting surface energy for surface activated wafers. Hence the results can be compared between these two runs without restriction. All bonded wafers have been subsequently annealed at 400 °C, during 70 or 120 hours, under nitrogen atmosphere.

After RT bonding and annealing, the wafers were systematically inspected by IR transmission imagery before and after annealing. The surface energies were extracted dynamically using the steady-state wedge opening method described with details in Appendix E.

6.3 Results presentation and discussion

6.3.1 Surface energy versus SiO_2 thickness for identical O_2 plasma exposure time

Figure 6.1 shows the surface energy as a function of the interfacial oxide thickness in Si/SiO_2 and SiO_2/SiO_2 wafer bonding. Two main observations can be formulated about O_2 plasma bonded pairs. First, there is an obvious loss of surface energy with the increase of the total interfacial oxide thickness for both wafer bonding configurations (Si/SiO_2 and SiO_2/SiO_2). The surface energy is evaluated at 2.35 J/m^2 for 1000 Å interfacial oxide and reduces to 1.3 J/m^2 with a 9000 Å SiO_2 film for SiO_2/SiO_2 wafer bonding, while

it is evaluated from 2.24 J/m^2 to 0.95 J/m^2 for Si/SiO_2 wafer bonding with the same total oxide thicknesses. Second, when considering the total interfacial oxide thickness (see Figure 6.2), the surface energies obtained for both wafer bonding configurations (Si/SiO_2 and SiO_2/SiO_2) are very close. Following these results, the vertical position of the bonded interface in the sandwich-like structure does not seem to play a role on the resulting bonding energy. One can then wonder how to explain the obtained results and their characteristics. What causes this strong correlation between surface energy and interfacial oxide thickness when bonded wafers are O_2 plasma surface activated? How to interpret the equivalence in terms of resulting surface energy between Si/SiO_2 and SiO_2/SiO_2 wafer bonding with identical interfacial oxide thicknesses?

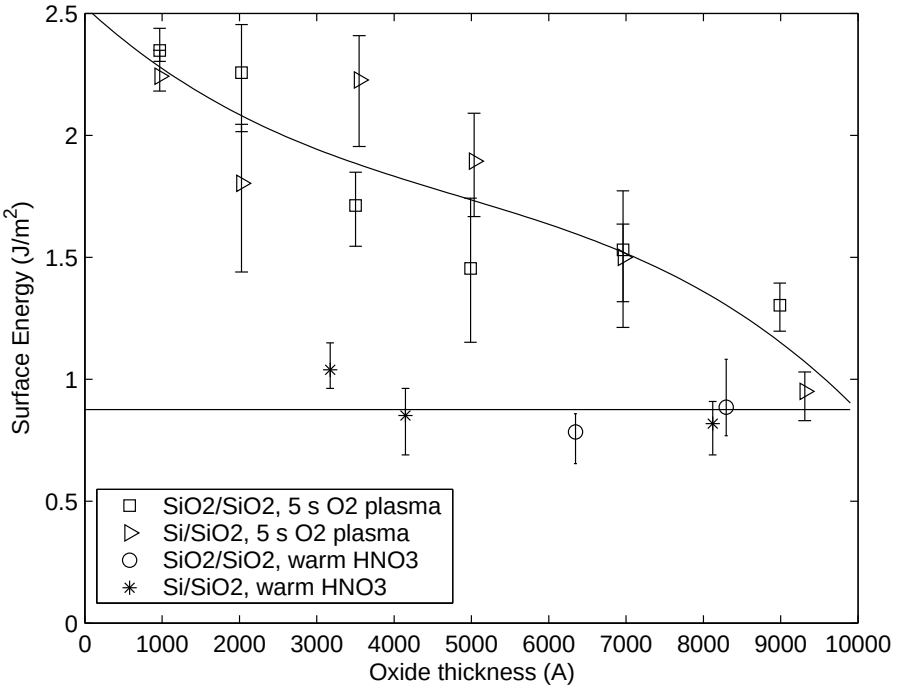


Figure 6.1: Surface energy as a function of the interfacial oxide thickness for Si/SiO_2 and $SiO2/SiO_2$ wafer bonding with O_2 plasma or warm nitric acid surface activation.

6.3.2 Analysis of the results

Several parameters are susceptible to influence the bonding strength in this case and have to be examined in order to explain the results. These are the roughness, due to the increase of layer thickness or due to the plasma action, the surface radicalization effect, due to O_2 plasma exposure, and, finally, the activation exposure time.

6.3.2.1 Surface roughness

In an early report [70], Hahn expected that a surface roughness difference between Si and SiO_2 was the cause of a dissimilar bonding strength. We investigated the rough-

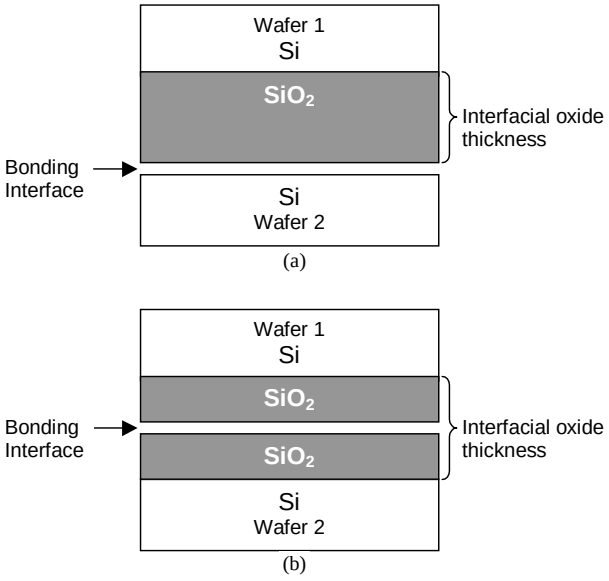


Figure 6.2: Schematic illustration of the sandwich-like structures: (a) Si/SiO_2 or (b) SiO_2/SiO_2 wafer bonding.

ness scope by AFM (Atomic Force Microscopy) measurements (see Figure 6.3) for three configurations: native oxide silicon, 2000 Å silicon oxide dry and wet thermally oxidized and 8000 Å (wet oxidations have been preceded and followed by dry oxidation steps of respectively 20 and 10 minutes, providing dryly oxidized interfaces). These measurements were made by contact mode with a silicon nitride micro-cantilever and ultra-sharp tip on squares of side 1 μm. Our results range from 0.88 Å to 1.31 Å in rms values (see Table 6.1), giving a quiet small roughness to all samples whith a slight increase according to the total grown oxide thickness.

We cannot therefore stipulate that the surface roughness is at the origin of an important loss of surface energy in this range of oxide thicknesses. For comparison purpose, in [78] a micro-roughness between 10 and 25 Å rms was considered to be acceptable, while in [47] a value of 2 nm is judged to be the limit of bondability which is far away from our measured values.

Analyzed Surface	Si with native SiO_2	SiO_2 2000 Å dry	SiO_2 2000 Å wet	SiO_2 8000 Å wet
Roughness: rms (Å)	0.69	0.88	1.08	1.31
Roughness: R_{max} (Å)	5.73	7.17	13.35	9.64

Table 6.1: Wafer surface topography measured by AFM on various natively or thermally oxidized samples (scanned area: 1 x 1 μm^2).

Additionally, this assumption is confirmed by the absence of surface energy variation with HNO_3 activated wafers, while varying the interfacial oxide thickness (Figure 6.1).

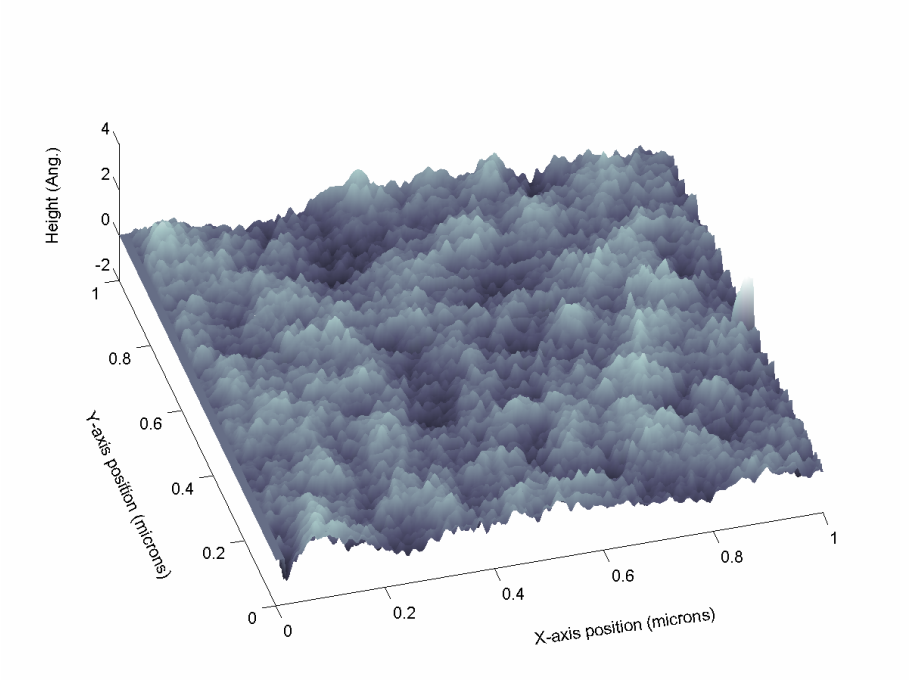


Figure 6.3: Wafer surface topography measured by AFM on prime hydrophylic silicon wafer.

These wafers have been degassed after their surface activation (400 °C during 1 hour, under nitrogen atmosphere). This step induced a drastic reduction of the activation efficiency but it ensured, in this case, that no excessive reaction by-product could weaken the resulting surface energy. By the way, it is worth to note that, for these wafers, there is no significant difference in terms of surface energy between Si/SiO_2 and SiO_2/SiO_2 wafer bonding. This contrasts with the results obtained in [98], where Si/SiO_2 bonded wafers presented higher surface energy than SiO_2/SiO_2 wafer bonding. The low diffusion of interfacial water through oxide short annealing can certainly explain different experimental results. Actually, relatively (6 hours at 300 - 500 °C) was considered in [98], whereas in our experiments, the annealing time was 70 hours, letting us suppose that diffusion had completed before the end of the annealing step.

Besides, a presumably micro-roughness variation could also originate from the O_2 plasma surface activation itself. Indeed, some authors [131, 36, 11] mentioned smoothing or, at the opposite, roughening of the surface as an effect of the O_2 plasma. A smoothing or roughening of activated surfaces could affect the resulting bonding strength, but as all the activated wafers (with different oxide layers thicknesses) were submitted to the O_2 plasma process step under the same conditions, any variation of roughness should be the same for all wafers. Moreover, the physical action in terms of the surface structure (smoothing or roughening) is not perceptible in surface energy measurements. Practically, the horizontal curve in Figure 6.7 is the linear regression of surface energies obtained with bonded wafers that were degassed (400 °C during 1 hour, under nitrogen atmosphere) after the surface activation. Hence, the only difference among the wafers belonging to both curves consists

in the presence (for high energy wafers) or the absence (for degassed wafers) of silanol groups at their surface but no physical change of the surface micro-roughness can have occurred. As the degassed wafers presented a remarkably constant surface energy for all exposure plasma periods, we are sure that no change of micro-roughness can have affected the resulting bonding strength, until at least 120 s exposure time (for 4000 Å thick oxide layers).

6.3.2.2 Chemical surface analyses

To analyze chemically O_2 plasma activated surfaces, we proceeded to contact angle measurements. This was a way to characterize the hydrophilicity degree of the surface by representing the silanol density, as presented by Lay in [101] or Bäcklund in [14] with various prebonding cleaning treatments. In [186], Dr. Zhang has made direct measurements after O_2 plasma treatments with different exposure times on Si surfaces and get values between 2 and 4° giving not significant difference according to the applied surface treatments. In this work, the method was applied in a different way: it was implemented after a silanization step. The silanization presents the advantage to change hydrophilic surfaces into hydrophobic ones by reaction with the siloxane radicals, inverting the contact angle measurement. Nevertheless, these experiments also yielded very close and inconsistent values: between 98 and 113° after silanization treatment. Therefore, this technique appears to be useful for qualifying the hydrophilic or hydrophobic character of a surface but not sufficiently sensitive to quantify precisely the silanol density. It then prevents us to conclude anything about the efficiency of surface activation among various O_2 plasma activated samples.

Besides, ToF-SIMS (Time of Flight - Secondary Ion Mass Spectroscopy) analyses were performed in order to quantify the O_2 surface activation chemical effects on thermally oxidized wafers surfaces. OH groups concentration has been measured using an incident beam covering square area of 100 μm side and two different areas of each sample have been examined for controlling the consistency of the measurements. As this measure was done in vacuum chamber, a degassing effect can have occurred and results have to be carefully considered. Two thermally oxidized wafers (2000 Å and 8000 Å) were O_2 plasma surface activated during 5 seconds and gave a ratio SiOH/SiO of, respectively, 55.9 and 43.9. Although these values constitute no evidence, they are an indication of an efficiency's difference of the O_2 plasma surface activation according to the silicon oxide layer thickness. Hence, with an identical O_2 plasma exposure time, it is expected that the radicalization effect (allowing silanol groups' formation) of plasma activation on treated surfaces will be more intense for thin oxide layers than for thicker ones.

6.3.2.3 Surface energy versus Oxide thickness for various Plasma exposure time

A key factor of this activation technique is the exposure time. Previous report [188] indicated that O_2 plasma surface activation has to be finely tuned in order to reach high surface energies for Si/Si wafer bonding. Optimal exposure was found out at 3 seconds. Actually, this exposure time has to be adjusted for every wafer bonding configuration

i.e. the bonded oxide layers thicknesses. We have examined this optimal exposure time in Si/SiO_2 and SiO_2/SiO_2 wafer bonding with thin interfacial layer (2000 Å). Thick interfacial layer has also been investigated in SiO_2/SiO_2 configuration only.

Thin interfacial oxide - SiO_2/SiO_2 Figure 6.4 illustrates the effect of insufficient or excessive pretreatment on surface energy by dynamic measurements for SiO_2 (1000 Å)/SiO_2 (1000 Å) wafer bonding. Insufficient plasma exposure (5s/one wafer) generated low surface energy due to a contamination by hydrocarbons which occurred on the non activated wafer. It originated from the lack of surface cleaning effect of O_2 plasma. The hydrocarbon was absorbed in SiO_2 (voids would have appeared in Si/Si wafer bonding [187]) but it weakened the bonding strength. At the opposite, excessive plasma exposure (10s/one wafer and 10s+10s/two wafers) still resulted in low bonding strength due to the excess of interface reaction by-product (10s+10s/two wafers), besides the hydrocarbon mentioned for (10s/one wafer) bonding. The surface energy distribution with insufficient or excess plasma treatment is illustrated in Figure 6.5. The obvious uniformity with (5s/one wafer) can also indicate a lack of silanol groups formed during the activation. (10s/one wafer) presents important bonding strength variations which is typical of an excess of by-product. Besides, the bonding strength of (5s+5s/two wafers) was too strong and the wafers collapsed during the surface energy measurement. It appears clearly that adequate plasma exposure (5s+5s/two wafers) is requested based on the SiO_2 thickness to reach the maximum surface energy (2.32 J/m^2).

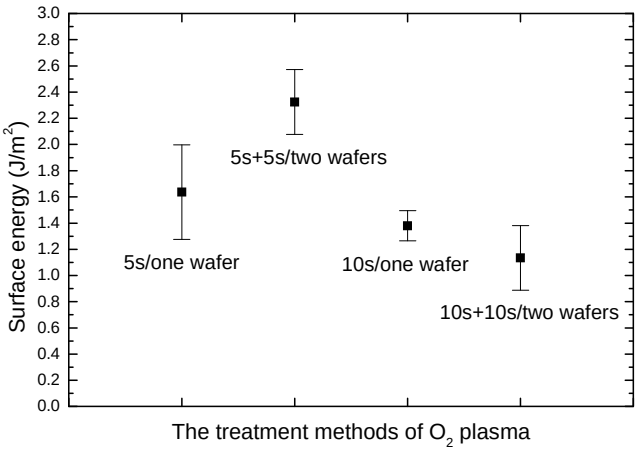


Figure 6.4: Bonding strength related to the methods of plasma treatment for SiO_2 (1000 Å)/SiO_2 (1000 Å) bonding, annealing at 400 °C during 120 hours.

Thin interfacial oxide - Si/SiO_2 Si/SiO_2 (2000 Å) wafer bonding configuration has also been studied with various exposure periods (from 5 s to 20 s) for SiO_2 surface, Si surface exposure was fixed at 5 s. Figure 6.6 gives the measured surface energies as a

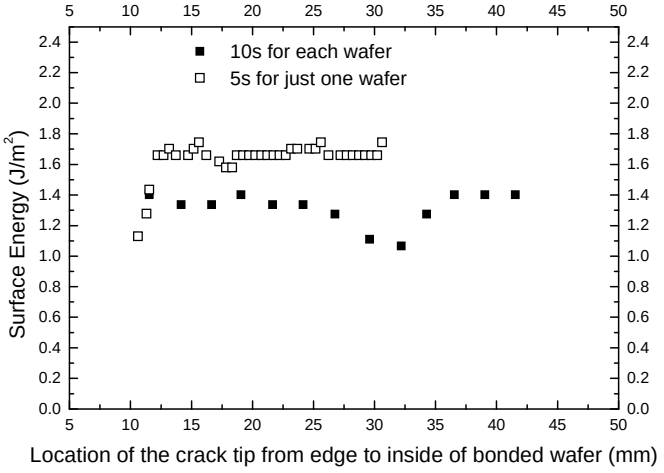


Figure 6.5: Effect of insufficient and excess plasma on the distribution of bonding strength, all wafers with 1000 Å SiO_2, annealing at 400 °C during 120 hours after pre-bonding.

function of plasma exposure time. Effects of insufficient or excess plasma exposure are obvious, maximum bonding strength is reached after 7 s exposure and equals 1.8 J/m^2. This value confirms again the non superiority of the Si/SiO_2 wafer bonding, nuancing commonly admitted ideas. It can be interesting to note that bonding reaction by-product generated visible voids for exposure time longer than 20 s.

Thick interfacial oxide - SiO_2/SiO_2 The shift of optimum exposure time becomes very important when increasing the bonded oxide layers. On the one hand, 40 s plasma pretreatment was performed for each wafer in SiO_2 (2500 Å)/SiO_2 (2500 Å) wafer bonding and yielded so high bonding strength that all samples collapsed during the dynamic testing [186, 188], despite a very slow wedge velocity (0.25 mm/min). It is worth to note that the theoretical surface energy of SiO_2 (4.1 J/m^2) is much higher than bulk silicon (2.5 J/m^2) [160]. No annealing voids appeared at the bonding interface after 400 °C annealing during 120 hours. On the other hand, Figure 6.7 gives the surface energy evolution with O_2 plasma exposure time for SiO_2 (4000 Å)/SiO_2 (4000 Å). It clearly evidences the possibility to reach a high surface energy (2.15 J/m^2) with a thick interfacial oxide layer (8000 Å), by adjusting the plasma exposure period (60 s).

6.3.2.4 Interpretation

Our interpretation of these results is based on the strike action of oxygen ions on activated surfaces. For silicon surfaces, this action evolves the formation of a silicon oxide layer [130] that saturates at a thickness of 60 Å after 4 minutes of exposure time [186]. For already oxidized layers no such oxidation can occur, but in both cases the plasma action results in a highly enhanced concentration of radicals, by breaking covalent bonds

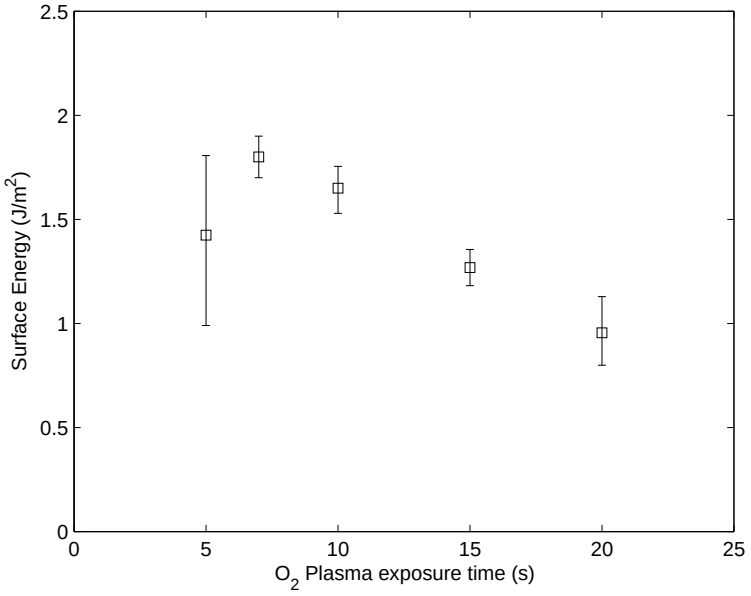


Figure 6.6: Surface energy as a function of O_2 plasma exposure time of SiO_2 surface in Si/SiO_2 (2000 Å) wafer bonding; Si surface activated with O_2 plasma during 5 s; annealing at 400 °C for 120 hours after pre-bonding.

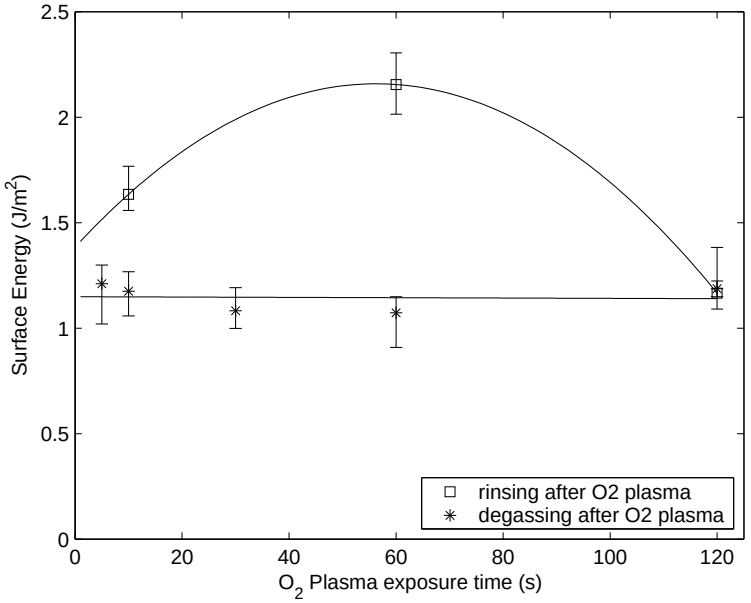


Figure 6.7: Surface energy as a function of O_2 plasma exposure time for SiO_2 (4000 Å)/SiO_2 (4000 Å) wafer bonding, annealing at 400 °C for 70 hours after pre-bonding.

at the surface, and generates a disordered surface structure [11]. In [177], it was reported that incident oxygen ions are highly mobile in SiO_2 and appear to diffuse inside the oxide layer. Hence, for thicker activated oxide layers, a significant part of ionized oxygen atoms can be absorbed into the oxide volume and react with the created radicals, reducing the O_2 plasma surface activation efficiency. This involves the competition between two post-activation reactions: radicals can form silanol groups or, otherwise, react with trapped oxygen atoms.

These two possibilities have been experienced, respectively, by rinsing wafers immediately after activation (see Figure 6.7) or by degassing activated wafers under nitrogen atmosphere. In the first case, high surface energies were achieved by adjusting the silanol groups density (i.e. the exposure time). Assuming that the surface cleaning role of O_2 plasma completed after a few seconds exposure, the density of OH- groups had to be maximized without yielding excess by-product (like observed with excessive exposure of 120 s). In the second case, radicals reacted during the annealing with absorbed oxygen atoms and produced constant surface energies for all plasma activation times.

6.4 Conclusions

After having analyzed the influence of interfacial oxide thickness on resulting surface energy for both Si/SiO_2 and SiO_2/SiO_2 wafer bonding, several conclusions can be set forth.

1. O_2 plasma surface activation needs to be optimized according to the interface layers (nature and thickness), in order to reach high bonding surface energies.

2. The slight increase of surface micro-roughness can not explain the drastic reduction of the surface energy with the interfacial oxide thickness.

3. The efficiency of O_2 plasma activation strongly depends on the oxide volume of activated wafers. It induces:

   a. An important loss of bonding strength when increasing the interfacial oxide thickness, for wafers submitted to identical activation time. Surface energy reduced from 2.35 J/m^2, for 1000 Å interfacial oxide, down to 1.3 J/m^2, for 9000 Å SiO_2 layer.

   b. A sharp shift of the optimum exposure time with the increase of the oxide thickness. It extends from 5 s, for SiO_2 (1000 Å)/SiO_2 (1000 Å) wafer bonding, up to 60 s for SiO_2 (4000 Å)/SiO_2 (4000 Å).

4. The understanding of O_2 plasma surface activation as a function of the interfacial oxide thickness enables the possibility to reach very high surface energies in situations that can be imposed by the process flow of specific tridimensional devices or MEMS i.e. constraints on the wafer bonding type (Si/SiO_2 or SiO_2/SiO_2) or on the interfacial layers thicknesses.

Chapter 7

PECVD oxide as intermediate film for wafer bonding: Impact of residual stress

7.1 Introduction

Plasma Enhanced Chemical Vapour Deposited (PECVD) silicon oxide is widely used in microelectronics and Micro-Electro-Mechanical Systems (MEMS) fields. Thanks to their low deposition temperature, PECVD films are very convenient for processes requiring low thermal budget. Plasma instead of heat ignites the chemical reaction and allows reaching high deposition rate. These process characteristics and the physical properties of PECVD oxide films set-up their utility in a wide range of applications. They are notably used as sensitive insulator layer in pH detection systems [43], sacrificial layer in MEMS fabrication [184] or nano-mechanical testing systems fabrication [12], as wave guide layer in optical systems [42] and [37], as thermally insulating layer in multilayered dielectric membranes [81], as passivation layer in Integrated Circuits (ICs) fabrication [15, 76, 106], as interfacial layer in wafer level packaging [53] and three-dimensional (3D) integration processes [157] and [34].

The variety of PECVD silicon oxide applications partly originates from the fact that PECVD process parameters can be tuned according to the requested properties for the deposited film. The most important deposition parameters are: (i) the Radio Frequency (RF) power, (ii) the ratio of the different precursor gases, (iii) the total flow rate, and (iv) the deposition temperature. Among the silicon oxide properties which strongly depend on the PECVD process parameters, we can mention: (i) the etch rate in buffered hydrofluoric acid (BHF), (ii) the material density, (iii) the optical index and (iv) the residual internal stress [52].

The control of the residual stress in a deposited PECVD layer might be a critical issue since it can limit the thickness of the deposited film to avoid the appearance of cracks [184]. When a higher density or a lower stress is required, a Rapid Thermal Annealing (RTA) can subsequently be applied on the deposited layer [51]. RTA process step impacts also other characteristics of the deposited silicon oxide such as its etch rate in BHF and its optical

index. RTA has the advantage of being lowly time consuming and fully compatible with a CMOS process, as it does not induce more diffusion than doping species activation. A RTA step can even be made after an implantation step in order to combine stress release and doping activation. A good understanding of the PECVD oxide film behaviour after thermal treatment is very valuable. As an example, depositing a Low Pressure Chemical Vapour Deposited (LPCVD) silicon nitride film over a sacrificial PECVD oxide layer constitutes a thermal treatment (usually as high as 800 °C) on the oxide which will affect its properties in terms of stress and etch rate. Those material properties changes must be considered to develop successful and reliable MEMS devices.

A main difficulty to be overcome in wafer bonding of PECVD silicon oxide is the wafer bow. In Reference [107], Lin and co-authors report that the wafer deflection constitutes a wafer bonding issue while Tan et al. in [156] mention that 25 μm is the wafer bow upper limit to achieve direct wafer bonding with 6-inch wafers. Additionally, the wafer bow prevents a good inter-wafer alignment in 3D integration direct wafer bonding [28] and [149]. Hence, three ways are figured out in order to decrease the wafer bow: (i) decrease the stressed film thickness, (ii) compensate the wafer global stress by depositing identically stressed films on the opposite wafer side [149], or (iii) reduce the residual intrinsic film stress by a specific technological mean. Obviously, for applications requiring a thick film, only the two last solutions are suitable. This work focuses on the latter strategy, i.e. decreasing the residual stress in the PECVD silicon oxide layer.

In this chapter, Section 7.3 explores the role of main PECVD deposition parameters: the total gases flow in the reactor chamber, the applied RF power, and the ratio between the two precursor gases (nitrous oxide and silane 5%). For each parameters combination, figures of merit are evaluated before and after RTA: the deposition rate, the residual stress and the BHF etch rate. From Section 7.3, a few oxide recipes are selected, based on their properties, and are further analysed and processed in the next parts of this work. In Section 7.4, the influence of RTA temperature and duration is discussed. Section 7.5 exposes the stress variability over time for lowly dense oxides. Section 7.6 is dedicated to surface roughness considerations. Surface roughness of the as-deposited oxide is measured as well as after RTA. Chemo-Mechanical Polishing (CMP) parameters are adjusted to produce the smoothest surface for each selected silicon oxide layer. Finally, Section 7.7 ends up with direct wafer bonding experiments, demonstrating the importance of considering the bow and, from there, the residual stress in PECVD oxide films for this application.

7.2 Experimental set-up

Three-inch diameter p-type $\langle 100 \rangle$ 380 μm-thick bulk silicon wafers are used as substrates. The PECVD silicon oxide is deposited in an OXFORD Plasmalab System 100. The size of the deposition chamber allows for processing three wafers simultaneously. The chamber consists of a top electrode with high uniformity shower head gas inlet top separated by substrate electrode heated and grounded. The frequency of the RF power generator applied to the top electrode is 13.56 MHz. Through the whole batch of experiment the pressure in the chamber is kept at 1 Torr and the substrate electrode temperature is also kept constant at 300 °C. The two precursor gases used to deposit the silicon oxide are nitrous oxide (N_2O) and silane (SiH_4) diluted in nitrogen at a concentration of 5%. In

the following, silane or SiH_4 stands for silane 5%. Variation ranges for the parameters are: from 200 to 1050 sccm for the total flow rate, from 5 to 17 for the gas ratio $[N_2O]/[SiH_4]$, and from 30 to 100 W for the RF power. In the first part of the study, the deposition time is 20 min, in order to get a film thickness between 1 and 2 μm, the deposition rate strongly depending on the deposition parameters. For roughness and wafer bonding experiments, the deposition time is adjusted according to the recipes to get 1.5 μm-thick films.

The thickness of the deposited film is measured with a Prometrix Spectramap System 100. It uses spectral analysis of reflected white light in the 400-800 nm range to provide accurate and repeatable thickness measurements from 20 nm to 5 μm on 3-inch wafers. This computer controlled system collects data on 10 sites per wafer and gives the mean value of the measured thickness, the standard deviation and the range of the measured points set.

The residual stress in the oxide layer is deduced by a measurement from the strain induced in the silicon substrate by the oxide layer deposition (change in wafer curvature). The wafer curvature before and after the deposition is obtained using the Dektak profilometer over a long scanned distance (50 mm). The profilometer gives the maximal deflexion of the wafer surface over the scanning line (see Figure 7.1). The curvature radius R is approximated by:

$$R = \frac{\left(\frac{L}{2}\right)^2}{2 \cdot h_{\max}} \tag{7.1}$$

where h_{max} is the maximal deflection of the wafer surface and L the scanning length. Once the strain is determined, the stress is easily calculated using the Hooke's law for elastic deformation. If the deposited film is much thinner than the wafer thickness, and the stress isotropically distributed through the cross section of the film, we can derive the Stoney equation [150]:

$$\sigma = \frac{E}{6 \cdot (1-\nu)} \cdot \frac{t_{\text{sub}}^2}{t_{\text{film}}} \cdot \left(\frac{1}{R_{\text{post}}} - \frac{1}{R_{\text{pre}}} \right) \tag{7.2}$$

where σ is the stress in the thin film, E and ν, respectively, the Young modulus (130 GPa) and Poisson ratio (0.28) of the substrate, tsub and tfilm, respectively, the substrate and film thicknesses and, R_{pre} and R_{post}, respectively, the curvature radius of the wafer before and after deposition. As the wafers do not have the same curvature radius before deposition (the h_{max} value can vary from 600 nm up to 15 μm), the curvature radius is systematically measured before and after deposition.

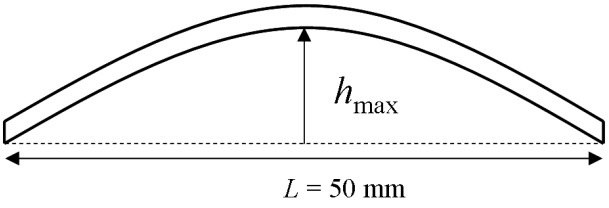


Figure 7.1: Evaluation of the wafer radius curvature by profilometer scan.

The BHF solution used to measure the etch rate is prepared in the following proportions: 87% NH_4F [40%], 13% HF [49%] in volume. The etching is performed at 20 °C without shaking.

An ADDAX RTA oven with a single 3-inch wafer chamber is used for the rapid thermal annealing. As observed by Dominguez et al. [51], the ambient gas during annealing does not have any impact on the RTA effect. Thus, the ambient gas during RTA is pure nitrogen, with a flow rate of 4 l/min during the heating phase and a flow rate of 6 l/min during the cooling phase. The heating rate is 700 °C/s and the cooling is efficient enough to drop down to a temperature of 500 °C in less than 2 s after a heating at 950 °C. The temperature is varied between 400 and 950 °C and the annealing time between 2 and 30 s.

The wafer surface microroughness is characterized with an Autoprobe CP from Park Scientific Instruments in contact mode with a nitride tip from Veeco.

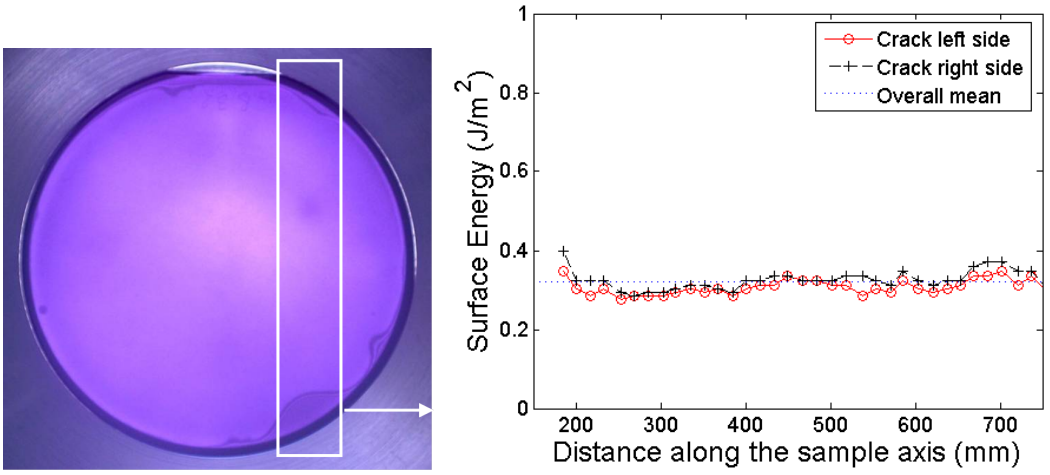
Chemical-Mechanical Polishing (CMP) is performed on a Mecapol P600 from Presi. Two pads also coming from Presi are used. The first, a LDR1 type pad is a semi-hard one embossed, non-woven and impregnated with polyurethane. The second pad in use, a PUR A1 type is a hard one, made up of rigid and micro-cellular polyurethane foam. For removal rate uniformity purpose, the polishing head is driven in the same rotational sense than the table at almost the same speed: 1 rpm is added to avoid any resonance effect between the head and the table. The slurry consumed is ACESOL 1212 from Kemesys: an alkaline solution with 100 nm colloidal silica particles, designed for interlayer dielectrics polishing. In order to find the best process parameters resulting in a smooth surface, rotational speed of the table is varied from 50 to 80 rpm. The slurry flow ranging from 75 to 125 ml/min and the head pressure is varied between 0.25 and 0.8 bars. The polishing time is 2 min on 1.5 μm-thick PECVD oxide samples. After CMP, all wafers are kept wet in DI water and are scrubbed in a SVG tool with a spin drying as final step.

In wafer bonding experiments, the wafers are inspected by infrared (IR) transmission imagery before and after annealing. The surface energy is dynamically extracted using the steady-state wedge opening method [20], measuring the crack length by IR light passing through the bonded pair and giving a direct image of the crack on a digital camera. A 100 μm-thick razor blade is mounted on a universal mechanical testing machine. The blade is inserted between the two 380 μm-thick wafers and moved at a constant rate, controlled by a computer. As illustrated in Figure 7.2, this set-up can perform dynamic surface energy measurements all along the diced samples, providing the crack length from many locations. Simple beam theory leads to the surface energy determination from the measured crack length, through the following relationship:

$$\gamma = \frac{3Eu^2h^3}{32a^4}, \tag{7.3}$$

where E is the uniaxial Young's modulus (150 GPa in our experiments), a is the crack length, u and h are the wedge and wafers thicknesses, respectively.

The impact of the triangle tip height (0.4635 mm) of the blade on surface energy extraction (increasing the real crack length) is also corrected in our calculations. The resulting accuracy of the crack length measurement is about of 0.1 mm (1 pixel $\approx$ 0.1 mm).



(a) (b)

Figure 7.2: (a) Infrared picture of a wafer bonded sample diced perpendicularly to the flat and (b) the measured surface energy all along the sample bonding interface.

7.3 Deposition parameters

Oxford Instruments company gives a standard recipe for PECVD oxide which constitutes a starting point for this study. In this section, the tested recipes are derived from that one, just varying one parameter at a time. The given standard oxide deposition parameters are mentioned in Table 7.1, where the recipe is referred as *OxideStd*.

7.3.1 Gas flow

The total gas flow is varied from 200 to 1050 sccm keeping all the other parameters constant (1 Torr, 100 W, 300 °C, $[N_2O{:}SiH_4] = 7$). Physical properties, i.e. deposition rate, residual stress and BHF rate, are measured before and after a 900 °C RTA of 15 s. Figure 7.3 plots the evolution of these properties as a function of the total gas flow.

The first observation is that the deposition rate increases linearly with the total gas flow, letting us assume that all the gases react and give rise to more oxide when more reactants are present. Besides, to get a uniform deposited oxide film over the whole wafer, the total gas flow has to be over 400 sccm. Below this value the standard deviation of the measured thickness is over 3%. This effect is due to the volume of our deposition chamber which allows to process three wafers at a time. In fact, the chamber requires a minimum gas flow passing through it to have a homogenous diffusion of the gases inside the chamber.

The residual stress and the etch rate appear to be strongly correlated, while they vary inversely. In fact, both of them vary moderately up to a total gas flow of around 700 sccm. The residual stress increases while the etch rate decreases with higher gas flow. Beyond this pivot value, the residual stress and BHF etch rate are both drastically modified, leading to very lowly stressed oxide films as well as very fast etched films. These trends are applicable

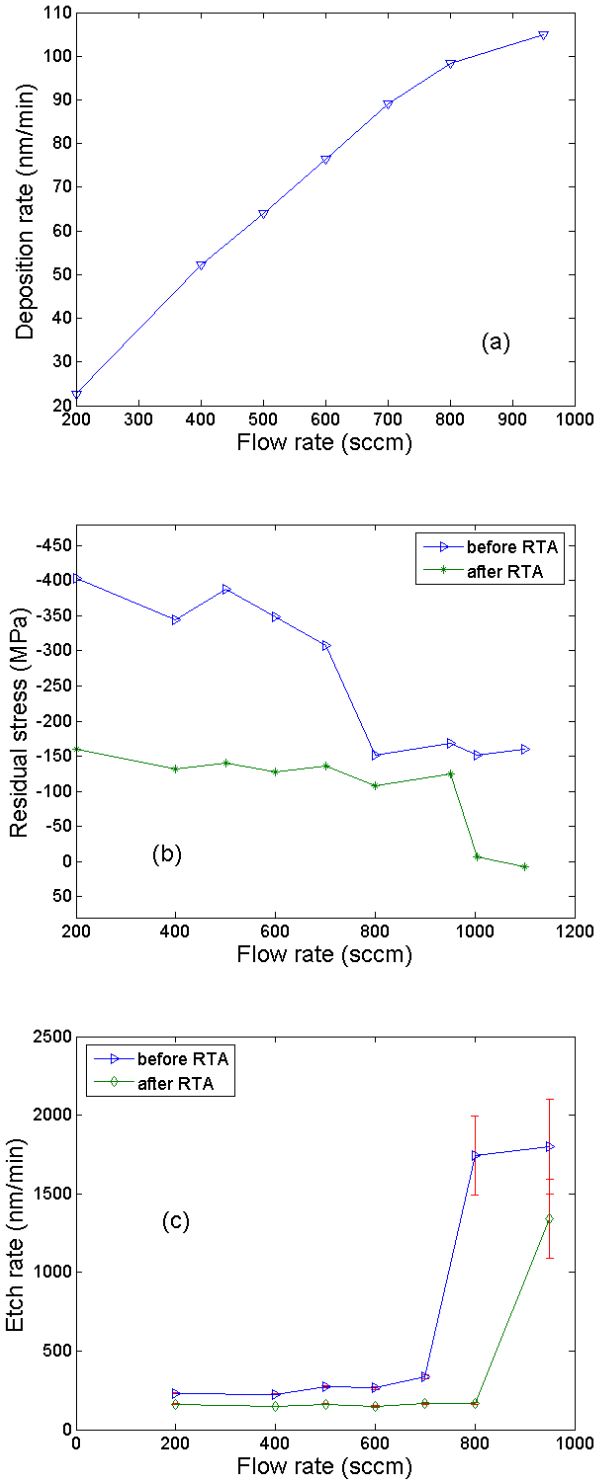


Figure 7.3: Figures of merit as a function of total precursor gas flow rate: (a) deposition rate, (b) residual stress, and (c) BHF etch rate.

Recipe reference	SiH_4 flow (sccm)	N_2O flow (sccm)	N_2 flow (sccm)	$[N_2O/SiH_4]$ ratio	RF Power (W)
OxideStd	75	525	-	7	100
OxideHiF	125	880	-	7	100
OxideLoP	75	525	-	7	30
OxideLoR	100	500	-	5	100
OxideTO	100	700	-	7	100
OxideILD	100	700	1000	7	30

Other deposition parameters: temperature = 300 °C, pressure = 1 Torr.

Table 7.1: Nomenclature and deposition parameters of selected representative oxide recipes; *OxideStd* is a recipe coming from Oxford Instruments, *OxideHiF* is adapted with a higher gas flow, *OxideLoP* is adapted with a lower pressure, *OxideLoR* is adapted with a lower $[N_2O/SiH_4]$ ratio, *OxideTO* is a recipe adapted as a stress/etch-rate trade-off, *OxideILD* is used as interlayer-dielectrics recipe

before and after RTA. Besides, RTA allows keeping an acceptable etch rate of 300 nm/min at 700 sccm while the residual stress is considerably reduced from -300 to -150 MPa. Above this total gas flow, it is not possible anymore to control the etch rate, the error bars on the graph indicating the non homogeneity of the etch rate. On the other hand, the residual stress in that case becomes null after RTA, which can be an advantage if the film is used as passivation layer or as bonding interface. One disadvantage of this low-stress high-etch rate oxide is that it is not stable over the time. This point will be detailed in Section 7.5.

7.3.2 RF Power

The power is varied from 30 to 100 W. Total gas flow is kept at 600 sccm, pressure at 1 Torr, $[N_2O]/[SiH_4]$ at 7 and the chuck temperature remains constant at 300 °C. Figure 7.4 presents the measurements done for these samples before and after RTA.

Previous studies [113] showed that the quality of the PECVD film strongly depends on the ratio $\eta P/F$, where η is the gas dissociation efficiency, P the power and F the total gas flow. A high ratio means that the energy transfer process is well matched to the presence of ion species, leading to well bonded atoms in the deposited layer. At contrary, a too low ratio will yield poor quality oxide with voids and nodules [133], where the atoms are weakly bonded. Stress and etch rate curves can be interpreted according to these statements. First, the stress continuously decreases with the applied power. At low power, the atoms are weakly bonded in the silicon oxide layer and do form voids, relaxing the internal stress. Rapid thermal annealing always leads to a stress decrease by a re-organization effect in the deposited layer. With a power of 30 W, a null stress oxide is obtained but for this oxide, stress varies with the time. This point will be detailed in Section 7.5. Second, the etch rate continuously decreases as the power increases. For low power, the etching of the deposited film in BHF is totally non uniform, the etching rate being determined at around 1700 nm/min with an uncertainty of 500 nm/min. The silicon oxide formed at low power has weakly bonded atoms and, therefore, is easily etched in fluoric acid solution. Nevertheless, the RTA reduces drastically the etch rate which also becomes more homogenous. At low

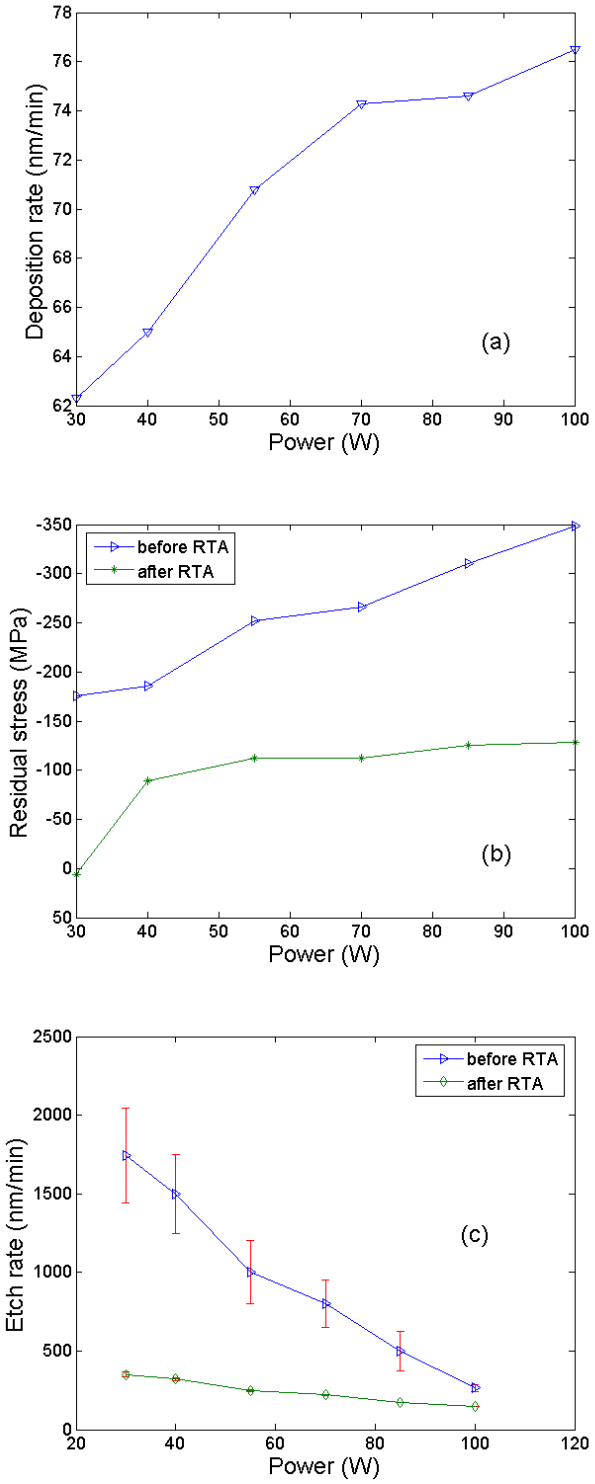


Figure 7.4: Figures of merit as a function of RF power: (a) deposition rate, (b) residual stress, and (c) BHF etch rate.

power and after RTA, the etch rate is at the order of 400 nm/min: a possible handling value. The oxide deposited at 30 W seems to be a good candidate for bonding and passivation applications, except its temporal instability as it will be explained in Section 7.5.

7.3.3 Precursor gases ratio

The ratio of the two precursor gases [N_2O/SiH_4] is varied from 5 to 17. Total gas flow is kept at 600 sccm, pressure at 1 Torr, power at 100 W and the chuck temperature remains constant at 300 °C. Figure 7.5 shows the measurements done for these samples before and after RTA.

The deposition rate increases when the silane partial pressure increases, i.e. at low [N_2O/SiH_4] ratio. The limiting factor for oxide deposition rate is the quantity of Si ions presents in the plasma. Besides, Figures 7.5(b) and 7.5(c) show that an oxide made of plasma with a low value of [N_2O/SiH_4] ratio is at the same time of poor quality. For too high silane concentration (below a gas ratio of 6), the etch rate increases and is not homogenous over the whole wafer surface area. We observe conjointly with the etch rate increase a decrease of residual stress. For Si-rich PECVD silicon oxide [117] the bond reaction energy is lower than for stoichiometric silicon dioxide, explaining the higher reactivity with BHF. As for the previous samples the RTA decreases the residual stress and the BHF etch rate. The mechanisms occurring are the same as for the two previous batches of experiments while from [117] and [56] we know that at high [N_2O/SiH_4] ratio more $Si-O$ bonds are formed while at low [N_2O/SiH_4] ratio more $Si-H$ bonds are formed, taking distance with stoichiometric silicon oxide. For a gas ratio of 6, the etch rate is brought back from 500 to 200 nm/min, which is an acceptable value to control oxide etching in a process. Stress free oxide is not obtained by varying the gas ratio.

7.4 Effects of RTA temperature and time

Various RTA times and temperatures are tested on samples with a 1.5 μm-thick oxide layer. The oxide recipe used for this analysis is *OxideStd* from Table 7.1. The RTA times are varied from 3 to 30 s and compared with a conventional thermal annealing of 30 min at 900 °C in 1.5 l/min N_2. The RTA temperature is increased from 400 to 950 °C (Figure 7.6) while the kept constant at 15 s. Etch rate and residual stress are then measured.

Below 500 °C, RTA has no impact on the deposited oxide. No reconstruction or impurities release occurs, as shown by the stability of the two measured parameters. As the temperature increases up till 950 °C, stress and etch rate decrease with similar trend. The literature [148] and [143] provides many explanations for this change in properties. The non stoichiometric SiOxNyHz film releases H and N atoms during the annealing and experiences the following network reaction:

$$SiO_x \rightarrow \left(\frac{x}{2}\right) SiO_2 + \left(1 - \frac{x}{2}\right) Si. \tag{7.4}$$

Between 500 and 700 °C, H is released but the bonds $Si-O$ do not suffer any rearrangement. Above 700 °C re-organization of $Si-O$ in SiO_2 occurs. In our experiments we do not measure the concentration of $Si-H$, $Si-N$, $Si-O$ bonds, but the macroscopic properties are recorded. A RTA of 900 °C during 15 s seems to be enough to reach the

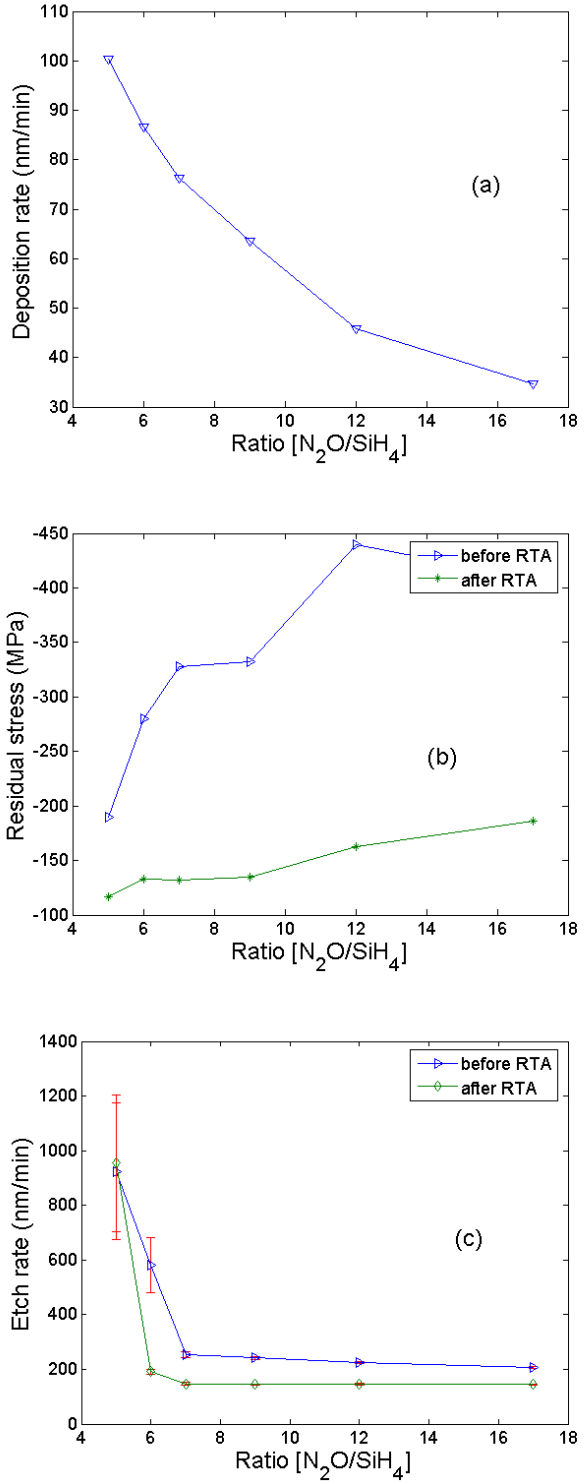


Figure 7.5: Figures of merit as a function of $[N_2O/SiH_4]$ the precursor gases ratio: (a) deposition rate, (b) residual stress, and (c) BHF etch rate.

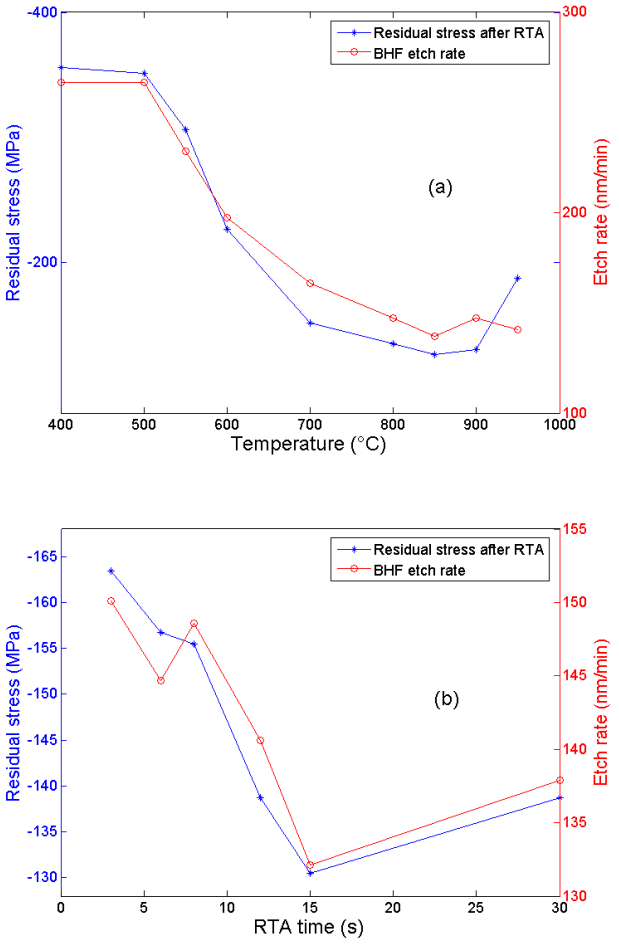


Figure 7.6: Impact of RTA (a) temperature and (b) time on residual stress and BHF etch rate.

best properties that one can get for a given oxide. The etch rate and the residual stress do not change significantly above 900 °C. Although the measurements in Figure 7.6(b) are quite noisy, it appears that the RTA time has also an influence. The residual stress and the BHF etch rate reach their minimal value in 15 s, respectively, -130 MPa and 133 nm/min. Taking into account the measurement error, one can say that the etch rate and the residual stress do not vary any longer above 15 s. After conventional furnace annealing (30 min at 900 °C under nitrogen atmosphere) the residual stress reaches a value of -160 MPa and the BHF etch rate a value of 129 nm/min. It clearly appears that RTA is the best method to anneal a PECVD oxide. The gain in etch rate reduction is similar to the one got from conventional furnace annealing, the gain in stress reduction is even better and the thermal budget is fairly low and does not induce extra diffusion of doping atoms in the CMOS electronics, for instance. As will be shown in Section 7.4, the grain size increases during RTA whereas no clear trend can be drawn concerning the roughness evolution. Besides, the strong correlation between the residual stress and the BHF etch rate evokes stress-corrosion cracking mechanism, as a mechanical energy affects the chemical properties of the material [73].

7.5 Time evolution

As mentioned above, the properties of PECVD oxide films vary over time especially when it is not dense. Based on the experimental results presented in Section 7.3, the oxide film can be considered as not dense when it is deposited with high total gas flow, under low RF power or at low [N_2O/SiH_4] ratio (Si-rich oxide). To draw a quantitative estimation of that variation, the residual stress of a representative oxide film is measured with respect to the time elapsed after deposition and after RTA. This 1.5 μm-thick silicon oxide film is deposited with the recipe *OxideHiF* in Table 7.1.

After deposition, the stress increases in absolute value from -226 MPa to -357 MPa at a rate of 44 MPa/min decade, and saturates after around 700 min (Figure 7.7(a)). It is clear that the variation of the residual stress after deposition has an exponential behaviour. Hence, the time evolution of the stress after deposition should be described adequately by a function of the type:

$$\sigma = \sigma_\infty - K \cdot \exp\left(\frac{-t}{\tau}\right) \tag{7.5}$$

where $K = \sigma_\infty - \sigma_0$, σ_0 is the initial residual stress, σ_∞ its final value and τ a time constant.

In Figure 7.7(b), the residual stress is plotted with respect to the time elapsed after RTA. Two curves are presented in this figure: the curve (a) is related to a RTA treatment immediately applied after deposition, while the curve (b) corresponds to a sample for which the RTA is applied only 9 days after deposition. The RTA parameters are 950 °C during 20 s. According to these measurements, the time elapsed between the deposition and the RTA appears to have an essential influence on the final value of residual stress. The time delay results in a significant shift of the residual stress. The wafer annealed immediately after the deposition experiences a stress reduction from -226 MPa down to -56 MPa. The item annealed 9 days after deposition presents a stress change from -357 MPa to 39 MPa.

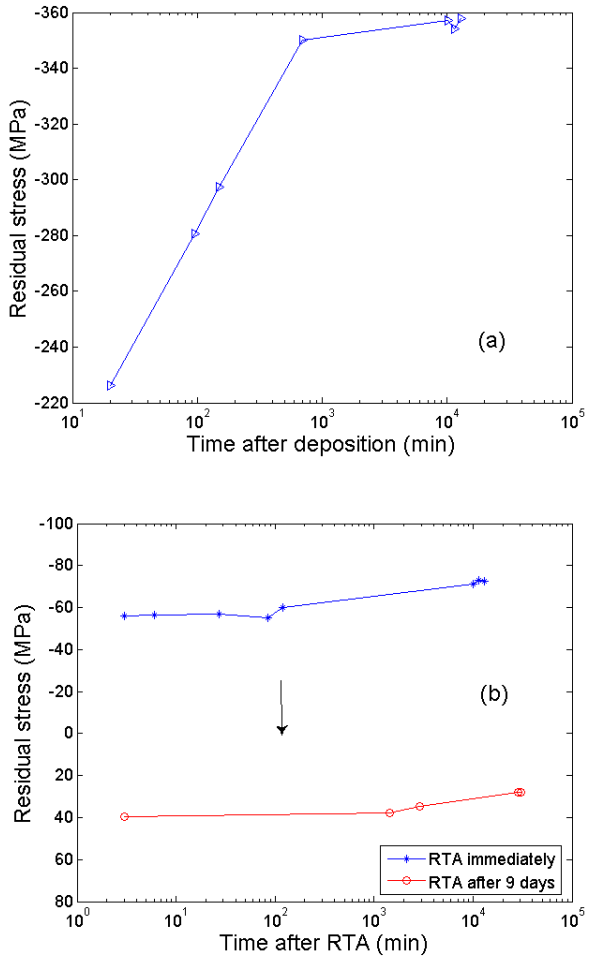


Figure 7.7: Residual stress as a function of (a) time after deposition and (b) time after RTA.

In this later case, the sign of the stress is inverted, evolving from compressive to tensile. The surprising point comes from the fact that the stress apparently increases spontaneously with time. In [71], we can find an interpretation of such variations. After deposition, weakly bonded $Si{-}O$ bonds of low dense oxides form silanol groups ($Si{-}OH$) by reaction with the ambient moisture. The effect of the thermal treatment is to reconstruct the $Si-O$ bonds but in a minimized stress configuration. We can suppose that after thermal treatment the same mechanism of silanol groups formation occurs but from a lower energy state, slowing down drastically the reaction.

7.6 Roughness measurement

Besides wafer bow considerations, it is essential to characterize the surface microroughness of oxide samples, candidates to wafer bonding. Indeed, the direct bonding mechanisms are very sensitive to this micron-scale parameter. According to [9], a surface roughness below 5 Å root mean square (RMS) is necessary to achieve direct wafer bonding. Therefore, various PECVD oxide films are scanned by an Atomic Force Microscope (AFM) on $1\,\mu\text{m} \times 1\,\mu\text{m}$ areas to evaluate their surface roughness.

7.6.1 As deposited oxides

AFM measurements are performed on four different PECVD oxides. The recipes are the standard pivot one coming from Oxford Instruments (referred as *OxideStd* in Table 7.1) and three other recipes directly derived from this first recipe. For each of them a characteristic parameter is varied in the stress relaxation direction: lower RF power (OxideLoP), lower $[N_2O/SiH_4]$ ratio i.e. silicon-rich (OxideLoR), higher precursor gas flow (OxideHiF).

Table 7.2 shows the average and RMS roughness for the different oxide recipes before and after RTA. As previously stated, a low $\eta P/F$ ratio yields an oxide with weakly bonded atoms, larger grains and voids. The roughness measurement confirms this fact: the densest oxide film (OxideStd) exhibits the lowest surface roughness of 35.6 Å RMS while lower stressed oxide recipes yield higher roughness films. Although it is a powerful technique to reduce the intrinsic stress, RTA does not help to lower the surface roughness. With OxideHiF recipe, RTA increases significantly the roughness from 45.2 to 53.6 Å RMS. At contrary, with other tested recipes, the variation is not clear and amounts to about 1 Å beyond or below the initial value. Nevertheless, it is obvious that in all cases the surface roughness of the PECVD oxides does not permit to proceed to a wafer bonding without a surface polishing.

7.6.2 After CMP

CMP experiments are conducted in order to obtain smoother surfaces. The process parameters are adjusted using the oxide recipe referred as *OxideILD* in Table 7.1. Thanks to its higher concentration in nitrogen, this oxide has better electrical properties [10] and is naturally used as interlayer dielectric.

Table 7.3 presents the results of the CMP tuning experiments. The film thickness standard deviation gives an estimation of the material removal uniformity. Based on this table, the following remarks can be formulated. First, the removal rate and the uniformity

Recipe name	RMS roughness before RTA (Å)	RMS roughness after RTA (Å)
OxideStd	35.6	34.4
OxideHiF	45.2	53.6
OxideLoP	40.7	39.2
OxideLoR	38.6	39.9

Table 7.2: Surface roughness before and after RTA for various oxide deposition recipes.

are both strongly dependent on the rotational speed. Hence, in order to keep the oxide film thickness as much uniform as possible it appears being suitable to work at the low speed of 50 rpm in our tests. Secondly, the pad type plays a determinant role on the roughness evolution: the LDR type pad results in a roughness strongly dependent on the rotational speed, while the PUR type pad gives almost steady roughness values with all tested parameters combinations. This RMS value is comprised between 3.31 and 3.84 Å and is compatible with direct wafer bonding. Consequently, a hard polishing pad like the PUR type comes out as the best option in order to reduce the oxide film roughness while limiting the material removal and its nonuniformity. Then, in accordance with the CMP results, all wafers prepared for wafer bonding are polished with the following parameters: hard pad PUR A1 type, slurry dispensed at 75 ml/min, table/head rotation speed of, respectively, 50/51 rpm, head pressure of 0.5 bar, and 2 min polishing time. The polishing is followed by a rinsing and a scrubbing stage.

Pad Type	Speed table/head (rpm)	Head pressure (bar)	Slurry flow (ml/min)	Removal rate (nm/min)	Thickness std dev (nm)	Roughness		
						Rmax (Å)	RMS (Å)	Ra (Å)
LDR	50/51	0.25	75	149	32	126.0	5.04	3.81
	60/61	0.8	125	284	51	43.6	4.15	3.15
	80/81	0.5	100	326	55	27.8	2.71	2.07
PUR	50/51	0.5	100	82	32	30.4	3.31	2.61
	60/61	0.25	125	140	52	38.8	3.84	3.00
	80/81	0.8	75	283	57	33.6	3.59	2.80

Table 7.3: Figures of merit for CMP process step according to process parameters.

Finally, although it is well established in the literature that the wafer curvature can play a role in the removal uniformity during the polishing [174] and [179], the material removal mapping of our polished samples shows that oxide is not faster removed at the center than near the edge during CMP, even with a 45 μm-bow sample.

7.7 Bondability

In order to illustrate the importance of considering the wafer's bow in microfabrication, and thus the residual stress in the oxide layer, we perform wafer bonding tests with various oxide recipes and film thicknesses. Indeed, during silicon wafer bonding, each wafer of the pair is elastically deformed to achieve conformity of the surfaces. During this process, the work of adhesion, which is equal to twice the surface energy, must be sufficient to enable the elastic deformation of the wafers, bringing their surfaces into contact. This criterion can be rewritten as:

$$W \geq \frac{dU_E}{dA}, \tag{7.6}$$

where W is the work of adhesion, U_E is the elastic energy accumulated in the wafers as they conform one to another, A is the area of created interface. The term dU_E/dA, the strain energy accumulation rate, is a function of the wafer profile and the substrate mechanical properties. Bonding two silicon wafers having opposite bowing as sketched in Figure 7.8 implies the storage of high elastic strain energy in the wafers. According to [167], the amount of elastic energy accumulated by the deformation of the wafers when they are brought into contact can be evaluated with the following relation:

$$\frac{dU_E}{dA} = \frac{1}{24} E h_1^3 \left(\frac{1+\nu}{1-\nu}\right) \left[\frac{(\kappa_2 - \kappa_1)^2}{1+\eta^3}\right], \tag{7.7}$$

where E is the Young's modulus of silicon, h_1 is the thickness of the thinnest wafer, ν is the Poisson's ratio of silicon, κ_1 and κ_2 are the curvatures of the wafers and $\eta = h_1/h_2$. The curvature κ is the inverse of the curvature radius and $\kappa_1 = -\kappa_2$ in the case illustrated in Figure 7.8. Corresponding to bows from 3 μm to 30 μm, the typical curvature of silicon 3-inch wafers is on the order of 0.01 - 0.1 m^{-1}. Hence, the strain energy accumulation rate, dU_E/dA, ranges from 0.15 to 15 mJ/m^2 when both bonded wafers are 30 μm bowed. Direct wafer bonding can thus occur at room temperature if the surface energy is greater than half of dU_E/dA. In addition, from Turner et al. in [166] we know that the bond front wave is instable on plain wafers. If the bonding criterion (7.6) is satisfied, the bond front wave propagates from the center until the edge. Otherwise, it does not progress at all due to a too high bow, preventing any bonding to take place. At the opposite, when a crack propagates at the interface by the insertion of a wedge, the stored elastic energy facilitates the crack propagation and contributes to decrease the overall toughness of the same quantity.

Practically, three recipes of PECVD oxides are selected for wafer bonding tests: OxideILD, OxideTO and OxideHiF referred in Table 7.1. These recipes are chosen for the following reasons. OxideILD has a high residual stress of -140 MPa after RTA, a low BHF etch rate (169 nm/min) and is used as interlayer dielectric. OxideTO is a good trade-off between low residual stress (-90 MPa after RTA), slow BHF etch rate (166 nm/min) and time stability. OxideHiF can achieve null stress with good time stability after RTA, as it is shown in Figure 7.7. Its BHF etch rate is 800 nm/min after RTA.

After the PECVD oxide deposition, the samples are polished according to the recipe established in previous section (7.6). Then, all wafers are cleaned twice in a piranha

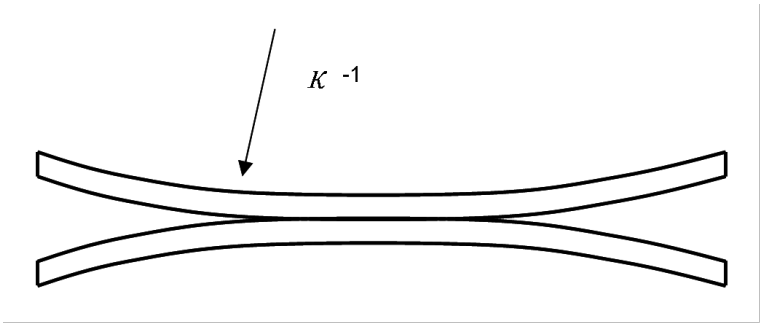


Figure 7.8: Schematic of the bonding process showing the bonding initiated from a central contact point.

solution (H_2SO_4:H_2O_2 = 5:2) at 110 °C during 10 min, each cleaning being followed by 10 min rinsing in DI (de-ionized) water. Immediately after the cleaning, they are spin-dried and manually brought into contact at room temperature and atmospheric pressure, forming PECVD SiO_2/Si assembled interfaces. After 24 h storage at room temperature, the wafers are annealed at 120 °C during 24 h in N_2 atmosphere, in order to enhance the bonding interface toughness [185].

The data of bonded wafer pairs are summarized in Tables 7.4 and 7.5. Except the 45 μm bowed wafer (Wafer#5), all polished samples enable direct wafer bonding. Hence, none of the selected oxide recipe is by-itself incompatible with hydrophilic silicon bonding. From the infrared images, the bonding interface quality is good and the limit between bonded and unbonded areas is clear. Voids caused by particles or trapped air between the joined surfaces do not enlarge during the annealing step, except for Wafer#4 for which large new voids appear. Two causes can explain these voids formation and enlargement. First, Wafer#4 is quite highly bowed. This bow weakens the interface toughness with an energy rate of 1.56 mJ/m^2. Hence, the interface can easily be debonded by gaseous H_2 or H_2O produced by the bonding reaction [186]. Second, although the annealing temperature is much lower than the deposition temperature, this can originate from a film degassing due to the absence of RTA treatment on this sample [136]. At contrary, on other samples the voids tend to disappear during the annealing.

It is worth noting that the measured surface energies of Wafer#1, #2 and #3 range from 320 to 140 mJ/m^2 after annealing, inversely varying with the stored elastic energy that ranges from 0.09 to 0.92 mJ/m^2. This observation let us consider that the strain energy accumulation rate, and thus internal stress in the oxide, is limitative on the possibility of assembling wafers as well as it may influence the final surface energy value. If needed, one can expect to enhance these resulting surface energies by performing a surface activation with oxygen plasma for instance or by increasing the post bonding annealing temperature. Besides, the accumulation of strain energy rate when joining a 45 μm bowed wafer with PECVD oxide on top and an almost flat silicon wafer is equal to 5.85 mJ/m^2. From our experiments, as direct bonding does not occur with wafer#5, the energy rate is in that case larger than the initial interface toughness. This brings by the way an upper estimation of the adhesion work at room temperature for a PECVD $SiO_2 - Si$ bonding interface. As the

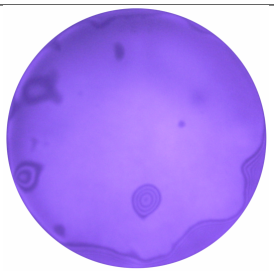
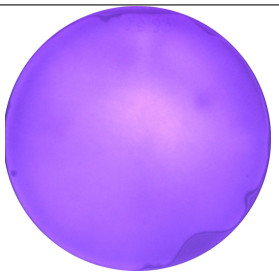
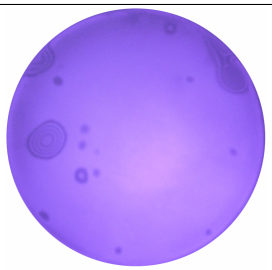
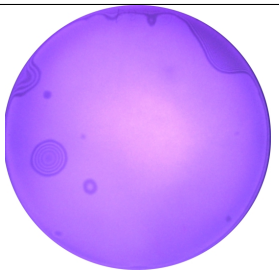
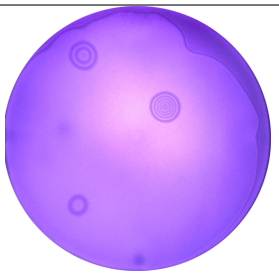
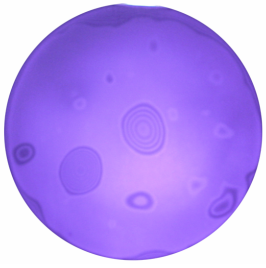
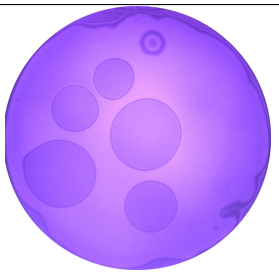
Wafers	Image before annealing	Image after annealing
Wafer#1		
Wafer#2		
Wafer#3		
Wafer#4		
Wafer#5		No Bonding

Table 7.4: Infrared pictures of wafer bonded samples.

Wafer reference	Oxide recipe reference	Film thickness (μm)	RTA 900 °C 15 s	Oxidized wafer bow* (μm)	Silicon wafer bow* (μm)	dU_E/dA (mJ/m^2)	γ after annealing (mJ/m^2)
Wafer#1	OxideHiF	1.5	Yes	4.3	-10.0	0.088	320
Wafer#2	OxideTO	1.5	Yes	4.8	2.9	0.160	290
Wafer#3	OxideILD	1.5	Yes	19.0	-0.6	0.916	140
Wafer#4	OxideILD	1.5	No	32.1	-8.1	1.560	160
Wafer#5	OxideHiF	2.7	No	45.2	1.3	5.850	-

Table 7.5: Mechanical data of wafer bonded samples, (*) wafers bows are measured prior to bonding.

work of adhesion varies rapidly with time [67], this estimated quantity reflects the instant surface energy when the surfaces are brought into contact. For comparison purpose, the surface energy value obtained by Tong and Gösele in [162] is about 59 mJ/m^2 for Si-SiO_2 interface with a thermally grown oxide and hydrophilic Si interface. The first elements explaining such substantial difference observed are (i) the surface roughness which reduces the surface area directly in contact at the bonding interface, (ii) the cleaning procedure may differ, leading to different density of bonding species and (iii) the dynamics of the bonding, i.e. the delay time between the cleaning and the bonding but, also and more importantly, the time elapsed before the surface energy measurement.

7.8 Conclusions

The scope of this chapter was to consider the use of PECVD oxide as intermediate layer in direct wafer bonding. For that purpose, a detailed analysis has been conducted in order to reduce the internal stress of PECVD oxide film by adjusting the main deposition parameters and by the use of thermal treatments. From the basis of a standard oxide recipe, films deposited with higher precursor gas flow (over 800 sccm), lower RF power (below 35 W) or with a [N_2O/SiH_4] ratio lower than five are particularly adequate to produce lowly stressed oxide films. However, lowering residual stress by increasing the gas flow or reducing the RF power is inevitably accompanied by an increase of etch rate in BHF. From these observations and with the use of RTA, very low compressive, stress free or lowly tensile oxide films can be obtained. RTA has proven to be the most efficient at a temperature over 900 °C and duration of 15 s to reduce the PECVD oxide film stress as well as the BHF etch rate and to enhance its long term stability by reorganizing the deposited film.

In order to enable the bondability of deposited oxide thin films, a CMP procedure was set-up. Hard polishing pad gives the lowest surface roughness with a limited oxide thickness removal.

Wafer bonding of prepared PECVD oxide films were successfully conducted with representative oxide recipes. Bonded samples showed that the resulting surface energy, after a low temperature annealing, tends to vary inversely with the elastic energy accumulated

by the conformation of the wafers during the direct bonding. About 45 μm wafer bow comes out as an upper bow limit, preventing direct bonding to occur. As a corollary, this limit gives an upper estimation of the instant work of adhesion when PECVD $SiO_2 - Si$ surfaces are brought into contact. All those experimental results highlight the importance of monitoring the residual stress in intermediate oxide layers to assure high quality and reliable bonding and thus technological routes for successful 3D integration.

Chapter 8

Wafer Bonding of PECVD SiO_2 Enhanced by Ductile Layers Inserted near the Interface

8.1 Introduction

The work presented in this chapter was published with Yannick Bertholet as first author in Acta Materialia [21].

In microelectronics, ductile materials are used as interconnects between the different levels of microsystems (Al, Cu, AlCu, ...), as metal contacts (W, PtSi, PtSi2, ...) or as solder connections (PbSn alloys, ...). These ductile layers also affect the distribution of stresses into the systems when they are subjected to external or internal (residual stresses of various origins) loading. In this chapter, the effect of the presence of ductile layers close to the interface on the toughness of bonded wafers is investigated theoretically as well as experimentally. In that frame, a canonical configuration is studied: metallic planes are buried under PECVD oxide films joined by direct wafer bonding.

8.2 Theoretical Approach

8.2.1 Basic principle

The resistance of an interface to the propagation of a crack under a pure opening mode is determined by two quantities: the fracture energy Γ_c (also frequently noted in the literature G_c) and the cohesive strength σ_c. Fracture occurs if the energy that the system can provide (release) to the interface crack, the so-called energy release rate G, is larger than Γ_c and if the local stress next to the crack tip σ is larger than the critical strength σ_c. In a perfectly elastic system, i.e. in the absence of relaxation mechanisms such as plastic flow, the critical strength condition is always satisfied because of the high stress concentration at the sharp crack tip. The fracture energy Γ_c is then equal to the adhesion energy Γ_0 which is almost equal to two times the surface energy $2\gamma_S$ (it is not "exactly equal" to $2\gamma_S$ because of surface reconstruction and lattice trapping effects [103]). When

dissipative phenomena take place during the cracking process, an extra contribution to the fracture energy, noted Γ_p, adds to the work of adhesion:

$$\Gamma_c = \Gamma_0 + \Gamma_p. \tag{8.1}$$

As Γ_p is a non-linear complex function of Γ_0, σ_c among other geometrical parameters [44, 57, 152, 171], the influence of the ductile interlayer was computed with a steady-state finite element method based on a multiscale modelling strategy, by Dr. Yannick Bertholet [21], inspired by Wei and Hutchinson [175].

8.2.1.1 Multiscale modelling of the problem

Figure 8.1 depicts how the problem was strategically decomposed in a multiscale model. From a macroscopic situation of debonding, the micron-scale layers constituting the system are:

1. a thick elastic substrate of thickness h_s, characterized by an isotropic linear elastic behaviour with Young's modulus E, and Poisson ratio ν;
2. a thin layer of metallic material (e.g. Cu, Al, Ti, ...) of thickness h_p, deposited on the substrate. The layer will dissipate energy by heat generation through dislocation generation and glide. The isotropic J_2 flow theory is used to represent the multiaxial plastic response of the layer. The mechanical behaviour is fully characterized by the stress strain response given in Figure 8.1 with Young's modulus E_p, Poisson ratio ν_p, yield strength σ_0 and strain hardening exponent n;
3. a thin layer of elastic materials of thickness he deposited on top of the metallic layers. For the sake of limiting the number of parameters of the model, the mechanical properties of the elastic layer are taken, here, equal to those of the substrate (i.e. E and ν).

At the nanoscale, the interface between the two multilayers is characterized by a traction-separation law (see Figure 8.1) which relates the normal stress σ to the normal displacement δ and which is characterized by the work of adhesion, Γ_0 and a peak stress σ_c [23, 30, 57, 116, 120, 168, 175, 180]. Recently, density functional theory based ab-initio calculations have been used to determine traction separation laws for purely brittle cleavage fracture such as envisioned here [46]. For pure cleavage "atomic separation" phenomena, one expects theoretical fracture energies and critical strengths in the range $\Gamma_0 \approx 1$ J/m^2 and $\sigma_c \approx$ 5-10 GPa [57, 88, 137]. A wedge is inserted in order to propagate a crack along the interface. Dimensional analysis leads to the following dependence of the fracture energy in the parameters of the model

$$\frac{\Gamma_c}{\Gamma_0} = F\left(\frac{\sigma_c}{\sigma_0}, \frac{R_0}{h_e}, \frac{E}{\sigma_0}, n, \frac{h_e}{h_p}, \frac{E}{E_p}, \nu, \nu_p\right) \tag{8.2}$$

where R_0, defined as

$$R_0 = \frac{E}{3\pi\left(1-\nu^2\right)}\frac{\Gamma_0}{\sigma_0^2}, \tag{8.3}$$

is an estimate of the size of the inelastic zone (it is the size of the zone where the condition for plasticity is satisfied if the interlayer is infinitely thick).

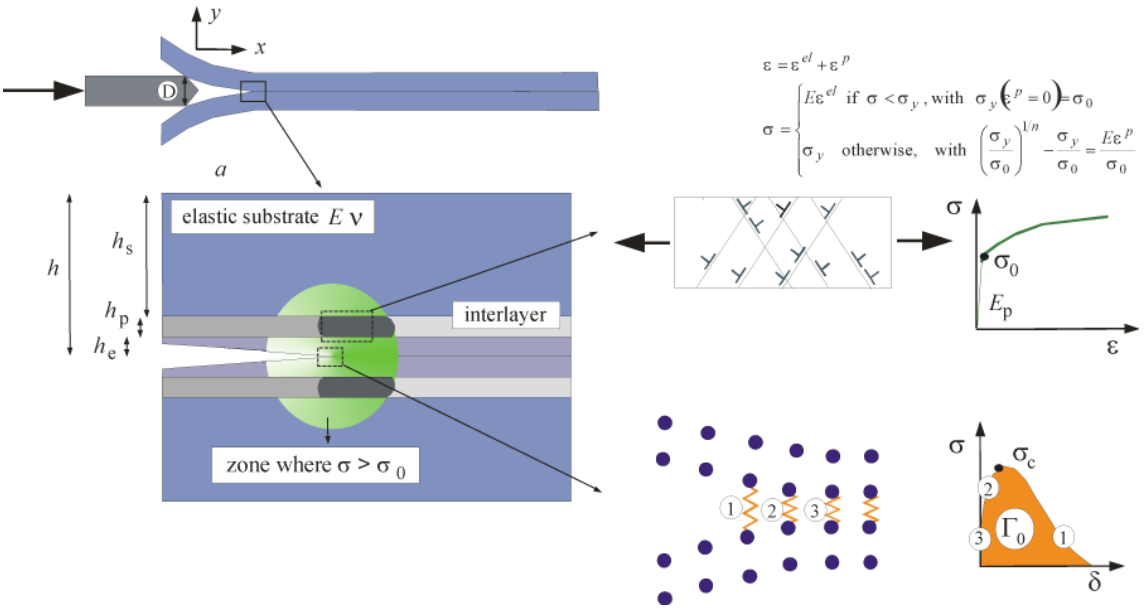


Figure 8.1: Description of the multiscale problem. The macroscopic scale (> 1 mm) sketch is the typical geometry and loading configuration used to estimate the interface fracture energy. The first level window around the crack tip depicts the microscale problem (≈ 1-5 μm), involving the interface between two thin elastic layers (h_e ≈ 50-500 nm) obtained by molecular bonding, the ductile interlayers (h_p ≈ 100-2000 nm) on both sides of the elastic layers and the zone of large stresses surrounding the crack tip. The stresses can be predicted quite accurately within the thin elastic layer using linear elastic behaviour and linear elastic fracture mechanics concepts except very near the crack tip within a zone of typically 5 atomic spacings. In that nanoscale zone (1-3 nm) shown on the right, the modelling of the non linear effects related to the large distortion and atomic plane separation requires the introduction of a traction-separation law. The response of the metallic interlayer under stresses larger than the yield stress lead to plastic deformation and strain hardening mechanism related to the generation and gliding of dislocations along the slip systems. A typical stress strain response is shown. *Bertholet et al. [21].*

8.2.1.2 Numerical procedures

This complex multiscale boundary value problem was solved with the finite element method using an efficient steady state formulation. Assuming that the crack (see Figure 8.1) is growing in the x direction, any rate quantity can be related to the x spatial derivative through the crack velocity. An iterative finite element solution procedure for this specific kind of steady state problem has been initially proposed by Dean and Hutchinson [45] to address various bulk and interface crack configurations. The formulation consists of finding an equilibrium solution for the displacements based on a previous approximate distribution of plastic strains in the ductile interlayer and then integrating the plasticity laws along streamlines to determine new approximations for stresses and plastic strains. This procedure is repeated until convergence is achieved. Since the test is symmetrical (see Figure 8.1), only half of the sample needs to be analyzed. Plane strain conditions are assumed. The wedge is modeled with a fixed boundary condition at a normalized distance from the plane of symmetry. Extremely fine meshes are required near the crack tip between the two elastic layers to properly resolve the fracture process taking place at the nano-scale and involving very small displacements. Very fine meshes are also needed within the ductile interlayer to get converged solutions. Note that the analysis of the limit problem of a very thick ductile layer has been already provided by Wei and Hutchinson [175].

8.2.1.3 Results of the model

A selection of results of the parametric study performed with the model presented above is proposed and discussed in this section in order to enlighten the complex couplings between the interface fracture response, mechanical properties of the interlayers and geometry. Figure 8.2 shows the evolution of the fracture energy σ_c/σ_0 (normalized by the work of adhesion) as a function of the cohesive strength σ_c/σ_0 (normalized by the yield strength of the interlayer) for various R_0/h_e and a fixed thickness ratio $h_p/h_e = 10$. The other parameters are taken constant: $E_p/\sigma_0 = 1300$, $E/E_p = 3$, $n = 0.1$, $\nu = \nu_p = 0.3$, typical of an aluminium interlayer inserted in between Si layers. First, the cohesive strength must be sufficiently large for allowing the stress in the interlayer to reach the yielding condition. If σ_c/σ_0 is lower than $3.5\sigma_0$, plastic dissipation is absent or negligible, in agreement with other analyses in the literature performed on systems involving crack propagation in plastically deforming materials [57, 168, 175]. Interfaces between elastic materials will usually lead to σ_c larger than several GPa while σ_0 is usually smaller than 500 MPa depending on the material, alloying elements, thickness and grain size [59]. Most systems will thus meet that constraint. Secondly, plastic dissipation takes place if the elastic layer thickness is sufficiently smaller than the size of the zone involving large stresses. Significant improvement of the fracture energy will take place only if $R_0/h_e > 2.5$ - 3.

Figure 8.3 shows the evolution of Γ_c/Γ_0 as a function of the inelastic zone size estimate R_0/h_e for various h_p/h_e and $\sigma_c/\sigma_0 > 1$. As expected, the fracture energy increases with increasing interlayer thickness: a ratio $h_p/h_e > 1$ is necessary to provide significant fracture energy enhancement for the present set of parameters. An optimum R_0/h_e is predicted (see also Figure 8.2) and this optimum increases with increasing interlayer thickness (a larger inelastic zone size is necessary to fully encompass a thicker interlayer). The reason for the presence of an optimum in the fracture energy evolution rather than a monotonously

growing value when increasing R_0/h_e is the following. For a given elastic layer (E and h_e are fixed) and a constant σ_c/σ_0 ratio, an increase of R_0 is equivalent to an increase of Γ_0/σ_0. As a first approximation, the dissipation Γ_p is equal to the product of $R_p\epsilon\sigma_0$ where R_p is the height of the plastic zone in the interlayer and ϵ is the average plastic strain in the interlayer. When R_0 is large enough, R_p is equal to h_p (see the sketches in Figure 8.2). The full interlayer yields plasticity and a regime of uniaxial deformation develops because of plastic incompressibility. Due to this high constraint, the apparent hardening rate remains very high, and the plastic strain remain approximately proportional to the stress, which is proportional to the square root of the energy release rate (as predicted by basic fracture mechanics argument). Scaling equation 8.1 by Γ_0 leads thus to

$$\frac{\Gamma_c}{\Gamma_0} = 1 + \frac{\Gamma_p}{\Gamma_0} = 1 + \frac{k\epsilon h_p \sigma_0}{\Gamma_0} = 1 + \frac{k h_p \sigma_0}{\sqrt{\Gamma_0}} \tag{8.4}$$

where k is a parameter of order one. Hence increasing even more R_0, i.e. increasing Γ_0/σ_0, leads to a decrease of Γ_c.

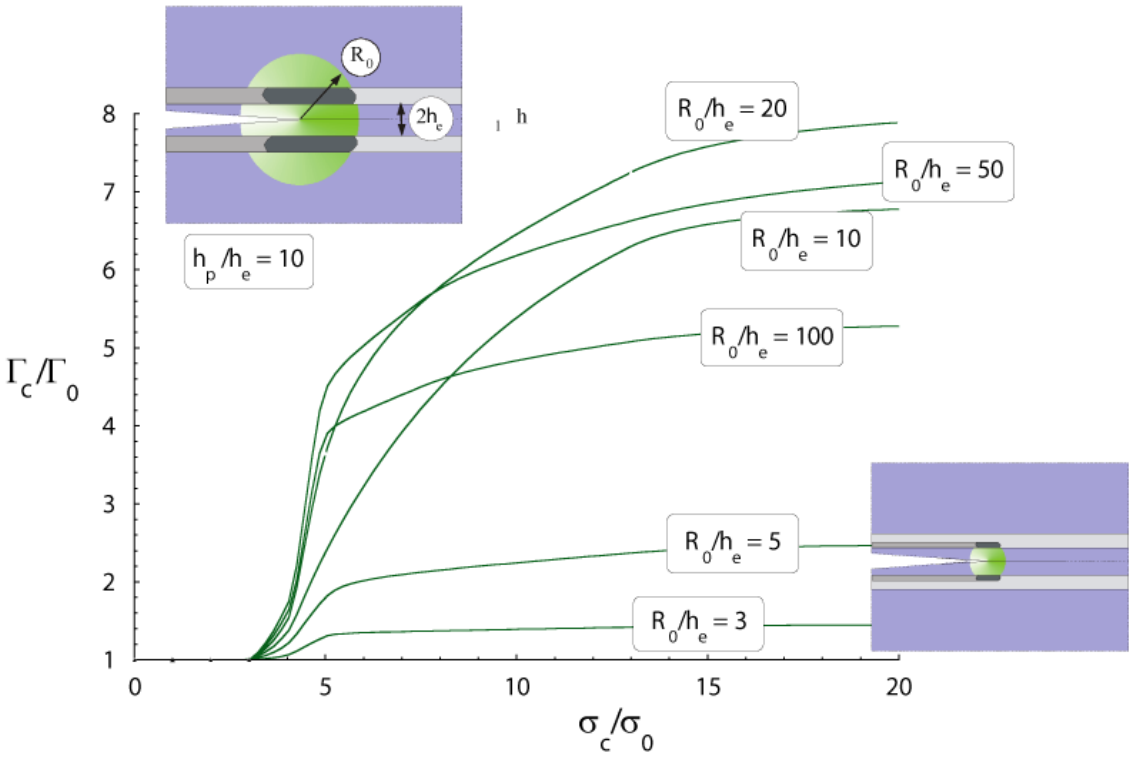


Figure 8.2: Fracture energy predictions by the multiscale model, variation of the fracture energy Γ_c/Γ_0 (normalized by the work of adhesion) as a function of the cohesive strength σ_c/σ_0 (normalized by the yield stress of the interlayer material) for different values of normalized "large stress zone" R_0/h_e and $h_p/h_e = 10$. *Bertholet et al. [21].*

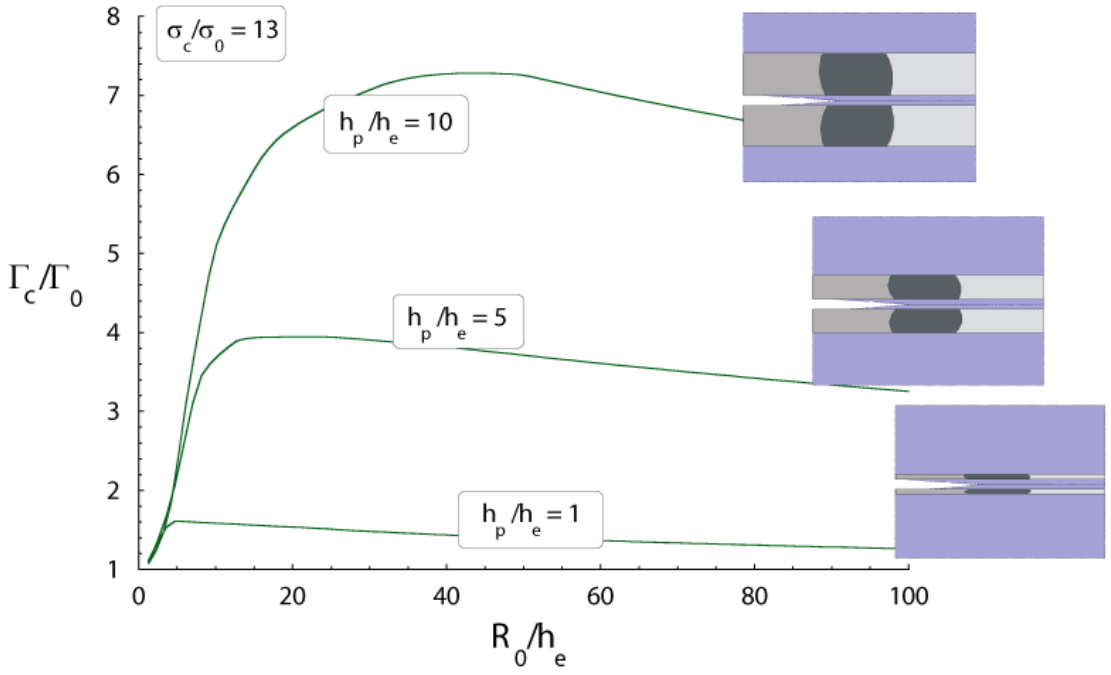


Figure 8.3: Fracture energy predictions by the multiscale model, variation of the fracture energy Γ_c/Γ_0 (normalized by the work of adhesion) as a function of R_0/h_e for different interlayer thicknesses h_p/h_e and $\sigma_c/\sigma_0 = 13$. All calculations were performed with $E_p/\sigma_0 = 1300$, $E/E_p = 3$, $n = 0.1$, $\nu = \nu_p = 0.3$. *Bertholet et al. [21].*

8.3 Experimental Demonstration

8.3.1 Materials and processing

In order to verify experimentally these theoretical predictions, multilayer structures were prepared from 380 μm thick silicon wafers covered, or not, by a 1 μm thick pure Al layer and by a 330 nm thick PECVD SiO_2 film.

Samples fabrication The 3 inch, p-type, <100> one side polished commercially available silicon wafers were first cleaned twice in a RCA-like solution (H_2SO_4:H_2O_2 = 5:2) at 110 °C during 10 minutes, each cleaning was followed by 10 minutes rinsing in DI (deionized) water. A 1 μm thick aluminium layer was evaporated in an e-gun Variant on a few wafers, before depositing 500 nm of PECVD oxide in an Oxford Plasmalab System100. On other wafers, an identical oxide was directly deposited after cleaning. The wafers were then annealed at 120 °C during 24 hours. This operation improves molecular bonding by preventing the PECVD oxide to release gaseous impurities during the post-bonding heat treatment. Both wafers pairs were surface polished by CMP (Chemo-Mechanical Polishing) in order also to enhance adhesion. Before polishing, the samples exhibited a RMS surface roughness of 6.27 nm and 1.40 nm, respectively with and without aluminium layer. The roughness was measured by atomic force microscopy and computed from 1 μm x 1 μm scanned areas. After polishing, the roughness was reduced to 0.30 nm and 0.27 nm, respectively. In the meantime, the oxide layer thickness was reduced down to 330 nm.

Wafer bonding The wafers were cleaned again and activated before bonding. The cleaning consisted of an immersion in concentrated nitric acid (70%) during 3 minutes, in order to remove all organic contaminants, before rinsing in DI water. The surface activation was performed by oxygen plasma in an Oxford RIE chamber during 1 minute with the following parameters: 100 sccm O_2 flow, 90 mTorr chamber pressure, about 300 V DC bias and 100 W RF power. Finally, the wafers were put in contact and bonded at room temperature under clean environment. The samples were finally annealed during 7 days at 120 °C under nitrogen atmosphere in order to favour the formation of Si-O-Si bonds.

Hence, exactly the same processing and bonding steps were applied on samples involving or not an interlayer.

8.3.2 Fracture tests method

The fracture energy Γ_c was measured using a wedge opening test method (e.g. [20, 145, 127]). Rectangular specimens of 10 mm width and 50 to 70 mm length were diced from bonded wafers. Only 4 to 5 measurable samples can be machined out of one bonded stack of wafers. The fracture tests were performed by inserting manually a thin razor blade along the interface between the two multilayers. Two different razor blades were used with thicknesses, measured by SEM, equal to 100 and 230 μm, respectively. The out of plane displacements under loading were measured using a Dektak profilometer. The elastic beam bending solution

$$\frac{D}{4}\left(2-3\frac{x}{a}+\frac{x^3}{a^3}\right)=u_y\left(x\right) \tag{8.5}$$

relates the crack length a, the displacement uy and wedge thickness D along the x-axis, with the origin of the x-axis located at contact point of the wedge with the beam. The crack length is obtained by performing a least square fit of the experimental data point using expression 8.5. Almost perfect fitting with regression coefficient $R > 0.999$ is observed for all experiments. The robustness of the method comes from that the overall behaviour of the system is linear elastic and that the displacement are very small, avoiding the perturbation of the anti-clastic effect (transverse curvature under beam bending) [145]. The fracture energy Γ_c is obtained from the value of the energy release rate which, for the elastic double cantilever beam geometry used here, writes

$$G=\frac{3ED^2h^3}{16a^4\left(1-\nu^2\right)} \tag{8.6}$$

where h is the total thickness of the arm, i.e. in the present context $h = h_s + h_p + h_e$. An average value of the fracture energy is obtained by repeating several times the measurements for each samples.

In the case of the multilayers without the Al interlayers, the crack length can be measured directly owing to the IR transparency of Si [135, 162, 127]. This method has been described elsewhere and provided here a consistency check for the indirect measurement based on equation 8.5.

8.3.3 Experimental results and discussion

All the fracture energy measurements are gathered in Figure 8.4. The plain circles belong to measurements performed on 6 specimens with interlayers and 6 specimens without interlayers. For each type of configuration, 3 specimens were tested with the thin wedge (D = 100 μm) and three specimens were tested with the thicker wedge (D = 230 μm). At least 2 different measurements corresponding to two different positions of the wedge along the interface were performed for each specimen. The open circles correspond to supplementary tests performed with the instrumented wedge opening test and the direct measurement of the crack length [20], which can only be made on transparent samples (i.e. without interlayers). In that case, one open circle corresponds to a mean value of crack length measurements performed at typically 15 or 20 different positions of the wedge. Hence, these results give an idea of the dispersion in the bonding quality among specimens. The experimental scatter is essentially caused by large scale bonding inhomogeneities at the level of the full wafers which leads to differences among specimens and sometimes within single specimens. Fracture surface analysis by x-ray diffraction and atomic force microscopy has confirmed that fracture always occurs along the bonded interface.

The average fracture energy in the absence of interlayer, i.e. $\Gamma_c = \Gamma_0$, is equal to 2.1 J/m^2. The value is quite high for PECVD SiO_2/PECVD SiO_2 interfaces [102, 176], owing to the very long thermal treatment. The average fracture energy in the presence of the 1 μm thick Al interlayer on both sides of the elastic layers is equal to 3.5 J/m^2 which means an increase by 67% when compared to Γ_0. Using E = 90 GPa for SiO_2,

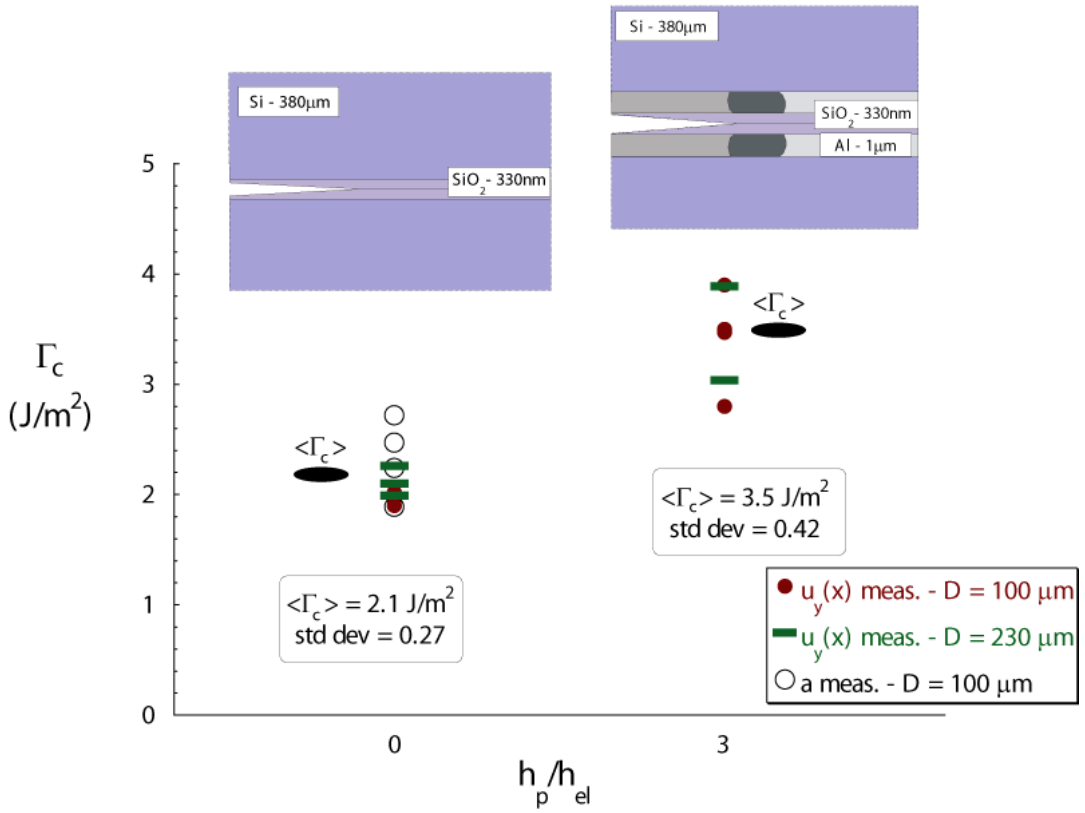


Figure 8.4: Fracture energy measurements with and without a dissipative interlayer. The average fracture energy for an interface between two layers of thermal SiO_2 layers grown on a Si wafer is equal to 2.1 J/m^2. Three types of measurements were made for generating and cross checking this value. If a 1 μm Al layer is inserted in between the Si wafer and the SiO_2 layer, the average fracture energy raises up to 3.5 J/m^2. *Bertholet et al. [21].*

$E_p = 70$ GPa, $\sigma_0 = 100$ MPa (a reasonable value for a 1 μm thick pure Al layer [45]) and $\Gamma_0 = 2.1$ J/m^2 leads to $R_0/h_e \approx 5$. Figure 8.2 shows that Γ_c/Γ_0 is not very dependent on σ_c. By considering the ratio $h_p/h_e = 3$, Figure 8.3 shows that the model predicts a value of Γ_c/Γ_0 lower than 2 in agreement with the experimental results.

This result lets us think that the interface strength σ_c is at least larger than 3-4 σ_c otherwise plastic dissipation would not occur, see Figure 8.2. This level of stress is necessary to allow plastic flow in the highly constrained near crack tip region, see also [102, 168, 176, 175]. This result has to be contrasted with the efforts made in the molecular bonding community over the last 2 decades to extract interface strengths using various tensile test configurations (see [127] for a recent review). Even when reducing the bonded area, these tests always lead to interface strength smaller than typically 50 to 80 MPa and usually much smaller. Such kind of tests obviously provide overall interface strengths controlled by the size of the largest bonding defect, and thus dependent on the size of the bonded area. The present concept of introducing a thin dissipative interlayer, although very time consuming, can thus be seen also as a method for identifying through inverse modelling the "intrinsic" interface strength.

8.4 Discussion and Conclusions

In this chapter, the interest of inserting thin dissipative layers to shield interfaces obtained by wafer bonding was theoretically demonstrated and experimental results are in accordance with simulated predictions. Moreover, from the results of the model, fracture energies equal to 5 to 10 times the interface intrinsic toughness Γ_0 can be expected when combining thin elastic layers and thick low-strength dissipative layers. Note, however, that the present model does not account for size effects related to thin plastically deforming layer [59] which provide a source of additional hardening and which would tend to mitigate the potential fracture energy enhancement. Calculations (not reported here) performed with higher strain hardening exponents showed a decrease of the attainable fracture energy. More advanced strain gradient plasticity theory or dislocation dynamics approaches would provide more accurate description of the plastic response in these very thin layers [57, 121, 176, 181].

From a technological viewpoint, inserting dissipative ductile interlayers could be used in many different applications requiring enhanced adhesion, on small or large bonded areas. Wafer bonding was the main motivation for this work because it is frequently a limiting step in nano- and microfabrication. But, as already used in some microelectronic applications, any type of interfaces, in multilayers or surface coatings, can be shielded whatever the origin of the weak interface toughness. Other dissipative media could be used such as polymers for instance. From a scientific point of view, the insertion of dissipative interlayers can also be seen as an indirect method for estimating, by inverse modeling, critical theoretical strengths of brittle interfaces.

Chapter 9

Thin Film Transfer Applied to the Fabrication of Multiple Gate MOS Transistors

9.1 Introduction

Thin film transfer is a fundamental process operation extensively studied, mainly for SOI wafers fabrication, through the revolutionary Smart-Cut process [13], or advanced strained SOI (sSOI) [65, 128]. One can mention also the work done at Queen's University for special substrates preparation including a buried tungsten silicide layer for integrating p-i-n diodes with low-loss coplanar wave-guide lines [63].

In the first part of this work (Chapter 3), the necessity of limiting the patterning is clearly evidenced. This fact is particularly true for the nitride film which stands as the mechanical core of the thin dielectric membrane because (i) it is the film with the highest Young Modulus as well as the highest fracture strength and (ii) it is the only material being in tensile stress, assuring the planarity of the membrane. Hence, as proven that spontaneous direct bonding of Si_3N_4 can be achieved [144], special SOI substrate preparation including a buried nitride film could be of great interest.

A second example of thin film transfer, presenting utmost interest in the frame of this work, concerns planar double-gate transistors fabrication. Indeed, double-gate devices constitute structures of first interest to be potentially implemented on thin dielectric membranes. Thanks to their bottom gate, a back-side control of the channel is applied, eliminating by the way any floating potential that could lead to drift effect appearance, as it is described in Chapter 4.

In this chapter, wafer bonding conditions are studied and optimized in the frame of an original planar double-gate transistors fabrication process.

9.2 Planar Double-Gate Concept

The growing interest of multiple gate (MuG) MOS devices is related to their superior electrical characteristics such as reduced short channel effects (SCE) compared to single

gate (SG) transistors which are becoming more and more important for MOS devices with channel length below 50 nm. Earlier, planar Gate-All-Around (GAA) SOI MOS devices have been fabricated by isotropically etching the buried oxide (BOX) to form a silicon bridge [41]. A major drawback of this technique is the limitation of the width to gate length (W/L) ratio to a value close to 1. In order to overcome this problem, fabrication of planar DG transistors by wafer bonding has been proposed [170]. The main advantages of this method are a) the flexibility to fabricate SG, DG as well as Silicon-on-Nothing transistors with the same process flow; b) the ability to define separate control for the top and bottom gates if needed; and c) the W/L ratio flexibility.

9.3 Main Fabrication Steps

The principle of the proposed fabrication process of DG structures is the transfer of a high quality thin silicon layer (coming from a SOI wafer) onto a thermally oxidized bulk silicon wafer presenting dry etched cavities into the oxide layer. The resulting structure is a thin suspended silicon layer above a cavity which corresponds to the future back gate. The main fabrication steps are presented in Figure 9.1. The fabrication process can be divided into two main parts: the preprocessing which is specific to the proposed planar DG process (Figure 9.1 (a)-(d)) and the standard CMOS process. In Figure 9.1 (a), the bulk silicon handle wafer is first thermally oxidized. Following this, the bottom gate cavities are patterned by sulphur hexafluoride (SF6) based RIE plasma. Next, a standard SOI wafer is bonded to the patterned thermal oxide of the bulk handle wafer. Before performing the bonding process, the surfaces of the wafers are treated accordingly to activate the surface and to remove any remnants of impurities. The wafers are manually bonded at room temperature and atmospheric pressure. After this, an annealing is performed to further strengthen the bonding and to remove any water contents from the bonded interface. Following this bonding step, the silicon substrate of the SOI wafer is removed using a grinding process followed by wet etch in a 10% TMAH (Tetra Methyl Ammonium Hydroxide) base solution as seen in Figure 9.1 (b) and (c). After the removal of the remainder of the silicon material, the buried oxide (BOX) layer of the SOI wafer is removed using buffered hydrofluoric acid (BHF) solution. The bonded wafer is checked once in a while until the layer becomes hydrophobic to water, which indicates the removal of all oxide materials. With the completion of these preprocessing steps, the bonded wafers are processed following the usual CMOS process steps. The silicon active islands are defined using reactive ion etching (RIE) as shown in Figure 9.1 (e). This is followed by the simultaneous thermal oxidation of the top and bottom gate and the filling of polysilicon by chemical vapor deposition (CVD) to form the bottom and top gates as shown in Figure 9.1 (g) and (h). Next, the polysilicon is doped using a flow of dopant gas where dopants diffuse into the polysilicon material. The alignment of the top and bottom gate corresponds to the standard capability of the available photolithography. During this critical step, the SOI layer is indeed thin enough to optically visualize and align the marks printed in the BOX, thus making this alignment process much easier. After this, the formation of the drain and source is made with ion implantations followed by the opening of the contact holes and finally metallization. The longitudinal cross-section and transversal cross-section of the final device is shown in Figure 9.1 (i) and Figure 9.1 (h) respectively. Figure 9.1 (j) shows a picture (top view) of a

final working planar DG device.

9.4 Thin Film Transfer

The thin film transfer constitutes a crucial part of this process for two main reasons. First, the yield in transistors production is directly correlated to the effective transferred surface area and has to be maximized. Second, the final transistors channels are made by the active Si film constituting small membranes at the end of the transfer process steps. Hence, preserving the integrity of these membranes is clearly essential.

9.4.1 Wafer Bonding Parameters

Surface Preparation. The wafers were cleaned in a SC1 solution (NH_3(28%):H_2O_2(30%):H_2O 1:4:20) at 60°C during 10 minutes and followed by 10 minutes rinsing in DI (de-ionized) water. We tested two types of surface activation: warm nitric acid dipping and oxygen plasma exposition. As observed during previous tests, oxygen plasma is not appropriate to activate SOI films because of the strong action of ions causing surface damages, reducing drastically the mobility of the carriers. Hence, all SOI wafers were activated with HNO_3 70% at 70°C during 15'. On the other hand, bulk wafers were activated alternatively with HNO_3 and O_2 plasma (5 pairs of each). The plasma activation was performed in the RIE chamber of an Oxford PlasmaLab System100 in the following conditions: 100 sccm O_2 flow, 90 mTorr chamber pressure, about 300 V DC bias, 100 W RF power and 5 s exposure time. Next, standard SOI wafers were manually bonded to the pre-etched and thermally oxidized handle wafers, at room temperature and atmospheric pressure.

Annealing. In order to strengthen the bonding energy, the wafers were annealed at atmospheric pressure and under nitrogen ambiance. We tested five different conditions covering all ranges of bonding mechanisms: 120°C, 2 hours ; 120°C, 144 hours ; 400°C, 3 hours ; 400°C, 95 hours and 1000°C, 10 hours.

9.4.2 Transfer Results and Discussion

The results were analyzed from two different points of view: a global observation of the surface and a close-up on the cavities.

9.4.2.1 Macroscopic Surface Analysis

Tables 9.2 and 9.1 present photographs taken along the transfer process steps, respectively for pure nitric acid activation and hybrid surface activation with oxygen plasma and nitric acid. Figures 9.2 and 9.3 expose the effective area loss for all wafers at each transfer step and give a mean to compare objectively the surface areas. These areas were extracted directly from the photographs of Tables 9.2 and 9.1 aided by image analysis software. In order to evaluate the surface energy at the bonding interface, the wafer bonding procedure was repeated with the same activation and annealing conditions on bulk samples with an identical oxide film and silicon interface. These results were calculated with steady-state

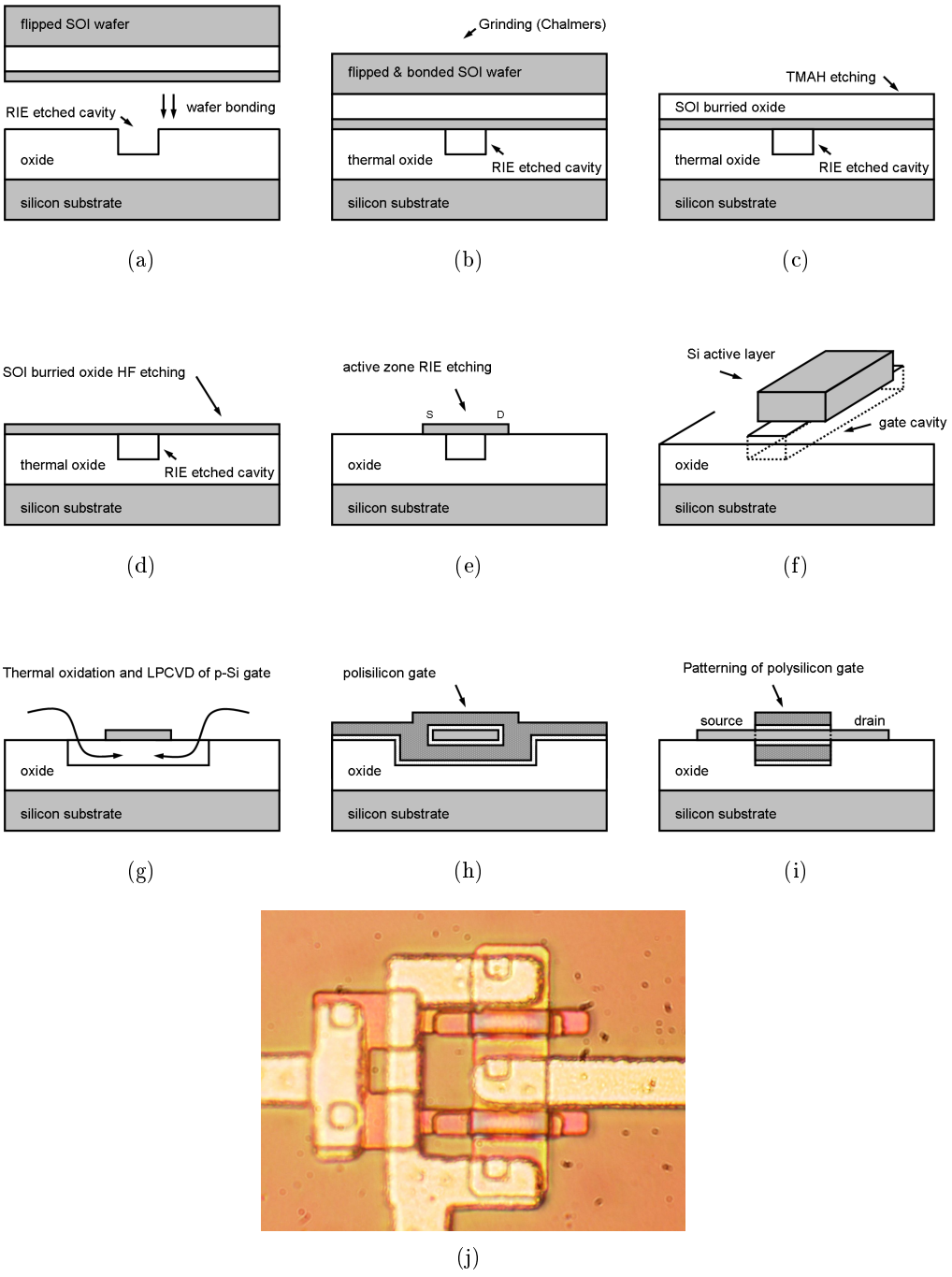


Figure 9.1: Main fabrication steps (a) Oxidation of handle silicon wafer, RIE etching and wafer bonding, (b) SOI substrate thinning via grinding, (c) LPCVD nitride deposition and TMAH etching, (d) BHF etching of SOI BOX, (e) Patterning of active silicon islands by RIE etching, (f) 3-D view of Si island, (g) MOS gate oxidation and CVD of polysilicon gate, (h) Transversal cross-section of the final device, (i) longitudinal cross-section of the final device, (j) picture of a final working DG MOS transistor.

opening method [20] and are given in Figure 9.4. However, the delay between the direct bonding and the annealing was not controlled and has varied among several samples. Regarding to [68], this delay may have influenced the measured surface energies which need be confirmed by further experiments.

From Figures 9.2 and 9.3, the final active surface area differs noticeably whether the samples were activated with HNO_3 or with the alternative O_2 plasma / nitric acid treatment, especially at low temperature.

For hybrid O_2 plasma / nitric acid activated wafers, the mean transfer rate is 90% and the defects present at their surface originate directly from direct bonding voids. Despite thermal treatments and the final TMAH etching, the dimensions of untransferred areas correspond closely to the size of the direct bonding voids. From their round shape but not circular and their lack of expansion, it is believed that these voids are constituted by trapped air.

Concerning the nitric acid activated samples, besides direct bonding bubbles, two kinds of defects are identified: 1) those originating from barely visible voids at direct bonding evolving to bubbles during the annealing step and 2) surface lost by TMAH lateral etching. The descriptions of these defects are detailed here below.

The two wafers concerned by this first type of defect are the 400°C, 95 hours and 1000°C, 10 hours annealed wafers. First, during the annealing of 95 hours at 400°C, barely discernable voids at room temperature swelled to bubbles of 1 cm radius. This voids expansion can possibly originate either from the thermal decomposition of surface contaminants, or be inherent to the bonding mechanisms. Indeed, room temperature voids are acting as bubble nucleation sites during thermal treatments [186]. Second, the same type of small direct bonding voids vanished during the annealing of 10 hours at 1000°C but corresponding expanded bubbles were completely revealed after the TMAH etching. In this case of high temperature annealing, the product of degassing was able to diffuse through the interface, explaining why the voids are not visible anymore after the annealing [162]. In the meantime, surface OH groups, created during the activation, may have reacted with ambient water molecules or hydrogen trapped in the bubbles, leading to unbonded areas revealed by the TMAH etching.

The second kind of defect present on warm nitric acid activated samples concerns the lateral etching during their immersion in TMAH. This etching of the SOI film took place from the bonding interface, under the SOI buried oxide (Figure 9.1 (c)). It is observable on both samples annealed at 120°C (2 hours and 144 hours) and, in less importance, the sample annealed at 400°C during 3 hours. On the one hand, the major part of the surface was removed from both wafers annealed at 120°C. On the other hand, some defects appeared at the centre and the edge of the wafer annealed at 400°C. The assumption of lateral etching is corroborated by the fact that these transfer defects are not exhibiting the perfectly circular shape as other bubbles but rather an irregular one. Our surface energy measurements (Figure 9.4), tend to show that the TMAH lateral etching cannot be related to a unique energy level. This could rather originate from the amount of water molecules at the interface: plasma activation is known to enhance water removal [11] while after 3 hours of annealing at 400°C, some water may remain at the interface of the nitric acid activated sample.

Finally, it is worth to note that the grinding step is not very detrimental to the effec-

tive transferred surface: most of lost areas correspond to unbonded spots. The grinding mechanical constraints are more prejudicial when applied to weakly bonded structures like the 120°C annealed wafers activated by nitric acid.

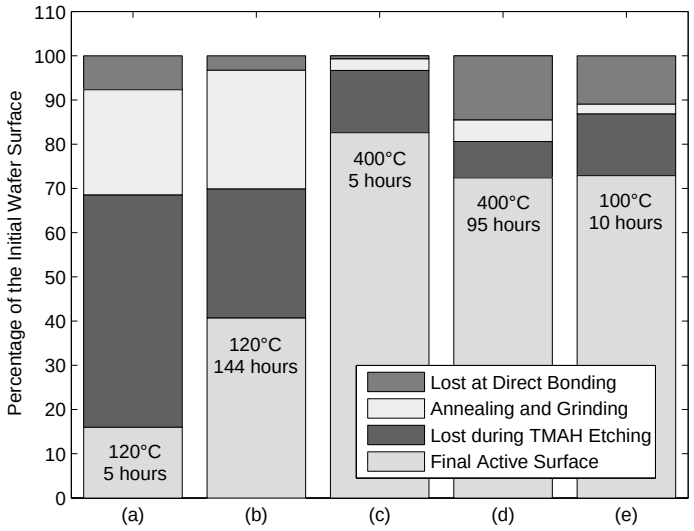


Figure 9.2: Effective surface loss as a function of the film transfer process steps and the annealing conditions, for pure nitric acid activated wafers.

9.4.2.2 Micron-Scale Observation

Small voids invisible in infrared images were revealed after the TMAH etching. Difficult to quantify, they are present on all samples in variable amount. In case of high temperature annealed wafers, their presence is notably reduced, particularly on which were activated by the hybrid oxygen plasma / nitric acid method. These voids are probably high pressure micro-cavities filled by bonding reaction by-product. Their lighter presence in case of high temperature annealing can be explained by a better diffusion of water and hydrogen molecules. Table 9.3 presents photographs of three size micro-cavities after the five annealing conditions under study here, for samples activated by the hybrid O_2 plasma / nitric acid method. The gas development from by-product bonding reaction is clear and in accordance with [162]: during an annealing at 120°C, the silanol groups polymerize and produce water molecules, as described by equation (9.1). At 400°C, the temperature is still too low for the silicon film to be oxidized by the interfacial water [118]. But the first polymerization process completes, forming strong covalent bonds. Tong and Gösele mention that the surface energy will then depend on both the real area in contact at the bonding interface and the density of bonding species [162]. At 1000°C annealing temperature, the water produced by reaction (9.1) oxidizes the silicon film according to reaction (9.2). Moreover, all reaction by-product diffuses through the bonding interface [111], while SiO_2 mass transport and viscous flow are enabled [162], leading to high bonding strength.

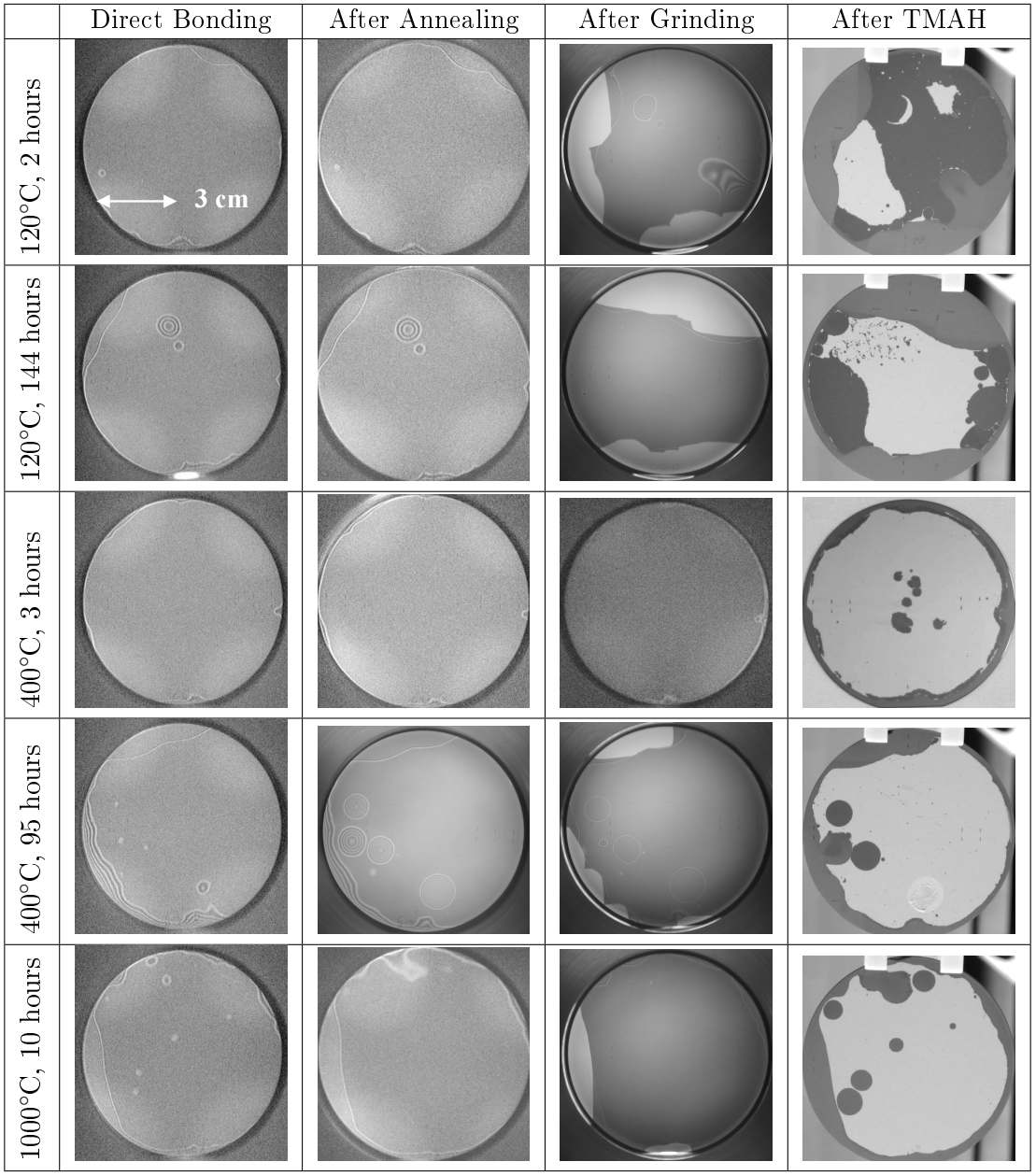


Table 9.1: Infrared and visible light photographs of bonded wafers at different steps of the transfer process (pure HNO_3 activation) for the 5 annealing conditions under study.

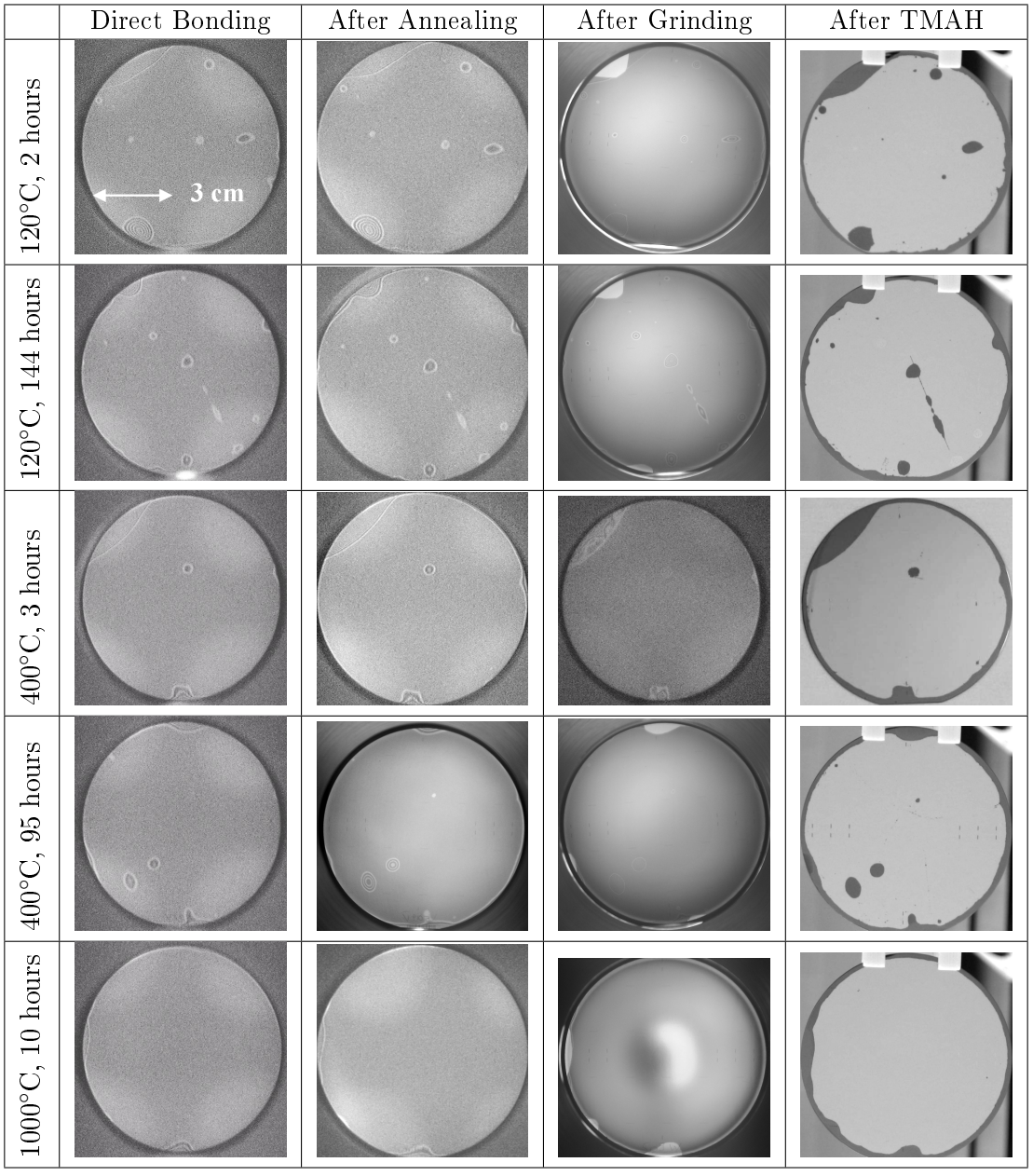


Table 9.2: Photographs of bonded wafers at different steps of the transfer process (O_2 plasma activation on the bulk wafers and warm nitric acid on the SOI wafers) for the 5 annealing conditions under study.

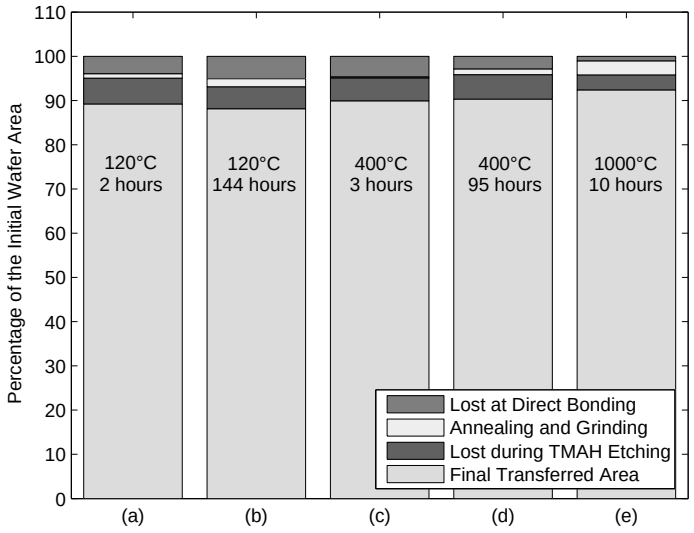


Figure 9.3: Effective surface loss as a function of the film transfer process steps and the annealing conditions, for samples activated by O_2 plasma on one side and nitric acid on the other one.

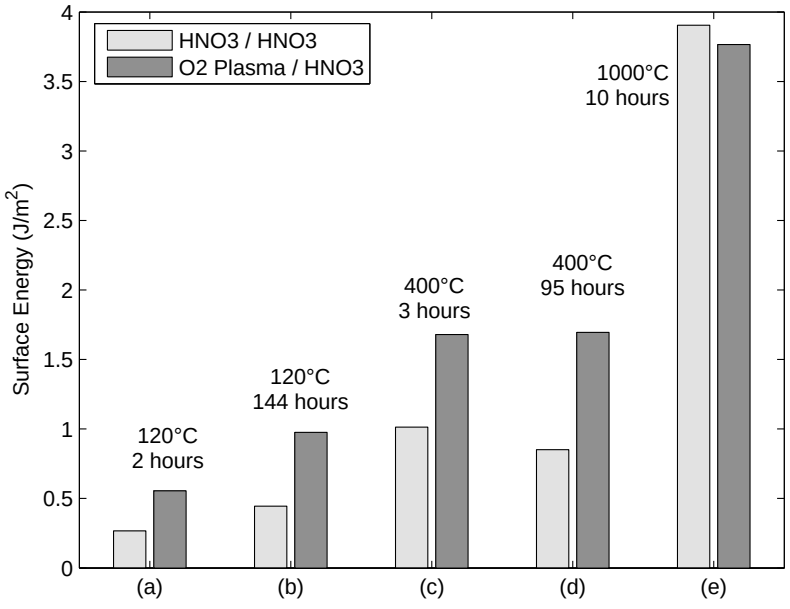


Figure 9.4: Surface energies of samples activated 1) by nitric acid on both sides, 2) by nitric acid on one side and O_2 plasma on the second one ; for the 5 annealing conditions under study.

$$\equiv Si - OH + HO - Si \equiv \rightarrow \equiv Si - O - Si \equiv + H_2O \quad (9.1)$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad (9.2)$$

The biggest structures are swelling progressively until bursting after 95 hours at 400°C. The diffusion phenomenon at 1000°C is very clear; the structures exhibit an almost 'flat' shape after this annealing. The middle size structures are less flexible and their deformation is not really visible. These ones are withstanding to 120°C and 1000°C but not 400°C annealing steps. Finally, the smallest cavities, which are used for double-gate devices, resisted to all annealing conditions. This can be explained by their favorable film thickness on cavity length ratio. It is worth to note that the level of completion of the bonding reaction and, hence, of degassing differs considerably between high and low temperature annealed wafers. Hence, if released samples (i.e. after TMAH etching) are submitted to subsequent thermal treatments, the bonding reaction continues and can lead to the bursting of small membranes due to the absence of capping substrate.

9.4.3 Double-gate devices process solution

From these experiments, most of the tested configurations are potentially usable in terms of transferred surface area. Nevertheless, in the context of double-gate transistors fabrication, high temperature steps may be performed after release of the membranes. In that case, it is preferable to anneal the wafers at high temperature (1000°C) to prevent the membranes bursting. Moreover, during the steady-state wedge-opening tests conducted on wafers annealed at 1000°C, the fracture occurred inside of the oxide film rather than at the bonding interface. Hence, we can state that these high temperature treatments are warrant of a better reliability of the devices. The hybrid oxygen plasma / nitric acid surface activation method is the most promising due to its high transfer rate. However, by security we processed warm nitric acid activated wafers because of a risk of negative charges introduction in the resulting buried oxide, as reported in [68].

9.5 Electrical Performances

The transistors were electrically characterized by Valeria Kilchytska and Tsung Ming Chung, using a HP 4145 Semiconductor Parameter Analyzer. The present results are reported for typical devices with a gate oxide thickness, t_{ox} = 30 nm, silicon film thickness, t_{Si} = 80 nm and BOX ≈ 400 nm, gate length L = 3 μm and width W = 6 and 15 μm. The transistor channel is not doped and then left to its intrinsic doping level which is approximately 10^{15} cm^{-3}. Figures 9.5(a) and (b) show, respectively, the I_{DS}-V_{DS} curves extracted at V_{DS} = 1.05 V and the I_{DS}-V_{DS} curves at various V_{GS} for the DG and SG devices with L = 3 μm and W = 6 μm. It is evident that current levels for DG are at least twice those of SG in strong inversion. These experimental results are in agreement with the double-gate MOSFET theory. In Figure 9.6 we see that DG devices exhibit much better subthreshold slope (S) compared to the SG devices. This improved S also corresponds to the higher transconductance to current ratio (g_m/I_{DS}) of DG in the subthreshold regime. It should be noted that the slight kink observed in the SG device is linked to the presence

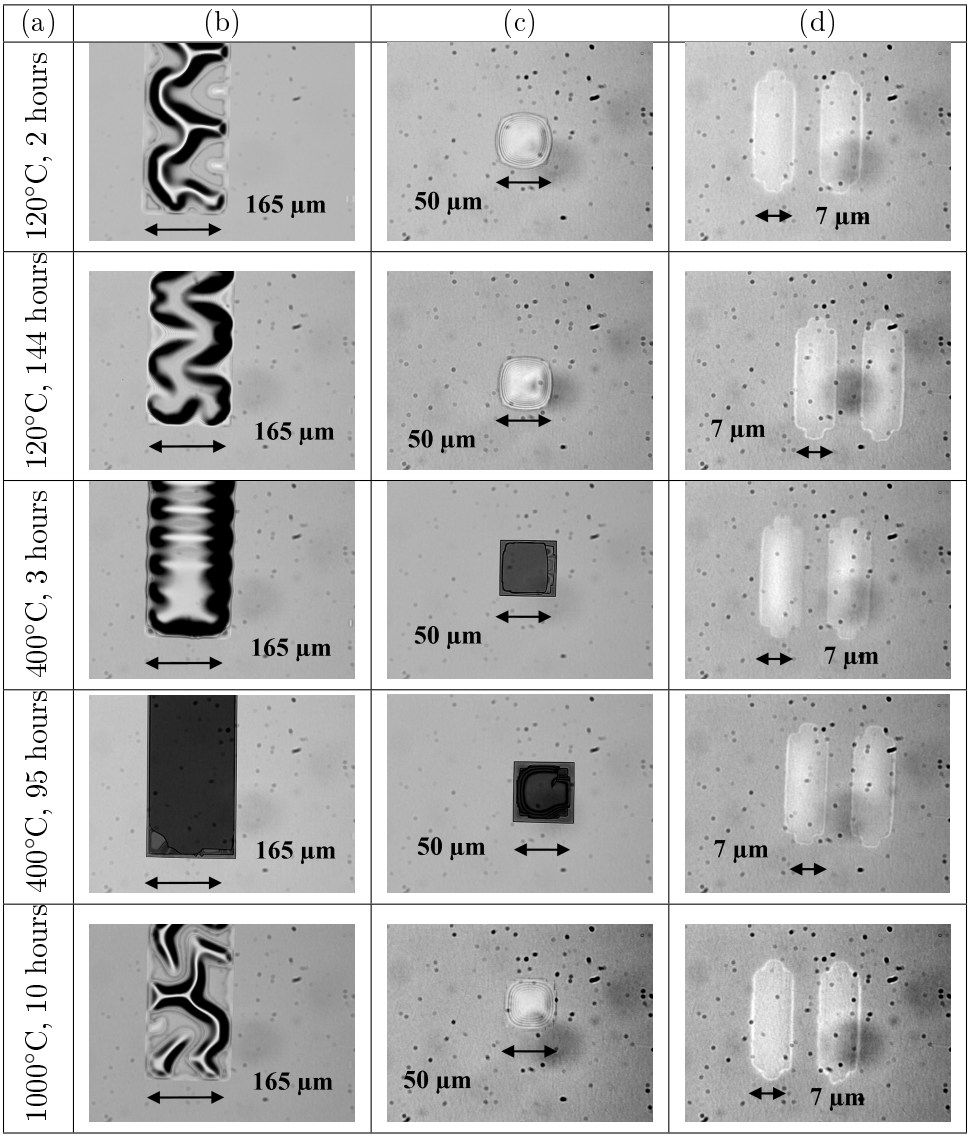
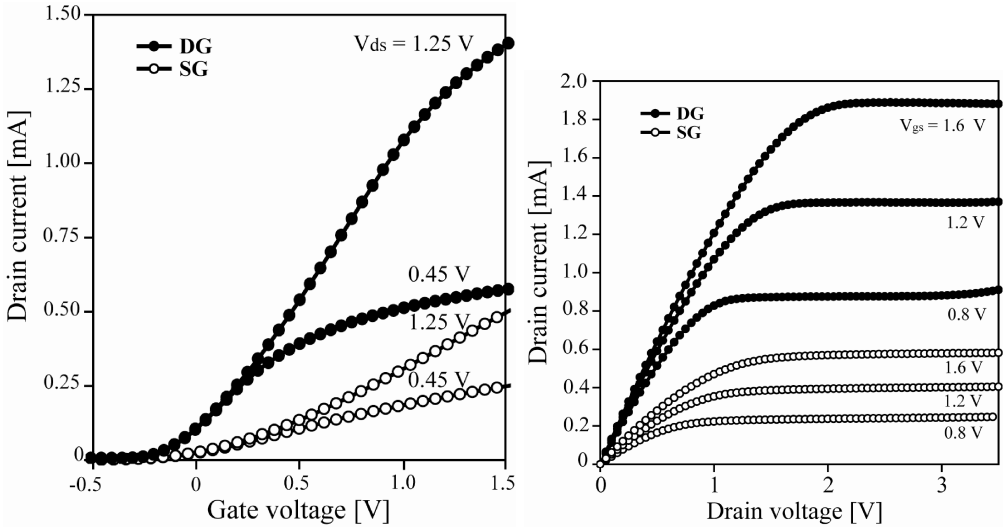


Table 9.3: Photographs of micro-cavities of three sizes (165 μm, 50 μm and 7 μm) that were bonded with O_2 plasma activation and 5 different annealing conditions.

of a lateral parasitic MOSFET which can be solved with an edge implantation. Still from Figure 9.6, we see that the current drive ratio between DG and SG at a fixed value of $g_m/I_{DS} \approx 12$ V^{-1} (close to the device threshold voltage) is approximately 3.1 whereas it is equal to 2.1 in strong inversion ($g_m/I_{DS} \approx 4$ V^{-1}). Values higher than 2 for the current drive ratio between DG and SG are directly related to volume inversion (VI) regime in the double-gate structure. In the strong inversion region, the efficiency of the VI regime is disappearing in the planar DG MOSFET working as a dual gate device [39]. In Figure 9.7, the transconductance ratio ($g_{m,DG}/g_{m,SG}$) between DG and SG for the various devices are shown for a W/L ratio of 5, where in a certain range of gate overdrive, V_{GO}, the ratio is much larger than 2, thanks to the VI effect in this regime. Figure 9.8 shows the Early voltage (V_{EA}) extracted at $V_{GS} = 0.60$ V for the DG and SG devices which reflects the output characteristics of a device with a W/L = 5. V_{DS} was chosen low enough to avoid the breakdown effect of the SG, thus making a fair comparison for both DG and SG. The tremendous improvement in the V_{EA} values of the DG over SG devices is again a mark of correct DG operation and reduced SCE [90].



(a) (b)

Figure 9.5: (a) I_{DS}-V_{GS} at $V_{DS} = 1.05$ V and (b) I_{DS}-V_{DS} curves at various V_{GS} (= 0.8, 1.2 and 1.6 V) for SG and DG MOSFETs with L = 3 μm and W = 6 μm.

9.6 Conclusions

In this chapter, the specific wafer bonding conditions were investigated in order to maximize the thin film transfered surface and then improve the yield in the frame of double-gate devices fabrication. As a conclusion, we can state that hybrid oxygen plasma / nitric acid surface activation method seems more effective in terms of annealing voids prevention. Moreover, a minimum of 88% transfered area rate was achieved for all conditions. Besides, for both activations methods, the best annealing conditions were found at high temper-

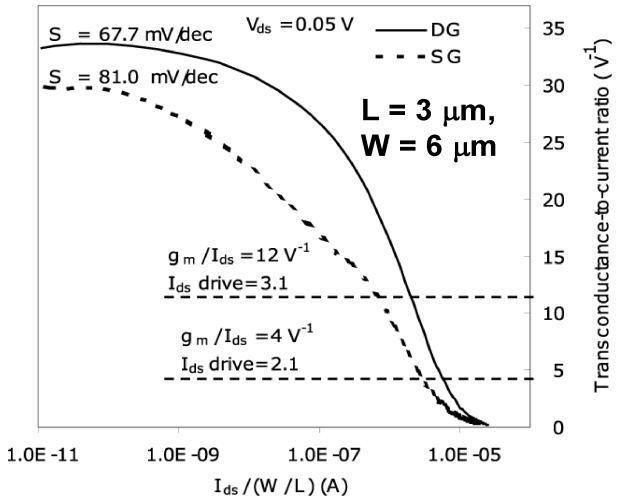


Figure 9.6: $g_m/I_{DS}/(W/L)$ curve for DG and SG devices at V_{DS} = 0.05 V for L = 3 μm and W = 6 μm.

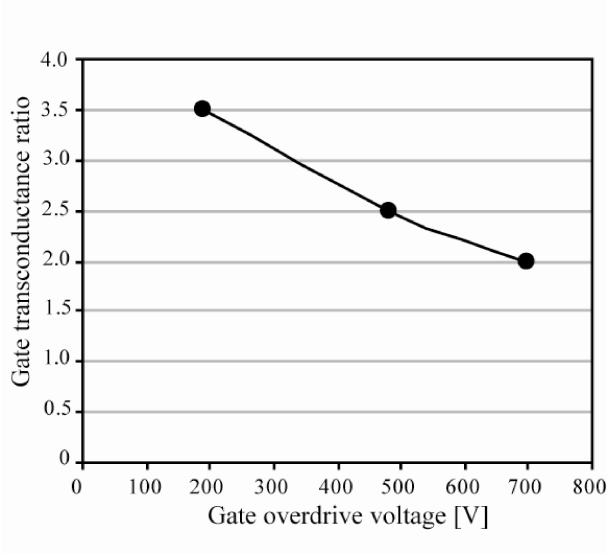


Figure 9.7: Transconductance ratio ($g_{m,DG}/g_{m,SG}$) at V_{DS} = 1.0 V for L = 3 μm and W = 15 μm

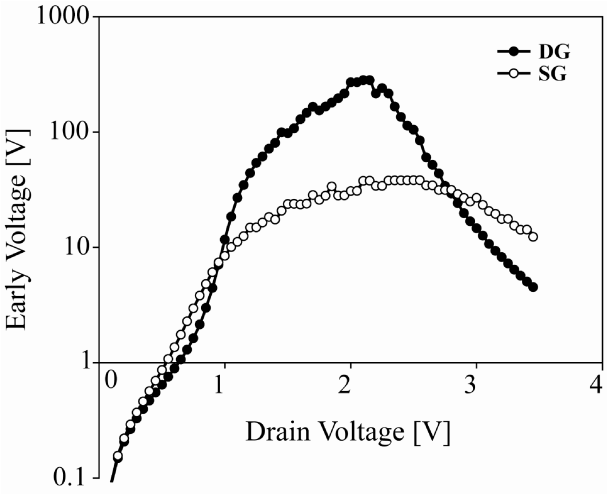


Figure 9.8: Early voltage for the SG and DG MOSFETs at V_{GS} = 0.6 V for L = 3 μm and W = 6 μm.

ature for three reasons: the cavities integrity during subsequent thermal treatments, the minimization of small voids density and the maximization of the surface energy. The successful realization of transistors according to this process flow demonstrates the viability of this method with nitric acid activation. Nevertheless, for its evidenced advantages, a full process using the hybrid oxygen plasma / nitric acid method would be of great interest to be realized. Finally, the electrical characterization of the devices does attest this viability. It appears that the fabricated DG MOSFETs devices have shown most of their expected properties.

Part IV

Conclusions

Chapter 10

Conclusions and Perspectives

In this thesis, we aimed contributing to the emergence of the concept of Novel Active Pressure Sensors (NAPS) in thin film SOI technology. This concept is based on the following trio of characteristics:

1. Thin Dielectric Membranes,
2. Fully-Depleted (FD) Silicon-on-Insulator (SOI) CMOS (Complementary Metal-Oxide-Semiconductor) Technology,
3. Active Transducers.

Starting from a technological opportunity, it was expected that the **potentialities** of the concept compared to the existing pressure sensors technologies, such as

1. very thin and uniform membranes with a well controlled thickness thanks to the BOX as etch stop layer,
2. (ultra-)low power, high temperature capabilities and radiations hardening in scale with FD SOI technology,
3. smart sensing behavior (frequency output, advanced architectures for an increased sensitivity) enabled by the implementation of active transducers,

were worth to face the **challenges** on the mechanical handling and numerical modeling related to the complexity of its physical structure. Indeed, the integration of MOS devices onto these membranes involve thin films stacks with complex patterning shapes coupled with unusual dimensional ratios between horizontal and vertical axes. This set of characteristics brings the NAPS concept into a new paradigm as it was described in the introduction.

In this work, the focus was set on the combination of demonstrators fabrication, electromechanical characterization and numerical simulations in order to address the question: "Does the Novel Active Pressure Sensor concept defined here represent a technological gap?" In other words, "Is such unedited configuration of pressure sensor can be really used as a pressure sensor?" The two following questions were then addressed: "Is there a tool for the pressure sensor designer?" and "Does the NAPS concept represent a suitable environment for studying electronic transport". Answering positively these questions was equivalent to

assess robustly the strain value at the device channel level through FE simulations. These topics were developed in the first part (part II) of the present thesis. In a second part (part III), the objective was to contribute to the emergence of such sensors from a more general point of view i.e. the applicative contexts of 3D-IC integration and special substrates preparation through the analysis of four case-studies and based on Direct Wafer Bonding (DWB).

10.1 Summary of the Work and Concluding Remarks

In the first part of the work, beyond the possibility of fabrication that was demonstrated by Dr. Jean Laconte [100], the potentialities of the concept of suspended FD SOI MOSFETs on very thin dielectric membranes as pressure sensing systems were evidenced. Both single devices and full oscillators implemented directly on the membranes were fabricated and characterized, showing a sensitivity of few percents in terms of drain current and frequency output signal variations. The sensing properties of a suspended MOS device under a dynamic pressure were experimented, demonstrating the applicability of such structure in shaft speed measurements for instance. Thermal characterization of suspended voltage controlled oscillators (VCOs) were also reported, confirming that it is possible to realize in the frame of the NAPS concept a system almost temperature independent by considering the output frequency ratio of a pair of suspended VCOs inversely sensitive to the pressure.

In addition, mechanical characterization of very thin membranes have been achieved for blanket as well as functionalized membranes by measuring the deflection under an applied pressure as well as their burst pressure. These measurements have highlighted a drastic loss of functionalized membranes robustness in comparison with blanket membranes. Indeed, for 800 μm-side square membranes, the burst pressure is almost divided by a 10 factor, dropping from a value superior to 5 bars for blanket membranes down to 0.5–1 bar for membranes with suspended VCOs. The membrane patterning was then supposed to be the cause of the robustness issue, in particular, large zones where the nitride is etched-out. Finite Element (FE) simulations have evidenced that (i) the mean stress is higher in patterned areas and (ii) there exist strain peaks at film discontinuities. Reformulated we have that, with film patterning, there is more surface exposed to high strain and there are more points where the strain is concentrated. As consequences, according to Weibull theory, the larger areas under a higher stress of patterned zones would lead to an increased fracture probability compared to blanket membranes. Besides, extracting strain values at points apparently highly stressed was shown to be an irrelevant method to address the membranes reliability issue. Therefore, linear elastic fracture mechanics concepts were briefly introduced. Complementary experiments have shown that a patterning effect on the membrane robustness may also be additive i.e. due to additionally deposited films, having a pattern. Furthermore, FE simulations produced essential informations concerning the strain distribution into the thin multilayered membranes. In fact, the strain has a high gradient near the borders and up to 30 μm away from the edges, as well as it exhibits a high fiber dependence. Beyond that distance, in the central region of the membrane, the strain has rather a plateau value, almost steady for all fiber levels as well as laterally. These results were very helpful for issuing sensor design rules in scale with the present context of

very thin dielectric membranes and active transducers. These rules invite to:

i. Implement reduced membranes sizes with reduced patterned structures (transducers) footprint, in order to ensure sufficient robustness;

ii. Position the active devices at the central region of the membrane for enlarging the process window (i.e. the lateral definition of the membranes).

On the basis of these recommendations, a series of novel architectures implementing only few or even single suspended devices driving an out-of-membrane oscillator and designed by Bertrand Rue, were experimented. Two of them emerged as applicable sensors, offering jointly good or outstanding sensitivity and good robustness. The first architecture is based on a single suspended N-Source device and the second on a cascaded PMOS mirror with four suspended devices. Their figures of merit are:

Configuration	Sensitivity (%/bar)	FS Variation (%)	Measured range		Burst Pres. (bar)
			Min (bar)	Max (bar)	
Intrinsic N-Source Mb: 250 x 400 μm^2 at the center	2.47	11.63	0.1	4.8	$\geq$ 4.8
Casc. PMOS Mirror Mb: 500 x 500 μm^2 50 μm from border	46.83	140.48	0.1	3.1	3.1

Table 10.1: *

The power consumption of the sensing stages of the circuits was estimated at a level as low as 2-3 μW.

Nevertheless, a drift phenomenon was newly observed. This effect appeared to be sensitive to the bias conditions, evoking a charging effect. The evaporation of a metal on the back side of the membrane eliminated the drift effect, indicating how the control on the back gate is an important parameter to maintain the electrical stability of the suspended devices.

At this stage of the work, it was possible to partially answer the applicability concern about the sensors. — *Yes, it is possible to fabricate pressure sensors in the proposed NAPS frame with:*

- *a good sensitivity,*
- *good robustness,*
- *and low-power consumption.*

... but they suffer from a drift effect that needs to be solved. Proposals are formulated in the next section.

Finally, it was intended to assess robustly the strain value at the device channel level through FE simulations. Starting from the N-Source functionally successful architecture, three numerical routes were followed. Indeed, in practice the system to be simulated is too complex to be addressed without simplifications. The first route was based on the fact that the device is located at the central region of the membrane, where the strain is at a plateau value, and assumes that the strain into the device is the same as the strain in the blanket membrane. The model implemented was then a 3D blanket membrane. In the second route, it was intended to refine the results of first blanket model by applying a kind of sub-modeling i.e. a strain correction based on accurate cross-sectional 2D models. The third route was the direct implementation of a 3D model including a device patterning but with a simplified structure in order to allow its computation. The simulation results obtained from these models were confronted with a direct resolution based on the piezoresistive theory, evaluated from electrical measurements of suspended devices (N- and P-MOS) and accurate piezoresistive coefficients. The electrical measurements were made on different devices and bias conditions, showing their consistency in terms of sensitivity to the pressure. The piezoresistive coefficients were extracted from four-point bending set-up measurements. Combining electrical characteristics under pressure of suspended N- and P-MOSFETs with identical layouts gives a very simple and original way for resolving stress components in the membrane. Nevertheless, *while the FE simulations yielded results on the order of the calculated stress values, none of them produced sufficiently accurate data to satisfy either the pressure sensor designer or the electronic transport scientist.*

The ways envisioned for going further are: (i) a more complete model of materials, including anisotropic behavior, (ii) a volume data extraction instead of punctual, (iii) the set-up of more complex model, closer to the actual structure, implemented by sub-modeling.

In the second part, all the case studies concerned hydrophilic Direct Wafer Bonding of silicon and silicon oxide either thermal or deposited by PECVD. They addressed questions in scale with 3D-IC integration and, therefore, are front-end-of-line compatible, except for the last case which concerned the transfer of a thin film in front-end-of-line.

Case Study 1 - The objective was to study the effect of the interfacial SiO_2 thickness on the resulting surface energy. This study was lead with thermally oxidized samples. In order to stay in BEOL-compatible conditions, the post-bonding temperature was limited at 400°C and the focus was set on a dry surface activation method: oxygen plasma. The first observation in this study was a progressive drop of surface energy (-45%) when the total interfacial SiO_2 thickness is increased (from 100 nm to 950 nm). Indeed, this drop was noticed in both Si/SiO_2 as well as SiO_2/SiO_2 configurations. Looking at a better understanding of the bonding mechanisms that could explain this first observation, three parameters were analyzed: the surface roughness, the radicalization effect and the plasma exposure time. First, the surface roughness was liable to vary with (i) the film thickness and (ii) the plasma activation process. Contact AFM measurements were performed and revealed that the surface roughness variability with the film thickness was negligible compared with the magnitude of the observed loss. This was corroborated by the fact that no such loss appears with HNO_3 activated wafers followed by a degassing. Looking at the effect of the plasma activation on the surface roughness, samples were activated

by O_2 plasma but were degassed afterwards, in order to annihilate the chemical effect of the activation. These wafers showed no loss of surface energy when the oxide thickness is increased, proving by the way the absence of effect coming from the surface roughness. Examinating the radicalization effect, ToF SIMS measurements made on a thin (200 nm) and on a thick (800 nm) oxide film have shown a lightly higher SiOH/SiO ratio on the sample with thinner oxide film, tending to show that a thinner oxide film has a higher surface concentration of radicals. Finally the plasma exposure time was investigated on a sample series with different SiO_2 film thicknesses. It showed that it is necessary to adjust plasma exposure according to the nature of the interfacial materials as well as the thickness of the activated films. An optimized plasma exposure enables high bonding strength for thick SiO2 bonding with a low temperature annealing (400°C).

This work, published in Microsystem Technologies, deals with a general optimization process and tries to bring a finer understanding of the bonding mechanisms. Moreover, this case is not only conceptual, but was of concern for Galchev [61] in a low-temperature-high-aspect ratio MEMS process.

Case Study 2 - PECVD oxide was considered as intermediate layer in direct wafer bonding. For that purpose, a detailed analysis has been accomplished in order to reduce the internal stress of PECVD oxide film by adjusting the main deposition parameters and by the help of thermal treatments. From the basis of a standard oxide recipe, films deposited with higher precursor gas flow (over 800 sccm), lower RF power (below 35 W) or with a $[N_2O/SiH_4]$ ratio lower than 5 are particularly adequate to produce lowly stressed oxide films. However, lowering residual stress by increasing the gas flow or reducing the RF power is inevitably accompanied by an increase of etch rate in BHF. From these observations and with the help of RTA, very low compressive, stress free or lowly tensile oxide films can be deposited. It was proven that RTA is the most efficient at a temperature over 900°C and duration of 15 s to reduce the film stress as well as the BHF etch rate and to enhance its long term stability, by reorganizing the deposited film.

After a CMP step, wafer bonding of prepared PECVD oxide films were successfully conducted with representative oxide recipes. Bonded samples showed that the resulting surface energy, after a low temperature annealing, tends to vary inversely with the elastic energy accumulated by the conformation of the wafers during the direct bonding. 45 μm wafer bow comes out as an upper bow limit, preventing direct bonding to occur. As a corollary, this limit gives an upper estimation of the instant work of adhesion when PECVD SiO_2-Si surfaces are brought into contact.

All those experimental results highlighted the importance of monitoring the residual stress in intermediate oxide layers to assure high quality and reliable bonding and thus 3D integration. Beyond the wafer bonding scope, the reduction or the modulation of the stress in an oxide film also applicable others contexts, like as intermediate layer on a thin membrane.

Case Study 3 - The concept consisting in inserting thin ductile interlayers next to a direct bonding interface was addressed. This concept supposed an enhancement of the interface toughness by dissipation of debonding energy in plastic deformation occuring in the interlayers. Therefore a multiscale model was presented, based on a system of of two symetrical bonded wafers. Each wafer wafer was constituted of a thick substrate

and two thin films. The first film was made of a metallic ductile material and modeled according to J2 flow theory. The second film was made of an isotropic linear elastic material. At the nanoscale, the interface between the two wafers was characterized by a traction-separation law, while a wedge was inserted in order to propagate a crack along the interface. This model, computed by Dr. Yannick Bertholet [21], predicted fracture energies fracture energies equal to 5 to 10 times the interface intrinsic toughness Γ_0, according to the relative film thicknesses and/or the yield stress of the dissipative layer. In practice, the system was implemented with 300 nm PECVD SiO_2 films as elastic bonding layer and 1 μ Al films as ductile interlayers, showing the pertinence and the efficiency of the concept. The average measured fracture energy for an interface between two PECVD SiO2 films on Si wafers was equal to 2.1 J/m2. When a Al layer was inserted in between the Si wafer and the SiO2 layer, the average fracture energy raised to 3.5 J/m2, involving a substantial improvement of the global toughness of the bonded wafers.

The configuration experimentally demonstrated here is canonical with plain layers. More generally, it gives an original and instructive point of view on the interaction between brittle bonding interfaces and close ductile materials in 3D-IC integration.

Case Study 4 - The aim was the fabrication of planar double-gate (DG) and silicon-on-nothing (SON) SOI MOS devices according to an innovative process. This process flow involved the transfer of a 100 nm thin silicon film from a standard SOI wafer onto an oxidized bulk wafer with pre-etched cavities. This transfer was implemented by a direct wafer bonding followed by the back-etching of the SOI wafer substrate and BOX by grinding, TMAH and BHF etching steps. Two main aspects were in scope: (i) maximizing the effective transfered surface area as it conditions directly the yield of the DG MOS devices and (ii) ensuring the Si film integrity locally, at the suspended channels level. Two main parameters were varied: the surface activation prior to bonding and the subsequent annealing conditions. Warm HNO_3 surface activation was applied on all SOI wafers in order to prevent any lattice damage due to a plasma strike action. At contrary oxidized bulk wafers were divided in two batches, surface activated either with HNO_3 or O_2 plasma. The annealing conditions were varied in terms of temperature (120, 400 and 1000°C) and duration (from 2 to 144 hours). The effective transfered surface area was quantified at each step of the process and equivalently prepared wafers were used for surface energies measurements. The combination of HNO_3 / O_2 plasma surface activation methods showed to be the most effective at all annealing conditions. In that case, the direct bonding voids were limited and the effectively transfered film area remains very close to the limit of these direct bonding voids. Besides, high temperature annealing gave best results in terms of suspended Si film preservation.

Thanks to this thin film transfer process optimization, planar SOI DG MOSFETs (as well as Silicon-on-Nothing SON devices) were successfully fabricated, leading to three publications based on the analysis of the performances associated with the DG / SON MOSFET architectures [38, 66, 89], and constitutes a basis for other types of thin film transfer or special substrate preparation implemented by direct wafer bonding.

10.2 Outlook

Besides the demonstration of the achievable sensitivity of the pressure sensors (and besides the enumeration of the various results of the previous section), another contributive aspect of this work is to draw the limitations of the present concept and its most immediate potential evolutions or revolutions. We list these new challenges as follows:

- Drift issue assessment,
- Continuous Si_3N_4 film on the membrane,
- Laterally accurate release of the membranes by Reactive Ion Etching (RIE),
- Alternative solution to on-membrane metal.

We discuss the two first challenges here below.

10.2.1 Drift Issue

Before going further, it seems essential to address the drift issue described in Chapter 4. Indeed, it conditions directly the applicability of the sensors. As this problem appears to origin from the floating back-gate potential of the suspended devices, it is needed to adjust a structural element. In practice, a classical metal layer evaporated on the back side of the membranes may not be reliably used. This is mainly due to high strain values which are on the order of 1% under high pressures, at the bottom fiber of the membranes. Nevertheless, three solutions for controling that potential are figured out as follows.

- The first solution consists in a post-process deposition of a mineral conductive layer on the back side of the membranes. An *in situ* doped amorphous silicon deposited at low temperature (50–300°C) in a PECVD chamber would be convenient [32, 122, 126]. Such material with a low stress ($\leq$200 MPa) and fairly conductive (100–1kΩcm) is documented by Oxford Instrument [7]. This solution is illustrated as 'Option 1(a)' in Table 10.2.

- Secondly, the process may be started on the basis of special substrates, embedding a conductive layer underneath the buried oxide. The most immediate location for that conductive layer is beneath the BOX ('Option 2(b)' in Table 10.2). However, it exposes the layer to the etchant solution during the membrane release. As this layer must withstand to high temperature BEOL steps, it can be made of silicon in any state of crystallinity i.e. amorphous, poly- or single-crystal. A selectivity to TMAH can be implemented in two ways [100]. First, the Si might be heavily p^{++} doped ($\geq 10^{20}$ cm^{-3}) producing an etching selectivity of 10% with respect to the substrate silicon; and second, the layer might be n-doped (the opposite doping type as the substrate) and electrochemically protected from a TMAH attack. Nevertheless, these two methods are not realistically implementable for a conductive layer of 100–300 nm. Therefore, an alternative configuration is preferred and consists in the embedding of a mineral conductive layer between a buried nitride film and the standard BOX, as sketched in 'Option 2(e)', Table 10.2. In this case, the thickness remains limited and

the etching stop is largely eased but at the expense of a quiet complex starting wafer to be fabricated.

- Thirdly, the back-gate control can be assured at the device-level by ...a back-gate! Indeed a successful fabrication of planar double-gate devices was demonstrated in the present thesis and necessitates only a short specific pre-process before continuing with a standard SOI MOS process (Chapter 9). In particular the bonding conditions for the thin layer transfer involved in the pre-process were optimized. This expertize is then directly available for attempting to address the drift issue. This configuration is illustrated in 'Option 3(c)', Table 10.2.

10.2.2 A Continuous Si_3N_4 Film

A second limitation of the concept is probably the patterning in the nitride layer. As an outcome from Chapter 3, the continuity of the suspended films is essential to ensure a good mechanical robustness to the membranes. This is particularly true for the nitride film which is the hardest film in the stack and ensures the resulting tensile stress of the membrane. Perfectly continuous nitride films could be implemented by the fabrication of specific starting wafers. Proposals for such wafers are depicted in Table 10.3 and optionally integrate a conductive layer, as discussed in the previous section. Finally, it is worth to note that starting the process with dedicated substrates with buried Si_3N_4 layers, the wafers do strictly follow the standard SOI process before the final post-process release operations. Resulting structure are illustrated in Table 10.2.

10.2.3 Novel Paradigm Change - A Step Towards Flexible Electronics

In Chapter 5, a simple method based on the piezoresistive theory and the combined strain sensitivities of a pair of P- and N-MOSFETs with identical designs was used to estimate the strain as a function of the pressure. This method is very useful to sensor designer in order to help him how to dispose his sensitive MOS transducers. Nevertheless, it has the limitation of the piezoresistive theory validity. At high levels of stress or when the size of the devices under study does shrink sufficiently [74], the relation between the applied strain and the resistance does not remain linear. When it is intended to study this relationship itself, the thin dielectric membranes do not seem to be a suitable environment. Therefore, going a step further would make sense. It is worth to note that flexible substrates are already platforms used for the study of electronic conduction in nanostructures or novel materials e.g. graphene [60]. In this environment, large deformations may easily be applied uniaxially in a calibrated way.

Besides, the circuit designs presented in this thesis, elaborated by Bertrand Rue, are already successfully implemented as strain sensors on 3x3 mm^2 small dies 200 μm-thick [142]. For these systems, the strain dissipation in the epoxy glue is a concern [72, 142]. Transferring SOI CMOS onto flexible substrates would certainly improve the coupling of the stress but also enable a shift from harsh environments applications towards robotics [104] or biomedical applications [77, 112, 114, 138]. One can note that strain sensors on flexible substrates do exist and are readily demanded but are so far limited to passive or TFT structures [77, 79, 189] or organic technologies [85].

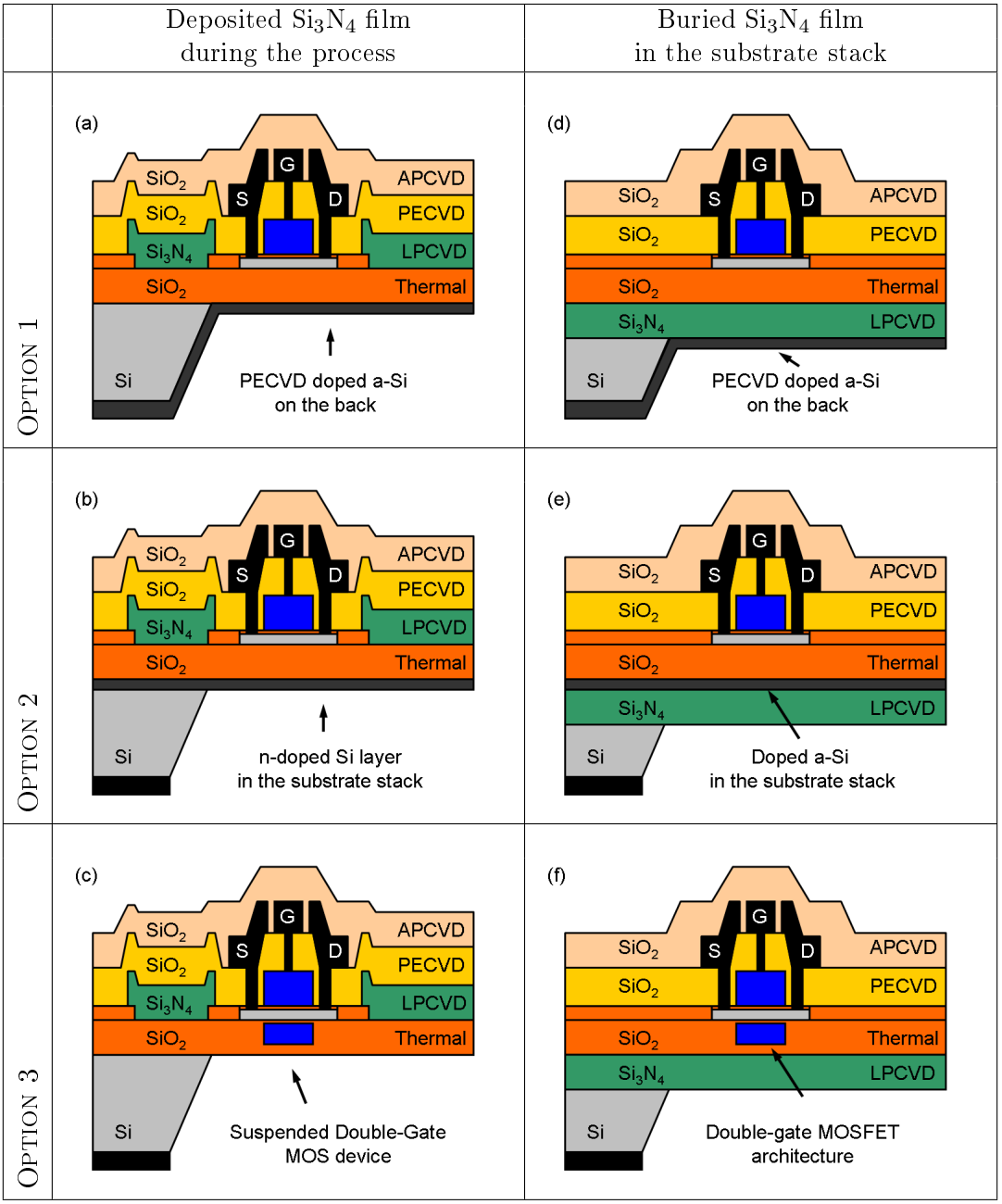


Table 10.2: Solutions envisioned on thin dielectric membranes for assessing the back-gate potential of suspended devices on thin dielectric membranes, combined with alternative substrates including a continuous buried nitride layer in the stack: Option 1 - deposition of a conductive layer in post-process, Option 2 - special starting substrate embedding a conductive layer, Option 3 - double-gate MOSFET architecture i.e. a local shielding.

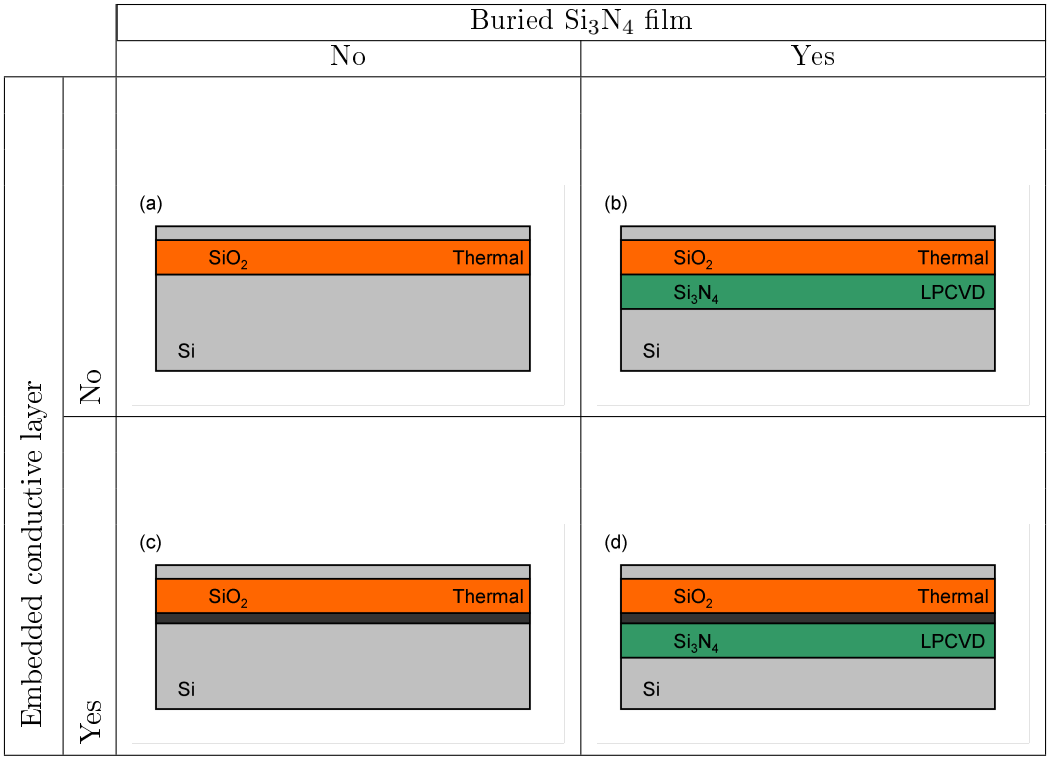


Table 10.3: The four configurations of special SOI substrates needed for realizing the structures presented in Table 10.2: (a) standard SOI wafer, (b) SOI wafer with extra buried nitride layer at the bottom of the stack, (c) SOI wafer with embedded conductive layer underneath the buried oxide (BOX) and (d) SOI wafer including an embedded conductive layer underneath the BOX and an extra buried nitride layer at the bottom of the stack.

Finally, among numerous publications dealing with wafer bonding of silicon onto polymer, we point out one paper from Tyndall National Institute [29] that addresses a novel change of paradigm: the transfer of a thin silicon film onto a flexible substrate (Figure 10.1). While being applied to a simple top silicon film from a SOI wafer, the process described in that paper is fully BEOL-compatible. It is based on adhesive bonding, grinding and back-side chemical etching, which are typical techniques under use in the present work ...and the wafer becomes the membrane.

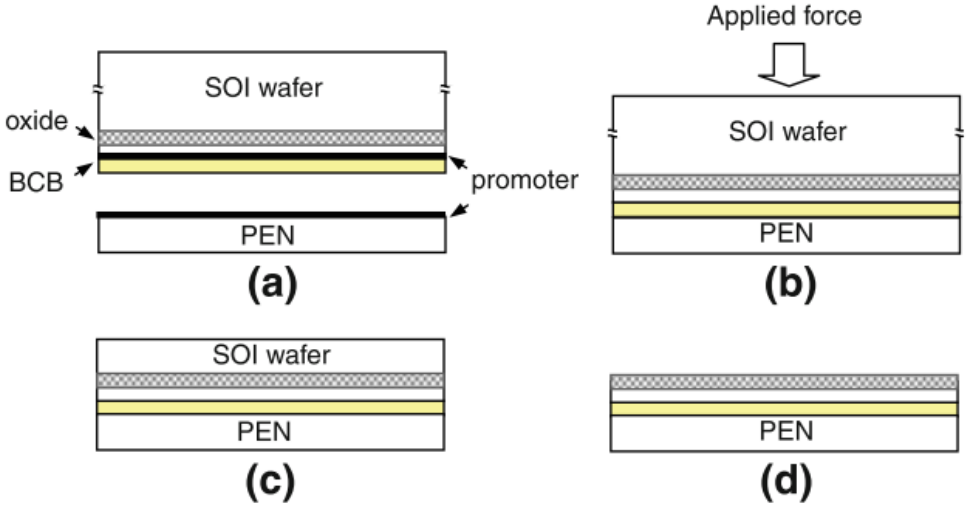


Figure 10.1: Schematic showing the process sequence to transfer single-crystalline Si onto flexible substrate: (a) spin-on adhesive promoter to PEN and SOI, spin-on BCB to SOI wafer, (b) bond and anneal 150°C, 48 h, 8.15 kPa, (c) first thinning by grinding and CMP, removes 370 μm Si (from 470 μm), and (d) second thinning by two-step wet etch, removes 100 μm Si. [29].

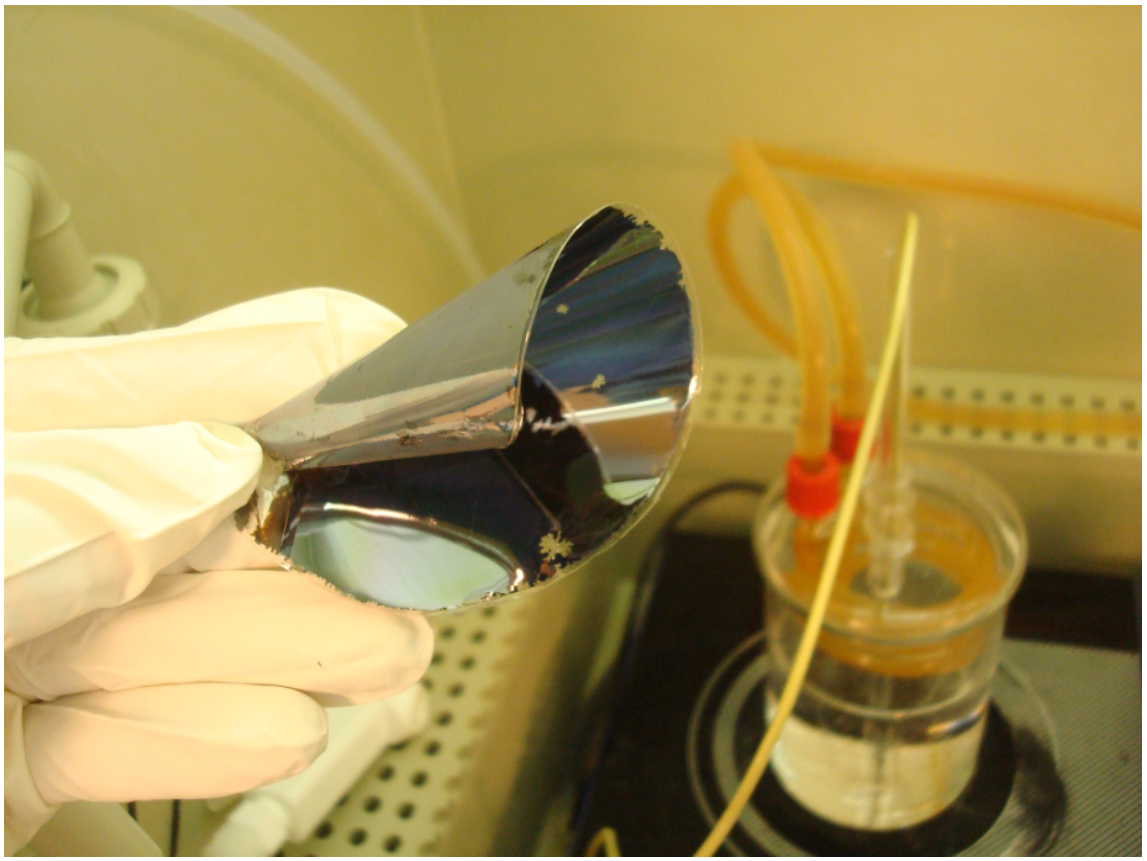


Figure 10.2: Curling 3-inch Si wafer thinned by TMAH (5%, 90°C) wet etching from 380 μm down to 17 μm, with a Protek B3 polymer front-side protection.

Je vois la Vie comme une grande course relais où chacun de nous, avant de tomber, doit porter plus loin le défi d'être un homme.

Romain Gary

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Appendix A

Membrane border devices - Stress evaluation

First, let us evidence that $\sigma_{yy} = \nu_{Si} \cdot \sigma_{xx}$, where σ_{yy} and σ_{xx} are stress components, ν_{Si} is the Poisson coefficient of the silicon and is worth 0.28. The axes are defined in Figure 1, p. xix.

By definition we have:

$$\varepsilon_{xx} = \frac{\sigma_{xx}}{E} - \frac{\nu\sigma_{yy}}{E} - \frac{\nu\sigma_{zz}}{E} \tag{A.1}$$

$$\varepsilon_{yy} = \frac{\sigma_{yy}}{E} - \frac{\nu\sigma_{xx}}{E} - \frac{\nu\sigma_{zz}}{E} \tag{A.2}$$

As the stress is essentially planar, we consider that $\sigma_{zz} = 0$. Moreover, exactly at the border of the membrane we have: $\varepsilon_{yy} = 0$. The identification is then immediate: $\sigma_{yy} = \nu_{Si} \cdot \sigma_{xx}$ in the channel of a device located at the border of a membrane.

Concerning the case of p. 2.4.2, the drain current in the NMOSFET, I_D, varies according to the stress as follows:

$$\frac{\Delta I_D}{I_{D_0}} = -\pi_{NMOS,\parallel} \cdot \sigma_{\parallel} - \pi_{NMOS,\perp} \cdot \sigma_{\perp} \tag{A.3}$$

Introducing the values from Table 2.1, the equation becomes:

$$\frac{\Delta I_D}{I_{D_0}} = -\pi_{NMOS,\parallel} \cdot \sigma_{xx} - \pi_{NMOS,\perp} \cdot \sigma_{yy} \tag{A.4}$$

$$= +1.97 \cdot \sigma_{xx} - 1.23 \cdot \sigma_{yy} \tag{A.5}$$

$$= +1.97 \cdot \sigma_{xx} - 1.23 \cdot (0.28 \cdot \sigma_{xx}) \tag{A.6}$$

From Figure 2.4, we know that the drain current increases by 4% ($= \Delta I_D / I_{D_0}$) under the applied force, which brings to the final identification:

$$\begin{cases} \sigma_{xx} = & 173\text{MPa} \\ \sigma_{yy} = & 48\text{MPa} \end{cases} \tag{A.7}$$

Appendix B

Piezoresistive Coefficients Determination Method

In order to determine the piezoresistive coefficients for the UCL-Winfab FD SOI CMOS technology, we started from the phenomenological basic piezoresistive equation, which writes

$$\frac{\Delta I_D}{I_{D_0}} = -\pi_{MOS,\parallel} \cdot \sigma_{\parallel} - \pi_{MOS,\perp} \cdot \sigma_{\perp}, \tag{B.1}$$

where $\Delta I_D / I_{D_0}$ is the MOSFET normalized drain current variation, $\pi_{NMOS,\parallel}$ and $\pi_{NMOS,\perp}$ are the coefficients under investigation, $\sigma_{\parallel}$ and $\sigma_{\perp}$ are both components of stress regarding to the current orientation.

For a given electrical bias, both coefficients are identified by the sequential application of parallel and perpendicular calibrated uniaxial stresses, while the device drain current is measured with and without the applied stress. A four-point bending set-up is used for the application of the uniaxial and calibrated stress. This set-up is illustrated in Figure B.1. A 3-inch fully processed wafer is inserted between four rods, while these rods are vertically precisely actuated by mean of a micrometer screw.

The magnitude of the tensile stress applied on the top-fiber of the wafer, i.e. at the location of the transistors, specifically between the two central rods, is expressed as follows:

$$\sigma = \frac{3Edt}{8a^2}, \tag{B.2}$$

where σ is the stress, E the Si Young Modulus (169 GPa), d the vertical displacement from the null stress position i.e. from the flat wafer position (500 μm/turn of the screw), t the wafer's thickness (800 μm), a the horizontal rods separation distance (1.5 cm). An opposite configuration of the rods (e.g. a vertical flip) produces an equivalent compressive stress in the top-fiber of the wafer.

Formally, the application of one value of stress is sufficient to identify one π coefficient. For instance:

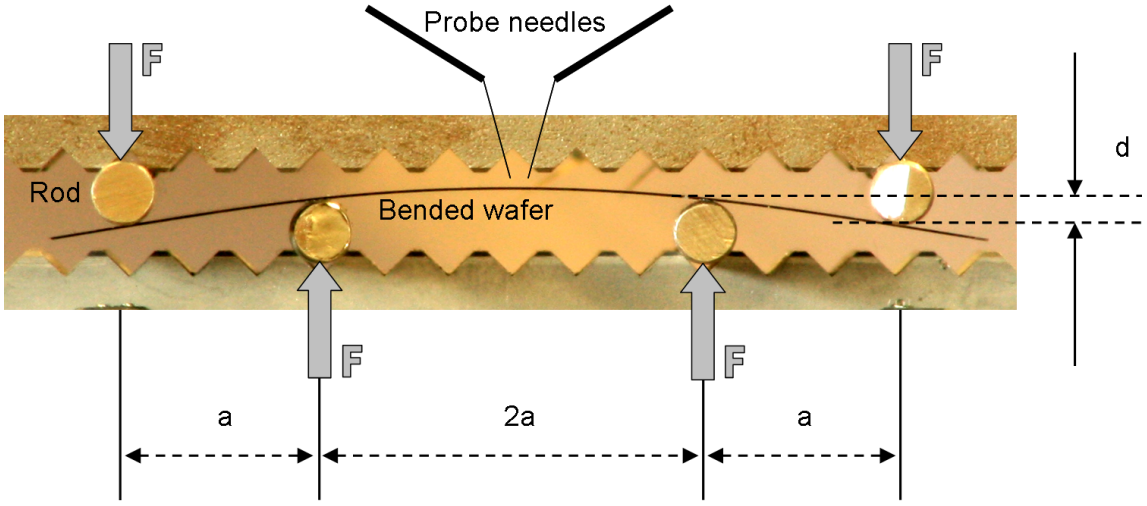


Figure B.1: Commented photograph of the four-point bending set-up; the wafer is 200 μm-thick in the illustration.

$$\pi_{NMOS,\parallel} = \frac{\left(I_{D,\sigma_1} - I_{D_0}\right)/I_{D_0}}{\sigma_{\parallel,1}}. \tag{B.3}$$

In order to provide some robustness to the measurement, a series of stress values σ_i with $i = \{1, 2, \cdots n\}$ may be applied to the device. A mean value of the π coefficient is provided by the slope of the linear regression of the measured $\left(I_{D,\sigma_i} - I_{D_0}\right)/I_{D_0}$, as illustrated in Figure B.2.

Additionally, provided that complete I_D-V_G curves are measured instead of single bias point for each stress value, the π coefficient may be extracted with the methodology described in Figure B.2 for all gate voltages. A more complete graph may then be plotted (Figure B.3), showing that the π coefficients depend on the bias conditions. This is a limitation to the piezoresistive phenomenological model. The linearity between the stress values (σ_i) and the current variations ($\left(I_{D,\sigma_i} - I_{D_0}\right)/I_{D_0}$) may be qualified by the evaluation of a residue, expressed by

$$R(V_G) = \left[\sum_{i=1}^{n} \left\{ \frac{\left(I_D(V_G,\sigma_i) - I_D(V_G,\sigma_0)\right)}{I_D(V_G,\sigma_0)} - \pi(V_G)\sigma_i \right\}^2 \right]^{1/2}. \tag{B.4}$$

This value is reported on the right-side vertical axis of Figure B.3. Complete results for both device doping-type (n and p) and both channel orientation ($\parallel$ and $\perp$) are reported in Section 5.3.3.

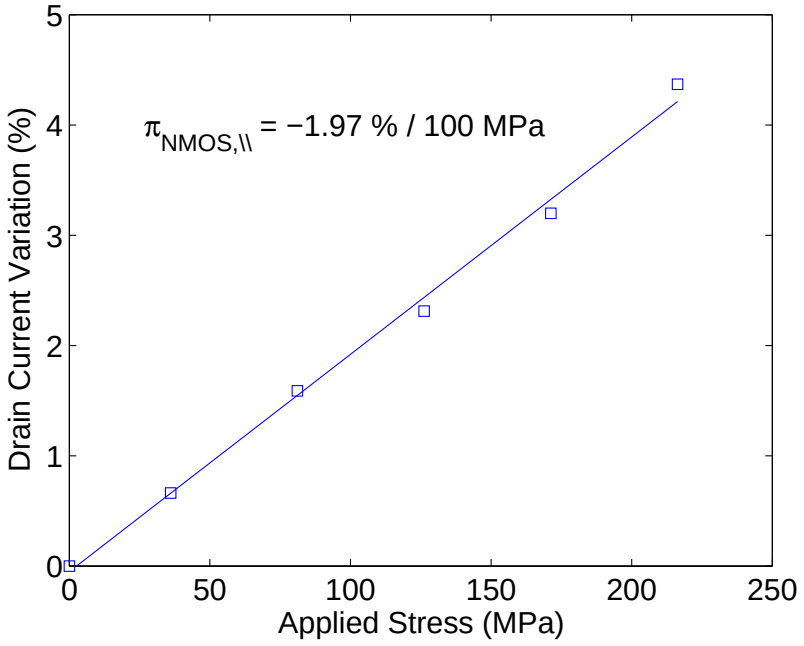


Figure B.2: π piezoresistive coefficient extraction for N-MOSFET from four-point bending set-up measurements; the device dimensions are 20 x 20 μm^2; the transistor is biased in saturation regime ($V_{DS} = V_G = +2V$, with $V_{GO} = 1.5$ V.

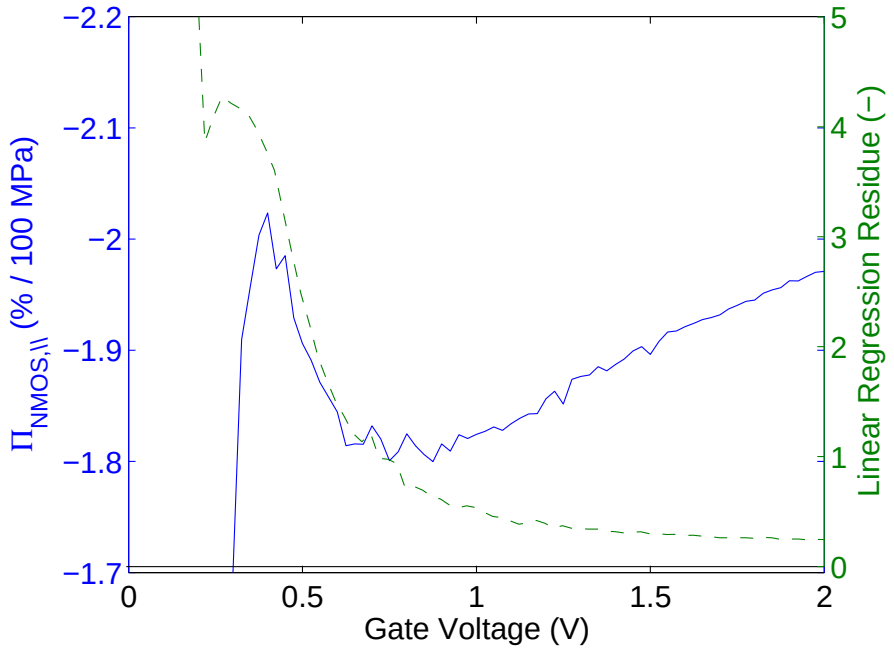


Figure B.3: Systematically extracted $\pi_{NMOS,\parallel}$ coefficient as a function of the gate voltage, $V_{DS} = +2V$.

Appendix C

Piezoresistive Coefficients Comparison

A representative number of piezoresistive coefficients present in the literature are reported in the following table.

Source	Technology	$\pi_{NMOS,\parallel}$	$\pi_{NMOS,\perp}$	$\pi_{PMOS,\parallel}$	$\pi_{PMOS,\perp}$
Smith [147]	Bulk Si	-3.10	-1.74	+7.19	-6.62
Thompson [159]	MOS	-3.55	-1.45	+7.17	-3.38
Bradley [27]	MOS IBM	-4.50	-3.50	+5.00	-4.50
	MOS TI	-3.20	-2.50	+4.15	-3.85
	MOS Lucent	-5.00	-3.50	+6.00	-4.00
Chang [33]	SOI MOS	-4.78	-3.01	+7.69	-5.63
Gallon [62]	SOI MOS	-4.97	-2.30	+6.48	-4.66
UCL [142]	*SOI MOS*	*-1.97*	*-1.23*	*+2.58*	*-2.43*

Table C.1: Piezoresistive coefficients reported in the literature for lightly doped bulk and SOI MOS technologies (1∼10 μm); units are %/100 MPa.

The coefficients measured for the UCL technology differ appreciably from those commonly reported. In this appendix, we list the technological specificities of each author and intend to draw hypothesis that could explain this difference.

Bradley in [27] extracts and compares the π coefficients of three technologies (IBM, Texas Instruments and Lucent). He mentions that "coefficient variations between processes are expected due to differences in technology details such as substrate (channel) doping and oxide thickness."

Moreover, he writes that π coefficients may appear higher than expected due to an insufficient biasing for entering the strong inversion and saturate the coefficients values. Furthermore, Bradley refers to "other researchers" who attribute discrepancies to "quantization within the quasi two-dimensional (2D) channel charge sheet."

Dr. Florent Rochette, in his remarkable PhD. dissertation [141], distinguishes the inversion layer (2D) from the bulk (3D) piezoresistivities in two points: (i) the sub-bands

occupancy is affected by the gate electric field, (ii) there are supplemental interactions occurring at the gate-dielectric / silicon interface. Three main surface interaction mechanisms, affected by the strain, are listed: (i) lattice phonons interaction, (ii) surface roughness diffusion, (iii) coulomb interaction with interface states. Dr. Rochette specifies that, due to these supplemental interactions, the mobilities $\mu_{2D} \approx \mu_{eff,3D}/3$ typically.

The core of Bradley's paper [27] concerns the study of the device channel length influence on the piezoresistive coefficients. As a result no such influence is noted, provided that a correction is made, due to the parasitic source resistance (Figure C.1). The investigated channel lengths ranged from 0.5 to 15 μm. Besides, Thompson [159] does not give the size of the analyzed devices: π coefficients are "extracted on industrial *long* n- and p-channel MOSFETs". He writes that coefficients are generally extracted at low strain and low electrical field. Chang [33] has measured 0.135, 0.45 and 10 μm-long devices in SOI technology. The full or partial depletion character of the technology is not mentioned. All devices were 10 μm-wide. He noticed a pronounced drain/source parasitic resistance effect for the short devices, but did not apply any correction on the measured π coefficients.

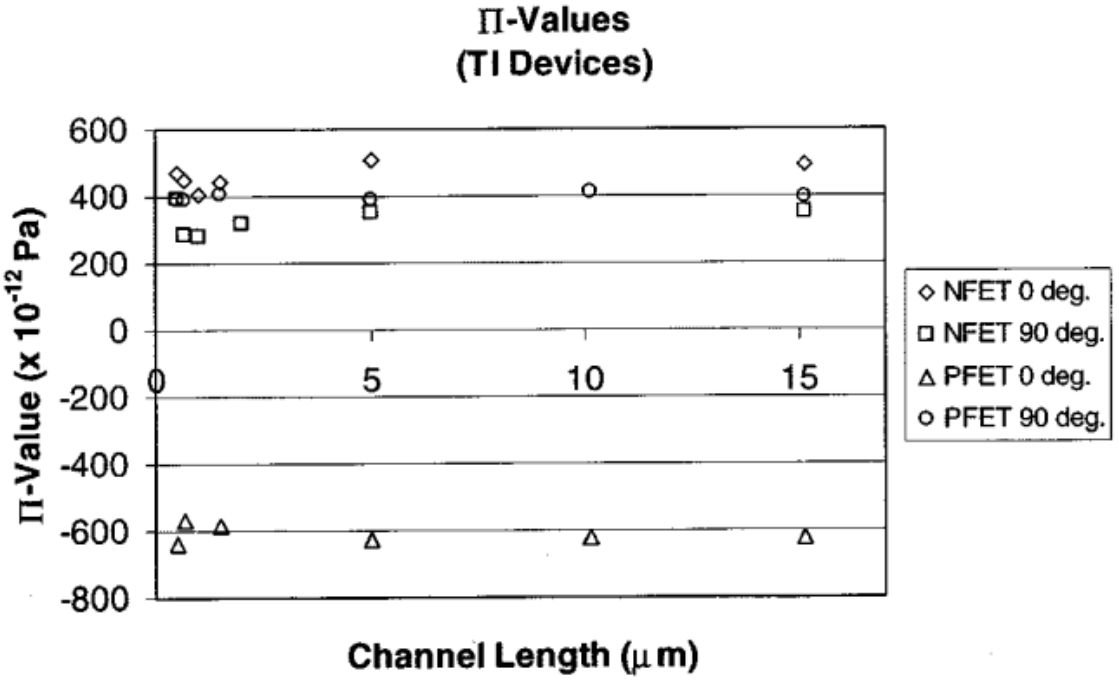


Figure C.1: Piezoresistive coefficients versus channel length for NMOS and PMOS devices in the Texas Instruments process [27].

The devices under test in Gallon [62] are 10 μm-wide and 0.13–10 μm-long either in bulk or PD SOI technologies. Devices with two different SOI processes were qualified (G01 and G02). The data reported in Table C.1 correspond to 10 μm-long, T_{ox}=6.5 nm devices from G02 process (high voltage devices). These coefficients are about 20% lower than wich obtained for similar device dimensions from G01 process (core devices). Both processes are very similar but differ in the gate oxide thickness (T_{ox}=2 nm for G01), thershold voltage

adjust, nominal length (0.13 μm for G01 and 0.35 μm for G02) and a slight source/drain implant adjustement.

In our case and from the analyzed papers, the difference between the measured π coefficients and typical values reported in Table C.1 cannot be explained by a simple gate oxide thickness change or an insufficient bias for entering strong inversion. Besides, the vertical electric field was investigated under- as well as over-the-threshold and reported in Table 5.2. As the gate oxide is 27 nm, the vertical electric field was varied from 0 to 0.74 MV/cm (V_G=2 V) for the NMOSFET and from 0 to -0.93 MV/cm (V_G=-2.5 V) for the PMOSFET. Fluctuations with the gate voltage were noticed but typical coefficient values were not obtained at any V_G. Besides, two authors (Gallon [62] and Chang [33]) have extracted the piezoresistive coefficients in saturation regime, as it is the case in the present work.

From Bradley [27], π divergence caused by parasitic source and drain resistances (R_{sd}) appeared only from 2 μm channel length. Although the devices under investigation in this work are 20 $\times$ 20 μm^2, this parameter could be checked. Indeed, Bradley noted that if $R_{sd}/R_{Channel} = 0.1$, the corresponding π coefficient may be affected by 40% according to the following relation:

$$\pi = \pi_{eff} \frac{1 + 2R_{sd}/R_{Channel}}{1 - 2R_{sd}/R_{Channel}} \tag{C.1}$$

where π and π_{eff} are respectively the actual and the measured piezoresistive coefficients.

Finally, the elements given by Claire Gallon, differentiating both SOI processes are also a starting point for further analysis. The reality is probably a combination a several of these parameters. Surface roughness or coulomb interactions with interface state may also be figured out to play a role. Nevertheless, no information is available concerning their order of magnitude. The influence of the Si film surface roughness is presently under investigation by Umesh Bhaskar [22].

Appendix D

Comsol - Simulations Framework

The descriptive comments provide directly from the Comsol Multiphysics User's Guide Version 3.3

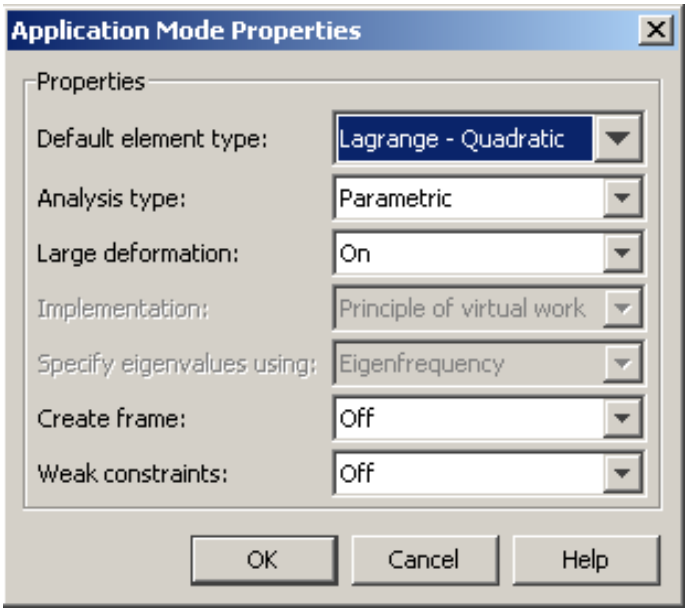


Figure D.1: Options selected for the Application Mode; the ruling application mode were "Solid, Stress-Strain (smld)" for the 3D models and "Plain Strain (smpn)" for the 2D models.

Lagrange Element Type

The preceding examples are special cases of the Lagrange element. Consider a positive integer k, the order of the Lagrange element. The functions u in this finite element space are piecewise polynomials of degree k, that is, on each mesh element u is a polynomial of degree k. To describe such a function it suffices to give its values in the Lagrange points of order k. These are the points whose local (element) coordinates are integer multiples

of $1/k$. For example, for a triangular mesh in 2D with $k = 2$, this means that you have node points at the corners and side midpoints of all mesh triangles. For each of these node points p_i, there exists a degree of freedom $U_i = u(p_i)$ and a basis function ϕ_i. The restriction of the basis function ϕ_i to a mesh element is a polynomial of degree (at most) k in the local coordinates such that $\phi_i = 1$ at node i, and $\phi_i = 0$ at all other nodes. Thus the basis functions are continuous and you have

$$u = \sum_i U_i \phi_i \tag{D.1}$$

The Lagrange element of order 1 is called the linear element. The Lagrange element of order 2 is called the quadratic element. The Lagrange elements are available with all types of mesh elements. The order k can be arbitrary, but the available numerical integration formulas usually limits its usefulness to $k \leq 5$ ($k \leq 4$ for tetrahedral meshes). *In this work the quadratic element was used.*

Convergence Criterion

The value in the Relative tolerance edit field gives the criterion for convergence; the value was set on 1e-6. The convergence criterion is as follows: Let U be the current approximation to the true solution vector, and let E be the estimated error in this vector. The relative error is the weighted Euclidean norm

$$err = \left(\frac{1}{N} \sum_i \left(|E_i| / W_i \right)^2 \right)^{1/2} \tag{D.2}$$

where N is the number of degrees of freedom. The software stops iterating when err is less than the relative tolerance. As the option *scaling* was set on automatic, the weight factors were $W_i = max(|U_i|, S_i)$, and S_i is 0.1 times the average of $|U_j|$ for all DOFs j having the same name as DOF i.

SPOOLES Direct Solver

The SPOOLES solver works on general systems of the form $Ax = b$ using the multifrontal method and direct LU factorization of the sparse matrix A. When the matrix A is symmetric or Hermitian, the solver uses an LDLT version of the algorithm, which saves half the memory. SPOOLES uses several preordering algorithms to permute the columns and thereby minimize the fill-in. The code is written in C. COMSOL Multiphysics uses SPOOLES version 2.2 developed by Cleve Ashcraft and collaborators (see http://www.netlib.org/linalg/spooles).

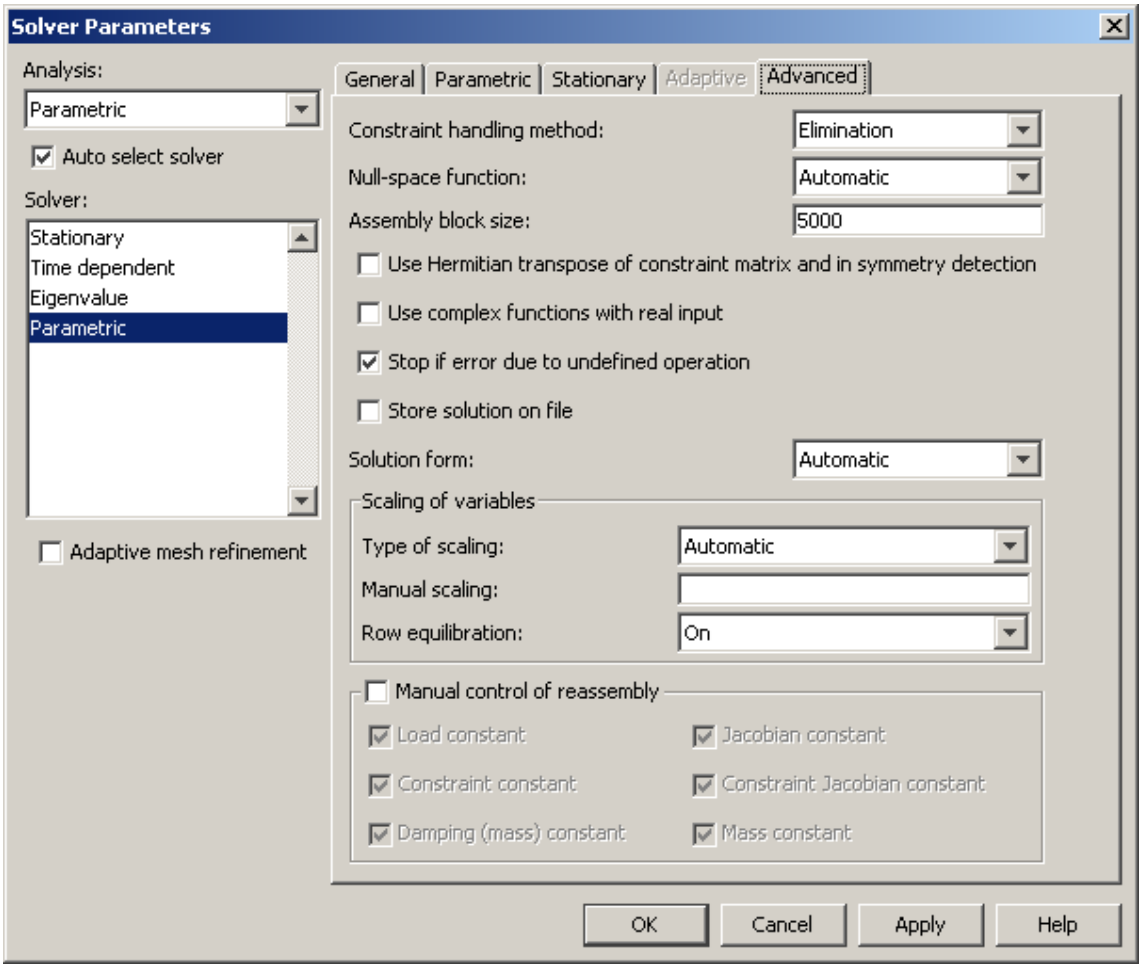


Figure D.2: Advanced solver parameters.

Extended mesh:	
Number of degrees of freedom:	126075
Base mesh:	
Number of mesh points:	5733
Number of elements:	4800
Tetrahedral:	0
Prism:	0
Hexahedral:	4800
Number of boundary elements:	2960
Triangular:	0
Quadrilateral:	2960
Number of edge elements:	448
Number of vertex elements:	20
Minimum element quality:	1.37E-4
Element volume ratio:	2.40E-4

(a) No patterning

Extended mesh:	
Number of degrees of freedom:	130041
Base mesh:	
Number of mesh points:	5940
Number of elements:	4925
Tetrahedral:	0
Prism:	0
Hexahedral:	4925
Number of boundary elements:	4432
Triangular:	0
Quadrilateral:	4432
Number of edge elements:	1088
Number of vertex elements:	77
Minimum element quality:	2.08E-4
Element volume ratio:	9.31E-4

(b) Global patterning

Extended mesh:	
Number of degrees of freedom:	202929
Base mesh:	
Number of mesh points:	9172
Number of elements:	12664
Tetrahedral:	0
Prism:	9790
Hexahedral:	2874
Number of boundary elements:	9686
Triangular:	5340
Quadrilateral:	4346
Number of edge elements:	1848
Number of vertex elements:	185
Minimum element quality:	0.0038
Element volume ratio:	7.81E-5

(c) Local patterning, mesh1

Extended mesh:	
Number of degrees of freedom:	283071
Base mesh:	
Number of mesh points:	12853
Number of elements:	10776
Tetrahedral:	0
Prism:	0
Hexahedral:	10776
Number of boundary elements:	10762
Triangular:	0
Quadrilateral:	10762
Number of edge elements:	2259
Number of vertex elements:	143
Minimum element quality:	7.95E-5
Element volume ratio:	2.37E-5

(d) Local patterning, mesh2

Figure D.3: Mesh statistics from Chapter 3 Comsol models.

Extended mesh:	
Number of degrees of freedom:	100467
Base mesh:	
Number of mesh points:	4805
Number of elements:	3600
Tetrahedral:	0
Prism:	0
Hexahedral:	3600
Number of boundary elements:	4980
Triangular:	0
Quadrilateral:	4980
Number of edge elements:	616
Number of vertex elements:	20
Minimum element quality:	0.0025
Element volume ratio:	6.67E-4

(a) 3D blanket membrane

Extended mesh:	
Number of degrees of freedom:	86913
Base mesh:	
Number of mesh points:	4150
Number of elements:	3120
Tetrahedral:	0
Prism:	0
Hexahedral:	3120
Number of boundary elements:	4764
Triangular:	0
Quadrilateral:	4764
Number of edge elements:	1144
Number of vertex elements:	80
Minimum element quality:	0.0011
Element volume ratio:	3.89E-4

(b) 3D patterned membrane

Extended mesh:	
Number of degrees of freedom:	23714
Base mesh:	
Number of mesh points:	3073
Number of elements:	5712
Triangular:	5712
Quadrilateral:	0
Number of boundary elements:	1552
Number of vertex elements:	73
Minimum element quality:	0.5547
Element area ratio:	0.0090

(c) 2D - along Y-Axis

Extended mesh:	
Number of degrees of freedom:	34316
Base mesh:	
Number of mesh points:	4427
Number of elements:	8305
Triangular:	8305
Quadrilateral:	0
Number of boundary elements:	1964
Number of vertex elements:	105
Minimum element quality:	0.5146
Element area ratio:	0.0081

(d) 2D - along X-Axis

Figure D.4: Mesh statistics from Chapter 5 Comsol models.

Appendix E

Measurement set-up and testing

The wafers under study were systematically inspected by IR transmission imagery before and after annealing. The surface energy was extracted dynamically using the steady-state wedge opening method [20]. The measurement set-up is represented in Figure E.1a. A razor blade of 100 μm thick (u) was mounted on a universal mechanical testing machine. The blade was inserted between the two wafers of thickness h (380 μm) and moved at a constant rate by means of a computer control. This home-made set-up can perform steadily dynamic surface energy measurement not only at the perimeter of the bonded wafer pairs as usual but at any locations of the diced samples. Simple beam theory leads to the following relationship between the crack length and the surface energy for the configuration presented in Figure E.1:

$$\gamma = \frac{3Eu^2h^3}{32a^4}, \tag{E.1}$$

where E is the uniaxial Young's modulus (150 GPa in our experiments), a is the crack length, u is the wedge thickness, h is the wafers thickness.

An image acquisition software (VISILOG 5.0) was used to record the images and measure the crack length at any testing time. The impact of the triangle tip height (0.4635 mm) of the blade on surface energy extraction (increasing the real crack length) was also corrected in our calculations. The resulting accuracy of the crack length measurement is about of 0.1 mm (1 pixel $\approx$ 0.1 mm). The error bars indicated on the surface energies graphs trace the highest and lowest levels of surface energy measured on the samples under concern.

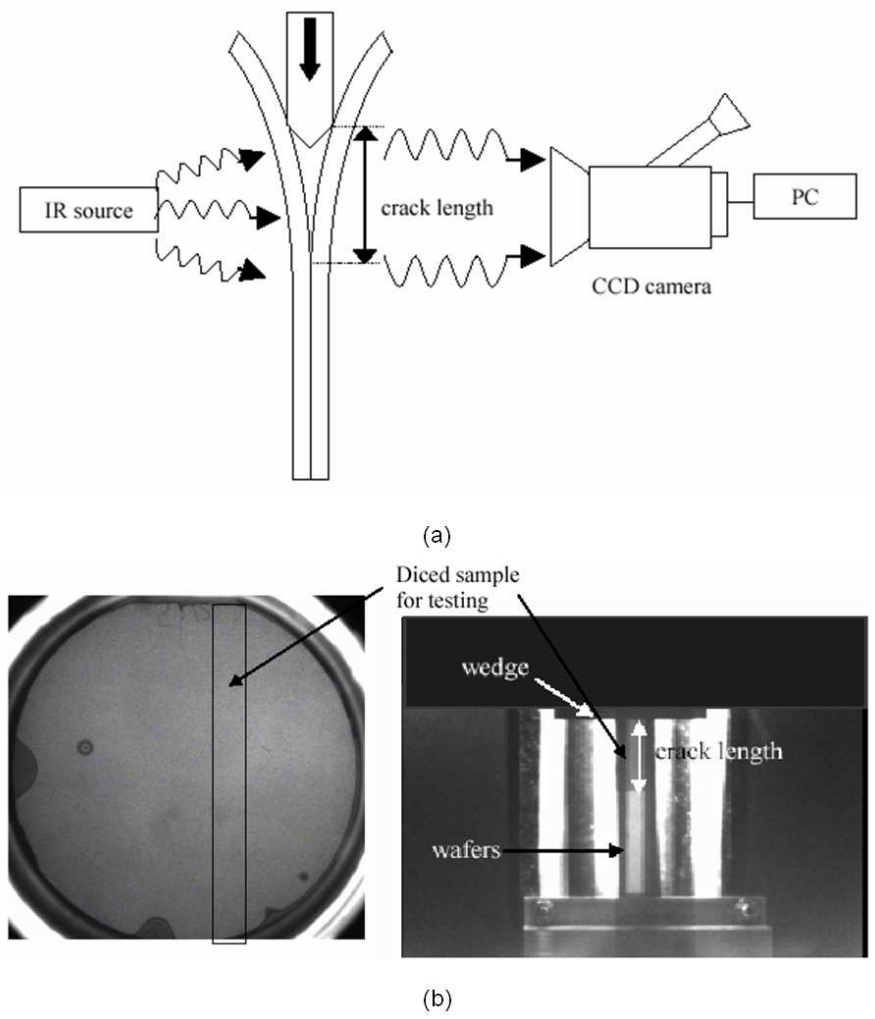


Figure E.1: Wedge-opening test: (a) principle, (b) set-up of measurement.