Solid-State Electronics 230 (2025) 109261

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Trap-rich high-resistivity silicon for improved on-chip monolithic transformers characteristics

Najeh Zeidi [a,b], Farès Tounsi [a,b], Jean-Pierre Raskin [c], Denis Flandre [a,*]

[a] SMALL Research Group, ICTEAM Institute, UCLouvain, Belgium
[b] SI2E Laboratory, National Engineering School of Sfax (ENIS), Sfax University, Tunisia
[c] RF-SOI Research Group, ICTEAM Institute, UCLouvain, Belgium

ARTICLE INFO

The review of this paper was arranged by Francisco F. Gamiz
Handling Editor: Francisco F. Gamiz

Keywords:
On-chip planar transformers
High-resistivity silicon (HR-Si)
Trap-rich layer
Power-transfer efficiency
Substrate losses
Interleaved transformer
Concentric transformer
Mutual inductance

ABSTRACT

This paper investigates the performance of monolithic on-chip planar transformers implemented on high-resistivity substrates incorporating a trap-rich layer (HR-Si + TR), using both experimental measurements and electromagnetic simulations. Two transformer topologies, i.e., interleaved and concentric, were fabricated, measured, and simulated on both standard silicon (Std-Si) and HR-Si + TR to assess the impact of substrate losses. Key figures of merit, including self-resonant frequency (SRF), mutual inductance, reactive and resistive coupling factors, and maximum power-transfer efficiency, were extracted and compared. Results show that the HR-Si + TR substrate markedly enhances both topologies: for the interleaved transformer, the SRF increases by 3.8 % from 3.66 to 3.80 GHz, while the peak power-transfer efficiency nearly doubles from 0.33 at 1.42 GHz to 0.63 at 2.26 GHz; for the concentric transformer, the SRF rises by over 31 % from 3.12 to 4.10 GHz, and the efficiency increases more than threefold from 0.06 at 1.48 GHz to 0.22 at 2.15 GHz. These improvements arise from the HR-Si + TR substrate's ability to substantially reduce the resistive mutual coupling factor by minimizing eddy current losses in the substrate and raising the impedance of the RC leakage path to ground, thereby limiting trace crosstalk and power leakage between traces. The benefits are particularly pronounced in the concentric topology, where the larger winding separation amplifies the impact of reduced substrate-induced losses.

1. Introduction

The integration of high-quality magnetic components via silicon microfabrication techniques is a critical step toward miniaturized and highly integrated power converters [1]. This challenge is particularly acute in the context of high-voltage digital isolators, where the miniaturization of inductors and transformers is constrained by stringent efficiency and reliability requirements. The need for large physical dimensions arises from the necessity to prevent thermal stress, line melting, partial discharges, and electrical breakdown, which are likely to occur in high-voltage environments [2]. Consequently, a significant deal of research has been devoted to inductor integration, with an emphasis on minimizing losses, maximizing the quality factor (Q), and achieving the highest inductance value within the smallest footprint [3–6]. Along with the use of high-permeability materials, substrate resistance is a key factor affecting performance [7]. Indeed, the low-resistivity silicon substrates used in the standard CMOS manufacturing process have historically limited the integration of high-quality passive components like spiral inductors, capacitors, and transformers [8]. High-resistivity (HR) silicon substrates have been proposed to mitigate substrate noise and enhance the Q-factor of these components [9]. However, parasitic surface conduction (PSC) at the oxide/HR-Si interface can offset these benefits [10–12]. The incorporation of a trap-rich (TR) layer on high-resistivity silicon (HR-Si) effectively suppresses PSC, significantly improving the performance of integrated spiral inductors [13,14]. This configuration directly affects all key parameters, including resonant frequency, Q-factor, and parasitic capacitances, enhancing overall efficiency and performance [7].

Similarly, the performance of inductor-based integrated micro-transformers is highly dependent on substrate resistivity [15], making its optimization a crucial step for their integration into CMOS technology [16]. Numerous studies have highlighted the critical role of substrate material in determining transformer performance, particularly at RF and microwave frequencies. For instance, Feng et al. [17] demonstrated that low-resistivity silicon (10 Ω·cm) results in significant intrinsic losses, whereas high-resistivity silicon (10 kΩ·cm) offers

* Corresponding author.
E-mail address: denis.flandre@uclouvain.be (D. Flandre).

https://doi.org/10.1016/j.sse.2025.109261
Received 8 July 2025; Received in revised form 16 September 2025; Accepted 30 September 2025
Available online 8 October 2025

superior performance by reducing power dissipation and enhancing the *Q*-factor, making it more suitable for high-frequency applications. Yunas et al. [18] showed that replacing standard silicon (Std-Si) with a high-resistivity glass substrate improved performance, including an increase in the resonant frequency from 60 MHz to 80 MHz and a doubling of the coil quality factor. Similarly, Chen et al. [19] reported that glass substrates improve transformer bandwidth and reduce losses. Advanced substrates, such as microporous silicon, have been shown to mitigate substrate-induced effects, such as eddy currents and capacitive coupling, leading to higher *Q*-factors, improved resonant frequencies, and increased maximum gain due to minimized power loss [20–22]. Substrate removal techniques, such as etching the silicon beneath the transformer and transferring the device on quartz, can also enhance performance by reducing the mutual resistive coupling factor and increasing maximum gain from 0.4 to 0.6, though these approaches face significant practical challenges for large-scale production [16]. The use of organic substrates, such as depositing thick polyimide layers after etching the silicon, has enabled integrated transformers to achieve ultra-high isolation (exceeding 7.5 kV) and exceptional efficiency (reaching 89.55 % at 374 MHz) across wide frequency ranges [23]. Nevertheless, techniques like backside etching or suspending the transformer structure pose significant challenges. In fact, these techniques carry a high risk of damaging the transformer structure and are less practical for mass production of RF integrated circuits, as they require costly, non-standard processing steps.

In this work, we introduce, for the first time, the use of a high-resistivity silicon with a trap-rich layer (HR-Si + TR) to implement and evaluate two on-chip transformer topologies: an interleaved transformer and a concentric transformer. This substrate, previously shown to simplify fabrication and enhance the performance of various passive components, was selected for its ability to suppress dominant substrate loss mechanisms. The HR-Si + TR technology combines bulk conduction reduction with the suppression of parasitic surface currents via the trap-rich layer, thereby enhancing substrate impedance at RF/microwave frequencies. This effectively reduces eddy-current and leakage-path losses, a benefit previously demonstrated for other RF passives, including CPW lines [24,25], inductors [7], and MIM capacitors [26], while maintaining full CMOS compatibility. To validate this approach, both transformer designs were fabricated and characterized on Std-Si and HR-Si + TR substrates, with key figures of merit, including *Q*-factor, coupling coefficients, self-resonant frequency (SRF), and power-transfer efficiency, assessed through experiments and electromagnetic simulations. Direct comparison of these metrics across substrates and topologies allows us to quantify the specific impact of the HR-Si + TR substrate and highlight its advantages for practical, high-performance, CMOS-compatible passive integration.

The paper is organized as follows: Section 2 describes the microfabrication flow used to produce the two transformers on both substrates. Section 3 introduces the figures of merit employed to evaluate the impact of substrate losses on transformer performance. Section 4 compares measurement results with electromagnetic simulations for the four structures and outlines the de-embedding procedure. Section 5 presents the results for the individual winding characteristics, followed by a detailed analysis of transformer performance. Finally, Section 6 concludes the work.

2. Fabrication process flow

To investigate the influence of substrate RF losses on transformer performance, two monolithic transformers were designed and fabricated: a high-coupling interleaved transformer and a low-coupling concentric transformer. These devices were implemented on two types of silicon substrates: (i) a Std-Si with a resistivity of 15 Ω·cm, and (ii) an HR-Si with a resistivity of 5kΩ·cm incorporating a 500 nm-thick TR undoped top polysilicon layer with a resistivity of approximately 10 kΩ·cm [27]. The aim of this research is not to determine which topology is inherently superior, but rather to quantify and explain, through measurements and simulations, how the HR-Si + TR substrate impacts each topology independently. The interleaved and concentric topologies were selected, on the one hand, for their ease of fabrication, as they require only two metal layers: one for the underpasses and another for the primary and secondary windings, and, on the other hand, because the substrate influences both windings simultaneously, unlike stacked transformers. In the stacked configuration, the upper winding is decoupled from the substrate and therefore experiences different loss mechanisms than the lower winding [28]. In the proposed topologies, magnetic coupling occurs primarily laterally (within the same metal layer) rather than vertically (across layers). This results in a more moderate coupling coefficient compared to stacked transformers but offers the advantage of lower interwinding capacitance owing to weaker lateral coupling between adjacent traces.

In the Std-Si process flow, insulation is provided by a 500 nm-thick thermally grown SiO_2 layer (wet atmosphere, 1000 °C), while in the HR-Si case, a 500 nm-thick undoped polysilicon layer is inserted beneath a 500 nm-thick PECVD (plasma enhanced chemical vapor deposition) SiO_2 layer. The transformer microfabrication process is identical for both substrates and involves three photolithography steps. Firstly, a 1 μm-thick aluminum (Al) layer is sputtered by e-beam ($\sigma = 1.72 \times 10^7$ S/m) and patterned as the underpasses in the two transformers. Secondly, a 0.8 μm-thick PECVD SiO_2 is deposited to serve as an insulating layer between the two conductive layers. The oxide is deposited in an Oxford Plasmalab System 100 (300 °C, 1 Torr, 30 W RF, 13.56 MHz, N_2O/SiH_4 ratio of 7). The SiO_2 layer is then photolithography patterned and etched with BHF (buffered hydrofluoric acid) to open vias to contact the bottom and top Al layers. Thirdly, a second metal deposition step (2 μm-thick of Al) is used to define transformer spiral coils, GSG (ground-signal-ground) access pads, and surrounding ground, with etching performed in a Corial system using a BCl_3 (boron trichloride) and Cl_2 (chlorine) mixture for dimensional accuracy. The main geometric parameters are the number of turns (N), track width (w), spacing between turns (s), track thickness (t), inner diameter (d), outer diameter (D), and spacing between the two concentric inductors (S), which are listed in Table 1 and illustrated in Fig. 1. For both topologies, *N*, *w*, and *s* are the same for primary and secondary windings.

3. Figure-of-merit for on-chip transformers

To investigate the effect of substrate losses on the transformer figure-of-merit, the first step is to analyze the influence of silicon substrate conductivity on each winding individually. This can be done by extracting the characteristics of each inductor in the low frequency (LF) band, below the self-resonant frequency (SRF), directly from the Z-matrix [29–31]. Specifically, the self-inductances (L_1 and L_2, from Eq. (1) with indices 1 and 2 denoting the primary and secondary windings, respectively), the *Q*-factors (Q_1 and Q_2, from Eq. (2), and the resonance frequencies (f_{r1} and f_{r2}, defined as the frequencies where *Q* falls to zero) are determined and compared for both topologies across the two evaluated substrates.

$$L_i = \frac{\Im(Z_{ii})}{2\pi f}\Big|_{f\to low-band};\ i = (1 \text{ or } 2) \tag{1}$$

$$Q_i = \frac{\Im(Z_{ii})}{\Re(Z_{ii})};\ i = (1 \text{ or } 2) \tag{2}$$

Table 1
Geometric dimensions of the two designed transformers (all values in μm, except N, which is unitless).

Parameters	*N*	*w*	*s*	*t*	*S*	*d*	*D*
Interleaved	3	20	10	2	10	280	620
Concentric	2	11	4	2	75	580	820

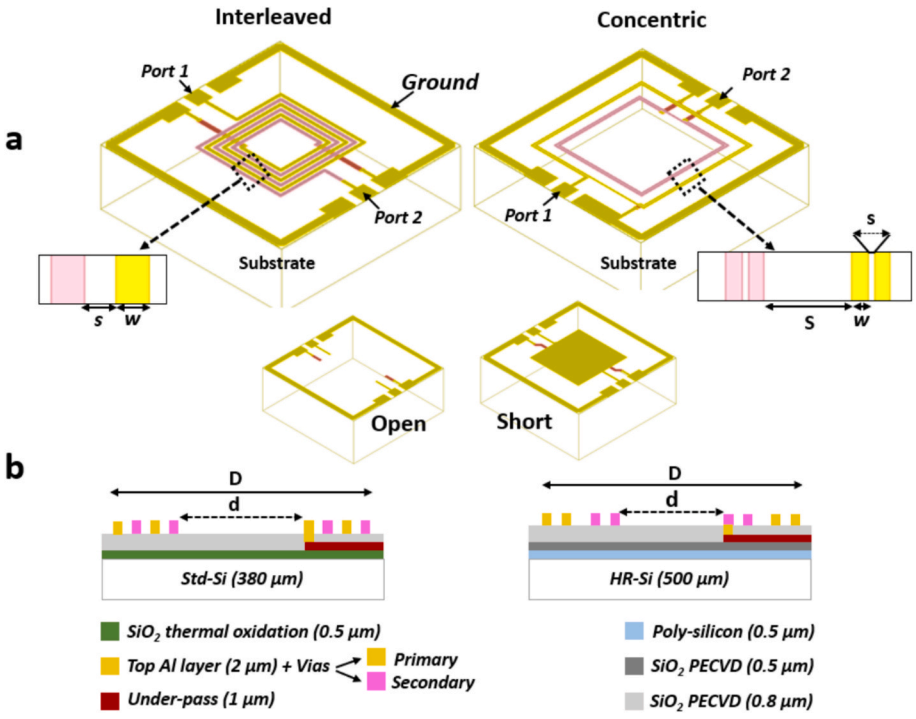

Fig. 1. Microfabrication overview: (a) perspective views of the designed structures, interleaved (left) and concentric (right), on the substrates (shown to scale), including the open and short calibration dummy structures; and (b) cross-sectional views illustrating the track arrangements in both topologies (interleaved, left; concentric, right) as well as the layer stacks in Std-Si and HR-Si + TR substrates. Both transformer topologies were fabricated on each substrate type.

In a second step, for an on-chip monolithic transformer intended for power-transfer applications, performance can be described in terms of the mutual inductance M (given in Eq. (3), the reactive and resistive mutual coupling factors K_{re} and K_{im} (given in Eqs. (4) and (5), respectively), and the maximum available gain, or power efficiency, G_{max} (given in Eq. (6) [23]. The latter serves as the most appropriate figure-of-merit, as it quantifies the maximum power gain achievable in passive RF components when both input and output ports are conjugately matched (for maximum power transfer). G_{max} can be derived from the Z-parameters and depends on the Q-factors of the primary and secondary windings, as well as the reactive and resistive coupling factors [16].

$$M = \frac{\Im(Z_{12})}{2\pi f}\Big|_{f\to low-band} \tag{3}$$

$$K_{re} = \sqrt{\frac{\Re(Z_{12}).\Re(Z_{21})}{\Re(Z_{11}).\Re(Z_{22})}}\Big|_{f\to low-band} \tag{4}$$

$$K_{im} = \sqrt{\frac{\Im(Z_{12}).\Im(Z_{21})}{\Im(Z_{11}).\Im(Z_{22})}}\Big|_{f\to low-band} \tag{5}$$

$$G_{max} = 1 + 2\left(x - \sqrt{x^2 + x}\right), \text{where } x = \frac{1 - {K_{re}}^2}{{K_{im}}^2 Q_1 Q_2 + {K_{re}}^2} \tag{6}$$

According to Eq. (6), it is clear that increasing the Q-factors and/or enhancing the mutual coupling directly leads to an increase in G_{max}. Therefore, improving transformer performance requires both maximizing the Q-factor of each winding and optimizing the coupling between ports. The following section analyzes these aspects in detail.

4. On-chip measurements validation

On-chip measurements were carried out at room temperature using a pair of GSG Infinity probes connected to a Keysight N5242B PNA-X vector network analyzer (26.5 GHz). A Short-Open-Load-Through (SOLT) calibration was performed in advance to establish the reference planes at the probe tips over the frequency range of 10 MHz–10 GHz. The measured S-parameters of the transformers resulting from experimental characterization were validated in Advanced Design System (ADS) software using the following material parameters: *(i)* the HR-Si substrate has a relative dielectric constant of 11.9, as specified by the manufacturer, while the deposited trap-rich polysilicon layer has a relative dielectric constant of 11.8 [27]; *(ii)* the thermally oxidized SiO_2, known for its high quality, has a relative dielectric constant of 4, consistent with reported values of 3.9–4.5 [32]; *(iii)* the dielectric constant of the PECVD SiO_2 layer was measured to be about 5.8 through the characterization of a metal-oxide-metal (MOM) capacitor fabricated with the same in-house process; and *(iv)* the electrical conductivity of Al, determined from resistance measurements of individual inductors, corresponding to about 1.72×10^7 S/m. The last two measurements were performed at 1 MHz using a 4284A LCR meter and an MP8MS probe station.

After ADS validation of the on-chip measurements, a de-embedding procedure was applied to both measured and simulated S-parameters to remove the effects of on-chip access pads, interconnect tracks, and parasitic ground planes. This allowed accurate extraction of the intrinsic transformer Z-parameters. The de-embedded Z-parameters (whether measured or simulated) were derived from the extrinsic S-parameters of the DUT (S^{DUT}), the open dummy (S^{open}), and the short dummy (S^{short}), according to the following equations sequence [33], where Y-parameters denote the admittance at each port derived from S-parameters [34].

$$Y^{DUT1} = Y^{DUT} - Y^{open} \tag{7}$$

$$Y^{short1} = Y^{short} - Y^{open} \tag{8}$$

$$Z = Z^{DUT1} - Z^{short1} \tag{9}$$

5. Transformers' figures of merit extraction

5.1. Individual winding characteristics

The measured and simulated curves used to extract the primary (L_1) and secondary (L_2) self-inductances of the two transformers on Std-Si and HR-Si + TR substrates are plotted in Fig. 2. In both cases, the curves remain relatively constant over a broad frequency range (10 MHz to 1 GHz), and values were extracted from the stationary region at 50 MHz. For the interleaved transformer, L_1 and L_2 are almost identical, close to 6 nH, reflecting the nearly identical geometry of the primary and secondary windings. For the concentric transformer, the larger primary winding results in a higher inductance for L_1 (9 nH) compared to L_2 (7 nH). Notably, the HR-Si + TR substrate consistently provides slightly higher inductance values, as confirmed by both measurements and simulations (see Tables 2 and 3 for interleaved and concentric topologies, respectively). This effect arises because the low-resistivity Std-Si substrate supports stronger eddy currents (Faraday's law) induced by the time-varying magnetic field of the spiral windings. These eddy currents generate opposing magnetic fields that partially cancel the primary flux, thereby lowering the effective inductance. By suppressing these losses, the HR-Si + TR substrate yields higher inductance values [35]. These findings are in agreement with previous studies on large spiral inductors comparing Std-Si, HR-Si, and HR-Si + TR substrates [7] Table 4.

Measured and simulated quality factor curves of the primary (Q_1) and secondary (Q_2) windings for both transformers on the two substrates are depicted in Fig. 3. The Q-factor, defined as the ratio of magnetic energy stored to energy dissipated per cycle, is a key indicator of inductor efficiency, with higher values reflecting lower losses. On Std-Si substrates, the low resistivity severely limits Q due to *(i)* strong eddy current losses induced by the inductor's time-varying magnetic field since more energy dissipation as heat ($P = I^2_{eddy}R_{sub}$), which thus increases the effective inductor series resistance, and *(ii)* the presence of larger parasitic capacitance (C_{sub}), which forms a lossy RC path to ground that leaks energy into the substrate [7]. Therefore, the presence of more intense eddy currents in the substrate dissipates more energy in the form of heat, which presents parasitic power not stored in the magnetic field of the inductor. In contrast, HR-Si + TR substrates, which offer higher resistivity (minimal eddy currents and therefore lower resistive losses) and improved insulation (dielectric losses are reduced), lead to a substantial improvement in the Q-factor [7]. In particular, for the interleaved transformer, the maximum primary Q_1 increases by about 2.7 times, from 2.11(@1.16 GHz) for Std-Si to 5.76(@2.09 GHz) on HR-Si + TR. For the concentric transformer, Q_1 max improves 2.8 times, from 1.32(@1.21 GHz) to 3.72(@2.07 GHz). These improvements are consistent across both topologies and closely match simulations (see Tables 2 and 3). The improved Q-factor does not only increase the efficiency of the inductors but also broadens their potential for use in RF/

Table 2
Measured and simulated characteristics of the interleaved transformer on Std-Si and HR-Si + TR substrates.

	Std-Si		HR-Si + TR	
	Meas	ADS	Meas	ADS
L_1 (nH)	6.019	5.875	6.110	6.013
L_2 (nH)	5.918	5.887	6.144	6.030
Q_1 max	2.111 @ 1.16 GHz	2.217 @ 1.17 GHz	5.761 @ 2.09 GHz	6.946 @ 2.54 GHz
Q_2 max	1.966 @ 1.16 GHz	2.216 @ 1.17 GHz	5.613 @ 2.23 GHz	6.906 @ 2.54 GHz
f_{r1} (GHz)	4.35	4.35	4.5	4.5
f_{r2} (GHz)	4.41	4.41	4.6	4.6
M (nH)	4.457	4.465	4.508	4.487
K_{im}	0.75	0.76	0.74	0.744
G_{max}	0.33 @ 1.42 GHz	0.35 @1.42 GHz	0.636@2.26 GHz	0.683@2.42 GHz
f_{res} (GHz)	3.66	3.7	3.8	3.9

Table 3
Measured and simulated characteristics of the concentric transformer on Std-Si and HR-Si + TR substrates.

	Std-Si		HR-Si + TR	
	Meas	ADS	Meas	ADS
L_1 (nH)	8.421	8.565	9.432	9.037
L_2 (nH)	6.756	6.600	7.381	6.983
Q_1 max	1.322 @ 1.21 GHz	1.40@ 1.22 GHz	3.721 @ 2.07 GHz	3.930 @ 2.24 GHz
Q_2 max	1.482 @ 1.5 GHz	1.490 @ 1.5 GHz	4 @ 2.56 GHz	4.610 @ 2.68 GHz
f_{r1} (GHz)	3.39	3.93	4.29	4.29
f_{r2} (GHz)	3.8	3.8	5	5
M (nH)	2.482	2.771	2.85	2.784
K_{im}	0.33	0.37	0.33	0.35
G_{max}	0.06 @ 1.48 GHz	0.07 @ 1.48 GHz	0.22 @ 2.15 GHz	0.26 @ 2.4 GHz
f_{res} (GHz)	3.12	3.12	4.1	4.2

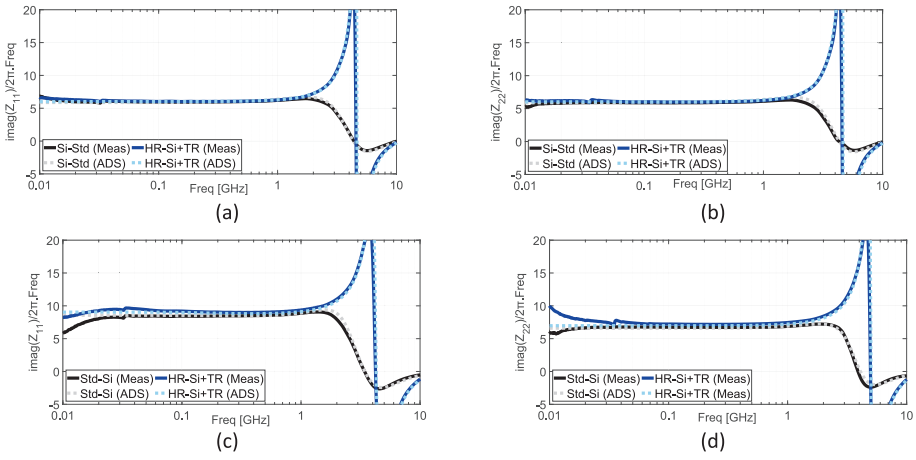

Fig. 2. Measured (solid lines) and simulated (dashed lines) self-inductances L_1 and L_2 on Std-Si and HR-Si + TR substrates for (a and b) the interleaved transformer and (c and d) the concentric transformer.

Table 4
Comparison of transformer performance across different substrate types.

Reference	Substrate	CMOS compatible	G_{max}	f_{res} (GHz)
[16]	Std-Std/ Quartz	Yes	0.4 @ 5 GHz/0.6 @ 8 GHz	–-
[18]	Std-Si/glass	No	–-	0.064/ 0.08
[20]	Std-Si/Si-porous	No	0.53 @ 3.3 GHz/ 0.77 @ 5.4 Ghz	4.4/ 11.3
Our work (interleaved)	Std-Si/HR-Si + TR	Yes	0.33 @ 1.42 GHz/0.63 @ 2.26 GHz	3.66/ 3.8
Our work (concentric)	Std-Si/HR-SI + TR	Yes	0.06 @ 1.48 GHz/0.26 @ 2.4 GHz	3.12/ 4.1

mmWave applications. Moreover, the HR-Si + TR substrate reduces parasitic capacitance between the inductor traces and the substrate, shifting the frequency range of maximum Q upward and yielding higher resonant frequencies. Specifically, the measured resonant frequency f_{r1} of the primary winding increases by about 3.6 % (from 4.35 GHz to 4.50 GHz) in the interleaved case and by about 25 % (from 3.39 GHz to 4.29 GHz) in the concentric case (see Tables 2 and 3). This observation has been validated in both transformer topologies, as evidenced by the delayed zero-crossing of the Q curve in the HR-Si + TR case compared to the Std-Si substrate (Fig. 3). Altogether, the reduction of substrate losses and parasitic capacitance explains the clear improvement in transformer performance on HR-Si + TR substrates, in line with previous studies on spiral inductors [7].

5.2. Transformers' figure-of-merit

The performance of the transformers as a function of substrate losses was analyzed at two levels of coupling. The first, purely inductive, considers *(i)* the mutual inductance (M) between the primary and secondary windings, which quantifies the electromagnetic coupling through the intertwined inductor traces, and *(ii)* the reactive mutual coupling factor (K_{im}), or simply coupling coefficient k, which indicates the efficiency of magnetic flux linkage between the windings (with $k = 1$ representing ideal lossless coupling). The latter is defined as the ratio of mutual inductance to the geometric mean of the self-inductances. At microwave frequencies (>1GHz), distributed effects become significant as the wavelength approaches the physical dimensions of the traces. Fig. 4 presents the measured and simulated M and k for the interleaved

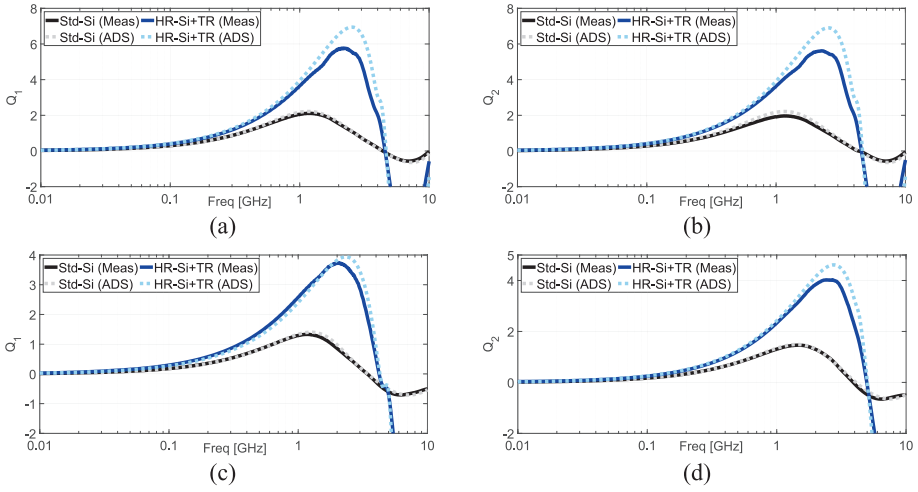

Fig. 3. Measured (plain lines) and simulated (dashed lines) Q_1 and Q_2 on Std-Si and HR-Si + TR substrates for (a and b) the interleaved transformer and (c and d) the concentric transformer.

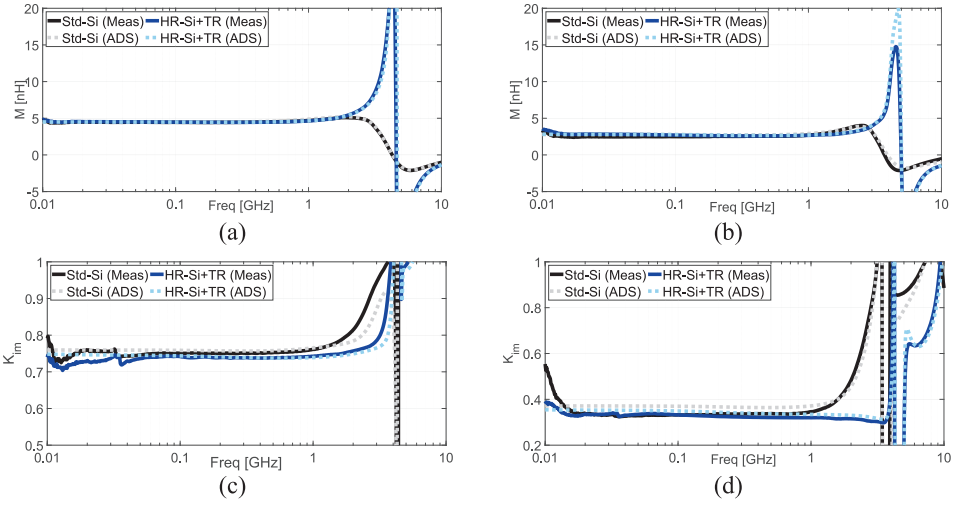

Fig. 4. Measured and simulated mutual inductance M and reactive coupling factor k on Std-Si and HR-Si + TR substrates, (a and c) for the interleaved transformer and (b and d) for the concentric transformer.

and concentric transformers on Std-Si and HR-Si + TR substrates. Again, eddy currents induced in the high-ρ substrate can slightly increase the net mutual inductance (see Tables 2 and 3, values extracted at 50 MHz). However, since k ($= M/\sqrt{L_1 L_2}$) is a function of the mutual inductance and self-inductances, and all decrease almost proportionally, k may remain unaffected. These results indicate that M and k primarily depend on the geometry and relative arrangement of the windings, with only minor influence from substrate resistivity. It is also noteworthy that poorly coupled or asymmetric transformer designs, where one winding is closer to the substrate, result in less improvement in M ensured by the high-ρ substrate, while larger windings induce stronger eddy currents beneath. As observed, the interleaved transformer exhibits a coupling coefficient k approximately twice that of the concentric design, underscoring the critical role of geometry in magnetic coupling efficiency.

At the second level of analysis, transformer performance is examined with respect to resistive losses (including conductor resistance, dielectric absorption, etc.) that degrade power gain. These are brought together in the resistive mutual coupling factor (K_{re}), which quantifies energy dissipation resulting from interactions between the primary and secondary windings (reduction of power transfer) and their environment (heat dissipation), which become significant with frequency. In other words, K_{re} refers to unwanted resistive paths between the primary and secondary windings of a transformer, typically through the substrate. These paths dissipate energy as heat, reduce efficiency, and degrade overall performance. Fig. 5a shows the measured and simulated K_{re} for the interleaved transformer on Std-Si and HR-Si + TR substrates, while Fig. 5b gives the corresponding results for the concentric transformer. At low frequencies, K_{re} approaches zero for both topologies, as coupling between the inductors is predominantly inductive and essentially lossless. It is worth noting that the interleaved transformer exhibits higher K_{re} at elevated frequencies due to skin and proximity effects, which alter current distribution and concentrate it on the conductor surface, raising resistive losses mainly in the adjacent traces. At higher frequencies, K_{re} assumes finite, non-zero values, which are significantly reduced for both topologies when using high-resistivity substrates. Indeed, low-resistivity substrates exacerbate eddy currents that oppose the transformer's magnetic field, dissipating energy as heat, and simultaneously act as low-resistance paths between windings, creating parasitic resistive connections that increase crosstalk and losses. Therefore, evaluating the reduction of substrate losses via K_{re} is essential for understanding its impact on the maximum available gain in both transformer topologies.

The G_{max} ($\leq$1 for passive components) represents the optimal power coupling capability of the transformer under ideal impedance-matching conditions to eliminate reflections, accounting for the transformer's intrinsic losses and parasitic elements. Fig. 6 presents the measured and simulated G_{max} versus frequency for the interleaved and concentric transformers on Std-Si and HR-Si + TR substrates. The results demonstrate that improving the Q-factors of the primary and secondary windings, while reducing resistive mutual coupling, directly leads to higher gain. A substantial improvement in G_{max} is observed for the interleaved transformer, which rises from 0.33 (@1.42 GHz) to 0.63 (@2.2 GHz), an improvement of over 90 %. The concentric transformer exhibits an even larger enhancement, increasing from 0.06 (@1.48 GHz) to 0.22 (@2.15 GHz), corresponding to a 267 % relative increase. This upward shift of the G_{max} peak results from the HR-Si + TR substrate suppressing parasitic surface conduction and increasing effective substrate impedance, which reduces resistive losses and lowers parasitic capacitance. These changes raise the resonant frequency and winding Q-factors, causing the maximum available gain to occur at a higher frequency.

On the other hand, the operating bandwidth, defined as the frequency range below the self-resonant frequency (SRF, f_{res}) where the device operates efficiently, also improves markedly. For the interleaved transformer, f_{res} increases modestly from 3.66 GHz to 3.8 GHz (a 3.8 % improvement), whereas for the concentric transformer, it rises from 3.12 GHz to 4.1 GHz (a 31 % improvement). These results confirm that transformer topology strongly governs the performance gains enabled by the HR-Si + TR substrate. In the interleaved case, where primary and secondary traces are adjacent and tightly packed, magnetic coupling is relatively strong; thus, while the efficiency nearly doubles (from 0.33 to 0.63), the improvement is moderated by persistent resistive mutual coupling. In contrast, the concentric transformer, with its radially separated windings and inherently weaker coupling, benefits more from the HR-Si + TR substrate by suppressing leakage paths and raising substrate impedance. Its efficiency improves by more than threefold from 0.06 to 0.22. This pronounced gain in the concentric design is attributed to the larger winding separation (75 μm), which lowers parasitic and resistive coupling between windings and allows the benefits of the quasi-lossless HR-Si + TR substrate.

The studied key figures of merit for both transformers are summarized in Tables 2 and 3. Overall, the reduction of substrate losses clearly enhances high-frequency performance, increasing the bandwidth and energy efficiency of on-chip transformers. These results demonstrate that HR-Si + TR substrates effectively broaden the operational range of integrated transformers, making them highly suitable for RF and microwave applications.

6. Substrate impact on transformers' characteristics

Similar to HR-Si + TR substrates, several studies have shown that alternative substrates, such as glass, porous silicon, quartz, and polyimide, can substantially enhance transformer performance compared to Std-Si. Table 1 summarizes key results from previous works, enabling a direct and relevant comparison with our findings. For instance, patterned ground shields (PGS) implemented beneath transformers can achieve a higher G_{max} (~0.75) compared to an unpatterned design, although this improvement becomes more pronounced at higher frequencies [16]. At low frequencies, ohmic losses associated with the ground pattern can slightly degrade the Q-factors of the coil-based transformer. On glass substrates, for example, an integrated interwinding transformer exhibited a 25 % increase in resonant frequency compared to Std-Si, rising from 64 MHz to 80 MHz [18], and nearly doubled the Q-factor of the individual coil (where L_1 and L_2 are the same) from 0.35 to 0.61. Porous silicon has also been reported to provide significant improvements over Std-Si for an interleaved transformer where G_{max} improved from 0.53 to 0.77 (~40 % increase), the f_{res}

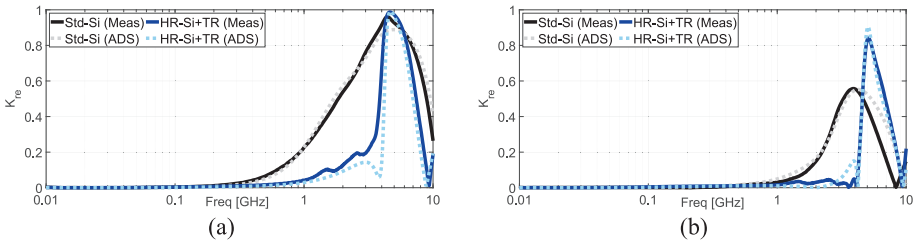

Fig. 5. Measured and simulated mutual resistive coupling K_{re} on Std-Si and HR-Si + TR substrates for (a) the interleaved transformer and (b) the concentric transformer.

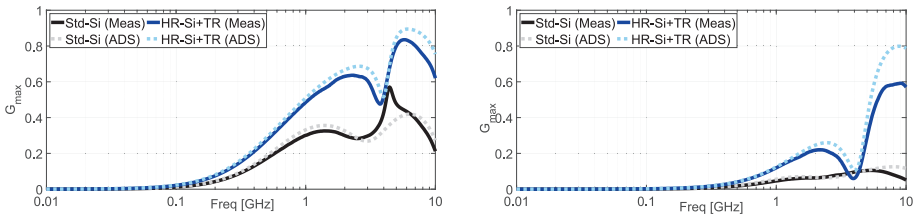

Fig. 6. Measured and simulated maximum available gain on Std-Si and HR-Si + TR substrates for (a) the interleaved transformer and (b) the concentric transformer.

increased from 4.4 GHz to 11.3 GHz (~157 % improvement), and the single-coil (where L_1 and L_2 are the same) *Q*-factor tripled, from 3.1 to 9.3 [20]. While porous silicon offers substantial performance gains, its fabrication is time-consuming and costly, limiting large-scale production. Likewise, replacing Std-Si with quartz beneath an interleaved transformer increased coil *Q*-factors from 3 to 8 (~2.6 times) above 3 GHz, while G_{max} improved from 0.4 to 0.6 after substrate etching [16].

In our work, the HR-Si + TR substrate achieves comparable or superior benefits, particularly in terms of resonant frequency and power gain efficiency. To the best of our knowledge, its use for integrated transformers has not yet been reported, and the primary aim of this work is precisely to fill that gap. The key advantage lies in the TR layer, which suppresses parasitic surface conduction (PSC) at the Si–SiO_2 interface. In standard HR-Si, fixed oxide charges can induce an inversion or accumulation layer that forms a conductive sheet, supporting leakage currents and aggravating eddy-current losses. By contrast, the TR layer introduces a high density of recombination centers that capture free carriers and pin the Fermi level, effectively eliminating this parasitic conduction path and restoring the effective substrate resistivity to values close to near-intrinsic values. This mechanism directly reduces substrate losses and boosts the effective winding quality factor. Our measurements confirm *Q*-factor improvements of ~ 2.7 times for the interleaved transformer and ~ 2.8 times for the concentric design. Since G_{max} depends strongly on both *Q*-factor and resistive mutual coupling, suppressing PSC also leads to substantial gains in power-transfer efficiency: G_{max} nearly doubled for the interleaved transformer and more than tripled for the concentric structure. The reported performance improvements are based on quantitative measurements (de-embedded S-parameters and derived metrics) and are corroborated by full-wave EM simulations, highlighting the critical role of the TR layer in enabling high-performance RF transformer integration.

Unlike glass or porous silicon, the HR-Si + TR is already employed in commercial SOI CMOS technologies (e.g., RF switches [36]), ensuring full CMOS compatibility and manufacturing scalability. This makes it particularly well-suited for high-performance RF transformer integration in applications such as digital isolators for power transfer and energy-harvesting circuits [37,38].

7. Conclusion

This work investigated the influence of high-resistivity silicon substrates with an undoped trap-rich layer (HR-Si + TR) on the performance of two on-chip planar transformer topologies: interleaved and concentric. Both structures were fabricated and characterized on standard silicon and HR-Si + TR substrates, with results validated through electromagnetic simulations. Key metrics, including self-inductance, individual winding quality factor, reactive and resistive coupling factors, mutual inductance, resonant frequency, and maximum power-transfer efficiency, were extracted to quantify the impact of substrate losses. The data demonstrated that substrate losses predominantly degrade the maximum available gain and increase resistive coupling at gigahertz frequencies, while mutual inductance and reactive coupling remain largely geometry-driven. Using HR-Si + TR improved the winding *Q*-factor by 2.5 times for the interleaved and 2.1 times for the concentric design, with self-resonant frequency increases of 3.8 % (3.66 to 3.80 GHz) and 31 % (3.12 to 4.10 GHz), respectively. Correspondingly, peak power-transfer efficiency nearly doubled for the interleaved design (0.33 at 1.42 GHz to 0.63 at 2.2 GHz) and more than tripled for the concentric topology (0.06 at 1.48 GHz to 0.22 at 2.15 GHz). The more pronounced gains in the concentric topology are attributed to its wider winding separation, which amplifies the benefits of reduced eddy-current and leakage-path losses. Importantly, HR-Si + TR is fully CMOS-compatible and introduces no significant fabrication overhead, making it a practical solution for high-performance on-chip transformers. These findings highlight its potential to enhance transformer efficiency and bandwidth in RF and microwave applications, including impedance-matching networks, isolation circuits, and power-transfer systems.

CRediT authorship contribution statement

Najeh Zeidi: Writing – original draft, Validation, Methodology, Investigation, Formal analysis, Data curation. **Farès Tounsi:** Writing – original draft, Visualization, Methodology. **Jean-Pierre Raskin:** Writing – review & editing. **Denis Flandre:** Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

The authors gratefully acknowledge the support of the “ISOP4HV” project, granted by the Walloon Region, Belgium, under the Win^{2}Wal program, which enabled the financing of microfabrication and characterization of the presented devices.

Data availability

Data will be made available on request.

References

[1] Ningning W, O’Donnell T, Roy S, Kulkarni S, Mccloskey P, O’Mathuna C. Thin film microtransformer integrated on silicon for signal isolation. IEEE Trans Magn 2007; 43:2719–21.
[2] K. Maniar, S. Mappus, T. Merkin, A. Triano and L. Trowbridge, “Addressing High-Voltage Design Challenges With Reliable and Affordable Isolation Technologies,” *Texas Instruments note,* 2022.
[3] Sun H, Liu Z, Zhao J, Wang L, Zhu J. The enhancement of Q-factor of planar spiral inductor with low-temperature annealing. IEEE Trans Electron Devices 2008;55: 931–6.
[4] Nishad PK, Ghosh D. Planar circular spiral inductors with improved Q and self-resonance frequency using compensatory capacitance technique. IEEE Trans Compon Packag Manuf Technol 2023;13:865–72.
[5] Tounsi F, Said MH, Hauwaert M, Kaziz S, Francis LA, Raskin J-P, et al. Variation range of different inductor topologies with shields for RF and inductive sensing applications. Sensors 2022;22:3514.
[6] Choi Y-S, Yoon J-B. Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for RF ICs. IEEE Electron Device Lett 2004;25:76–9.

[7] N. Zeidi, M. Rack, N. André, J.-P. Raskin, F. Tounsi and D. Flandre, "Effect of Silicon Substrate Resistivity on Large-Area High Voltage Spiral Inductor Performance," *IEEE Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP)*, Valetta, Malta, 2023.

[8] Benaissa K, Yang J-Y, Crenshaw D, Williams B, Sridhar S. RF CMOS on high-resistivity substrates for system-on-chip applications. IEEE Trans Electron Dev 2003;50:567–76.

[9] Raskin J-P, Viviani A, Flandre D, Colinge J-P. Substrate crosstalk reduction using SOI technology. IEEE Trans Electron Dev 1997;44:2252–61.

[10] Huang Y, Liu F, Cristoloveanu S, Ma S, Nabet M. C-V characterization of the trap-rich layer in a novel Double-BOX structure. Solid-State Electronics 2024;218:108951.

[11] Lederer D, Raskin J-P. Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers. Solid State Electron 2003;47:1927–36.

[12] Lederer D, Raskin J-P. Effective resistivity of fully-processed SOI substrates. Solid State Electron 2005;49:491–6.

[13] Liu S, Zhu L, Allibert F, Radu I, Zhu X, Lu Y. Physical models of planar spiral inductor integrated on the high-resistivity and trap-rich silicon-on-insulator substrates. IEEE Trans Electron Devices 2017;64:2775–81.

[14] Nyssens L, Rack M, Schwan C, Zhao Z, Lehmann S, Hermann T, et al. Impact of substrate resistivity on spiral inductors at mm-wave frequencies. Solid State Electron 2022;194:108377.

[15] H. Jiang, Z. Li and N. Tien, "Reducing silicon-substrate parasitics of on-chip transformers," *15th IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.02CH37266)*, Nevada, USA, 2002.

[16] Ng KT, Rejaei B, Burghartz J. Substrate effects in monolithic RF transformers on silicon. IEEE Trans Microw Theory Tech 2002;50:377–83.

[17] Feng Z, Lueck MR, Temple DS, Steer MB. High-performance solenoidal RF transformers on high-resistivity silicon substrates for 3D integrated circuits. IEEE Trans Microw Theory Tech 2012;60:2066–72.

[18] Yunas J, Hamzah AA, Majlis BY. Surface micromachined on-chip transformer fabricated on glass substrate. Microsyst Technol 2009;15:547–52.

[19] Chen C-H, Huang C-H, Horng T-S, Wu T-S, Chiu S-M, Hung C-P, et al. Very compact transformer-coupled balun-integrated bandpass filter using integrated passive device technology on glass substrate. California, USA: IEEE MTT-S International Microwave Symposium; 2010.

[20] Chong K, Xie Y-H. High-performance on-chip transformers. IEEE Electron Device Lett 2005;26:557–9.

[21] Gu L, Li X. High-performance CMOS-compatible solenoidal transformers with a concave-suspended configuration. IEEE Trans Microw Theory Tech 2007;55:1237–45.

[22] R. Ribas, J. Lescot, J. Leclercq, J. Karam and F. Ndagijimana, "Monolithic micromachined planar spiral transformer," *GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 20th Annual. Technical Digest 1998 (Cat. No.98CH36260)*, Georgia, USA, 1998.

[23] Haiwang L, Kaibo L, Kaiyun Z, Yuqian M, Wenbing W, Tiantong X. Ultra-high-isolation mutual-embedded transformer in organic substrate for digital isolator. IEEE Electron Device Lett 2024;45:665–8.

[24] Rack M, Allibert F, Raskin J-P. Modeling of semiconductor substrates for RF applications: Part I—Static and dynamic physics of carriers and traps. IEEE Trans Electron Dev 2021;68:4598–605.

[25] Rack M, Allibert F, Raskin J-P. Modeling of semiconductor substrates for RF applications: Part II—Parameter impact on harmonic distortion. IEEE Trans Electron Dev 2021;68:4606–13.

[26] Shim Y, Raskin J-P, Neve CR, Rais-Zadeh M. RF MEMS passives on high-resistivity silicon substrates. IEEE Microwave Wirel Compon Lett 2013;23:632–4.

[27] Nabet M, Rack M, Yan Y, Nguyen B-Y, Raskin J-P. Double buried oxide trap-rich substrates for high frequency applications. IEEE Electron Device Lett 2023;44:570–3.

[28] Tounsi F, Flandre D, Rufer L, Francis LA. Performances evaluation of on-chip large-size-tapped transformer for MEMS applications. IEEE Trans Instrum Meas 2020;69:7051–60.

[29] Cendoya I, de No J, Sedano B, Garcia-Alonso A, Valderas D, Gutierrez I. A new methodology for the on-wafer characterization of RF integrated transformers. IEEE Trans Microw Theory Tech 2007;55:1046–53.

[30] Abdelhadi N, Ridha BM, Rabia M, Abdelkader B, Tekkouk AB, Zineb B. Integrated interleaved transformer in an isolated full-bridge buck converter. J Circ Syst Comput 2023;33:2450168.

[31] Derkaoui M, Yamina B, Azzedine H. Modeling and simulation of an integrated octagonal planar transformer for RF systems. Discover Appl Sci 2020;2:1–14.

[32] Volksen W, Miller RD, Dubois G. Low dielectric constant materials. Am Chem Soc 2010;110:56–110.

[33] S. Chouaibi, M. H. Said, D. Nasr, M. B. Ayed, D. Flandre and F. Tounsi, "Mutual Inductance Evaluation Between Two Parallel Conductors on a PCB," *30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Istanbul, Turkey, 2023. https://doi.org/10.1109/ICECS58634.2023.10382803.

[34] K. Subramaniam, A. V. Kordesch and M. Esa, "Nine-Element Lumped Metal-Insulator-Metal (MIM) Capacitor Model for RF Applications," 31st *IEEE/CPMT International Electronics Manufacturing Technology Symposium*, Petaling Jaya, Malaysia, 2006.

[35] El Kaamouchi M, Delatte P, Moussa MS, Raskin J-P, Vanhoenacker-Janvier D. Temperature behavior of spiral inductors on high resistivity substrate in SOI CMOS technology. Solid State Electron 2008;52:1915–23.

[36] Esfeh BK, Rack M, Makovejev S, Allibert F, Raskin J-P. A SPDT RF switch small-and large-signal characteristics on TR-HR SOI substrates. IEEE J Electron Devices Soc 2018;6:543–50.

[37] G. Gonçalves, M. A. Martins and J. R. Fernandes, "Energy harvesting circuit using integrated transformer," IEEE International Symposium of Circuits and Systems (ISCAS), Brazil, 2011.

[38] Gonçalves H, Martins M, Fernandes J. Fully integrated energy harvesting circuit with −25-dBm sensitivity using transformer matching. IEEE Trans Circuits Syst Express Briefs 2015;62(5):446–50.