Towards Suspended Geometric Diodes for TeraHertz Rectenna Solar Cells Using Wafer-Scale CVD Graphene on Cu Thin Films

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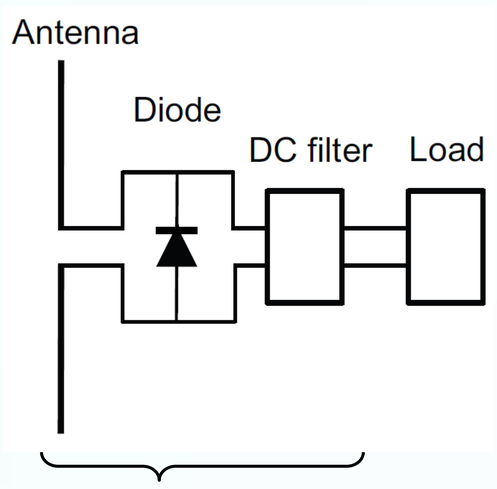
> Abstract <

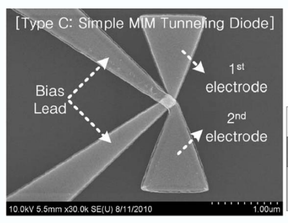
Micron-size antennas coupled to high-frequency diodes convert the AC electric field harvested from ambient radiation to useable DC power. Currently, investigated rectifying antennas (rectennas) based on metal/insulator/metal (MIM) diodes present frequency limitations due to their intrinsic RC response time and have poor impedance matching to the antenna [1]. MIM diodes use the tunneling effect through their thin insulator to create the non-linear behavior resulting in rectification [2]. Geometric diodes however use the ballistic transport of charge carriers in planar structures smaller or comparable to the mean free path to obtain the asymmetric behavior. Graphene structures exhibit a carrier mean free path exceeding 300 nm at room temperature [3] and have an extremely low capacitance due to their planar configuration. This makes them suitable to reach a 30 THz target frequency. Networks of rectennas could be used in solar cells for thermophotovoltaic energy harvesting. We present our progress on device characterization on SiO_2 and large-scale fabrication of suspended CVD graphene devices on Cu thin films.

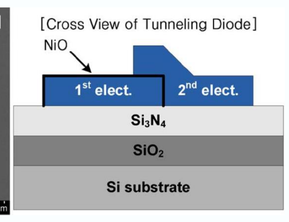
> Context

To replace metal/insulator/metal diodes by graphene geometric diodes for solar energy harvesting applications

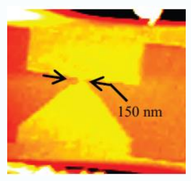


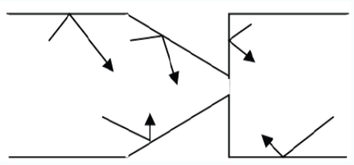
Rectenna powering a load [1]





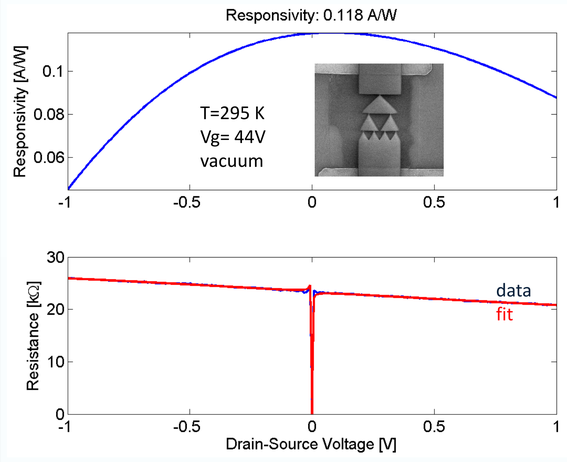
MIM tunneling diode [2]

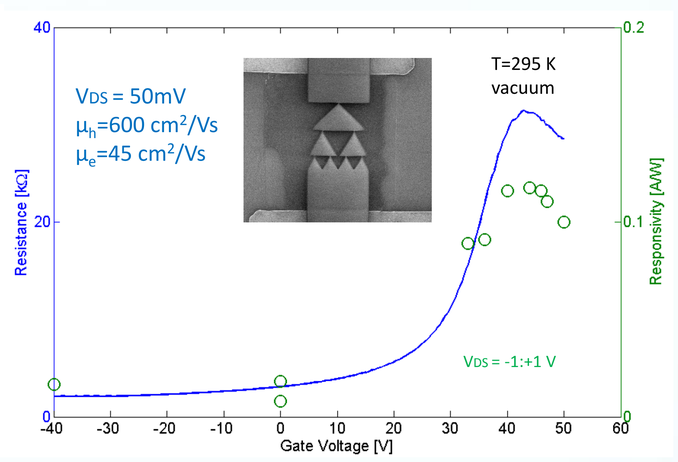




Geometric diode [1]

> Results with transferred devices





- Responsivity is computed from DC measurements as: $\Re = \frac{1}{2} \cdot \frac{I''(V_{ds})}{I'(V_{ds})}\Big|_{V_{ds}=0}$
- Measured values are close to results in [1] for flakes.

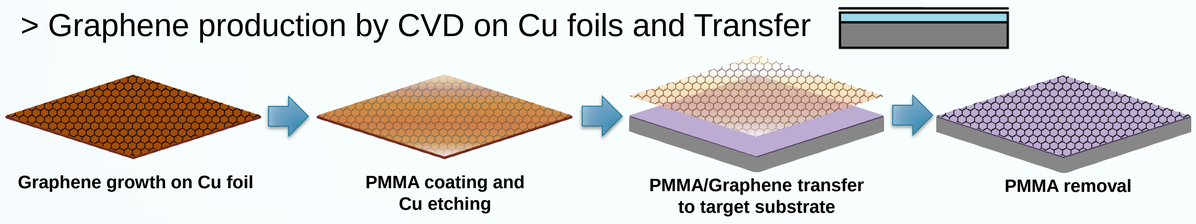
> Transferred Graphene on SiO_2 Fabrication

>> Optical lithography

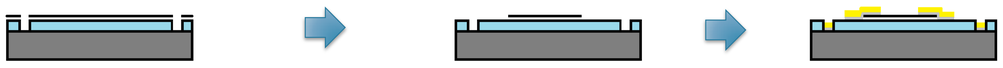
Applying the CMOS platform tools to CVD graphene

> Grow 90 nm thermal oxide on 3” Si wafer

> Graphene production by CVD on Cu foils and Transfer



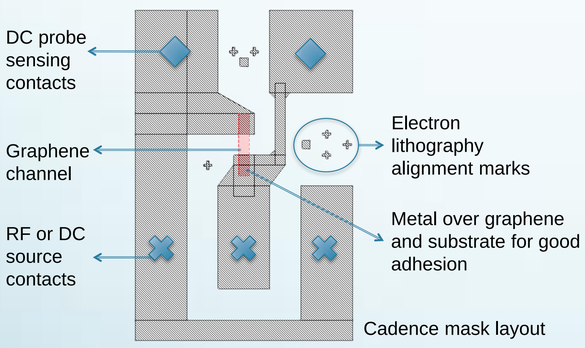
Spin-coat with low density PMMA and etch the Cu in $FeCl_3$, then transfer to SiO_2 layer. Dissolve PMMA again to relax constraints, cure and then remove.

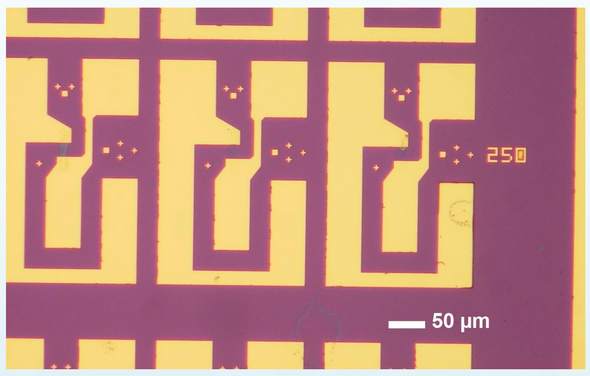


Etch alignment marks in SiO_2 for optical lithography

Create graphene channel by O_2 plasma etch

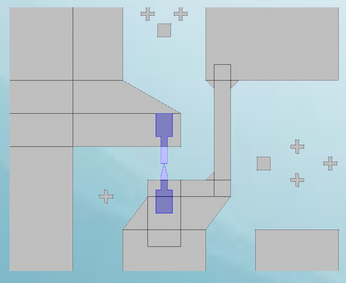
Metal deposition and Liftoff



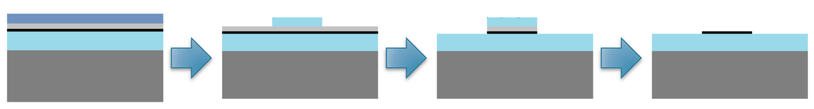


>> Electron beam lithography

Define the pattern of the geometric diode



E-beam cadence mask layout



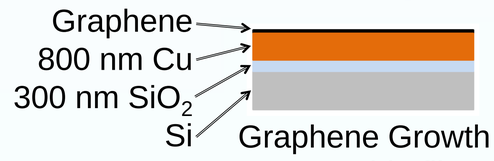
40 nm HSQ
180 nm PMMA
Graphene
SiO_2/Si

Expose HSQ to leave SiO_2 and develop

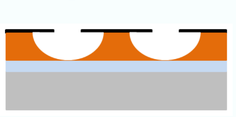
O_2 plasma etch

Acetone removal

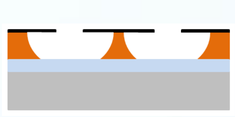
> Transferless Suspended Graphene on Cu Thin Film



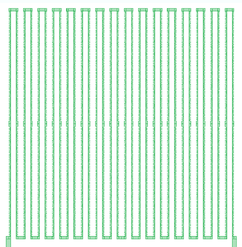
Graphene Growth on Cu thin film



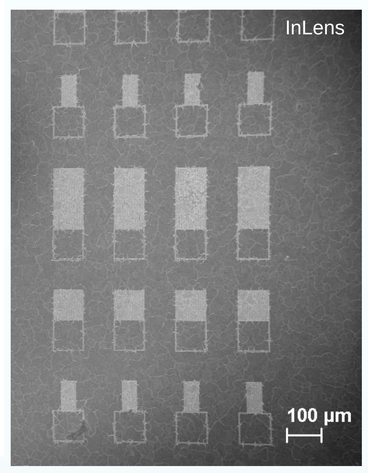
Single lithography step, O_2 plasma, Cu etch & CPD

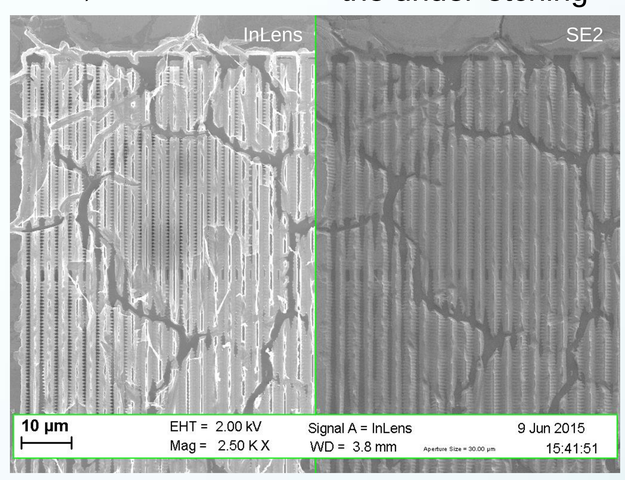


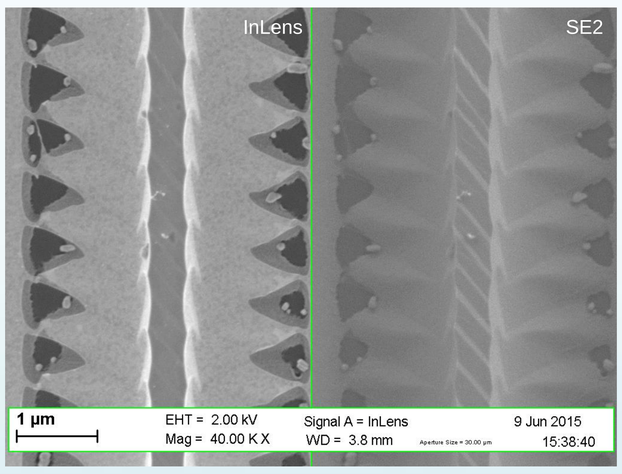
Timing controls the under-etching

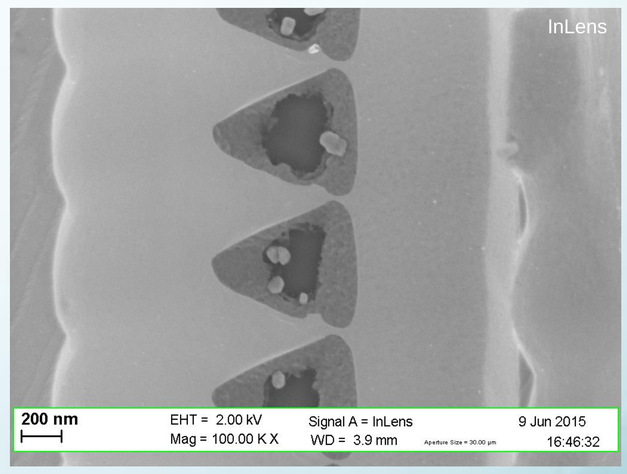


Inter-Digitated Electrodes used as antennas (Layout)









> Perspectives

>> Device modeling

Transport properties could be simulated by Drude or tight-binding models
Harmonic balance could be used to assess the high frequency behavior

>> Couple the diodes to THz antennas and illuminate

> DC measurements under illumination with a 10 μm wavelength CO_2 laser can be performed in collaboration with the VUB in Brussels

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> References

[1] Z. Zhu et al., IEEE 37th Photovoltaic Specialists Conference, pp. 002120–002122, 2011.
[2] K. Choi et al., *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3519–3528, 2011.
[3] G. Moddel et al., Solid State Communications, vol. 152, no. 19, pp. 1842 – 1845, 2012.