Low-Power, High-Sensitivity Temperature Sensor Based on Ultrathin SOI Lateral p-i-n Gated Diode

Guoli Li, Nicolas André, *Member, IEEE*, Qi Chen, Huiru Wang, Laurent A. Francis, *Member, IEEE*, Yun Zeng, Lei Liao, *Member, IEEE*, and Denis Flandre, *Senior Member, IEEE*

***Abstract*— In this work, we present a silicon-based p-i-n thermal diode, with post-CMOS MEMS processing (deep reactive ion etching and Al deposition) and annealing (at 250 °C). The MEMS processing degraded device stability as well as thermal sensing linearity and sensitivity, while the local annealing recovered the device performance (forward and reverse characteristics) by reducing the trap density and improving the carrier lifetime. After annealing, the on-membrane diode can achieve stabilized thermal linearity with a high sensitivity of ∼2.25 mV/°C at 0.02–0.03 μA low constant current, in the temperature range from room temperature to 200 °C, under a back-gate bias of 90 V to achieve a fully-depleted condition in the intrinsic (I) region and decrease the trap-assisted recombination at the front surface which dominates and degrades the device forward output current. To be compatible with commercial 1.0-μm SOI CMOS technology, a front gate with a 25-nm-thick oxide dielectric is proposed and simulated in Atlas/SILVACO to optimize the device performance and achieve the same thermal characteristics under a front-gate bias of 1.0 V, showing its potential in low-power consumption electronics. The temperature sensor investigated in this work shows its industrial capability in gas sensing and integrated circuit applications.**

Manuscript received May 1, 2019; revised June 28, 2019 and July 16, 2019; accepted July 18, 2019. This work was supported in part by the Technology Program (Major Project) of Changsha under Grant kq1804001), in part by the National Nature Science Foundation of China under Grant 61811540408, and in part by the Micro+ Project co-funded by the European Regional Development Fund (ERDF) and Wallonia, Belgium. The review of this paper was arranged by Editor D. J. Young. *(Corresponding author: Guoli Li.)*

G. Li and D. Flandre are with the Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education, School of Physics and Electronics, Hunan University, Changsha 410082, China, also with the Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China, and also with the Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain, 1348 Ottignies-Louvain-la-Neuve, Belgium (e-mail: liguoli_lily@hnu.edu.cn).

N. André and L. A. Francis are with the Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain, 1348 Ottignies-Louvain-la-Neuve, Belgium.

Q. Chen, H. Wang, Y. Zeng, and L. Liao are with the Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education, School of Physics and Electronics, Hunan University, Changsha 410082, China.

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Digital Object Identifier 10.1109/TED.2019.2930244

***Index Terms*— Linearity, low power, p-i-n diode, sensitivity, SOI, thermal sensing (temperature sensor).**

I. Introduction

In RECENT years, with ongoing advancements in microfabrication technology, requirements for a smaller size, lower power consumption, wider temperature ranges, and on-chip sensor-electronics co-integration have challenged the conventional temperature detection techniques. To fulfill these stringent requirements, temperature sensors based on varied materials and technologies are proposed [1]–[3]. A GaN-on-SiC based heterojunction diode was designed and fabricated to measure the temperature from 300 to 650 K with a maximum sensitivity of −2.19 mV/° [i.e., degree is used here for Kelvin (K) or degree Celsius (°C) indifferently] at a forward current (I_F) of 10 μA with a device diameter of 400 μm [1]. An advanced 4H-SiC p-i-n diode in [4] and [5] can offer a sensitivity up to −4.5 mV/° and a nearly ideal linearity (>99.93%) from room-temperature (RT) up to 460 °C with applied current densities up to 0.1 mA/cm^2 and a forward voltage of 2.16 V at RT. In [6], a SiC Schottky barrier diode has been integrated with a MOS capacitor for gas (i.e., hydrogen) detection; it operates in the temperature range from RT to 200 °C with a sensitivity of −1.52, resp. −2.13 mV/° at an I_F of 1.0 mA, resp. 1.0 μA.

However, CMOS-based Si temperature sensors have become increasingly vital because of the rapid steady growth of low-cost integrated circuit (IC) applications and the necessity for effective thermal management in systems-on-chip [7]. The maximum operating temperature for bulk silicon CMOS is generally limited to 150 °C, while SOI technology increases this limit to more than 200 °C–250 °C [7], [8]. Being used as the most accurate CMOS temperature sensor in a wide variety of applications, e.g., humidity, pressure, flow, stress, and gas concentration [7], the Si-based p-n junction shows potential advantages over other types of devices [bipolar junction transistor (BJT), MOSFET] for thermal sensing, including its on-chip integration feasibility with electronic circuits, low manufacturing cost, high sensitivity, absolute temperature measurement (as well as the low-temperature) capability, and long-term stability [9], [10]. For example, in [11] and [12], the Si-based lateral diode works from 300 to 550 K with

thermal sensitivities of −2.1 and −1.6 mV/° at forward biasing currents of 0.005 and 0.1 μA, respectively, higher than the −1.29 and −1.23 mV/° obtained in the MOS transistor.

Extensive work on Si-based thermodiodes has been carried out in Cambridge University, within an SOI CMOS-compatible microhotplate platform [2], [7], [13]–[15]. The SOI p-i-n diode can operate in an extremely wide temperature range of 80–1050 K at a driving current of 100 μA with a sensitivity of −1.13 mV/° and high linearity. However, when the diode is used as a temperature sensor, it is best to operate it at relatively low forward currents/low power to avoid self-heating, the influence of the series resistances, and to increase the sensitivity to values closer to −2.2 mV/° [14]. On the other hand, the accuracy and linearity of the p-i-n thermodiode can be enhanced by eliminating the p-well doping of the (I) region in [13] and [15]. Moreover, along with the SOI p-i-n thermodiode for thermal sensing (with the transient thermal response time below 10 ms), the microhotplate has been widely used in multi-sensing applications [16]–[18], e.g., high sensitive NO_2 gas sensing [19], a diode-based CMOS MEMS thermal flow sensor [20], an alcohol sensor [21], and a MEMS chip for fluidic applications [22].

In this research, we report the optimization of such a thin SOI-based p-i-n diode for thermal sensing at a lower current level, with high sensitivity and stable characteristics. The same p-i-n diode with a 10-μm-long intrinsic region (I) was used previously for optical sensing and achieved multiple wavelength detection in the visible wavelength range while operating in the reverse condition [23]. This paper studies, in depth, the diode thermal sensing capability when operating in the forward condition. Section II describes the post-CMOS MEMS processing [i.e., deep reactive ion etching (DRIE) and aluminum e-gun deposition], to form the membrane structure and the back-gate electrode. Section III discusses the impact of the MEMS process on the diode forward characteristics and thermal sensing performance. After low-temperature annealing (at 250 °C, using the heating element embedded in the same membranes [7]) and under back-gate biasing (of 90 V to achieve full depletion), the on-membrane diode can achieve high stabilized thermal sensing linearity and sensitivity in the temperature range from RT to 200 °C. This features high capability in IC applications (150 °C–200 °C [7]) and gas sensing (CO at 100 °C, H_2 at 200 °C, NH_3 at 150 °C–200 °C, and H_2O at 240 °C [24]–[26]). Finally, numerical simulation in Atlas/SILVACO has been performed for device behavior interpretation and optimization. Using a front gate with 25-nm-thick oxide, available in the SOI CMOS technology, the gate operating voltage can be reduced to a low voltage of 1.0 V, for compatibility with low-power electronics applications [27].

II. Device Description and Processing

The device samples used in this work were manufactured using commercial 1.0-μm SOI CMOS technology that enables the monolithic integration of p-i-n diodes, MOS transistors, a microhotplate, and control circuits, rated for long-term operation at high temperatures. Consequently, MOS transistors and p-i-n diodes with a polysilicon gate can be embedded both on the silicon substrate and in a membrane created by backside micromachining, as depicted in Fig. 1, where the 1-μm-thick buried oxide (BOX) acts as an effective etch-stop layer during DRIE of the Si substrate to ensure membrane high uniformity and device reproducibility [23]. The SOI microhotplate in Fig. 1 was originally designed as a multi-sensing system (e.g., light, flow, and humidity [18], [20], [22]) for harsh-environment industrial applications, with a microheater for local heating. The microheater and the diode anode and cathode terminals are here built from aluminum (Al) metallization, because of its low cost and industrial technology availability. A higher-cost tungsten option is also available for higher temperature applications. The device multilayer stack comprises Si_3N_4 (560-nm thick, as a passivation layer), SiO_2 (2.5-μm thick, to form the stressless membrane where the photodiode is embedded), polysilicon (300-nm thick, for implantation protection), SiO_2 (25-nm thick, gate dielectric for the MOS transistor), Si (250-nm thick, active layer), and SiO_2 (1.0-μm thick, BOX), as depicted in the schematic cross section of the diodes in Fig. 1. The bottom orange layer in Fig. 1 represents an additional 1-μm-thick aluminum (Al) layer, which can be specifically deposited backside by e-gun evaporation. A back-gate voltage can then be applied to Al, to modify the depletion condition in the intrinsic (p-type lightlydoped) region, while the top polysilicon gate was left unconnected here. The experimental results reported in the next section are fully representative of the numerous on-substrate and on-membrane diodes we measured in this work and in previous ones [32], after different process steps.

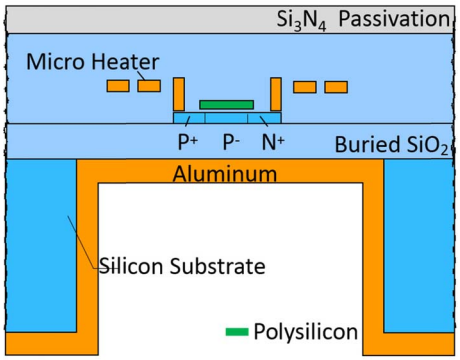

Fig. 1. Cross section view of the SOI lateral p-i-n diode on membrane (M10), i.e., microhotplate platform: Si_3N_4 passivation (gray), SiO_2 dielectric (light blue), silicon (dark blue, 250-nm thick), polysilicon (green, 300-nm thick), aluminum contacts, microheater, and deposition layer (orange).

III. Experimental Proceeding and Application

In the Si-based thermodiode, the constant current mode is the most widely used sensing mode, with a wider temperature range and better linearity compared to the constant voltage mode [7]. When operated at a constant forward driving current (I_F), the diode can be used for temperature sensing measuring the strong and linear temperature dependence of the corresponding forward bias voltage drop (V_F).

A. Ideality Factor and Temperature Coefficient

The ideal current–voltage (I–V) characteristic of a p-n junction diode is often described by the Shockley equation [28]

$$I = I_S\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{1}$$

where the thermal voltage kT/q is 25.8 mV at RT of 27 °C and I_S is the specific current term related to the diffusion of carriers. I_S is dependent on the square of the intrinsic carrier density, n_i^2, as given in (4). Additionally, generation–recombination (G–R) processes in the depleted region need to be taken into account. Therefore, at a given forward bias V_F, the net forward current I_F can be approximated by the sum of diffusion and G–R currents, as described in (2). The major G–R process in the depletion region is the capture process, i.e., recombination [29]

$$I_F = I_S\left[\exp\left(\frac{qV_F}{kT}\right)1\right] + I_{\mathrm{GR}}^0\left[\exp\left(\frac{qV_F}{2kT}\right)1\right] \tag{2}$$

$$I_F \propto \exp\left(\frac{qV_F}{\eta kT}\right)\left(\text{for } V_F \gg \frac{kT}{q}\right) \tag{3}$$

$$n_i^2 \propto T^3 e^{\frac{-E_g}{kT}}. \tag{4}$$

The recombination current is the latter component in (2) in the forward biasing condition, proportional to n_i (described by $I_{\mathrm{GR}}^0 \propto n_i$). The experimental results can in general be represented by an empirical form in (3) for $V_F \gg kT/q$, where the ideality factor η depends on the diode technology and the device operation regime. A diode ideality factor η close to 1 indicates the dominance of the diffusion current, while ~2 indicates the dominance of the G–R mechanism, as expressed in (2).

The p-n diode can be best used for thermal sensing in forward conditions where the diffusion current is dominant. Under such a constant I_F current scheme, the diode forward voltageV_F decreases linearly with increasing temperature T, as given in (5) and derived from (3)

$$V_{F2} - V_{F1} = -d \cdot (T_2 - T_1) \tag{5}$$

where the slope d of one V–T curve is expected to remain constant and decrease with the increased bias current [30]. For the silicon-based diode, the thermal sensitivity $\Delta V_F/\Delta T$ varies from −1.2 to −2.3 mV/° depending on the forward driving current, as given by (1), technology, physical parameters of the junction, and geometry. As the G–R current is related to the volume of the depleted region [33], therefore a very low volume of the depletion region can lead to a very low value of the I_{GR}^0 saturation current, preserving the thermal linearity with temperature [13], [31].

B. Degradation Caused by DRIE

Typical I_F–V_F characteristics are presented in Fig. 2(a) for the standard on-substrate Si diodes (here noted S10 for intrinsic length $L_i = 10$ μm), with temperature variation from RT to 200 °C. The corresponding ideality factor η versus forward current at RT is depicted in Fig. 2(c), interpolated and then extracted on the basis of (3) at each bias point. At RT,

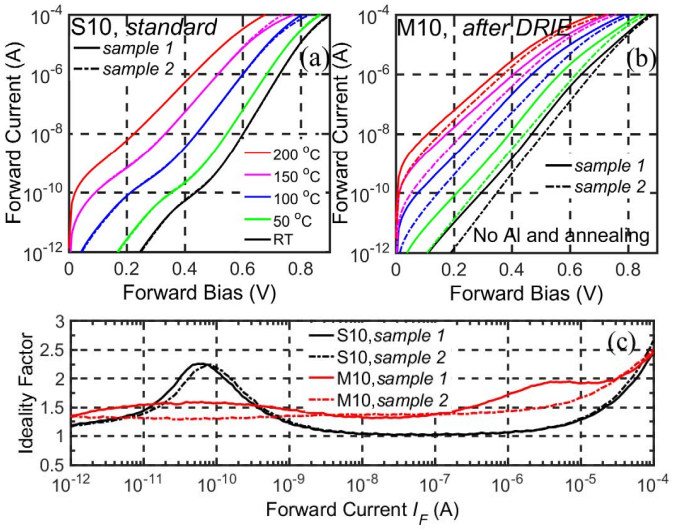

Fig. 2. Representative forward characteristics of (a) S10 on the standard silicon substrate and (b) M10 diodes within the on-membrane structure, with the ideality factor η extracted at RT as a function of (c) forward current for several devices.

the G–R current is dominant in the diodes S10 in the V_F range of 0.1–0.3 V, while diffusion becomes dominant with increased forward bias of ~0.5–0.7 V. Correspondingly, the ideality factor η varies from 2 to 1 with increasing forward current [Fig. 2(c)]. When T increases from RT to 150 °C, the diffusion saturation current I_S increases with n_i^2 and becomes larger than I_{GR}^0 within the 0.1–0.3 V range, thereby dominating in a wider range of V_F and I_F.

After the DRIE processing step to form the MEMS structure (Fig. 1), the I_F–V_F characteristics of two on-membrane diodes M10 are presented in Fig. 2(b). Obvious degradation in the device I_F–V_F curves and the η factor is observed [Fig. 2(b) and (c)]. The ideality factor η of M10 is higher than 1 over the full bias range [around 1.5 in Fig. 2(c)] indicating the predominance of the G–R current, as will be confirmed by simulations in Section IV. Furthermore, in the M10 diodes, the device stability is absent when considering several samples. In comparison, the I_F–V_F curves of S10 devices [Fig. 2(a)] appear very reproducible from one sample to another.

C. Annealing and Gate-Biasing Effect

A back-gate bias ranging from −60 to 90 V can be applied on the diodes M10 after e-gun deposition of an Al backside electrode onto the thick BOX (Fig. 1) to control the electrical depletion condition in the diode and, in turn, the I–V characteristics. Fig. 3 presents the representative forward I_F–V_F curves of the devices before and after annealing of different samples.

Before annealing, no stabilized forward characteristics can be observed in the M10 diodes [Fig. 3(a) and (c)], i.e., still dominated by the G–R mechanism. After local heating (at 250 °C, for 30 min) is carried out onto the diodes M10 by the on-membrane microheater, the recovery of forward I–V characteristics is observed, as depicted in Fig. 3(b) and (d). When the back-gate bias $V_G = 90$ V is applied to achieve the fully-depleted (FD) condition in the intrinsic region [32],

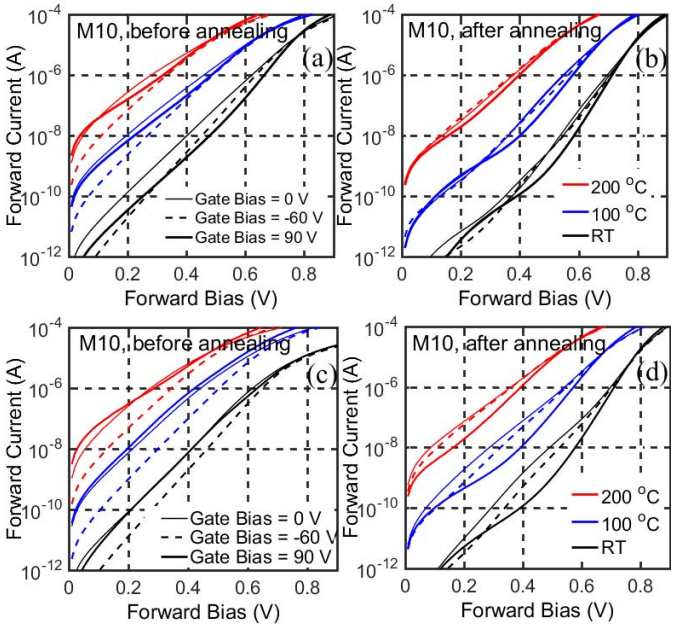

Fig. 3. Representative forward characteristics of the two representative M10 diodes with back-gate Al deposition, (a) and (c) before and (b) and (d) after annealing, under back-gate biases = −60, 0, and 90 V.

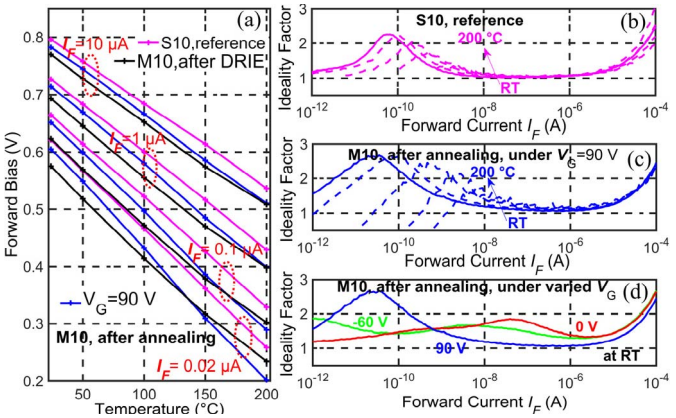

Fig. 4. (a) Thermal linearity and (b)–(d) η factor as a function of forward current, with temperature ranging from RT to 200 °C, in the (a) and (b) S10 diode (pink curves) and M10 diode (a) before (black lines) and (a), (c), and (d) after annealing under gate biasing [(a) and (c) 90 V and (d) −60, 0, and 90 V at RT].

the lateral p-i-n diodes exhibit typical, standard I–V characteristics in the forward condition, similar to those of the diodes S10, i.e., first dominated by the G–R current, then by the diffusion current with increasing forward bias. In this case, the forward I–V curves of different samples become more reproducible after annealing, under FD conditions, thereby achieving device reliability and stability in the bias range of interest. No further shift in the forward characteristics is observed while several cycles of annealing are carried out on the M10 diode.

D. Thermal Linearity and Sensitivity

A detailed analysis of thermal linearity, sensitivity, and ideality factor is presented in Fig. 4, for the standard diodes S10 and the M10 after different MEMS processing steps.

TABLE I
LINEARLY STABILIZED THERMAL SENSITIVITY IN THIS WORK

Sensitivity (mV/deg.)	0.02 μA	0.03 μA	0.1 μA	1.0 μA	10 μA
S10	−2.08	−2.02	−1.94	−1.74	−1.56
M10, V_G = 90 V	−2.26	−2.24	−2.07	−1.80	−1.57

In the diodes S10, the forward current is chosen in the range of 0.02–10 μA [Fig. 2(a)], where the diffusion current is dominant. The corresponding η of S10 as a function of forward current and temperature (RT to 200 °C) is presented in Fig. 4(b). The η at RT is close to 1 [33], leading to excellent linearity of V_F versus temperature relation for constant current. As a reference, the S10 diode with the standard SOI technology shows a good sensitivity of −2.08 to −1.56 mV/° at forward currents of 0.02–10 μA, from RT to 200 °C, as listed in Table I. Note that the sensitivity in S10 is close to −2 mV/° at 0.065 μA as in [7]. The lower absolute value of this coefficient (e.g., −1.56 mV/°C at I_F = 10 μA in diode S10) is generally expected when the forward current is higher, leading to higher forward voltage, as the junction exhibits parasitic series resistance [14].

In the diode M10, before annealing and without gate biasing, it is obvious to see that thermal sensing linearity is absent in the temperature range of RT to 200 °C, at any constant driving current, but especially at the lowest current (e.g., 0.02 μA), as shown by the black lines in Fig. 4(a), due to G–R current predominance.

After local annealing and with a back-gate bias V_G = 90 V to achieve the FD condition in the intrinsic region, the thermal sensing linearity in Fig. 4(a) is improved in the diode M10, with the sensitivity extracted in Table I. The best thermal linearity is obtained for M10 at V_G = 90 V as illustrated with the blue lines in Fig. 4(a), with a sensitivity of −2.26 to −1.57 mV/° at forward currents of 0.02–10 μA, in the temperature range of RT to 200 °C. The ideality factor versus forward driving current curves illustrate in Fig. 4(c) that M10 (at V_G = 90 V) is comparable to the reference S10 [Fig. 4(b)], indicating the device recovery in the μA range.

Fig. 4(d) indicates that the gate biases of −60 and 0 V cannot optimize the depletion condition in the intrinsic region and guarantee the dominance of the diffusion current (η close to 1 at RT) in the device forward driving current, due to the oxide charge and trap defects studied in the next section.

The high sensitivity (−2.26, resp. −2.07 mV/°) and linearity of the FD diode M10 at a low forward driving current (at 0.02 μA, resp. 0.1 μA) with forward voltage drop from 0.601 to 0.204 V, resp. 0.651–0.289 V, in the temperature range of RT to 200 °C, promotes its optimized and stabilized use in industrial applications discussed in the Introduction, but requires a high back-gate bias of 90 V due to the thick BOX.

IV. Device Simulation and Optimization

To fully understand and interpret the in-depth physics related to the forward characteristics in the diode M10 and be able to propose further optimizations, device numerical simulation is performed in Atlas/SILVACO [34].

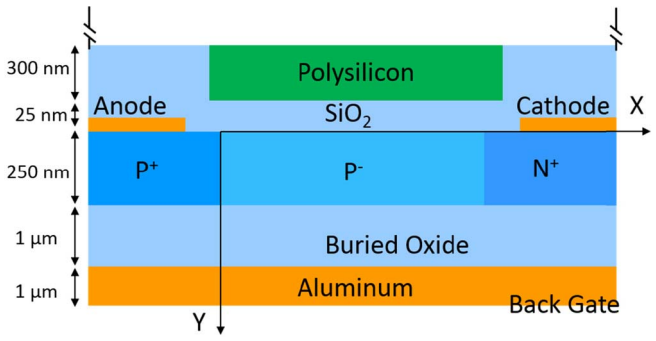

Fig. 5. Cross section of the 2-D SOI lateral p-i-n diode implemented in Atlas/SILVACO.

TABLE II
SIMULATION PARAMETERS

Condition	Carrier Lifetime (s)	D_{it} Distribution ($cm^{-2}\cdot eV^{-1}$)
Before Al	2×10^{-8}	$D_{itA(f)} = D_{itD(f)} = 1\times10^{12}$ (*front*) $D_{itA(b)} = 1\times10^{13}$; $D_{itD(b)} = 1\times10^{12}$ (*back*)
After annealing	1×10^{-6}	$D_{itA(f)} = D_{itD(f)} = 1\times10^{12}$ (*front*) $D_{itA(b)} = D_{itD(b)} = 1\times10^{12}$ (*back*)
After annealing (optimized case)	5×10^{-6}	$D_{itA(f)} = D_{itD(f)} = 1\times10^{11}$ (*front*) $D_{itA(b)} = D_{itD(b)} = 1\times10^{11}$ (*back*)

A. Simulation Setup

The 2-D device schematic view is depicted in Fig. 5, to investigate the annealing and back gate effects on the forward characteristics of the diode M10. The electrical parameters, listed in Table II, are set in the numerical model for the M10 before and after annealing, with a primary investigation in [32] by the low-frequency noise and reverse leakage characteristics. Similar to experimental devices, the width of the simulated diode is 60 μm, the length of the P^- region (i.e., intrinsic length L_i) is 10 μm, the length of the P^+ and N^+ regions is 2.5 μm, the active Si film thickness is 250 nm, and the BOX thickness is 1.0 μm. The multilayer stack and its corresponding material thicknesses are fixed according to Fig. 1 (Section II). The doping levels of the P^+, P^-, and N^+ regions are, respectively, 1×10^{20}, 5×10^{16}, and 1×10^{20} cm^{-3}. The backside 1.0-μm-thick Al layer is used as the back-gate electrode. Contacts of the anode and cathode electrodes are ohmic.

B. Forward Characteristics Interpretation

Fig. 6(a) presents the simulated forward characteristics of the diode M10 before annealing, where the interface donor (D) and acceptor (A) trap distributions (D_{it}) have respective peak densities of $\sim1\times10^{12}$ and 1×10^{13} $cm^{-2}\cdot eV^{-1}$ at the back interface (as DRIE was processed from the backside) and $\sim1\times10^{12}$ $cm^{-2}\cdot eV^{-1}$ at the front interface, while the volume carriers' lifetime τ is set to 0.02 μs, as obtained in [32]. The simulated forward I_F–V_F curves appear in fair agreement with the experimental observations of Fig. 3(a) and (c). The corresponding reverse leakage current for the diode M10 before annealing is depicted in the inset, as it was demonstrated and discussed in detail in [32]. In the reverse condition, the interface trap-assisted generation (TAG) process dominated the

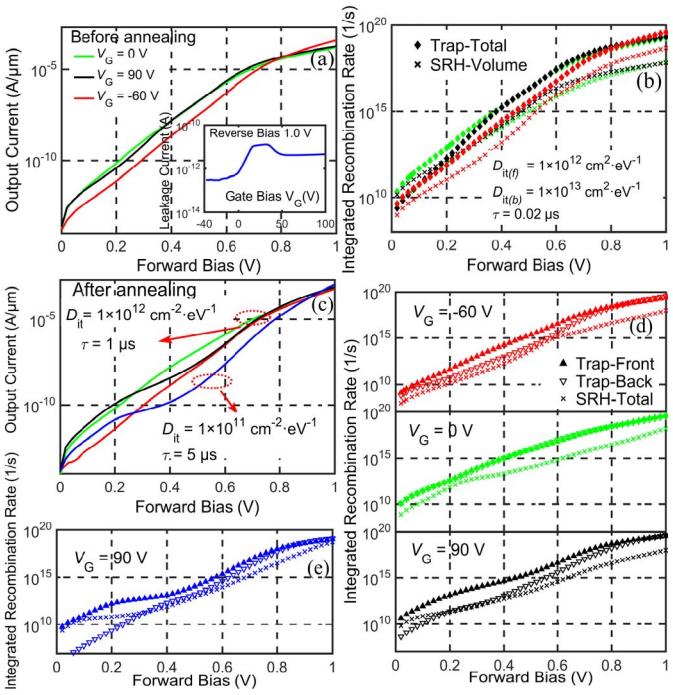

Fig. 6. (a) Simulated diode current at RT versus forward bias and (b) integrated TAR rate at the front and back surfaces and the SRH volume recombination rate in the M10 diode before annealing (with the parameters set as the "Before Al" condition in Table II), under gate biases of −60, 0, and 90 V. (c) Simulated diode output current and (d) and (e) corresponding recombination rates at RT of the M10 diode after annealing (with the parameters separately set as the "After Annealing" conditions in Table II) under gate biases of −60, 0, and 90 V.

diode reverse leakage behavior, especially the one contributed by the back interface, due to the higher density of $D_{itA(b)}$ and also a larger variation of the back surface potential (altered by the back-gate bias from −60 to 90 V). In the forward bias condition, the detailed G–R components are presented in Fig. 6(b), including the SRH volume and total trap-assisted recombination (TAR) rates. It is clearly seen that in the diode M10 before annealing, the front and back surface TAR processes dominate the device forward behaviors, degrading the diode thermal sensing capability.

After annealing [Fig. 6(c)–(e)], considering the decreased surface recombination velocity and improved carrier effective lifetime [23], the interface trap distribution is first implemented with a decreased peak density of $\sim1\times10^{12}$ $cm^{-2}\cdot eV^{-1}$ at the back and front interfaces, while the volume carriers' lifetime τ is set to 1.0 μs, and second to a peak density of $\sim1\times10^{11}$ $cm^{-2}\cdot eV^{-1}$ at both interfaces and volume carriers' lifetime τ to 5.0 μs as listed in Table II. When the back-gate bias $V_G = 90$ V (in black and blue curves) achieves the FD condition in the intrinsic region, the forward I–V curves of M10 in Fig. 6(c) are shifted down comparing to those of the devices before annealing, becoming close to the S10 I–V curves in Fig. 2(a), and in quantitative agreement with the experimental observations in Fig. 3(b) and (d). As for the integrated recombination rates correspondingly depicted in Fig. 6(d) and (e), the TAR at the front surface dominates and degrades the device forward output current of M10, indicating that the device output behavior in the forward mode

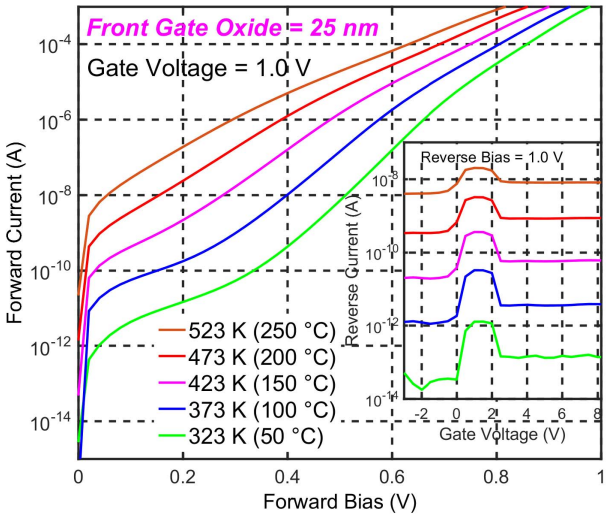

Fig. 7. Simulated forward current of the front-gated M10 diode after annealing, with the temperature varied from 323 to 523 K, as a function of front gate bias (gate oxide = 25 nm). Device parameters are set as the "After Annealing" conditions in Table II. The inset depicts the corresponding leakage current of the device at a reverse bias of 1.0 V.

is mainly affected by the front surface in which side the anode and cathode electrodes are located. The external bias V_G is applied to achieve the FD condition in the intrinsic region and minimize the TAR rate at the interfaces especially in the front interface, then optimize the diode forward characteristics in Fig. 6(c) and (e) at $V_G = 90$ V. In this research, with the trap density of 1×10^{11} cm^{-2}·eV^{-1}, the diode M10 presents the best forward characteristics, under $V_G = 90$ V, related to lower recombination rates.

C. Optimized Characteristics With a Front Gate

In the commercial 1.0-μm SOI CMOS technology, the p-i-n diode is monolithically integrated with MOS transistors, featuring a 300-nm-thick polysilicon gate and a 25-nm-thick SiO_2 layer as the gate dielectric, as depicted in Fig. 5. Using the polysilicon as the front gate (in this case, the silicon substrate is a floating contact) and implementing the electrical parameters of the optimized case of the diode M10 (i.e., volume carriers' lifetime $\tau = 5$ μs; interface traps $D_{itA(f)} = D_{itD(f)} = D_{itA(b)} = D_{itD(b)} = 1 \times 10^{11}$ cm^{-2}·eV^{-1} at the front and back interfaces in Table II), the forward anode current versus voltage characteristics are simulated under a front-gate voltage of 1.0 V, as well as the reverse cathode current versus front gate bias (at a reverse bias of 1.0 V) for temperatures of 50, 100, 150, 200, and 250 °C (Fig. 7). With temperature increase, the reverse leakage current increases due to its dependence on n_i [33].

Based on the reverse characteristics depicted in the inset of Fig. 7, the FD condition can be achieved in the p-i-n diode, with a front-gate voltage of 1.0 V for the whole temperature range. Thereafter, the forward characteristics of the p-i-n diode can be optimized to operate at a very low voltage of $V_G = 1.0$ V. In this case, the diode with a front gate bias can achieve and demonstrate good thermal linearity for a temperature range from 50 °C to 250 °C as depicted in Fig. 7,

TABLE III
THERMAL SENSITIVITY IN THE FRONT-GATE CASE

Sensitivity (mV/deg.)	0.01 μA	0.02 μA	0.03 μA	0.1 μA	1.0 μA
V_G= 1.0 V	−2.28	−2.25	−2.22	−2.10	−1.83

and the high sensitivity extracted in Table III. The diode voltage drops from 0.585 (resp. 0.534 in Fig. 7) to 0.084 V at $I_F = 0.02$ μA, with a demonstrated sensitivity of −2.25 mV/° in the temperature range of RT (resp. 50 °C in Fig. 7) to 250 °C. Moreover, the optimized diode can achieve good thermal linearity at I_F down to 0.01 μA with a sensitivity of −2.28 mV/°, with low-power consumption for thermal sensing and control application. Overall, based on the ideality factor in Fig. 4(b)–(d) [as well as device reproducibility and stability in Fig. 3(b) and (d)], in the range 1.0–0.02 μA of I_F, the sensitivity of the lateral p-i-n gated diode evolves as expected from the theory of diffusion current [14] and consistent between the experimental optimization and simulation analysis.

V. CONCLUSION

In this research, we investigated the optimization of the thermal sensing performance of a lateral SOI on-membrane p-i-n diode, after post-CMOS MEMS processing using DRIE and Al back-gate e-gun deposition. The forward I–V characteristics of the diode are degraded by the MEMS process steps, but are recovered and stabilized after carrying out low-temperature annealing (at 250 °C for 30 min, using the heating element embedded in the same membranes) and under a back-gate bias (here of 90 V experimentally due to the 1-μm-thick BOX) to achieve the FD condition in the intrinsic region of the diode. The device then achieves high thermal linearity in the large temperature range of RT to 200 °C with excellent sensitivity of −2.26 (−2.24) mV/° at 0.02 (0.03) μA constant forward current. Using Atlas/SILVACO simulations calibrated on experiments, we demonstrate that implementing a front gate with a 25-nm-thick SiO_2 dielectric, the device operation can also be optimized at a low gate bias of 1.0 V, extending the promising thermal sensing performances (i.e., linearity and sensitivity) up to 250 °C, thanks to better control of the front surface condition. The p-i-n diode studied in this work finally shows optimal low-power capability for gas sensing and IC thermal management applications.

REFERENCES

[1] S. Madhusoodhanan, S. Sandoval, Y. Zhao, M. E. Ware, and Z. Chen, "A highly linear temperature sensor using GaN-on-SiC heterojunction diode for high power applications," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1105–1108, Aug. 2017. doi: 10.1109/LED.2017.2714865.

[2] S. Santra, P. K. Guha, M. S. Haque, S. Z. Ali, and F. Udrea, "Si diode temperature sensor beyond 300°C," in *Proc. Int. Semiconductor Conf. (CAS)*, 2007, pp. 415–418. doi: 10.1109/SMICND.2007.4519747.

[3] V. A. Krasnov, S. V. Shutov, S. Y. Yerochin, and O. M. Demenskyi, "High temperature operation limit assessment for 4H-SiC Schottky diode-based extreme temperature sensors," *IEEE Sensors J.*, vol. 19, no. 5, pp. 1640–1644, Mar. 2018. doi: 10.1109/JSEN.2018.2883544.

[4] C. D. Matthus, T. Erlbacher, A. Hess, A. J. Bauer, and L. Frey, "Advanced 4H-SiC p-i-n diode as highly sensitive high-temperature sensor up to 460°C," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3399–3404, Aug. 2017. doi: 10.1109/TED.2017.271127.

[5] S. Rao, G. Pangallo, and F. G. D. Corte, "4H-SiC p-i-n diode as highly linear temperature sensor," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 414–418, Jan. 2016. doi: 10.1109/TED.2015.2496913.

[6] G. Brezeanu *et al.*, "High temperature sensors based on silicon carbide (SiC) devices," in *Proc. Int. Semiconductor Conf. (CAS)*, Oct. 2015, pp. 3–10. doi: 10.1109/SMICND.2015.7355147.

[7] M. Mansoor, I. Haneef, S. Akhtara, A. D. Luca, and F. Udrea, "Silicon diode temperature sensors—A review of applications," *Sens. Actuators A, Phys.*, vol. 232, pp. 63–74, Aug. 2015. doi: 10.1016/j.sna.2015.04.022.

[8] B. Gentinne, J.-P. Eggermont, D. Flandre, and J. P. Colinge, "Fully depleted SOI-CMOS technology for high temperature IC applications," *Mater. Sci. Eng. B*, vol. 46, nos. 1–3, pp. 1–7, 1997. doi: 10.1016/S0921-5107(96)01921-6.

[9] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ of ± 0.1 C from $-55°$C to $125°$C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005. doi: 10.1109/JSSC.2005.858476.

[10] I. Tobehn, A. Steinke, A. Albrecht, H. Hansch, M. Kunze, and T. Ortlepp, "Silicon based temperature sensors with extended temperature range and simple one-point calibration," in *Proc. 6th Int. Conf. Sensor Device Technol. Appl. (SENSORDEVICES)*, Apr. 2015, pp. 50–53.

[11] M. Malits and Y. Nemirovsky, "Comprehensive comparison of integrated temperature sensors in CMOS-SOI technology," in *Proc. IEEE Int. Conf. Microw., Commun., Antennas Electron. Syst. (COMCAS)*, Tel Aviv, Israel, Nov. 2015, pp. 1–5. doi: 10.1109/COMCAS.2015.7360443.

[12] M. Malits and Y. Nemirovsky, "Nanometric integrated temperature and thermal sensors in CMOS-SOI technology," *Sensors*, vol. 17, no. 8, p. 1739, 2017. doi: 10.3390/s17081739.

[13] A. De Luca, V. Pathirana, S. Z. Ali, D. Dragomirescu, and F. Udrea, "Experimental, analytical and numerical investigation of non-linearity of SOI diode temperature sensors at extreme temperatures," *Sens. Actuators A, Phys.*, vol. 222, pp. 31–38, Feb. 2015. doi: 10.1016/j.sna.2014.11.023.

[14] F. Udrea, S. Santra, and J. W. Gardner, "CMOS temperature sensors—Concepts, state-of-the-art and prospects," in *Proc. Int. Semiconductor Conf.*, Oct. 2008, pp. 13–15. doi: 10.1109/SMICND.2008.4703322.

[15] A. De Luca, V. Pathirana, S. Z. Ali, and F. Udrea, "Silicon on insulator thermodiode with extremely wide working temperature range," in *Proc. 27th Transducers Eurosensors, 17th Int. Conf. Solid-State Sens., Actuators Microsyst. (TRANSDUCERS & EUROSENSORS)*, 2013, pp. 1911–1914. doi: 10.1109/Transducers.2013.6627166.

[16] Y. Li, J. Yu, H. Wu, and Z. Tang, "Design and fabrication of a CMOS-compatible MHP gas sensor," *AIP Adv.*, vol. 4, no. 3, 2014, Art. no. 031339. doi: 10.1063/1.4869616.

[17] S. Z. Ali, F. Udrea, W. I. Milne, and J. W. Gardner, "Tungsten-based SOI microhotplates for smart gas sensors," *J. Microelectromech. Syst.*, vol. 17, no. 6, pp. 1408–1417, 2008. doi: 10.1109/JMEMS.2008.2007228.

[18] P. K. Guha *et al.*, "Novel design and characterisation of SOI CMOS micro-hotplates for high temperature gas sensors," *Sens. Actuators B, Chem.*, vol. 127, no. 1, pp. 260–266, Oct. 2007. doi: 10.1016/j.snb.2007.07.047.

[19] S. J. Park *et al.*, "High sensitive NO_2 gas sensor with low power consumption using selectively grown ZnO nanorods," *J. Nanosci. Nanotech.*, vol. 10, no. 5, pp. 3385–3388, 2010. doi: 10.1166/jnn.2010.2261.

[20] A. De Luca, C. Falco, E. L. W. Gardner, J. D. Coull, and F. Udrea, "Diode-based CMOS MEMS thermal flow sensors," in *Proc. 19th Int. Conf. Solid-State Sens., Actuators Microsyst.*, Jun. 2017, pp. 2211–2214. doi: 10.1109/TRANSDUCERS.2017.7994516.

[21] S. Santra *et al.*, "ZnO nanowires grown on SOI CMOS substrate for ethanol sensing," *Sens. Actuators B, Chem.*, vol. 146, no. 2, pp. 559–565, 2010. doi: 10.1016/j.snb.2010.01.009.

[22] M. Mansoor *et al.*, "An SOI CMOS-based multi-sensor MEMS chip for fluidic applications," *Sensors*, vol. 16, no. 11, p. 1608, 2016. doi: 10.3390/s16111608.

[23] G. Li *et al.*, "Multiple-wavelength detection in SOI Lateral PIN diodes with backside reflectors," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7368–7376, Sep. 2017. doi: 10.1109/TIE.2017.2694393.

[24] A. P. Lee and B. J. Reedy, "Temperature modulation in semiconductor gas sensing," *Sens. Actuators B, Chem.*, vol. 60, no. 1, pp. 35–42, 1999. doi: 10.1016/S0925-4005(99)00241-5.

[25] S. K. Rai, K. W. Kao, S. J. Gow, and J. A. Yeh, "Ultrathin (~10 nm) InN resistive gas sensor for selectivity of breath ammonia gas by using temperature modulation," in *Proc. 11th IEEE Annu. Int. Conf. Nano/Micro Eng. Mol. Syst. (NEMS)*, Apr. 2016, pp. 17–20. doi: 10.1109/NEMS.2016.7758307.

[26] P. Gwizdz, M. Radecka, and K. Zakrzewska, "Array of gas sensors based on TiO_2 upon temperature modulation," in *Proc. 15th Int. Sci. Conf. Optoelectron. Electron. Sensors (COE)*, 2018, pp. 1–4. doi: 10.1109/COE.2018.8435162.

[27] M. de Souza, M. A. Pavanello, and D. Flandre, "Low power highly linear temperature sensor based on SOI lateral PIN diodes," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2016, pp. 1–3. doi: 10.1109/S3S.2016.7804382.

[28] W. Shockley, "The theory of *p-n* junctions in semiconductors and *p-n* junction transistors," *Bell Syst. Tech. J.*, vol. 28, no. 3, pp. 435–489, 1949.

[29] G. Li, "Theoretical and experimental study of innovative thin-film gated SOI lateral PIN optoelectronic device," Ph.D. dissertation, Univ. Catholique de Louvain, Louvain-la-Neuve, Belgium, 2017.

[30] G. Li *et al.*, "Silicon-on-insulator photodiode on micro-hotplate platform with improved responsivity and high-temperature application," *IEEE Sensors J.*, vol. 16, no. 9, pp. 3017–3024, May 2016. doi: 10.1109/JSEN.2016.2530020.

[31] S. Santra, P. K. Guha, S. Z. Ali, I. Haneef, and F. Udrea, "Silicon on insulator diode temperature sensor—A detailed analysis for ultra-high temperature operation," *IEEE Sensors J.*, vol. 10, no. 5, pp. 997–1003, May 2010. doi: 10.1109/JSEN.2009.2037822.

[32] G. Li, V. Kilchytska, N. André, L. A. Francis, Y. Zeng, and D. Flandre, "Leakage current and low-frequency noise analysis and reduction in a suspended SOI lateral p-i-n diode," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4252–4259, Oct. 2017. doi: 10.1109/TED.2017.2742863.

[33] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007, ch. 2, pp. 73–75.

[34] *Atlas User's Manual: Device Simulation Software*, Silvaco Inc., Santa Clara, CA, USA, Feb. 2016, pp. 100–696.