Environmental Analysis of RF Substrates

Benjamin Vanhouche†, Pieter Cardinael‡, Lizzie Boakes, Lars-Åke Ragnarsson, Cédric Rolin, Jean-Pierre Raskin‡, Bertrand Parvais†
imec, Leuven, Belgium †also with Vrije Universiteit Brussel, Brussels, Belgium, ‡ ICTEAM, UCLouvain, Louvain-la-Neuve, Belgium
benjamin.vanhouche@imec.be

***Abstract*—** In order to incorporate environmental considerations into the decision criteria used to select substrates for radio-frequency integrated circuits (RF IC) technologies, we report here a comparative cradle-to-gate life cycle assessment (LCA) for Si and III-V state-of-the-art RF technologies. It appears that the global warming potential (GWP) of GaN-on-SiC is penalized by the high manufacturing energy of SiC wafers. Although less impactful than SiC, GaAs substrates show a higher GWP than Si-based technologies, which is also linked to an energy-intensive wafer fabrication. For GaN-on-Si, the epitaxy of the ~2.5 um-thick III-N layers represents an important part of the emissions making it ~30% more impactful than TR SOI substrates. In terms of abiotic depletion potential (ADP), the relatively large amount of Ga and As required to fabricate GaAs wafers leads to the highest ADP of all substrates. SiC also shows a high ADP due to the energy-intensive wafer fabrication. A significantly lower ADP is obtained for Si-based technologies.

Keywords—Life cycle assessment, wafer, Silicon, Silicon-on-insulator, Gallium Nitride, Gallium Arsenide, Silicon Carbide, Global Warming Potential, Abiotic Depletion Potential

I. Introduction

It is known for several decades that the environmental impact of human activities leads to the crossing of planetary boundaries **[1] [2]**. Among the different planetary boundaries, Climate change is often reported because of the serious consequences of global warming, which are extensively exposed in IPCC reports **[3]**. To mitigate the associated risks, the Paris agreements aim to limit the global warming to +1.5 to +2°C by reducing the Greenhouse gases emissions by 7-8% every year. Ideally, all sectors should follow this trend, especially those with a large impact. The current impact of the ICT sector is estimated to account for ~3-4% **[4]** of the total annual emissions and is expected to increase, notably because of the fast increase in the number of devices and connections **[5]**. The emissions of these devices can be studied with life cycle assessments (LCAs). As an example, the emissions related to smartphones during their whole life cycle is in the order of 70 $kgCO_{2eq}$ **[6], [7]**. Interestingly, 70% of it originates in the production phase and only 20% in the use phase. 38% of the production part is due to the manufacturing of integrated circuits (IC). There are several ICs in a smartphone, each implementing a certain functionality. In this paper, we focus on the telecommunication (or RF) module. It becomes especially important to quantify the environmental aspects of RF ICs given that the number of connected devices is still expected to grow quickly, with the advent of future generations like 5G and 6G **[8]**.

The RF module (Figure 1) is composed of several blocks: (i) digital modem, (ii) RF chip and (iii) front-end module (FEM). In the digital modem, digital signals are processed and are then converted into the analog domain with DAC/ADC. Digital blocks are almost always made of Silicon CMOS technologies. The sustainability of these digital technologies is an important topic that is starting to gain attention **[9], [10], [11]**. This paper focuses on the 2 others blocks operating in the Analog/RF domain: the RF transceiver and the FEM. In these blocks, the signal is modulated to high frequency and amplified before being sent to the antennas. In the analog/RF domain, the technological choices are driven by several figures of merit (FoM), e.g. high signal to noise ratio (SNR); and high operating frequency. In addition, the handle wafer cannot be considered solely as a mechanical substrate (as is the case in digital technologies) because of the parasitic substrate-related effects that can occur at high frequencies and lead to RF losses and crosstalk if the substrate is conductive **[12]**. Semi-insulating and high resistive substrates are used to mitigate these concerns. In this paper, we will investigate several low-RF losses substrates that are relevant candidates for use in future generation RF FEM and transceivers. High resistivity Si has been used in Silicon-on-insulator (SOI) technologies for many years to reduce the crosstalk and short-channel effects **[12]**. Further RF loss reduction can be achieved by an additional passivation with a Trap-Rich (TR) layer, which is usually made of polysilicon. On the other hand, technologies based

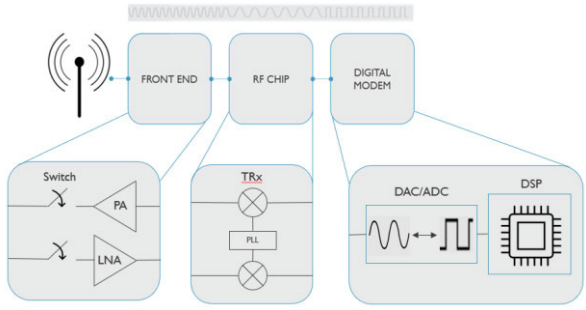
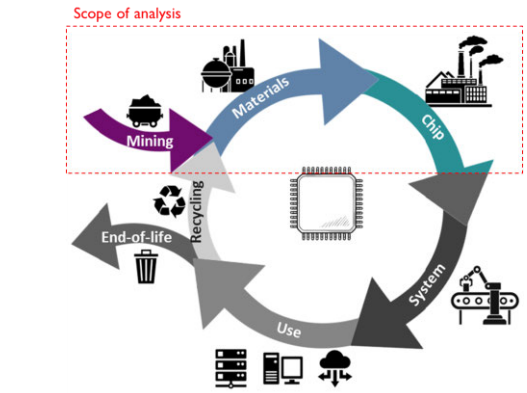


Figure 1 Block schematic for RF module.



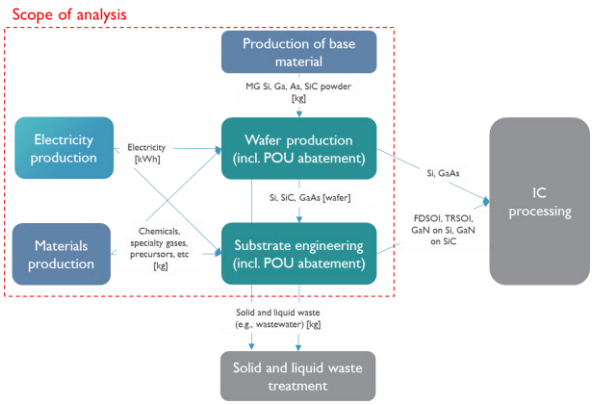


Figure 2. Breakdown of the cradle to gate scope for this study.

ISBN 978-3-00-079330-1 — Presented at the Electronic Goes Green 2024+ Conference

on wide-bandgap semiconductors, typically III-V (GaAs) and III-N (GaN) materials, are attractive both for implementing high-performance transistors functioning at a high supply voltage and for their semi-insulating properties.

In this paper, we propose to investigate the environmental impact of semiconductor RF substrates. The substrate represents the largest part, in volume and mass, of the end device. It is also expected that it has a non-negligible impact on the environmental impact of chip manufacturing. From existing studies on logic silicon-based chips (from N65 to N2), the Si substrates represent between 6% and 15% of the GWP and between 4% and 7% of the ADP **[11]**. Substrate engineering to reach RF requirements could increase that proportion. Our study aims at guiding technology choices by adding environmental indicators to the usual electrical FoM used in pathfinding. In this way, extending the PPAC-E (power, performance, area, cost + environment) concept introduced for digital technologies in **[13]** to the RF domain. This paper will focus on the RF substrates that are the most relevant for 5G applications and beyond (Table 1). It includes both wafers and engineered substrates. To avoid any confusion, we will keep the following nomenclature through the paper: a wafer is considered as one slice of the semiconductor ingot. It is made of only one material, without any further processes performed after the slicing. In the following, Si, GaAs and SiC substrates are the considered wafers. Engineered substrates are wafers that underwent further processing steps (epitaxy, deposition, etching, etc.). In this paper, TR SOI, fully depleted (FD) SOI, GaN-on-Si and GaN-on-SiC substrates are considered as engineered substrates. The term "RF substrate" is used to describe either a wafer or an engineered substrate.

II. Methodology

Life Cycle Assessment (LCA) is used to evaluate and compare the environmental impact of the different substrates. It follows the methodology defined by ISO14040 **[14]**, which consists of 3 steps: Goal and scope definition, life cycle inventory analysis, life cycle impact assessment. An interpretation step is also mandatory in parallel to the other steps.

A. Goal and scope definition

Scope - A cradle-to-gate LCA is used, meaning that we start from the extraction of the materials up to the end of the fabrication process. In other words, the focus is on the fabrication of IC, and the use-phase and the end-of-life of the device are not considered. This contrasts with many studies that focus on the use phase **[15]**. Moreover, previous studies **[6], [7]** reported that for user devices such as smartphones, the emissions mainly come from the production part (70%) and among it, the IC fabrication is the main contributor (38%). The detail of the scope is shown in Figure 2.

Functional unit - The definition of the functional unit (FU) is an important topic for LCA practitioners. It defines the service or product that is assessed by the LCA and it defines what will be benchmarked among the different technologies. It is important to keep this FU in mind while analysing the results. The chosen FU here is 1cm² of substrate, without any device on top. The unusable area of the wafer is not taken into account here (wafer yield = 100%) and all the processed wafers are considered (line yield = 100%, e.g. no broken wafer during the process). The motivation behind the FU is that we are comparing substrates with different sizes (from 150 to 300mm of diameter). Choosing a wafer as FU would thus make no sense and it is preferable to choose a certain wafer area. 1cm² is a standard normalized value for wafer area. It is worth noting that while this FU is well suited to benchmark the manufacturing cost, it does not include the fact that different aspects must be considered when benchmarking technologies at circuit/system application level. For instance, because of its higher power density, a GaN power amplifier will be more compact than its CMOS counterpart, for a given output power specification **[16]**.

Indicators - Only two indicators are considered in this study, Global Warming Potential (GWP) and Abiotic Depletion Potential (ADP). The GWP expresses the amount of Greenhouse Gases (GHG) released during the fabrication of the substrate. Every GHG has a certain GWP, expressed in kg $CO_{2,eq}$ to assess their contribution to climate change **[17]**. The final GWP of the substrate is also expressed in $kgCO_{2,eq}$. The ADP quantifies the material scarcity and expresses how much the device depletes abiotic resources. The ADP of a material *i* is computed w.r.t. a reference material *ref,* which is usually Antimony (Sb):

$$\boldsymbol{ADP_i = \frac{DR_i/(R_i)^2}{DR_{ref}/(R_{ref})^2}}.$$

with *DR* the extraction rate (in kg/year), *R* the ultimate resource of material in Earth's crust (in kg). ADP is expressed in kg Sb_{eq} **[18]**. A limitation of this indicator is that the ultimate resource is used and not the usable one. It is worth mentioning that electricity has an ADP. Even though the ADP is a measure of the scarcity and electricity is intangible. The ADP of electricity is due to all the materials used during the production and distribution of the electricity (e.g. power plant, distribution network, etc.).

Normalization and weighting – It can be tricky to analyse the results when they are expressed with different indicators. What is less sustainable between consuming $1kgCO_{2,eq}$ in term of GWP or $1kgSb_{eq}$ in term of ADP? To answer this question, normalisation factors (NFs) have been defined by JRC **[19]**. The way NFs are computed is by dividing the total impact per year in each indicator and dividing this by the number of human beings on earth.

$$NF_i = \frac{Total\ impact\ per\ year_i}{\#person\ on\ earth}$$

By using these NFs to normalize the impacts, we obtain a result in *person* for each indicator. These results show the impact of the

TABLE 1 - LIST OF THE SUBSTRATES WITH THEIR IMPORTANT FEATURES.

Substrates	Si	FDSOI	TRSOI	GaAs	GaN on Si	GaN on SiC
Size (diameter)	300mm	300mm	300mm	150mm	200mm (can be upscaled to 300mm)	150mm
Main Application / Location	Transceiver (TRX) / RF Chip	Transceiver (TRX) / RF Chip	Switch / Front end	Power Amplifier / Front end	Power Amplifier / Front end	Power Amplifier / Front end
Addition information	Most common substrate	Widely used in RF	State of the art performance for switches	III-V substrate	Combines good GaN properties with Si low cost and ease of use	State of the art for GaN substrate

number of people, over the course of a year, this activity represents. The results are different for each indicator but can be compared among them as they are now expressed in the same unit. Nevertheless, it is worth highlighting a few limitations of these NFs. First, the quality of the data for the total impact per year is not always perfect and can be questioned. Also, the NFs are based on the *Total impact per year*. If the *Total impact* increases from one year to the next, but the impact of the activity remains the same, the normalized impact of this activity will decrease due to a higher NF. This is questionable as the actual impact is not lower and therefore, not more sustainable. One improvement could be to consider the planet boundaries for every indicator instead of the total impact. In this work, we will provide results in both in their own indicators and normalized ones.

In order to address the relative importance of an indicator with respect to the other indicators, weighting factors (WFs) are introduced **[20]**. After normalization, the weighted average of the different indicators is calculated, resulting in a single FoM. This method has also limitations: the WFs are based on surveys on the population and LCA experts, literature reviews and robustness of the indicators. Even though these WFs are well documented and follow a clear methodology, they are based on a surveys and arbitrary choices.

B. Life cycle inventory analysis

The life cycle inventory is based on imec.netzero, an LCA tool developed in imec **[11]**. The tool consists of databases, process flows and fab models. The databases contain the life cycle inventory of the different steps, and characterization factors. The process flows are lists of steps. We will now describe the main steps of the flow considered for the different RF substrates (Table 2).

Si wafer – The fabrication starts with the extraction of raw materials: quartz or silica sand. It is then reduced to metal grade (MG) silicon. This MG Si in then purified using the Siemens process to electronic grade (EG) silicon. A Czochralski process is then performed to reach single crystal Silicon ingot. Finally, the ingot is sliced into wafers. The model for the Si wafer fabrication is based on Ecoinvent **[21]**.

SOI substrates – The fabrication of an SOI substrate by SmartCut process **[22]** requires 2 Si wafers (flow described in previous paragraph): the "Seed" and the "Handle". For the TR SOI, a thick layer (~2 µm) of polycrystalline silicon is deposited on top of the Handle wafer (this step is skipped for the FDSOI). Both wafers are then oxidized. Hydrogen ions are implanted in the seed wafer a few nm below the Si surface through the oxide. The 2 substrates are then bonded together with an oxide-oxide bonding. A rapid thermal annealing is used to split the two substrates at the location where the ions were implanted, leaving a thin Si film on the oxide and forming the SOI substrate. The remaining Seed Si wafer can then be reused as a seed. The number of reuses is set at 50 times in the present study. After 50 uses, the wafer is too thin to be treated properly by the tools. The process includes additional annealing, cleaning, and polishing steps, which are considered in the model.

GaAs wafer – The flow is based on the model made by Smith **[23]**. After extraction, Gallium and Arsenic are purified up to 7N and annealed to reach polycrystalline GaAs. GaAs ingots are obtained using Vertical Gradient Freeze (VGF) process. This VGF uses a furnace that heats GaAs up to 1200°C **[24]**, operating for between one and two weeks per ingot. Our model assumes a duration of one week. The high thermal budget makes this a very energy-intensive process. Once the ingot has been manufactured, it is sliced into wafers.

GaN-on-Si engineered substrate – Starting from Si wafer (process flows described earlier), GaN and intermediate buffer layers are grown using metalorganic chemical vapor phase epitaxy (MOVPE) using organic precursors (TMGa, TMAl, NH_3). The process last ~3hours to achieve the considered 2.5um thickness of the III-N layers.

GaN-on-SiC engineered substrate – The SiC wafer is firstly fabricated from SiC powder made with Acheson Process **[25]**. Afterward, the ingot is grown with physical vapor transportation (PVT) method. PVT sublimizes the SiC powder; the SiC gas then propagates up to a Seed crystal placed above the reactor, where the ingot is grown. The method requires high temperatures (above 2000°C), which makes it very energy intensive. Once the ingot is grown, it is sliced into wafers. The model to assess the impact of SiC wafer fabrication is based on **[26]**. A MOVPE step is then performed on top of the SiC wafer to grow the GaN film. Given a smaller lattice mismatch between GaN and SiC, compared to GaN and Si, a thinner buffer is considered here (1.25µm).

C. Scenario Definition

As explained previously, the processes are energy-intensive, meaning that they consume a large amount of electrical energy. It is therefore worth mentioning how the electricity is considered in our simulations. The impact of the electricity on GWP and ADP depends on the electricity mix and distribution network, which is location dependent. For instance, France mainly produces electricity with nuclear power plants while China is mainly using coal. The carbon intensity of electricity in France is therefore lower than in China, respectively 62 gCO2eq/kWh vs 882 gCO2eq/kWh **[27]**. The impact of the distribution network is location sensitive, but it also depends on the electrical voltage that is used. Low voltage network is larger than high voltage one, therefore its impact is also higher. Even if, in practice, the different substrates are not produced in the same place, this analysis will consider the same electricity source for the fabrication of each substrate, which is the global electricity mix from Ecoinvent **[28]**. Furthermore, a medium voltage type of electricity is considered for the default scenario. The motivation behind it is that industries with high volume manufacturing usually have their own

TABLE 2 - OVERVIEW OF THE FABRICATION STEPS CONSIDERED IN THIS WORK.

Substrates	**Si**	**SOI**	**GaAs**	**GaN on Si**	**GaN on SiC**
Fabrication steps (process)	MG Si	Si wafers	Ga – As	Si wafer	SiC powder
	EG Si (Siemens)	SOI substrate (SOI process)	Ga 7N – As 7N (purification)	GaN on Si (GaN Epitaxy)	SiC ingot (PVT)
	Si ingot (Czochralski)		Polycrystalline GaAs (Annealing)		SiC wafer (slicing)
	Si Wafer (Slicing)		GaAs ingot (VGF)		GaN on SiC (GaN Epitaxy)
			GaAs wafer (slicing)		

TABLE 3 - ELECTRICITY MIX PER SCENARIO

Scenario	*Electricity GWP ($gCO2_{eq}$/kWh)*	*Electricity ADP ($mgSb_{eq}$/kWh)*
A – Global electricity mix	708	0.650
B – Belgian electricity mix	206	0.833
C – Onsite electricity production	507	0.156
D – Improved epitaxy throughput	708	0.650

transformers and take their electricity from the medium voltage distribution network. Nevertheless, several scenarios will be considered to analyse the impact of this assumption. The impact of the electricity for different scenarios is shown in Table 3.

III. RESULTS

A. Life Cycle impact assessment

Scenario A (default)

The results for scenario A are plotted in Figure 3. For GWP, the GaN-on-SiC substrate is one order of magnitude higher than the other substrates. This is mainly due to the high impact of the SiC substrate fabrication. Referring to the breakdown for the SiC substrate (Figure 4), growing the ingot with the PVT process represents almost the entire part of the emissions. The GWP of the other substrates is comparable. GaAs has the second highest GWP, mainly due to the VGF process (Figure 4), which is long and energy intensive. GaN-on-Si substrate is the third highest. Its associated GWP is mainly due to the electricity consumption, which is significant for the epitaxy step as shown in Figure 5. For the three last substrates (TRSOI, FDSOI and Si) the global warming potential mainly comes from the Si wafer fabrication. Looking at the breakdown (Figure 4), the Siemens process (to produce EG Si) and the Czochralski process (to grow to ingot) are responsible for the largest part of the impact as these steps are very energy intensive.

Regarding ADP, GaAs substrate has the largest impact, mainly due to the production of As and Ga (Figure 4) that are relatively scarce materials **[18]**. GaN-on-SiC has the second largest ADP, resulting from the production of SiC wafer that uses PVT process.

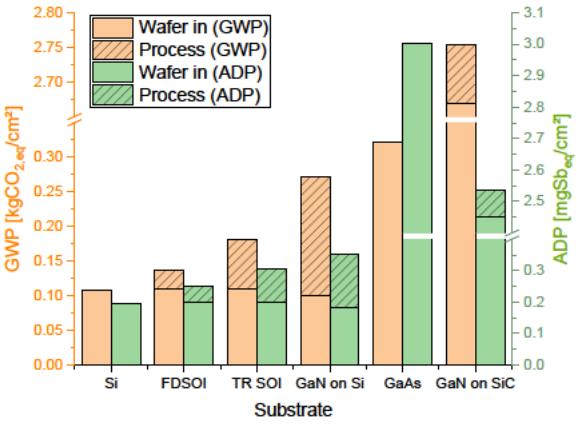


Figure 3 : Global Warming Potential (GWP) and Abiotic Depletion Potential (ADP) of RF substrates in $kgCO_{2eq}$ and $mgSb_{eq}$ respectively. The electricity mix is the one from Scenario A. "Wafer in" refers to the raw wafer (Silicon, GaAs and SiC). "Process" refers to the process done on top of the wafer (SOI process or epitaxy) to reach the engineered substrate (FD SOI, TR SOI, GaN on Si, GaN on SiC).

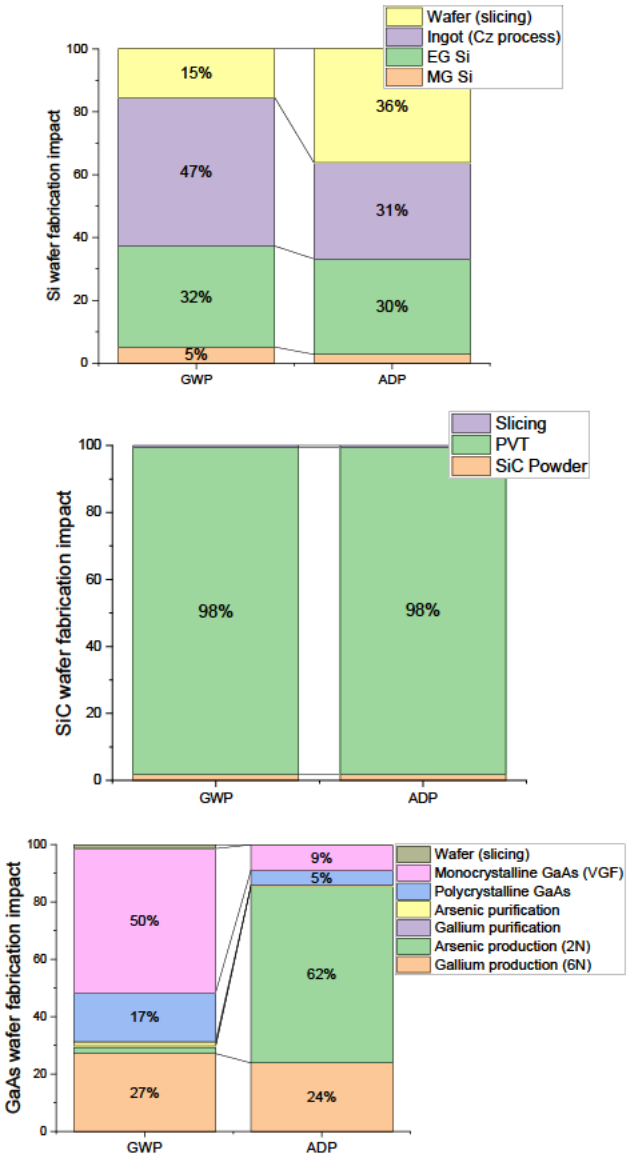


Figure 4. Breakdown, per step, of the impacts (GWP and ADP) of the wafer fabrication (a) Si wafer, (b) SiC wafer, (c) GaAs wafer. These wafers correspond to the "wafer in" in Figure 3.

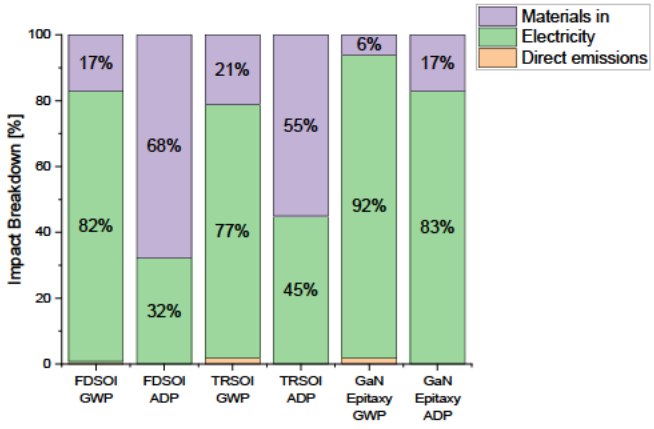


Figure 5. Breakdown of the impacts (GWP and ADP) of the processes for the engineered substrates (FDSOI, TRSOI, GaN on Si, GaN on SiC). These processes correspond to the "Process" in Figure 3. The "GaN epitaxy" is common to "GaN on Si" and "GaN on SiC".

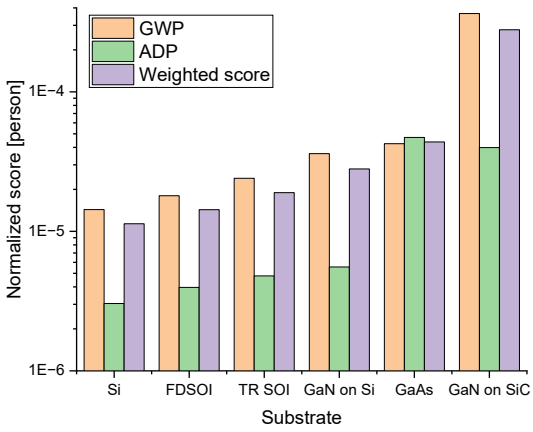


Figure 6: Global Warming Potential and Abiotic Depletion Potential of the different substrates normalized with Normalization factors defined be JRC. Weighted score based on the weighting factors defined by JRC for the 2 indicators. The electricity mix is the one from Scenario A.

The Si based substrates are one order of magnitude lower than GaAs and GaN-on-SiC. Among them, GaN-on-Si is slightly higher. The ADP of epitaxy is mainly due to the electricity consumption rather than the materials that are used. Indeed, relatively low amounts of Ga are used to fabricate a thin film of III-N material. The ADP of the Si wafer is distributed between the three last steps of its fabrication, i.e. purification step to EG Si, Czochralski process to grow the ingot, slicing into wafers. The ADP of MG Silicon is very low: raw Si is not scarce at all as it is the 2nd most abundant element on earth **[29]**. For the FDSOI and TRSOI processes, their ADP is dominated by the materials that are used, typically slurries for the CMP steps.

The normalized and weighted scores for every substrate are shown in Figure 6. The GWP is higher than ADP for every substrate except GaAs. This highlights the particularly high ADP of GaAs wafer. For the other substrates, climate change impact is more concerning than resource depletion. Even though GaAs has the highest ADP, the weighted score follows the same trends as the GWP. This is explained by the fact that the weight of GWP is higher than ADP in the weighted average.

Scenario B (Belgian electricity mix)

This scenario simulates the fabrication of the substrates in Belgium. As shown in Table 3, the Belgian electricity mix has a lower GWP than the Global electricity mix, but a comparable ADP. This is why only the GWP will be analysed here (Figure 7). As mentioned above, all the processes are energy intensive. Reducing the GWP of the electricity mix has therefore a significant impact: depending on the substrate, the GWP is reduced by a factor 1.7 up to 3.3 compared to Scenario A. Even though GaN-on-SiC remains far above other substrates in terms of GWP, the strongest reduction by changing electricity mix is observed for GaN-on-SiC, followed by GaN-on-Si. This can be explained by the fact that the GWP of both SiC wafer manufacturing and GaN epitaxy is largely dominated by electricity consumption.

Scenario C (Onsite electricity production)

As a significant part of the ADP of electricity comes from the distribution network, an efficient way to reduce the ADP is therefore to produce the electricity on-site. Scenario C simulates an onsite production of electricity with natural gas in a combined cycle power plant, taking also into account the losses due to the conversion from

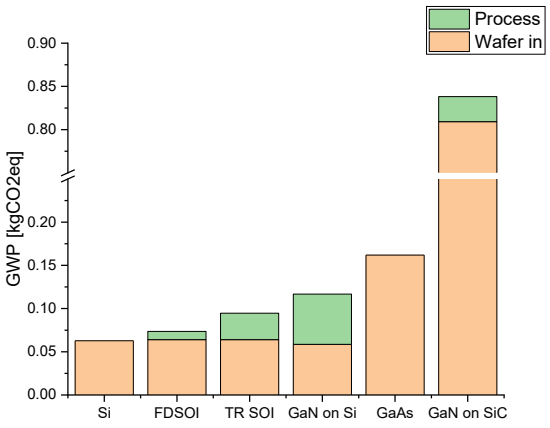


Figure 7. GWP of the substrates fabricated with a Belgian Electricity mix (Scenario B). “Wafer in” and “Process” are defined in Figure 3.

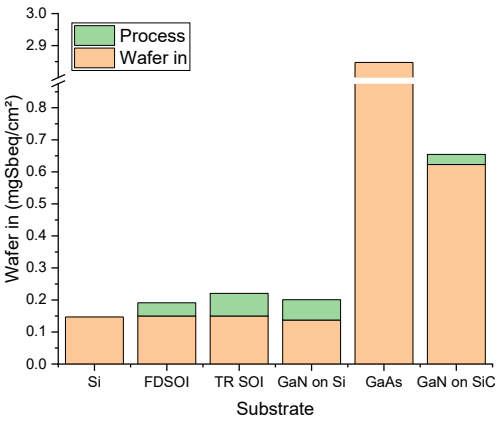


Figure 8. ADP of the substrate for onsite electricity production with CHP (Scenario C). “Wafer in” and “Process” are defined in Figure 3.

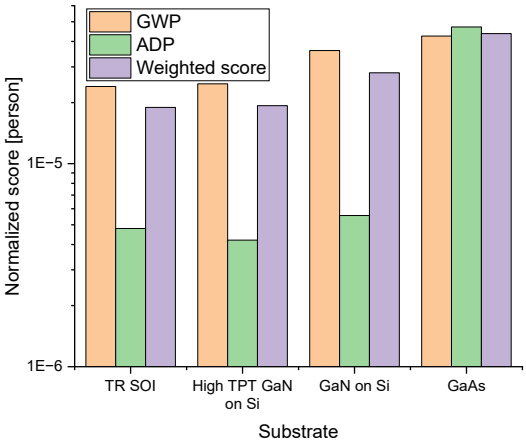


Figure 9. Global Warming Potential and Abiotic Depletion Potential of the different substrates normalized with Normalization factors defined be JRC. Weighted score based on the weighting factors defined by JRC for the 2 indicators. The electricity mix is the one from Scenario D. “High TPT GaN on Si” refers to a GaN on Si substrate with a throughput for GaN Epitaxy that has been doubled.

low to medium voltage (1% considered **[30]**). As shown in Table 3, the on-site electricity production mainly affects the ADP of electricity. So, only the ADP results will be analysed here. The results for this scenario are plotted in Figure 8. In this scenario, the GaN-on-Si substrate has a lower ADP than TRSOI, although it stays in the same order of magnitude. The reason is that electricity has a strong contribution to the ADP of epitaxy. Compared to Scenario A, a strong decrease in the ADP of GaN-on-SiC substrates is observed. It is a consequence of the large contribution of electricity in the manufacturing of SiC wafer. On the other hand, the ADP of GaAs wafers only decreases by 5%. Indeed, the high ADP of this wafer mainly comes from the use of scarce materials like Ga and As rather than from the electricity use.

Scenario D (Improved epitaxy throughput)

As shown in scenario A, even though the epitaxy is the only step to go from a Si wafer to a GaN-on-Si engineered substrate, it can have a higher impact than the Si wafer. The long epitaxy process time results from the thick buffer that is grown to relax the lattice mismatch between GaN and Si. Scenario D considers a fab with an epitaxy throughput improvement by a factor 2, and a proportionally reduced step duration. The results of this scenario are shown in Figure 9. By reducing the impact of the epitaxy by a factor of 2, the GWP of GaN-on-Si is reduced by 1.46 and its ADP is reduced by 1.32. Looking at the normalized score, GaN-on-Si is now in the same order of magnitude of TRSOI, slightly higher for GWP and slightly lower for ADP. Because of the higher weight of GWP in the weighted score, TRSOI keeps a smaller final normalized score, even if both are comparable (1.89e-5 vs 1.93e-5 [person]).

B. Interpretation

The results show that electricity has a large impact on GWP. Using non-fossil based electricity mix can thus strongly reduce the climate change impact. The impact of electricity over ADP is smaller than over GWP, especially for the GaAs wafer where reducing the ADP of electricity has only a small impact. Indeed, reducing the ADP of GaAs seems difficult as the material is inherently scarce due to the use of large amount of Gallium and Arsenic. A significant reduction of ADP can be obtained by reducing the scarce materials used, typically using thin film like in GaN-on-Si. Indeed, one advantage of GaN-on-Si over GaAs is the fact that only a very limited amount of Ga is used per wafer, which significantly reduced the ADP compared to an entire wafer. Nevertheless, epitaxy has a non-negligible impact, especially for GaN-on-Si. Reducing the thickness of ADP is promising to reduce the impact of GaN-on-Si and reach something close to TRSOI. It is important to keep in mind that this analysis is done for 1 cm² of substrate. The fact that one technology has a higher score than another one does not directly mean this technology is less sustainable. The area of each technology to reach the same application should be considered in future research.

C. Benchmark

This subsection compares our bottom-up results with the top-down data provided by other companies. Industry sustainability reports often contain only GWP. ADP will therefore not be considered here. Also, the benchmark is limited to SOI and Si substrates, given the lack of data for the other substrates.

Data in manufacturers sustainability reports are often aggregated or incomplete to be able to compute an impact per wafer. The report for SUMCO **[31]** was selected here since it provides the most relevant information to compute the impact per wafer. SUMCO is a wafer manufacturer which starts from polysilicon (electronic grade) and provides Si wafers. They are then only responsible for the Czochralski process and the slicing. The number expressed in $kgCO_{2eq}$/wafer only contains the Scope 1 & 2 **[32]**, which correspond respectively to the direct emissions, and the indirect emissions due to electricity consumption. The rest of the supply chain is not considered. Nevertheless, the complete Scope 3 is also provided and can be included to find emissions per wafer and per cm². Taking the average over the past 4 years, we find 72.72 gCO_{2eq}/cm^2. The information related to this computation is available in Table 4.

The benchmark for SOI wafers is based on Soitec's sustainability report 2021-2022 **[33]** and financial report 2021-2022 **[34]**. The emissions per wafer are not directly provided. Nevertheless, with the information in the financial report, it is possible to do an economical allocation of the emissions related to all the 300mm wafers. The capacity of production is also available, we can thus find the impact per wafer and per cm² equal to 117.28 gCO_{2eq}/cm^2. All the information related to this computation is available in Table 5.

In both cases, the bottom-up results are slightly higher than the top-down ones. It can be explained by the different electricity mixes considered. Indeed, the sustainability reports are company specific and consequently location specific. The carbon intensity of the electricity can therefore vary significantly. Analysing the report of SUMCO, a carbon intensity around 0.4 $kgCO_{2eq}$/kWh can be deduced. Soitec's fab for 300mm SOI wafers fabrication is based in Bernin, France and Pasir Ris, Singapore. In both cases, the carbon intensities are lower than the ones considered in our analysis. This has a large impact because, as mentioned above, the manufacturing process is energy intensive. Other limitations can be pointed out, such as the difference in scope, in methodology, the aggregated data like the fact that all the 300mm SOI wafer are considered the same, we do not include the differences between FDSOI, RFSOI, Imager-SOI,

TABLE 4 - TOP-DOWN COMPUTATION BASED ON SUMCO SUSTAINABILITY REPORT [31].

SUMCO reports				
Year	***2019***	***2020***	***2021***	***2022***
Scope 1 (tCO2eq)	26	25	27	28
Scope 2 (tCO2eq)	702	765	812	765
Scope 3 (tCO2eq)	612	694	758	882
Impact per wafer, scope 1 & 2 (kgCO2eq/wafer)	27.6	28.6	26.8	23.7
Number of wafer	26,377	27,622	31,306	33,460
Total Impact per wafer (kgCO2eq/wafer)	50.8	53.7	51	50
Impact per cm² (kgCO2eq/cm²)	**71.87**	**76**	**72.12**	**70.82**

TABLE 5 - TOP-DOWN COMPUTATION BASED ON SOITEC FINANCIAL AND SUSTAINABILITY REPORTS [33] [34].

Soitec reports	
Total emission (tCO2eq)	249,147
Total revenue (€ million)	862.7
Emission per € (tCO2eq/€ million)	288.7
Revenue for 300mm SOI substrate (€ million)	488
Emissions for all 300mm SOI wafer (tCO2eq)	140,934
Number of 300mm SOI wafer	1,700,000
Emissions per 300mm SOI wafer (kgCO2eq/wafer)	82.9
Emissions per cm² (gCO2eq/cm²)	**117.28**

etc. Also, the economical normalization can lead to differences. Nevertheless, this benchmark shows that the results found in this paper are in the same order of magnitude as what we can find in companies reports.

D. Criticality

Indicators that are usually used to assess the sustainability of materials from a social perspective are criticality (based on economic importance and supply risk) and the conflict minerals list. A mineral is defined as "conflict mineral" if the minerals trade can be used to finance armed groups, fuel forced labour and other human rights abuses, and support corruption and money laundering **[35]**. There are currently 4 materials in the list: Tin, Tungsten, Tantalum and Gold, and none of them are used in the substrates analysed in this paper. A focus will thus be done on the criticality.

A material is defined as critical if it exceeds a certain threshold in term of economic importance (EI) and supply risk (SR). The computations of the indicators for EI and SR are defined here **[36]**. The list of critical materials depends on the location, indeed a country that hosts the production of a material has a lower supply risk than another one which does not produce the same material. In this paper, we will analyse the list defined by EU **[36]** and USA **[37]**.

For the EU, Gallium, Arsenic and Silicon metal are on the list of critical materials. In term of SR, Gallium has by far the highest score, followed by Arsenic and then Silicon Metal. For the EI, Silicon Metal is the most important, followed by Gallium and then Arsenic.

For US the most recent list is provided by USGS **[37]**. Among the materials of interest of this paper, this list contains arsenic and gallium. Nevertheless, the breakdown on the quantitative data for this list is not provided. The only quantitative data available is the one for the list of 2018 **[38]**. It is worth mentioning Silicon has not been evaluated. Gallium and Arsenic in the list. All the indicators are higher for Gallium.

Another list is provided for critical materials for energy [**39**]. Even though this list is slightly out of the scope, it contains several materials studied in the paper. A breakdown of their Supply risk and Importance to energy for short and medium term is given. Among the studied material, Gallium is the most critical, followed by Silicon Carbide and Silicon.

Although every material considered in this study is mentioned at least once, Gallium is on every list with high indicators. From a geopolitical perspective, it seems important to reduce Gallium as much as possible. Therefore, using Gallium in thin film (GaN on Si or GaN on SiC) or removing it from the fabrication process (SOI, Si) is better than using bulk GaAs.

It is also worth noting that, even though no conflict minerals are used in the fabrication of the substrates, some of them are used in the process for chip manufacturing. These ones must also be reduced, or their provenance must be tracked. This aspect should be part of the discussion for the technology choice.

IV. CONCLUSION

This paper analysed and compared the environmental impact of several substrates for RF applications, using a cradle-to-gate LCA for GWP and ADP impact. The substrates with the larger impact are GaN-on-SiC for GWP and GaAs for ADP. The breakdown of the impact is also given, highlighting the main contributors to the different impacts. The electricity consumption in the PVT for the GWP and ADP of GaN-on-SiC, the Ga and As production for the ADP of GaAs and the epitaxy for GaN-on-Si are important contributors. Several scenarios have also been simulated to reduce the impacts. It was observed that using less carbon-intensive electricity has a large impact on GWP for almost all the substrates, especially GaN-on-SiC. Using onsite energy production also reduces substantially the ADP of the substrates, except for GaAs wafer where the high ADP of the substrates is inherently linked to the materials used. Reducing the thickness of GaN layer can also substantially reduce the impact of GaN-on-Si and reach scores comparable to TRSOI.

Finally, the geopolitical aspect of the materials used has been studied through the scope of critical materials in Europe and US. Gallium is present on all the list with the highest score, nevertheless it is worth mentioning than Arsenic, Silicon metal and Silicon Carbide all belongs to, at least one list of critical materials.

Our study intends to guide the choice of the substrate for a technology, taking into account its environmental impact, in addition to the standard KPIs. Moreover, the breakdown can help future work to focus on specific steps to reduce the impact significantly.

ACKNOWLEDGMENT

The authors would like to thanks Laurent Van Winckel, François Chancerel, Lan Peng, Jakob Visker, Tobias Peissker, Laura Nyns and Sourish Banerjee for their inputs and their precious help.

REFERENCES

[1] D. H. Meadows, D. L. Meadows, J. Randers, and W. W. Behrens, "The Limits To Growth," in *Green Planet Blues*, 5th ed., Routledge, 2015.

[2] K. Richardson *et al.*, "Earth beyond six of nine planetary boundaries," *Sci. Adv.*, vol. 9, no. 37, p. eadh2458, Sep. 2023, doi: 10.1126/sciadv.adh2458.

[3] H. O. Pörtner *et al.*, "Climate change 2022: Impacts, adaptation and vulnerability," IPCC, 2022. Accessed: Mar. 28, 2024. [Online]. Available: https://library.wur.nl/WebQuery/wurpubs/594799

[4] D. Bol, T. Pirson, and R. Dekimpe, "Moore's Law and ICT Innovation in the Anthropocene," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Feb. 2021, pp. 19–24. doi: 10.23919/DATE51398.2021.9474110.

[5] "Cisco Annual Internet Report - Cisco Annual Internet Report (2018–2023) White Paper," Cisco. Accessed: Mar. 28, 2024. [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html

[6] L.-P. P.-V. P. Clément, Q. E. S. Jacquemotte, and L. M. Hilty, "Sources of variation in life cycle assessments of smartphones and tablet computers," *Environ. Impact Assess. Rev.*, vol. 84, p. 106416, Sep. 2020, doi: 10.1016/j.eiar.2020.106416.

[7] N. Moreau *et al.*, "Could Unsustainable Electronics Support Sustainability?," *Sustainability*, vol. 13, no. 12, Art. no. 12, Jan. 2021, doi: 10.3390/su13126541.

[8] "Ericsson Mobility Report November 2023," 2023.

[9] S. B. Boyd, *Life-Cycle Assessment of Semiconductors*. Springer Science & Business Media, 2011.

[10] L. Boakes *et al.*, "Cradle-to-gate Life Cycle Assessment of CMOS Logic Technologies," in *2023 International Electron Devices Meeting (IEDM)*, Dec. 2023, pp. 1–4. doi: 10.1109/IEDM45741.2023.10413725.

[11] "imec.netzero." Accessed: Mar. 28, 2024. [Online]. Available: https://netzero.imec-int.com/

[12] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2252–2261, Dec. 1997, doi: 10.1109/16.644646.

[13] M. Garcia Bardon *et al.*, "DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 41.4.1-41.4.4. doi: 10.1109/IEDM13553.2020.9372004.

[14] 14:00-17:00, "ISO 14040:2006," ISO. Accessed: Mar. 28, 2024. [Online]. Available: https://www.iso.org/standard/37456.html

[15] "Gallium Nitride and Silicon Carbide Fight for Green Tech Domination - IEEE Spectrum." Accessed: Mar. 28, 2024. [Online]. Available: https://spectrum.ieee.org/silicon-carbide

[16] "PA Survey." Accessed: Mar. 28, 2024. [Online]. Available: https://ideas.ethz.ch/Surveys/pa-survey.html

[17] Intergovernmental Panel On Climate Change, *Climate Change 2021 – The Physical Science Basis: Working Group I Contribution to the Sixth Assessment Report of the Intergovernmental Panel on Climate Change*, 1st ed. Cambridge University Press, 2023. doi: 10.1017/9781009157896.

[18] L. Van Oers and J. Guinée, "The Abiotic Depletion Potential: Background, Updates, and Future," *Resources*, vol. 5, no. 1, Art. no. 1, Mar. 2016, doi: 10.3390/resources5010016.

[19] E. Crenna, R. Pant, S. Sala, and M. Secchi, *Global normalisation factors for the environmental footprint and Life Cycle Assessment*. Luxembourg: Publications Office of the European Union, 2017.

[20] S. Sala, A. K. Cerutti, and R. Pant, "Development of a weighting approach for the Environmental Footprint".

[21] "market for single-Si wafer, for electronics - GLO - single-Si wafer, for electronics | ecoQuery." Accessed: Mar. 28, 2024. [Online]. Available: https://ecoquery.ecoinvent.org/3.10/cutoff/dataset/5951/documentation

[22] X.-Q. Feng and Y. Huang, "Mechanics of Smart-Cut® technology," *Int. J. Solids Struct.*, vol. 41, no. 16, pp. 4299–4320, Aug. 2004, doi: 10.1016/j.ijsolstr.2004.02.054.

[23] B. L. Smith, "Development and Life Cycle Assessment of Advanced-Concept III-V Multijunction Photovoltaics".

[24] "Growth - Crystal Growth Technologies: Wafer Technology." Accessed: Mar. 28, 2024. [Online]. Available: http://www.wafertech.co.uk/growth.htm

[25] P. J. Guichelaar, "Acheson Process," in *Carbide, Nitride and Boride Materials Synthesis and Processing*, A. W. Weimer, Ed., Dordrecht: Springer Netherlands, 1997, pp. 115–129. doi: 10.1007/978-94-009-0071-4_4.

[26] S. Schmidt, A. Díaz, S. Glaser, and M. Makoschitz, "A 'life cycle thinking' approach to assess differences in the energy use of SiC- vs. Si power semiconductors".

[27] "electricity, high voltage, production mix - CN-CCG - electricity, high voltage | ecoQuery." Accessed: Apr. 09, 2024. [Online]. Available: https://ecoquery.ecoinvent.org/3.10/cutoff/dataset/26503/impact_assessment

[28] "market group for electricity, medium voltage - GLO - electricity, medium voltage | ecoQuery." Accessed: Mar. 28, 2024. [Online]. Available: https://ecoquery.ecoinvent.org/3.10/cutoff/dataset/13269/documentation

[29] "Abundance of elements in Earth's crust," *Wikipedia*. Apr. 06, 2024. Accessed: Apr. 09, 2024. [Online]. Available: https://en.wikipedia.org/w/index.php?title=Abundance_of_elements_in_Earth%27s_crust&oldid=1217486691

[30] R. Itten and R. Frischknecht, "Life Cycle Inventories of Electricity Mixes and Grid".

[31] "Sustainability Report 2023".

[32] "Homepage | GHG Protocol." Accessed: Mar. 28, 2024. [Online]. Available: https://ghgprotocol.org/

[33] "2021- - Soitec," Soitec - Corporate - EN. Accessed: Apr. 09, 2024. [Online]. Available: https://www.soitec.com/en/company/sustainability-reports/2021-2022

[34] "2022-2023 - Soitec," Soitec - Corporate - EN. Accessed: Apr. 09, 2024. [Online]. Available: https://www.soitec.com/en/investors/financial-reports/2022-2023

[35] "Conflict Minerals Regulation: The regulation explained." Accessed: Mar. 28, 2024. [Online]. Available: https://policy.trade.ec.europa.eu/development-and-sustainability/conflict-minerals-regulation/regulation-explained_en

[36] Directorate-General for Internal Market, Industry, Entrepreneurship and SMEs (European Commission), M. Grohol, and C. Veeh, *Study on the critical raw materials for the EU 2023: final report*. Publications Office of the European Union, 2023. Accessed: Mar. 28, 2024. [Online]. Available: https://data.europa.eu/doi/10.2873/725585

[37] "U.S. Geological Survey Releases 2022 List of Critical Minerals | U.S. Geological Survey." Accessed: Mar. 28, 2024. [Online]. Available: https://www.usgs.gov/news/national-news-release/us-geological-survey-releases-2022-list-critical-minerals

[38] N. T. Nassar and S. M. Fortier, "Methodology and technical input for the 2021 review and revision of the U.S. Critical Minerals List," U.S. Geological Survey, 2021–1045, 2021. doi: 10.3133/ofr20211045.

[39] "2023 Critical Materials Assessment," 2023.