# Fully Liquid-Metal-Printed $SnO_2$ Thin-Film Transistors With $Al_2O_3$ Dielectrics

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***Abstract*— In this work, we present the first demonstration of fully printed thin-film transistors (TFTs) using the liquid-metal printing (LMP) technique for both the $SnO_2$ channel and $Al_2O_3$ dielectric layers and investigate annealing impact on the microstructure of LMP-$SnO_2$ films and electrical behavior of LMP-based $SnO_2$ TFTs. Through experimental characterization and TCAD simulations, we find that the overall device performance initially degrades below 310 °C due to increased oxygen vacancy ($V_O$) concentration but recovers at higher temperatures owing to the reduction in $V_O$ concentration and crystallization-induced suppression of interface defects. The LMP-$SnO_2$ TFTs on $SiO_2$/p$^+$-Si substrate annealed at 600 °C achieve a field-effect mobility of 10.35 $cm^2 \cdot V^{-1} \cdot s^{-1}$. The performance is further improved by implementing the LMP-$Al_2O_3$ gate dielectric, yielding a subthreshold swing (SS) of 654 mV/dec and a threshold voltage of 0.95 V. Finally, a functional zero-$V_{GS}$-load nMOS inverter unit, comprising both depletion and enhancement mode $SnO_2$ TFTs, demonstrates the potential application of this LMP technique for integrated circuits. This work establishes a novel strategy for fabricating high-performance metal–oxide TFTs and circuits via fully LMP-based manufacturing.**

***Index Terms*— Annealing, liquid-metal printing (LMP), TCAD simulation, thin-film transistors (TFTs), tin oxide.**

## I. Introduction

With the rapid development of high-performance electronic devices and integrated circuits, metal–oxide–semiconductor thin-film transistors (TFTs) have become core components for high-resolution displays [1], wearable devices [2], and next-generation flexible electronics [3]. Although the InGaZnO-based TFT technology has been industrialized, the development of vacuum-free, cost-effective, and energy-efficient fabrication process remains crucial [4], [5]. As an emerging metal–oxide synthesis method, liquid-metal printing (LMP) process utilizes van der Waals force to directly transfer the naturally formed, atomically thin metal–oxide films from the surface of liquid metal (e.g., Ga, Sn, In, Bi, and their alloys) onto the target substrate [6], [7], [8], [9]. This process eliminates the need for stringent vacuum conditions and can be directly conducted under ambient atmosphere [10], [11], offering significant advantages such as environmental friendliness, low cost, and process simplicity.

Recently, the liquid-metal printed $SnO_2$ has emerged as an active channel material for oxide TFTs, because of the low melting point (231.9 °C) of its tin (Sn) precursor, controllable phase transition from p-type SnO to n-type $SnO_2$, high optical transparency, and wide bandgap [12], [13]. Here, the formation of $SnO_2$ usually involves a state transition from $Sn^{2+}$ to $Sn^{4+}$, in which post-treatment like annealing is often carried out [14]. Previous studies have successfully fabricated the $SnO_2$ TFTs using the LMP techniques, achieving a field-effect mobility of 7.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ through optimization of printing and post-annealing temperatures [4]. Moreover, according to thermodynamic principles, the oxide that results in the greatest reduction of Gibbs free energy will dominate on the surface of the alloy liquid metal. Utilizing this property, the LMP technique has also been extended to fabricate various high-k dielectric films such as $Al_2O_3$, $HfO_2$, $Ga_2O_3$, and $Gd_2O_3$ [15], [16], combined with gas injection methods. For example, the LM-based $HfO_2$ insulators can exhibit a high dielectric constant of 39 and an ultrathin thickness of ~0.5 nm [15]. However, current studies only focused on the material properties of single-layered dielectric films. The monolithic integration of both channel and dielectric layers via full LMP processes remains unrealized for TFTs. Achieving such integration would further reduce fabrication costs while enhancing process compatibility.

In this work, we monolithically integrate the LMP-based $Al_2O_3$ gate dielectrics with $SnO_2$ channels to fabricate the fully liquid-metal printed TFTs (designated as FLMP-$Al_2O_3$/$SnO_2$

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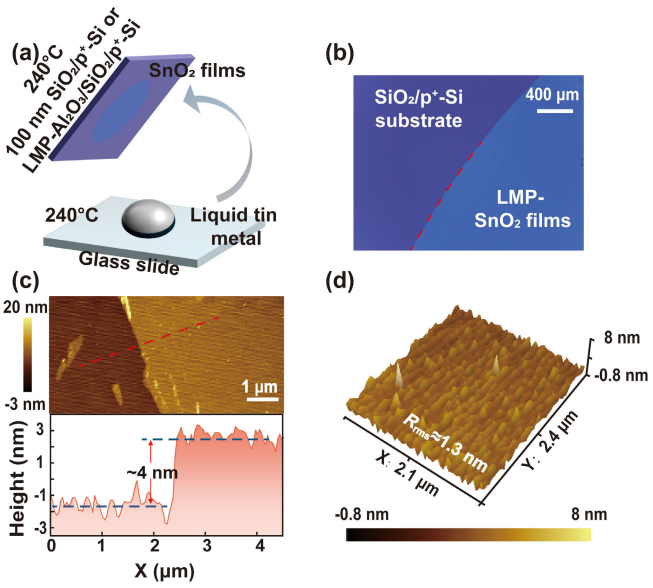


Fig. 1. (a) Schematic of $SnO_2$ films synthesized via LMP on two target dielectric/$p^+$-Si substrates. (b) Optical microscopy image of LMP-$SnO_2$ films on 100-nm $SiO_2/p^+$-Si substrate. (c) AFM surface topography and step-height profile of LMP-$SnO_2$ films on 100-nm $SiO_2/p^+$-Si substrate. (d) Top surface morphology of LMP-$SnO_2$ films on 100-nm $SiO_2/p^+$-Si substrate.

TFTs). Moreover, we optimize device performance using post-thermal annealing, uncovering the underlying mechanisms of defect evolutions and their impact on electrical characteristics through experimental characterization and Silvaco TCAD ATLAS simulation. Simultaneously, performance testing and evaluation are conducted on the LMP-$Al_2O_3$ dielectric layer. Finally, we demonstrate a functional zero-$V_{GS}$-load nMOS inverter using these devices, establishing a viable pathway for low-cost, vacuum-free electronics manufacturing via LMP.

## II. Experiments

To fabricate the bottom-gate staggered $SnO_2$-based TFTs, the $SnO_2$ layer is synthesized via LMP, as schematically depicted in Fig. 1(a). High-purity tin granules (5 g, 99.999%) are melted on a glass slide at 240 °C for 30 min under ambient atmosphere and scraped with an additional glass slide to remove any preexisting oxide layers with possible airborne contaminants. In the meantime, the target dielectric/$p^+$-Si substrate (1 × 1 cm) is preheated to the same temperature to avoid the solidification of the liquid metal during transfer. Here, two target dielectric/$p^+$-Si substrate configurations are implemented: 1) the commercial standard 100-nm-thick $SiO_2/p^+$-Si and 2) the LMP-$Al_2O_3/SiO_2/p^+$-Si (fabrication method is described in the following paragraph). Then, the dielectric/$p^+$-Si substrate is briefly touched (<1 s) with the liquid-metal surface that had a freshly formed metal–oxide. As a result, a naturally formed $SnO_2$ film is transferred onto the dielectric via van der Waals force. Next, the printed film is patterned using photolithography and wet etching in a 1-mol/L HCl solution, followed by a 10-min annealing at different temperatures ranging from 250 °C to 800 °C in ambient conditions. Finally, source and drain contacts (20-nm-thick Pd) are formed by thermal evaporation and photolithographic patterning, with the TFT channel dimensions defined as width/length ($W/L$) = 20/13 $\mu$m.

The LMP-$Al_2O_3/SiO_2/p^+$-Si sample is fabricated as described hereafter. To enhance adhesion by leveraging the affinity of liquid metal–oxides for oxidized surfaces, the $p^+$-Si is pre-treated in dry air at 1000 °C for 5 min to form a thin $SiO_2$ adherent layer prior to $Al_2O_3$ printing. Subsequently, the $Al_2O_3$ film is printed onto the pre-treated $p^+$-Si substrate at 400 °C via LMP process from a Ga–Al alloy (10 wt% Al), which is prepared by melting high-purity metals (99.999% Ga and Al) at 450 °C for 2 h in air. The remaining solidified metal is eliminated through ethanol cleaning (50 °C) and mechanical wiping with lint-free swabs. The liquid-metal printed films are kept under vacuum prior to characterization by atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), and grazing-incidence X-ray diffraction (GIXRD). The XPS measurements are performed without surface pretreatment. Since the film thickness (6 nm for LMP-$Al_2O_3$ and 4 nm for LMP-$SnO_2$) is smaller than the effective XPS probing depth, the measured XPS signal can reflect the overall film composition. Moreover, metal–insulator–metal (MIM) structures of Pd/LMP-$Al_2O_3$/Au and Pd/LMP-$Al_2O_3/SiO_2/p^+$-Si are fabricated with the electrode dimension of 160 × 160 $\mu$m. The capacitance–voltage ($C-V$) curves of the MIM capacitors are measured using an Agilent 4294A precision impedance analyzer. The transfer curves of the LMP-based $SnO_2$ TFTs and the current density–electric field (J–E) curves of the MIM structure are measured in dark ambient conditions using a Keithley 4200 semiconductor characterization system. Here, a positive voltage sweep with a step of 0.167 V and a current compliance of 1 mA is set for the J–E measurements. Also, the breakdown is identified by an abrupt and irreversible increase in leakage current, which is immediately limited by the preset current compliance. The numerical simulations have been performed in the Silvaco TCAD ATLAS platform to elucidate the underlying physical mechanisms [17].

## III. Results and Discussion

### A. Device Characteristics of LMP-$SnO_2$ TFTs

The $SnO_2$ films fabricated by LMP on $SiO_2/p^+$-Si substrate exhibit large lateral dimensions spanning several square millimeters, with continuous surfaces free of cracks and pinholes, as depicted in Fig. 1(b). AFM images of the LMP-$SnO_2$ films on $SiO_2/p^+$-Si substrate show an ultrathin film thickness of ~4 nm and a root-mean-squared surface roughness ($R_{rms}$) of ~1.3 nm, as depicted in Fig. 1(c) and (d). This value closely matches $R_{rms}$ of the underlying $SiO_2$ (~1 nm), confirming that the film's surface morphology is predominantly governed by the underlying substrate [7]. Notably, the $R_{rms}$ and thickness of the LMP-$SnO_2$ films remain stable under different annealing temperatures, and the substrate type does not affect the printing thickness.

Generally, a post-thermal annealing needs to be carried out for optimizing the electrical performance of the LMP-based $SnO_2$ TFTs [4]. Because of the excellent thermal stability of the $SiO_2$, we first investigate the electrical evolution

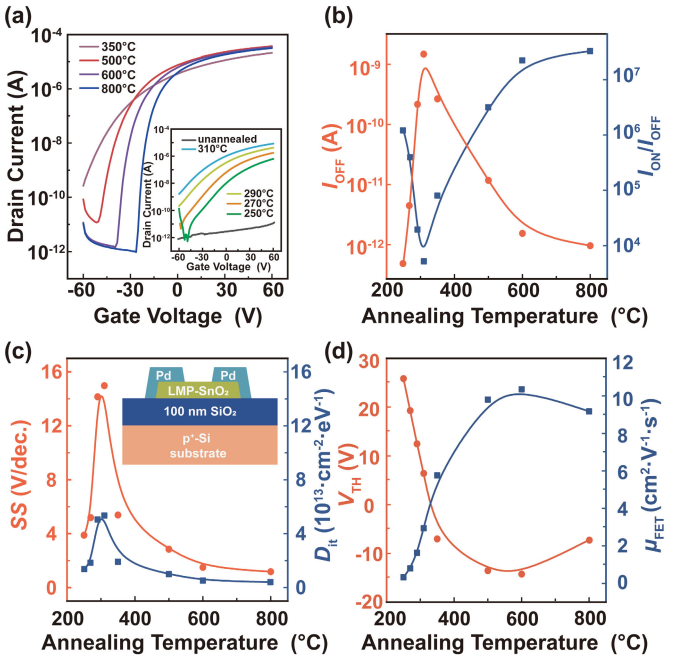


Fig. 2. (a) Transfer curves ($I_{DS}$–$V_{GS}$) of LMP-$SnO_2$ TFTs (fabricated on 100-nm $SiO_2$/p$^+$-Si substrate) at various annealing temperatures ($V_{DS}$ = 1 V). (b) $I_{ON}/I_{OFF}$ (blue) and $I_{OFF}$ (red). (c) $D_{it}$ (blue) and SS (red). Inset: schematic of the LMP-$SnO_2$ TFTs. (d) $\mu_{FET}$ (blue) and $V_{TH}$ (red) as a function of annealing temperature.

of $SnO_2$ TFTs printed on an industrially produced 100-nm $SiO_2$/p$^+$-Si substrate [designated as LMP-$SnO_2$ TFTs, schematic structure is shown in the inset of Fig. 2(c)] and clarify the impact of the post-thermal annealing on material properties and defects. Fig. 2(a) presents the transfer curves ($I_{DS}$–$V_{GS}$ measured at $V_{DS}$ = 1.0 V) of LMP-$SnO_2$ TFTs under various annealing temperatures ranging from 250 °C to 800 °C. Hence, Fig. 2(b)–(d) summarizes their key electrical parameters, including the OFF-state current ($I_{OFF}$), ON-OFF current ratio ($I_{ON}/I_{OFF}$), threshold voltage ($V_{TH}$), linear field-effect mobility ($\mu_{FET}$), density of interface defect states ($D_{it}$), and subthreshold swing (SS). Given the ultrathin (~4 nm) $SnO_2$ channel layer, the depletion capacitance can be neglected in device analysis [9], [18]. Therefore, $D_{it}$ can be estimated from the extracted $SS$ values, based on the expression of $SS = (\log_e 10 \cdot k_B T)/q \cdot [1 + q(D_{it})/C_{ox}]$, where $q$ is the elementary charge, $k_B$ is Boltzmann's constant, $T$ is temperature, and $C_{ox}$ is the gate oxide capacitance density (34.5 nF·cm$^{-2}$ for 100-nm $SiO_2$) [19]. Moreover, the $\mu_{FET}$ is calculated by the expression of $\mu_{FET} = (\partial I_{DS}/\partial V_{GS}) \cdot [(W/L) \cdot C_{ox} \cdot V_{DS}]^{-1}$ at $V_{DS}$ = 1 V. As shown in Fig. 2(a), the LMP-$SnO_2$ TFTs without annealing exhibit weak n-type characteristics due to the low printing temperature (240 °C), where incomplete oxidation of Sn metal at the liquid-metal surface resulted in a mixed $Sn^{2+}/Sn^{4+}$ phase with low free electron concentration and poor conductivity [12]. By implementing the post-annealing treatment, the device performances significantly enhance, presenting as two distinct stages with increased temperature. As depicted in Fig. 2(a)–(d), in the first stage (Stage I-annealing temperature < 310 °C), the LMP-$SnO_2$ TFTs cannot be completely turned off, even at a large bias of $V_{GS}$ = −50 V. Concurrently, the $I_{ON}/I_{OFF}$ ratio decreases from $1.19 \times 10^6$ (at 250 °C) to $5.17 \times 10^3$ (at 310 °C), while SS increases from 3.89 to 14.97 V/dec. Although $\mu_{FET}$ increases slightly, the overall performance declines. In the second stage (Stage II-annealing temperature > 310 °C), the TFT performance is progressively improving. $I_{ON}/I_{OFF}$ ratio increases substantially from $5.17 \times 10^3$ (at 310 °C) to $3.28 \times 10^7$ (at 800 °C), and $SS$ decreases from 14.97 to 1.17 V/dec. Here, $\mu_{FET}$ continuously increases with annealing temperature and achieves the maximum value of 10.35 cm$^2$·V$^{-1}$·s$^{-1}$ at 600 °C. Still increasing temperature up to 800 °C, $\mu_{FET}$ slightly degrades, due to the formation of the amorphous $SnO_2$ phase, which enhances carrier scattering [20], as confirmed by the absence of characteristic peaks for any phases in the GIXRD pattern at 800 °C, as depicted in Fig. 3(c). Consequently, optimal performance of the LMP-$SnO_2$ TFT is achieved after a 600 °C post-annealing, yielding $\mu_{FET}$ of 10.35 cm$^2$·V$^{-1}$·s$^{-1}$, SS of 1.50 V/dec, $V_{TH}$ of −14.20 V, and $I_{ON}/I_{OFF}$ of $2.23 \times 10^7$.

## B. Defect Analysis and Simulation

To elucidate the physical insights and mechanisms underlying the two-stage electrical evolution with annealing, we perform a systematic analysis by combining Silvaco ATLAS simulations and XPS characterizations. Here, the bulk defect states within the $SnO_2$ bandgap comprise three primary components: an acceptor-like tail state near the conduction band minimum (CBM), a donor-like Gaussian state, and an acceptor-like Gaussian state [21], [22]. Among these defect states, donor-like Gaussian states ($g_{GD}$) exert the most significant influence on the electrical behavior of the $SnO_2$ TFTs under the external biasing, because of the trap energy level residing near the Fermi level ($E_F$) [23], [24]. Furthermore, $g_{GD}$ is mainly attributed to oxygen vacancies ($V_O$) within the material [25]. To track their evolution, O 1s XPS spectra of the LMP-$SnO_2$ films annealed at various temperatures are depicted in Fig. 3(a). Here, the O 1s peak is fit into metal–oxygen bonds (M–O, 530.8 eV) and oxygen vacancies ($V_O$, 532.5 eV) [26]. Notably, no significant hydroxyl group peak is observed and is therefore excluded. In Stage I of the post-annealing (< 310 °C), the $V_O$ concentration increases from 33% (at 270 °C) to 50% (at 310 °C), which stems from the competition between the generation of oxygen vacancies and oxidation in tin oxides. As the film crystallizes, the adsorbed oxygen species ($O^-$ and $O^{2-}$) are desorbed, releasing trapped electrons and increasing $V_O$ concentration [27]. However, within this temperature range, the rate of oxygen penetration from ambient to fill vacancies is slower than the vacancy generation rate, resulting in a net increase of $V_O$ [28]. In Stage II (> 310 °C), the oxygen penetration rate increases, leading to a reduced $V_O$ concentration of 28% at 600 °C. Moreover, the Sn 3d spectra of the LMP-$SnO_2$ film [Fig. 3(b)] show consistent Sn $3d_{5/2}$ and Sn $3d_{3/2}$ peaks binding energies at 486.8 and 495.3 eV under all annealing temperatures, respectively [26]. This stability confirms complete oxidation of Sn to the $Sn^{4+}$ state.

Subsequently, we incorporate the evolution of $V_O$ defects into the simulation to analyze their specific impact on device electrical characteristics. Fig. 3(d) compares the simulated and

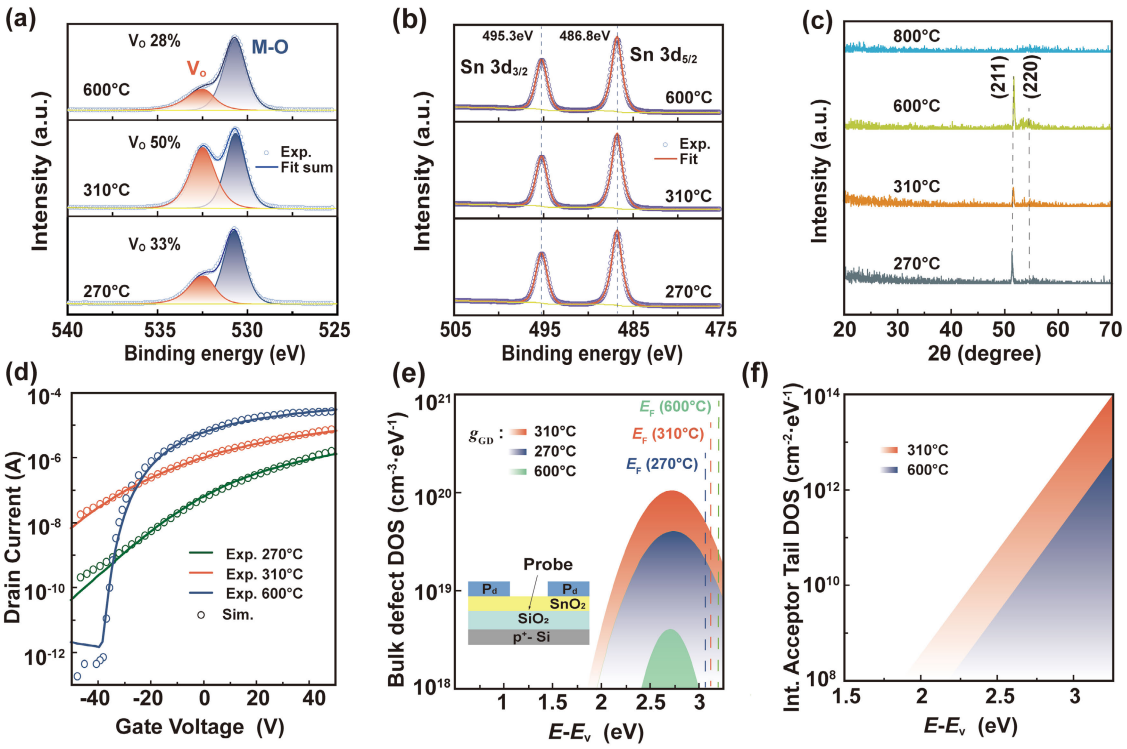


Fig. 3. XPS spectra of O 1s (a) and Sn 3d (b) obtained from the LMP-$SnO_2$ films at different annealing temperatures. (c) GIXRD patterns of the LMP-$SnO_2$ films at different annealing temperatures. (d) Simulated and experimental transfer curves ($I_{DS}$–$V_{GS}$) of LMP-$SnO_2$ TFTs at annealing temperatures of 270 °C, 310 °C, and 600 °C ($V_{DS}$ = 1 V). (e) Bulk subbandgap defect states in $SnO_2$, and $E_F$ under zero $V_{GS}$ at different annealing temperatures. Inset: probe position of $E_F$ in simulation. (f) Interface defect states at the $SnO_2$/insulator interface.

experimental transfer curves at three key temperatures (270 °C, 310 °C, and 600 °C), where 600 °C is selected as the representative high-temperature point based on the overall trend consistency. Here, the simulated $SnO_2$ TFTs were constructed with the same structure and dimensions as the experimental devices. The $p^+$-Si gate was assigned a work function of 5.13 eV, and the $SiO_2$ gate dielectric was modeled with a permittivity of 3.9. The $SnO_2$ channel was defined with a bandgap of 3.26 eV, an electron affinity of 4.5 eV, and electron and hole density of states at 300 K of $3.51 \times 10^{18}$ $cm^{-3}$ and $1.13 \times 10^{19}$ $cm^{-3}$, respectively [21]. Simulation results reveal that $N_{GD}$ (the total density of states of $g_{GD}$) should increase from $4.0 \times 10^{19}$ $cm^{-3} \cdot eV^{-1}$ (at 270 °C) to $1.1 \times 10^{20}$ $cm^{-3} \cdot eV^{-1}$ (at 310 °C) as shown in Fig. 3(e). Here, the increased donor defects inject additional electrons into $SnO_2$ material, shifting $E_F$ closer to the CBM (as shown in Fig. 3(e), the inset depicts the probe position of $E_F$), which increases the ON-state current and decreases $V_{TH}$. However, because the peak of $g_{GD}$ lies near $E_F$ ($E_{GD}$ = 2.73 eV), the increased donor-like defect states impede the shift of $E_F$ toward the valence band maximum (VBM) under negative gate bias, resulting in higher $I_{OFF}$ in the TFTs. In contrast, between 310 °C and 600 °C, the reduction in $N_{GD}$ (from $1.1 \times 10^{20}$ $cm^{-3} \cdot eV^{-1}$ at 310 °C to $4.0 \times 10^{18}$ $cm^{-3} \cdot$ $eV^{-1}$ at 600 °C) facilitates $E_F$ shift toward the VBM under negative gate bias, significantly lowering $I_{OFF}$. However, the decreased donor-like Gaussian states also reduce the ON-state current, which is opposite to the experimental observations. Therefore, the variation in interface defect states is further considered. As indicated by the GIXRD results in Fig. 3(c), the intensity of the (211) and (220) peaks increases at 600 °C, demonstrating enhanced crystallinity of the LMP-$SnO_2$ film. This improvement reduces the density of interface defect states, which aligns with the extracted $D_{it}$ shown in Fig. 2(c). Here, since the interface donor-like defect states are located close to the valence band, they exhibit negligible influence on device characteristics. Therefore, the acceptor-like interface states dominate the interface defects, and their density is expected to correspond to the *SS*-extracted $D_{it}$ value. The densities of acceptor-like interface tail states and donor-like Gaussian bulk states are iteratively adjusted to fit the experimental $I_{DS}$–$V_{GS}$ curves. Finally, the derived acceptor-like interface defect states density decreases from $1.1 \times 10^{14}$ $cm^{-2} \cdot eV^{-1}$ at 310 °C to $5.0 \times 10^{12}$ $cm^{-2} \cdot eV^{-1}$ at 600 °C, as depicted in Fig. 3(f). This reduction allows the Fermi level $E_F$ to move closer to the CBM, further enhancing $I_{ON}$. Therefore, the performance improvement observed in Stage II is primarily attributed to two factors: 1) the reduction in oxygen vacancy ($V_O$) concentration (associated with $N_{GD}$ reduction); and 2) the reduction in the density of interface defect states $D_{it}$.

### C. Device Characteristics of FLMP-$Al_2O_3$/$SnO_2$ TFTs

Fig. 4(a) presents the top-view optical micrograph of the FLMP-$Al_2O_3$/$SnO_2$ TFTs, and the inset depicts a schematic of the bottom-gate staggered device. Here, both the $Al_2O_3$ gate dielectric and the $SnO_2$ channel layer are fabricated using the LMP technique. The LMP-$Al_2O_3$ films on the $SiO_2$ adhesion layer exhibit large lateral dimensions with continuous surfaces free of pinholes, and AFM analysis further confirms a uniform

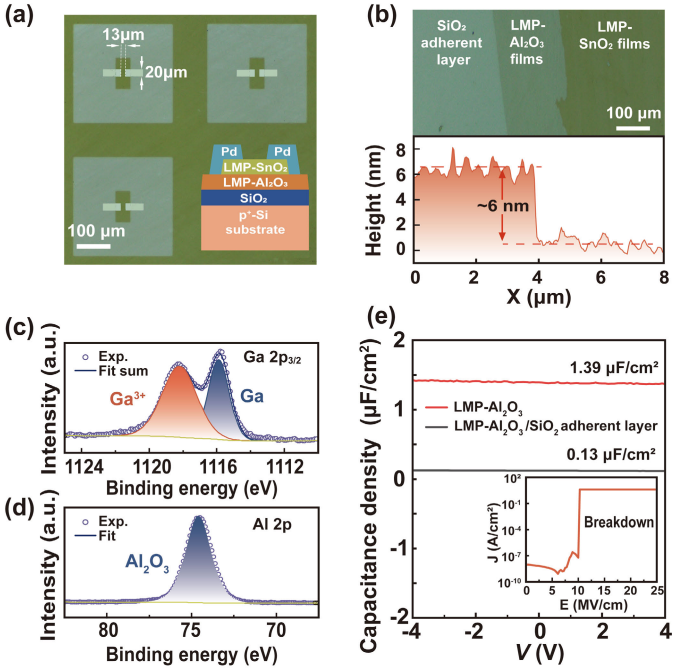


Fig. 4. (a) Top-view optical micrograph of the FLMP-$Al_2O_3$/$SnO_2$ TFT. Inset: schematic of the FLMP-$Al_2O_3$/$SnO_2$ TFT. (b) Surface optical microscopy image of LMP-$SnO_2$ and LMP-$Al_2O_3$ films on $SiO_2$ adherent layer (top) and the step height profile of LMP-$Al_2O_3$ film (bottom). XPS spectra of (c) Ga $2p_{3/2}$ and (d) Al 2p obtained from the LMP-$Al_2O_3$ films. (e) $C-V$ curves of LMP-$Al_2O_3$ and LMP-$Al_2O_3$/$SiO_2$ dielectric layers at 10 kHz. Inset: J–E curve of the LMP-$Al_2O_3$ MIM structure.

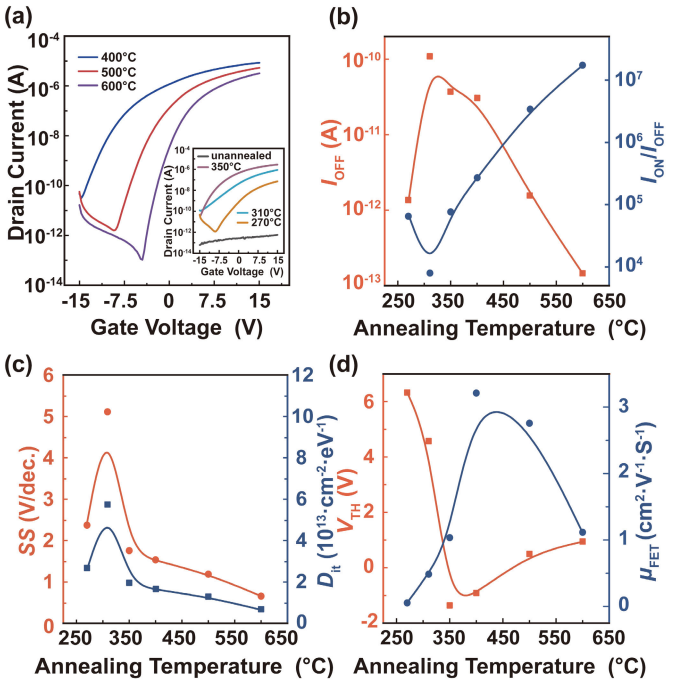


Fig. 5. (a) Transfer curves of FLMP-$Al_2O_3$/$SnO_2$ TFTs at various annealing temperatures ($V_{DS}$ = 1 V). (b) $I_{ON}/I_{OFF}$ (blue) and $I_{OFF}$ (red). (c) $D_{it}$ (blue) and $SS$ (red). (d) $\mu_{FET}$ (blue) and $V_{TH}$ (red) as a function of annealing temperatures.

film thickness of ~6 nm, as shown in Fig. 4(b). Notably, a small amount of Ga can still diffuse into the LMP-$Al_2O_3$ film and partially oxidize. As shown in the Ga $2p_{3/2}$ spectra of the LMP-$Al_2O_3$ film [Fig. 4(c)], two components are observed at 1118.0 eV ($Ga^3$) and 1115.9 eV ($Ga^0$) [16], with relative concentrations of 60% and 40%, respectively. Meanwhile, the Al 2p spectrum exhibits a peak at 74.6 eV [Fig. 4(d)], confirming that Al exists mainly in the form of $Al_2O_3$ [29]. Most importantly, the total Ga concentration in the film is only about 4.5% of the total (Ga + Al) atomic content, calculated from the sensitivity factor corrected area of the Ga 2p and Al 2p peaks. Moreover, the MIM structure is also fabricated to evaluate the insulating properties using capacitance–voltage ($C-V$) measurements. The calculated LMP-$Al_2O_3$ capacitance density is 1.39 $\mu$F/cm$^2$, corresponding to an equivalent oxide thickness (EOT) of 2.48 nm and a high dielectric constant ($k$) of 9.42 [Fig. 4(e)]. Meanwhile, as shown in the inset of Fig. 4(e), the J–E curve reveals that the 6-nm-thick LMP-$Al_2O_3$ dielectric exhibits a low leakage current density of $10^{-8}$–$10^{-9}$ A/cm$^2$ and a high breakdown electric field of ~10 MV/cm. These values are comparable to or exceed those of conventional $Al_2O_3$ films deposited by atomic layer deposition (ALD) [30], [31]. Moreover, the total capacitance density of LMP-$Al_2O_3$ film with $SiO_2$ adhesion layer is 0.13 $\mu$F/cm$^2$.

Fig. 5(a) presents the transfer curves ($I_{DS}$–$V_{GS}$) of the FLMP-$Al_2O_3$/$SnO_2$ TFTs under various annealing temperatures, with extracted electrical parameters shown in Fig. 5(b)–(d). The overall annealing-dependent performance trend is similar to that of TFTs fabricated on the 100-nm-thick $SiO_2$/$p^+$-Si substrates, including the stage transition temperature at 310 °C. However, the FLMP-$Al_2O_3$/$SnO_2$ TFTs exhibit lower field-effect mobility. This is mainly attributed to a decreased film quality resulting from sequential LMP steps. Furthermore, the onset temperature for $\mu_{FET}$ degradation is lower (~400 °C) in the FLMP-$Al_2O_3$/$SnO_2$ TFTs, potentially arising from crystallization phase changes within the $Al_2O_3$ dielectric itself at high annealing temperatures [32]. However, the overall trend evolution remains attributable to changes in $V_O$ concentration and the density of interface defect states ($D_{it}$). Optimal device performance is achieved after annealing at 600 °C, yielding a $\mu_{FET}$ of 1.12 cm$^2$·V$^{-1}$·s$^{-1}$, a $V_{TH}$ of 0.95 V, an $SS$ of 654 mV/dec, and an $I_{ON}/I_{OFF}$ ratio of $1.73 \times 10^7$. Here, device performance is expected to improve significantly with process refinement, particularly by replacing manual transfer with mechanized transfer techniques and eliminating the adhesion layer through alternative methods.

### D. Application of FLMP-$Al_2O_3$/$SnO_2$ TFTs

Finally, a zero-$V_{GS}$-load nMOS inverter comprising the depletion-mode (D-mode) and enhancement-mode (E-mode) TFTs is constructed, as the circuit schematic is shown in the inset of Fig. 6(a). The D-mode and E-mode operation in TFTs can be achieved by modulating the annealing temperature. Here, the RPI Poly-Si TFT model is leveraged [33], based on the electrical parameters extracted from FLMP-$Al_2O_3$/$SnO_2$ TFTs annealed at 350 °C and 600 °C. The device annealed at 600 °C functions as an E-mode TFT, exhibiting $V_{TH}$ of 0.95 V, $\mu_{FET}$ of 1.12 cm$^2$·V$^{-1}$·s$^{-1}$, and an $SS$ of 654 mV/dec. In contrast, the device annealed at 350 °C functions as a D-mode TFT, which shows a $V_{TH}$ of–1.36 V, a $\mu_{FET}$ of

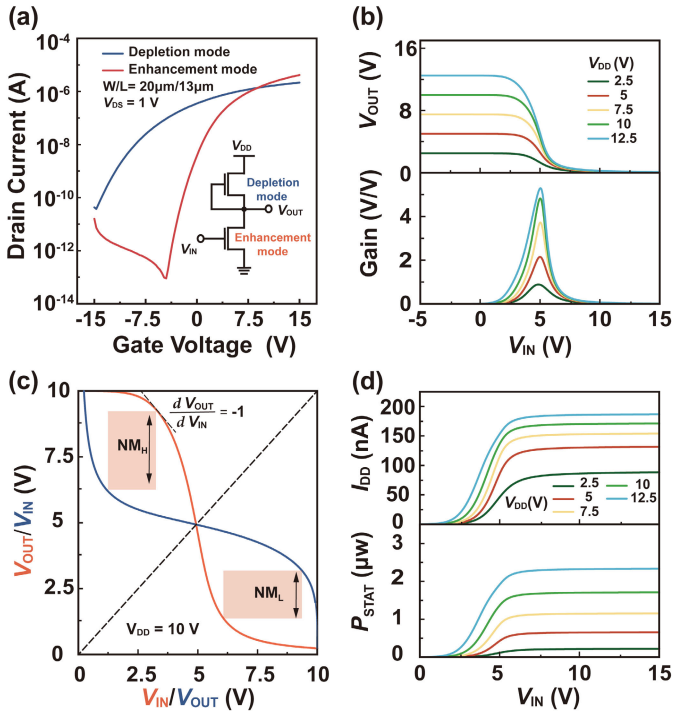


Fig. 6. (a) Experimental transfer curves ($I_{DS}$–$V_{GS}$) of the D and E-mode FLMP-$Al_2O_3$/$SnO_2$ TFTs at $V_{DS}$ = 1 V for zero-$V_{GS}$-load nMOS inverter. Inset: circuit schematic. (b) VTC curves (top) and the voltage gain (bottom) with $V_{DD}$ of 2.5–12.5 V. (c) Noise margin evaluation at $V_{DD}$ = 10 V. (d) $I_{DD}$ (top) and $P_{STAT}$ (bottom) curves with $V_{DD}$ of 2.5–12.5 V.

1.04 $cm^2 \cdot V^{-1} \cdot s^{-1}$, and an *SS* of 1.72 V/dec. The corresponding transfer curves are presented in Fig. 6(a). Fig. 6(b) displays the representative voltage transfer characteristics (VTCs) with clear logic transitions under a supply voltage ($V_{DD}$) range of 2.5–12.5 V, which confirms the standard nMOS inverter operation. A voltage gain of 5.29 is achieved at $V_{DD}$ = 12.5 V. Noise margins, defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$ [7], reach 64% and 41% of $V_{DD}/2$ at a $V_{DD}$ of 10 V [Fig. 6(c)]. The static current ($I_{DD}$) and static power dissipation ($P_{STAT}$) range from 86 to 185 nA and 0.21–2.31 $\mu$W, as shown in Fig. 6(d). As a result, these performance figures demonstrate the potential viability of this LMP technology in integrated circuits applications.

## IV. Conclusion

In this work, we have developed fully liquid-metal-printed $SnO_2$ TFTs, where both the $Al_2O_3$ dielectric layer and the $SnO_2$ semiconductor channel are fabricated using the LMP process under ambient atmosphere. The electrical performance of LMP-$SnO_2$ TFTs with a standard 100-nm $SiO_2$/$p^+$-Si substrate during the annealing process exhibits a two-stage characteristic, with a transition point at 310 °C. In Stage I (<310 °C), overall device performance degrades; the $I_{ON}/I_{OFF}$ decreases by a factor of 230, while the *SS* increases by a factor of 3.85 from 250 °C to 310 °C and the TFTs cannot be completely turned off. It is primarily attributed to the increasing $V_O$ concentrations, as confirmed by XPS measurements and Silvaco simulations. Conversely, in Stage II (>310 °C), $V_O$ concentrations reduce. Simultaneously, enhanced crystallinity decreases $D_{it}$. These dual mechanisms synergistically optimize the device performance. Moreover, the $C - V$ measurements demonstrate that LMP-$Al_2O_3$ films exhibit dielectric properties comparable to ALD-deposited counterparts, with a dielectric constant of 9.42. Based on this, the fully LMP-fabricated $SnO_2$ TFTs with LMP-$Al_2O_3$ dielectrics exhibit $\mu_{FET}$ of 1.12 $cm^2 \cdot V^{-1} \cdot s^{-1}$, an *SS* of 654 mV/dec, $V_{TH}$ of 0.95 V, and an $I_{ON}/I_{OFF}$ of $10^7$ with an annealing temperature of 600 °C. Finally, a zero-$V_{GS}$-load nMOS inverter is modeled using the fully LMP-fabricated $SnO_2$ depletion and enhancement-mode TFTs, demonstrating its potential application in future integrated circuits.

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