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(Invited) Current Status and Trends in RF Silicon-on-Insulator Material and Device

Tuesday, 15 May 2018: 16:40

Room 309 (Washington State Convention Center)

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Performance of RF integrated circuit (IC) is directly linked to the analog and high frequency characteristics of the transistors, the quality of the back-end of line process as well as the electromagnetic properties of the substrate.

This last decade Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency commercial applications pushing the limits of CMOS technology. Partially depleted SOI MOSFET is now the mainstream technology adopted by all major foundries and fabless companies for the design of several wireless sub-systems. Today, more than 95 percent of substrates used in fabricating cellular and connectivity switches for handsets are SOI (from Navian market analyst, 2016 report) whereas it was not even in production in 2008, GaAs being mainstream at that time. Beside main switch, front-end module complexity has increased drastically: more than ten integrated switches are required in 4G Tier 1 phones, plus antenna tuners as well as Low Noise Amplifiers (LNA). RF-SOI Power Amplifiers (PA) market adoption is slowly ongoing being mainly position on entry market favoring price-performance-integration trade-off.

The concept of trap-rich SOI substrate proposed in 2005 is at the origin of the RF-SOI success story. Indeed, substrate losses and crosstalk were the remaining killer features of Si-based technologies for RF applications these last decades. Thanks to the introduction of a high density of defects called traps at the buried oxide (BOX) / Si handle substrate interface, it has been possible to manufacture high-resistivity (HR) SOI substrates characterized with an effective resistivity as high as 10 kΩ.cm. Those traps originate from the grain boundaries in a thin (less than 1 μm-thick) polysilicon layer. This high-resistivity characteristic, which is conserved after a full CMOS process, translates to very low RF insertion loss (< 0.15 dB/mm at 1 GHz) along coplanar waveguide (CPW) transmission lines and purely capacitive crosstalk similarly to quartz substrate. It has been shown that the presence of a trapping layer does not alter the DC or RF behavior of SOI MOS transistors. And more importantly, it has been demonstrated that harmonics level originated from the substrate is reduced by at least 20 dB moving from standard

resistivity SOI substrate ($\sim 10 \Omega\cdot\text{cm}$) to high resistivity SOI ($\sim 1 \text{ k}\Omega\cdot\text{cm}$), and an additional drop of 40 dB is achieved with the innovative trap-rich HR SOI substrate. The low harmonic level achieved is comparable with insulating substrate. The improvement of the HR SOI substrate with the introduction of defects brings also clear benefits for the integration of passives, such as the quality factor of spiral inductors, tunable MEMS (microelectromechanical systems) capacitors, as well as for the reduction of the substrate noise (crosstalk) between devices integrated on the same chip, etc. Université catholique de Louvain and Soitec have been working together to manufacture the trap-rich SOI substrate concept to further improve the high-frequency performance of commercially available HR-SOI substrates. In 2013, Soitec has unveiled a new flavor of HR-SOI called RF-eSITM-SOI, for enhanced Signal IntegrityTM substrate with a measured effective resistivity as high as $10 \text{ k}\Omega\cdot\text{cm}$. RF-eSI-SOI substrate can really be considered as a lossless Si-based substrate. Beyond switch, RF-eSI-SOI technology opens the path to further system integration in the Front-End Module (FEM) space as well as even more complex mixed signal System-on-Chip. Based on its 45 nm baseline SOI process, GlobalFoundries just released a RF-SOI mmW offering targeting applications like 5G, satellite communication, automotive radar, WiGig, backhaul. The SOI substrates roadmap for RF and millimeter-waves applications will be presented.

Future generations of mobile communication systems such as 5G or the Internet-of-Things will require transistors with better high frequency performance at lower power consumption. The advanced MOS transistors in competition are FinFET and Ultra Thin Body and Buried oxide (UTBB) SOI MOSFETs. Both devices have been intensively studied these last years. Most of the reported data concern their digital performance. Their analog/RF behavior will be described and compared in the paper. Both show pretty similar characteristics in terms of transconductance, Early voltage, voltage gain, self-heating issue but UTBB outperforms FinFET in terms of cutoff frequencies thanks to their relatively lower fringing parasitic capacitances.

The relative impact of the transistor characteristics and the substrate properties on different RF ICs performances will be presented. As it will be demonstrated, the use of specific RF test structures at the early stage of a technological node development is of first importance to analyze the transistor parasitic resistances and capacitances, the transistor cutoff frequencies, the self-heating, and the substrate coupling and non-linear behavior.

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