CHAPTER 4

PERFORMANCES OF ALTERNATIVE MOSFETS IN SOI TECHNOLOGIES

4.1 Introduction

Low power, low voltage silicon-based technologies have recently been developed to produce highly integrated mixed mode circuits for wireless applications. Historically device scaling remains the primary method by which the semiconductor industry has improved productivity and performance. From the 100 nm technology node, upcoming CMOS technologies will have to face many grand technological challenges. In this context, the most critical issue consists in the so-called short-channel effects (SCE). These parasitic effects tend to degrade the subthreshold characteristic, increase the leakage current and lead to a related dependence of the threshold voltage on channel length. They have been reported theoretically and experimentally in the literature and solutions have been proposed. Instead of working on the gate engineering by reducing the dimension of the gate, we propose and study two alternative structures, the Dynamic Threshold MOSFET (DTMOS) and the graded channel MOSFET (GCMOS). Better performances for low power DC and RF applications are obtain using these structures compared to conventional MOSFET.

In the following sections, RF figures of merit are given. And the Dynamic Threshold and Graded Channel MOSFET are studied from DC and RF point of view.

4.2 Relevant figures of merit for RF applications

This section is dedicated to the definition of several figures of merit of RF transistors. They are based on the scattering matrix parameters, and will be deduced from the expressions presented in Chapter 2. The relationship between some

interesting figures of merit and a classical equivalent circuit of a MOSFET will be established.

4.2.1 Figures of Merit of integrated transistors

Usually, the performances of RF transistors are evaluated using different definitions of gain, the ROLLET's factor, which is the condition of inherent stability, and some characteristic parameters related to the equivalent noise sources of the device. As the noise has not been studied in this work, the noise parameters will not be described.

The transducer gain (G_t) of a transistor is defined as the ratio between the power delivered to the load and the available input power (section 2.1). The transducer gain is equal to $|s_{21}^2|$ and can be deduced directly from the measurement. This gain is not a relevant figure of merit for MOSFET transistor. Indeed, the reference impedance of the measured S-parameters being usually 50Ω, the transistor is far from conjugate matching condition. Thus the transducer gain is extremely low.

The current gain, currently used at lower frequencies, is given by

$$|H_{21}| = \frac{|Y_{21}|}{|Y_{11}|} \tag{4.1}$$

with $Y_{11} = \frac{i_1}{v_1}\Big|_{v_2=0}$ and $Y_{21} = \frac{i_2}{v_1}\Big|_{v_2=0}$. It can also be expressed as a function of the scattering parameters

$$|H_{21}| = \left| \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}s_{21}} \right| \tag{4.2}$$

This current gain has some interesting properties as it is mainly independent of the extrinsic resistance of the MOSFET. But, as for the transducer gain, it imposes specific condition at the transistor accesses (A short circuit at the output). These conditions are not optimal to extract the maximum of power from the device.

The voltage gain can also be defined ($|y_{21}/y_{22}|$), but it is not often used.

A more interesting definition of gain, will be the *Gain figure* defined by BOD-

WAY in [1]. It is defined as the ratio between the forward (from gate to drain) and reverse (from drain to gate) transducer gain. And it is given by

$$GF = \frac{|s_{21}|^2}{|s_{12}|^2} \tag{4.3}$$

This definition is invariant to changes in generator and load impedances. It gives information on the ability of the device to provide power to a load. Indeed, when the device is not able to provide power, it behaves as a passive, and reciprocal, device. Thus $s_{21} = s_{12}$ and the GF is equal to 1. Unfortunately, this definition of gain does not care about the stability of the device.

The inherent stability of transistors is evaluated by the ROLLET's factor defined by

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta_s|^2}{2|s_{12}s_{21}|} \tag{4.4}$$

where $\Delta_s = s_{11}s_{22} - s_{12}s_{21}$

When $k > 1$ the device is unconditionally stable, which means that whatever the passive load impedance at an access, the real part of the input impedance at the other access will never be negative. If $k < 1$, the device is potentially unstable. That means that specific passive load impedances can make the device unstable. It is then useful to determine approximately these impedances, and to avoid to use them, in order to ensure stability.

Now that the stability factor has been defined, the maximum available gain for a stable device (MAG) can be defined.

$$MAG = \left|\frac{s_{21}}{s_{12}}\right|^2 \left(k - \sqrt{k^2 - 1}\right) \tag{4.5}$$

This relation is extremely similar to the gain figure defined above, but with the introduction of a correcting factor, related to the stability of the device. When the device is unstable, this gain does not exist, because $k < 1$.

Another definition has been proposed by MASON in [2]. The unilateral gain (ULG) is the maximal available gain of a device when the stability is ensured by using a lossless feedback network to cancel the reverse transmission of the

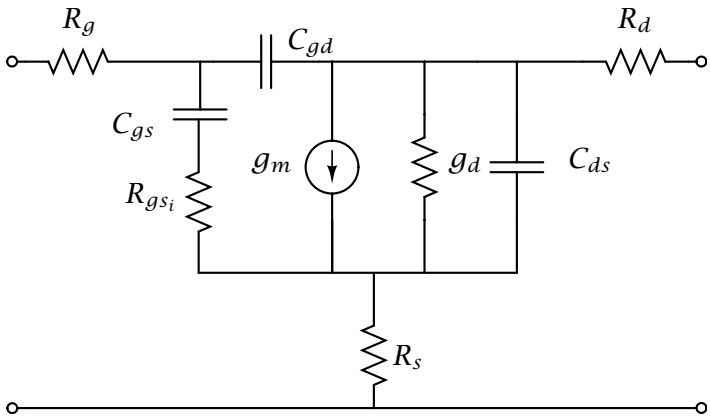


Figure 4.1: Simple small signal equivalent circuit of a MOSFET

device (s_{12}). This gain is defined by

$$ULG = \frac{\frac{1}{2}\left|\frac{s_{21}}{s_{12}} - 1\right|^2}{k\left|\frac{s_{21}}{s_{12}}\right| - \Re\left(\frac{s_{21}}{s_{12}}\right)} \tag{4.6}$$

It can be calculated for any devices, but it is extremely sensitive to the measurements noise [3].

4.2.2 Cut-off frequencies

Based on the different gains, it is possible to define several cut-off frequencies, as the frequency for which a gain becomes equal to unity or 0 dB.

The most used ones are the followings:

f_t : This is the most widely used definition of cut-off frequency. And it is defined as cut-off frequency of the current gain H_{21}. It can be approximated for a MOSFET, considering the equivalent circuit of Figure 4.1, by the following relation

$$f_t \approx \frac{g_m}{2\pi C_{gg}} \tag{4.7}$$

where C_{gg} is the total gate capacitance of a MOSFET ($C_{gg} = C_{gs} + C_{gd}$), and g_m is the transconductance. f_t is only function of the intrinsic parameters of the MOSFET. It is then an important coefficient to compare different technologies and devices. As it is nearly proportional to g_m and $1/C_{gg}$, which are proportional to the width of the transistor, f_t is nearly

not sensitive to the total width of a MOSFET.

f_c : When the equivalent circuit of the MOSFET is known, another cut-off frequency is sometimes used to described the intrinsic performances of MOSFETs. The intrinsic cut-off frequency is defined by

$$f_c = \frac{g_m}{2\pi C_{gs}} \tag{4.8}$$

The intrinsic cut-off frequency is equal to the classical cut-off frequency (f_t) when the capacitance C_{gd} is small compared to C_{gs}. It is usually not the case for deep sub-micron MOSFET [4].

f_{max} : Usually called the maximum frequency of oscillation, f_{max} is defined using the MAG or the ULG. It is the highest frequency where the device is able to provide power when it is in a stable state. As for f_t, it is possible to develop a simplified expression of f_{max} based on the equivalent circuit of Figure 4.1. SZE in [5] provides the following relation

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + g_d \left(R_g + R_s + R_{gs_i}\right)}} \tag{4.9}$$

It is important to notice that f_{max} is expressed as a function of f_t. Contrarily to f_t, f_{max} is sensitive to the width of the gate, and to all the parasitics which surround the transistor.

f_t and f_{max} are directly extracted from S-parameters measurement as the cut-off frequencies of H21 and MAG respectively. For transistor having a cut-off frequency higher than the measurement frequency band, f_t and f_{max} can be evaluated by Equations (4.7) and (4.9). The accuracy of these equations is close to 10%.

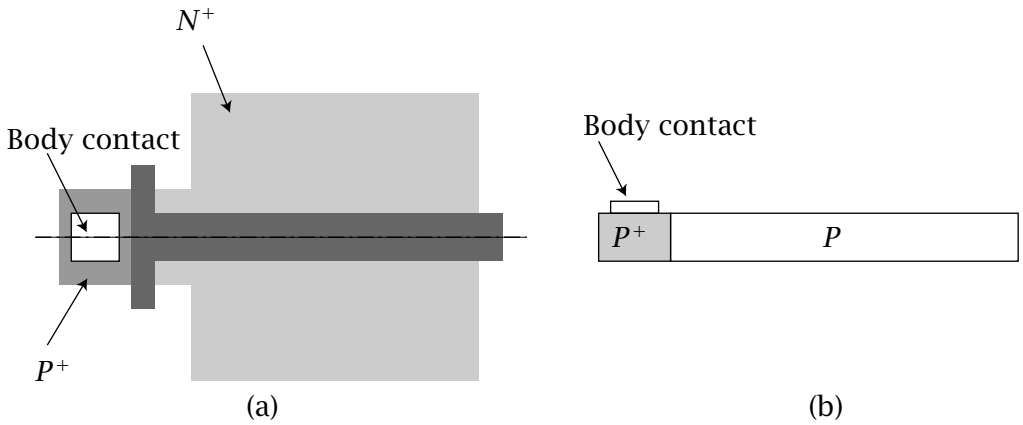


Figure 4.2: Schematic top view (a) and cross section (b) of the body contact of a DT nMOSFET

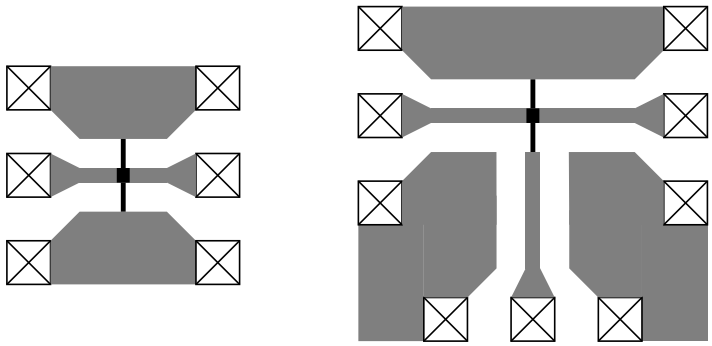
4.3 The Dynamic Threshold MOSFET

4.3.1 Introduction

Back in the eighties, a new operating mode of SOI MOSFET was proposed by COLINGE in [6]. Connecting the floating substrate to the gate in a short channel SOI MOSFET allows lateral bipolar current to be added to the MOS channel current and thereby enhances the current drive capability of the device. More recently, ASSADERAGHI [7] proposed to use that structure for Low-Voltage operation ($V_{gs} < 0.7V$), defining the Dynamic Threshold MOSFET (DTMOS). In the following sections, properties of the DTMOS will be presented, and some specific aspects of its frequency behavior will be explained.

4.3.2 Device fabrication

DTMOS are fabricated using standard SOI PD CMOS processes. The floating body of the SOI MOSFET is connected to the gate using a P^+-metal contact, as shown in Figure 4.2. The width of the MOSFET is optimized to ensure a good control of the body potential by the body contact. The maximum width per finger of a DTMOS is then limited. For example, one body contact was considered efficient for transistor width smaller than 3.3 μm in the PD technology that we use for our experiment. This technique does not require any additional step to a classical SOI PD process, as it is the technique used to avoid the kink effect



(a) (b)

Figure 4.3: Measured structure of MOSFET and DTMOS (a) and 3-ports (b)

of the PD MOSFETs, connecting the floating body to the source, or any other potential reference.

DTMOS with a gate length of 0.25 μm and 3.3 μm per fingers were fabricated using a conventional SOI PD process using a moderate and a high resistivity silicon substrate. The gate oxide, the active film, the buried oxide and the silicon substrate have thicknesses of 5 nm, 100 nm, 400 nm, and 330 μm respectively.

For comparison purposes, two other transistor were fabricated. The first one, called 3-ports, is similar to the DTMOS, but the body contact is connected to an external terminal. The second one is a body-tied to the source MOSFET, the body contact is connected to the source of the transistor.

Figure 4.3 shows an artistic view of the different transistors embedded in CPW structures.

4.3.3 DC characteristics

In DTMOS operation, the transistor body is connected to the gate of the MOSFET, and the condition $V_{gs} = V_{bs}$ is constantly applied. This condition is applied to the classical definition of the threshold voltage, to define the threshold voltage of the DTMOS.

The threshold voltage of a MOSFET is given by

$$V_{th} = 2\Phi_f + V_{fb} + \gamma\sqrt{2\Phi_f - V_{bs}} \tag{4.10}$$

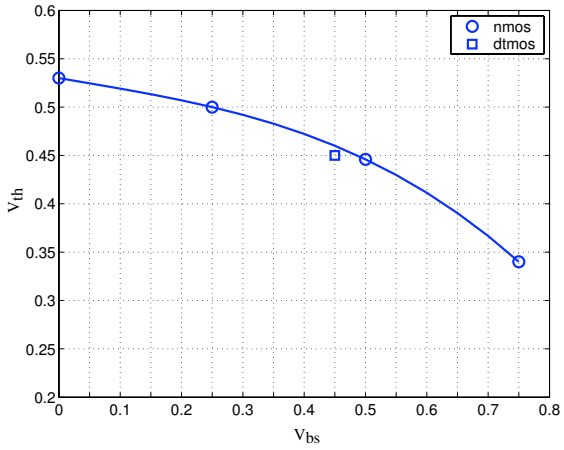


Figure 4.4: Threshold voltage of a MOSFET as a function of the body-source forward bias.

where Φ_f is the Fermi potential, V_{fb} is the flat-band voltage and V_{bs} is the body to source potential.

In a DTMOS, any change of the gate potential will induce a variation of the body potential, changing dynamically the threshold voltage [8].

When the threshold is reached, $V_{gs} = V_{th} = V_{bs}$. Substituting V_{th} to V_{bs} in equation (4.10) yields

$$V_{th} = V_{fb} + 2\Phi_f - \frac{\gamma^2}{2}\left(1 - \sqrt{1 - \frac{4V_{fb}}{\gamma^2}}\right) \tag{4.11}$$

The threshold voltage is then lower than the threshold voltage of a conventional MOSFET having the same technological parameters [9].

Figure 4.4 shows the evolution of the threshold voltage of the 3-ports as a function of the body potential, and the threshold voltage of the DTMOS. The extracted threshold voltage of the DTMOS was nearly $100mV$ lower than the threshold voltage of a similar MOSFET having its body tied to the source ($V_{bs} = 0\ V$).

The lower threshold voltage of the DTMOS does not come at the expense of an increase of off-state leakage current because at $V_{gs} = V_{bs} = 0$ DTMOS and standard body-tied device have the same effective threshold voltage. In fact, at that bias point, they are both identical and present the same leakage current. Due to the dynamic reduction of its threshold voltage, the DTMOS exhibits nearly an ideal subthreshold swing. Figure 4.5 shows the subthreshold

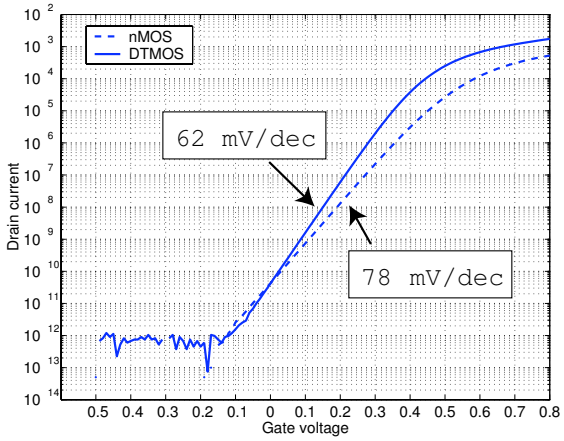


Figure 4.5: Comparison of the subthreshold swing of a DTMOS and a NMOS with gate length of $0.25\mu m$ and a total width of $40\mu m$

swing of a DTMOS and a body-tied NMOS with gate length of 0.25 μm and 12 fingers of 3.3 μm connected in parallel. The control of the body potential by the gate ensures a better control of the channel, canceling the negative influence of the body factor of the transistor, allowing us to obtain an ideal subthreshold regime.

Another important improvement of the DTMOS is obtained above threshold. Indeed, as the gate voltage of the DTMOS increases, its "effective" threshold voltage, defined using Equation (4.10), is reduced. The amount of current driven by the DTMOS is then higher than for a NMOS having the same gate voltage overdrive (GVO= $V_{gs} - V_{th}$). Figure 4.6 shows the curves of drain currents versus drain voltages for a DTMOS and NMOS having the same dimensions. The gate voltage applied to the DTMOS is close to 0.75 Volts, which was the limit before the body to source junction begins to conduct a significant current. As shown, a gate voltage of nearly $1V$ was necessary for the body-tied MOSFET to have the same output current.

The dynamic modulation of the threshold has also a strong influence on the transconductance deduced from the $I_{ds} - V_{gs}$ curves. Indeed, the transconductance of the DTMOS is significantly higher than for a MOSFET [7][10][11]. Figure 4.7 shows the drain current and the transconductance of a DTMOS and a NMOS. The difference can be explained using the four terminal model of the MOSFET

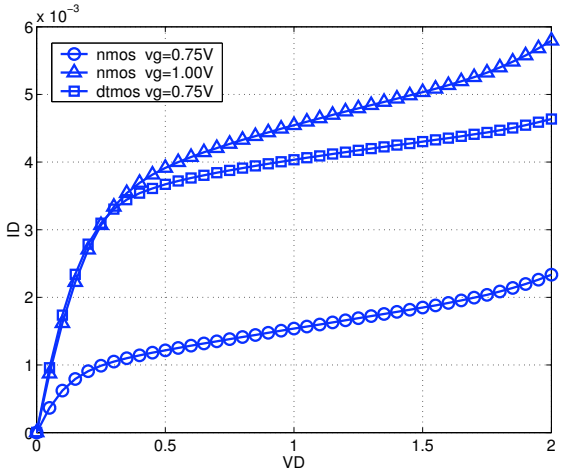


Figure 4.6: Output characteristics of a DTMOS and NMOS with gate length of $0.25\mu m$ and a total width of $40\mu m$ for different applied gate voltages

[12]. In that model, the variation of the drain current can be expressed as [13]:

$$\Delta I_{ds} \approx g_m \Delta V_{gs} + g_{mb} \Delta V_{bs} + g_d \Delta V_{ds} \tag{4.12}$$

where g_m, g_{mb} and g_d are respectively the gate to source, the body to source and the drain to source transconductance. V_{gs}, V_{bs} and V_{ds} are the voltage applied to the gate, the body and the drain. For the DTMOS, as the body and gate are connected together, the total gate/body to source transconductance will be equal to $g_m + g_{mb}$, g_{mb} being proportional to the body effect. But, this increase of the total transconductance comes at the cost of a higher input capacitance. Indeed, the total body/gate capacitance is made of the gate capacitance of a MOSFET and the depletion capacitance [14].

To increase the dynamic threshold effect, the transconductance and the current drive capability of a DTMOS, a large body effect is essential [10]. It is interesting to note that the requirements on the body effect are opposite for a DTMOS and a normal MOSFET [15].

The increase of the body potential in the DTMOS provides to this device other interesting properties. The vertical electric field is lowered, inducing a better mobility compared to similar MOSFET [16]. Moreover, the depletion region under the channel is reduced, providing for short channel DTMOS better output conductance than for MOSFET [17]. This property can be observed in Figure 4.6,

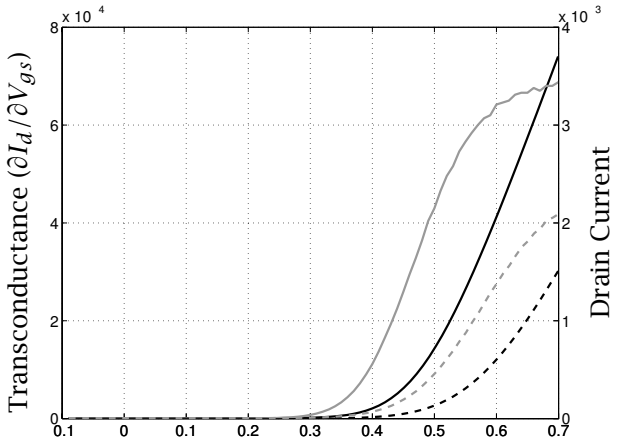


Figure 4.7: Drain current (black curves) and transconductance (grey curves) of a DTMOS (dashed lines) and a NMOS (plain lines) at $VD = 50mV$

where the drain current of NMOSFET and DTMOS are compared. Indeed even if DTMOS and MOSFET have nearly the same drain current at the beginning of the saturation region, the slope of the drain current of the DTMOS is significantly lower. EARLY voltage of 7 V was observed for the DTMOS, which was twice the value of the EARLY voltage of the MOSFET. Also, according to LEE in [18], lesser device degradation due to hot-carriers have been observed in DTMOS, thanks to the reduction of the electric field.

4.3.4 Frequency behavior

In this section, the small signal characteristics of the DTMOS will be presented. Contrary to usual field effect transistors, the DTMOS shows a strong variation of its small signal parameters at medium frequency. In fact, if the scattering parameters of the DTMOS are compared to those of a similar MOSFET, having the same cut-off frequency, the s_{21} of the DTMOS exhibits an anomalous kink in the lower part of the frequency band (Figure 4.8) [12]. For this reason, the frequency analysis of the DTMOS will be split into two paragraphs. First, the DTMOS will be analyzed for frequencies under 5 GHz, and then the higher frequency behavior will be described. In order to understand the different mechanisms responsible of the weird behavior of the DTMOS s_{21}-parameter, a MOSFET with similar dimensions, having its floating body connected to a microwave pad has been measured. This transistor called 3-ports allows to study separately the

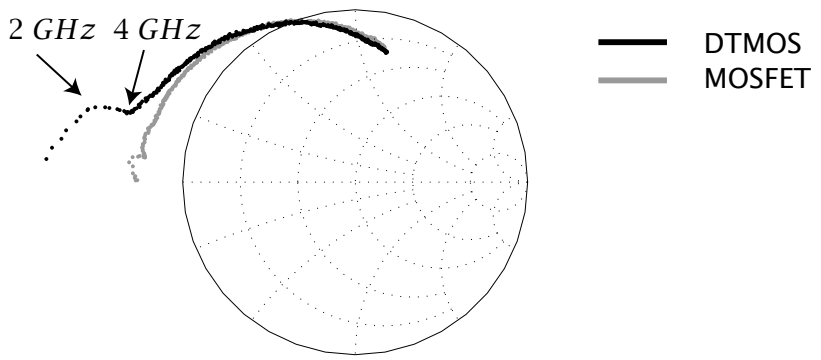


Figure 4.8: Measured s_{21} parameter of a DTMOS (black) and a MOSFET (grey) with the same bias ($V_{gs} = V_{bs} = 0.7V$, $V_{ds} = 1V$)

influence of signals coming from the gate or from the body.

4.3.4.1 Medium frequency

As presented in Figure 4.8, the parameters of the DTMOS are evolving strangely at a few GHz. In order to study this phenomenon, measurements using a low frequency VNA (100 KHz-4 GHz) have been performed in addition to the measurements made between 40MHz and 40GHz. Up to a few GHz, the use of TLR calibration is irrelevant because of the frequency limitation of the algorithm. Immitance corrections have to be used (section 2.4.2.3).

In DTMOS, the body has an important influence in the device behavior. It is then necessary to model it properly. For this purpose, a new equivalent circuit has been introduced. This equivalent circuit, shown in Figure 4.9, is based on the four terminal model of the MOSFET [13]. Because of the frequencies of interest, the non-quasi static elements are neglected. The gate and the body of the transistor are connected together through a base resistance. Contrary to the classical representation of the four terminals model, complex impedances are used to model the body to source and body to drain junctions instead of a simple capacitance.

Based on the equivalent circuit, it is possible to develop approximated expressions for the Y-parameters of the DTMOS. Considering that at low frequency, the effect of the gate, drain and source resistances are negligible, the

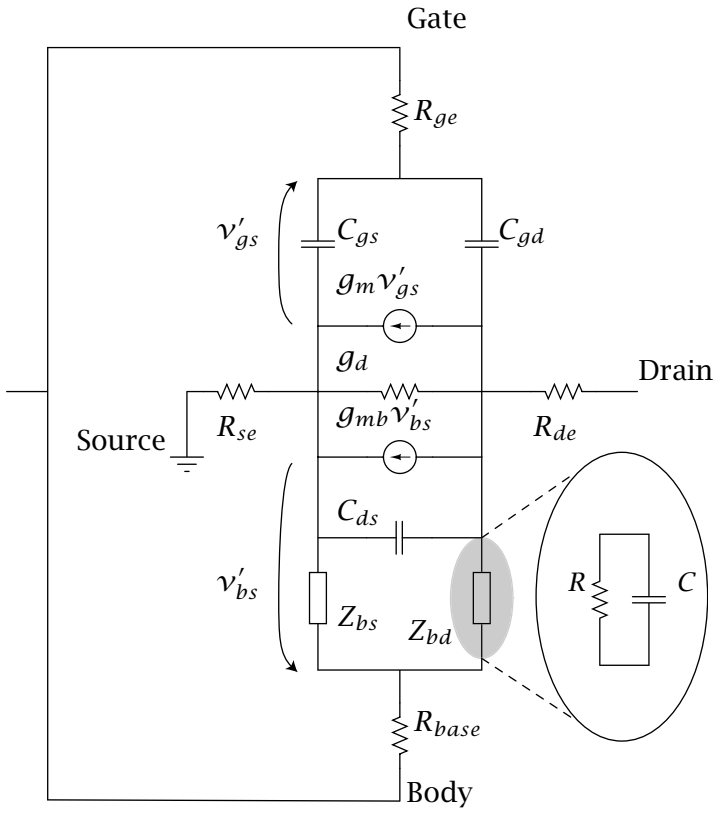


Figure 4.9: Equivalent circuit for medium frequency application of the DTMOS

following simplified expressions are obtained:

$$y_{11} = \underbrace{j\omega(C_{gs} + C_{gd})}_{y_{11_g}} + \underbrace{\left(R_{base} + \frac{Z_{bs}Z_{bd}}{Z_{bs} + Z_{bd}}\right)^{-1}}_{y_{11_b}} \tag{4.13a}$$

$$y_{12} = \underbrace{-j\omega C_{gd}}_{y_{12_g}} - \underbrace{\left(\frac{Z_{bs}}{Z_{bd}R_{base} + Z_{bs}R_{base} + Z_{bs}Z_{bd}}\right)}_{y_{12_b}} \tag{4.13b}$$

$$\begin{aligned} y_{21} = \underbrace{g_m - j\omega C_{gd}}_{y_{21_g}} &+ \underbrace{g_{mb}\left(\frac{Z_{bd}Z_{bs}}{Z_{bd}R_{base} + Zbs R_{base} + Z_{bs}Z_{bd}}\right)}_{y_{21_{b1}}} \\ &- \underbrace{\left(\frac{Z_{bs}}{Z_{bd}R_{base} + Z_{bs}R_{base} + Z_{bs}Z_{bd}}\right)}_{y_{21_{b2}}} \end{aligned} \tag{4.13c}$$

$$y_{22} = \underbrace{g_d + j\omega\left(C_{gd} + C_{ds}\right)}_{y_{22_g}} + \underbrace{g_{mb}\left(\frac{R_{base}Z_{bs}}{Z_{bd}R_{base} + Z_{bs}R_{base} + Z_{bs}Z_{bd}}\right)}_{y_{22_{b1}}} + \underbrace{\left(\frac{Z_{bs} + R_{base}}{Z_{bd}R_{base} + Z_{bs}R_{base} + Z_{bs}Z_{bd}}\right)}_{y_{22_{b2}}} \tag{4.13d}$$

where the indexes "g" and "b" indicate a contribution from the gate and from the body, respectively.

It is important to note that all the terms corresponding to the substrate contain the same polynomial expression at the denominator.

Due to the complexity of the equivalent circuit, no direct extraction procedure can be used to determine the values of the different components. In spite of the complexity, it is still possible to estimate the values of some of the elements using the analysis of other devices, as described hereafter.

In order to limit the number of unknowns, the values of the extrinsic resistance R_{ge}, R_{se} and R_{de} have been estimated by applying the inversion method, presented in section 3.3.3, to a classical MOSFET having the same physical dimension than the DTMOS. The total transconductance ($g_m + g_{mb}$) is estimated as the transconductance extracted from the DC measurements, as well as the output conductance (g_d). The value of g_m is determined by using the 3-ports with an external terminal connected to the floating body. The gate to drain

Intrinsic elements				
$g_m\ (mS)$	$g_d\ (mS)$	$C_{ds}\ (fF)$	$C_{gs}\ (fF)$	$C_{gd}\ (fF)$
15	.5	3.5	77	24

Substrate elements				
$g_{mb}\ (mS)$	$C_{Z_{bs}}\ (fF)$	$R_{Z_{bs}}\ (\Omega)$	$C_{Z_{bd}}\ (fF)$	$R_{Z_{bd}}\ (\Omega)$
5	47	7e3	9	∞

Resistances				
$R_{ge}\ (\Omega)$	$R_{de}\ (\Omega)$	$R_{se}\ (\Omega)$	$R_{base}\ (\Omega)$	
13	3	3	2.9e3	

Table 4.1: Extracted parameters of the equivalent circuit of a DTMOS with a gate length $L = 0.25\mu m$ and a total with $W = 40\mu m$ at $V_{gs} = 0.7V$ and $V_{ds} = 1V$

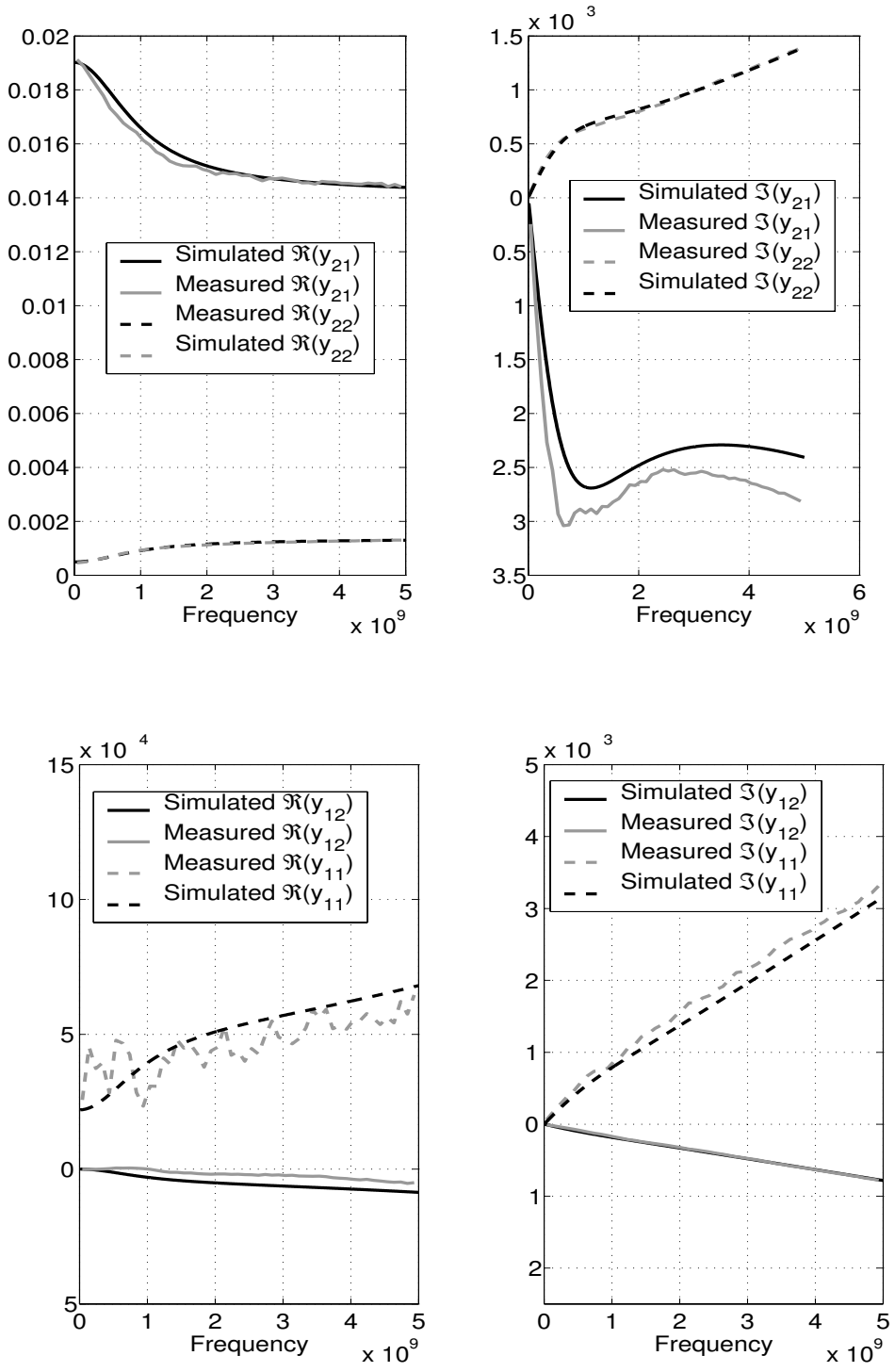


Figure 4.10: Comparison of measured y-parameters of a DTMOS, and the simulated parameters using the equivalent circuit presented in Figure 4.9

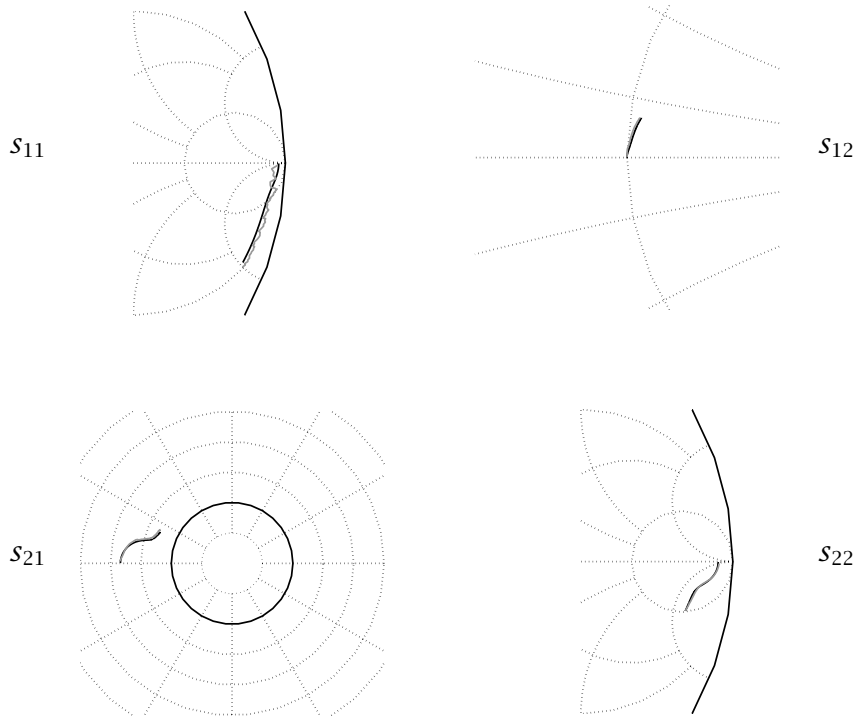


Figure 4.11: Comparison of measured and simulated s-parameters of DTMOS at $V_{gs} = 0.7\ V$ and $V_{ds} = 1\ V$

transconductance of the MOSFET is extracted, when the MOSFET has the same biased as the DTMOS. The base resistance is estimated using the base current.

The other parameters are extracted using some optimization steps. The values of the equivalent circuit element extracted from measurements are given in Table 4.1 for a DTMOS biased with a gate voltage $V_{gs} = 0.7\ V$ and a drain voltage $V_{ds} = 1\ V$. The frequency response of the equivalent circuit is compared to measurements in Figures 4.10 to 4.11. Pretty good agreement between measurements and simulations is obtained, confirming the validity of the considered equivalent circuit.

Discussion The benefits of the DTMOS reduce themselves as the frequency is increased. Indeed, the "extrinsic" output conductance, defined by $\Re\left(y_{22} + y_{12}\right)$ increases versus frequency, and the "extrinsic" transconductance, $\Re\left(y_{21} + y_{12}\right)$, decreases.

The useful effect of the DTMOS is related to the g_{mb} of the transistor. As the frequency increases, the low pass filter, composed by R_{base} and Z_{bs} begins

to stop the RF signal, avoiding it to modulate the potential of the junction (v'_{bs}). The influence of the g_{mb} vanishes when a signal comes from the gate. The "extrinsic" transconductance falls from $(g_m + g_{mb})$ to g_m.

The equivalent circuit can be used to develop simple expression to explain this phenomenon. By combining Equations (4.13c) and (4.13b) yields a simple expression of the "extrinsic" transconductance of the DTMOS, R_{bd} is neglected because the drain to body junction is reverse biased, the following equation is obtained:

$$\Re\left(y_{21} + y_{12}\right) = gm + \frac{g_{mb}}{1 + R_{base}/R_{bs}} \frac{1}{1 + \tau^2\omega^2} \tag{4.14}$$

where $\tau = (R_{base}(C_{bs} + C_{bd}))/(1 + R_{base}/R_{bs})$

The constant τ is the time constant of the input R-C network of the body, and, using the values presented in Table 4.1, it corresponds to a frequency $f_0 = 1/\tau = 1.3\ GHz$.

When the frequency increases, more RF signals from the drain modulates the potential of the body (v'_{bs}). The current source $g_{mb}v'_{bs}$ follows the signal from the drain, increasing the "extrinsic" output conductance. The simplified expression of the "extrinsic" output conductance is given by

$$\Re\left(y_{22} + y_{12}\right) = g_d + g_{mb}\frac{R_{base}^2 C_{bd}(C_{bd} + C_{bs})}{(1 + R_{base}/R_{bs})^2} \frac{\omega^2}{1 + \tau^2\omega^2} \tag{4.15}$$

The output conductance is increasing from g_d to $g_d + g_{mb}(C_{bd}/C_{bs} + C_{bd})$.

To determine accurately the transition frequency above which the dynamic modulation of the body potential is not efficient anymore, S-parameters measurements were made with VNA from RODE & SCHWARTZ (ZVR, 100 KHz-4 GHz). Figure 4.12 shows the "extrinsic" transconductance and output conductance of a DTMOS, a 3-ports, and a body-tied MOSFET fabricated on a medium resistivity substrate. In our experiment, the highest gains of the DTMOS for analog applications are obtained for frequencies below 200 MHz. At such a low frequency, the decrease of the transconductance and the increase of the output conductance are negligible.

It is important to notice that the output conductance of the body-tied MOSFET is also increasing above 200 MHz. This variation of the output conductance

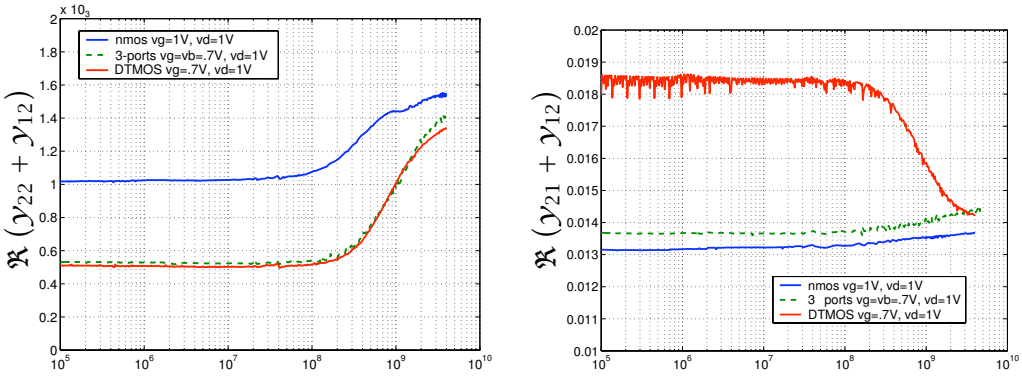


Figure 4.12: Output conductance (a) and transconductance (b) of similar MOSFET made on a medium resistivity substrate biased at $V_{gs} = 0.7\ V$ and $V_{ds} = 1\ V$

are mainly related to phenomenon occurring in the thin film of silicon, and not in the under-laying substrate. Indeed, similar variations have been observed using a high resistivity substrate. Thus, the variation of the output conductance can be related to a g_{mb} controlled by the drain through the body to drain junction.

4.3.4.2 High frequency

When the frequency becomes higher than a few GHz, the DTMOS acts similarly to a conventional MOSFET. There is no weird behavior in the parameters except a lightly higher input conductance, due to the body contact. The equivalent circuit of the DTMOS can be approximated by a classical equivalent circuit of a field effect transistor, but with an input conductance, corresponding the base resistance (R_{base}) added in parallel to the gate to source capacitance. The methods presented in Chapter 3 can be used to extract the values of the intrinsic equivalent circuit elements, the resistance being determined previously using a classical MOSFET.

Even if there is a reduction of the output transconductance of the DTMOS at high frequency, it exhibits higher performances than comparable MOSFET at the same bias. In our experiment, an increase of $250mV$ of the gate voltage was necessary for a MOSFET to reach nearly the same cut-off frequency than the DTMOS (Figure 4.13).

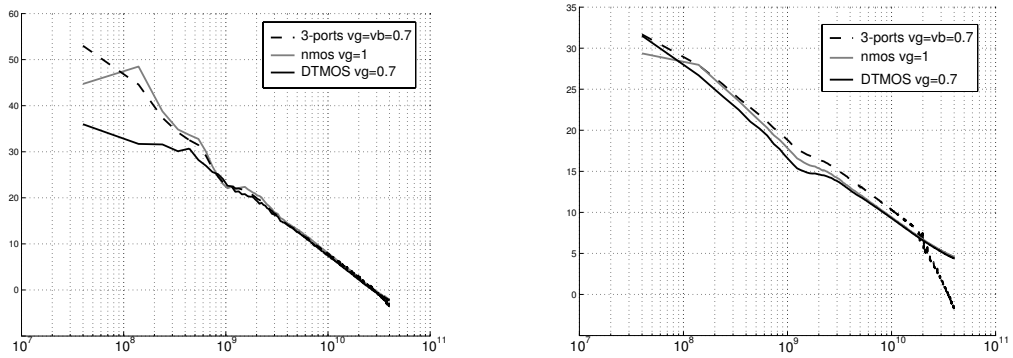


Figure 4.13: Gain current (a) and Maximum available gain (b) of a 3-ports, a DTMOS with $V_{gs} = V_{bs} = .7$ and $V_{ds} = 1$ and a MOSFET with $V_{gs} = 1V$ and $V_{ds} = 1V$ versus frequency

For deep submicron devices, some authors have shown performances of DTMOS that were unreachable for similar MOSFET [19]. In [20], HIROSE *et al.* show DTMOS with a gate length of $L = 80\ nm$ with a $f_{max} = 140\ GHz$. For such small devices, the increase of the mobility and the reduction of SCE of the DTMOS can increase significantly the performances of the devices.

Discussion At high frequency, the only benefit of the DTMOS is related to the reduction of its threshold voltage, allowing the transistor to conduct more current and having a higher transconductance than a usual MOSFET for the same bias. It has been confirmed when the different gains of a DTMOS, a MOSFET, and a 3-ports, having its body-potential controlled by a terminal, were compared (Figure 4.13). The gate, the drain and the body of the DTMOS and the 3-ports were under the same bias. The gain curves are nearly the same for these devices, and then no RF signals from the gate are influencing significantly the potential of the substrate. The difference between the MAG's at high frequency is related to the increase of parasitics for the 3-ports due to the connection of the body to a measurement pad. And the lower value of the current gain of the DTMOS at low frequency is related to the small leakage current in the body to source junction.

After extracting the equivalent circuit of the DTMOS and the 3-ports, the transconductances were compared to the values extracted from DC curves (Fig-

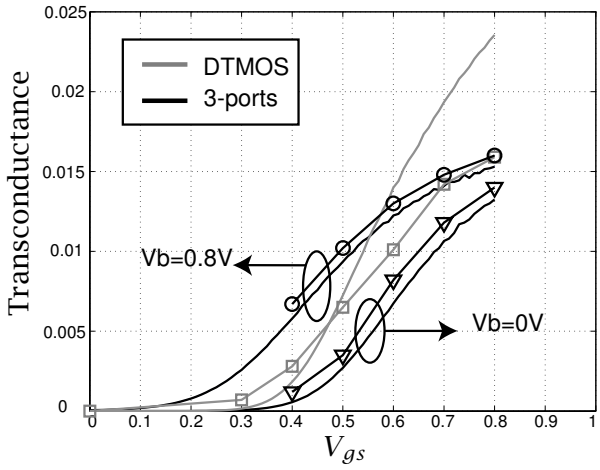


Figure 4.14: Extracted transconductance from DC (lines) and RF (symbols) of a DTMOS and a 3-ports with $V_{ds} = 1.5V$

ure 4.14). The transconductance of the DTMOS seen at high frequency is similar to the transconductance of the 3-ports, and is nearly 30% lower than its DC transconductance. These results allow to extract simply the g_{mb} of the device. Indeed, it can be considered as equal to the difference between the DC and RF transconductance.

Practically, the contact between the gate and the floating body of the DTMOS does not bring any RF advantages as only DC bias is acting through this contact. On the contrary, it introduces real impedance at the input of the transistor, and as a consequence a loss of power. Indeed, any part of the incident power that goes through this input impedance does not bring any useful effect. For RF applications, it could be clever to separate the DC and RF bias of the DTMOS, the body potential could be raised in order to reduce the threshold voltage of the DTMOS, without introducing the parasitic input impedance, but this will probably introduce more parasitic capacitance. The tradeoff between the parasitics has to be correctly evaluated.

4.3.5 Summary

Dynamic threshold MOSFET has been studied into details. The lower threshold voltage, and higher transconductance of the DTMOS compared to MOSFET have been confirmed for low frequency operation. At high frequency, we demonstrate that the benefit of the DTMOS in terms of cut-off frequencies are related to the

static reduction of its threshold voltage, and not to dynamic modulation of the transistor body. An equivalent circuit has been proposed and validated in order to model the transient its behavior from DC up to high frequencies.

Instead of connecting the body of the transistor to the gate, the body contact can be used to create original functions in a circuit using only one device. Some of them are presented in Appendix C.

4.4 The Graded Channel MOSFET

4.4.1 Introduction

Asymmetric doped channel MOSFET's have recently been investigated by several authors in bulk [21][22] and SOI technologies as a possible solution for the problems of premature drain break-down, hot carrier effects, and threshold voltage (V_{th}) roll-off issues in deep submicrometer devices. In these works, the doping of the channel region is performed by a tilted ion implantation in the source side after the gate formation. The high concentration at the source end improves the threshold voltage roll-off and drain induced barrier lowering, while the low doping near the drain ensures high mobility, reduced peak electric field and impact ionization. Recently, Pavanello *et al.* in [23] have presented a new asymmetrically doped body device, called the graded-channel SOI nMOSFET (GC) shown in Figure 4.15. The asymmetric doping profile was obtained by varying the position of the V_{th} implant along the channel, preserving the body region near the drain at natural wafer doping. The GC SOI processing is fully compatible with the conventional FD SOI MOSFET process flow, with no additional steps needed. Similar to a DMOS [24], the device can be viewed as two sub-devices connected in series: an enhancement mode device at the source side, and a depletion mode device at the drain side, each having a different V_{th} and a different "channel" length (L_{ND} and $L - L_{ND}$). The effective channel length (L_{eff}), when the device is ON, is mainly determined by the P-doped region, which is much shorter than the physical gate length. As the result, for the same physical drawn gate length, the GC device can provide higher drive current, higher peak transconductance,

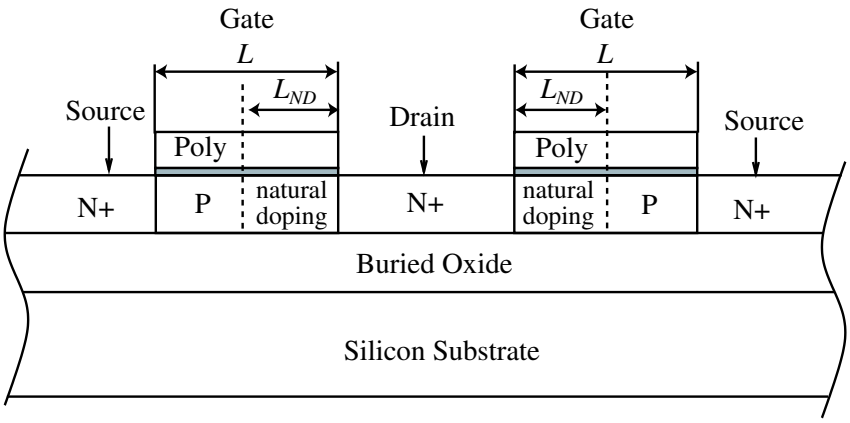


Figure 4.15: Cross-section of interdigitized GC SOI nMOSFETs

higher output resistance than a conventional CMOS device with uniformly doped channel, resulting in a high performance device with high cutoff frequency and high gain as demonstrated in the next sections.

4.4.2 Device fabrication

Graded channel nMOSFETs are fabricated using standards SOI CMOS process. A part of the channel is protected from the V_{th} implant to ensure a low doping level near the drain. The mask, which protects the pMOSFET during the V_{th} implant of the nMOSFET can be used. GCMOS can also be realized in multiple V_{th} technologies. The doping level of each part of the transistors can then be controlled accurately. Since the masks are not self aligned with the gate, the GC structure can suffer from misalignment. No additional photolithographic steps are needed to be included in the full CMOS processing.

GCMOS were fabricated according to 0.5 μm FD SOI technology, 0.5 μm FD SOS technology having multiple threshold voltages, and 0.25 μm SOI PD technology with the body tied to the source. The ratio between the length of natural doping region (L_{ND}), and the physical gate length (L) was equal to 0.5 ($L_{ND}/L = 0.5$).

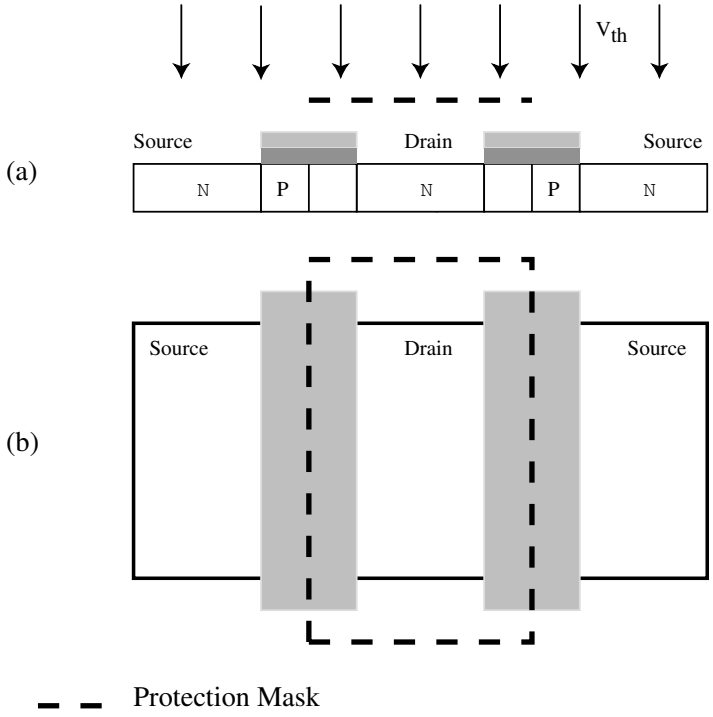


Figure 4.16: Cross section (a) and top view (b) of a GCMOS when the V_{th} implant is performed

4.4.3 DC characteristics

In this section, the DC properties of GC nMOSFET will be presented. First experimental results, that have caused our interest in that device will be presented, then a more behavioral study of this component based on 2D simulations, will be presented. From this analysis, benefits and limitations of the GC structures will be deduced.

4.4.3.1 Introduction

As presented by PAVANELLO in [23], the graded channel exhibits very interesting output characteristics compared to conventional fully depleted MOSFET. Figure 4.17 shows the output characteristics of various GCMOS with a drawn gate length of $2\mu m$ and nMOSFET with a gate length of 1 and 2 μm for a GVO ($V_{gs} - V_{th}$) set to 150 mV. Very flat characteristics are obtained for the different GC structures in saturation, inducing very high EARLY voltages and then extremely low output conductance. The length of the P-doped region has a strong

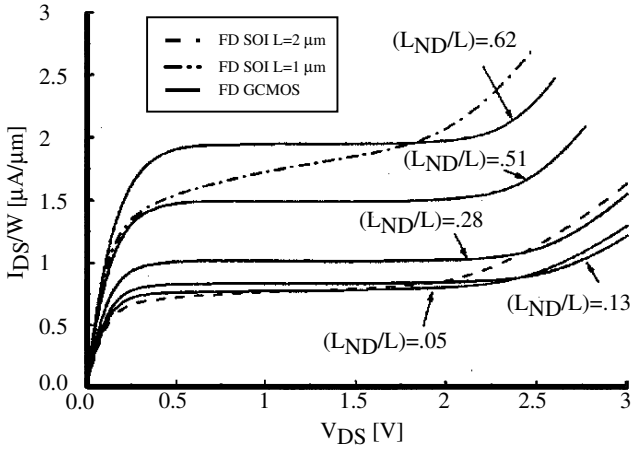


Figure 4.17: Measured I_{ds}/W vs. V_{ds} curves for GC and FD devices, as presented in [23]

influence in the current drive capability of the device. Indeed, it is mainly that region that fixes the output current of the device, defining the effective length of the device. Indeed, the 2 μmGCMOS with the L_{ND}/L ratio equal to 0.5 exhibits nearly the same saturation current as the MOSFET with a gate length of $1\mu m$ (Figure 4.17). Furthermore, the GCMOSFET exhibits higher break-down voltage than a MOSFET conducting nearly the same current.

In these measurements, the graded channel structure allows the reduction the effective channel length of the transistor, the increase of its EARLY voltage and its break-down voltage. This is the opposite of what it is obtained traditionally when the gate length is reduced.

Thus, the transconductance of the GCMOS is higher than for MOSFET with the same physical gate length, and its output conductance is lower.

In the following paragraphs, a study of GCMOS is presented, in order to determine the most important factors that influence the performances of GCMOS in dynamic regime.

4.4.3.2 Simulation Results

Numerical simulation of GC MOSFETs have been performed using the 2D Atlas simulator from SILVACO [25]. The physical gate length was set equal to 2 μm and the ratio L/L_{ND} to 0.5. Similar uniformly doped MOSFETs with gate length of 1 μm and 2 μm were also simulated. The technological parameters are sum-

	Thicknesses (nm)		Gate lengths (μm)		Regions doping levels (cm^{-3})		
	t_{si}	t_{ox}	L	L_{ND}	P-doped	ND	S/D
NMOS1	100	30	1	0	3.5×10^{16}	10^{15}	10^{20}
NMOS2	100	30	2	0	3.5×10^{16}	10^{15}	10^{20}
GCMOS	100	30	2	1	3.5×10^{16}	10^{15}	10^{20}

Table 4.2: Technological parameters used for the graded channel simulations with Atlas from Silvaco

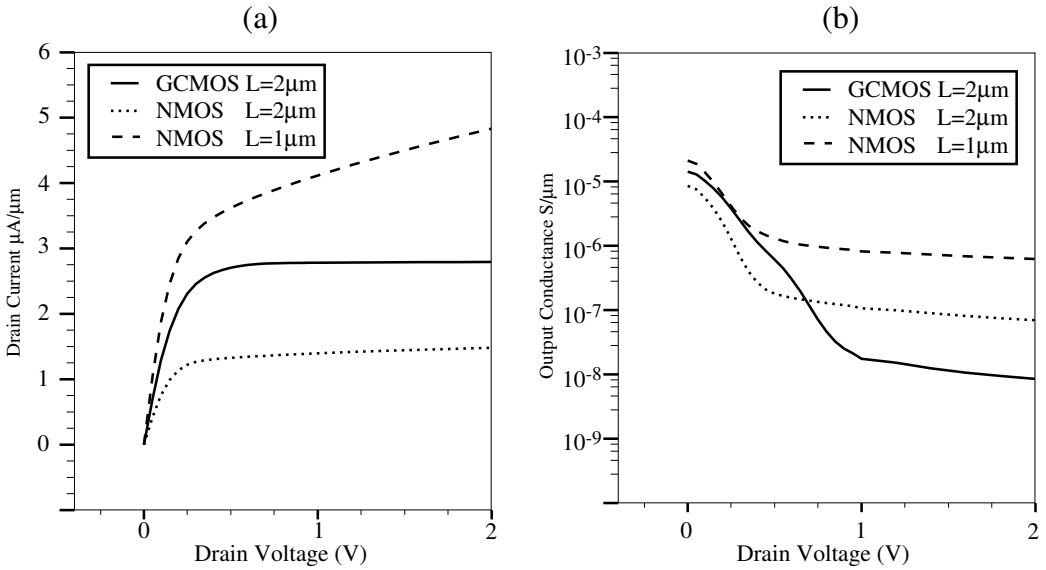


Figure 4.18: Drain current and output conductance of a $2\mu m$ GCMOS ($L/L_{ND} = 0.5$), a $1\mu m$ MOSFET, and a $2\mu m$ MOSFET under $V_{gs} = 0.6V$

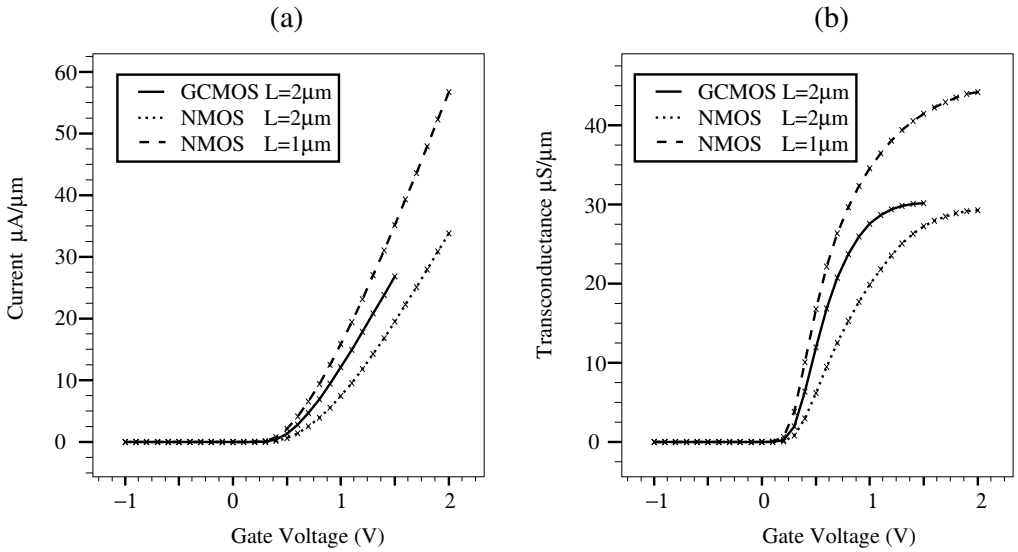


Figure 4.19: Drain current and transconductance of a $2\mu m$ GCMOS ($L/L_{ND} = 0.5$), a $1\mu m$ MOSFET, and a $2\mu m$ MOSFET under $V_{ds} = 1V$

marized in Table 4.2. Both simulated transistors have the a threshold voltage equal to 0.35 V.

The output characteristics of the transistors ($I_{ds} - V_{gs}$, $I_{ds} - V_{ds}$) and their derivative (g_m, g_d), are first analyzed. The GCMOS properties are then explained using the simulated electron concentration in the GCMOS channel. Finally, the simulated longitudinal electric field is used to explain the benefit of GCMOS in terms of break-down voltage.

Output characteristics The $I_{ds} - V_{ds}$ characteristic of the 3 transistors have been compared for various applied gate voltage. At low gate voltage overdrive ($V_{gs} - V_{th}$), the output current of the GCMOS is nearly similar to the output current of the 1 μm MOSFET, as predicted by PAVANELLO. But, when the gate voltage is raised, the output current increase of the GCMOS is lower than the one of the 1 μm-MOSFET. Then, The GCMOS output current is staying in between the 1 μm- and 2 μm-MOSFET (Figure 4.18a).

The output conductances are deduced from these simulations and shown in Figure 4.18b ($V_{gs} = 0.6\ V$). The GCMOS exhibits an extremely low output conductance, even lower than the 2 μm-MOSFET. But surprisingly, the minimum conductance is reached at a higher drain voltage than for the other transistors.

The $I_{ds} - V_{gs}$ characteristics have also been compared in order to evaluate the effect of the GCMOS structure on the transconductance of transistors. Drain current and corresponding transconductance are shown in Figure 4.19 ($V_{ds} = 1V$). As explained previously, the increase of the GCMOS drain current is lower than for the 1 μm MOSFET, but it still bigger than for the 2 μm-MOSFET. Then the transconductance of the GCMOS lies, as the output current, in between the two MOSFETs curves. It is interesting to note that the maximum transconductance of the GCMOS is similar to what it is observed for the 2 μm MOSFET, at the same applied bias.

Figure 4.20 shows the simulated transconductance versus drain current for the MOSFETs and GCMOS at $V_{ds} = 1V$, for various gate voltages ($0V < V_{gs} < 2V$). When the current is low, the GCMOS exhibits nearly the same transconductance than the 1 μm MOSFET. Their effective channel lengths are then similar. As the

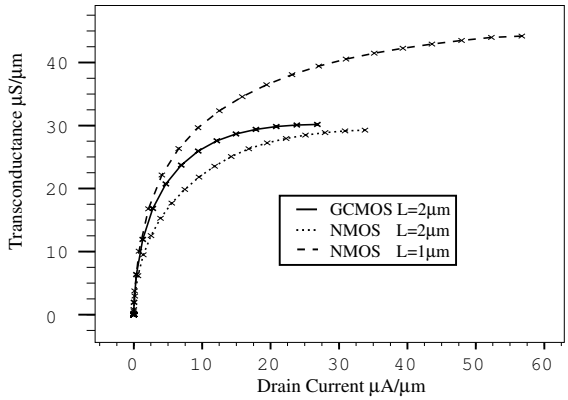


Figure 4.20: Simulated transconductance of a $1\mu m$, $2\mu m$ MOSFETs, and a $2\mu m$ MOSFET versus the total drain current for various gate voltages, and $V_{ds} = 1V$

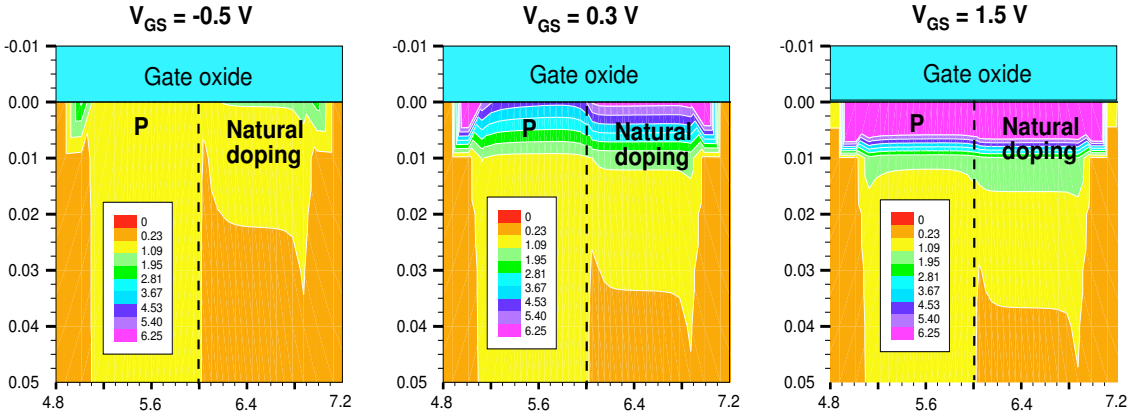


Figure 4.21: Electron concentration ($10^x/\text{cm}^3$) in the thin active silicon film for a $2\mu m$ GCMOS ($L/L_{ND} = 0.5$) at $V_{ds} = 0V$ and $V_{gs} = -0.5,\ 0.3$ and $1.5V$

current increases, corresponding to an increase of the gate voltage, the transconductance of the GCMOS becomes lower than for the 1 μm MOSFET and tends to become equal to the 2 μm MOSFET transconductance. The effective channel length of the GCMOS becomes longer as the gate voltage is increased.

Electron concentration The electron concentration under the gate has been simulated in order to explain the different properties observed in the output characteristics. Figure 4.21 shows the evolution of the electron concentration for different gate biases, at $V_{ds} = 0\ V$. Below threshold, there is no inversion layer under the gate in the P-doped region. When the threshold voltage, extracted from the $I_{ds} - V_{gs}$ curve at $V_{ds} = 0.05\ V$, is reached, an inversion layer

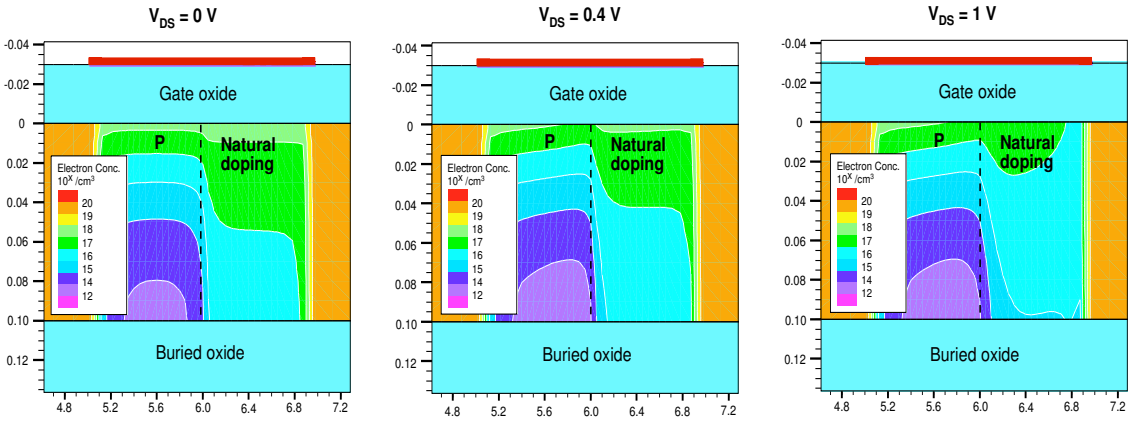


Figure 4.22: Electron concentration in the thin active silicon film for a $2\mu m$ GCMOS ($L/L_{ND} = 0.5$) at $V_{gs} = 0.6V$ and $V_{ds} = 0,\ 0.4$ and $1V$

appears under the gate in the P-doped region. A channel is already created in the ND region. Thus, the P-doped region controls the threshold voltage, and the behavior of the transistor close to the threshold. Under that bias, the ND region acts like a resistance, which connect the P-doped region to the drain. Moreover, if the gate voltage is increased further, the electron concentrations in the two part of the transistor tend to become equal, as for a conventional and uniformly doped MOSFET.

Figure 4.22 shows the simulated electron concentration for a gate voltage V_{gs} of 0.6 V and a drain voltage V_{ds} of 0 , 0.4 and 1 V. The device can be viewed as two sub-devices connected in series: an enhancement mode device at the source and a depletion mode device at the drain side. At V_{ds} of 0 V and V_{gs} = 0.6 V, the whole channel from source to drain is in inversion and the GC MOS is in linear regime. When V_{ds} is increased to 0.4 V pinchoff is appearing in the P-doped region, under that bias the output conductance exhibit a little kink, but continues to decrease as the drain voltage is increased (Figure 4.18b). Finally at $V_{ds} = 1\ V$, pinchoffs can be observed in both doped and undoped channel regions. It is under this last bias condition, when the two equivalent sub-devices for the doped and undoped regions are in saturation mode, that the output conductance of the GCMOS reaches is minimal value, as shown in Figure 4.18b, for $V_{ds} = 1\ V$. The electron concentration in the P-doped region is nearly the same than at $V_{ds} = 0.4\ V$. The current is kept nearly constant, thus

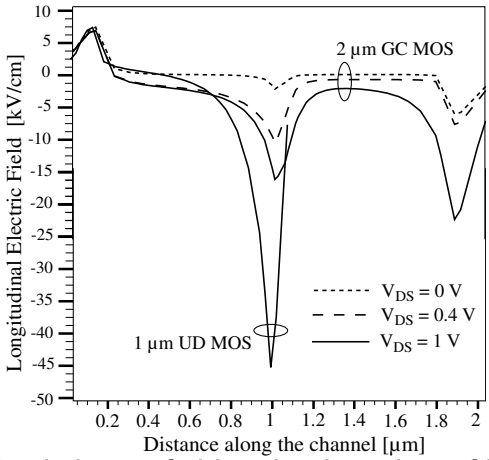


Figure 4.23: Longitudinal electric field in the thin silicon film for a $2\mu m$ GCMOS ($L/L_{ND} = 0.5$) ans $1\mu m$ MOSFET under $V_{gs} = 0.6V$ and $V_{ds} = 0,\ 0.4$ and $1V$

the output conductance has to be extremely low. We call this regime the double saturation regime.

Electric fields Figure 4.23 presents the longitudinal electric field in the thin silicon film for the 2 μm GCMOS ($LND/L = 0.5$) and the 1 μm MOSFET under $V_{gs} = 0.6\ V$ and $V_{ds} = 0,\ 0.4$ and $1\ V$. The distribution of the longitudinal electric field in the doped and undoped regions of the GCMOS is clearly shown. Comparing the longitudinal electric field for MOSFET and GCMOSFET with the same effective channel length, an important reduction of the peak electric field at the drain side is achieved with GC MOS. This reduction of longitudinal electric field means lower impact ionization, hot electron degradation as well as higher breakdown voltage.

Conclusion 2D simulations have provided an intrinsic analysis of the graded channel transistor. The benefits of the GCMOS deduced from its output characteristic have been confirmed by simulation. The reduction of the effective gate length at low gate voltage overdrive has been proved. The double saturation regime has been defined, as the optimal bias conditions were the GCMOS has its smaller effective channel length, and its lower output conductance.

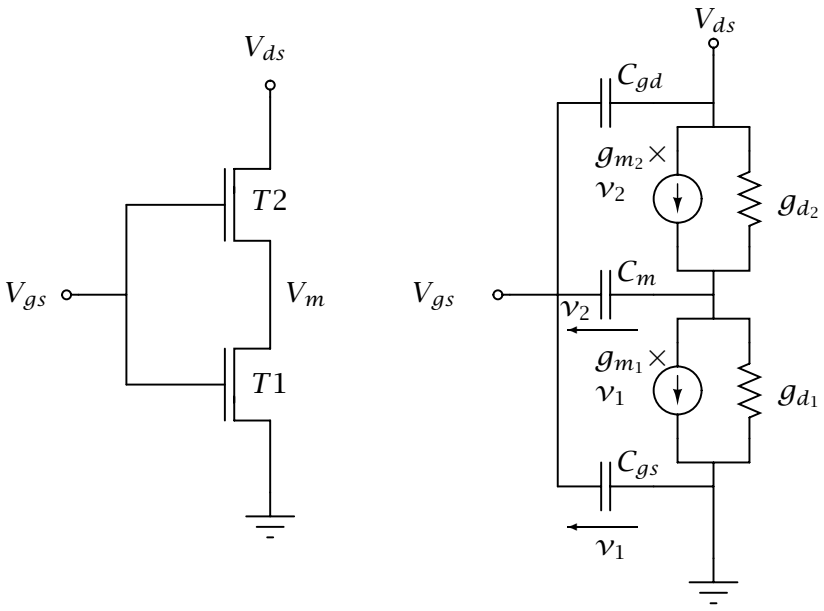


Figure 4.24: Simplified model of GCMOS using a cascode.

4.4.3.3 Modeling

The GCMOS structure can be seen as two cascoded transistors, having the same gate but two different threshold voltages [26]. The low frequency equivalent circuit of the GCMOS is shown in Figure 4.24.

By using the simple equivalent circuit, the transconductance and output conductance of the GCMOS can be defined as a function of the two subtransistors transconductances and conductances

$$g_{m_{tot}} = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=0} \approx g_{m_1} + g_{d_1}\frac{g_{m_2} - g_{m_1}}{g_{d_1} + g_{d_2} + g_{m_2}} \tag{4.16}$$

$$g_{d_{tot}} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=0} \approx \frac{g_{d_1} g_{d_2}}{g_{d_1} + g_{d_2} + g_{m_2}} \tag{4.17}$$

Equations (4.16)-(4.17) can be used to confirm the benefit of the double saturation regime. Indeed to maximize the transconductance, and to minimize the output conductance, the transconductance of the transistor T2 has to be maximized and its output conductance minimized. These conditions are reached simultaneously when the transistor T2 is in saturation regime.

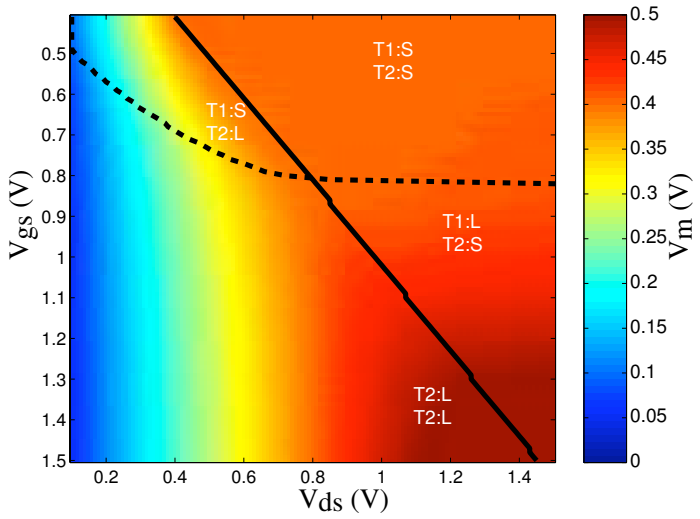


Figure 4.25: Simulated potential at the interface between the two sub-transistors with $V_{th_1} = 0.4V$ and $V_{th_2} = 0V$ versus V_{gs} and V_{ds}

To understand more intuitively the behavior of the GCMOS, its equivalent circuit has been simulated using simple MOS current equations for the two sub-transistors T1 and T2.

The current of the transistor T1 is given by

$$\begin{cases} I_{ds_1} = \mu C_{ox} \frac{W}{L - L_{ND}} \left(\left(V_{gs} - V_{th_1} \right) V_m - \frac{\lambda}{2} V_m^2 \right) \\ \frac{\partial I_{ds_1}}{\partial V_m} = \frac{I_{ds_{sat}}}{V_{ea}(L - L_{ND}) + V_{ds_{sat}}} \quad \text{when } V_{ds} \geq V_{ds_{sat}} \end{cases} \tag{4.18}$$

And the current of the transistor T2 is given by

$$\begin{cases} I_{ds_2} = \mu C_{ox} \frac{W}{L_{ND}} \left(\left(V_{gs} - V_m - V_{th_2} \right) \left(V_{ds} - V_m \right) - \frac{\lambda}{2} \left(V_{ds} - V_m \right)^2 \right) \\ \frac{\partial I_{ds_2}}{\partial (V_{ds} - V_m)} = \frac{I_{ds_{sat}}}{V_{ea}(L_{ND}) + V_{ds_{sat}}} \quad \text{when } V_{ds} \geq V_{ds_{sat}} \end{cases} \tag{4.19}$$

The total current of the GCMOS is obtained by imposing $I_{ds_1} = I_{ds_2}$ for a given gate and drain voltage.

By using this simple set of equations, four operation regimes can be defined for the GCMOS, depending on the operation regime of each subtransistor (Linear

	V_{th} (V)	L (μm)	W (μm)	V_{ea} ($V/\mu m$)	μ	λ	$C_{ox}(F/\mu m^2)$
T_1	0.4	1	80	10	500	1	1.15×10^{-15}
T_2	0	1	80	10	500	1	1.15×10^{-15}

Table 4.3: Parameters used for the simulation of GCMOS with the simple MOSFET equation

or Saturate).

Figure 4.25 shows the potential at the interface between the two subtransistors (V_m) versus the applied gate and drain voltage. The technological parameters used for the simulation are given in Table 4.3.

The knowledge of the potential V_m allows us to define the limit between the linear and saturation regime for each transistor. Then the limit of the double saturation regime is obtained. As predicted by the 2D simulation, there is a gate potential above which the double saturation regime cannot be obtained. This limit corresponds to the bias point where both sub-transistors saturate simultaneously. That gate voltage might not correspond to the gate voltage of the maximum transistor transconductance.

The highest gate voltage that can be used ensuring the double saturation is given by solving the following set of equations

$$\begin{cases} V_m = \frac{(V_{gs}-V_{th_1})}{\lambda} \\ V_{ds}-V_m = \frac{(V_{gs}-V_m-V_{th_2})}{\lambda} \\ \mu C_{ox}\frac{W}{L-L_{ND}}\left((V_{gs}-V_{th_1})V_m - \frac{\lambda}{2}V_m^2\right) = \mu C_{ox}\frac{W}{L_{ND}}\Big((V_{gs}-V_m-V_{th_2}) \\ \qquad\qquad (V_{ds}-V_m) - \frac{\lambda}{2}(V_{ds}-V_m)^2\Big) \end{cases} \tag{4.20}$$

If the gate length of the sub-transistors are considered equal ($L - L_{ND} = L_{ND}$), and if $\lambda = 1$, the solutions of the system are

$$V_{gs} = V_{th_1} + (V_{th_1} - V_{th_2}) \tag{4.21a}$$

$$V_m = V_{th_1} - V_{th_2} \tag{4.21b}$$

$$V_{ds} = 2V_{th_1} \tag{4.21c}$$

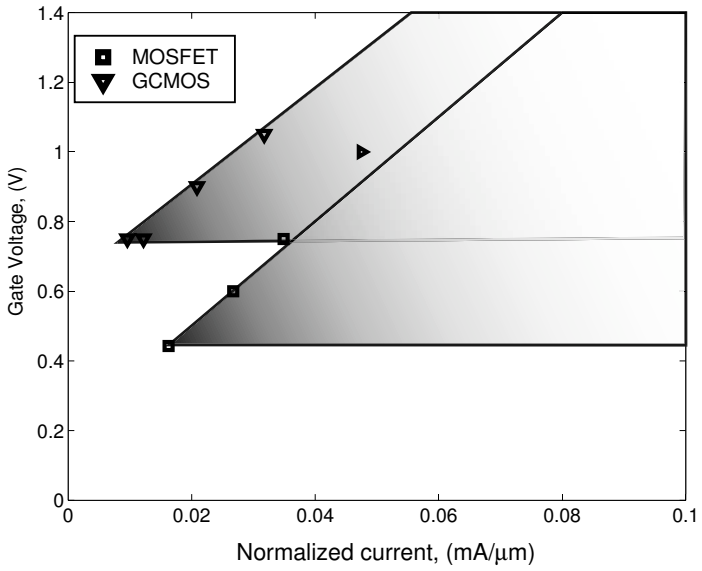


Figure 4.26: Biasing conditions allowing us to achieve a f_t>10 GHz.

Thus to ensure a large range of bias were the double saturation can be used, the gate voltage defined by Equation (4.21a) must be as large as possible. The difference between the two threshold voltage must be large. But, the threshold voltage of the first transistor must be kept relatively low to ensure the double saturation regime for a relatively small drain voltage (Equation (4.21c)).

4.4.4 RF properties

DC analysis shows that graded channel transistors have interesting properties in the double saturation regime. As explained above, the double saturation regime occurs only when specific bias conditions are applied. Depending on the technology, the maximum transconductance, which is the most important factor for the RF performances of MOSFET, might not occur in the double saturation regime. Thus, it is not relevant all the time to evaluate the RF performances of GCMOS using only the highest cut-off frequencies (f_t, f_{max}).

In the following sections, RF performances and potentialities of GCMOS will be demonstrated using various figures of merit. Various transistors from various technologies are used (FD SOS and PD body-tied to the source GCMOS).

Cut-off frequencies Usually, the RF performances of transistors are discussed in terms of maximum of f_t or f_{max}. The optimal performances are obtained in strong inversion, with a high gate voltage overdrive, and a large current when the transconductance is maximal. These criteria are not relevant for GCMOS, as the maximum of transconductance does not occur in the double saturation regime, as explained previously.

A most relevant figure of merit to compare GCMOS with conventional MOSFET is the power, or current consumption required to reach a given cut-off frequency, but not the maximum f_t.

Figure 4.26 shows the bias required to ensure a $f_t > 10\ GHz$ for a SOS FD MOSFET with $L = 0.5\ \mu m$ and $W = 200\ \mu m$ and a GCMOS with the same geometrical dimension but with $L - L_{ND} = 0.5$. The threshold voltages are equal to $0.7\ V$, and to $0.4\ V$ for the GCMOS and MOSFET respectively.

Thanks to its smaller effective gate length, the GCMOS allows to reach a $f_t > 10\ GHz$ using a smaller among of current. Thus, the total power consumption is lower for the GCMOS than for the MOSFET.

Equivalent circuit The components of the equivalent circuit of the transistors can be compared to provide more informations on transistors performances. The equivalent circuit for the GCMOS is considered the same as for a conventional MOSFET. Basically, the GCMOS is, as a MOSFET, composed of several sub-transistors connected in series. Then, the equivalent circuit of the intrinsic part of the GCMOS will be composed of the same components than for the MOSFET.

Unfortunately, the method presented in Chapter 3 cannot be used for extract the equivalent circuit of GCMOS. As presented by PAVANELLO in [27], the gate to drain (C_{gd}) and gate to source (C_{gs}) capacitances of a GCMOS are not equal when $V_{ds} \approx 0$. Then, the inversion method, presented in section 3.2.4, cannot be used to extract the extrinsic resistances of GCMOS.

To avoid that limitation, values of extrinsic resistances extracted from a MOSFET having the same geometrical dimensions as the GCMOS have been used to estimate the extrinsic resistances of the GCMOS. Table 4.4 provides extracted values of g_m, g_d and C_{gg} of a GCMOS with a total width of 120 μm and a physical

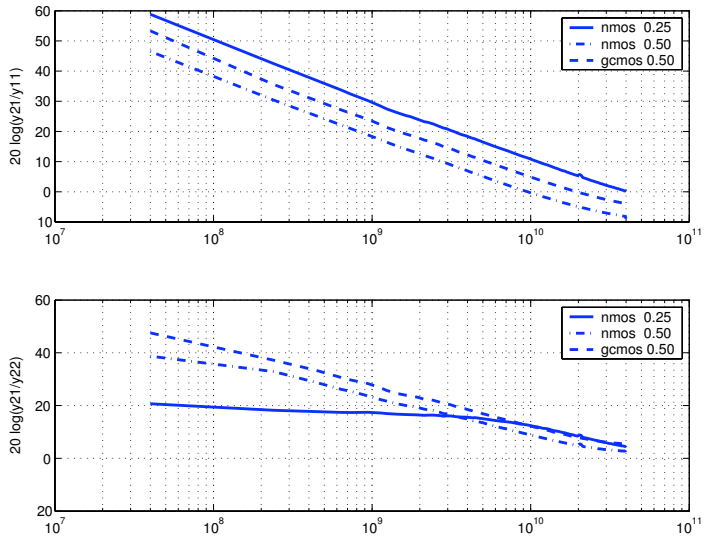


Figure 4.27: Measured RF current and voltage gains versus frequency for PD SOI MOSFET's and GCMOS at Vg=1 V, Vd=1.5 V.

gate length of 0.5 μm and a MOSFET with a total width of 120 μm and a physical gate length of 0.25 μm fabricated on a SOI PD technology biased at $V_{gs} = 1\ V$ and $V_{ds} = 1.5\ V$. The body of each transistors is tied to the source. Figure 4.27 shows the RF current and voltage gain of these transistors. We added a MOSFET having the same geometry as the GCMOS to the graph for comparison. The cut-off frequency of the GCMOS is twice as high than those from a conventional MOSFET with the same geometry, but twice as small than the one of a MOSFET with the gate length of 0.25 μm. As explained above, the cut-off frequency, f_t, is proportional to g_m and $1/(C_{gs} + C_{gd})$. Since, g_m is proportional to the inverse of the effective channel length and the gate capacitance is proportional to the physical dimension of the gate, the GCMOS must have the same total gate capacitance as the $0.5\mu m$ MOSFET, and the same g_m as the $0.25\mu m$ long MOSFET. This is confirmed by the extracted values (Table 4.4).

To highlight the benefit of the output conductance decrease in the GCMOS structure, the voltage gain, which is proportional to g_m/g_d, is also presented in Figure 4.27. Higher values are obtained for the GCMOS than for other devices. This highlights the increase of the output conductance in the GCMOS compared to classical devices, by up to more than a factor of 10 for the same effective length.

Name	V_{gs}	V_{ds}	f_t (GHz)	g_m (mS)	g_d (mS)	C_{gs} (fF)	C_{gd} (fF)	g_m/g_d	C_{gs}/C_{gd}
MOSFET $L = 0.25\mu m$	1	1.5	38	11.5	1.8	32	14.5	6.38	1.5
GCMOS $L = 0.5\mu m$ $L_{ND} = 0.25\mu m$	1	1.5	19	9.8	0.3	62	20	32.7	3.1

Table 4.4: Extracted values of the equivalent circuit of a MOSFET and GCMOS made on PD SOI technology. Their body is tied to the source.

Conclusion RF performances of GCMOS have confirmed the advantages deduced from the DC analysis. A reduced effective channel length and a decrease of the output conductance has been also deduced from RF study.

4.4.5 Summary

The graded channel MOSFET structure has been analyzed from both DC and RF point of view. The reduction of the effective channel length of the GCMOS and its extremely small output conductance compared to conventional MOSFET has been explained using simulation, and a simple, intuitive modeling.

A new operation regime, where the benefits of GCMOS are optimal, called double saturation regime has been defined. In that regime, the two regions of the GCMOS (P-doped region and Naturally doped region) are in saturation. The current is mainly controlled by the P-doped region, as well as the transconductance of the device. The ND region acts like an active resistance that reduces the influence of the drain potential on the P-doped region. Thus extremely low output conductances are obtained.

The double saturation regime only occurs when the gate voltage overdrive is relatively low (depending on the used technology), which means that the GCMOS structure is extremely interesting for low voltage application, as it provides an increase of the transconductance, since the channel length is reduced, and a drastic decrease of the output conductance, which is nowadays one of the performance limiting factors of transistors.

4.5 Conclusion

In this chapter, we presented two alternative structures of MOSFET that allow to obtain better performances than conventional MOSFET for low voltage, low power microwave applications.

The DTMOS transistor has been presented as an efficient way to reduce the threshold voltage of transistor, and to reach at low bias the maximum performance of a PD CMOS technology. But to increase the benefit of the DTMOS compared to conventional MOSFET, MOSFET transistors must have a high threshold voltage and a high body factor, to take a real advantage of the threshold voltage reduction dues to the DTMOS effect. This is at the opposite of the actual trends in microelectronic.

The GCMOS transistor has been presented has an elegant technique, which allows the reduction of the effective gate length of a transistor and simultaneously the decrease of its output conductance. The production of graded channel is fully CMOS compatible. Very promising results were obtained, on various technologies. Further investigation should be done to determine the optimal doping level for each part of the GCMOS, taking into account the doping level influence on the mobility,...

Both alternative structures of transistors allow to increase the performances of MOSFET, for a given gate length, and especially for Low-Voltage operation.

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