Sub-mmWave Transmission Lines on Silicon-Based Technologies

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***Abstract* — In modern complementary metal-oxide semiconductor (CMOS) process, the quality of the transmission line is very crucial to the integrated circuit (IC) design. However, with the continuous scaling of the advanced CMOS node, the compact back-end-of-line (BEOL) drastically influence the performance of all passive circuits, which cannot be completely overcome due to the physical limit. After a comprehensive comparison with the various transmission lines from the state-of-the-art, three optimum transmission lines (stripline, microstrip, and coplanar waveguides) based on GlobalFoundries (GF) 22FDX® are designed and measured. Then, these proposed transmission lines are benchmarked with silicon-filled waveguide to evaluate the potential of the later when moving to the sub-mmWave domain. It shows that the low loss (0.25, 0.46, and 0.6 dB/mm reduction at, respectively, W-band, D-band, and H-band compared with planar TLs) of silicon-filled waveguide opens a new window for the IC designers, especially above 300 GHz.**

***Keywords* — CMOS, Sub-mmWave, transmission line, silicon-filled waveguide.**

I. Introduction

Transmission line (TL) forms the cornerstone of modern integrated circuits. They do not only connect individual devices, but can also build up matching networks, filters, power splitters, etc. In CMOS technologies, TLs are built using the back-end-of-line (BEOL) metal layers. The main types of TL are the microstrip (MS, Fig. 1b) and coplanar waveguide (CPW, Fig. 1a) configurations. MS lines use a substrate-shielding bottom ground plane built in the lower metal levels while CPW lines rely on coplanar ground planes as the current return path [1]. Thus, MS lines are insensitive to the substrate electrical properties while CPW lines are substrate-sensitive.

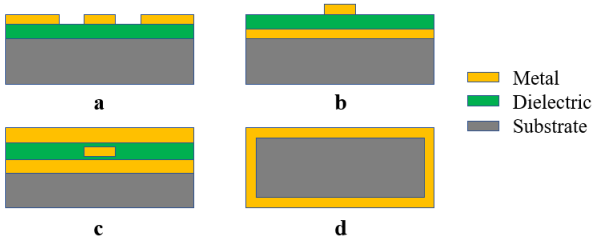

Fig. 1. Cross-section view of TL topologies investigated in this work: (a) CPW, (b) MS, (c) stripline, (d) rectangular waveguide.

CMOS process keeps moving to shorter nodes and thus higher integration levels, featuring f_t and f_{max} in the range of 300 to 400 GHz [2]. However, as the CMOS node scales down, the BEOL also vertically shrinks and sees bottom metal and dielectric layers thickness reduction as illustrated in Fig. 2 for the 65, 40 and 28 nm nodes [3]. Even highly shrunk CMOS technology nodes still feature thick metal layers in their BEOL to enable low-loss RF passives. However, due to skin-effect, metallic losses increase at higher frequencies, which cannot always be compensated by increasing the metal thickness.

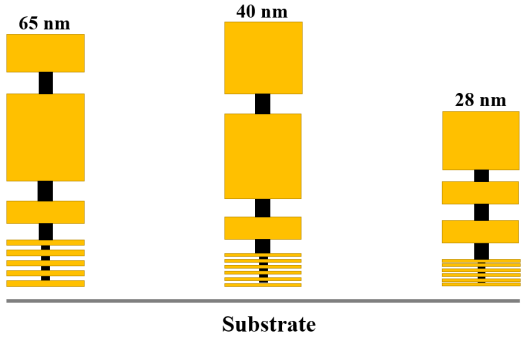

Fig. 2. Simplified cross sections of 65, 40, and 28 nm CMOS BEOL. (adapted from [4]).

As TLs are made using BEOLs, their performances are strongly linked to the BEOL characteristics (number of metal levels, thickness of metal and dielectric layers, conductivity of metal layers, etc.). To illustrate this, Fig. 3 summarizes published TL losses for MS and CPW lines across different CMOS nodes and at an arbitrary frequency of 60 GHz. Both standard (STD, 10 ~ 20 Ω.cm) and high resistivity (HR, > 1k Ω.cm) substrates are used in those studies.

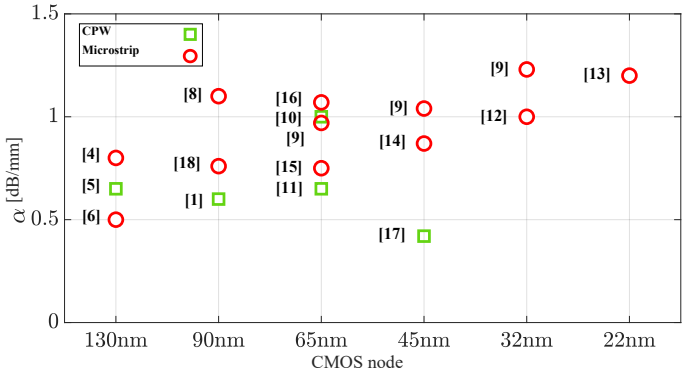

Fig. 3. Published TL losses for different CMOS nodes at 60 GHz.

(1) In general, MS losses tend to increase in more advanced technologies for which overall BEOL thickness reduction leads to increased conductor losses.

(2) For CPW lines built on HR substrates ([1], [5], [11], [17]) this trend is not observed. On HR substrates CPW can be built by stacking more (or all [17]) metal layers even if it brings the signal line closer to the substrate, as electric fields inside HR substrate have a negligible contribution [7] compared with metallic losses to the total TL losses. For this reason, on a given CMOS node the CPW can usually achieve better performance than the MS when a high resistivity (HR) substrate is used. This is no longer true when standard resistivity substrate is used [10].

In this paper, the performance of optimized TLs in commercial advanced mmWave CMOS technology (22FDX®) is investigated and in view of sub-mmWave applications. This study is meant to serve as a benchmark for future investigations. An alternative TL approach based on integrated silicon-filled waveguide (WG) is also investigated. In Section II, the design of planar TLs is described. Section III details the measurement setup and the TL parameters extraction procedure. Section IV explains the concept of integrated waveguides on silicon. Section V discusses the advantages of silicon-filled WG for sub-mmWave TL.

II. Description of Transmission Line Topologies

In this study three different TLs are designed and fabricated: a Stripline (SL, Fig. 1c) and a Microstrip in the GlobalFoundries' 22FDX® process and a CPW on a HR substrate with special P- and N-doping patterns to reduce parasitic surface conduction from a 22FDX® split-process experiment similar with [19]. The SL is investigated here because of its potential interest for sub-mmWave applications since the signal line is completely shielded all around and thus it is not sensitive to neighbouring devices and should not couple to parasitic substrate modes. All these TLs are designed to feature a 50 Ω characteristic impedance. The signal strips are designed in QA layer for SL, and QB layer for both MS and CPW. Their geometrical details are shown in Table 1.

Table 1. Details of three TLs in GF 22FDX®.

Topology	Substrate	Cross-Section (µm)	Length (µm)
Stripline	STD	W = 2	300, 700
Microstrip	STD	W = 9	300, 700, 1700
CPW	HR (PN patterns)	W = 35, S = 25 Wg = 200	760, 2000

III. Experimental Setup

The TLs are measured from 0.2 GHz to 130 GHz on an MPI Prober station, with a Keysight VNA N5291A and mm-wave frequency extenders, as well as a pair of Form-Factor Infinity Ground-Signal-Ground (GSG) probes with 100 µm-pitch. A Line-Reflect-Reflect-Match (LRRM) calibration is performed on an Impedance Standard Substrate (ISS) Calkit. The propagation constant (γ) is extracted with a multiline Thru-Reflect-Line de-embedding method [20]. The measured results of planar TLs up to 130 GHz are presented in Fig. 4. The figure shows that the proposed MS demonstrates significantly better performance (0.41 dB/mm at 60 GHz) than the data reported in [13] (1.2 dB/mm at 60 GHz). This improvement could partly be explained by the use of a more resistive metal layer (LB) for the signal strip, a narrower strip width in [13] and the use of a different BEOL option limiting the ground planes design to thin and more lossy metal layers. The CPW features the lowest losses (0.23 dB/mm at 60 GHz) and beats the state-of-the-art even on other nodes thanks to the use of HR substrate with special P- and N-doping patterns. At 60 GHz, the SL exhibits losses that are roughly twice those measured on the MS, which seems to be the price to pay to obtain a fully-shielded TEM mode within the BEOL. Those large losses are due to important metallic losses in the narrow (2 µm-wide) metal width of the signal line needed to achieve a 50 Ω characteristic impedance.

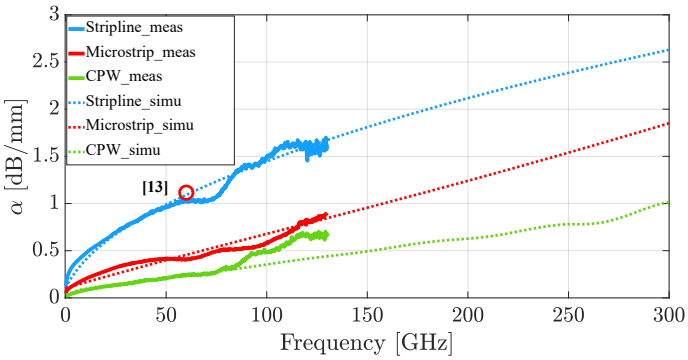

Fig. 4. Attenuation loss for measured TL up to 130 GHz and simulated TL up to sub-mmWave.

To the best of the authors' knowledge, the presented MS and CPW exhibit superior performance in comparison with the state-of-the-art. In order to evaluate their potential use for sub-mmWave applications, those TLs are simulated using CST software with the purpose of anticipating their losses at higher frequencies. In those simulations the full GF 22FDX® BEOL is taken into consideration. Fig. 4 also shows the good agreement obtained between measurement and simulation results up to 130 GHz. The difference between the CPW simulation and measurement above 85 GHz is attributed to parasitic coupling and parasitic mode generation during the measurements [21]. As the simulated results of the proposed CPW, MS, and SL match well with the measurements, they give confidence on the accuracy of the extrapolated TL performance beyond 130 GHz. Those data are treated as benchmarks in this paper for TL losses in the sub-mmWave range.

IV. Silicon-Integrated Waveguides

The TLs presented in Sections II and III show excellent results compared with the state-of-the-art. However metallic losses increase as $\sqrt{f}$ due to the skin effect in the BEOL metal layers, which might become an issue for applications at sub-mmWave range. For this reason, another TL approach has been proposed in the literature based on Si-integrated rectangular waveguides [22]-[24] (Fig. 1d). Silicon-integrated WGs have been demonstrated in two forms: air-filled and Si-filled WGs. Air-filled WG can be fabricated by utilizing a double H-plane split in a three-wafer stack [24], showing an averaging loss of 0.039 dB/mm between 220-325 GHz. Silicon-filled WG can be fabricated from DRIE BOSCH

process etched HR silicon covering by metal surrounding [23], showing the loss of 0.43 dB/mm at 325 GHz.

Si-integrated WG sustains very low losses even in the sub-mmWave range. Also, for a given bandwidth, the air-filled metallic waveguides perform significantly better than the Si-filled WG, which suffers from substrate losses due to the presence of silicon inside the WG. Nevertheless, the reported losses for Si-filled WG remain considerably lower than the ones shown in Fig. 4 for planar TLs, including the low-loss CPW on HR substrate with PN patterns. Also, thanks to the high relative permittivity of silicon (11.9), the silicon-filled WG overall dimension can be shrunk by roughly 40 times (volume-wise) when compared with the air-filled rectangular WG. Low insertion loss and reduced geometry make Si-filled WG attractive for sub-mmWave applications. To study the performance of integrated rectangular WG, silicon-filled waveguides and their feeding transitions are designed for three distinct frequency bands from W-band to the sub-mmWave range. The HR silicon ($\rho = 5\ k\Omega.cm$) is surrounded by aluminium ($\sigma = 3.56x10^7\ S/m$) sidewalls (thickness = 1 µm, surface roughness = 200 nm). The design of the CPW-to-waveguide transition is based on the one presented in [25], and is scaled for the different bands. In order to study the interest of the WG topology in those frequency ranges, the waveguide widths A are chosen as: 600 µm (W-band), 420 µm (D-band), and 240 µm (H-band). The height (B) is kept at half of the width to ensure the TE_{10} remains the dominant mode of operation. A 3D view of the Si-filled waveguide with the two transitions on each side is shown in Fig. 5 and as simulated in CST. The geometry of a single transition and its dimensions are given in Fig. 6 and Table 2, respectively.

Fig. 5. 3D view of the proposed Si-filled waveguide and transitions.

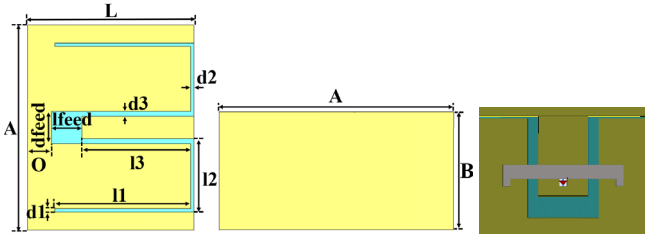

Fig. 6. Geometry of designed transition: (a) transition, (b) cross-section, (c) excitation method in the CST Suite simulation setup.

Table 2. Parameters of transitions & Si-filled waveguide.

Parameter		A	B	L	l1	d1	l2
Value (µm)	W-band	600	300	490	400	10	215
	D-band	420	210	350	252	56	160
	H-band	240	120	186	137	32	93
Parameter		**d2**	**l3**	**d3**	**lfeed**	**dfeed**	**O**
Value (µm)	W-band	10	320	14	90	94	70
	D-band	28	210	25	10	80	102
	H-band	16	140	15	10	55	20

The simulations are based on double-sides Perfect Electric Conductor bridge excitation (Fig. 6c) with the frequency-domain solver. Two different homogeneous lengths are simulated for each waveguide. The return losses of the three simulated silicon-filled waveguides can be seen in Fig. 7, which are below -10 dB from 77 to 130 GHz for W-band, 105 to 190 GHz for D-band, 185 to 330 GHz for H-band. The WG losses of the proposed Si-filled WGs are extracted using the L-L de-embedding algorithm. They are shown in Fig. 8 where they are compared with experimental results reported in the literature and with the planar TL simulated results presented in Fig. 4. For all studied frequency bands, the silicon-filled waveguides behave significantly better in terms of losses than the planar TL benchmarks. The simulated results are in good agreement with the measured data reported in the literature (0.121 dB/mm at 105GHz in [22], 0.43 dB/mm at 325 GHz in [23]). At 105 GHz, the simulated WG has an 0.25 dB/mm reduced loss compared with the simulated CPW line (featuring the lowest line losses among planar TLs considered in this paper). Similarly, an 0.46 dB/mm and 0.6 dB/mm improvement in losses can be achieved in D-band and H-band, respectively. This further demonstrates the intrinsic advantage of waveguides when compared to planar devices. The very similar $\alpha(f)$ curves for the different designs also suggest that this structure can be extended to higher frequency bands with very low level of losses as well.

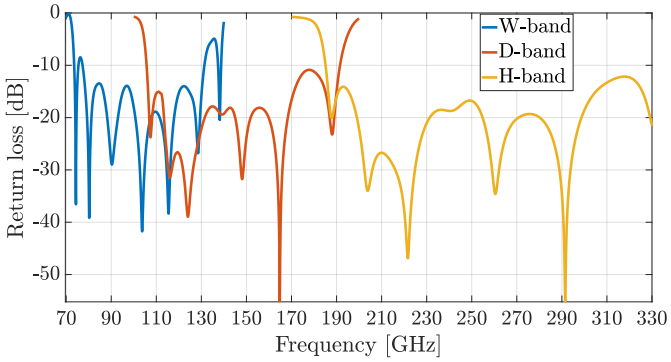

Fig. 7. Return losses of three simulated silicon-filled waveguides up to sub-mmWave range.

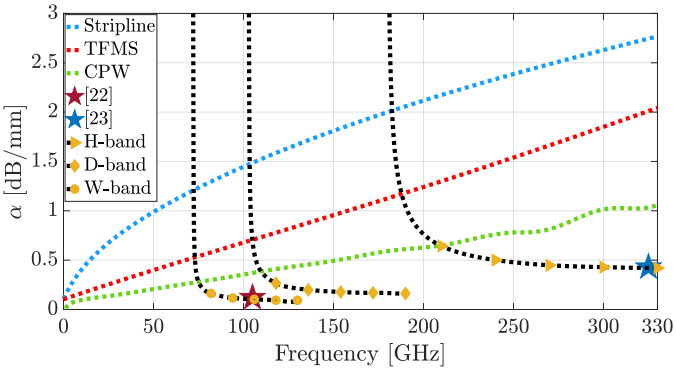

Fig. 8. Comparison of attenuation loss versus frequency for three proposed silicon-filled waveguides and the three TL benchmarks.

Realizing WG in an industrial CMOS technology can be envisaged in three ways. In the first case, the WG is designed

in the substrate, that requires through-silicon via compatible CMOS process. Another way would be to design the WG inside the BEOL dielectric layers. Given the 22FDX® BEOL, the minimum cut-off frequency (and considering A = 2 × B) is above 1 THz, which is too high for sub-mmWave application. A third way would be using other thick dielectrics such as BCB on top of the fully CMOS-processed wafers using post-process techniques [26]. It is estimated that the footprint of planar TL and WG will become comparable in the D-band frequency range (cross-section width: 485 µm for proposed HR CPW with PN pattern, and 420 µm for D-band WG). As the WG cross-dimensions scale inversely with frequency, the silicon-filled WG will have the advantage of miniaturization starting from 250 GHz. Compared with conventional MS and CPW lines, an added advantage of silicon-filled waveguide is its complete isolation from the rest of the substrate. This makes it insensitive to crosstalk and prevents coupling to and from parasitic surface mode. In addition to the loss improvements of WG compared with planar TLs, planar TLs will not be really convenient above 300 GHz due to higher mode excitation. This further highlights the attractiveness of Si-filled WG as transmission lines for future sub-mmWave applications based on CMOS technology.

V. Conclusion

A comprehensive investigation of classic TLs in different CMOS nodes (from 130 nm to 22 nm) based BEOLs is presented in this paper. The general trend of TL attenuation loss in different BEOLs, substrates and topologies has been discussed. Three optimum TLs (Stripline, MS, CPW) on GlobalFoundries 22FDX® process are simulated, fabricated and characterized. A good agreement between simulations in CST considering the full GF 22FDX® BEOL and the measurements is observed for the attenuation loss. The extrapolated results serve as the benchmark to evaluate silicon-filled waveguide's potential in sub-mmWave domain. Three silicon-filled waveguides in W-band, D-band, and H-band are simulated and compared with previously published experimental data. These proposed silicon-filled waveguides are highly attractive with their low loss (0.25, 0.46, and 0.6 dB/mm reduction at, respectively, W-band, D-band, and H-band compared with planar TLs) and small-scale characteristics. The IC designers should start considering the use of silicon-filled WG above 300 GHz due to the appearance of higher order modes along classical planar TLs. Thus, the silicon-filled WG become a great option for future sub-mmWave advanced technologies.

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