Impact of III-N buffer layers on RF losses and harmonic distortion of GaN-on-Si Substrates

P. Cardinael[#1], S. Yadav[*], M. Zhao[*], M. Rack[#], D. Lederer[#], N. Collaert[*], B. Parvais[*+], J.-P. Raskin[#]

[#]ICTEAM, UCLouvain, Louvain-la-Neuve, Belgium

[*]imec, Leuven, Belgium

[+]VUB, Brussels, Belgium

[1]pieter.cardinael@uclouvain.be

***Abstract* — The reduction of substrate RF losses and non-linearities is key to enable high-performance GaN-on-Si HEMT based RF front-end modules. In this paper, the impact of the epitaxial III-N buffer layers on substrate RF losses and harmonic distortion is studied experimentally using coplanar waveguide (CPW) structures. In contrast to a SiO_2/Si stack, a strong hysteresis in the RF losses (quantified using effective resistivity ρ_{eff}) of the HEMT stack is observed when the chuck DC bias is swept. A comparative analysis of various material stacks suggests that the hysteresis originates from the large time constants (much larger than 1 s) associated with the traps in the III-N layers. Harmonic distortion, on the other hand, shows much weaker hysteresis effect than ρ_{eff} during chuck bias sweeps.**

***Keywords* — GaN-on-Si HEMTs, RF losses, effective substrate resistivity, harmonic distortion, C-doped III-Ns**

I. Introduction

GaN-on-Si HEMT technology is a promising platform for front-end modules aimed at 5G and beyond applications [1-3]. However, compared to the more commonly used semi-insulating SiC substrate, finite resistivity of Si wafer is at the origin of substrate radiofrequency (RF) losses, crosstalk, and non-linearities [4,5]. This leads to degraded performance for both HEMTs (e.g. lower power added efficiency for amplifiers, poor isolation and linearity for switches) and passive devices (lower Q factors for inductors) [6].

The origin of RF losses in GaN-on-Si technology has been widely investigated in recent years and it is commonly accepted that they are caused by a parasitic surface conductive (PSC) layer located close to Si surface [7,8]. During MOCVD growth of III-N layers, group III elements (Ga and Al) diffuse back into Si, creating a p-doped channel at the surface of the high-resistivity (HR) Si substrate. Combined effects of Al/Ga doping, Si substrate impurities, charges in the nitride layers and interfaces, and strain at III-N/Si interface can result into a PSC layer [8]. To quantify substrate RF loss contribution, the effective substrate resistivity ρ_{eff} figure-of-merit is commonly used [5,8,9]. For CPW lines, ρ_{eff} represents conductive losses in the substrate independently of metallic losses and is useful in comparing multi-layered material stacks [10].

In addition to RF losses, a conductive substrate usually exhibits degraded linearity performance. It was shown that for Silicon-on-Insulator (SOI) substrates, the harmonic distortion (HD) measured on a CPW line can be correlated with ρ_{eff}, and its modulation with DC bias applied to either the CPW central conductor or the substrate [5]. Bias dependence of ρ_{eff} (and CPW loss parameter α) has also been observed in the CPW lines fabricated on GaN-on-Si substrates [7,8]. However, the situation here is more elaborate than for SiO_2/Si stacks (such as used in SOI technology) and the study of ρ_{eff} and HD in GaN-on-Si should include the more complex and doped semiconducting III-N buffer layer stack (Fig. 1a). For instance, charge transport and trap dynamics inside the III-N buffer have been used to explain on-state resistance (R_{ON}) dispersion in GaN HEMTs with C-doped III-N buffer [11,12]. Analogously, the defects and dopants in III-N layers should also impact the parasitic conduction at III-N/Si interface.

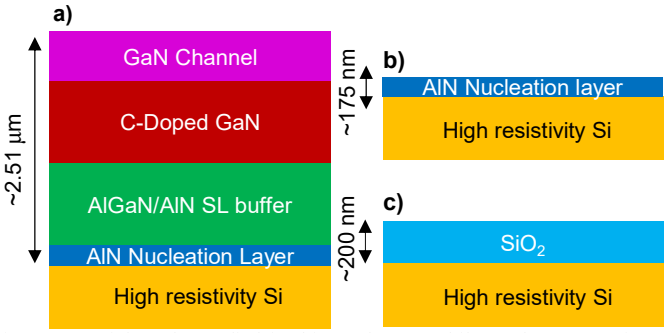

Fig. 1. Material stacks studied in this work. a) Multilayered GaN-on-Si RF HEMT buffer and GaN channel (without the 2-DEG inducing Al(Ga)N or Al(In)N top barriers). b) AlN nucleation layer grown on Si. c) Reference SiO_2/HR-Si substrate.

In this paper, we investigate the impact of III-N epitaxial buffer on substrate conductive losses (i.e., ρ_{eff}) and HD measured on CPW lines in GaN-on-Si technology. It is observed that ρ_{eff} for multi-layered GaN-on-Si HEMT buffer stack exhibits large hysteresis during chuck bias sweeps. By comparing with AlN-nucleation-layer/Si and SOI samples (Fig. 1b and 1c), it is shown that this behavior is due to slow trapping/de-trapping phenomena occurring inside the III-N buffer. We observe that unlike ρ_{eff}, harmonics do not show a significant hysteresis during chuck bias sweeps.

Table 1. Description of the different samples used in this study.

Sample	Si Resistivity	Material stack	Processing
A1	3-6 kΩ·cm (B doped)	~2.51 µm HEMT buffer/Si	CPW metal
A2	3-6 kΩ·cm (B doped)	~2.51 µm HEMT buffer/Si	140 nm SiO_2 + CPW metal
A3	3-6 kΩ·cm (B doped)	~2.51 µm HEMT buffer/Si	140 nm SiO_2 + N implant + CPW metal
B	3-6 kΩ·cm (B doped)	175 nm AlN /Si	8.5 nm Al_2O_3 (ALD) + CPW metal
C	> 5 kΩ·cm (n-type)	200 nm SiO_2/Si	CPW metal

II. Experimental Details

The III-N samples used for this study were grown using MOCVD on 200 mm HR-Si (3-6 kΩ·cm) substrates (Table 1) [7]. The GaN-on-Si stack comprises a ~175 nm AlN nucleation layer, a ~1.2 µm AlGaN strain relax buffer, a ~1 µm C-doped GaN layer, and a 300 nm unintentionally doped (UID) GaN layer. The Al(Ga)N top barrier layers were not grown to avoid formation of a 2-DEG channel. Some of the wafers were subjected to additional process steps of SiO_2 deposition (sample A2) and SiO_2 deposition followed by nitrogen ion implantation (sample A3). The nitrogen implant was limited to ~600 nm depth into the nitride layers as suggested from SRIM simulations [8]. For sample B, only the AlN nucleation layer was grown, and to prevent DC leakage at large DC biases, a thin (8.5 nm) layer of Al_2O_3 was deposited by atomic layer deposition (ALD). A typical HR-SOI sample was used as a reference sample (sample C).

CPW lines were fabricated on these samples and RF measurements were performed on 4 mm and 2 mm-long lines in a dark environment using a PNA-X N5242A Vector

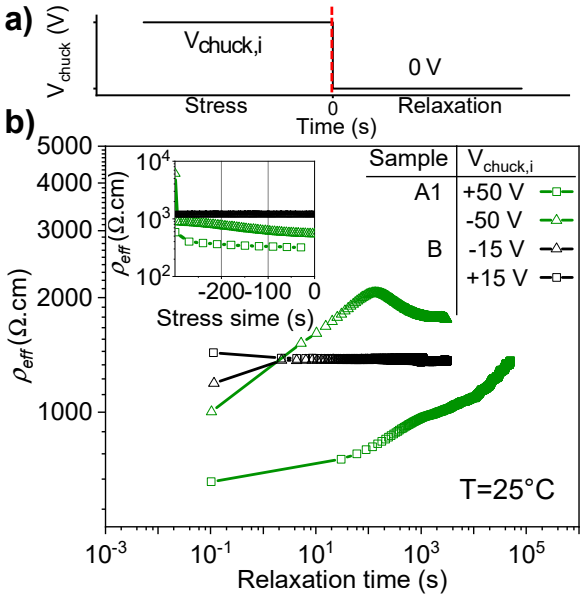

Fig. 2. a) Chuck bias stress/relaxation sequence. b) Relaxation of ρ_{eff} for samples A1 and B after stressing at different chuck biases for 300 s (inset). At t = 0 s, bias is switched from $V_{chuck,i}$ to 0 V. Slower trapping processes are observed for sample A1 and equilibrium is not reached even after more than 100 s relaxation.

Network Analyzer. Line-line de-embedding method was used to remove the parasitic pads contribution [13]. ρ_{eff} was then extracted from the de-embedded data [10] and averaged in the 0.8- 3 GHz range. Substrate-induced harmonic distortion was measured at fundamental tone of 0.9 GHz [5]. In addition to the fundamental (H1), the 2nd (H2, 1.8 GHz) and 3rd (H3, 2.7 GHz) harmonic power were measured at the output.

To study the effect of III-N buffer on ρ_{eff} and HD, the chuck bias is swept in the following sequence: 0 V → +50 V→ -50 V→ 0 V. To determine the appropriate voltage ramp rate, ρ_{eff} is monitored over time during a stress/relaxation sequence (Fig. 2a). For sample A1 (~2.51 µm HEMT buffer), ρ_{eff} stabilizes after a 300 s stress, both at +50 V and -50 V chuck bias (inset of Fig. 2b), corresponding to an average 10 V/min ramp rate. However, for traps (e.g. C related) in Ga(Al)N, emission processes can be much slower compared to capture processes, with time constants much larger than 1 s (Fig. 2b) [14]. Therefore, a 10 V/min ramp rate can be too high for trap relaxation processes and thus may not lead to an equilibrium ρ_{eff}(V) curve for samples A1 and A2 as discussed in the next section. On the other hand, for sample B, ρ_{eff} nearly saturates within a few seconds (Fig. 2b) for initial chuck biases of ±15 V. It is noted that a lower voltage stress is applied in samples B and C due to a much lower AlN or SiO_2 thickness as compared to samples A1-A3.

III. Results

A. Bias-Dependence of Effective Resistivity

Fig 3 shows the ρ_{eff} as a function of substrate bias. Samples A1 and A2 both show a large hysteresis, with a flatband voltage shift ΔV_p ≈40 V after having ramped the chuck bias to +50 V ($-V_{chuck}$ = 50 V). This is in strong contrast with the SiO_2/Si sample (C) which shows negligible hysteresis (Fig. 3c). Furthermore, after the first half of the sweep, only ~40% of the original ρ_{eff} value is recovered. A similar trend is seen for both samples A1 and A2, which indicates that vertical leakage is not the cause of the observed behavior as sample A2 has a 140 nm SiO_2 layer which would effectively prevent any DC leakage. Sample A3 presents a reduced hysteresis, and a reduction of ρ_{eff} modulation for $-V_{chuck} < 0$V. This is attributed to possible Fermi level pinning in the upper half of the GaN bandgap due to N-implantation [15].

Sample B shows a much lower hysteresis compared to samples A1 and A2 and a similar trend to the SOI sample C. This suggests that the large hysteresis and the "butterfly" feature in ρ_{eff}(V) curves for samples A1 and A2 is mainly induced by the III-N layers in the multilayer stack. The ρ_{eff}(V) trend of samples B and C can be correlated to their top-down metal-insulator-semiconductor (MIS) capacitance-voltage curve in Fig. 4. Interestingly, conductivity at 0 V is n-type for sample B, despite a starting p-type bulk Si and Al/Ga back-doping during AlN growth [7]. We previously linked this bulk type-inversion in HR CZ-Si wafers to activation of oxygen-related thermal double donors [8]. This is the reason that sample B has C-V characteristics similar to an n-type SOI substrate.

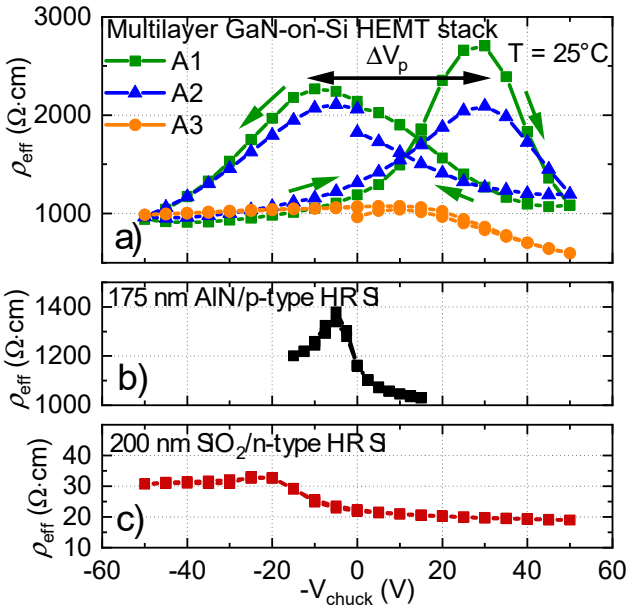

Fig. 3. Bias dependence of ρ_{eff} for all studied samples at room temperature. For all samples, CPW slot width is S=50 µm and bias ramp rate is 10 V/min. a) Large hysteresis is observed only for samples A1 and A2 (quantified with ΔV_p). b) Sample B (AlN/Si) shows a similar behavior to SiO_2/Si reference sample C (c).

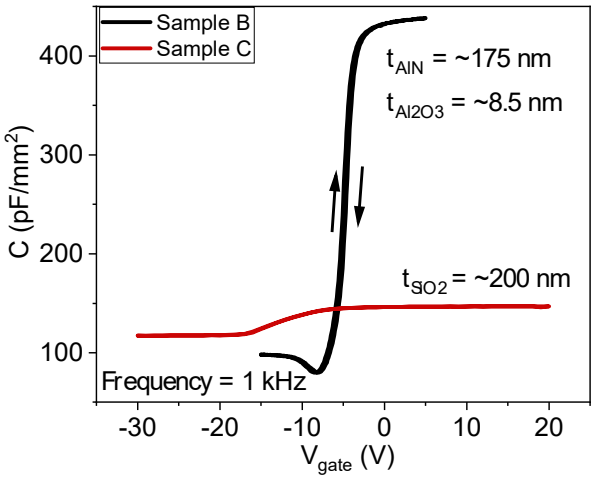

Fig. 4. Top-down MIS CV measurements for sample B (AlN/Si) and C (SiO_2/n-type HR-Si reference). Surface inversion is observed at 0 V for AlN sample, suggesting an inversion of the p-doped Si surface as well as conductivity type change in HR-Si after AlN growth.

B. *Harmonic Distortion*

Harmonic distortion (HD) for the samples at varying chuck bias is plotted in Fig. 5 at H1 of 15 dBm. Measurement conditions (ramp rate of 10 V/min and sweep direction) were kept the same as the ρ_{eff}(V) scans. Samples A1 and A3 (with multilayer buffer stack) show HD levels of less than -75 dBm for the entire bias range. This is comparable with commercially available trap-rich HR SOI wafers at similar ρ_{eff} [5,16]. Bias dependence of HD is reduced after isolation implant (sample A3), particularly for $-V_{chuck} < 0$ which is as expected from ρ_{eff}-V_{chuck} characteristics. For samples B and C, HD approximately follow the ρ_{eff} -V_{chuck} and C-V characteristics i.e. HD is large when surface inversion or accumulation is present [16].

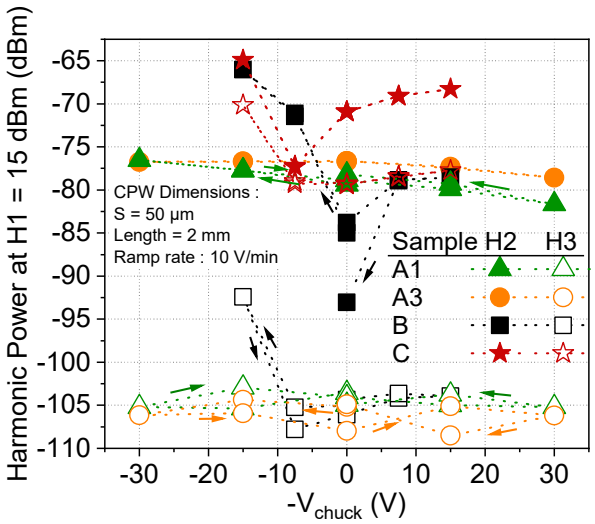

Fig. 5. Variation of 2nd (H2) and 3rd (H3) harmonic power with substrate bias measured on 2 mm-long CPWs for the different studied samples at 25°C. Arrows indicate sweep direction. A very weak chuck bias-dependence is observed for samples with thick III-N buffer (A1, A3) as compared to AlN/Si stack (sample B).

IV. Discussion

A. *On the Origin of Hysteresis in ρ_{eff}*

Hysteretic effects during bias sweeps were also previously observed in GaN-on-Si buffer stacks. In [11], C-doping in GaN was shown to have a strong impact on the recovery of the 2-DEG conductance after a negative substrate ramp. A very small hysteresis in sample B, C, and A3 (Fig. 3) indicates that the large hysteresis in samples A1 and A2 does not originate from the Si substrate, which is similar for all samples. It also shows that traps at AlN/Si interface, or border traps in AlN, do not play a significant role in the time scales used here. We suggest that asymmetric capture (short)/emission (long) time constants of traps in the III-N buffer layers (strain relax buffer and/or C-doped GaN layer) can explain the ρ_{eff}(V) characteristics of samples A1 and A2. The slow emission process is confirmed by the large relaxation time constants seen in Fig. 2b. Charging of these traps shifts the flatband voltage of the metal/nitride-buffer/Si (a MIS structure) stack as indicated by the shift in peak ρ_{eff} position (ΔV_p).

To further investigate this dynamic effect, ρ_{eff}(V) scans were performed at different chuck temperatures (Fig. 6). A decrease in overall ρ_{eff} can be observed due to lower bulk HR-Si resistivity at higher temperatures [8, 17]. More interestingly, the hysteresis reduces with temperature. For example, a ΔV_p of only ~10 V is observed at 175 °C as compared to ~40 V at 25 °C. In [14], it was shown that time constants in heavily C-doped buffers strongly decrease with temperature. Consequently, hysteresis related to the slow emission of buffer traps reduces, and the high temperature [ρ_{eff}(V)] curve is closer to an equilibrium curve.

B. *Effect of HEMT isolation implant on ρ_{eff}-V curves*

The nitrogen ion implant is used to enable DC isolation of HEMTs by creating a large concentration of traps in the GaN active layers and suppressing the 2-DEG [1]. As discussed in

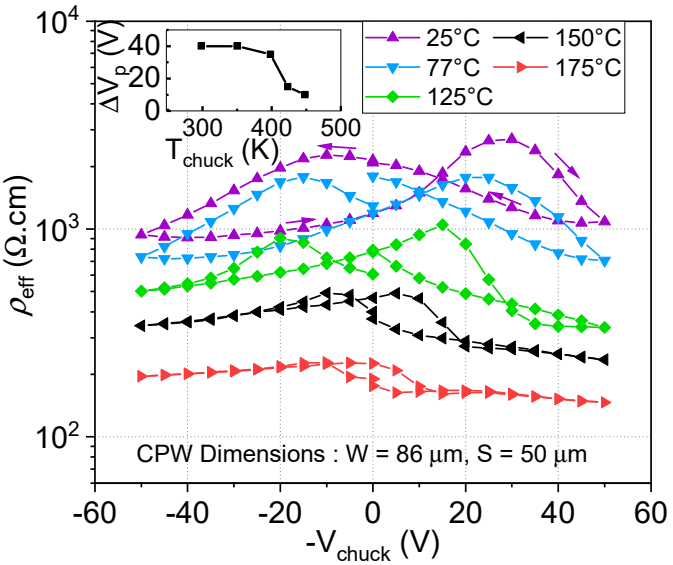

Fig. 6. ρ_{eff} of sample A1 versus chuck bias at different chuck temperatures. Both ρ_{eff} and the hysteresis decrease as the chuck temperature is increased. Inset : the trap-induced flatband shift ($\sim\Delta V_p$) is lower at higher temperatures.

the previous section, the hysteresis is strongly reduced after the nitrogen implant (Fig. 3a). Furthermore, ρ_{eff} modulation is limited for $-V_{chuck} < 10$ V. While for sample A1 ρ_{eff} drops by ~2× after ramping the voltage to 50 V, sample A3 shows only ~8 % change for the same bias range. In this bias region, the back-gate or chuck charge is mirrored onto the implanted GaN layers (trapped charge) and change in the PSC layer charge is very small. In other words, for $-V_{chuck} < 10$ V, the Fermi level movement in the N-implanted GaN layer is restricted. We speculate that defects in the upper half of the GaN bandgap can explain this behavior. This is consistent with literature, where deep levels at around E_c-0.9 eV were linked to nitrogen ion implantation [15].

C. *Correlation of ρ_{eff} and Harmonics*

In HR SOI wafers, a higher ρ_{eff} can be strongly correlated to lower HD levels [5]. This correlation is also observed for samples B and C, where a minimum in HD is observed for bias points close to a bias where a maximum in ρ_{eff} is found (Fig. 5). However, while this correlation seems to hold for the studied multilayer stacks at $-V_{chuck} = 0$ V (samples A1, A2, and A3), the HD for samples A1 and A2 have much lower hysteresis than that suggested from the ρ_{eff}(V) curves. For sample A3, a reduction of HD levels in the $-V_{chuck} > 10$ V region is observed, whereas a decrease in ρ_{eff} in the same region would suggest an increase of HD levels. These discrepancies indicate that prediction of substrate HD at different bias points for GaN-on-Si stacks cannot be based solely on the inspection of the ρ_{eff}(V) curve and more work is needed to accurately model the response of III-N/HR-Si stack to a large-signal bias.

V. Conclusion

To understand the RF small-signal (RF losses) and large-signal (linearity) behavior of MOCVD grown GaN-on-Si HEMT substrates, chuck bias dependent characterization of CPW lines is performed. A larger hysteresis in effective resistivity ρ_{eff} is observed. By comparing various material stacks (SiO_2/Si, AlN/Si, HEMT III-N Buffer/Si), we find that a large hysteresis is mainly caused by traps located inside III-N buffer layers, which exhibit a large discharging time constant. Also, as expected from the trap-limited process, hysteretic effects strongly reduce at higher temperatures. However, the HD *vs*. bias scans showed much lower hysteresis. Therefore, prediction of substrate non-linearity based on ρ_{eff} is more complex as compared to HR-SOI technology and physical modeling of the III-N buffer layers is needed to estimate HD levels.

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