2023 IEEE 23rd International Conference on Nanotechnology (IEEE-NANO 2023)
July 2-5, 2023 Jeju, Korea

The non-Landauer Bound for the Dissipation of Bit Writing Operation

Léopold Van Brandt and Jean-Charles Delvenne
ICTEAM, UCLouvain, Belgium
leopold.vanbrandt@uclouvain.be

2023 IEEE 23rd International Conference on Nanotechnology (NANO) | 979-8-3503-3346-6/23/$31.00 ©2023 IEEE | DOI: 10.1109/NANO58406.2023.10231222

***Abstract*—We propose a novel bound on the minimum dissipation required in any circumstances to transfer a certain amount of charge through any resistive device. We illustrate it on the task of writing a logical 1 (encoded as a prescribed voltage) into a capacitance, through various linear or nonlinear devices. We show that, even though the celebrated Landauer bound (which only applies to bit erasure) does not apply here, one can still formulate a "non-Landauer" lower bound on dissipation, that crucially depends on the time budget to perform the operation, as well as the average conductance of the driving device. We compare our bound with empirical results reported in the literature and realistic simulations of CMOS pass and transmission gates in decananometer technology. Our non-Landauer bound turns out to be a quantitative benchmark to assess the (non-)optimality of a writing operation.**

I. Introduction

Landauer's bound [1]–[3] states that an erasure of a bit, stored in an electronic device or any other type of physical memory, must dissipate at least $kT \ln 2$ (where k is Boltzmann's constant and T is the temperature). This figure cannot be taken as a benchmark for the dissipation of any kind of operation in digital circuits, however. Indeed it does not apply to logically reversible operations such as writing (or switching or copying) a bit into an empty memory, e.g. bringing the state of the memory from a logical 0 to a logical 1. Sub-kT bit-switching operations have been for instance discussed and carried out experimentally by [4], [5], exhibiting a trade-off between speed and dissipation of the operation.

While an arbitrarily low dissipation can indeed be theoretically achieved by implementing an arbitrarily slow process, here we show that, for any linear or nonlinear driving device and any specified time Δt for the bit writing operation, there *is* a fundamental lower bound, yet "non-Landauer", which predicts the minimum dissipation than can be achieved with the optimal protocol. Our bound is not limited to bit writing process but can assess any operation involving a charge flow through dissipative devices.

The work has been supported by the Research Project "Thermodynamics of Circuits for Computation" of the National Fund for Scientific Research (F.R.S.-FNRS) of Belgium.

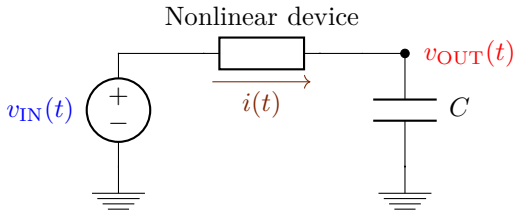

Figure 1. Charging a (possibly non-constant) capacitance through some (possibly nonlinear) dissipative dipole.

In Section II, we define the bit writing operation, first generally and then particularized for a capacitance load, and we present a novel lower bound for the energy dissipation of the process. In Section III we compare our bound with experimental results [4] and simulations of CMOS devices. We show for example that for the chosen parameters, an nMOS pass gate is two decades away from optimality, while a transmission gate is only a factor two over the bound, thereby illustrating the scope of our bound as a benchmark of efficiency. Conclusions are in Section IV.

II. Problem Statement and Main Result

With a view to a large class of nonlinear physical systems made of both dissipative and energy-storing components, we are most generally interested in *charge transfer* from one circuit (referred to as the "input") to another ("output") through a driving device. In the schematic depicted in Figure 1, the charges are supplied by an ideal voltage source while the load is a constant capacitor, for illustrative purposes and without loss of generality at this stage. The transmitting dipole has a finite conductance, thus is *dissipative*, but is otherwise arbitrary: it may be a linear resistor (modelling for instance the path losses) or a CMOS gate.

The storage circuit exploits the charge $q(t)$ as state variable to represent a logical 0 ($q(t) = q_0 = 0$, by convention) or a logical 1 ($q(t) = q_1$, positive). We focus on the bit writing operation, i.e. switching from 0 to 1 through a charge transfer. Our goal is thus to bring a charge Δq on the capacitor in a specified time Δt, however by minimizing the *energy dissipation* as much as possible. The Δt will sometimes be referred to as

write time or *response time* and obviously depends on the input signal $v_{\rm IN}(t)$, the behaviour of the transmission device and on the capacitive load. For a given circuit, an imposed Δt therefore partly determines the properties of the input signal, notably its speed. There might be additional technological constraints restricting the shape of the input signal (maximum supply voltage, finite slew rate,...).

A. Definitions of the Important Physical Quantities

In Figure 1, $v_{\rm IN}(t)$ and $v_{\rm OUT}(t)$ denote the input and output node voltages, respectively, and

$$\delta v(t) \equiv v_{\rm IN}(t) - v_{\rm OUT}(t), \tag{1}$$

the voltage difference across the dipole. Let $i(t)$ be the electrical current flowing through the transmission device. The charge transferred from the input to the output during a time interval Δt is

$$\Delta q \equiv \int_{t_0}^{t_0+\Delta t} \mathrm{d}q = \int_{t_0}^{t_0+\Delta t} \frac{\mathrm{d}q(t)}{\mathrm{d}t}\ \mathrm{d}t = \int_{t_0}^{t_0+\Delta t} i(t)\ \mathrm{d}t. \tag{2}$$

For the special case of a constant capacitance output load (Figure 1), we have $i(t) = C\,\mathrm{d}v_{\rm OUT}(t)/\,\mathrm{d}t$ and

$$\Delta q = C\left(v_{\rm OUT}(t_0+\Delta t) - v_{\rm OUT}(t_0)\right) = C\,V_1, \tag{3}$$

V_1 being the prescribed voltage defining the logic level 1.

It is instructive to carry out the *energy balance* of the circuit. The energy supplied at the input splits, as a result of (1), into two components:

$$E_{\rm IN} = E_{\rm dissip} + E_{\rm bit}. \tag{4}$$

$$E_{\rm bit} = \int_{t_0}^{t_0+\Delta t} v_{\rm OUT}(t)\, i(t)\ \mathrm{d}t \tag{5}$$

is the reversible component of the supplied energy, "profitably" transferred to the storing element. For the special case of the constant C, we of course retrieve

$$E_{\rm bit} = \frac{1}{2}CV_1^2 = \frac{\Delta q^2}{2\,C}. \tag{6}$$

Thereafter, we will most often refer to this quantity (6) as the *bit energy*, following [4]'s terminology.

The *energy dissipation* of the switching operation is

$$E_{\rm dissip} = \int_{t_0}^{t_0+\Delta t} \delta v(t)\, i(t)\ \mathrm{d}t. \tag{7}$$

Only a device with an infinite conductance ($i(t)/\delta v(t) = \infty$) is able to transmit the charges (finite non-zero $i(t)$) while keeping $\delta v(t) = 0$, which would result in $E_{\rm dissip} = 0$ according to (7). This theoretical limit case actually corresponds to a simple lossless (zero resistance) connecting wire between the source and the storing element.

B. Lower Bound for the Dissipation

We may consider a yield coefficient assessing the efficiency of the charge/energy transfer in the circuit of Figure 1:

$$\frac{E_{\rm bit}}{E_{\rm IN}} = \frac{E_{\rm bit}}{E_{\rm bit}+E_{\rm dissip}} = \frac{1}{1+E_{\rm dissip}/E_{\rm bit}}, \tag{8}$$

which approaches 1 as the *loss ratio* $E_{\rm dissip}/E_{\rm bit}$ (dissipation normalized by the bit energy) decreases. The main result of this paper is a general lower bound on $E_{\rm dissip}$:

$$E_{\rm dissip} \geq E_{\rm dissip,min} \equiv \frac{\Delta q^2}{\overline{G}\,\Delta t} = \frac{\left(\int_{t_0}^{t_0+\Delta t} i(t)\ \mathrm{d}t\right)^2}{\overline{G}\,\Delta t}, \tag{9}$$

where

$$\overline{G} \equiv \frac{1}{\Delta t}\int_{t_0}^{t_0+\Delta t} \frac{i(t)}{\delta v(t)}\ \mathrm{d}t \tag{10}$$

may be interpreted as the *average* conductance of the nonlinear driving device over the whole charging time interval. The derivation is proposed in Appendix A, based on Cauchy-Schwarz inequality. The formulation (9) is general in the sense that it does not depend on the output load (whose a constant C is a special important case).

The bound is tight, i.e. the bit writing operation is energetically optimal, if the voltage difference across the nonlinear device is constant (Appendix A):

$$\delta v(t) = \Delta V = \text{constant}. \tag{11}$$

Remarkably, the condition (11) is general in the sense that it does not rely on any assumption regarding the transmission device of Figure 1. It is important to acknowledge that, despite its apparent simplicity, the condition (11) can be hard to translate into a optimal $v_{\rm IN}(t)$ in practical switching circuits exhibiting substantial nonlinearities (see CMOS applications in Section III-B). The shape of the $v_{\rm IN}(t)$ such that (11) is satisfied can indeed be very complex to implement.

For the important special case of a constant output capacitance (see (3)), (9) expands as

$$E_{\rm dissip} \geq \frac{1}{2}CV_1^2\,\frac{2C}{\Delta t\,\overline{G}}. \tag{12}$$

That is, the loss ratio is bounded by the following relation:

$$\frac{E_{\rm dissip}}{E_{\rm bit}} \geq \frac{E_{\rm dissip,min}}{E_{\rm bit}} = \frac{2C}{\Delta t\,\overline{G}}. \tag{13}$$

In (13), the quantity $C/\overline{G}$ reminds us the time constant of a linear RC circuit (discussed in detail below in Section III-A), however extended to a general nonlinear circuit through the definition (10). Equation (13) tells us that the dissipated energy decreases as the write time Δt, whose value is relative to the time constant of the circuit, increases. This trend is the classical speed/dissipation tradeoff [5], [6]. We have provided (10) and (12) to predict the minimum dissipation, as well as the optimal protocol (11) to achieve it.

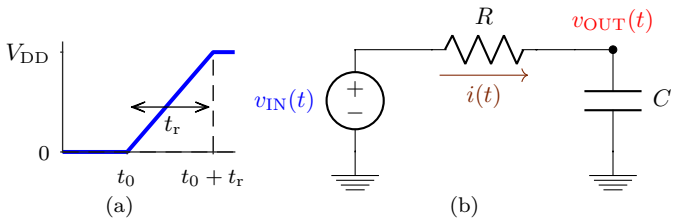

Figure 2. (a) Linear input ramp. (b) Linear RC circuit.

III. Applications

In this section, we exploit our fundamental lower bound to discuss the energy efficiency of several practical switching electronic circuits.

A. Linear RC circuit

The experimental setup of [4], intended to prove that it is possible to write a bit with a sub-kT dissipation, can be modelled as depicted in Figure 2: a constant capacitor ($C = 100\,\mathrm{pF}$) is charged by a voltage ramp through a series resistor ($R = 1.1\,\mathrm{k\Omega}$). Whereas [4] only describes the input signal as "smooth and gradual", we reasonably assume a linear ramp (Figure 2(a)) [5]. We will show that, for the speed regime studied by [4], the exact shape of the signal has a negligible influence on the experimental results.

This preliminary case study can be covered in detail analytically. Subsequently, the *exact* dissipation is computed according to (7), for some response time Δt.

In the most general case, we must distinguish V_1, the voltage defining the logic level 1, from V_{DD}, the *supply voltage* corresponding here to the final amplitude of the voltage ramp. For a non-zero R, we have necessarily $v_{OUT}(t) < v_{IN}(t)$, meaning that $v_{OUT}(t)$ never reaches exactly V_{DD}. V_1 must therefore be suitably defined, for instance as a fraction of V_{DD}, that is $V_1 = \alpha V_{DD}$ with α close to unity. Thus, most generally, the output response time Δt differs from the rise time of the input ramp (t_r): both situations $\Delta t < t_r$ and $\Delta t \gg t_r$ can occur, depending on the choice of α and the speed of the input ramp relative to the RC time constant. If the RC dynamics is negligible, $V_1 \approx V_{DD}$ can be rigorously assumed.

1) Quasi-Static Case: We first focus on the conditions selected by [4] for a sub-kT measurement. We compute $RC = 110\,\mathrm{ns}$, while t_r ranges between $64\,\mu\mathrm{s}$ and $640\,\mu\mathrm{s}$ [4]. The quasi-static condition ("slow" input and "slow" bit writing operation) $t_r \gg RC$ is comfortably verified, which implies that $v_{OUT}(t)$ closely follows $v_{IN}(t)$, with almost no delay. We emphasize that $\delta v(t)$ is small, yet non-zero and measurable (down to the nV [4], [5]). We may consider $V_1 \approx V_{DD}$ ($\alpha \approx 100\,\%$) together with $\Delta t \approx t_r$.

In this speed regime, the exact dissipation can be shown to tightly match the proposed lower bound (12) that takes the simplified form

$$E_{dissip} \approx E_{dissip,min} = E_{bit}\,\frac{2RC}{\Delta t}, \tag{14}$$

since $\overline{G} = 1/R = \text{constant}$. While the lower bound, in a general context (9)(13) as well as in the linear case, is a novel contribution to our knowledge, we should mention that the dissipation in quasi-static conditions (right-hand side of (14)) was already obtained earlier [5]–[8]. Furthermore, we show in Figure 3 that the predictions are in excellent agreement with [4]'s experimental results, up to small discrepancies, which we attribute to the non-idealities of the measurement [4], [5]. The combined experimental, analytical modelling and theoretical prediction efforts comforts us in a major conclusion: although there is no such a thing as "Landauer's $kT\log 2$ bound" to write a bit, there is a fundamental minimum dissipation, precisely given by (14) for an RC circuit in slow conditions. Equation (9) generalizes it for the wide class of nonlinear devices, whose adiabatic logic gates [5]–[8] or conventional CMOS gates are examples.

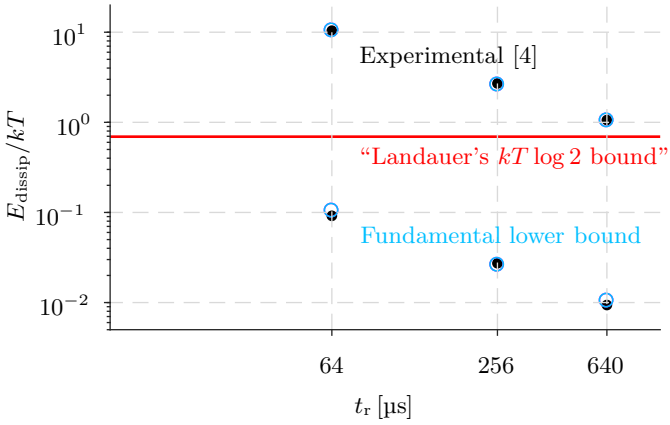

Figure 3. Dissipated energy versus switching time for the RC circuit in quasi-static conditions, two different $V_1 = 500\,\mu\mathrm{V}$ and $50\,\mu\mathrm{V}$ (bit energies are $E_{bit} = 3000kT$ and $E_{bit} = 30kT$, respectively) [4].

2) Faster Bit-Switching Case and Optimal Protocol: We move back to our general problem stated in Section II: given an imposed response time Δt (for v_{OUT} to reach at least V_1) can we find an optimal $v_{IN}(t)$ so as to minimize the energy dissipation? The answer is yes. It can be shown by direct calculation that the *affine* $v_{IN}(t)$ sketched in Figure 4 satisfies the optimality condition (11), where ΔV must be chosen as a function of V_1 and Δt:

$$\Delta V = V_1\,\frac{RC}{\Delta t}. \tag{15}$$

The minimum dissipation (14) is naturally obtained with this optimal protocol. In Figure 5, we compare for different speeds (Δt) the dissipation of the linear ramp (Figure 2(a)) with the lower bound achieved with the affine input (Figure 4). Only the quasi-static regime ($\Delta t \gg RC$) was assessed by [4], [5]. Interestingly, we show, by comparison with the minimum-dissipation pro-

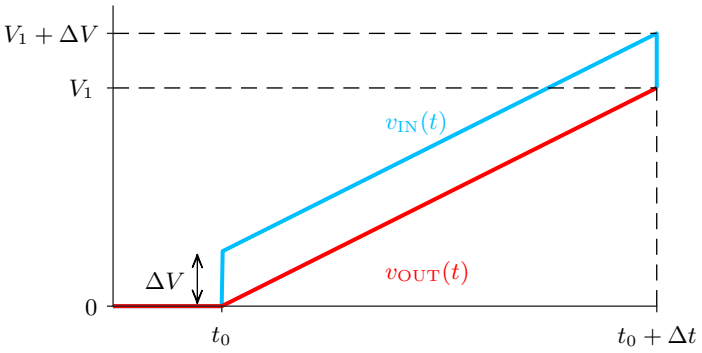

Figure 4. Optimal protocol to achieve the minimum dissipation for the linear RC circuit.

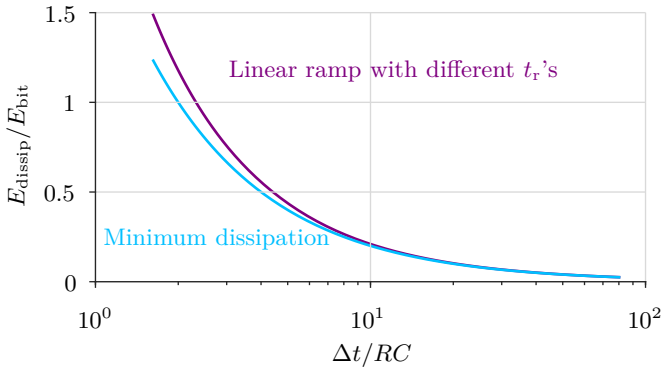

Figure 5. Dissipated energy $E_{\rm dissip}$ versus switching time Δt for the RC circuit at various speeds. The linear input ramp (of fixed amplitude $V_{\rm DD}$ but different $t_{\rm r}$'s.) is compared to the optimal affine protocol. The switching time Δt is here defined at $V_1 = 80\,\%\,V_{\rm DD}$.

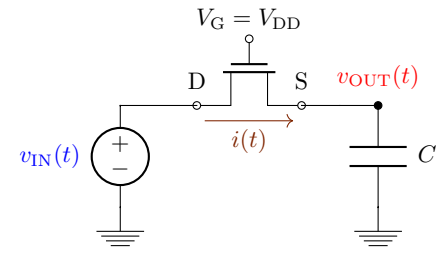

Figure 6. nMOS pass gate driving a capacitor.

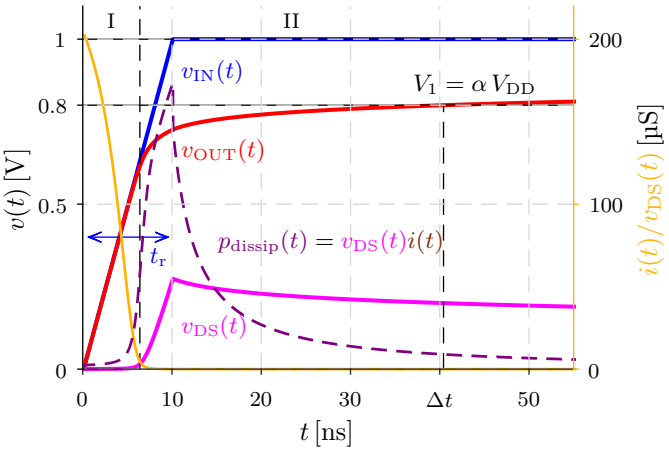

Figure 7. Simulated pass gate: 28 nm FD-SOI regular-$V_{\rm th}$ nMOS of minimal dimensions $L = 30\,$nm and $W = 80\,$nm; $V_{\rm DD} = 1\,$V; $C = 1\,$fF; input rise time $t_{\rm r} = 10\,$ns.
Logical 1 definition (defining the bit-switching time): $V_1 = 80\,\%\,V_{\rm DD}$.
The dissipated power $p_{\rm dissip}(t)$ (in magenta) is plotted in arbitrary units.

tocol, that the linear ramp deviates from optimality as the speed increases.

B. The nMOS Pass gate

The charge transfer process from the supplying input to the capacitive load can be enabled or disabled at will provided that the driving device (abstractly represented by a box is Figure 1) is a controlled switch. This is the primary digital application of the MOS transistor. We will thus firstly study the energy efficiency of the switching operation through an *nMOS pass gate*, which constitutes a realistic and important nonlinear practical case of our lower bound (12) for the dissipation.

A pass gate, implemented with an nMOS transistor, is connected to a constant capacitor in Figure 6. The charging process is ensured by a linear input voltage ramp (as previously sketched in Figure 2(a)) whose rise time $t_{\rm r}$ can vary by several orders of magnitude. $V_{\rm DD}$ is the supply voltage of the used CMOS technology.

For this realistic case, we avoid to resort to a simplified analytical model of the transistor that would be highly inaccurate and unfaithful to the small-dimension effects in the most advanced technologies [9] favoured for digital circuit design [10]. Instead, in the same spirit as [5, Section V], we have performed SPICE simulation in the time domain, compatible with the industrial process design kits. We emphasize that methodology and our main result (9) do not require any analytical model of the studied circuit, even though it was first illustrated for the linear RC circuit.

1) Transient Simulation: The simulated waveforms in switching conditions are depicted in Figure 7, using a colour code consistent with Figure 6. The voltage defining the logic level 1 is $V_1 = 0.8\,$V and the response time Δt is extracted as the time needed for $v_{\rm OUT}(t)$ to reach at least V_1, about 40 ns for the illustrated case. We further observe that the nMOS is incapable to fully pass the logical 1 to be written on the capacitor. Although this behaviour is well known [10], we will revisit and reinterpret it with the introduced notions of instantaneous and average conductances (10) that appears in the minimum-dissipation formula (12).

The nMOS transistor is a strongly nonlinear device, in the sense that the current flowing from the drain (by convention input of the pass gate in Figure 6) to the source (output) is a nonlinear function of its terminal voltage differences ($v_{\rm GS}$, and $v_{\rm DS} \equiv \delta v$), from strong to weak inversion [9]. Consequently, the conductance of the transistor (defined as $i(t)/\delta v(t)$) varies a lot during the bit writing operation. We conceptually distinguish two phases in Figure 7.

In the first (I) phase, the charging process is efficient.

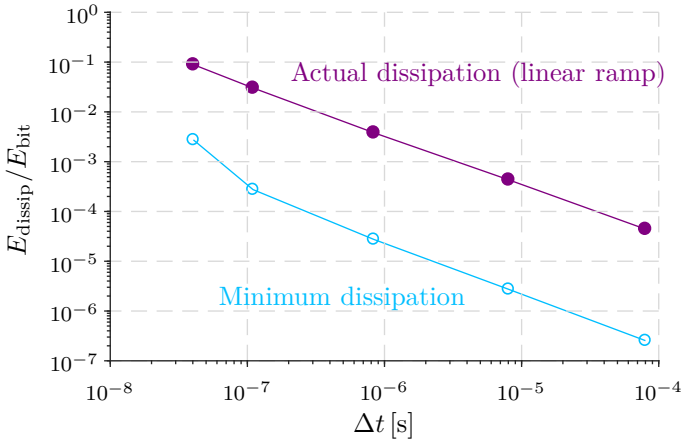

Figure 8. Capacitance bit writing through an nMOS pass gate (same parameters as Figure 7, but different t_r's): dissipation versus response time Δt. All the quantities were extracted from SPICE circuit simulations.

The $v_{GS}(t) = V_{DD} - v_{OUT}(t)$ is large ($\gg V_{th}$, the threshold voltage of the transistor), meaning that the MOS is in *strong inversion* (large conductance $i(t)$). Thanks to the driving capability of the device, $v_{OUT}(t)$ closely follows $v_{IN}(t)$ (similarly to [4]'s experiment on the RC circuit in the quasi-static switching conditions discussed in Section III-A). As long as the $\delta v(t)$ remains small (the transistor is in linear region), the instantaneous dissipated power $p_{dissip}(t)$ is low.

Then, in the second (II) phase, the charge transfer becomes more and more inefficient. The $v_{GS}(t)$ gets close or even below the V_{th}, i.e. the transistor operates in weak inversion (low conductance), and $v_{OUT}(t)$ painfully follows $v_{IN}(t)$ ("the nMOS is not good at passing a 1" [10]). The larger $\delta v(t)$ (see Figure 7) increases the dissipation, which experiences a peak at 10 ns. Although $v_{OUT}(t)$ already reaches more than 60 % V_{DD} in the first phase (while the final objective is 80 % V_{DD}), the second phase of the charging process dominates the energy dissipation of the bit writing operation.

2) Analysis of the Dissipation: In Figure 8, we have plotted the dissipation, extracted from the transient simulations performed for different t_r, as a function of the response time (that must be also be empirically extracted for each t_r). We again observe, this time for the nonlinear MOS device, the trend $E_{dissip} \propto 1/\Delta t$, widely reported for the linear *RC* circuit (see Section III-A and associated references). The fact that the total dissipation is quite high (10 % of the bit energy $CV_1^2/2$ for the fastest case of Figure 7) is attributed to the poor conductance of the transistor in the second phase of the charging process discussed here above.

To the actual dissipation we compare the minimum dissipation of the form (12) (constant capacitance load but general nonlinear driving device). For each simulated case, the average conductance is calculated according to (10) and all the quantities of (12) are then known. We remind that (12) predicts the lowest dissipation that could, in theory, be achieved with the optimal protocol $v_{IN}(t)$ guaranteeing the criterion (11) (not determined in this first paper and left for further work). The discrepancy with the exact dissipation is more than two orders of magnitude which reveals that as of it, the linear profile for $v_{IN}(t)$ results in a highly inefficient switching process in terms of dissipation.

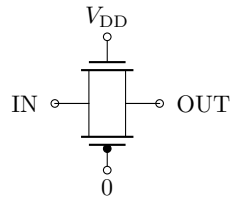

Figure 9. CMOS transmission gate.

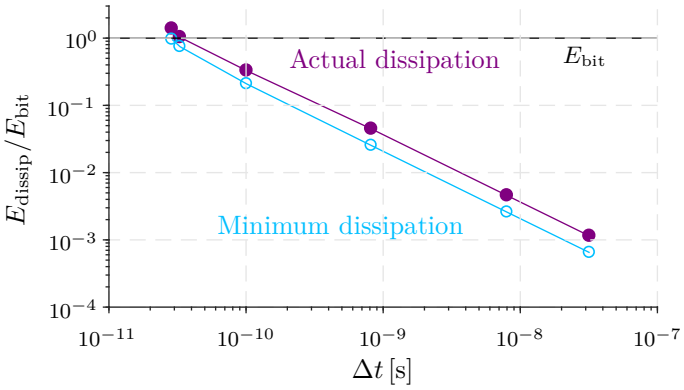

Figure 10. bit writing through a CMOS transmission gate with a linear ramp (same transistor dimensions and parameters as Figure 7; t_r range from 1 ps to 40 ns): dissipation versus response time Δt.

C. The CMOS Transmission Gate

The CMOS transmission gate was introduce to reduce the shortcoming of the pass gate highlighted above, as our bound allows to quantify.

The schematic of the CMOS transmission gate is provided in Figure 9. The complementary pMOS transistor added in parallel with the nMOS overcomes the difficulty of fully passing a logical 1. When $v_{OUT}(t)$ becomes larger than $V_{DD}/2$ and closer to V_{DD}, the conductance of the pMOS increases and it takes over from the nMOS for further charge transfer. Since there is always one of the two transistors which is highly conductive instantaneously, the charging process remains efficient all the way. The bit-switching time is reduced, compared to the single pass gate of Figure 6, and so it the energy dissipation.

The dissipation is depicted in Figure 10 for different speeds. For a response time of $\Delta t = 40$ ns (same as discussed for the nMOS pass gate in Figures 7 and 8), we can find $E_{dissip} \approx 10^{-3}\, E_{bit}$ in Figure 10, i.e. a reduction of the dissipation by a factor 100. When the speed is further increases by using smaller t_r for the linear ramp, the dissipation increases accordingly. There is a minimum

write time $\Delta t \approx 30\,\mathrm{ps}$ for given supply voltage V_{DD} and load C.

The energy efficiency of the CMOS transmission gate is highlighted by our bound (12), also extracted and represented in Figure 10. For all the speed, the ratio $E_{\mathrm{dissip}}/E_{\mathrm{dissip,min}}$ (13) is smaller than 2. Such result is a consequence of the excellent switching capability of the transmission gate, even when the input signal is a simple linear ramp. This gap could be narrowed even further by resorting to an optimal protocol.

Finally, it is interesting to observe that the actual dissipation *exceeds* E_{bit} for the fastest cases, that is the yield of the energy transfer defined in (8) falls below 50 %. This means that of the energy supplied by the input, less than 50 % is stored as a reversible energy in the capacitor whereas more than 50 % are wasted as heat by the transmission gate.

IV. Discussion and Conclusions

Revisiting [4]'s experimental results, we highlighted the fact that the actual dissipation can be computed analytically and tightly matches both the experimental results and the prediction of the novel, "non-Landauer" fundamental bound that we have derived and introduced. We have also addressed the non-quasi-static (fast input) case. Moreover, we investigated realistic CMOS pass and transmission gates, through SPICE simulations that are compared to our theoretical bound. The observed discrepancies are consistent with our knowledge of the MOS transistor behaviour and their limitations. Our fundamental bound can be regarded as a tool to compare the energy efficiency different bit-switching architectures and protocols, even across various technologies and not only CMOS thanks its generality. We hope to provide further application examples in future work, such as diode, quantum dots [11] or adiabatic logic gates [5]–[8].

Moreover, our "non-Landauer" lower bound, in its most general form (9), not dependent on the linear capacitive load: it predicts the energy cost of passing a certain amount of charge in a certain amount of time through an arbitrary dissipative device. Although we have illustrated it on bit writing operation, where the bit is recorded as a voltage level in a linear capacitance, we wish to generalise to arbitrary devices, with multiple inputs and outputs as well as with a dynamic internal behaviour. We believe the port-Hamiltonian framework [12] is suitable toward that goal. Applications could include more complex circuits such as SRAM bitcells (dynamic nonlinear capacitive load).

References

[1] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM journal of research and development*, vol. 5, no. 3, pp. 183–191, 1961.

[2] J. Izydorczyk, "Three Steps to the Thermal Noise Death of Moore's Law," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 18, no. 1, pp. 161–165, 2009.

[3] J. M. Parrondo, J. M. Horowitz, and T. Sagawa, "Thermodynamics of information," *Nature physics*, vol. 11, no. 2, pp. 131–139, 2015.

[4] A. O. Orlov, C. S. Lent, C. C. Thorpe, G. P. Boechler, and G. L. Snider, "Experimental Test of Landauer's Principle at the Sub-$k_{\mathrm{B}}T$ Level," *Japanese Journal of Applied Physics*, vol. 51, no. 6S, p. 06FE10, 2012.

[5] G. L. Snider, E. P. Blair, C. C. Thorpe, B. T. Appleton, G. P. Boechler, A. O. Orlov, and C. S. Lent, "There is No Landauer Limit: Experimental Tests of the Landauer Principle," in *2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO)*. IEEE, 2012, pp. 1–6.

[6] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.-C. Chou, "Low-Power Digital Systems Based on Adiabatic-Switching Principles," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 2, no. 4, pp. 398–407, 1994.

[7] Y. Ye and K. Roy, "Energy Recovery Circuits Using Reversible and Partially Reversible Logic," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no. 9, pp. 769–778, 1996.

[8] M. P. Frank, R. W. Brocato, B. D. Tierney, N. A. Missert, and A. H. Hsia, "Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS ," in *2020 International Conference on Rebooting Computing (ICRC)*. IEEE, 2020, pp. 1–8.

[9] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, ser. The Oxford Series in Electrical and Computer Engineering Series. Oxford University Press, 2011.

[10] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. John Wiley & Sons, IEEE Press, 2010.

[11] C. S. Lent, M. Liu, and Y. Lu, "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling," *Nanotechnology*, vol. 17, no. 16, p. 4240, 2006.

[12] H. Gernandt, F. Haller, T. Reis, and A. J. van der Schaft, "Port-Hamiltonian formulation of nonlinear electrical circuits," *Journal of Geometry and Physics*, vol. 159, p. 103959, 2021.

Appendix A
Lower Bound for the Dissipation

We prove our main result (9) with the *Cauchy–Schwarz inequality*, applied to a special scalar product that is the integral of the product of two functions:

$$\left(\int f(t)\, g(t)\, \mathrm{d}t \right)^2 \leq \int \big(f(t)\big)^2\, \mathrm{d}t \cdot \int \big(g(t)\big)^2\, \mathrm{d}t. \quad (16)$$

Let $f(t) \equiv \sqrt{i(t)/\delta v(t)}$ and $g(t) \equiv \sqrt{i(t)\delta v(t)}$. The direct application of (16) provides

$$\begin{aligned} \left(\int_{t_0}^{t_0+\Delta t} i(t)\, \mathrm{d}t \right)^2 &= \left(\int_{t_0}^{t_0+\Delta t} \sqrt{\frac{i(t)}{\delta v(t)}} \cdot \sqrt{i(t)\delta v(t)}\, \mathrm{d}t \right)^2 \\ &\leq \underbrace{\int_{t_0}^{t_0+\Delta t} \frac{i(t)}{\delta v(t)}\, \mathrm{d}t}_{\equiv\, \Delta t\, \overline{G}} \cdot \underbrace{\int_{t_0}^{t_0+\Delta t} i(t)\delta v(t)\, \mathrm{d}t}_{=\, E_{\mathrm{dissip}}} \end{aligned} \quad (17)$$

We identify the Δq defined in (2) and we rewrite (17) as (9), the main result of this paper.

The Cauchy-Schwarz inequality (thus our lower bound) is *tight* is lower bound if and only if the vectors $f(t)$ and $g(t)$ are collinear, i.e. $\sqrt{i(t)/\delta v(t)} \propto \sqrt{i(t)\delta v(t)}$ or $\delta v(t) = \Delta V = \text{constant}$.