Linearity Enhancement in Asymmetric Self-Cascode Composed by FD SOI nMOSFETs

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***Abstract*—In this paper, the linearity of the Asymmetric Self-Cascode composed by Fully Depleted SOI nMOSFETs is experimentally evaluated, using transistors with different channel lengths. The abnormal (flat) transconductance of this composite transistor is used to promote a linearity enhancement. Disregarding the gain, the minimum harmonic distortion for low-power low-voltage applications has been obtained for the shortest transistor near the source and longest transistor near the drain.**

Keywords—asymmetric self-cascode, channel length, FD SOI nMOSFETs, analog performance, linearity

I. Introduction

The self-cascode structure is a well-known configuration to improve the analog characteristics of MOSFETs and is composed by two transistors in series association with short-circuited gates, operating as a single device [1]. Commonly, both transistors present identical channel doping concentrations and hence, same threshold voltages (V_{TH}). Based on this structure, an alternative configuration has been proposed, named Asymmetric Self-Cascode (A-SC), depicted in Fig. 1, where the transistor near the drain (M_D) exhibits smaller threshold voltage than the transistor near the source (M_S), achieved by the reduction of channel doping concentration [2]. In Fig. 1, L_S and L_D are the channel lengths of M_S and M_D transistors, respectively. The total channel length is given by L_S + L_D, however, since V_{TH} of M_D is lower than M_S, the transistor close to the drain has its channel already inverted for V_{GS} close to V_{TH} of the A-SC structure, diminishing the effective channel length to only L_S [2] under certain bias conditions. This composite transistor promotes larger drain current (I_D) and transconductance (g_m), lower output conductance (g_D) and higher intrinsic voltage gain (A_V) compared with a uniformly doped transistor with equal total channel length [2, 3].

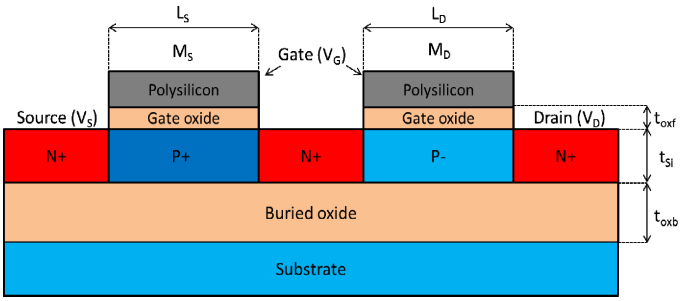

Fig. 1. Asymmetric Self-Cascode structure of FD SOI nMOSFETs.

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Reference [4] presents a study of the channel width influence of M_S (W_S) and M_D (W_D) transistors on the electrical characteristics of the A-SC structure. In this paper, an abnormal g_m has been observed, with a flat region, when W_S is larger than W_D (i.e., M_S resistance lower than M_D resistance). Considering the channel lengths and the transistors resistances, this effect should occur when L_S is smaller than L_D.

An important parameter for analog applications is the harmonic distortion, which corresponds to a modification in the output signal in relation to the input signal, by introducing harmonic frequencies to the fundamental signal. The main figures of merit are the total, second and third order harmonic distortions (THD, HD2 and HD3, respectively) [5]. According to [6], a linearity improvement is achieved for the A-SC structures by using long L_S and L_D due to the increase of A_V. However, since the difference between L_S and L_D is not high, the abnormal and flat g_m has not appeared in these results. The aim of this paper is to assess the harmonic distortion of this composite transistor by varying L_S and L_D, taking advantage of this abnormal and flat g_m.

II. Methodology

The harmonic distortion analysis has been performed with transistors operating as amplifiers, inserting an input signal at the gate terminal (V_{IN}), given by (1), which is composed by a sinusoid with amplitude (V_A=50mV) superposed to the DC component (gate voltage overdrive, $V_{GT}=V_{GS}-V_{TH}$, in order to compensate for the differences among the threshold voltages of the transistors). In (1), $\omega=2\times\pi\times f$ corresponds to the angular frequency, where f is the signal frequency and t is the time [7]. Fig. 2 presents the schematics of the harmonic distortion in the MOSFET, where I_{D1}, I_{D2} and I_{D3} are the amplitudes of the fundamental, second and third order harmonic distortions of the drain current, which compose the output signal.

$$V_{IN} = V_{GT} + V_A \times sin\,(\omega \times t) \quad (1)$$

The integral function method has been used to extract THD, HD2 and HD3 from the DC I–V curves, dispensing the need of AC measurements. This is valid as long as quasi-static operation can be assumed, that is up to about one tenth of the device intrinsic cut-off frequency, given by g_m/C_G where C_G is the input gate capacitance.

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III. Devices Characteristics

The measured transistors have been fabricated in the FD SOI CMOS technology from UCLouvain, Belgium. The single transistors present channel lengths varying from 0.75µm to 10µm and channel width of 20µm. The gate oxide (t_{oxf}), silicon film (t_{Si}) and buried oxide (t_{oxb}) thicknesses are 31, 80 and 390nm, respectively. The M_S transistor features channel doping concentration of about $6\times10^{16}cm^{-3}$, whereas the M_D transistor presents the natural wafer doping concentration in the channel ($1\times10^{15}cm^{-3}$) [8].

IV. Results

Firstly, the DC analysis has been performed to identify the trends by varying L_S and L_D in order to obtain the plateau in g_m. In sequence, the linearity analysis has been carried out.

A. DC Analysis

Fig. 3 presents I_D (A) and g_m (B) as a function of V_{GT} for L_S=0.75µm varying L_D, extracted at V_{DS}=1.5V. One can notice that the increase of L_D reduces I_D and g_m, which is linked to the larger M_D resistance. The impact of L_D on I_D and g_m vs. V_{GT} curves is high due to the lower L_S (smaller M_S resistance).

In Fig. 4, I_D (A) and g_m (B) are presented as a function of V_{GT} for L_D=10µm changing L_S, extracted at V_{DS}=1.5V. It is possible to note that the increase of L_S also reduces I_D and g_m, since the M_S transistor dominates the I_D flow in the A-SC [2]. However, the impact of L_S on I_D and g_m seems to be apparently lower compared with the impact of L_D, which is opposite to the results obtained in [4] when W_S and W_D have been varied. In the present paper, the larger M_D resistance (L_D=10µm) reduces the effectiveness of the impact of L_S on I_D and g_m vs. V_{GT}.

Looking at Fig. 3 and 4, one can verify the anomalous behavior of g_m when $L_S < L_D$, and it becomes more evident as larger L_D in relation to L_S. This feature might be of great interest for nonlinearities analysis when g_m gets rather flat, that might improve the linearity. To understand this anomalous g_m, Fig. 5 exhibits the potential at the intermediate node (V_X) between M_S and M_D as a function of V_{GT} varying L_D with L_S=0.75µm (A) and changing L_S with L_D=10µm (B), obtained at V_{DS}=1.5V. In the case of the A-SC L_S=1.5µm; L_D=10µm (Figure 5(B)), one can see a high V_X at low V_{GT}, which implies a larger g_m. When V_{GT} is incremented, V_X suddenly reduces, diminishing g_m. For larger V_{GT}, V_X stabilizes, in this case, there is an increase of g_m until the moment where the mobility degradation and the similar electron concentrations between M_S and M_D transistors become significant, reducing g_m again, since the effective channel length tends to $L_S + L_D$.

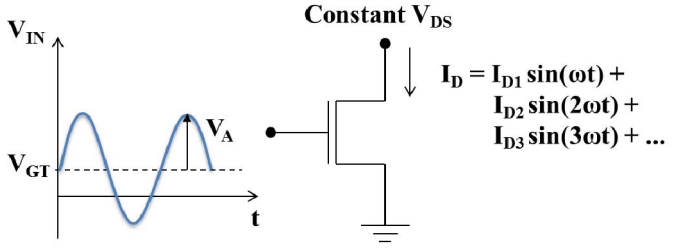

Fig. 2. Schematics of the harmonic distortion in the MOSFET.

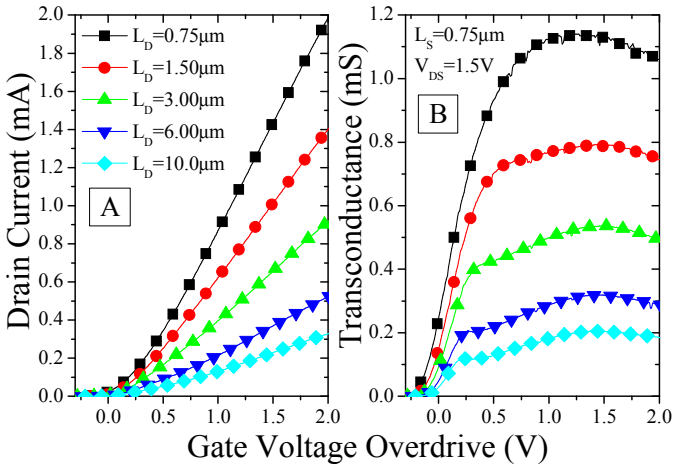

Fig. 3. Drain current (A) and transconductance (B) as a function of the gate voltage overdrive for L_S=0.75µm varying L_D, extracted at V_{DS}=1.5V.

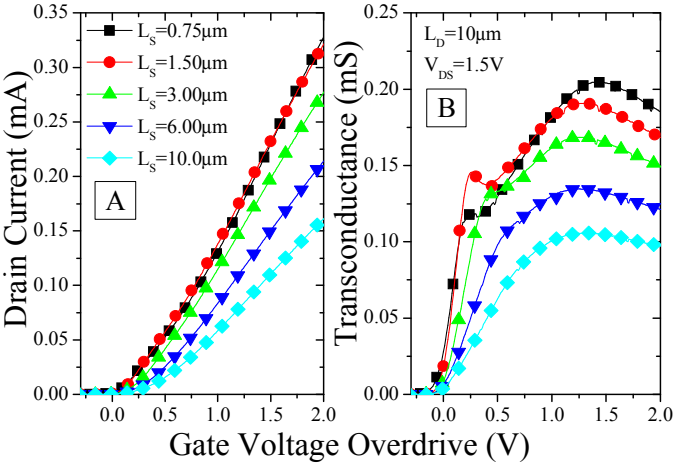

Fig. 4. Drain current (A) and transconductance (B) as a function of the gate voltage overdrive for L_D=10µm varying L_S, extracted at V_{DS}=1.5V.

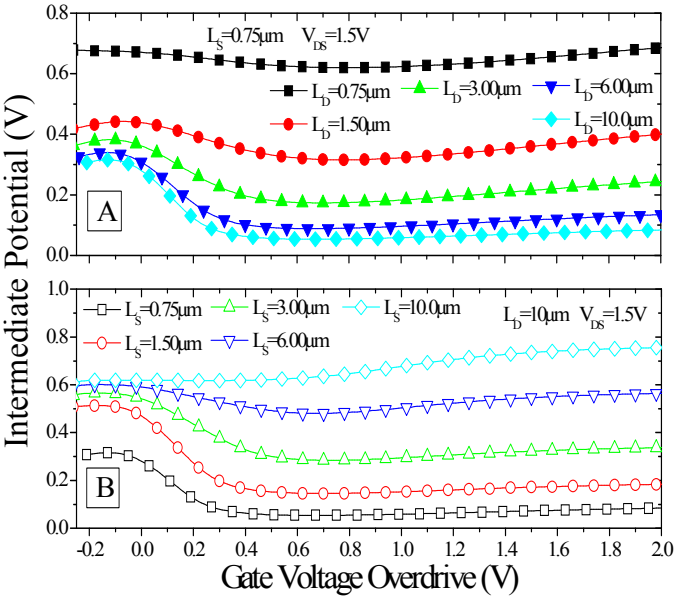

Fig. 5. Intermediate potential as a function of the gate voltage overdrive for L_S=0.75µm changing L_D (A) and for L_D=10µm varying L_S (B), extracted at V_{DS}=1.5V.

With the increase of L_D (Figure 5(A)), the larger M_D resistance reduces the intermediate potential. On the contrary, by incrementing L_S (Figure 5(B)), the higher M_S resistance increments V_X.

The intrinsic voltage gain, given by $(g_m/I_D)\times V_{EA}$, is plotted against L_D (A) and L_S (B) in Fig. 6, extracted at V_{DS}=1.5V and V_{GT}=200mV. One can observe that the increase of L_D increments A_V, but the improvement caused by the increment of L_S is larger, since the M_S device controls the A-SC structure.

B. Harmonic Distortion Analysis

Once the DC analysis has been finished, the next step has been the study of harmonic distortion. Fig. 7 and 8 present THD (A), HD2 (B) and HD3 (C) as a function of V_{GT} for, respectively, L_S=0.75µm varying L_D and L_D=10µm changing L_S. In both figures, THD and HD2 are practically the same, whereas HD3 is around 30dB to 40dB lower than HD2. However, its study is important because HD2 is suppressed in differential amplifiers [5]. Besides that, THD is given by HD3 when the negative linearity peaks are present in HD2.

According to [9] and disregarding the nonlinearity in the output conductance, HD2 is given by (2). The gate voltage overdrive at which the minimum HD2 is obtained is linked to the point of maximum transconductance.

$$HD2 = (1/2) \times V_A \times (dg_m/dV_{GT}) / (2 \times g_m) \qquad (2)$$

When L_D is incremented, the maximum transconductance is displaced to higher gate voltage overdrive (Fig. 3). However, when L_S is increased, the transconductance peaks are obtained at lower gate voltage overdrive (Fig. 4). The same trends occur for the negative linearity peaks in HD2 (Fig. 7(B) and 8(B)).

Based on Fig. 7, it is possible to verify that the increase of L_D promotes a significant improvement in HD2 and THD for V_{GT}<400mV, reducing in 10dB at V_{GT}=200mV, which is very suitable for low-power low-voltage (LPLV) applications. This excellent characteristic is related to the flat g_m as a function of V_{GT}, indicating that I_D vs. V_{GT} curve is more linear at low gate voltage overdrive.

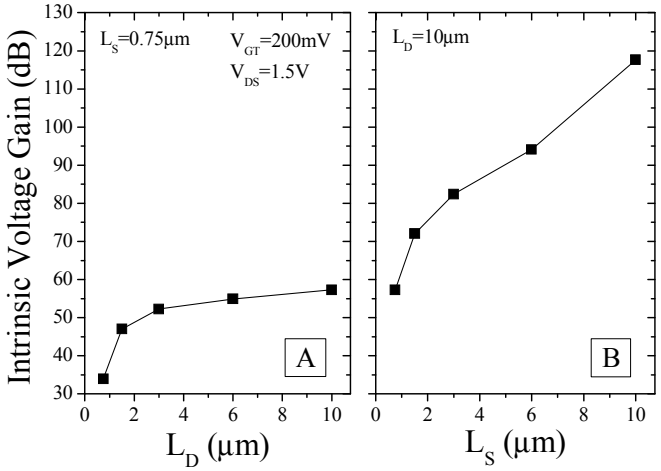

Fig. 6. Intrinsic voltage gain as a function of L_D with L_S=0.75µm (A) and as a function of L_S with L_D=10µm (B), extracted at V_{DS}=1.5V and V_{GT}=200mV.

For V_{GT}>400mV, there is a decrease of HD2 with the reduction of L_D. This feature can be explained by plotting dg_m/dV_{GT} as a function of V_{GT} in Fig. 9. For lower V_{GT}, one can note that the increase of L_D reduces dg_m/dV_{GT} and, consequently, HD2. For higher V_{GT}, dg_m/dV_{GT} maintains practically at same level. However, by looking at Fig. 3, there is a larger g_m when L_D diminishes. This way, based on (2), HD2 is lower when L_D reduces for higher V_{GT}. According to Fig. 7(C), the increase of L_D also reduces HD3 for V_{GT}<700mV, thanks to the lower d^2g_m/dV_{GT}^2.

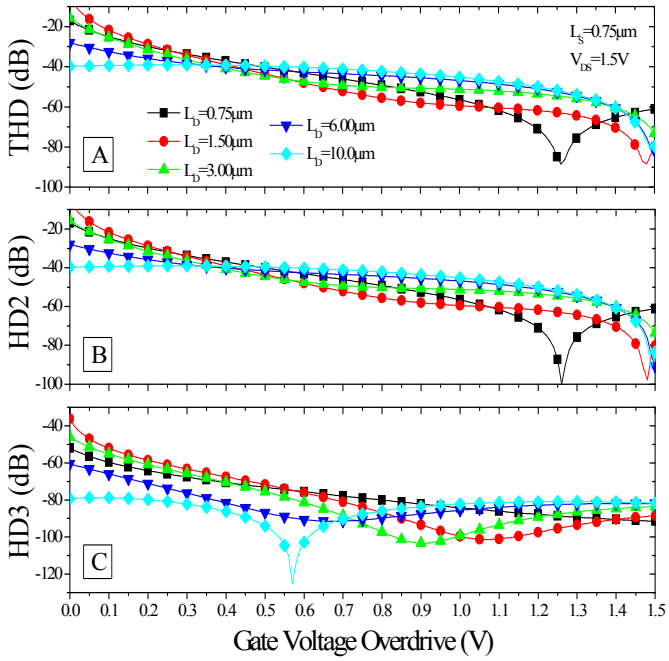

Fig. 7. THD (A), HD2 (B) and HD3 (C) as a function of the gate voltage overdrive for L_S=0.75µm varying L_D, extracted at V_{DS}=1.5V.

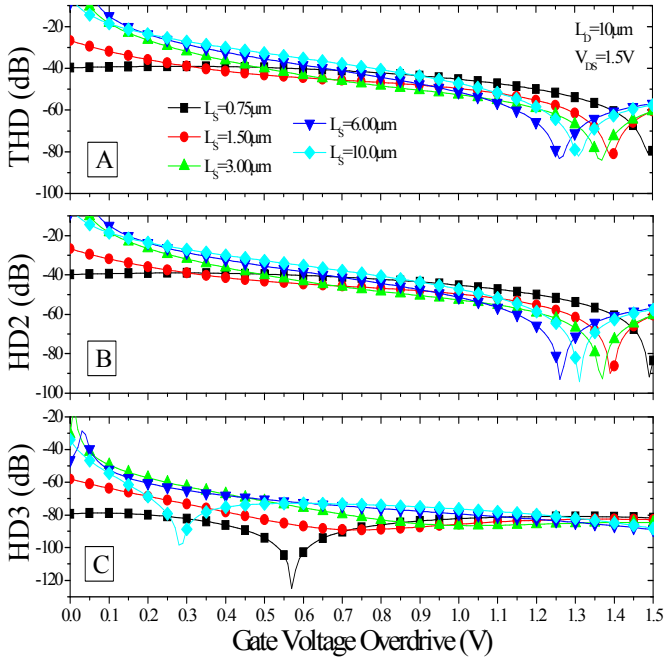

Fig. 8. THD (A), HD2 (B) and HD3 (C) as a function of the gate voltage overdrive for L_D=10µm varying L_S, extracted at V_{DS}=1.5V.

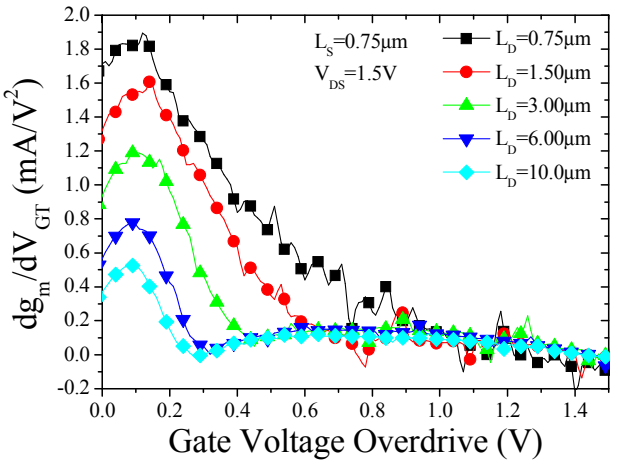

Fig. 9. dg_m/dV_{GT} as a function of the gate voltage overdrive for L_S=0.75µm varying L_D, extracted at V_{DS}=1.5V.

Looking at Fig. 8, on the contrary, the increment of L_S reduces the harmonic distortion for higher gate voltage overdrive due to the more premature negative linearity peak, linked to the point of maximum transconductance. However, for lower gate voltage overdrive, the minimum THD, HD2 and HD3 are obtained when L_S is reduced, since the transconductance becomes flatter.

In order to address the linearity behavior considering the different A_V among the devices, Fig. 10 presents THD/A_V (A), HD2/A_V (B) and HD3/A_V (C) plotted as a function of L_D and L_S, extracted at V_{GT}=200mV and V_{DS}=1.5V. The normalization by the intrinsic voltage gain allows for determining the effective harmonic distortion to obtain the same amplitude in the output signal. According to these results, it is possible to note that the increase of L_D from 0.75µm to 10µm reduces the normalized HD2 and HD3 in 32dB and 39dB, respectively, when the intrinsic voltage gain is taken into account, due to the increment of the intrinsic voltage gain and flatter transconductance.

By incrementing L_S, one can observe a decrease of the harmonic distortion since the intrinsic voltage gain significantly increments with L_S, as indicated in Fig. 6(B). In other words, the positive impact of short L_S in achieving the best linearity disregarding A_V due to the flatter g_m (Fig. 8) is not sufficient to improve the figures of merit of the harmonic distortion when the intrinsic voltage gain is considered (Fig. 10). The normalized THD reduces by 45dB when L_S increments from 0.75µm to 10µm due to the larger intrinsic voltage gain.

V. Conclusions

This paper has presented an experimental analog study of the influence of channel lengths of M_S and M_D transistors on the DC characteristics in order to obtain flatter transconductance and larger intrinsic voltage gain. These features have been used to achieve the best linearity in LPLV applications. It has been observed that the increase of L_D and reduction of L_S have become g_m flatter, improving the linearity. Besides that, an increase of A_V has been noticed with the increment of L_S and L_D. Disregarding A_V, the minimum harmonic distortion for LPLV

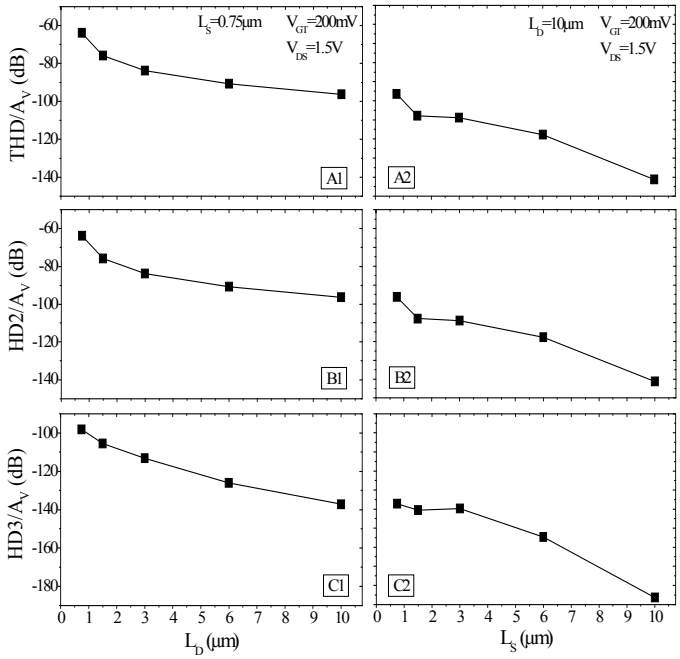

Fig. 10. THD/A_V (A), HD2/A_V (B) and HD3/A_V (C) as a function of L_D (1) and L_S (2), extracted at V_{DS}=1.5V and V_{GT}=200mV.

applications has been achieved for short L_S and long L_D, reducing THD in 10dB at V_{GT}=200mV for the A-SC L_S=0.75µm; L_D=10µm structure comparing with the A-SC L_S=L_D=0.75µm structure.

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