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Scanning probe microscopy study of electronic properties of oligothiophenes thin films

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To my parents

*Avec tout ce que je sais
on pourrait faire un livre.
Avec tout ce que je ne sais pas
on pourrait faire une bibliothèque.
- Sacha Guitry-*

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List of main abbreviations and symbols

μ	Field-effect mobility
k	Dielectric constant
Φ	Work function
σ	Electrical conductivity
σ_{trap}	Density of trapped charge
γ_p	Surface free energy
γ_w	Water surface free energy
AFM	Atomic force microscopy
BCB	Benzocyclobutene
BP	Tetrabenzoporphyrin
BaTiO ₃	Barium titante
BC	Bottom contact
C ₁₀	Decyltrichlorosilane
CP-AFM	Conducting probe atomic force microscopy
CPD	Contact potential difference
C ₆₀	Buckminsterfullerene
C _i	Capacitance
CMOS	Complementary metal oxide semiconductor
CV	Cyclic voltametry
ddOD4T	α -3,7-dimethyldinyloctyl. α' -dodecylquaterthiophene
DOTT	Dioctylterthiophene
DH4T	α , ω - dihexylquaterthiophene
EFM	Electronic force microscopy
$E_{\text{nb/mol}}$	Interaction energy per molecule
E_{mol}	Potential energy of single molecule
E_{bind}	Binding energy
GB	Grain boundary
g_m	Transconductance
HOPG	Highly oriented pyrolytic graphite
HOMO	Highest occupied molecular orbital
IGR	Inter grain region
ITO	Indium tin oxide
I_{dlin}	Linear current

I_{dsat}	Saturation current
$I_{\text{on/off}}$	On-to-off current ratio
KPFM	Kelvin probe force microscopy
LbL	Layer-by-layer
LUMO	Lowest unoccupied molecular orbital
L	Channel length
MOSFET	Metal-oxide-semiconductor field-effect transistor
MFM	Magnetic force microscopy
MoS ₂	Molybdenum disulfide
MIM	Metal-insulator-metal
NSOM	Near-field scanning optical microscopy
OTFT	Organic thin film transistor
OLED	Organic light emitting display
P3HT	Poly (3-hexylthiophene)
PQT	Poly (3, 3'''-didodecylquaterthiophene)
PVAIA	Poly (vinyl acetate)-co-poly(itaconic acid)
PS	Polystyrene
PMMA	Polymethylmethacrylate
PVA	Poly (vinyl alcohol)
PVP	Poly (vinyl phenol)
P α MS	Poly (α -methylstyrene)
PCFF	Polymer consistent force field
R_s	Source resistance
R_c	Total contact resistance
SAM	Self-assembled monolayer
Sm	Smectic phase
STM	Scanning tunneling microscopy
STS	Scanning tunneling spectroscopy
SiO ₂	Silicon dioxide
TEM	Transmission electron microscopy
TC	Top contact
UHV	Ultra high vacuum
UPS	Ultraviolet photoemission spectroscopy
V_d	Drain voltage
V_g	Gate voltage
V_{th}	Threshold voltage
W	Channel width
wt	Weight percent
XRR	X-ray reflectivity

Overview of the Thesis

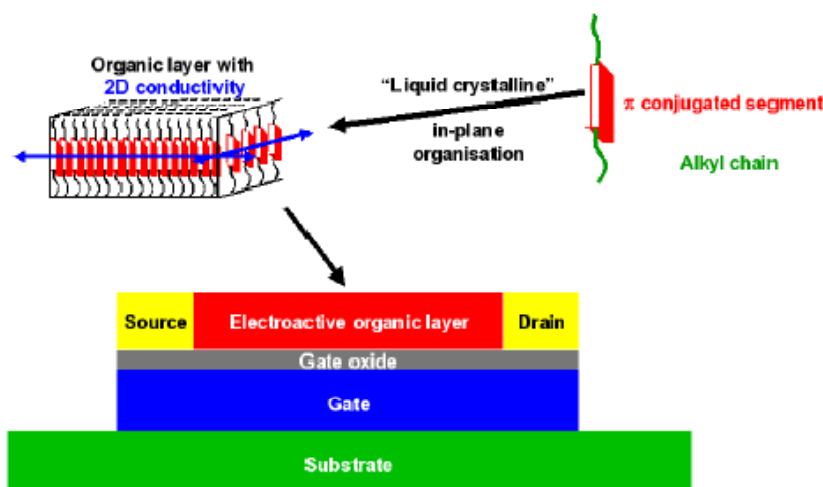
Organic semiconductors have been studied since the early 1950s, and the large amount of work devoted to them allowed a better understanding of their charge transport properties. Major progresses have been made over the recent years in terms of transistor performance due to their potential applications in cheap, flexible, and large area electronic devices, e.g. low cost information displays on mechanically flexible plastic, logic for smart cards and radio-frequency identification tags (RFID). For the realization of such devices, field effect transistors (FETs) are essential.

Among the potential organic semiconductor materials, conjugated oligomer-based ones such as oligothiophenes and thiophene derivatives with alkyl side chains have shown promising high field-effect mobilities. In fact, the electrical properties of these conjugated oligomers are essentially controlled by molecular order. For example, the performances of FET based on sexithiophene (6T) have been improved by a factor of nearly 50^[1] by controlling the molecular ordering in the evaporated film, from the short-range ordered 3-dimensional (3D) structure to a well-organized 2-dimensional (2D) arrangements. Indeed, long-range ordering in films of molecular materials can be achieved by controlling the experimental conditions during film deposition, such as substrate temperature and the rate of deposition of the precursors. Such highly ordered molecular systems provide charge carrier mobilities well above that of amorphous silicon, namely $\mu_{\text{sat}} > 1 \text{ cm}^2/\text{Vs}$ ^[2,3].

Within the extensive range of the oligothiophenes, alkyl-substituted oligothiophenes have attractive electrical properties compared to the non-substituted ones; easier processability of the material, enhanced performance of the devices ^[4,5,6]. In this type of organic materials, the conduction mechanism involves charge transport across π - π stacked molecules. High charge mobility thus requires conjugation along the main molecular axis and favorable molecular stacking (Scheme 1). Moret et al ^[6] demonstrated that the presence of a typical herringbone (zigzag pattern of V-shaped) organization in non-substituted oligothiophenes, minimizes the repulsion between π orbitals and favors π - π interactions between neighbor molecules. However, dialkyl-substituted oligothiophenes

Overview of the Thesis

are one of the most promising *p*-type organic materials as they are able to self-assemble in close packed crystalline structures. This property favors the mobility while their solubility in common organic solvents favor their processability.



Scheme 1 Schematic diagram of a FET device with an active semiconducting organic layer. The conjugation and the π - π stacking direction are fast charge transport directions.

Since the carrier mobility of solid organic semiconductors critically depends on the molecular order and on the π - π interactions, a thorough understanding of the structural properties in the condensed phase of α , ω - dialkyl terminated oligothiophenes is mandatory. Nevertheless, the conditions for growing highly crystalline thin films and fabrication of such crystalline structures requires complicated machinery. Furthermore, large area production is rather difficult and complicated and would require large and expensive vacuum systems. Previous studies show that, a more attractive way leading towards cheap, simple and large area

electronics is processing from solution, for example by drop-casting, spin-coating or inkjet printing. Such procedures call for soluble organic semiconductors that at the same time exhibit good intermolecular order to minimize charge carrier scattering and in this way to guarantee high transistor performance. However, working with soluble compounds considerably adds complexity in terms of self-assembly and morphology. It is important therefore, to understand the interplay between chemical structures, solubility, self-assembly, and the resulting device performance in order to gain powerful tools for the realization of high performance organic electronic compounds. Hence, understanding the structure formation i.e, the growth process, and finding ways to optimize the structural definition is a prerequisite for technological progress in acquiring the basic functional properties of OTFTs.

In a previous research program supported by the Wallonia Region realized in collaboration with the ULB and the UMH, the synthesis and the processing of new alkyl-substituted oligothiophene molecules was developed. Studies of the structure, morphology of thin films of those molecules and macroscopic electrical properties of transistors based on them were realized. It was observed, among other, that the substrate surface modification of the silicon substrates with silanes enhances the electrical performances of FET based on these molecules.

However, the origin of this performance enhancement was unclear. Also the microscopic electronic properties of the molecules and of the transistors were not characterized, at all. In this respect, this thesis is devoted to the thorough characterization and understanding of the relationship between the structure, the substrate surface treatment and the electronic properties of organic liquid crystalline molecules (alkyl-substituted oligothiophenes) in both their crystalline and liquid-crystalline phases, especially to the "in-situ" characterization of the potential distribution and charge trapping effects in the channel of OTFTs based on these molecules. The

microscopic data obtained are correlated to the macroscopic performances of the OTFTs. Attempts were also made to improve the transistors performance by using a nanocomposite gate dielectric based on polyvinylalcohol charged with silica nanoparticles. To reach these goals, the main techniques used in this project were Scanning Tunneling Microscopy and Spectroscopy (STM/ STS) to characterize the electronic properties (energy levels and band structure) of individual molecules and Kelvin Probe Force Microscopy (KPFM) to characterize the voltage distribution in FET fabricated with those molecules on both inorganic and organic dielectric layers.

The first chapter of this manuscript is a literature survey and is divided into five parts. The first one presents the organic semiconductors from different points of view such as electrical classification, structural classification and architectures. The second part briefly introduces and discusses gate dielectrics and their properties. The third and four parts briefly explain the charge transport mechanisms in OTFTs and device parameter extraction. The last part of this chapter is devoted to give an overview on some of the most convenient scanning probe microscopy techniques which are used to study electronic properties of either individual molecules or thin-films of TFT devices.

In chapter 2, we report on the STM and STS study of the structure and electronic properties of self-assembled monolayers of oligothiophene molecules. In particular, the molecular arrangements of two different alkyl-substituted oligothiophenes, α,α' -dihexylquaterthiophene (DH4T) and α,α' -dioctylterthiophene (DOTT), in monolayers on molybdenum disulfide (MoS_2) were studied with a joint theoretical / experimental approach. Scanning tunneling microscopy (STM) was used both at the liquid/solid interface and in dry conditions to investigate the ordering of the conjugated oligomers in two-dimensional layers. The electronic

property of individual molecules in DH4T and DOTT monolayers was also studied using STS spectroscopy. Charge carrier transport in OTFTs mostly occurs within few monolayers of semiconducting thin-film, close to the gate dielectric surface. Thus, it could be of interest to first study the molecular arrangement and electronic properties of monolayers based on the mentioned molecules and second, to study the structure and electronic properties of the thin-films of these molecules in OTFT devices.

Chapter 3 is devoted to the Kelvin Probe Force Microscopy (KPFM) study of Organic Thin-Film Transistors (OTFTs) on both modified and unmodified SiO₂ gate dielectrics. The organic transistors were made based on three alkyl-substituted oligothiophenes which were already introduced in previous chapters i.e. DH4T, DOTT and ddOD4T molecules. After attempting to optimize the thickness of the active layers, to make them suitable for performing KPFM measurements via modifications in thin-film preparation process, the morphology and local electronic properties of devices under operation were investigated by AFM and KPFM, respectively. Different parameters such as V_g -dependency, V_d -dependency, hysteresis and charge trapping effects were studied and are reported.

Finally, chapter 4 presents a study on DH4T-based OTFTs using polymer gate dielectrics with and without embedded nanoparticles. We adopted poly (vinyl alcohol) (PVA) as a gate insulator using a spin-coating method for the OTFTs. We put our efforts on the preparation and characterization of the PVA layers with and without the SiO₂ nanoparticles. The surface properties of nanocomposite gate dielectrics were studied by means of contact-angle and roughness measurements while the dielectric properties were characterized via capacitance and leakage-current measurements within metal-insulator-metal (MIM) structures. Furthermore, the performance of OTFTs was investigated by electrical measurements and KPFM microscopy.

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** Chapter 1 **

Introduction

1.1 Organic semiconductors

The most important component of an organic thin-film transistor (OTFT) device is the semiconductor being used as active layer. Thus, the establishment of correlations between molecular structure and solid-state organization, film morphology and electrical performance is of great interest to the organic electronics community. The particular purpose of this section is to study these branches. First, some elementary conditions that π -conjugated materials should fulfil in order to enable decent OTFT performance are reminded below:

- As the most efficient charge transport occurs along the direction of intermolecular π - π stacking, the molecules should be oriented with the long axes perpendicular to the TFT substrate.
- At reasonable applied electric fields charge carriers should be able to be injected into the channel of TFT. This implies that the highest occupied molecular orbital (HOMO)/ lowest unoccupied molecular orbital (LUMO) energies of the individual molecules be at levels where holes/ electrons can be injected. Some examples are shown in Table 1.1.
- Efficient charge transport between the adjacent molecules occurs via the overlap of frontier orbitals. The crystal structure of the material should thus allow sufficient overlap.
- The material should be extremely pure since impurities act as charge traps.

Chemical structures of some of the most representative organic semiconductors and three alkyl-substituted oligothiophene molecules employed in this work are shown in Fig.1.1 and Fig.1.2, respectively. DH4T has been widely studied as active layer in organic transistors due to its good carrier mobility ^[1]. DOTT was employed as active layer, with the goal of exploiting its liquid crystalline attributes and self-assembly to render high quality devices. ddOD4T provides a good solubility and also deliver a liquid crystalline character at RT.

The liquid crystalline property was expected to provide better semiconducting characteristics related to the absence of grain boundaries, known to act as charge carrier traps ^[2].

1.1.1 Electrical classification

Organic semiconductors present a large range of carrier mobility ranging from 10^{-5} to 10^1 cm^2 / Vs . As can be seen in Fig.1.3, these values place the organic semiconductors far below the MOSFET technology based on silicon. However, they have already surpassed the amorphous silicon by one order of magnitude and have crossed the threshold of commercial applications ^[3].

Generally, OTFT devices show either p-type or n-type conductivity depending on the organic semiconductors used in their architectures. A p-type (n-type) material is one in which holes (electrons) are more easily injected than the other species. In particular, they are characterized by a high ionization potential (electron affinity). Most organic semiconductors are p-type semiconductors. The reasons of this imbalance observation lie in two facts.

First, n-type organic semiconductors tend to oxidize when exposed to oxygen. Second, the hydroxyl groups present at the surface of SiO_2 act as traps and immobilize electrons at the semiconductor-dielectric interface ^[5].

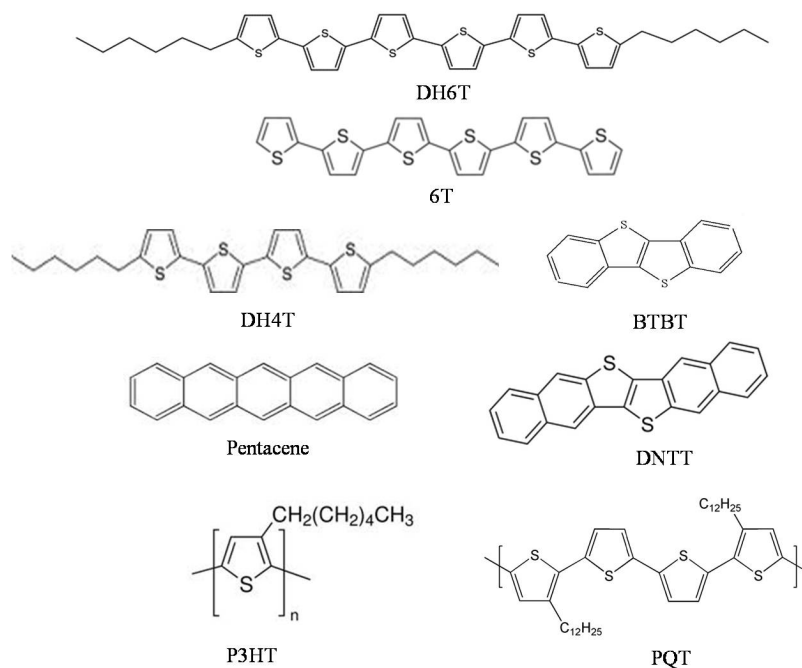


Figure 1.1 Chemical structures of some of representative organic semiconductors [from top to bottom, left to right]: dihexylsexithiophene (DH6T), sexithiophene (6T), α , α' -dihexylquaterthiophene (DH4T), [1]benzothieno[3,2-b][1]benzothiophene (BTBT) –pentacene, dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), poly (3-hexylthiophene) (P3HT) and poly (3,3'''-didodecylquaterthiophene) (PQT).

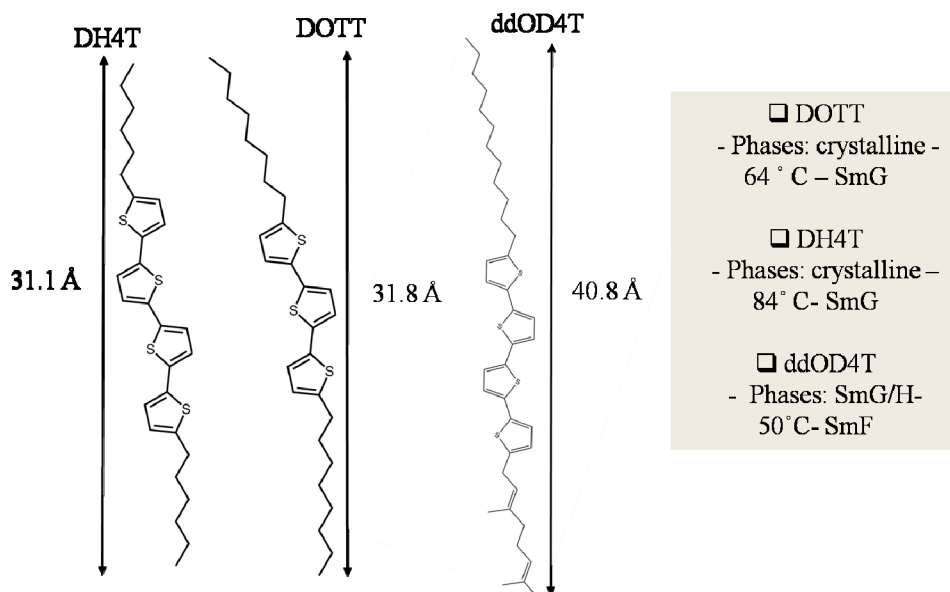


Figure 1.2 Chemical structures and first liquid crystalline phase transition temperature of α, α' -dihexylquaterthiophene (DH4T), dioctylterthiophene (DOTT) and α -3,7-dimethyldienyloctyl- α' -dodecylquaterthiophene (ddOD4T) molecules which have been studied in this work.

Further, in order to inject electrons, normally low work function metals such as calcium or magnesium should be employed since the LUMO level of organic semiconductor lies around 3 eV (see Tab.1.1) but the problem is, on one hand that these metal electrodes are not environmentally stable; and on the other hand, p-type materials still reach better mobilities even when proper low work function electrodes are employed in combination with n-type species.

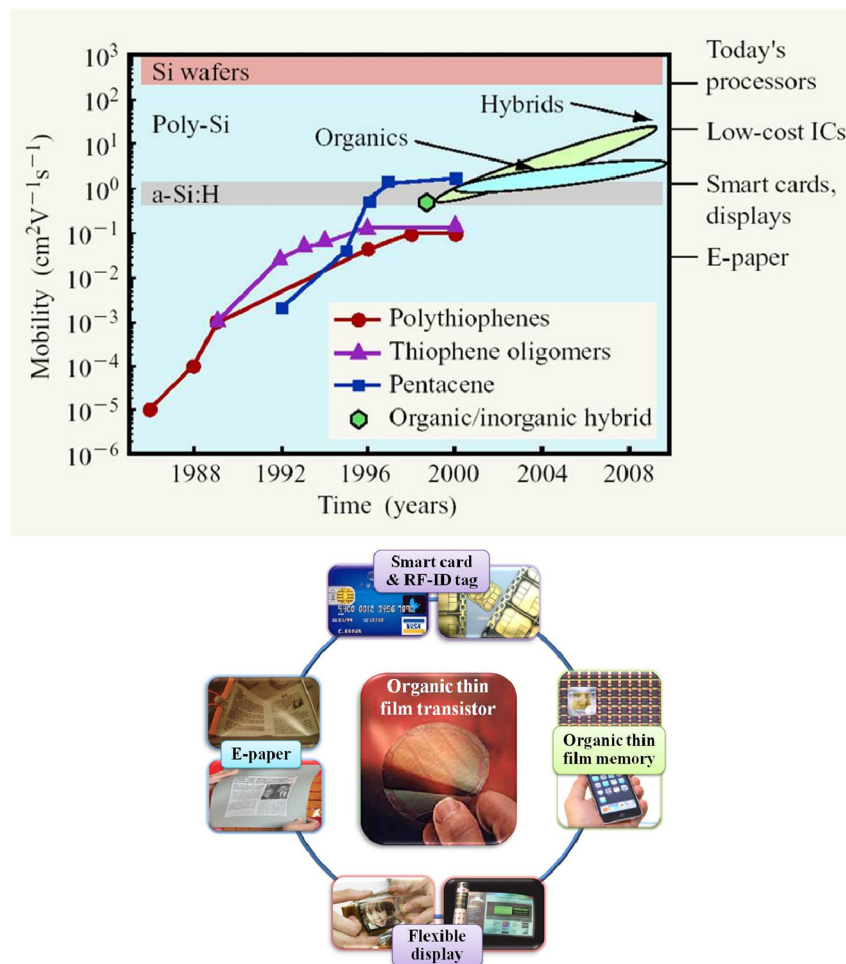


Figure 1.3 Evolution of OTFTs performance with time for organic and inorganic semiconductors (up); a number of low-cost and large-area electronic applications of OTFTs (down). (top graph from ^[4])

Table 1.1 Approximate HOMO / LUMO energies for some representative organic semiconducting materials. Here, CV stands for cyclic voltametry and UPS for ultraviolet photoemission spectroscopy. diperfluorohexylcarbonyl-2,2': 5',2'': 5'', 2'''-quaterthiophene (DFHCO-4T), 6, 13-bis(triisopropyl-silylethynyl)-pentacene (TIPS-PEN) and [6,6]-phenyl-C₆₁-butyric acid methyl ester (PCBM). Note that the fluorinated quaterthiophene derivative exhibits ambipolar transport. (From ^[6])

Organic semiconductor	HOMO (eV)	LUMO (eV)	Technique	Reference
P3HT	4.9	2.7	CV	[5]
PQT	5.2	2.9	CV	[7]
DH4T	4.9	-	UPS	[8]
DFHCO-4T	6.3	4.0	CV	[9]
Pentacene	5.0	3	UPS	[10]
TIPS-PEN	5.3	3.5	CV	[11]
PCBM	6.1	3.7	UPS	[12]

Nevertheless, n-type channel OTFTs are needed because they can have several applications in the fabrication of complementary inverters, ring oscillators and shift registers for radio-frequency identification tags and complex circuits. Fullerene derivatives ^[13] and perylene tetracarboxylic diimide compounds ^[14] which have delivered field-effect mobilities up to 5 and 2.1 cm²/ Vs, are examples of performant n-type semiconductors.

1.1.2 Structural classification

Organic semiconductor materials primarily consist of carbon, hydrogen and oxygen. Various classes of organic semiconductors such as small molecules, oligomers and polymers have been used in OTFTs applications depending on their chemical structure. In these materials, common feature of π -conjugated bonds and weak Van der Waals interactions between the adjacent molecules/polymer chains

Introduction

are observed; in contrast to inorganic semiconductors which present strong covalent bonds. Hereafter, each category will be addressed based on increasing the complexity.

Small molecules: This class of compounds is characterized by a well-defined molecular weight. Small-molecules deposited through *vacuum sublimation* have led to an increase of internal order which further delivered higher field effect mobilities. Single crystals of pentacene ($35 \text{ cm}^2 / \text{Vs}$)^[15] and rubrene ($20 \text{ cm}^2 / \text{Vs}$)^[16] are examples of such compounds with remarkable performance. However, *precursor route*^[17] and *side-chain substitution*^[18] are the other synthesis approaches designed to be compatible with solution deposition of small molecules.

Compounds formed by connecting rings along an imaginary line and composed of a few and fixed monomer units, are called oligomers and also belong to the small molecules' family. An important class of heterocyclic linear oligomers are the alkyl-substituted thiophene oligomers like dihexylquaterthiophene (Fig.1.1). Large π -conjugation lengths extending along the long molecular axes and molecular packing along the short molecular axis (π -stacking), are of the main features of these rod-like rigid molecules. As an example, sexithiophene derivatives in top-contact OTFT configuration have shown mobilities up to $1.1 \text{ cm}^2 / \text{Vs}$ ^[19]. However, one of the drawbacks of these electron-rich oligomers is their easy oxidation (doping) in air because of their HOMO energies. This problem, also observed in polymer family, then causes bulk conductivities and on-to-off current ratios which usually do not exceed 10^4 .

Polymers: The semiconducting properties of conjugated polymers allow achievement of a range of electronic and optoelectronic devices. These compounds (two examples depicted in Fig.1.1) with an alternating single and double bonds provide the processing advantages of plastics as well as the semiconductors' optoelectronic

properties. They are generally solution processed and devices based on them have developed in both performance and reliability as a result of a variety of different factors such as:

- Availability of polymer materials with lower density of chain defects, better chemical purity and higher molecular weights.
- Better understanding of thin-film microstructure which helps a better control of the polymer process; and realizing requirements for gate dielectric and source / drain contacts which play the role of forming an active layer with semiconducting layer and injecting charges, respectively.
- Advancement in more controlled solution and printing-based device manufacturing processes.

In order to have high-performance solution-processable polymer semiconductors, two different approaches have considered. In the first approach, the aim is to achieve high mobility by designing the material to induce *microcrystalline* ^[20] or *liquid-crystalline* ^[21] order by self-organization or by specific interactions with a templating substrate. The second approach tries to attain a uniform path for charge transport, along which carriers face with a minimum degree of site energy fluctuations, through establishment of completely *amorphous* microstructures. In spite of the fact that usually higher mobilities are achieved from the first approach, impressive device performance based on triarylamine compounds (10^{-3} - 10^{-2} cm² / Vs) combined with good operating, environmental and photo stability have recently been demonstrated with second approach.^[22]

1.1.3 Architectures

In the fabrication of OTFTs, two main architectures are frequently applied: the *top contact* and the *bottom contact* configurations. The physical difference between the two is the order of fabrication steps. Namely, the source / drain contacts can be deposited before or after the semiconductor layer to create bottom or

top contact devices, respectively. There is also another possibility to build the entire transistor on top of the semiconductor layer such that the insulator and gate contact are successively deposited on top of either of two contacts or semiconductor layer. This configuration is called top gate architecture. All four of these architectures are shown schematically in Fig.1.4.

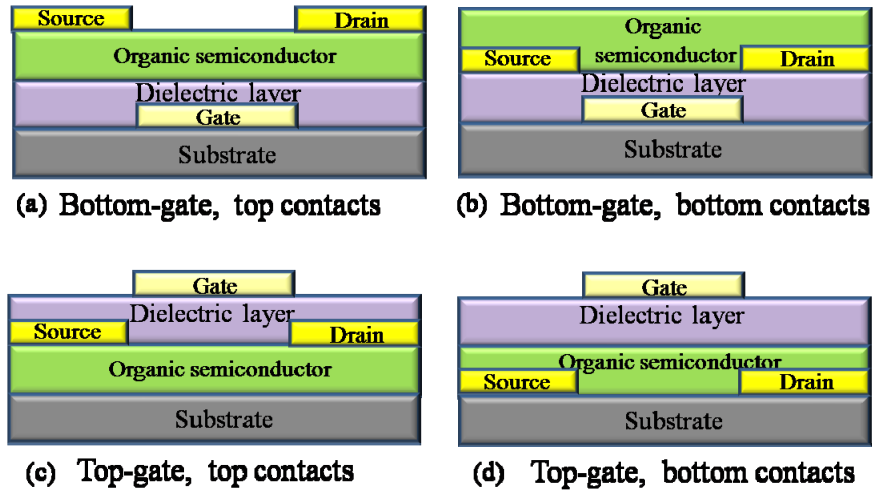


Figure 1.4 Cross-section of possible OTFT architectures, including (a) top contacts, (b) bottom contacts, (c) top contacts with a top gate, and (d) bottom contacts with a top gate.

As the metal-semiconductor contact area in top-contact configuration (Fig.1.4 a) is increased, OTFTs based on this geometry exhibit lower contact resistance.¹ In this case, the major contribution

¹ In traversing an OTFT channel from source to drain, charges are (1) injected from source contact into the semiconductor channel; (2) transported across the length of the channel; and (3) extracted from the channel into the drain. These

to contact resistance is the *access resistance*. The origin of the access resistance is explained by the fact that charge carriers should pass the way from the source contact on top of the film down to the accumulation layer (the channel) at the semiconductor-insulator interface and then back up to the drain contact to be extracted. Therefore, the thickness of the organic semiconductor layer should not be too large in order to minimize the access resistance. Nevertheless, some researchers believe that the access resistance can be ignored in top contact devices because the contact metal penetrates the film down to the accumulation layer (perhaps due to large peak-to-valley roughness of the semiconductor film or the nature of the process of metal deposition) ^[23]. Bottom- contact configuration (Fig.1.4 b) provides some advantages with respect to the top-contact devices. That is, access resistance is not an issue anymore since the contacts are in the same plane as the OTFT channel. Moreover, very small channel dimensions ($W, L < 10 \mu\text{m}$) can be patterned on the insulator using conventional photolithography. However, a limitation of this configuration is the nonideal film morphology often seen in the vicinity of contacts. It has been reported in the literature ^[24] that organic semiconductor grain sizes are very small near the contacts, reasonably due to heterogeneous nucleation phenomena.

Concerning the two top-gate OTFT architectures (Fig.1.4 c and 1.4 d), both configurations face two additional concerns i.e. the top surface roughness of the semiconductor where the channel forms and the establishment a stable interface between the insulator and the top of the semiconductor layer. For example, deposition of top insulator material via solution method may damage the underlying

processes can be roughly thought of as three resistors in series. The resistances associated with charge injection and collection steps can be grouped into the “contact resistance”, while the resistance associated with crossing the channel length in the semiconductor is termed the “channel resistance”. In an ideal OTFT, the source and drain contacts are ohmic, meaning the value of the contact resistance is negligibly small in comparison with the electrical resistance of the semiconductor (i.e., the channel resistance).

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semiconductor film. Furthermore, care must also be taken regarding the alignment of the top gate contact with respect to the channel. It should be ensured that the gate electrode reaches completely the entire length (L) of the device. Any misalignment of the gate electrode cause additional contact resistance as a result of ungated semiconductor regions at one or both of the contacts. However, with the two top-gate architectures, one can preferably choose the top-contact/ top-gate configuration (Fig.1.4 c) because bottom-contact/ top-gate devices suffer from contact resistances².

Several methods, described hereunder, have been used or may be used to characterize and measure the contact resistances present in OTFTs.

Extrapolation of device resistance to zero channel length: In this method, several pairs of source and drain contacts with different channel lengths but constant width (W) on the same semiconductor film are fabricated. One can measure the total OTFT resistance and makes a plot of resistance versus channel length (R vs. L). Linear extrapolation of the plot to $L = 0$ eliminates the channel resistance and gives the contact resistance as the y-intercept. Although the technique is straightforward to perform and understand, it has two disadvantages. First, it requires the fabrication and testing of several devices in order to obtain R vs. L plot, it could be annoying. Second, the contact resistance obtained by this method combines the individual source and drain resistances together.

² Besides the access contact resistance, there are also other types of resistances originating from the device configuration such as: channel sheet resistance which is related to the lateral decay of doping (charge) concentration; geometrical spreading resistance which is related to the shape of the electrodes and the overlap resistance which results from the source/drain overlap with the gate.

Gated Four-Probe Measurements: This technique provides more information than the R vs. L approach by separating the individual contributions of the source and drain contacts. It utilizes two narrow voltage-sensing electrodes, located between the source and drain electrodes and slightly extended into the channel. During the OTFT electrical characterization, voltage-sensing electrodes sense the channel potential at the two probe positions (V_1 , V_2) without passing any current. In the linear regime of the device operation, the potential versus channel position profile is then plotted. The presence of the contact resistances at the source and drain electrodes results in a smaller than expected slope of the profile. Hence, by linear extrapolation between V_1 and V_2 , the profile is estimated and finally the individual source and drain contact resistances are calculated by dividing the voltage drops ΔV_s and ΔV_d by the source-drain current, respectively. The limiting point of this approach is that the extrapolated channel potential profile will only be valid for linear regime of OTFT operation, where the channel potential profile can be expected to be linear and uniform.

Kelvin Probe Force Microscopy: This technique can be used to determine the source and drain contributions to the contact resistance, directly while the previously described techniques required extrapolation of measured data in order to calculate the contact resistance. This technique will be explained in more details at the end of this chapter. A collection of experimental OTFT contact resistance values are shown in Table 1.2, as an example.

Introduction

Table 1.2 OTFT contact resistance values: solution deposited polymers and oligomers. poly-9, 9'-dioctyl-fluorene-co-bithiophene (F8T2) and [6,6]-phenyl-C₇₁-butyric acid methyl ester (C₇₀-PCBM). (TC: top contact; BC: bottom contact; R_s : source resistance; R_c : total contact resistance.)

Semiconductor	Contact metal	TC/ BC	$R_c(\Omega\text{cm})^b$	Method	Ref.
P3HT	Polymer films (<i>p</i> - channel)				
	Au	BC	1×10^4	R vs. L	[25]
	Au	BC	$R_s < 5 \times 10^3$	KFM	[26]
	Ag	BC	$R_s = 2 \times 10^4$	KFM	[26]
	Cr/Au	BC	$R_s = 2 \times 10^4$	KFM	[26]
F8T2	Au	BC	$R_s = 1 \times 10^7$	KFM	[26]
	Cr/Au	BC	$R_s > 7 \times 10^7$	KFM	[26]
C ₇₀ -PCBM	Soluble oligomer (<i>n</i> -channel)				
	Au	BC	$\sim 1 \times 10^6$	R vs. L	[27]

1.2 Gate dielectrics

Organic thin-film transistors typically operate in accumulation mode^[28]. Thus, for a *p*-type semiconductor, holes are induced at the gate dielectric/semiconductor interface by applying a negative gate bias and form an accumulation layer or channel. The main part of the required voltage to create this channel is determined by the capacitance of the dielectric. Considering the simplest gate dielectric i.e. a vacuum or air interface, the charge induced on the semiconductor is $Q = CV = (\epsilon_0 A/t) V$, where ϵ_0 is the permittivity of vacuum, A is the area and t is the distance between the electrode and

the semiconductor. In the case of a material such as SiO_2 used as the gate dielectric, the induced charge for a given voltage is $Q = CV = (K\epsilon_0 A/t) V$, where K is the dielectric constant of the material.^[29] In order to reduce the voltage required to induce the same amount of charges in the semiconductor, one can increase the capacitance, C , through increasing the dielectric constant, K , or reducing the film thickness, t . Achieving an optimal dielectric film requires the optimization of these two parameters, K and t .

1.2.1 Parameters affecting the dielectric constant

The dielectric constant of a material is a measure of its polarizability in response to an electric field. The charge reorganization which can be in the form of interfacial or space charge motion, ionic motion, dipolar motion and electronic motion can cause this polarizability. In the case of materials for organic transistor applications, electronic and ionic polarization will primarily be responsible for dielectric polarizability. There are several parameters which can have a decisive role in dielectric constant of a material including:

- *Thickness*: In order to increase the capacitance of a dielectric material, the thickness can be decreased. However, the reduction of the thickness is subject to the limitation of acceptable leakage currents, effective insulation of the gate and sufficient dielectric breakdown strength. As the dielectric films get thinner, the potential for pinhole defects increases because the interfaces are very close. This, further, leads to larger leakage currents. Indeed, the organization of the film is really important in order to achieve the thinnest dielectric film. With this respect, successful efforts have been done to produce ultrathin self-assembled monolayer films based on densely packed alltrans aliphatic chains.^[30,31]
- *Roughness*: It is believed that the dielectric roughness can reduce the mobility in OTFTs due to the disorder induced in

the accumulation layer. Roughness disturbs π - π stacking, which is important for efficient charge transport ^[32]. An increase of grain boundaries and the irregular channel geometry in rough films can reduce the mobility up to 98% for pentacene TFTs by varying the gate dielectric from normal SiO₂ on Si (rms: 1.7 nm) to SiO₂ over rough TiW (rms: 92 nm) ^[33].

- *Film morphology*: The dielectric film morphology is as important as of the film morphology in device performance. Grain boundaries in a dielectric film can also serve as leakage pathways and polycrystalline films can have microscopic variations in K ^[34].
- *Dielectric-semiconductor interface*: Optimizing the performance of OTFTs can be ensured by controlling the chemistry and physics of the dielectric-semiconductor interface. The importance of the dielectric-semiconductor interface is well described in the study of Chua *et al* ^[5]. They found that removing the interface traps can reveal n -type behaviour in organic semiconductors already thought to show only p -type conduction. This result suggests that the semiconducting properties of an organic material are highly governed by the nature of the dielectric and semiconductor interface.
- *Processing*: Development of organic electronics industry as an inexpensive and easy to organize technology require “ease of processing” and manufacturing processes that avoid expensive and massive lithography patterning steps ^[35]. In this sense, solution-phase deposition methods which are compatible with printing techniques would be highly desirable. So far, several solution-phase process have been developed such as dip-coating ^[36], spin-coating ^[22b] and layer-by-layer (LbL) ^[37] deposition.
- *Reliability*: Preservation of the dielectric integrity during the shelf-life and operation-life of devices is another factor which helps to achieve useful devices. Charging of the dielectric,

modifications in dielectric constant/resistivity over time are a number of typical dielectric failure mechanisms. It has been shown for e.g. that the dielectric constant and resistivity of hygroscopic dielectrics like PVA ^[38] can be affected by humidity.

1.2.2 Major classes of dielectric materials

This section presents the standard dielectric materials including two major classes of inorganic and polymer dielectrics that have been used for TFT applications.

- *Inorganic dielectrics:* One of the standard and well-known dielectric is SiO₂, which is frequently grown as an amorphous thermal oxide on top of silicon. As a benchmark, it has excellent insulating properties due to its large bandgap (8.9 eV) and thermodynamic stability. The basis of complementary metal oxide semiconductor (CMOS) technology is formed by the system of Si and SiO₂ ^[34,39]. However, in spite of its excellent dielectric properties SiO₂ is not adoptable for flexible applications and is not easy to print or solution process. Alternative approaches have been considered to overcome this problem and attempts have been done to use ultra-thin anodized SiO₂ ^[40], ultra-thin SiO₂ on alumina ^[41] and silica nanoparticles ^[37] as gate dielectric materials compatible with flexible substrates and potentially solution processable. Higher *K* dielectrics materials are being considered with respect to the SiO₂ limitations. Although OTFTs based on SiO₂ with a thickness to 10-12 nm have been fabricated, they suffered from large leakage currents. It was then supposed that higher *K* materials could provide equivalent performances using thicker films and thus be attractive alternatives of SiO₂. Several different high-*K* materials have been employed ^[34] and some representative examples are listed in Table 1.3. According to the table, TiO₂

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has a very high dielectric constant. This permittivity is due to strong contribution to polarization from soft phonons involving titanium ions ^[34, 42]. However, TiO₂ films tend to have high defect densities that create high leakage paths and thus limit its application as a useful dielectric. Methods have been employed to incorporate TiO₂ into composite and layered dielectrics using SAMs and surface treatments in order to decrease the leakage current in TiO₂ ^[43,44]. But overall, the good dielectric quality of inorganic oxides in most cases requires vacuum processing combined with high temperatures and sputtering deposition. This issue highlights the requirement of finding alternatives such as the use of organic dielectrics which are also compatible with flexible OTFTs.

Table 1.3 Dielectric properties for common inorganics. Aluminium oxide (Al₂O₃) and tantalum oxide (Ta₂O₅).

Dielectric	K	Thickness (nm)	Capacitance (μF/cm ⁻²)	Leakage (Acm ⁻²)	Ref.
SiO ₂ (standard)	3.9	300	0.01	10 ⁻⁷	[34]
SiO ₂ (thin)	3.9	2.1	1.6	0.1	-
TiO ₂	80	8-12	6-34	High	[34]
Al ₂ O ₃	9	4.8	1.7	10 ⁻⁸	[34]
Ta ₂ O ₅	26	5-6	4-5	<1	[34]

- *Polymer dielectrics:* Polymers have the advantage of being solution processable and usually applied via dip-coating or spin-coating methods. They are flexible and show no special challenge in manufacturing flexible devices. These features make them to be considered as a second major class of materials selected as gate dielectrics for OTFT applications. Common polymers such as polymethylmethacrylate (PMMA)

and polystyrene (PS) are some of the early polymers studied due to their ready availability^[38,9,45]. However, these films suffer from the low capacitances which made them less attractive than other polymers. Poly (vinyl alcohol) (PVA) and poly (vinyl phenol) (PVP) are two of the most extensively used polymer dielectrics for organic electronics applications^[46,47,48,49]. One of the main advantages of using these two polymers is their ability to be deposited as top gate dielectric on an organic semiconductor because of the wide range of solvent systems for these materials. In particular, the solvent systems for PVA and PVP are water and ethanol, respectively which are orthogonal to the semiconductor common solvent. Moreover, for further improvement of robustness of these dielectrics one can use cross-linking agents such as melamine-co-formaldehyde^[48,50] or hexamethylene tetraamine. Fully organic TFTs have been produced and reported in the literature^[47] by using photolithography and oxygen plasma etching processes. Some common examples of polymers used as gate dielectric are depicted in Table 1.4.

Introduction

Table 1.4 Dielectric properties for common polymers. Poly (vinyl alcohol) (PVA), polymethylmethacrylate (PMMA), polystyrene (PS), poly (vinyl phenol) (PVP), divinyltetramethyldisiloxane- bis(benzocyclobutene)(BCB), cyanoethylpullulan (CYEPL) and cyclic transparent optical polymer (CYTOP).

Dielectric	K	Minimum thickness (nm)	Capacitance (nF/cm ²)	Leakage (Acm ⁻²)	Ref.
PVA	10	500	17.8	--	[38]
PMMA	3.5	160	19.5	--	[51]
PS	2.6	122	19	10 ⁻⁴ -10 ⁻⁷	[9]
PVP	6.4	450	7.4	10 ⁻⁷	[50]
BCB	2.65	50	47	~10 ⁻⁵	[52]
CYEPL	12	1200	--	High	[46]
CYTOP	2-2.1	430-700	4.4-2.7	~10 ⁻⁶	[53]

There are also other alternative gate dielectric approaches which will be briefly discussed hereafter:

- *Anodization of thin-metal films:* It is one of the convenient strategies to fabricate TFT devices using the SiO₂-heavily doped Si systems. In order to transfer this concept to flexible systems, attempts have been done to combine gate electrode with gate dielectric via sputtering thin-metal films, subsequently followed by an anodization process. Several groups have reported on the fabrication of anodized alumina/aluminum^[43], titanium oxide/ titanium^[54] and tantalum oxide/tantalum^[40] combinations as gate dielectric/gate metal systems. For example, tantalum metal films have been sputtered onto Si substrates and anodized to produce ~50 nm thick amorphous tantalum oxide (Ta₂O₅) films^[40]. TFTs based on this system and dihexylquinquithiophene (DHQT) as active layer showed *p*-channel mobilities of 0.02- 0.04 cm² V⁻¹s⁻¹.

- *Surface treatment of inorganic materials:* The use of organic monolayers or thin polymer films, to modify the surface of inorganic dielectric materials, can improve the performance of OTFT devices. Researchers in 3M have reported that the use of alkyl phosphonic acid monolayers as SAMs, enhance the mobility in pentacene on alumina TFTs up to $2\text{-}3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ ^[55]. Surface treatment also enhanced the mobility and threshold voltage of pentacene and C_{60} on SiO_2 OTFTs. Alkyl, alkylamine and fluoroalkyl silanes were used to modify SiO_2 ^[56]. Polymers have also been employed as modifiers to decrease the dielectric roughness and thus to improve the TFTs performance. In a research study of evaporated pentacene-based OTFTs, smooth, rough (roughened through reactive ion etching) and PS-coated (thickness of 10 nm) SiO_2 dielectrics were compared. Saturation mobilities increase from 0.02 to 0.31 and $0.94\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ on rough, smooth and polymer-coated SiO_2 , respectively ^[57].
- *Self-assembled monolayers:* As mentioned above, SAMs are used to modify the properties of insulators. They can also be considered as a monolayer dielectric under careful preparative conditions. Vuillaume's group was the pioneer of using this approach ^[30,58]. They used alkyltrichlorosilanes as monolayer insulators in metal insulator silicon structures. Si was covered by a thin native oxide layer (1-1.5 nm). Although the leakage currents for thin SiO_2 (thickness below 3 nm) are $10^{-3}\text{-}10^{-1}\text{ A/cm}^2$, applying octadecyltrichlorosilane as a monolayer, reduced the leakage current by five orders of magnitude down to 10^{-8} A/cm^2 ^[58]. This was achieved by controlling the *order* of monolayer film by keeping the temperature below a critical value during the solution deposition. It was found that having an all *trans* structure for alkyltrichlorosilane films, is imperative in order to decrease the leakage current.
- *Nanocomposite and nanostructured gate dielectrics:* A suitable gate dielectric for flexible organic thin-film

transistors is not easily obtained with a single material. The use of multilayers containing different materials allows making a balance between the strengths and weaknesses of individual polymer and inorganic materials. Particularly, high-K insulators offer excellent dielectric constants, but suffer from poor interfaces with organic semiconductors. Instead, polymer dielectrics generally have low capacitances, but outstanding film-forming properties. Several efforts have been done to blend ceramic and polymeric materials of the nanoscale with the aim of producing nanostructured dielectrics with desirable properties. The general approach has been to fill a polymeric material with high capacitance nanoparticles. Table 1.5 presents some examples of different composite materials studied in the literatures recently.

For instance, Su and co-workers^[59] used the sol-gel method to synthesis bismuth titanate nanoparticles within a polyacrylate matrix. The size of the nanoparticles was around 50 nm and an effective dielectric constant as high as 10 was obtained; but detailed characterization of the matrix was not explained further. In another study, TiO₂ nanoparticles were embedded in PVA^[60]. TiO₂ nanoparticles were dispersed in aqueous solution of PVA with poly (melamine-co-formaldehyde) and the solution was spun onto the substrate. The film preparation process ended with heating the substrate in order to cross-link the polymer. Although a modest increase of the dielectric constant was obtained for 600- nm thick films, pentacene-based TFTs using this composite exhibited high mobilities ($> 0.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) and reasonable on/off ratios around 10^3 . Threshold voltage was measured to be $\sim -7 \text{ V}$ which is reasonably high, suggesting the presence of static charge at the dielectric-semiconductor interface.

Another report described the combination of commercially available barium titanate nanopowders with

PVA and PVA-co-poly (vinyl acetate)-co-poly (itaconic acid) (PVAIA) in aqueous solutions ^[61]. The dielectric constants obtained was around 11-12, but the amount of loaded barium titanate was not reported. Pentacene-based devices using these gate dielectrics, showed low threshold voltages (-0.8-1.2 V) and high mobilities ($\sim 0.4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$). However, the higher dielectric constant films (~ 12) showed somehow lower mobility than films with lower dielectric constant (~ 9).

In the case of polymeric nanocomposite gate dielectrics, the control of the nanostructure of polymer/dielectric material by controlling the chemistry between the nanoparticles and the dielectric is another important issue. Researchers at Bell labs have characterized core-shell nanostructured dielectric material precisely, in 2005 ^[44]. They used narrowly dispersed anatase phase TiO_2 nanoparticles in PS. TiO_2 nanoparticles had rod-shape with the size of $\sim 15 \times 4 \text{ nm}$ and $K=31$. PS was synthesized by atom transfer radical polymerization and its end was functionalized with a phosphonate moiety in order to bind strongly to TiO_2 . The combination of TiO_2 and phosphonate-terminated PS resulted in a narrowly dispersed core-shell architecture revealed by dynamic light scattering. Pentacene- based TFTs using these gate dielectrics which showed dielectric constant of ~ 8 , had high mobilities up to $0.2 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$ and on/ off ratios of about 500 for unpatterned devices. The presence of TiO_2 nanoparticles in the gate dielectric decreased the break down voltage from $> 100 \text{ V}/\mu\text{m}$ for neat PS to $\sim 25 \text{ V}/\mu\text{m}$ for 18 vol % films.

Table 1.5 Dielectric properties of nanoparticle-based dielectrics.

Material	K	Thickness (nm)	Capacitance (nF/ cm ⁻²)	Ref.
BaTiO ₃ -PVA	9-12	170	62.5	[61]
TiO ₂ - PVA	5.4	600	--	[60]
TiO ₂ - PS	8.2	870	8	[44]
SiO ₂ -PDDA LbL	6	300	--	[37]

1.3 Charge transport

Charge transport in organic semiconductors cannot be described by the common “band-model” which refers to the mechanisms occurring in crystalline inorganic solids such as metals and semiconductors^[62]. The main reason of the failure of this model in the interpretation of charge transport mechanisms in organic semiconductors, is not considering a crucial phenomenon i.e. polarization in these materials. The polarization phenomenon happens in organic semiconductors as follows: A charge carrier residing on a molecular site tends to polarize its neighboring region. This polarization cloud can move with the charge so that the travelling entity cannot anymore be considered as a naked charge and it will be a “dressed” charge. This formed species is called a *polaron*. In conjugated solids, the main polarization effect is that of the clouds formed by the π -electrons. In this sense, an acceptable description of charge transport in organic semiconductor materials can be based on the Holstein concept^[63] of small-polarons. However, additional models have been proposed:

- *Band-like transport*: This model has been applied for delocalized carriers in ultrapure single-crystals such as rubrene and polyacenes at low temperatures^[64]. The problem with this model is the ultimate value of the mobility and its temperature dependence which need to be resolved^[65,66].
- *Hopping*: This model is generally used to characterize the amorphous polymers in which thermally activated charges hop through a distribution of localized states^[67]. The barriers generated by energetic disorder can be overcome at high temperatures which improves transport by providing the required energy for charge carriers. An Arrhenius-like law: $\mu \sim \exp(-\Delta/k_B T)$ has often been used to fit the temperature dependency. Δ denotes the activation energy which increases with the amount of disorder^[68]. In the case of semicrystalline polymers which have less random structures and contain partially crystalline lamellae loaded in an amorphous matrix, the charge transport is most likely controlled by grain boundary effects^[69]. Although the exact mechanism is not yet understood, it is probable that the band-like transport occurs within the ordered lamellae layers while hopping takes place within the disordered intergranular material.

1.3.1 Trap-controlled transport

Organic thin-films are generally polycrystalline and sometime even amorphous. Thus, they include extrinsic defects which can dominate the charge transport. On a time average, the charge carriers are multiply trapped by and released from trap states associated with the defects which leads to an effective mobility, μ_{eff} .^[70,71] On that basis, “*trap-controlled band*” and “*trap-controlled hopping*” transport models can be employed to describe the conduction mechanisms in defect-assisted devices. Both models are similar to each other. In both scenarios, the principle is thermal activation to a transport level.

The simplest case is to consider transport in extended states and localized states with a fixed trap depth, e.g. due to a specific chemical impurity. According to the mobility edge picture (Fig. 1.5 (a)), increasing the degree of disorder in a solid influence the spectral density of trap states. The discrete trap levels which may exist in a crystal are smeared out as disorder increases. The mobility edge position (line between hatched and white area in Fig. 1.5 (a)) depends on the degree of disorder. At high levels of disorder, localization extends well into the energy bands. At the mobility edge, the mobility as a function of energy increases, abruptly, as shown in Fig.1.5 (b).

For the simple case of traps with a discrete energy E_t and a density N_t , the low temperature approximation of the effective mobility is given by equation (1):

$$\mu_{eff} \approx \frac{n_f}{n_t} \mu_0 = \frac{N_c}{N_t} \exp\left[-\frac{(E_c - E_t)}{KT}\right] \mu_0 \quad (1)$$

In “trap-controlled band transport” model, n_f and n_t respectively are the density of free- and trapped-electrons and μ_0 is the intrinsic mobility. N_c and E_c are the density of extended states and corresponding energy of these states, respectively. In this case measuring the mobility as a function of temperature reveals the trap depth $E_c - E_t$.^[53]

In the “trap-controlled hopping” transport model the effective mobility can be written as equation (2):

$$\mu_{eff} \propto \frac{N_H}{N_t} \exp\left[-\frac{(E_H - E_t) + E_b/2}{KT}\right] \quad (2)$$

N_c in equation (1) is replaced by the density of hopping sites, N_H , at the energy E_H . If the activation energy of the hopping process $E_b/2$ is

known, the trap depth, $E_H - E_t$ can be estimated from equation (2). For example, the depth of 0.26 eV with an activation energy of 0.14 eV of discrete traps in inorganic As_4S_4 has been estimated with this approach.^[72]

Charge carrier traps within the organic semiconductors can be caused by different origins (factors) such as structural defects, chemical impurities, gate dielectric and water adsorption. Extended structural defects such as edge dislocations or grain boundaries can result in significant defect densities in organic crystals, e.g. 10^{19} cm^{-3} ^[73]. In addition, the chemical nature of the gate dielectric, water adsorbed on its surface and the polarity of the gate dielectric can influence the charge transport.

OTFTs often exhibit a current hysteresis (difference between the forward and the reverse sweeps). In addition, there is often a persistent shift of the transfer characteristics when a gate bias is applied for a prolonged time. These phenomena are known as electrical instability or gate bias stress effects. Trapping of charges in long-lived trap states causes the electrical instability. The term “long-lived” refers to a trapping and release time which is long compared to the time needed to measure a transfer characteristics or a surface potential profile (e.g. 1 min). The shift of the transistor characteristics (threshold voltage shift) ΔV_t can be used to estimate the surface density of long-lived traps according to equation (3):^[74]

$$\tilde{N} = \frac{C_i \Delta V_t}{e} \quad (3)$$

The long-lived trap states may be extrinsic in nature (e.g. certain chemical groups on the surface of the gate dielectric)^[74] or resulted from structural defects within the semiconductors.

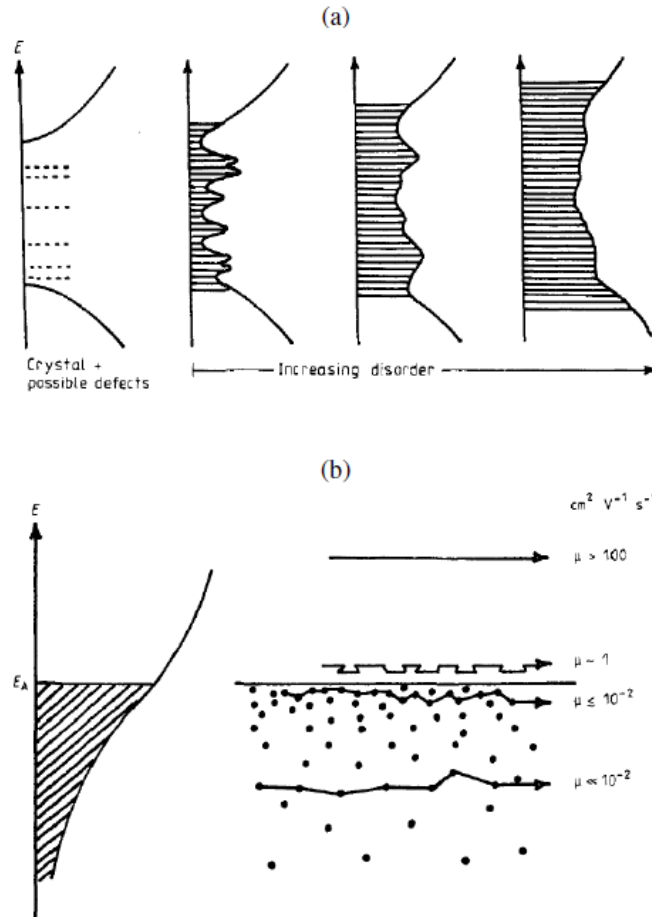


Figure 1.5 Influence of increasing disorder on the band structure of a solid. The hatched areas mark localized states, i.e. the spectral density of trap states. As disorder increases, the width of discrete trap levels (left) increases and, eventually, the discrete trap levels are completely smeared out (right). In addition, more and more states become localized. (b) Schematic representation of the mobility edge. The mobility edge separates localized states (hatched area) from extended states. At the mobility edge, the mobility as a function of energy abruptly rises. (From ^[53])

Subthreshold swing, S , is another important device parameter which could be a measure of deep trap density according to equation (4). This parameter is a measure of how easily a transistor can be switched from the off-state to the on-state.

$$S = \frac{KT \ln 10}{e} \left[1 + \frac{e^2}{C_i} N_o \right] \quad (4)$$

In this equation, both deep bulk traps and the interface traps contribute to N_o (unit: $\text{cm}^{-2}\text{eV}^{-1}$). The lower limit of the subthreshold swing is obtained with $N_o = 0$. At $T = 300\text{K}$, this lower limit is ≈ 60 mV/dec. In other word it is impossible to measure a subthreshold swing steeper than 60 mV/dec in a field-effect transistor.

In conclusion, charge transport in organic semiconductors is influenced by various factors such as: morphology of the organic semiconductor, presence of defects at the organic semiconductor/insulator interface and diffusion of gas molecules from the ambient exposure. Charge trapping (investigated by KPFM in chapter 3), molecular reorientation and dipole formation at the semiconductor/insulator interface are the phenomena resulting from one or all of these parameters.

1.4 Device parameter extraction

Parameter extraction is a leading issue in characterization of charge transport mechanisms in organic transistors. As the drain current I_d depends on the drain voltage V_d and the gate voltage V_g , the current-voltage (I-V) curves can be plotted in two ways: the *output characteristics*, where a set of drain current versus drain voltage curves are drawn for various gate voltage values, and the *transfer characteristics*, in which the drain current is plotted as a function of the gate voltage for a given drain voltage. In the former case i.e. output characteristics, the curves are divided into a linear

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regime at low V_d and the saturation regime when $V_d > V_g$. The current in both regimes is given by equations (5) and (7), respectively.

$$I_{dlin} = \frac{W}{L} \cdot C_i \cdot \mu \cdot (V_g - V_{th}) \cdot V_d \quad (5)$$

The field-effect mobility (μ) corresponding to linear regime is calculated using the transconductance (g_m) from equation (6).

$$g_m = \left(\frac{\partial I_d}{\partial V_g} \right)_{V_d} = \frac{W}{L} \cdot C_i \cdot \mu \cdot V_d \quad (6)$$

$$I_{dsat} = \frac{W}{2L} \cdot C_i \cdot \mu \cdot (V_g - V_{th})^2 \quad (7)$$

Here W is the channel width, L the channel length, C_i the capacitance of the insulator, μ the mobility in the semiconductor and V_{th} the threshold voltage. (V_{th} is the gate voltage beyond which the conducting channel forms). Parameter extraction mainly involves mobility, μ , and threshold voltage, V_{th} . The most extensive technique to extract the μ and V_{th} includes plotting the square-root of I_{dsat} as a function of V_g in the saturation regime, because of the simple analytical form of the I_{dsat} equation. However, it should be noticed that there are two assumptions which make this equation simple but somehow disputed: (1) gradual channel approximation; and (2) constant mobility. There are several evidences that the second criterion is not obtained in organic transistors. First, according to the trapping model, it is predicted that the mobility increases with gate voltage. The second one is mobility degradation, a process by which mobility tends to decrease as the gate voltage increases. In the following the second problem will be discussed. Figure 1.6 illustrates the reason why extracting parameters under saturation regime conditions seems to be problematic.

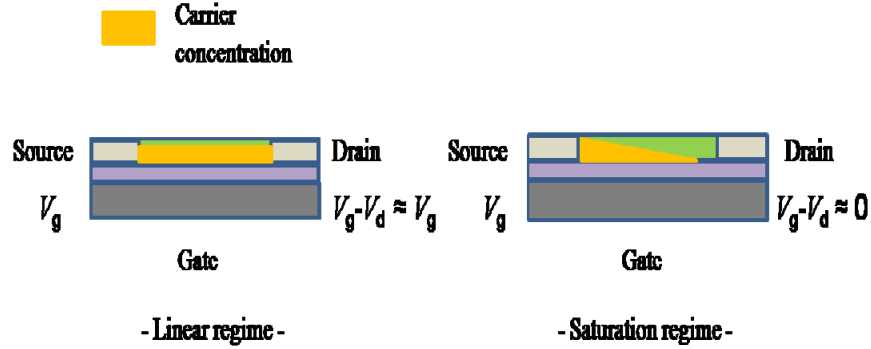


Figure 1.6 Charge distributions along the channel in a thin-film transistor. In the linear regime (left), the voltage at source and drain is nearly identical, so the carrier concentration is constant along the channel. In the saturation regime (right), the voltage is V_g at source and practically zero at drain, and the carrier concentration drops to zero when passing from source to drain. (From ^[75])

The transistor is considered as a two-dimensional structure. Thus, as an essential consequence the voltages at source and drain are not necessarily equal; In particular, the voltage is V_g at source and $V_g - V_d$ at drain; hence, the electrical potential at the insulator-semiconductor interface may not be constant all over the channel depending on the respective values of V_g and V_d . In the linear regime, $V_d \ll V_g$, the potential does not noticeably vary, while in the saturation regime, $V_d \geq V_g$, the potential varies after reaching the so-called pinch-off voltage ($V_d \approx V_g - V_{th}$). When reaching the pinch-off voltage, the voltage at the drain drops to zero and the potential along the channel decreases from V_g to zero when passing from the source to the drain. The pinch-off point gradually moves towards the source beyond the pinch-off voltage, and the potential variation along the channel maintains this magnitude. If the mobility is V_g dependent, one has to investigate the mobility all over the channel in order to have an exact

estimation of the saturation current. This is not easily feasible because the V_g -dependency of mobility for a given device is not known beforehand. Thus, for this reason, parameter extraction from the linear regime is the preferred technique in MOSFETs and will be the one adopted here.

As the threshold voltage is an important parameter that plays a central role in circuit modeling in FETs, numerous methods have been developed to extract it. Most of these methods are performed in linear regime and have their own advantages and drawbacks. A recent review can be found in ^[76].

As already mentioned, the quasi-universal method used in OTFTs to extract the V_{th} is based on plotting the square root of the saturation currents as a function of the V_g . Regarding the I_{dsat} equation, this should result in a straight line that crosses the V_g axis at $V_g = V_{th}$. But, in practice, the actual curve is not a straight line due to the mobility-dependency and contact resistance. Rather, it presents an upward curvature at low V_g and a downward curvature at high V_g . Consequently, in this kind of curve, the extracted mobility and V_{th} largely depend on the voltage range used for the linear fitting. In this sense, we illustrate two alternative methods to extract V_{th} in linear regime. The first one is, *linear-extrapolation method* ^[77] which is the most widely employed method by the researchers but it presents the disadvantage of being dependent of the series resistances of the FET. As the I_d vs. V_g curve deviates from a straight line at gate voltage above V_{th} due to series resistance and mobility degradation effects, it is common practice to find the point of maximum slope by a maximum in the transconductance, fit a straight line to the curve at that point, and extrapolate to $I_d = 0$, as illustrated in Fig.1.7. The second method is *second-derivative method* ^[78] which consists of plotting the second derivative of the linear I_d (or transconductance change) as a function of V_g . In this case, V_{th} is determined by peak of the curve. An example of calculating V_{th} with this method is shown in Fig.1.8. The advantage of this method is that it is insensitive to both

the contact resistance and the gate-voltage dependency of the mobility although on the other hand, it is highly sensitive to noise in the measurement.

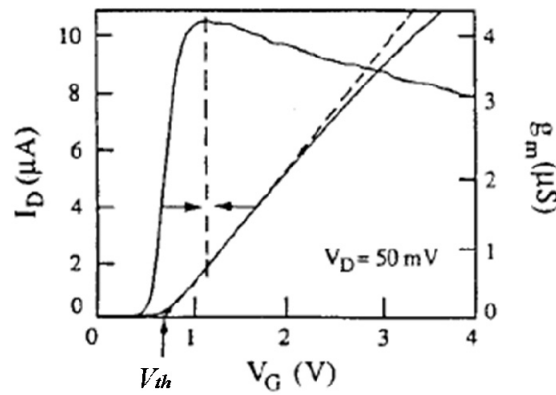


Figure 1.7 Example of drain current and transconductance vs gate voltage curves to illustrate threshold voltage extraction by linear-extrapolation method. (From ^[77])

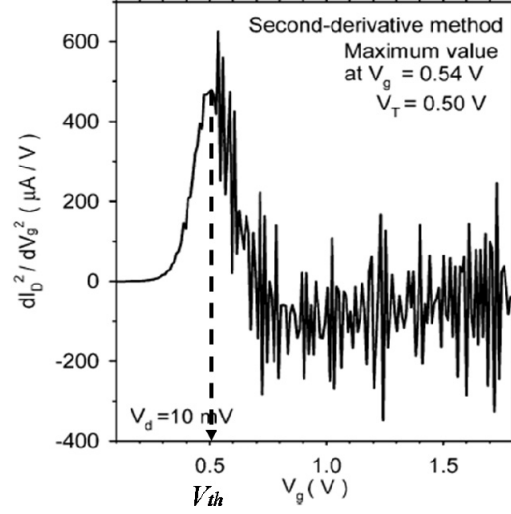


Figure 1.8 Example of the threshold voltage extraction by second-derivative method in linear regime. (From [76])

The other important parameter in OTFTs is the $I_{on/off}$ ratio which should be as high as possible and exceed 10^7 for practical applications. Frequently, in order to create an accumulation layer at the organic semiconductor/insulator interface, a large gate voltage is needed. This high gate voltage also induces an ohmic contribution to the drain current because of the bulk conduction of organic semiconductor. This ohmic contribution results in a current flow into the bulk semiconductor parallel to the channel which can mask the saturation behavior at high drain voltages. For highly doped semiconductors

$$I_{on/off} \sim 1 + C_i V_d \cdot \frac{\mu}{2t\sigma} \quad (8)$$

While for lightly doped is

$$I_{on/off} = \frac{\mu}{\sigma} \cdot \frac{C_i^2 \cdot V_d^2}{e \cdot N_A \cdot t^2} \quad (9)$$

In equation (9), N_A is the doping-induced charge density in the semiconductor^[79]. t is the semiconductor thickness. e and σ stand for the electric charge and conductivity, respectively. One can understand the required protocols for achieving high $I_{on/off}$ ratios from these equations which consist in using of thin semiconductor films, high-capacitance insulators and materials with high mobility to conductivity ratio.

1.5 Scanning probe microscopy techniques (SPM)

Many new research directions have been established in the past years based on techniques such as scanning tunneling microscopy (STM)^[80] with atomic-scale imaging and atomic force microscopy (AFM)^[81] which was originally introduced for high resolution surface topography of conducting or nonconducting materials. Scanning probe microscopy (SPM) includes STM, AFM, and other application modes based on AFM, some examples are magnetic force microscopy (MFM)^[82], electronic force microscopy (EFM)^[83], kelvin probe force microscopy (KPFM), conducting probe-AFM (CP-AFM), near-field scanning optical microscopy (NSOM)^[84] and scanning capacitance microscopy (SCM)^[85]. The evolution of AFM as an advanced and developed scanning probe technique with broad applications in academic and industrial research is a merit for a microscope which was initially introduced as a small part of STM. Mapping various surface properties such as mechanical, electrical, thermal, electromagnetic, etc. require the knowledge of surface topography. In this sense, most SPM techniques are based on surface scanning.

This section intends to explain and highlight those of SPM techniques which have the potential to directly provide correlations

between the electronic properties and the local film structure and have already made important contributions to the field of organic electronics. With this respect, we briefly introduce STM, KPFM and CP-AFM techniques with marking some of their applications, hereafter.

1.5.1 Scanning tunneling microscopy (STM)

The scanning tunneling microscope (STM) was developed in 1982 by Binning and Rohrer^[86], who both received Noble Prize for their work in 1986. STM is a local probe with the unique capability of imaging and manipulating single atoms or molecules on conducting or semi-conducting surfaces. Taking this capability into account, new insights have been provided into the physics, chemistry, and molecular biology processes on solid surfaces during the last decades. STM principle is based on exploiting quantum mechanics which allows electrons to “tunnel” through a classically forbidden gap. Particularly, if a sharp metallic tip is brought into such close proximity of a conducting surface, the wave functions of tip and the sample start to overlap. This typically occurs when the distance is less than 1 nm. If a bias voltage is then applied between the tip and sample, a tunneling current will be measured which strongly depends on the distance between tip and sample. If a positive bias is applied to the sample, electrons will tunnel from the filled tip states into the empty sample states and vice versa. STM images are usually recorded in constant-current mode because in most cases the surface of the sample is not flat and this mode is most likely to keep the tip from crashing or striking the surface. In this mode a feedback loop is used to adjust the distance between the tip and the sample to keep the current constant at a predefined value while the tip is raster scanned across the surface. The principle of STM operation is shown in Fig.1.9. As also indicated in this figure, the XYZ positioning device is controlled by piezoelectric crystals during scanning. The sample (or tip) is positively or negatively biased so that a small tunneling

current flows between the surface and the tip. This tunneling current can be written as:

$$I = bV \exp(-AZ)$$

Where b and A are constant. V is the applied bias and Z is the distance between the tip apex and sample surface. Due to the value of Z in argument of the exponential, STM is able to achieve atomic resolution, since the current changes by nearly one order of magnitude due to a change in distance as small as 0.1 nm. There is another mode for STM imaging which is called, constant-height mode. In this mode, the servo feedback for the z piezoelectric crystal is turned-off and the voltage and height are both held constant while the current changes according to the tip-sample distance. The constant-height mode can be useful when scanning over an area which is small and flat since it allows very fast scanning and avoiding thermal drift.

The primary applications of STM were focused on the imaging of semiconductor, inorganic and metal surfaces. Studying physisorbed organic molecules, “immobilized” by the formation of densely packed two-dimensional layers at the solid-liquid interface in the late 1980s, revealed the more important potentials of STM. Reduction of the molecules mobility on the surface was a prerequisite for high-quality imaging and highly stimulated STM investigations under ambient conditions at the liquid-solid interface.

Thiophene derivatives such as oligothiophenes^[88], cyclothiophene^[89] and polythiophene^[90] have recently attracted considerable attention due to their well defined chemical structures, improved solubilities and various electronic properties^[91, 92].

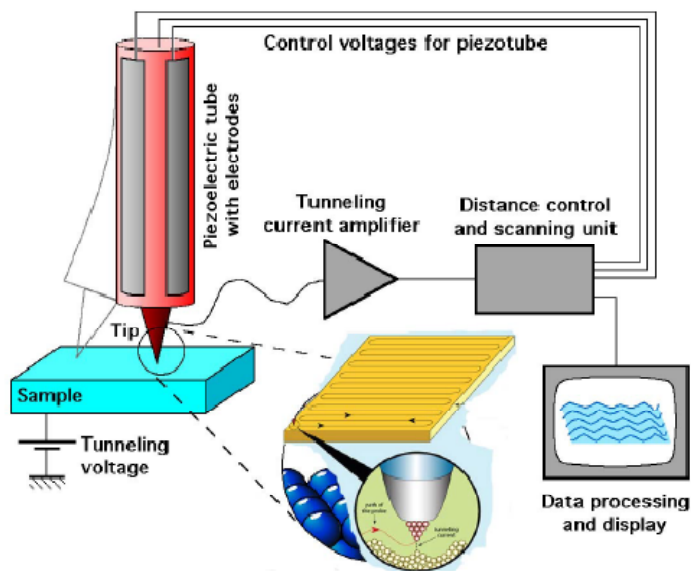


Figure 1.9 STM schematic working principle (From ^[87])

The property of a molecular assembly is both dominated by property of individual molecules and spatial arrangement of the molecules in the assembly ^[91, 93]. Accordingly, understanding the single molecule's property and molecular arrangement is of great importance in the fabrication of thiophene-based devices. Several studies have shown that thiophene molecules can self-organize and form supramolecular structures when adsorb on certain substrates. These molecular structures can be varied with respect to the fine balance between intermolecular interactions and molecule-substrate interactions and as a result provide desirable functionalities ^[94]. Given the permanent challenge in molecular science i.e. the ‘direct observation’ and ‘investigation of molecular nanostructures at solid surfaces’, STM revealed to be one of the most appropriate tools to study the molecules adsorbed onto a solid substrate ^[95].

Alkyl-substituted oligothiophenes are important thiophene derivatives with novel properties^[91, 92]. Their ability to adsorb on different substrates have been investigated by different research groups. For example, Stabel and Rabe^[91] reported a STM study of α,ω -dihexylsexithiophene on highly oriented pyrolytic graphite (HOPG) surface. Müller *et al.*^[96] reported novel substituted dialkylquinquethiophenes on HOPG. It was found that the self-assemblies were affected by formyl-substitutions. In another study^[97], molecular architectures of alkyl- and carboxylic-substituted oligothiophenes on HOPG were studied. It was demonstrated that the electrostatic interactions between the alkyl chains and carboxylic groups, attached at different positions on each molecule, played an important role in the formation of the ordered assemblies.

1.5.2 Kelvin Probe Force Microscopy (KPFM)

In OTFTs, thin-films of semiconducting layers can generally be prepared from mainly two main processes including solution-processing or vapor-deposition on dielectric substrates. During film deposition, crystalline nucleation and growth of semiconducting organic molecules are considerably affected by physical interactions between the molecules and dielectric substrates leading to different molecular orientations, crystalline phases and crystalline grains within the first few monolayers which are in direct contact with the substrate. In this sense, controlling the self-assembly process is of great importance since the performance of OTFT device is intrinsically related to the locally ordered crystalline structure near dielectric layers^[98]. Thus, SPM techniques based on AFM such as KPFM and CP-AFM are proposed as powerful tools to *directly* characterize crystalline morphologies and grain boundaries of organic semiconductor films generated on dielectric substrates simultaneously with the electronic properties.

Kelvin probe force microscopy (KPFM) is a convenient and standard technique for measuring the contact potential differences

(CPDs) between a reference electrode (tip) and a sample ^[99,100,101,102]. In this technique, two conductors (sample and tip) are considered as a parallel plate capacitor with a small spacing. According to a simple model, the contact potential between the two materials is $V_{CPD} = -(\Phi_1 - \Phi_2)/e$. Φ_1 and Φ_2 are the work functions of the conductors, including changes due to the adsorbed layer. A periodic vibration between the two plates at a frequency ω induces an alternative current (AC) with the same frequency.

$$i(t) = (V_{bias} + V_{CPD})\Delta C \omega \cos \omega t$$

The technique is based on detecting the zero point of the AC current while the additional bias voltage is applied between the two plates (tip and sample) until the electric field between them disappears. Therefore, CPD can be measured by $V_{CPD} = -V_{bias}$. In order to improve the performance of OTFTs, current efforts have focused on recognizing the correlations between the device structure, film morphology and charge transport properties. For example, contact resistances at the source and drain electrodes can considerably affect current flow in OTFTs depending on the device geometry i.e. top-contact or bottom-contact ^[103,104,105]. Thus, imaging the potential distribution along the conducting channel during device operation can be an effective approach to characterize these contact resistances. For instance, a sharp potential drop along the channel represents a high resistance of charge carrier transport at given V_d and V_g values. Several groups have demonstrated the use of KPFM in potential imaging in bottom-contact polythiophene ^[106,107,108] and pentacene-based devices ^[109].

There is another important process which strongly impacts the performance of such devices: *charge-trapping*. This phenomenon is rather difficult to characterize. More specifically, it is known that trapping occurs but the exact origin and its reason are not very clear. Is it primarily associated with obvious morphological features, such as domain interfaces and grain boundaries or with extrinsic chemical

or electronic effects? To answer these questions, SPMs can be employed to map the spatial distribution of traps in a film, characterize the effects of oxygen, water and other species on local trap formation and even study the kinetics of charge trapping at different carrier concentrations. KPFM is capable of indirectly monitoring trap evolution through variations in threshold voltages and potential profiles in OTFTs ^[110]. Recently, Janssen and coworkers used KPFM to measure trap evolution on the gate oxide as a function of ambient conditions exposure in planar transistor geometry. They found that water accumulation is responsible for charge immobilization at this surface ^[111]. In another study, Marohn and coworkers studied charge trapping using EFM measurements on pentacene-based OTFTs after turning off both the gate- and source-drain biases. Surprisingly, they found that trapping was not associated with visible grain boundaries in pentacene-film, and was not distributed uniformly in space ^[112]. More detailed descriptions and examples about KPFM and its applications can be found in chapter 3 of this manuscript.

1.5.3 Conducting probe-AFM (CP-AFM or CS-AFM)

This SPM based technique uses conducting probes to measure the current-voltage (I - V) relationship and resistance (conductance) of conducting materials. Conducting-probe AFM is also called current-sensing AFM ^[98,113]. This technique provides outstanding capabilities in study of nanoscale electrical transport measurements such as ^[114].

- Ability to acquire high-resolution images of samples before, during or after I - V measurement.
- Ability to collect I - V data on highly-resistant samples or surrounded by insulating regions.

These features make CP-AFM an attractive choice for studying electrical transport of nanotubes, nanoparticle assemblies, micro- or

nanofabricated semiconductor devices and individual molecules. Early CP-AFM studies revealed the ability of performing two basic kinds of electrical measurements: stationary point contact and two-dimensional resistance maps. The current sensitivity of CP-AFM is about 1 pA with a noise level of < 0.5 pA. One of the important applications of point-contact CP-AFM is “spreading resistance profiling” of dopant concentration in a material ^[115]. This technique has also been employed to measure conductance of individual semiconductor nanoparticles ^[116], adsorbed molecules on graphite and thin molecular crystals on Au. The second type of measurement, “resistance mapping” involves simultaneous imaging and resistance measurements ^[117]. Frisbie and coworkers ^[118,119,120,121] have used CP-AFM to study resistance in sexithiophene crystals vacuum sublimated on the SiO₂/Si substrates with predefined Au source-drain electrodes. According to Fig.1.10, a variable channel length transistor could be fabricated using a microfabricated Au electrode (drain) in contact with one sexithiophene grain, an Au-coated AFM tip as a positionable electrode (source) and a highly doped Si substrate as the gate. Figure 1.11 shows typical characteristics of Au-coated AFM probe used for CP-AFM measurement. As a final example, Fig.1.12 (a) shows an AFM topography image of a single-crystal of sexithiophene (6.9 nm thick) in contact with an Au electrode (25 nm tall) on SiO₂ before performing a point contact I - V measurement. I - V profiles were recorded at different positions on the grain, using ~ 100 -nN applied load on the probe-sexithiophene contact. As it can be seen in Fig.1.12 (b), the point-contact profiles at each position are rectifying. Especially, larger currents are obtained for positive probe bias, proposing that sexithiophene is a hole-transport material and the probe is a better hole injector than the Au wire, probably due to the high field (large voltage drop) assisted with the probe point contact. Current decreases monotonically by increasing probe-electrode distance at fixed probe voltage, reflecting increasing resistance due to the grain.

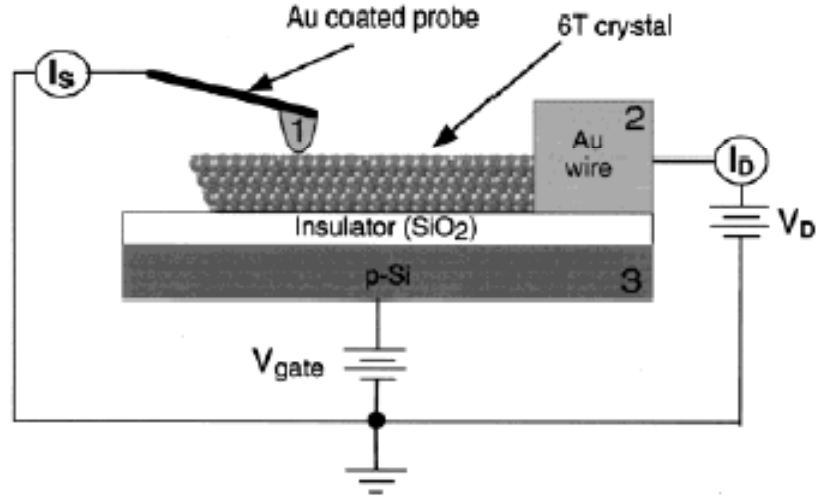


Figure 1.10 Scheme of the CP-AFM experiment in which an Au-coated AFM tip (1) is used to make electrical contact to crystal layers of sexithiophene (6T) grown by vapour deposition on SiO₂/Si. A microfabricated Au wire (2) serves as a drain electrode. The highly doped Si substrate is the gate (3). (From ^[118])

The above mentioned few examples of the ability to probe transport characteristics on local length scales by CP-AFM demonstrate its ability to quantify the effects of microstructure and contacts on the performance of OTFTs.

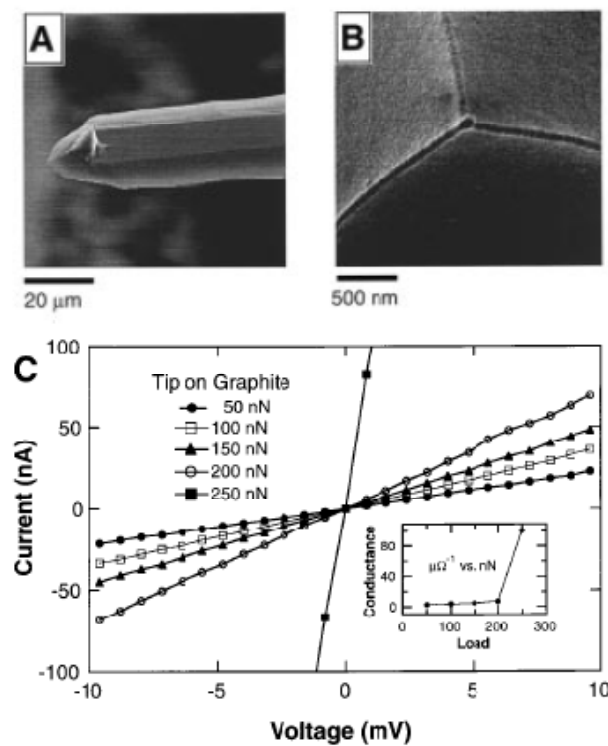


Figure 1.11 (A and B) SEM images of an Au-coated CP-AFM tip. (C) I-V characteristics of Au tips in contact with graphite as a function of compressive load. The inset shows conductance (I/V) versus load. The increase in conductance with increasing load is expected since the tip-graphite contact area will also increase with load. (From ^[113])

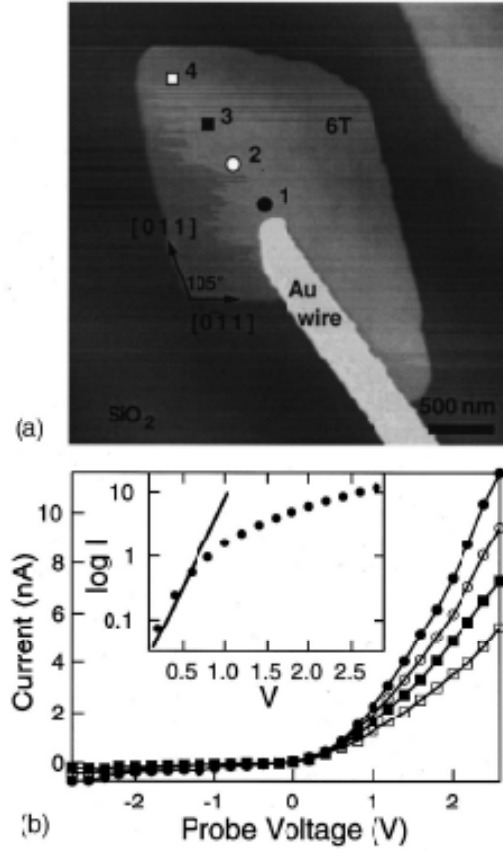


Figure 1.12 AFM topograph of a 6T grain contacted by a nanofabricated Au wire on SiO₂. Point-contact I-V measurements were recorded at each of the numbered positions. (b) I-V traces obtained at each of the numbered positions in (a). The inset shows a semi-log plot of the data for point 1, where current appears to have an exponential dependence on voltage (at low voltage) revealing a barrier to charge injection of ~ 0.5 eV. (From ^[119])

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* Chapter 2 *

Self-assembly and electronic properties of alkyl-substituted oligothiophenes: STM and STS study¹

Abstract

The molecular arrangements of two different alkyl-substituted oligothiophenes, α,α' -dihexylquaterthiophene (DH4T) and α,α' -dioctylterthiophene (DOTT), in monolayers on molybdenum disulfide (MoS_2) were studied with a joint theoretical / experimental approach. Scanning tunneling microscopy (STM) was used both at the liquid/solid interface and in dry conditions to investigate the ordering of the conjugated oligomers in two-dimensional layers. DH4T and DOTT form well-ordered monolayers at large scales with interdigitated packings on MoS_2 . In addition, DOTT exhibits an arrangement in which a dimer-type stacking of the conjugated backbone with an interlocking of the alkyl side chains is formed. Molecular modeling simulations have been used to provide insights into the microscopic morphology and to assess the stability of the different assemblies of DOTT and DH4T on MoS_2 .² The

¹ The experimental part of this chapter has been performed in UCL and the molecular modelling simulations have been done in UMONS in collaboration with Prof. Lazzaroni's group. The molecules were synthesized by the group of Prof. Geerts in ULB.

² Part of this chapter has been published in the Journal of Physical Chemistry C.

electronic property of individual molecules in DH4T and DOTT monolayers was also studied using STS spectroscopy.

2.1. Introduction

Over the past couple of decades, oligothiophenes have drawn much attention in the field of organic electronics, not only as model compounds for polythiophenes but also as promising materials by themselves.^[1] Indeed, their interesting electronic and transport properties combined with good stability under ambient conditions allow for their application in thin-film transistors^[2] or light-emitting diodes.^[3] For example, sexithiophene derivatives present a high charge carrier mobility ($1.1 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ in top-contact thin-film transistor configuration), as reported by Halik et al.^[4] These rod-like rigid molecules have efficient π -conjugation extending along their molecular long axis and reveal molecular packing along the short molecular axis, with π -stacking. Alkyl-substituted oligothiophenes, particularly, symmetrical α, α' -disubstituted compounds, have also been investigated because of their increased solubility and enhanced (electro)chemical stability,^[5] compared to the other oligothiophene derivatives. Moreover, the combination of the rigid aromatic core and the flexible side groups in their structure induces the formation of liquid crystalline mesophases, which may improve the charge transport properties by self-healing structural defects.^[6,7] This family of compounds also shows improved electronic performances (i.e. higher electron mobility) when the structural ordering is enhanced in the material.^[8] Therefore it is of prime interest to focus on the nanoscale structural and electronic properties of such compounds once adsorbed on surfaces.

In this context, SPM-based techniques such as scanning tunneling microscopy (STM), current-sensing atomic force (CS-AFM), Kelvin probe force microscopy (KPFM) or electrical force microscopy (EFM) are particularly interesting due to their ability to directly correlate the local electronic and structural properties of thin films and have already made important contributions into the field of organic electronics.^[9,10] Amongst these methods, STM offers a

powerful way to investigate the molecular arrangements of organic compounds in the very first monolayers at surfaces. It is a tool of choice to image, analyze, and monitor self-assembled molecular systems on substrates under various conditions (ambient, vacuum or liquid-solid interfaces) with resolution down to the (sub-) molecular level.^[11,12] Combined with theoretical simulations, it allows to precisely determine the structural organization in those self-assembled monolayers.

Undoubtedly, the liquid/solid interface is becoming more and more popular for studying self-assembly processes and structures on surfaces, as it provides an interesting environment for the dynamic exchange of molecules between the adsorbed layer and the liquid phase, repairing defects in the self-assembled layers.^[13] For example, it was found that *n*-alkanes, alkylbenzenes and molecules bearing long alkyl side groups with planar and extended π -systems can be adsorbed (and form ordered monolayers) from a solution onto highly oriented pyrolytic graphite (HOPG) surfaces.^[14,15]

In this context, several STM studies have shown the possibility of adsorption of thiophene derivatives on HOPG^[15b, 16, 17] or of polythiophenes.^[18,19] Among those studies, several have reported that some oligothiophene derivatives form ordered monolayers at the liquid-graphite interface such as alkylated oligothiophenes,^[16b,16d] alkylated oligothiophenes with halogen substituents^[17a] or carboxylated oligothiophenes.^[15b] These studies showed that the formation of the physisorbed monolayer strongly depends on the structure and the length of the oligothiophene and the presence of halogen substituents. The layer could also be stabilized by the presence of carboxylic groups, which can form hydrogen bonding. It was proposed as a general rule that oligomers with alkyl substituents at β positions tend to spontaneously self-assemble on HOPG, and that, in contrast, α - and α,α' -substituted derivatives are rarely adsorbed on HOPG.^[16b] However, such α - and α,α' -substituted oligothiophenes adsorb perfectly on MoS₂.^[16a] To our knowledge, among these studies,

only one reports on the self-assembly of α,α' -dihexylquaterthiophene (DH4T) on MoS_2 ^[16a] while dioctylterthiophene (DOTT) has never been studied on that surface.

In this chapter, we compare the adsorption of DH4T and DOTT as self-assembled monolayers on MoS_2 . These two thiophene derivatives were chosen for their potential applications as active materials in the field of organic thin-film transistors.^[2] MoS_2 was chosen as the substrate because: (i) molybdenum is known to be thermally stable on a wide range of dielectrics (SiO_2 , Si_3N_4 and HfO_2) and thus it appears to be a promising electrode material for future thin-film transistor industry,^[20] and (ii) specific interactions may take place between the sulfur-containing molecular adsorbates and the MoS_2 surface. STM at the liquid/solid interface and in dry conditions was used to image the self-assembly of these compounds. In parallel, force-field-based molecular modeling simulations were used to gain extra information on the supramolecular arrangements and to assess the stability of the different assemblies of DOTT and DH4T on MoS_2 .

2.2. Experimental part

Materials. α,α' -dihexylquaterthiophene (DH4T), dioctylterthiophene (DOTT) and α -3,7-dimethyldienyloctyl- α' -dodecylquaterthiophene (ddOD4T) molecules were synthesized as described elsewhere.^[21] The chemical structure of DH4T and DOTT molecules is shown in Figure 2.1. 1-phenyloctane and ethanol were purchased from Sigma-Aldrich and used without further purification. MoS_2 was purchased from SPI Supplies and was freshly cleaved prior deposition of the oligothiophene solutions.

STM characterization. All STM measurements were carried at room temperature. Nearly saturated solutions of DH4T and DOTT in 1-phenyloctane or ethanol were deposited onto the freshly cleaved surface of MoS_2 . Samples with solutions in phenyloctane were used for STM analysis at the liquid/solid interface. Samples with ethanol solutions were used for STM analysis in air after complete solvent

evaporation. The images were collected on a Agilent 5500 SPM microscope (Agilent Technologies) using mechanically cut Pt/Ir tips. Filtered images were obtained by reconstruction from the power spectrum after selection of the peaks corresponding to the monolayer structure.

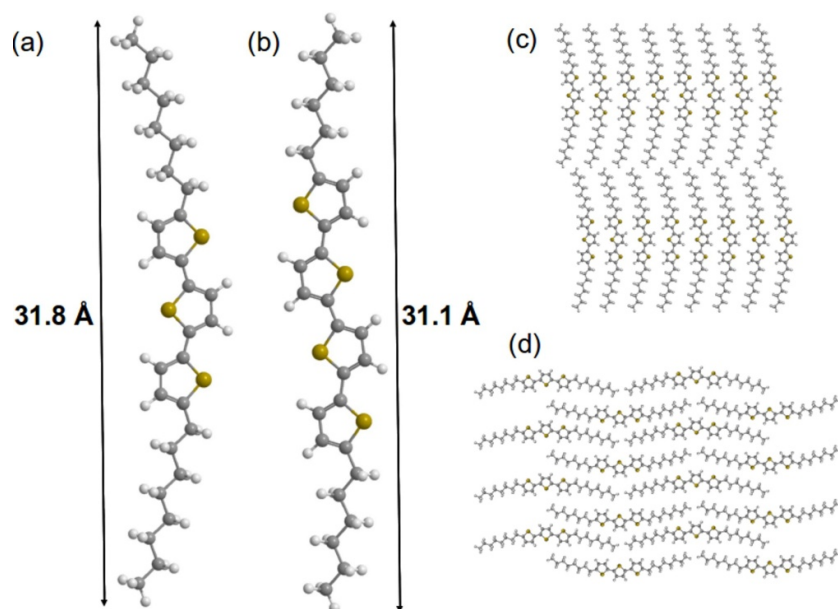


Figure 2.1 Chemical structures and extended length of the two alkyl-substituted oligothiophenes: (a) DOTT and (b) DH4T. Possible structural organizations for the DOTT monolayers: perfect lamellar (c) and brick-wall (d) packings both maximizing the molecule-substrate interactions.

Molecular modeling. Molecular mechanics simulations have been carried out on different assemblies of DOTT and DH4T molecules on MoS₂ surfaces. The calculations have been performed with the Accelrys Materials Studio 6 molecular modeling package, using the Polymer Consistent Force Field (PCFF)^[22, 23] which was previously tested on thiophene-based structures. The atoms of the

MoS₂ substrate were kept fixed in their position, since physisorption is not expected to alter the geometry of the substrate surface. Indeed, surface reconstruction of MoS₂ only occurs at very high temperature, above 1200 K.^[24] Periodic boundary conditions were used.

The unit cells of the monolayers of DOTT and DH4T on MoS₂ extracted from the STM images have been used as the starting point to model the molecular assembly. First DOTT and DH4T molecules are arranged in planar assemblies having a unit cell consistent with the STM measurements.

Next, a simulation box is built by making interact those planar assemblies with a MoS₂ surface large enough to accommodate them in such a way to avoid molecular overlap when periodic boundary conditions are applied to simulate the infinite assemblies. The geometry of the molecular assembly is then optimized via energy minimization and the final morphology is compared with the experimental one and energetically characterized. For each selected assembly, we calculate the total potential energy of the system, the potential energy of the supramolecular assembly alone (i.e., the molecular layer in the absence of the surface), the substrate-monolayer interaction energy and the binding energy per molecule. The higher the binding energy, the more stable a molecule in the monolayer is with respect to a single, isolated molecule adsorbed on the substrate. This is calculated as follows:

$$E_{bind} = \frac{E_{pot} - NE_{mol} - E_{sub}}{N} \quad (1)$$

where E_{bind} is the binding energy per molecule, E_{pot} the total potential energy of the system, E_{mol} the potential energy for an isolated molecule on the surface, E_{sub} the potential energy of the MoS₂ surface and N the number of molecules in the unit cell.

Because the modeled systems have different size and different number of molecules, the energetic term that can be directly compared for the different assemblies is the binding energy, which is

an energy "per molecule", but nevertheless contains information on the intermolecular interactions.

STS measurement. Spectroscopic data have been recorded with the STM tip located over the thiophene moities and also for bare MoS₂. Tunneling spectra were recorded with the feedback loop disabled. *I-V* curves were measured fast (on the order of 100 ms) in order to minimize effects of tip or sample drift during the acquisition of the tunneling spectra. The points where the local *I-V* curves have been acquired are shown in corresponding STM image. The presented curves are averaged of curves. Over 100 curves were measured for each system in order to check reproducibility and identify any possible artifacts.

2.3. Results and discussion

MoS₂ was also chosen as substrate because, though much efforts were done to investigate whether three α,α' -substituted oligothiophenes i.e. DH4T, DOTT and ddOD4T can form stable monolayers on HOPG, the only molecule that could somehow be detected was ddOD4T. It could temporarily adsorb from 1-phenyloctane onto the HOPG surface though, the most of the acquired images were fuzzy and required filtration to be able to be interpreted. DH4T and DOTT did not form a stable monolayer film on HOPG which may be explained by the difference in the length of the alkyl side chains.

In Fig.2.1, two limiting cases of expected molecular organizations for the self-assembled monolayers of DOTT are presented. If molecule-substrate interactions dominate, molecules should lay on MoS₂ with the thiophene cores flat on the substrate and with either a lamellar organization (Fig.2.1(c)) or a brick-wall one (Fig.2.1(d)).

2.3.1 STM experimental results

a) STM on DH4T at the phenyloctane/MoS₂ interface

Figure 2.2 (a), (b) shows the STM images of DH4T adsorbed at the phenyloctane/MoS₂ interface together with the corresponding filtered images (Fig. 2.2 (d),(e)). DH4T forms stable and ordered monolayers with oval brighter areas arranged parallel to each other, in a brick-wall structure similar to the one presented in (Fig. 2.1(d)). Oval structures are organized in rows, shifted laterally compared to adjacent rows. The length of those oval features approximately corresponds to the length of the oligothiophene moiety (1.7 nm). According to the resonance enhanced tunneling model, the contrast in STM current images is basically ruled by the energy difference between the frontier orbitals of the adsorbate and the Fermi level of the substrate.^[25] Therefore, the conjugated core of the molecule exhibits a higher current value than the aliphatic end groups due to the higher tunneling probability. For this reason, in Fig. 2.2, the conjugated thiophene cores of the molecules appear brighter while the darker parts of the image can be referred as to the alkyl end groups, which are supposed to lie down between the brighter parts.^[16b,26] The measured separations between two adjacent thiophene cores parallel and perpendicular to the molecule axes are about 3.3 nm and 0.9 nm, respectively, which are large enough to host one or two alkyl chains in between. The observed structure is similar to the one observed by Azumi et al. for the same system.^[16a]

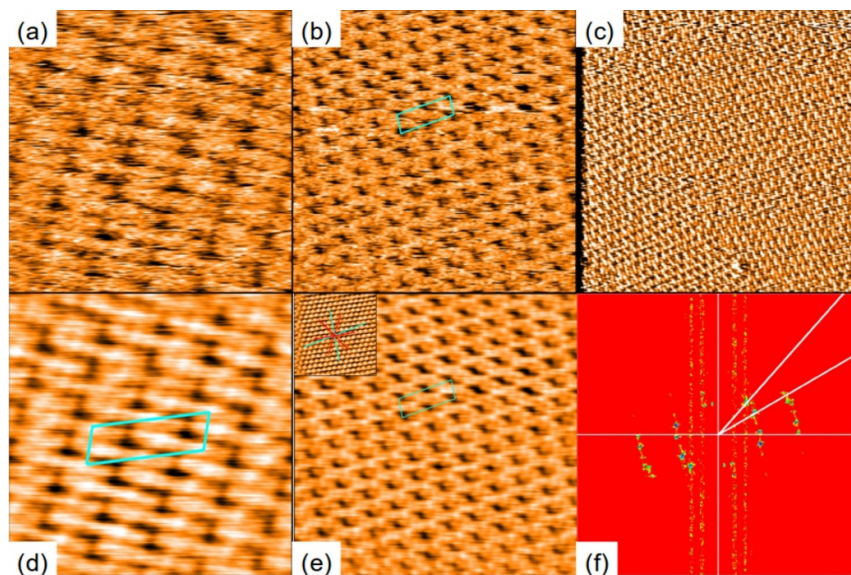


Figure 2.2 Top: raw STM current images of DH4T adsorbed at the phenyloctane/MoS₂ interface (700 pA, -1.00 V) (a) 8.5×8.5 nm², (b) 17.5×17.5 nm², (c) 40×40 nm². Bottom: (d) and (e) filtered images corresponding to the images in (a) and (b), respectively; (f) power spectrum of the image presented in (c). The unit cell determined on the basis of the STM results is drawn in cyan. The inset in (e) presents the underlying MoS₂ substrate with the directions of the DH4T and MoS₂ lattices marked in cyan and red, respectively.

The conjugated cores are assumed to lie flat on the basal plane of the MoS₂ surface and separated by alkyl chains. The alkyl chains cannot be resolved due to their high conformational mobility on the time scale of the STM measurements. It can also be assumed that the electron density of the thiophene cores is so large that it is not possible to discriminate the alkyl chains.

Using the underlying MoS₂ lattice as an internal reference, the unit cell adsorbate structure was measured. It is characterized by the following parameters: $a=3.36\pm0.13$ nm, $b=1.13\pm0.05$ nm, $\gamma = 81.3\pm1.9^\circ$, close to those reported previously ^[16a]. The

corresponding unit cell is drawn in cyan on the STM images (Fig. 2.2 (b), (d) and (e)). As can be seen in the inset in Fig. 2.2(e) which presents the STM current image of the underlying MoS₂ substrate, the axes of the DH4T adlayer (cyan lines) are not oriented along one of the axes of the substrate lattice (red lines). The long axis of the DH4T molecules also does not seem to be oriented along one of these axes.

This is confirmed when considering Fig. 2.2(c) that presents a larger scale image of the DH4T monolayer with a domain boundary running through the analyzed region from the upper left corner of the image down to the bottom center. This DH4T monolayer clearly presents different orientations on both side of the boundary. This is confirmed by the presence of doubled lattice peaks in the corresponding power spectrum image (Fig. 2.2(f)). The angle between the two surface lattices (white lines in Fig. 2.2(f)) is equal to $17\pm 1^\circ$. This value does not correspond to typical angles of the MoS₂ hexagonal lattice and strongly suggests that the DH4T layers do not have a preferential orientation with respect to the underlying substrate lattice.

b) STM on DOTT at the phenyloctane/MoS₂ interface

Figure 2.3 (a-c) presents STM current images of DOTT adsorbed at the phenyloctane/MoS₂ interface, along with the corresponding filtered images (Fig. 2.3 (d-f)). DOTT also forms stable and ordered monolayers. According to the electronic nature of the aromatic and aliphatic moieties, it can again be concluded that the brighter parts correspond to the oligothiophene π -system^[16b,26] and the alkyl chains are supposed to lie down between the brighter parts.

The layer arrangement is characterized by a (dimer) lamella-type structure. In this structure, double rows of molecules are formed separated by the length of approximately one alkyl side group. In that zone, the alkyl side groups are supposed to interdigitate to enhance Van der Waals interactions. The heteroaromatic moieties in the rows are arranged in a way that each second one is displaced by the length

of one aromatic unit. The measured distance between the thiophene cores in two adjacent rows is about 3.2 nm. Within the rows, the brighter spots are separated by a distance of about 1.0 nm, which suggests that one of the alkyl side groups is sandwiched between two aromatic units in the row. This organization is characterized by the following parameters determined using the underlying MoS₂ lattice as a reference: $a = 3.44 \pm 0.27$ nm, $b = 1.13 \pm 0.08$ nm, $\gamma = 79.3 \pm 1.0^\circ$. The corresponding unit cell is drawn in cyan on the STM images (Fig. 2.3 (b,d-f)).

The layer arrangement is rather similar to the one observed by Azumi et al. for α - α' -didodecylquaterthiophene (DD4T) adsorbed on MoS₂.^[16a] Both observations suggests that the length of the alkyl substituents strongly influences the molecular organization with a transition from a brick-wall arrangement as the one depicted in Fig. 2.1(d) for short alkyl chains to a double-row (dimer) lamellar arrangement for longer alkyl chains.

The inset in Fig. 2.3 (f) presents an STM current image of the underlying MoS₂ substrate. The orientation of the axes of the DOTT lattice is shown in cyan while the orientation of the substrate lattice axes is materialized by the red lines. As for DH4T, there is no registry between both lattices, suggesting that there is also no preferred orientation of the DOTT molecules with respect to the MoS₂ lattice.

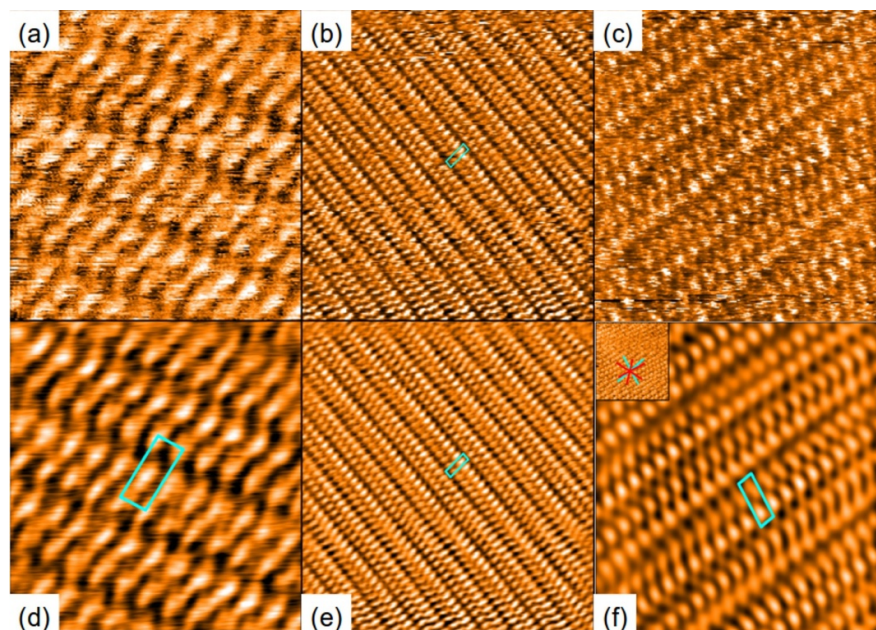


Figure 2.3 Top: raw STM current images of DOTT adsorbed at the phenyloctane/MoS₂ interface (200 pA, -1.3 V), (a) 10×10 nm², (b) 35×35 nm², (c) 20×20 nm². Bottom: (d), (e) and (f) filtered images corresponding to the images presented in (a), (b) and (c) respectively. The unit cell determined on the basis of the STM results is drawn in cyan. The inset in (f) presents the underlying MoS₂ substrate with the directions of the DOTT and MoS₂ lattices drawn in cyan and red, respectively.

In few cases, a second molecular arrangement (Fig. 2.4) was observed. In this organization, the molecules seem to be arranged in single rows with the aromatic units separated by alkyl side chains in each row. For this structure, the distances between adjacent thiophene cores are measured to be around 2.7 nm and 0.9 nm, respectively. The measured unit cell for this configuration is characterized by $a = 2.60 \pm 0.11$ nm, $b = 0.94 \pm 0.05$ nm, $\gamma = 66.3 \pm 1.1^\circ$.

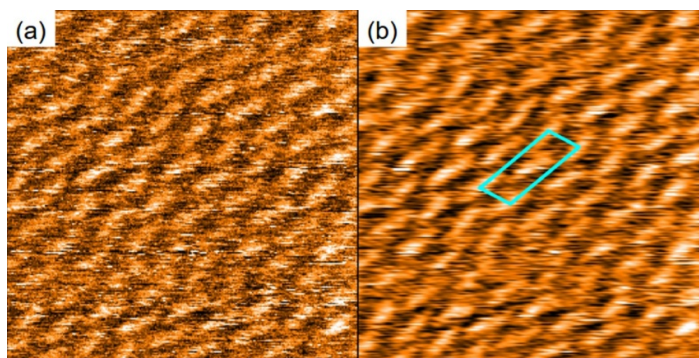


Figure 2.4 STM current images of the alternative assembly of DOTT adsorbed at the phenyloctane/MoS₂ interface ($10 \times 10 \text{ nm}^2$, 10 pA , -1.2 V). (a) Raw image, (b) filtered image with the unit cell drawn in cyan.

The organic liquid/solid interface provides an interesting environment to carry out self-assembly experiments in monolayers and their investigation by scanning tunneling microscopy. Compared to the sample preparation and measurements in dry or vacuum conditions, the liquid/solid interface has a number of advantages. One of these advantages is the possibility of dynamic exchange of molecules adsorbed on the surface and in the liquid phase which leads to repair of defects in the self-assembled layers. An example of this dynamic exchange is shown in Fig. 2.5 for DOTT molecules. Those images were obtained consecutively, i.e. the time lapse was 30 seconds. In the first image, there is a defect (pointed with the cyan circle), due to the absence of one molecule constituting a dimer, which probably desorbed into the solvent. However, in the second image, this defect is healed by adsorption of another molecule from the solvent to the surface.

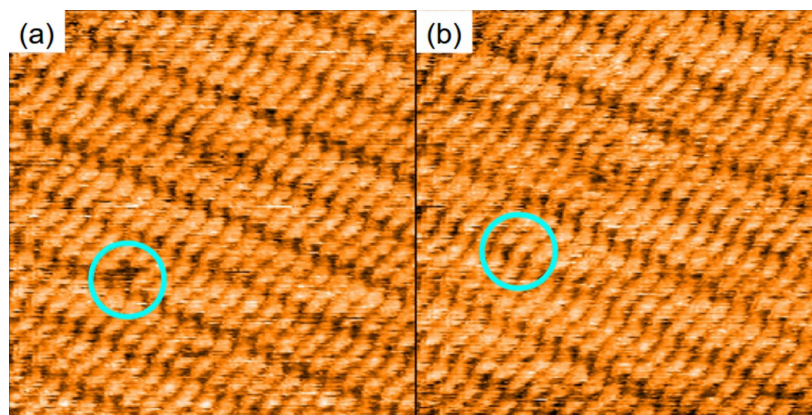


Figure 2.5 STM current images ($25 \times 25 \text{ nm}^2$, $I = 160 \text{ pA}$, $V = -1.3 \text{ V}$) of DOTT adsorbed at the phenyloctane/ MoS_2 interface showing the self-repairing of a defect in the self-assembled monolayer. The place of the mobile molecule is highlighted by cyan circles.

c) STM on DH4T and DOTT on MoS_2 in dry conditions

Figure 2.6 shows STM images of DOTT and DH4T adsorbed from ethanol solutions onto MoS_2 and imaged in dry conditions.

Interestingly, DOTT molecules are well-ordered on large scales on the surface and form the dimer row structure, as already observed at the liquid/solid interface (Fig. 2.3). They self-assemble into parallel lamellae in which two molecules couple together to form dimers, with lamellae separated by alkyl groups.

DH4T molecules seem to be packed face-on with respect to the basal plane of the surface and separated by alkyl chains. The measured distance between the thiophene cores in two adjacent columns is about 3.4 nm and the distance between the neighboring molecules in a row is estimated to be 1.2 nm.

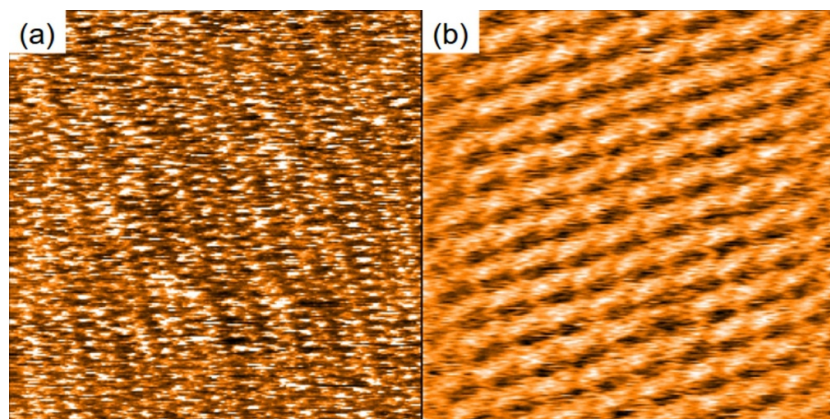


Figure 2.6 STM current image of DOTT (left) and DH4T (right) adsorbed on MoS₂ in dry conditions. (DOTT: 300 pA, -1.3 V, 65×65 nm²) and (DH4T: 300 pA, -1.2 V, 10×10 nm²).

This arrangement is similar to that observed at the phenyloctane/MoS₂ interface (Fig. 2.2) as well as by Azumi and co-workers for the same molecule adsorbed on MoS₂.^[16a] However, their results were obtained at the 1,2,4-trichlorobenzene/MoS₂ interface and not in dry conditions nor in a phenyloctane solution. The similar results obtained in the three cases can provide evidence for a solvent-independent supramolecular ordering, which is probably due to the high affinity of DH4T for MoS₂.

It is worth noting that in the monolayers of both α -alkylated oligothiophenes, direct π - π stacking of the thiophene cores does not take place and they are separated by alkyl chains either at liquid/solid interface or in dry condition. This arrangement seems to be favorable to cover the surface as densely as possible.^[16a]

2.3.2 Theoretical modeling

a) Modeling of single molecules on MoS₂

Before modeling the DOTT and DH4T molecular assemblies, the adsorption of single DOTT and DH4T molecules on MoS₂ was studied to determine whether there are preferential adsorption geometries and orientations for the molecules. This is important since the fitting of supramolecular monolayers into the substrate unit cells will force the molecules to adopt a particular orientation, given the surface structure of MoS₂.

The modeling procedure was the following: the molecule was made to interact with a large surface of MoS₂, and a molecular mechanics minimization was performed. Then, the total potential energy for the system was calculated, after minimization, during a complete rotation of the molecule in the plane of the surface, with steps of 30°. Fig. 2.7 shows the first rotation steps for a DOTT molecule (each rotation has been color-coded differently).

During the rotation of the molecules the average energies and their fluctuations are 120.9 ± 0.6 kcal · mol⁻¹ and 220.9 ± 0.7 kcal · mol⁻¹ for DOTT and DH4T, respectively. Because the fluctuation found in the energy during the scan is comparable with the thermal energy kBT at room temperature (0.6 kcal · mol⁻¹), it can be concluded that DOTT and DH4T do not have highly preferred adsorption sites and orientations on MoS₂. This conclusion is in agreement with the observation (Fig. 2.2) that the angle between different DH4T domains is not equal to one of the characteristic angles of the underlying MoS₂ lattice and that the unit cells determined for both systems are not oriented along one of the axis of the hexagonal lattice of the substrate.

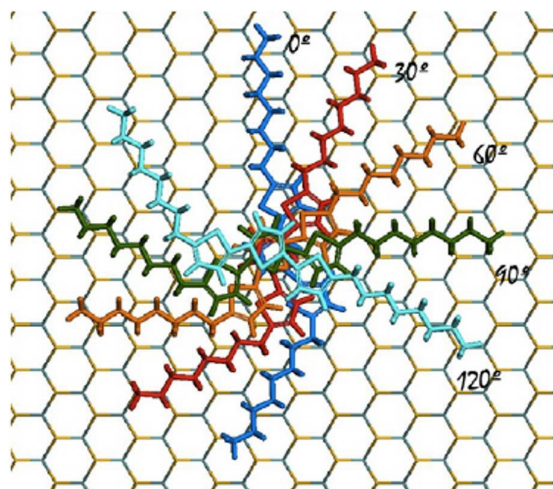


Figure 2.7 Rotations of a DOTT molecule adsorbed on MoS_2 between 0° and 120° . The molecule is color-coded for each rotation.

b) Modeling of DH4T and DOTT monolayers

Figure 2.8(a) and Figure 2.9 show the DOTT assembly on MoS_2 that fits best the STM images. The unit cell parameters for this DOTT assembly are: $a = 3.40 \pm 0.24$ nm, $b = 1.23 \pm 0.14$ nm, $\gamma = 66 \pm 11^\circ$ (see Fig. 2.10), which are in rather good agreement with the experimental parameters within the experimental error ($a = 3.44 \pm 0.27$ nm, $b = 1.13 \pm 0.08$ nm and $\gamma = 79.3 \pm 1.0^\circ$). In this monolayer, DOTT molecules are fully planar on the surface (tilt angle is zero) and are fully extended having the length given in Fig. 2.1. The molecules are indeed organized in a dimer-type structure in which one can observe that the DOTT molecule rows are alternately separated by less than the length of one octyl side group and by approximately the length of the octyl side group. Based on this result, one may conclude that the dimer-type structure is more stable than

the interdigitated one, which was indeed scarcely observed (see Fig. 2.4).

Figure 2.8(b) shows the DH4T assembly that was obtained based on the experimental results. This figure shows a brick-wall organization, with unit cell parameters of $a = 3.29$ nm, $b = 1.08$ nm and $\gamma = 86^\circ$, in rather good agreement with the experimental ones, i.e. $a = 3.36 \pm 0.13$ nm, $b = 1.13 \pm 0.05$ nm, $\gamma = 81.3 \pm 1.9^\circ$. As for DOTT, the tilt angle is zero. The differences between the two types of packing, named double-row for DOTT and brick-wall for DH4T, are highlighted in Figure 2.9. However for DH4T, the side view of the assembly shown in Fig. 2.8 (b) highlights the difficulties in fitting the molecular assembly into the MoS₂ simulation box. Molecules at one of the simulation box boundary are not planar because the simulation box is too small to accommodate all the molecules flat on the surface. This "mismatch" increases the energy of the system.

Therefore, the size of the simulation box was increased of one MoS₂ unit in both a and b directions to form a new assembly, named DH4T-alt, having the following parameters: $a = 3.48$ nm, $b = 1.18$ nm and $\gamma = 88^\circ$. Figure 2.8(c) shows the top view of the DH4T-alt assembly in which all the molecules lie flat on the surface (tilt angle equal to zero) with a length corresponding to the extended length of the molecule (Fig. 2.1).

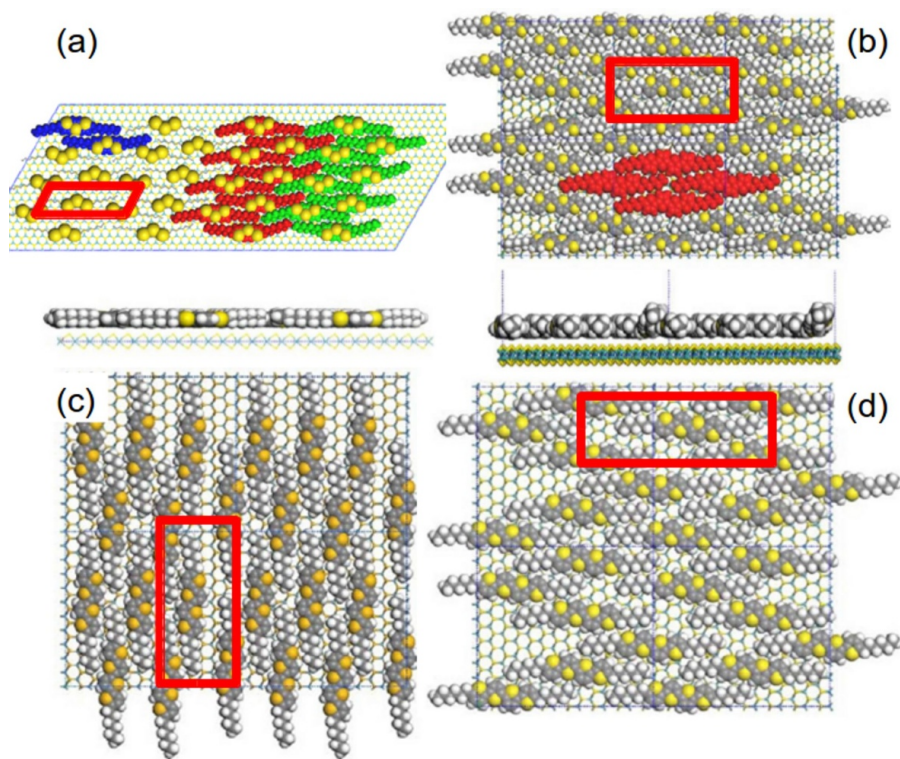


Figure 2.8 Top and side views of assemblies on MoS₂. (a) Top and side views of the simulation box used to model the DOTT monolayer on MoS₂. In the top view sulfur atoms of DOTT are highlighted in yellow balls to better identify the molecular pattern. A single lamella, in blue, is also shown. Two molecular double rows are highlighted in red and green, respectively. The monolayer unit cell is also displayed in red. (b) DH4T model based on the experimental STM data; to highlight the brick wall structure of the monolayer, some molecules are displayed in red and six simulation boxes are shown (the simulation boxes boundaries are displayed by the blue dashed lines). Top view of the DH4T-alt (c) and of the DH4T-alt-90 (d) assemblies on MoS₂ (four simulation boxes are shown to highlight the brick wall molecular arrangement).

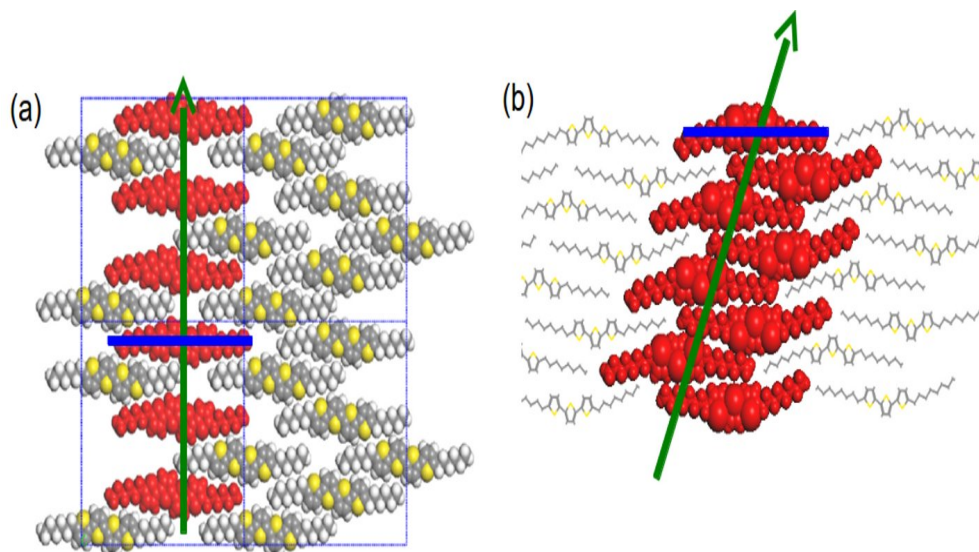


Figure 2.9 (a) In the monolayer of DH4T (brick-wall), the molecules are interdigitated with their main axis oriented perpendicular to the direction of propagation of single molecular rows (green arrow). (b) In the monolayer of DOTT (double row lamellar), the main axis of the molecules is tilted with respect to the direction of propagation of the lamellae.

Increasing the size of the simulation box has the consequence that the monolayer is less dense compared to that shown in Fig. 2.8(b). To match at best the monolayer unit cell with the MoS₂ lattice, we built a new monolayer, named DH4T-alt-90, obtained by rotating the DH4T-alt monolayer by 90°. The DH4T-alt-90 monolayer (Fig. 2.8(d)) is characterized by the following unit cell parameters: $a = 3.88$ nm, $b = 1.19$ nm and $\gamma = 87^\circ$.

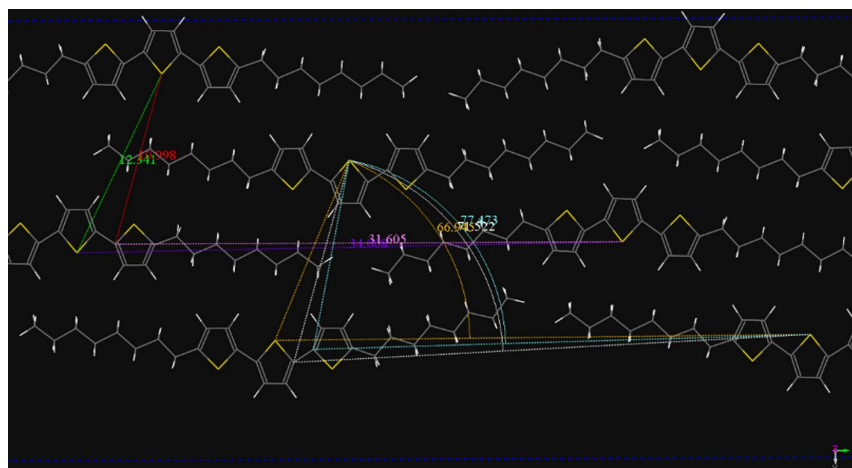


Figure 2.10 Scheme illustrating for DOTT the origin and magnitude of the uncertainty on the unit cell parameters extracted from the theoretical modeling.

As shown in Fig. 2.8(c, d), the DH4T-alt and DH4T-alt-90 assemblies also differ by the way molecules are aligned with respect to the MoS₂ surface: molecules are aligned along the zigzag and harmchair directions of the substrate, respectively. Comparing the three simulated structures with the experimental results it seems that the most probable organization for DH4T is the DH4T-alt one.

The results of the energetic analysis performed on the DOTT, DH4T, DH4T-alt and DH4T-alt-90 assemblies are reported in Table 2.1.

Table 2.1. Interaction energy per molecule between monolayer and surface (E_{nb}/mol), potential energy of single molecule on surface (E_{mol}) and binding energy (E_{bind}) are reported for the four assemblies. All energies are expressed in kcal.mol^{-1} .

Assembly	E_{nb}/mol	E_{mol}	E_{bind}
DOTT	-56.6	120.6	-4.0
DH4T	-56.4	219.9	-5.5
DH4T-alt	-59.5	219.9	-7.8
DH4T-alt-90	-58.7	219.9	-7.6

As expected, the energetic results for DH4T show that the DH4T-alt and DH4T-alt-90 assemblies, in which all the molecules are adsorbed flat on the surface, are the most stable because of the better interaction of the molecules with the surface (E_{nb}). This suggests that the real structure is probably in between that of DH4T-alt and DH4T-alt-90.

Because of the different number of molecules in the simulation boxes for the different systems, all the energies related to the DOTT and all the DH4T monolayers should not be compared; the only energy that can be compared is the binding energy, because this energy is expressed per single molecule. The results indicate that the energetic stabilization related to the formation of a monolayer on MoS_2 is larger for DH4T than for DOTT, which originates from a denser packing since DH4T is linear while DOTT has a curved

(banana) shape. In both cases, the interdigitation of the alkyl groups drives the formation of the monolayer on MoS₂, as the thiophene oligomers are separated by alkyl groups with close contact interactions. Regarding the two limiting cases of Fig. 2.1(c, d), the organization of DOTT and DH4T on MoS₂ is close to the case (d) (brick-wall or tilted brick-wall, i.e. double-row), which strongly differs to what is observed on other surfaces (e.g. glass, mica, graphite), for which the other limiting cases can be observed.^[17e]

2.3.3 Scanning tunneling spectroscopy of DH4T and DOTT

In order to probe the electronic properties of DH4T and DOTT molecules on MoS₂, STS measurements of the adlayers were performed under ambient conditions at liquid/solid interface (phenyloctane as solvent). STS measurements were first performed on bare MoS₂ both in air and at phenyloctane interface. The acquired tunneling spectra are shown in Fig. 2.11 and 2.12, respectively. However, it seems that what we observe is different than what has been reported in the literatures (Fig.2.13). However, it should be noted that those experiments have been performed in UHV which improve the accuracy of the measurements compared to the experiments performed in air or at liquid/solid interface. According to the previous studies, the band-gap of MoS₂ is 1.65 eV^[27] which is though smaller than the experiment value, 1.90 eV.^[28] Figure 2.14 presents the projected density of states (PDOS) of Mo and S atoms. It can be divided into three regions: region A, states ranging from -14.6 to -12.7 eV mainly originates from S (3s) states; region B, states ranging from -6.2 to -0.25 eV originate from Mo (4d) and S (3p) states, with small contribution from Mo (sp) states; region C, states in the range 1.4-5.0 eV correspond to S (3p) and Mo (4d) states. Besides the band-gap at Fermi level, a large gap exists in the occupied states, separating region A from B.

While a clear gap is observed between occupied and unoccupied states at Fermi level in Fig.2.14, we do not see such gap in our measurements for both dry and at phenyloctane interface conditions. This difference makes the interpretation of our STS results on bare MoS₂ more complicated.

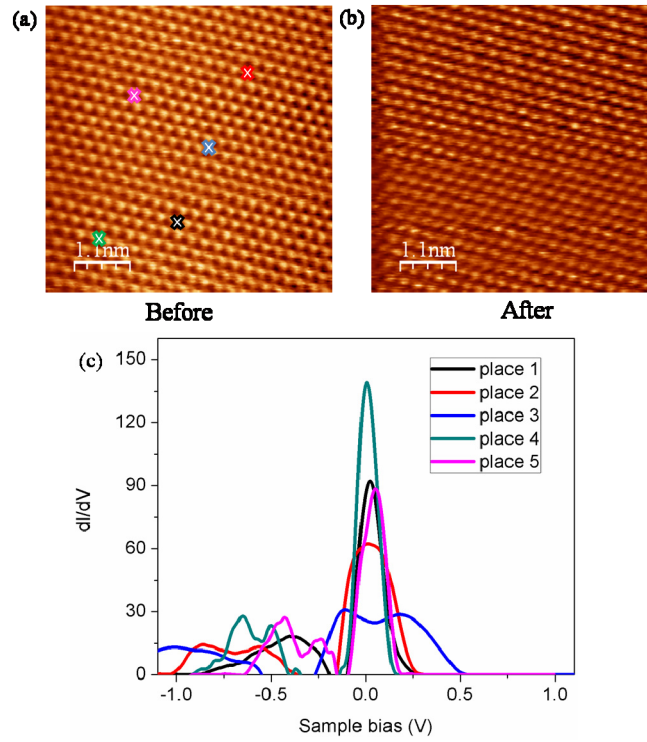


Figure 2.11 An example of dI/dV - V curves obtained at different points on bare MoS₂ in dry conditions (in air). Each colored cross in (a) corresponds to the recorded STS signal shown in (c). STM images in (a) and (b) were acquired before and after recording the STS signal, respectively.

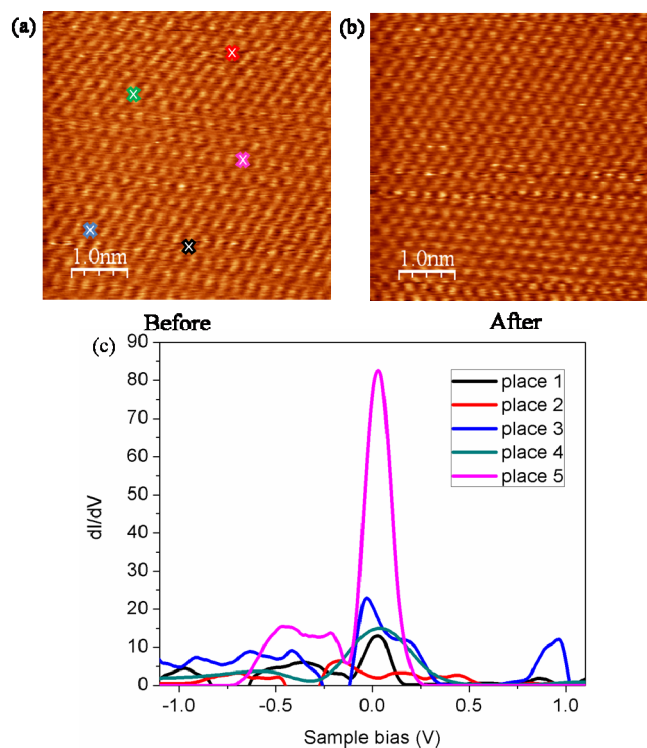


Figure 2.12 An example of dI/dV - V curves obtained at different points on bare MoS_2 at liquid/solid interface. Each colored cross in (a) corresponds to the recorded STS signal shown in (c). STM images in (a) and (b) were just acquired before and after recording the STS signal, respectively.

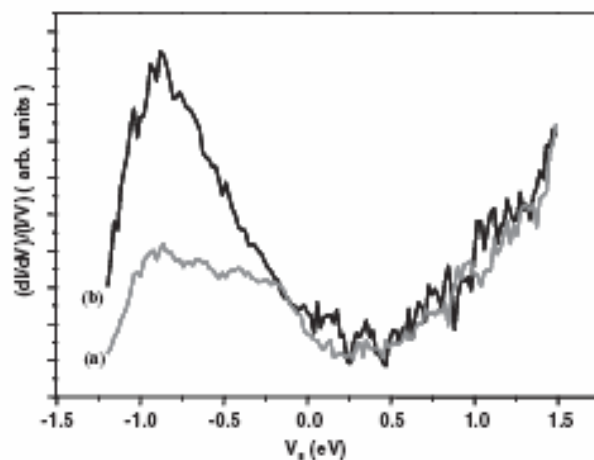


Figure 2.13 $(dI_t/dV_s) / (I_t/V_s) - V_s$ curves on terrace (a) and ridge (b) of bare MoS_2 in UHV conditions. (From ^[29])

Figure 2.15 show typical $I-V$ and $dI/dV-V$ curves from the adlayers of DH4T and DOTT molecules at liquid/solid interface. In these figures, averaged $I-V$ curves acquired on DH4T and DOTT molecules are presented. The average was recorded consecutively at different locations in the adlayer. According to these figures, the resulting curves are asymmetric, with larger currents obtained for negative sample bias. The $I-V$ data for both DH4T and DOTT reveal a region around the Fermi-level (zero-level of energy) in which the detected tunneling current is suppressed.

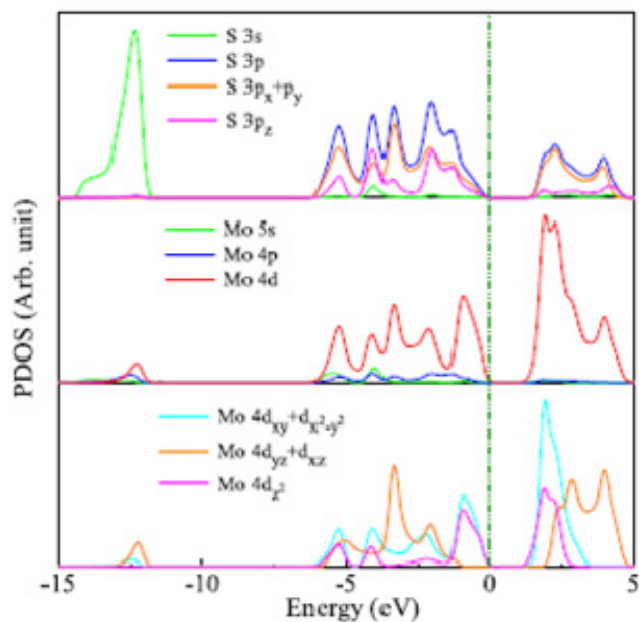


Figure 2.14 Projected density of states of S and Mo atoms. The Fermi levels are at zero, denoted by the dash line. (From ^[27])

The dI/dV - V curves reflect the local density of states (LDOS) of adsorbates. Applying a proper bias on substrate imply the Fermi-energy of the substrate to resonate with molecular orbitals (HOMO and LUMO) of the adlayers ^[22a]. This results in a sharp change in the dI/dV - V curve. The edge defined by the cross point of the tangents of the zero-current plateau and uplift part of the curve represents the HOMO and LUMO energy states, respectively. Therefore, the energy gap between HOMO and LUMO can be measured as the separation between these two edges ^[23b].

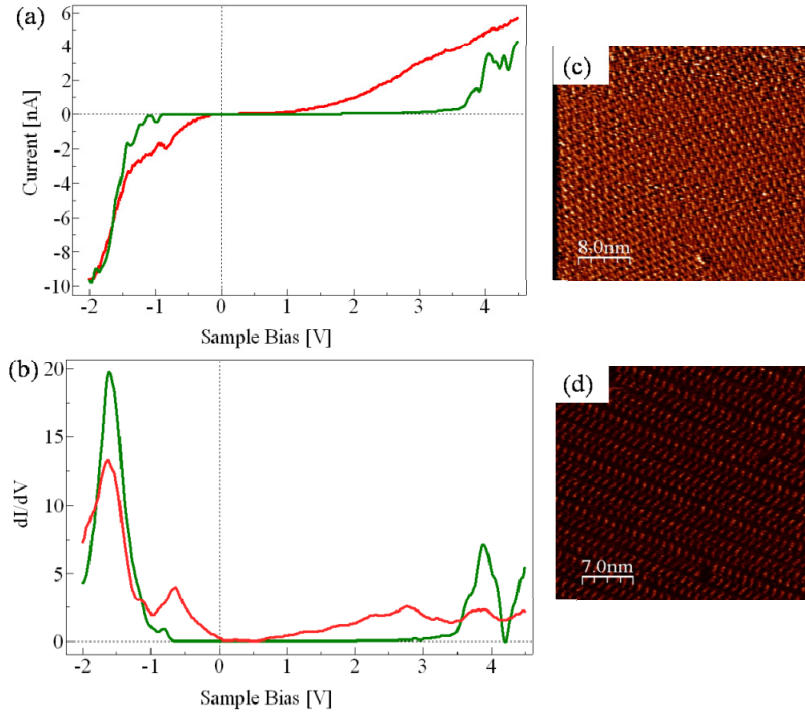


Figure 2.15 STS (a) and dI/dV - V curves (b) acquired with the tip located on DH4T (red) and DOTT (green) adlayers adsorbed on MoS₂ at liquid/solid interface; (c) and (d) example of corresponding STM images of DH4T and DOTT, respectively.

However, the value of experimentally observed gap around Fermi level does not correspond to the values in the literatures. We think that there are certainly interactions (convolutions) between layer and

MoS₂ DOS that do not allow determining the actual position of HOMO and LUMO band-gap.

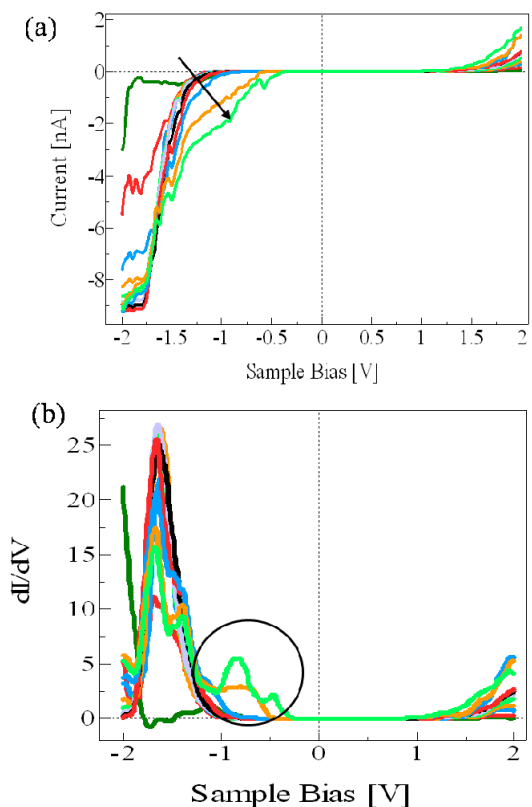


Figure 2.16 STS (a) and dI/dV - V curves (b) acquired with the tip located above the DH4T adlayer adsorbed on MoS₂ at liquid/solid interface. The different colors are corresponding to consecutive spectra recorded at the same location.

It should be noted that most STS measurements are reported under UHV-conditions. There are limited numbers of STS studies on

organic molecules at the liquid/solid interface. According to ^[30] the reason of this matter may come from the poor reproducibility of experiments caused by drift, presence of the liquid or/and the mobility of the adsorbate. In this sense, modifications of the I-V curves after consecutive STS measurements at a certain point, have also been sometimes observed at the liquid/solid interface (Fig.2.16). As it can be seen in Fig.2.16 (b) new peaks appeared after consecutive measurements. This is probably due to the removal of the molecules from the surface by the strong electrical field in the tunneling gap during the recording of the spectra. This hypothesis is strengthened when we compare the position of the new small peaks in Fig.2.15 (b) with the position of peak on bare MoS₂ at negative voltages (~ -0.8 eV) in Fig.2.13. ^[29]

2.4. Conclusions

The self-assembly properties of two alkyl-substituted oligothiophenes on MoS₂ were studied by STM both at the liquid-solid interface and in dry conditions. The experimental unit-cell parameters in the case of the liquid-solid interface were compared with the results of molecular modeling simulations to give insights into the supramolecular arrangement of the observed morphologies. Our results indicate that DOTT and DH4T form well-ordered monolayers at large scales on MoS₂, with interdigitated packing, in double-row lamellae (for DOTT) or brick-wall organization (for DH4T), while not having preferred adsorption sites and orientations.

The electronic properties of the self-assembled structures formed by DH4T and DOTT have been probed locally with scanning tunneling spectroscopy at the solution/MoS₂ interface. However, the values of the band gap could not be accurately determined because, on one hand, measurements were done at the liquid/solid interface and, on the other hand, our data on bare MoS₂ did not correspond to those reported in the literature which were frequently obtained in UHV conditions.

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* Chapter 3 *

Kelvin probe force microscopy study of organic thin-film transistors on SiO₂

Abstract

This chapter deals with the Kelvin Probe Force Microscopy (KPFM) study of Organic Thin-Film Transistors (OTFTs) on both native and modified SiO₂ gate dielectrics¹. The organic transistors are based on the three alkyl-substituted oligothiophenes which already introduced in previous chapters i.e. DH4T, DOTT and ddOD4T. After the optimization of the thickness of the active layers via modifications in thin-film preparation process, the morphology and local electronic properties of the devices under operation were investigated by AFM and KPFM, respectively. Different behaviors such as V_g -dependency, V_d -dependency, hysteresis and charge trapping effects were studied and are reported here. The role of the gate insulator modification with a self assembled monolayer (C₁₀) on

¹ Parts of this chapter have been published : 1. Afsharimani, N.; Nysten, B., Electronic properties of dioctylterthiophene-based organic thin-film transistors: A Kelvin probe force microscopy study. *Thin Solid Films* **2013**, 536 (0), 295-301.
2. Afsharimani, N.; Nysten, B., Scanning probe microscopy study of electronic properties in alkyl-substituted oligothiophene-based field-effect transistors. *Vacuum* **2013**, 90 (0), 17-24.

the above properties has also been studied. In order to have a better correlation between the microscopic and macroscopic properties, the performance of the devices was evaluated macroscopically, as well. Smaller and more densely packed crystals in addition to the more uniform films were observed on the silanized devices. Clear V_g and V_d dependency of the surface potential profiles were measured, in all cases.

3.1. Introduction

Organic thin film transistors (OTFTs) have recently drawn attentions due to their interesting features such as structural flexibility, low processing temperature and low production costs. However, there remain some fundamental issues related to the carrier charge transport in organic systems including charge injection at the interfaces between the organic films and the metal electrodes and electrical conduction near grain boundaries ^[3, 4]. Therefore, it is important to locally investigate the structure and the microscopic electrical properties of the active organic films.

Kelvin Probe Force Microscopy (KPFM) has the potential to directly provide correlations between the electronic properties and the local film structure. Moreover, with this technique it is possible to investigate the effects of contacts, structural defects and grain boundaries on device operation. Several research groups have already successfully applied KFM to measure the local electric potential profiles across the source and drain electrodes on OTFTs ^[5, 6]. Growing efforts have focused on determining the correlation between the device structure, film morphology and charge transport properties. For instance, it has already been shown that the contact resistances at the source and drain electrodes can significantly affect the current flow in OTFT devices especially, depending on the device geometry (top contact ^[7] or bottom contact [BC]) ^[8]. Hence, an effective approach to characterize the contact resistances is to map the potential distribution along the conducting channel during device

operation. At given values of V_D and V_G , a drop in potential along the channel represents the resistance of charge carrier transport.

Among the groups who used KPFM for imaging the surface potentials in BC polythiophene^[9] or pentacene-based devices^[10], Puntambekar and coworkers^[6a], for example, have studied the potential drop between the source and drain in TC and BC pentacene devices using KPFM. Figure 3.1 shows a schematic diagram of their KPFM measurement which was performed in lift mode for a BC device containing a vapor-deposited pentacene film^[6a]. They measured the surface potential using a nulling technique with the help of a feedback circuit. Figure 3.2 shows AFM topographic and surface potential images of BC and TC of devices with ~30nm thick evaporated pentacene films on SiO₂ substrates. According to this figure, there is a clear change in the morphology of the grown pentacene film between the channel and on the electrodes in BC device [Fig.3.2 (a)].

This discontinuity in the morphology which has also been observed by others^[8b, 11], resulted in potential drops near both the source and drain contacts. In the potential image [Fig.3.2 (b)], a potential drop of almost half of the drain potential is observed. This observation suggests that the presence of the discontinuous pentacene morphology at the source and drain plays an important role in charge transport. However, for the TC device, the AFM topography revealed uniform pentacene morphology with no discontinuous growth near the electrodes.

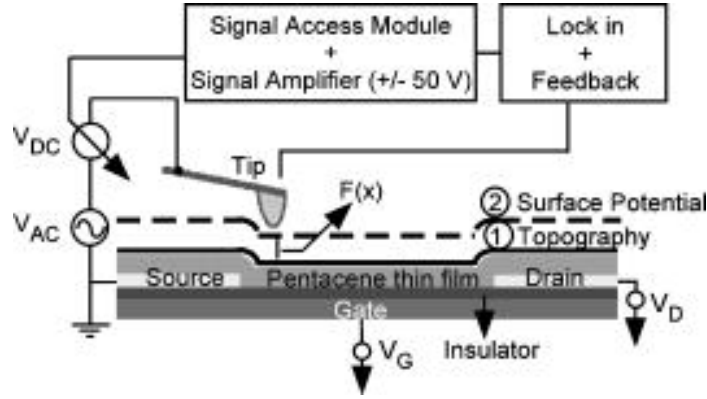


Figure 3.1 Schematic of the KFM setup for imaging potentials in a bottom pentacene TFT. Topographic and potential images are acquired simultaneously. After each topographic line scan (1), the tip is lifted off the surface (~ 10 nm) and the surface topography is retraced while recording the surface potential (2) (from Puntambekar et al.^[6a]).

Moreover, the surface potential image in Fig. 3.2 (d) showed a uniform potential distribution across the channel with small drop at the contacts and no sharp drop within the channel.

Puntambekar and coworkers have also measured the surface potential profiles for BC and TC device at different drain and gate biases. Figure 3.3 (a) shows profiles of the BC devices taken at fixed $V_D = -10$ V and different V_G between +40 to -40 V.

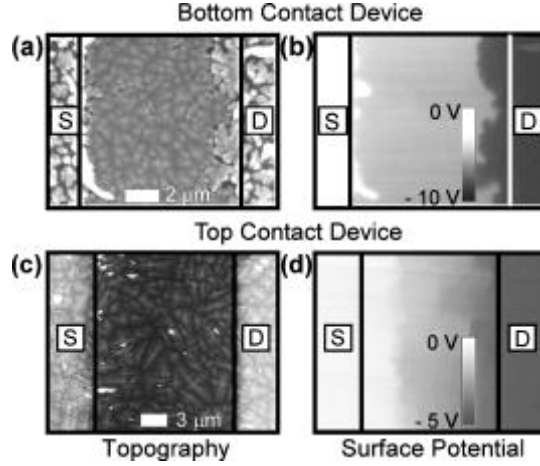


Figure 3.2 Topographic (a), (c) and corresponding surface potential images (b), (d) for BC and TC TFTs. $V_D = -10$ V for (b), $V_D = -5$ V for (d) and $V_G = 0$ V for both cases. Labels S and D indicate the source and drain electrodes, respectively. The solid vertical lines indicate the edge between the contacts and the conducting channel. For the BC TFT, length (l)/width (w) = $10\text{ }\mu\text{m}/100\text{ }\mu\text{m}$. For the TC TFT, the $l/w = 16\text{ }\mu\text{m}/300\text{ }\mu\text{m}$ (from Puntambekar et al.^[6a])

According to these profiles, there was a sharp drop in the potential at the source and drain when the device was turned on ($V_T \sim 27$ V). Contrary to TC device in Fig.3.3 (b), the BC transistor was contact limited because of the fact that the potential drop at the contacts (source + drain) became larger than the drop across the channel when the device was in linear regime. Nevertheless, in both geometries the contact and channel resistances decreased with the increasing (negative) gate bias but did not depend strongly on the drain bias.

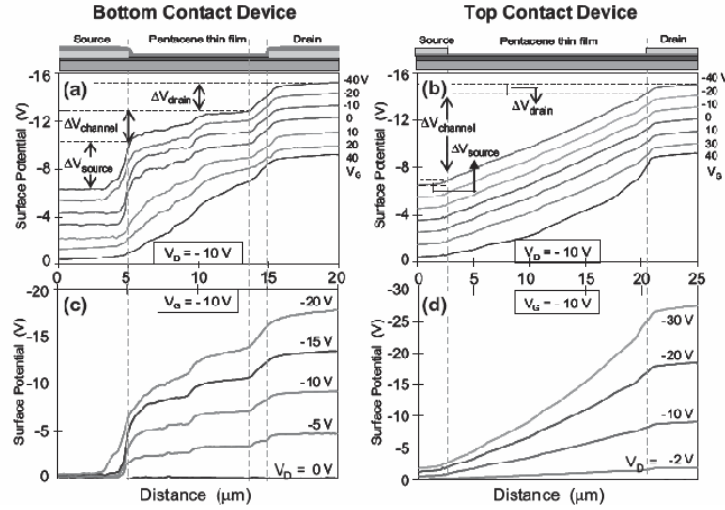


Figure 3.3 (a), (c) show a set of surface potential profiles for a BC TFT with a schematic of the device at the top for reference. For (a) $V_D = -10$ V and $V_G = 40$ to -40 V. The profiles are artificially offset for clarity of viewing. For (c) $V_G = -10$ V and $V_D = 0$ to -20 V. The channel length as defined by the lithography is $10\text{ }\mu\text{m}$. The outer dashed lines indicate the edge between the contacts and the channel. (b), (d) show a similar set of profiles for a TC TFT. In this case, the channel length was $\sim 18\text{ }\mu\text{m}$. The profiles in each device were taken at the same spot in the channel. Zero bias profiles are not subtracted from any of the data shown here. (from Puntambekar et al.^[6a]).

As another example, Xu and co-workers^[12] have studied the local potential distribution in tetrabenzoporphyrin (BP) bottom-contact thin-film transistor with atomic force microscope potentiometry. In their study, the presence of grain boundaries and cracks is shown to have imperious effect on the device performance. It is found that abrupt and considerable potential drops mainly appeared at the grain boundaries and cracks in the BP film when the transistor is under operation. In another study^[10] KPFM images of pentacene-based thin-film transistors showed potential drops both at the source contact and grain boundaries in polycrystalline pentacene films. However,

the potential drops were large at the source with the magnitude dependent on contact metal, compared to the potential drops at grain boundaries. The results showed that the device performance can be contact limited and in their case the carrier injection appeared to be much more difficult than extraction.

According to a study of OTFTs based on polytriarylamine (PTAA)^[13], simultaneous I-V and KPFM (in lift-mode) measurements of the current and potential profiles in the channel were correlated to all operating regimes of a transistor. (Fig.3.4)

Figure 3.4 (a) shows the drain current as a function of the applied gate bias of a pristine device while the drain bias was -9 V. For negative gate biases, a hole-accumulation layer is formed at the insulator/semiconductor interface and current between source and drain is flowing (I and II). For positive gate voltage the transistor is switched-off (III). The surface potential and the current were simultaneously measured. The obtained potential profiles are depicted in Fig.3.4 (b) for gate biases equal to -30 V, -10 V and 15 V.

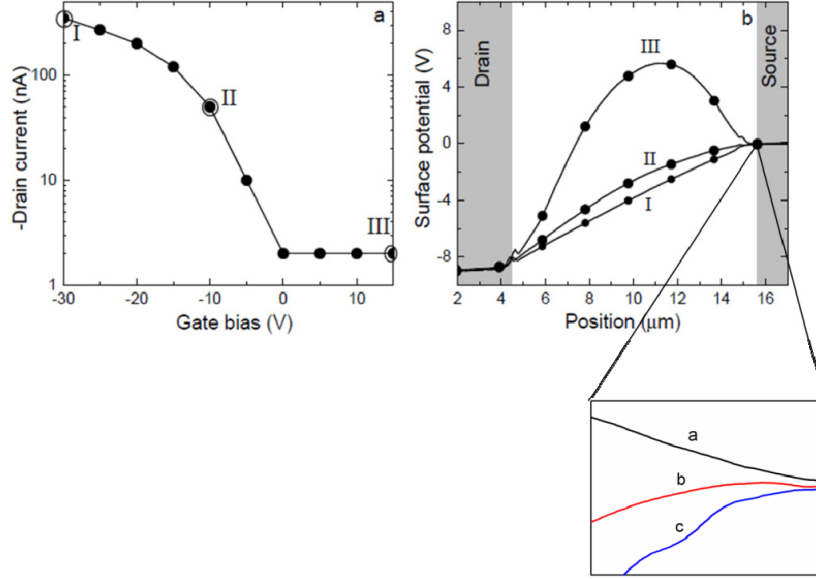


Figure 3.4 (a) Drain current of a PTA transistor as a function of gate bias. The drain voltage was -9 V . The source was grounded. (b) Potential profiles corresponding to the transfer curves shown in (a), indicated with I, II and III for gate biases of -30 V , -10 V and 15 V . (From ^[13])

Qualitatively, the potential profiles in the accumulation regime can be explained as follows. In the linear regime when the drain bias is much smaller than the gate bias, the charge density is only determined by the applied gate bias and the charge distribution is uniform over the channel. Thus, the lateral field due to the small drain bias is constant and the potential profile is a straight line (I). When the gate bias becomes larger than the drain bias, the charge carrier density distribution becomes non-uniform with a decreasing density from source to drain. By decreasing the charge carrier density, the conductance decreases and thus the lateral electric field decreases monotonically from drain to source due to the continuity of the current density. Therefore, the potential profile is curved (getting

convex) from drain to source, the situation which is known as “saturation” (II). This development in shape is visible in the potential profiles of Fig. 3.4 (b). When the applied gate bias is increased beyond the threshold voltage, the transistor channel is depleted and a potential barrier appears. This barrier prevents the positive charge carriers to move from the source to the drain electrode and hence the transistor is switched off, in agreement with the simultaneously measured negligible drain current at positive gate bias (III).

In our work we have looked at these qualitative changes as: (a) switched-off state (b) flat-band situation and (c) linear or saturation regimes depending on the applied gate voltage. (Shown in the zoom scheme of Fig.3.4 (b)). It should be noted that the presence of contact resistances and drops for e.g. at the grain boundaries in the potential profiles, make the precise interpretation and discrimination between the operating regimes sometimes complicated.

Charge trapping in organic electronic devices is another process which is not yet very clearly understood and is an important problem that strongly impacts the performance of such devices. Charge trapping and its following effects such as hysteresis and bias-stress effects are phenomena that referred to effects in either the semiconductor and/or the semiconductor/dielectric interface ^[14]. Organic semiconductors are known to contain a high density of traps resulting from grain boundaries, imperfect ordering, interface states and chemical impurities. For example, concurrent imaging by KPFM has revealed localized surface potential wells at the grain boundaries (GBs), indicating that GBs serve as charge-carrier traps ^[15]. Charge trapping near the semiconductor/dielectric interface, mainly due to hydroxyl groups on the gate dielectric surface ^[16], is usually believed to be responsible for threshold voltage shifts. However, in some cases, mobile ions in the dielectric or active material have been reported to have a dominant effect ^[7, 17].

In this chapter, the microscopic investigations of three different alkyl-substituted oligothiophene-based TFTs in which SiO₂ gate

dielectric has been either modified or not modified, are presented. The gate modifications has been done in turns with an alkylsilane in order to identify its influence on the electrical behaviors such as V_g – and V_d – dependency of the surface potential profiles, contacts and charge trapping effects.

3.2. Experimental part

Materials: DH4T, DOTT and ddOD4T were synthesized as described elsewhere ^[18]. Toluene (Fischer Scientific, HPLC grade) was used as solvent without further purification. In order to chemically modify the SiO_x surfaces, decyltrichlorosilane, (C₁₀), (ABCR, 97%) self-assembled monolayers (SAMs) were deposited prior to the active organic layer on SiO_x substrates in liquid-phase. Extra dry toluene (99.8%) and dichloromethane were purchased from Acros and used without further purification.

Deposition of SAMs: The silanization of the grid oxide of devices with C₁₀ was done in liquid (10 mM of C₁₀H₂₁Cl₃Si in extra dry toluene) under argon atmosphere. The samples, previously cleaned by 10 min UV-ozone exposure, were immersed in the solution at RT and left to react for 16 hours. Afterwards, they were rinsed in dichloromethane for analysis and dried with nitrogen.

TFT fabrication:

DOTT-based OTFTs: Bottom-contact OTFTs were fabricated with DOTT. Highly doped silicon wafers with a thermally-grown 126-nm-thick silicon oxide layer were used as the substrate. 70-nm-thick gold electrodes separated with a channel length of 50 μ m (width of 1 mm) were fabricated on the substrate using a lift-off technique. A 2-nm-thick Ti layer was deposited prior to gold as an adhesion promoter.

In order to perform KPFM, DOTT was deposited both on untreated and treated SiO_x grids. It was first dissolved in toluene at a

3%wt concentration. After sonication and filtration of the solution, the active layer was deposited by spin coating with a two steps procedure, i.e. $v_1 = 5000$ rpm, $t_1 = 60$ s and $v_2 = 5500$ rpm, $t_2 = 60$ s on preheated devices (80°C). The solvent was then allowed to completely evaporate. For the Macroscopic measurements, the DOTT solutions with the same concentrations were deposited by both spin-coating and drop-casting methods; though just drop casted devices showed FET behaviours.

ddOD4T-based OTFTs: Bottom-contact OTFTs were fabricated with ddOD4T. Highly doped silicon wafers with a thermally-grown 126-nm-thick silicon oxide layer were used as the substrate with 70-nm-thick gold electrodes and a 2-nm-thick Ti layer prior to gold as an adhesion promoter.

In order to perform KPFM, ddOD4T was deposited both on untreated and treated SiO_x grids. It was first dissolved in toluene at a 3%wt concentration. After sonication and filtration of the solution, the active layer was deposited by spin coating with a two steps procedure, i.e. $v_1 = 5000$ rpm, $t_1 = 60$ s and $v_2 = 5500$ rpm, $t_2 = 60$ s on preheated devices (85°C). The solvent was then allowed to completely evaporate. For the macroscopic measurements, the ddOD4T solutions with the same concentration were deposited by drop-casting method.

DH4T-based OTFTs: Bottom-contact OTFTs were fabricated with DH4T. Highly doped silicon wafers with a thermally-grown 126-nm-thick silicon oxide layer were used as the substrate with 70-nm-thick gold electrodes and a 2-nm-thick Ti layer prior to gold as an adhesion promoter. The channel length and the width of the devices were 20 μ m and 0.1 mm, respectively.

In order to perform KPFM, DH4T was deposited both on untreated and treated SiO_x gates. It was first dissolved in toluene at a 0.4%wt concentration. After sonication and filtration of the solution, the active layer was deposited by spin coating with $v = 5000$ rpm,

$t = 60$ s on preheated devices (150°C). Similar to the previous cases, drop-casted films were used for macroscopic I-V measurements.

Table provide the detailed process sheet used to fabricate standard OTFTs with standard source-drain electrodes. All sequences were performed in a class 100 cleanroom, starting from commercial boron highly doped ($\rho = 10^{-3}\Omega\text{cm}$) 3 inch silicon wafers. It is worth noting that within the procedures, thermal oxidation plays an important role in the performance of the OTFTs. Based on our observations, devices made by wet-oxidation procedure showed leakage problems probably due to the poor quality of the oxide layer. In contrast, devices which their dielectric layer made by dry-oxidation showed less leakage current perhaps due to the better quality of the oxide layer. Unfortunately, this phenomenon was not further studied.

Characterization method:

Structural characterization: X-ray reflectivity measurements were carried out with a modified Siemens D5000 2-circles goniometer fitted to a Rigaku rotating anode operated at 40 kV and 300mA, delivering Cu $K\alpha$ radiation of 0.15418nm wavelength. Monochromatization and collimation are achieved with the help of a collimating curved multilayered mirror, delivering a close-to-parallel beam of about 0.00850 angular divergence. The beam size is defined by a 40- μm -wide slit. The intensity is scaled to unit incident intensity and corrected for spill over at very low angles of incidence. The reflectograms are reported as a function of the wave vector of the incident photon from the interface in vacuum, i.e. $k_{z0} = (2\pi / \lambda) \sin\theta$ where λ is the X-ray wavelength and θ is half of the angle between the incident and reflected beam. For a well-ordered film, Bragg reflections can also be observed at certain k_z values. They give the spacing d of the individual layers which is related to the molecular length of the deposited organic material: $d = \pi / k_{z0}$. It is also possible to estimate the average thickness of a monolayer, d_0 , from the location of the first minimum in the reflectivity curve, $k_{z0,\text{min}}$. For a

thin organic film (below 4 nm), this minimum is related to the film thickness by the relationship: $d_0 = \pi / 2k_{z0, \text{min.}}$ ^[19]

Table 3.1. *Process sheet for OTFT fabrication with standard Au contacts.*

Step description	Products/Instruments	Parameters
Cleaning standard	H ₂ SO ₄ :H ₂ O ₂ 1:1	30 min.
	HF	15 s
Thermal oxidation	Koyo furnace	120 nm, 1000°C, 130 min.
Ellipsometry	Sentech	
Protective coating	Blue photoresist	Coating: 4000 rpm, 30s Baking: 160°C, 2 min.
Etching SiO ₂	BHF/ H ₂ O DI	1 min. / rinser dryer: 5 min.

Chapter 3

Metallization	e-gun Varian Al	200 nm, rotate, back, deposition rate: 1 Å/s
Photoresist stripping	HNO ₃ fuming/ H ₂ O DI	10 min./ rinser dryer: 5 min.
Annealing metal	Al	432°C, 30 min
Lithography	AZ 5214 , SÜSS, Mask aligner	Coating: 5400 rpm, 30s
Lift-off	SÜSS, Mask aligner	1 st bake: 110°C, 85s/ 1 st exposure: with mask 275 W, 2.3 s, vacuum
reversal	AZ 726 MIF H ₂ O DI	2 nd bake: 118°C, 45 s/ 2 nd exposure: blank mask 235 W, 9s, soft
		Development: 70 s Rinser dryer: 5 min.
Optical inspection	Polyvar	

Metallization	e-gun Vacotec Au	70 nm, lift-off, front. Deposition rate: 1 Å/s
Lift-off	acetone	50°C, ultrasonication 10 s
Protective coating	Blue photoresist	Coating: 4000 rpm, 30 s Baking: 160°C, 2 min.
Dicing	Tempress 602	10×20 mm ²

Microscopic electrical characterization: KPFM measurements were performed under ambient conditions on a Agilent 5500 SPM microscope (Agilent Technologies). PointProbe EFM probes (Pt/Ir-coated) (Nanosensors) were used. These probes typically have a resonance frequency around 120 kHz and a spring constant of a few N.m⁻¹. Topographic imaging and surface-potential mapping by KPFM were performed simultaneously using a dual lock-in. In this setup, the cantilever is mechanically excited close to its resonance frequency by the first lock-in and topographical images are classically acquired by maintaining the vibration amplitude at this frequency constant. Simultaneously a bias voltage, $V_{bias} = V_{DC} + V_{AC} \cos(\omega_{el} t)$, is applied to the tip with the second lock-in amplifier. The frequency ω_{el} of the AC component was chosen far from the probe resonance frequency, typically around 20 kHz. The tip-sample electrostatic interactions lead to an additional oscillation at the frequency ω_{el} proportional to the tip-surface electrostatic force.

The vibration amplitude at ω_{el} is measured with the second lock-in and is fed into a feedback loop that adjusts the DC bias to nullify the vibration amplitude. Under these conditions, mapping the value of V_{DC} allows to image the surface potential. Details about KPFM and its applications can be obtained in ^[20]. Figure 3.5 shows the experimental set-up for performing KPFM measurements.

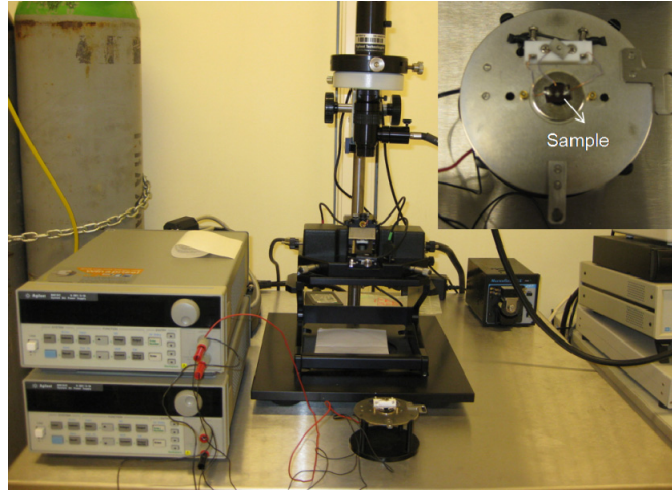


Figure 3.5 KPFM set-up used in this work. Inset: a close-up view of the fabricated OTFT ready for performing simultaneous topography and electrical measurements.

Charge trapping protocol: In order to study charge trapping in our devices we followed the protocol shown in Fig.3.6 (b). The principle of the trap state spectroscopy is the following. In a first step, the trap states are populated by operating the transistor in on-situation where the gate voltage is above the threshold voltage. Subsequently, the transistor is switched-off. This drives all the mobile charges out of the accumulation layer and only trapped charges remain. Since our experiments last for several minutes, they reveal deep traps with long life-time for which the dynamics is slow and the trap-release happens

on time scales much larger than 1s at room temperature. Finally, by consecutive scanning of the surface, one can map the surface potential profiles related to the trapped charges. This procedure is shown in Fig.3.6 (a) from top to bottom, respectively.

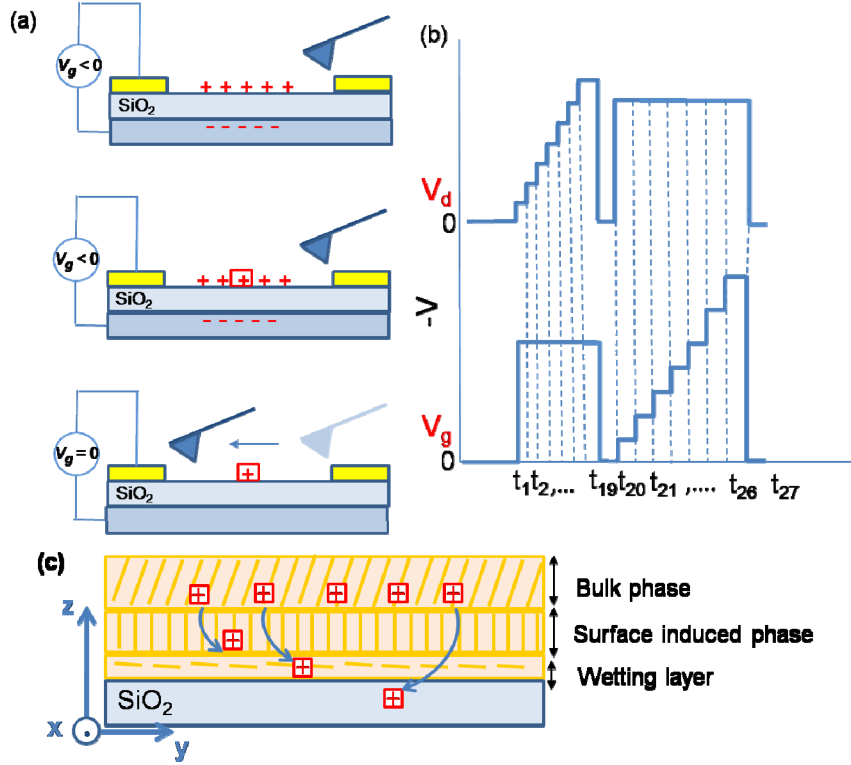


Figure 3.6 (a) Schematic representation of the trap state spectroscopy. (b) Corresponding protocol of tuning the V_g and V_d in our TFTS in order to study charge trapping phenomena. (c) Schematic representation of the possible location of trapped charges with respect to the different morphological phases of the semiconducting film including: wetting layer, surface-induced phase and bulk phase.

According to the literatures ^[21, 22], there may be different phases in semiconducting film deposited on SiO₂ substrate including a wetting layer at the very interface with the SiO₂ surface which may in turn be followed by a thin-film induced phase and a bulk phase as shown in Fig.3.6 (c). It is worth noting that the position of trapped charges may be influenced by the presence of these morphological phases. This means that a charge can either be trapped on top of the layers of the film (bulk phase) or in the bottom layers (surface-induced phase) or at the interface with SiO₂ (wetting layer) or even, inside the gate dielectric. These situations are shown in Fig. 3.6 (c). As the KPFM measurements are performed in the plane of x-y axes, getting information along the z-direction and knowing the exact position of the trapped charges is not possible.

Macroscopic electrical characterization: The current-voltage measurements were executed under ambient conditions using a low signal probe station with probeshield (PM8PS). 4 SMU's with 10 fA resolution 2 SMU's with 0.1 fA resolution. The gate and drain voltages are swept over a specific range and the corresponding drain current is measured. Because of the variety of transient effects, the V_g and V_d are set to the initial values which are then held for a pre-selected time (*hold time*) prior the voltage sweep. Each voltage step is followed by a *delay time* before measuring the appropriate current. Since the hold and delay times can impact the measured curves, they should be chosen so that an equilibrium is acquired between a steady state regime and the device aging. Similar to ^[23] we set the hold and delay times to 40 s and 0.5 s, respectively.

3.3. Results and discussion

3.3.1 KPFM study on DOTT-based OTFTs

3.3.1.1 Crystal size optimization

In OTFTs, electrical conduction is generally confined within a few monolayers close to the grid oxide surface^[5]. Therefore, films which are obtained by evaporation or spin-coating methods could be more preferred compared to those which generally formed by drop-casting since they propose smoother, more uniform and thinner films. However, it should be noticed that, in practice, macroscopic characterization of devices based on spin-coated films generally show poor electronic properties compared to the drop-casted films. In contrast, devices based on spin-coated films are more suitable for performing microscopic measurements like KPFM since they propose smoother, more uniform and thinner films. These observations have been also confirmed by Marohn's group^[24] which have reported on the differences observed in macroscopic and microscopic properties of spin-coated and drop-casted TIPS pentacene-based transistors.

Previous structural analyses of DOTT thin films including XRR, AFM, TEM and electron diffraction^[25] have shown that DOTT thin films spin coated on pure or silanized SiO₂ substrates present a layered structure. At room temperature, in the crystalline phase, the thin film structure is the same as that of bulk DOTT with the same in-plane and out-of-plane lattice parameters. In that phase, the DOTT molecules are oriented perpendicular to the substrate surface. The film morphology consists in large crystallites, a few micrometers in size, dispersed on an almost continuous very thin film of DOTT. When heated up to higher temperatures, in the corresponding smectic phases, the DOTT thin films retain their layered structure while DOTT molecules are slightly tilted with respect to the substrates.

On that basis, before performing KPFM measurements on our devices, we also tried to modify the film morphology by optimizing the preparation method. Therefore, two strategies were used. First, we tried to deposit the molecules on pre-heated substrates in order to decrease the thickness by transferring them into the liquid crystalline phase and second, we tried to modify the spin-coating parameters. We spin-coated DOTT films on native SiO₂ from either 0.4% or 3% (w/w in toluene) solutions with different speeds. After different deposition parameter testing, it was found that the best spin-coating conditions are achieved for a two-step process regardless of the solution concentration. Figure 3.7 shows the optical microscope images of the DOTT films from 3% solution concentrations deposited at different temperatures and spin-coating parameters on native SiO₂ substrates. According to the images, DOTT molecules form crystals in a dispersed fashion with a relatively homogeneous film underneath. However, applying a two step spin-coating process together with the pre-heating of the substrate resulted in a more homogeneous film without any large crystals on top [Fig.3.7(c)].

The formation of multilayers and the homogeneity of the DOTT film underneath prepared by a two-step spin coating process were also confirmed by the XRR characterization. Figure 3.8 (a) and (b) show the optical microscope images of the DOTT films from 3% solution concentrations deposited at different spin-coating parameters on native SiO₂ substrates at $T \sim 80^{\circ}\text{C}$ with $V=5000$ rpm, $t=60$ s and $V_1=5000$ rpm, $t_1=60$ s, $V_2=5500$ rpm, $t_2=60$ s, respectively.

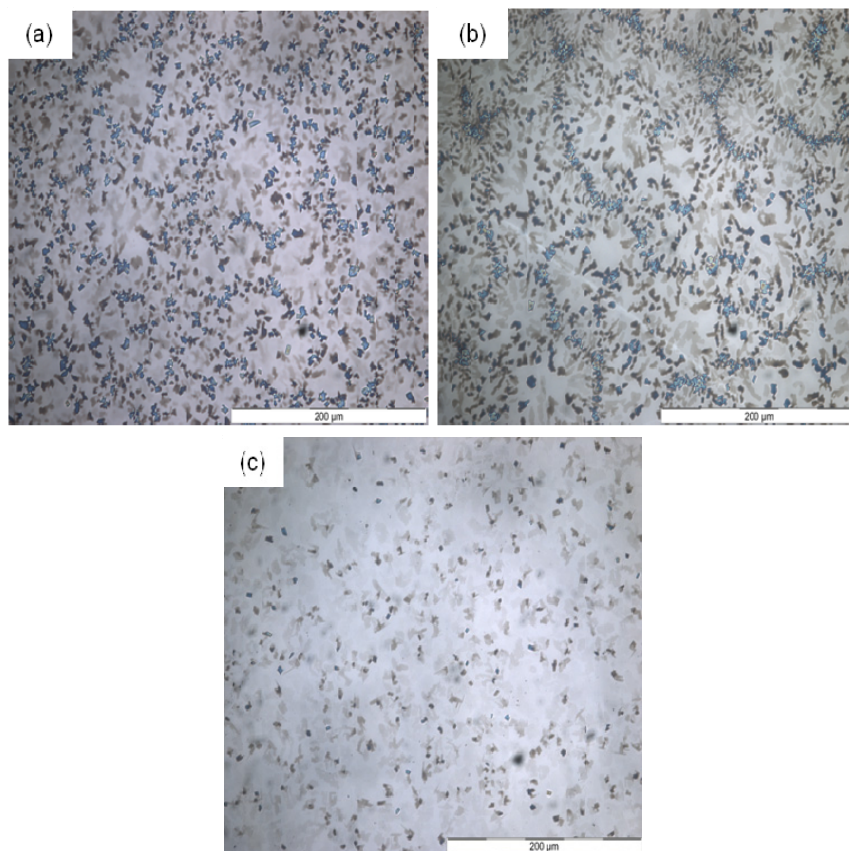


Figure 3.7 200 μm scale optical microscope images of the DOTT films from 3% solution concentrations deposited at different temperatures and spin-coating parameters on native SiO₂ substrates; (a) $V=3000$ rpm, $t=30\text{s}$, $T \sim 80^\circ\text{C}$ (b) $V=3000$ rpm, $t=30\text{s}$ at RT and (c) $V_1=3000$ rpm, $t_1=30\text{s}$, $V_2=5500$ rpm, $t_2=60\text{s}$ at $T \sim 80^\circ\text{C}$.

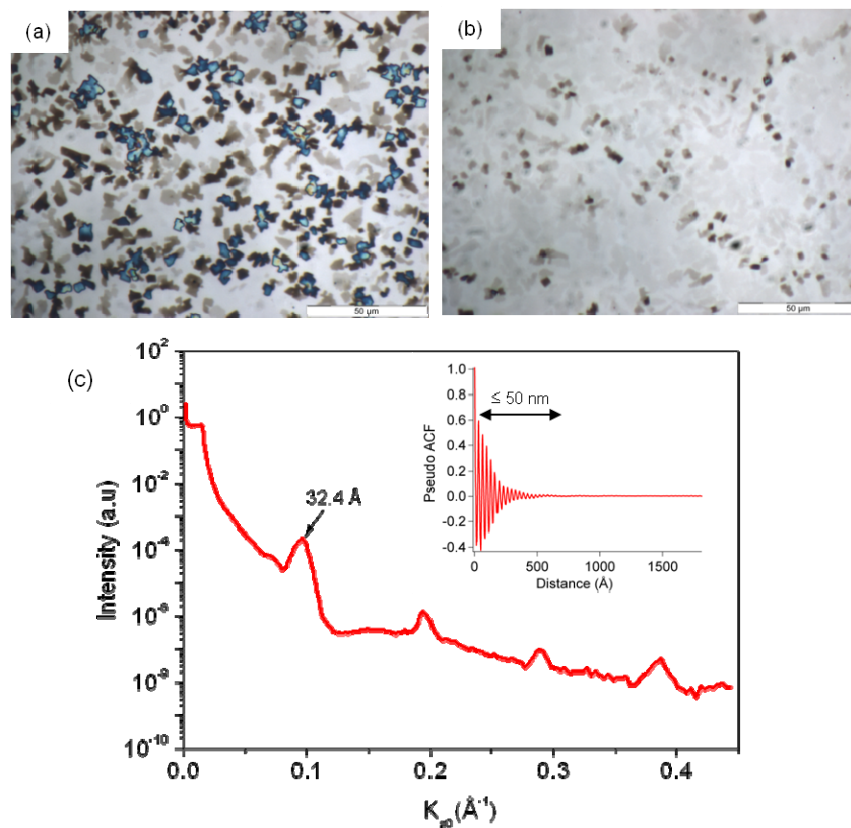


Figure 3.8 A $50\text{ }\mu\text{m}$ scale optical microscope images of the DOTT films from 3% solution concentrations deposited at different spin-coating parameters on native SiO_2 substrates at $T \sim 80^\circ\text{C}$; (a) $V=5000$ rpm, $t=60$ s, (b) $V_1=5000$ rpm, $t_1=60$ s, $V_2=5500$ rpm, $t_2=60$ s. (c) X-ray reflectogram of the sample in (b). Inset shows the corresponding Patterson function derived from the reflectogram.

As has been shown earlier ^[25], the films grown on Si/SiO₂ by spin-coating present a regular layered structure of DOTT molecules. This is supported by the presence of Bragg peaks in the XRR spectra [Fig. 3.8(c)]. The position of the Bragg peaks yields an interlayer repeat unit of 32.4 Å that approximately matches the full extended length of a DOTT molecule. This implies that the smectic layer stands parallel to the substrate and that the DOTT molecules lie perpendicular or slightly tilted with respect to the substrate. The inset of Fig. 3.8(c) presents the Patterson function. This function is obtained from the Fourier transform of the X-ray reflectivity and it gives information in direct space on the roughness and variation of the electron density in the thin film. The regular oscillations of the Patterson function decrease when the distance from the substrate increases. The decay length of these oscillations corresponds to the height up to which perpendicular layers are regularly stacked, i.e. the size of coherently-scattering domains.

3.3.1.2 Surface potential measurement of DOTT-based OTFTs

KPFM was used in order to *simultaneously* study the structural properties and the electric potential profiles of bottom-contact OTFT devices based on DOTT. In KPFM, the measured surface potential, V_{sp} , is equal to $V(x) + \Delta\phi(x)$, where $V(x)$ is the local potential and $\Delta\phi(x)$ is the difference between the work function of the tip and the sample (contact potential). The effect of $\Delta\phi(x)$ can be removed by doing scans at zero drain and gate bias voltages and by subtracting the measured contact potential to the scan measured with biased electrodes as in reference ^[5].

Macroscopically, it has been shown that transistors based on DOTT molecules exhibit *p*-type behaviour; i.e., the channel majority carriers are holes. A schematic of the experimental setup and a typical transfer curve of both treated and untreated devices at

constant drain voltage $V_d = -5$ V are shown in Fig. 3.9. It has been shown that the control of the molecular structure and morphology of the organic semiconductor at the semiconductor/dielectric interface by applying the self-assembled monolayers (SAMs) can enhance the performance of OTFTs. Widely used as molecular platforms in the fabrication of OTFT on oxide surfaces, alkylsilanes are known to affect grain size and to improve the charge transport^[26]. As expected, the larger current values in our study are also obtained for the devices with C₁₀ modification of the grid oxide. Moreover, the threshold voltage (V_{th}), defined as the gate voltage above (below) which the source-drain current varies linearly with the gate voltage, is approximately equal to -5 V in the treated device, a value shifted towards lower values compared to that estimated on the sample without grid surface treatment, $V_{th} \approx -14$ V. These observations confirm that the use of self-assembled monolayers (SAMs) indeed allows enhancing the performance of OTFTs.

Figure 3.10 shows topography, typical potential image and potential profiles obtained for a 50 μ m wide-channel transistor without gate surface modification. According to the topography (Fig. 3.10(a), (b)), line profile measurements and phase image, the whole channel surface is covered with a uniform DOTT film with, on top of it, flat crystals. A typical surface potential image is presented in Fig. 3.10 (c) ($V_d = -4$ V, $V_g = -10$ V). The surface potential profiles at various drain and gate voltages were extracted from the surface potential images along the blue line indicated in Fig. 3.10 (a). The surface potential profiles presented in figure 3.10 (d) were acquired at different gate voltages (-20 V $\leq V_g \leq 0$ V) for a fixed drain voltage ($V_d = -8$ V). The vertical dotted lines mark the geometrical edges of the source and drain located on the right and left, respectively.

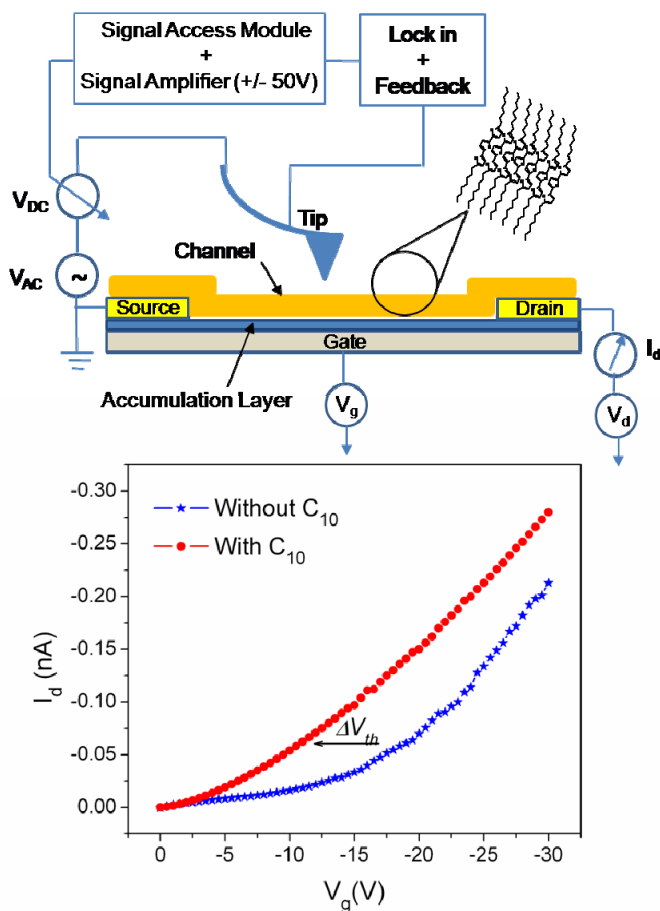


Figure 3.9 Up: Schematic of the experimental setup and the OTFT structure. The chemical structure of DOTT molecules is shown, as well. Down: Typical transfer characteristics of a DOTT-OTFT with $50\ \mu\text{m}$ channel length for both treated and untreated SiO_x gate dielectric ($V_d = -5\ \text{V}$). Threshold voltage shift shown as ΔV_{th} .

The gate-voltage dependency of the profiles may be clearly observed. This is one of the key features of these experiments with KPFM because it confirms that the measured potential, which in principle is a surface property, is governed by the interfacial potential in the accumulation layer. Bürgi and co-workers have truly shown the importance of measuring the interfacial potential with KPFM technique. They have taken potential profiles on a P3HT-based transistor for which the dielectric was patterned into hydrophobic and hydrophilic regions, the hydrophobic region being obtained using hexamethyldisilazane (HMDS) treatment. The resulting step-like increase of the mobility in HMDS treated region was clearly reflected in the measured potential profile ^[5].

From the profiles in Fig. 3.10(d), a threshold voltage of ~ -10 V was estimated as the gate voltage value at which the measured surface potential do not anymore linearly follows the gate voltage due to the charge accumulation in the channel. This value is different from the one that was determined on the same device from macroscopic measurements (~ -14 V). This difference may be due to charge trapping effects in the device under prolonged operation in ON condition during I - V measurements. Since KPFM measurements were performed a few days after the macroscopic characterization, it is possible that trapped charges were released and caused the shift of V_{th} towards lower values. The shift of V_{th} under prolonged operation may be due to mobile charge carrier trapping in the channel on pre-existing or stress-generated localized states in the semiconductor, in the gate dielectric or at the active interface. These trapped charges no longer contribute to the current, but are still part of the electrostatic charge on the gate dielectric induced by the gate voltage [see Figure 3.13 and charge trapping discussion].

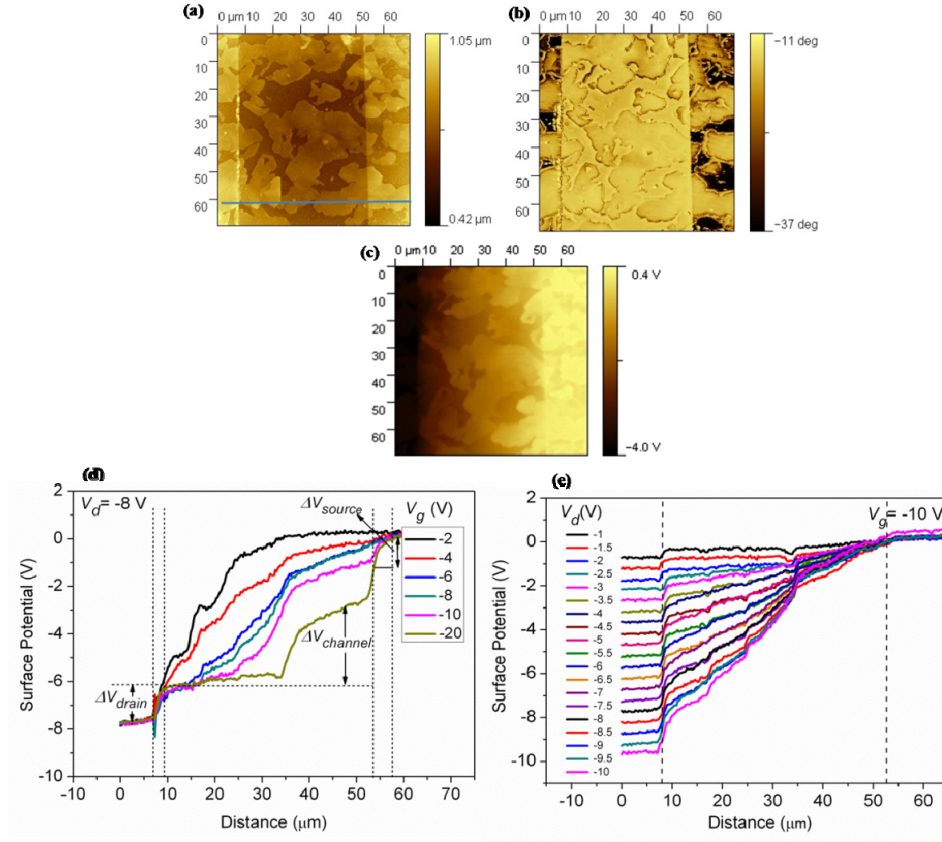


Figure 3.10 Potentiometry of DOTT/SiO₂ thin-film transistor (50 μm channel length). (a) $70 \times 70 \mu\text{m}^2$ topographic image; (b) phase image; (c) corresponding surface potential image at $V_d = -4 \text{ V}$, $V_g = -10 \text{ V}$; (d) potential profiles acquired along the horizontal line shown in (a) as a function of gate voltage, with $V_d = -8 \text{ V}$; (e) potential profiles as a function of drain voltage, with $V_g = -10 \text{ V}$; the vertical dotted lines indicate the edge between the contacts and the conducting channel.

Thus, applying a higher gate voltage is needed to achieve the same mobile carrier concentration and current^[27]. As the device turns on ($V_{th} \sim -10$ V), surface potential drops are observed at the source and drain electrodes. These drops appear to be smaller than those observed in the channel, indicating that the device is not mainly contact limited. The effective drop at the source or drain somewhat extends into the channel because of the extension of the grain growing off the contact into the channel, as shown in Fig. 3.10 (a). Profiles in Fig. 3.10 (d) also show a potential drop in the channel which develops as the device turns on. This is due to the cracks and grain boundaries in the film which are frequently observed in bottom contact OTFTs^[28].

Figure 3.10 (e) shows the surface potential profiles in the channel at fixed $V_g = -10$ V with V_d varying between -1 and -10 V. In these profiles, increasing potential drops are observed both across the channel and at the drain contacts with increasing V_d .

Figure 3.11 shows topography, typical potential image and potential profiles obtained for a ~ 50 μm wide-channel transistor with surface modification (C_{10} alkylsilane) of the gate oxide. These molecules are often used as molecular platform in the fabrication of OTFTs on silicon oxide surfaces, since they are known to affect the grain size and improve charge transport^[26]. The quality of the silane layer on our SiO_2 substrates was checked by water contact angle measurements and X-Ray Reflectivity (XRR). The autocorrelation function of the electronic density profile obtained from the reflectogram showed the formation of a C_{10} layer with a thickness of 12.6 Å. [see Fig. 3.12]

Based on the topography [Fig. 3.11 (a)] and line profile measurements, DOTT seems to have properly covered the channel surface as for the untreated device. However, in this case the number of crystals increased and their lateral size seems to be smaller. They also seem to be more densely packed with less regions not covered by crystals. An example of a surface potential image taken at $V_d = -4$ V and $V_g = -10$ V with respect to the source electrode, is shown in Fig. 3.11 (b). The surface potential distribution is uniform across the channel and slightly decreases from source to drain electrode. The surface potential profiles at different gate voltages ($-10 \text{ V} \leq V_g \leq 0 \text{ V}$) for a fixed drain voltage ($V_d = -8 \text{ V}$) are shown in Fig. 3.11(c). The vertical dotted lines mark the geometrical edges of the source and drain located at the right and left, respectively. In this case, the threshold voltage is estimated to be around ~ -4 V.

For this device with silanized gate dielectric, there is almost no shift in threshold voltage between the macroscopic and microscopic measurements. This may be due to the effect of silanization which may suppress the hysteresis and charge trapping effects (see Fig. 3.14 and Fig. 3.15 and related discussion). As the device turns on, a potential drop appears at the source contact. The voltage drops at the source and drain contacts are also smaller than that of the channel, showing that the device is not contact limited. In addition, no sharp potential drop is observed in the channel compared to the untreated device [Fig. 3.10(d)], especially at high voltages. This may be due to the effect of silanization which has affected the formation of the crystals on top of the channel and modified the grain boundaries.

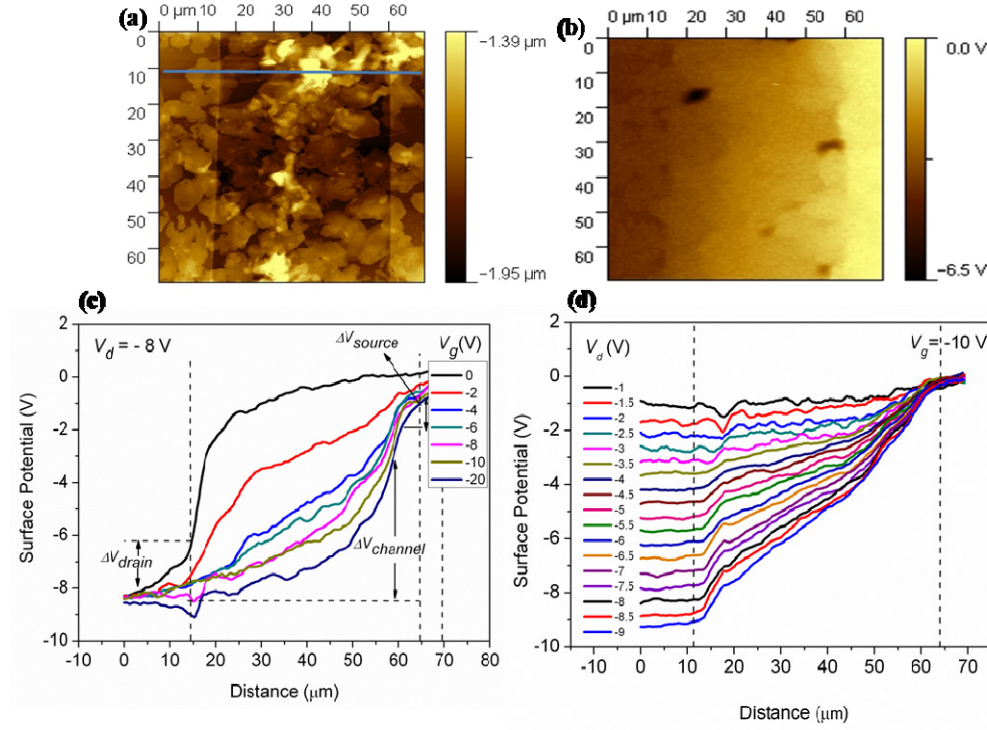


Figure 3.11 Potentiometry of DOTT/C₁₀/SiO₂ thin-film transistor (50 μm channel length). (a) 70×70 μm² topographic image; (b) corresponding surface potential image at $V_d = -4$ V, $V_g = -10$ V; (c) potential profiles acquired along the horizontal line shown in (a) as a function of gate voltage, with $V_d = -8$ V; (d) potential profiles as a function of drain voltage, with $V_g = -10$ V; the vertical dashed lines indicate the edge between the contacts and the conducting channel.

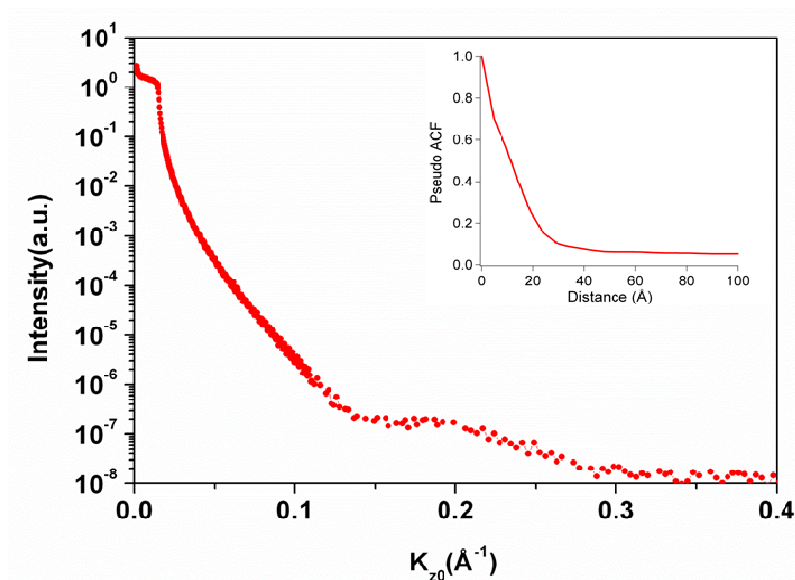


Figure 3.12 XRR and corresponding autocorrelation function (inset) of the electronic density profile for C₁₀ layer deposited on SiO₂ substrate.

A schematic model of how the surface treatment can improve the surface structure and morphology of the film by modifying the molecular ordering and grain boundaries is shown in Fig. 3.13. According to this model, modifying the dielectric surface with SAMs helps the molecular ordering and eliminates structural disorder which later acts as traps. The improved surface chemistry can lead to a better π - π stacking ^[29], resulting in an increase of the charge carrier mobility as shown in Fig.3.13. Moreover, the water-related trap formation due to the hydrophilic SiO₂ surface can be neglected after the treatment and consequently, several transistor parameters like a shift of threshold voltages are modified.

3.3.1.3 Charge trapping and hysteresis effects

In order to study charge trapping effects, KPFM measurements were realized by varying V_g and V_d according to certain protocols consisting in the progressive biasing of the devices followed by their switching off and the KPFM measurement of the surface potential (see the experimental section). As it can be seen in Fig. 3.14 for the untreated OTFT, a positive electrostatic potential is observed in the channel after biasing the device in the on-state for an extended period of time and then switching it off, except after the first polarisation ramp that was realized with $V_g = 0$ V. For the two other polarization ramps realised with a negative bias of the gate, large surface potential values were measured in the channel, attributed to the presence of trapped charges. The accumulation of these charges is illustrated by the KPFM images in Fig.3.14(c) and (d) and the corresponding profiles (red and blue curves).

Figure 3.15 presents the KPFM images and the surface potential profiles obtained on a silanized OTFT after biasing ramps in the on-state and the switching-off in the off-state. As it was the case for the untreated OTFT, a positive surface potential is measured in the channel after polarization of the device with a negative bias voltage applied to the grid, suggesting again the presence of trapped charges. After the second ramp, the measured surface potential is much larger than after the first one. This is consistent with the fact that the gate voltage was decreased down to -20 V, compared to the -10 V value applied during the first ramp. The comparison of Fig. 3.14(a) and 3.15(a) indicates that charge trapping occurs along the whole channel for both devices.

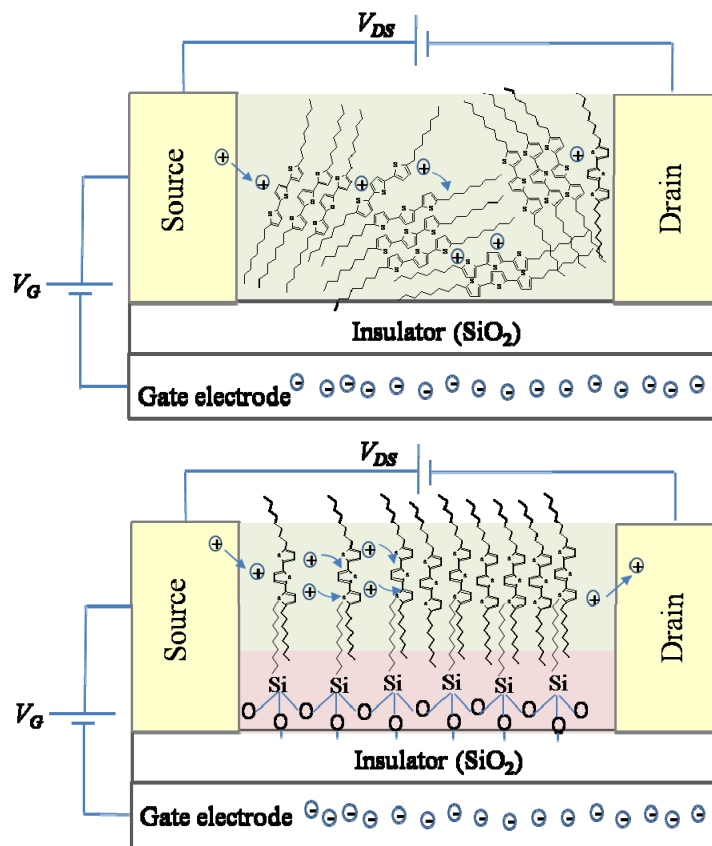


Figure 3.13 Schematic model of the surface treatment effect on DOTT structure before (up) and after (down) silanization. It should be noted that in this scheme only the surface-induced phase of the semiconducting film has been shown.

In addition, in the case of the untreated device, charge trap density varies smoothly along the channel indicating a more or less homogeneous trap state density; while in the treated device charge trap density is inhomogeneous suggesting that in this case defect states near source and drain contacts and/or at grain boundaries play a major role in charge trapping. However, when we compare potential profiles obtained in the same conditions on the silanized and the untreated devices (Fig. 3.15 (c and blue curve) and Fig. 3.14 (c and blue curve), respectively), one clearly see that the surface potential, i.e. the amount of trapped charges is much lower on the silanized device.

In order to have a better understanding of the trap formation, we also monitored the surface potential as a function of biasing time and we calculated the density of trapped charges for both the treated and untreated devices. The surface potential profiles as a function of bias-stressing time have been collected in 3 different regions of the channel including: crystals (Cryst.), inter grain regions (IGR) and grain boundaries (GB). The thin films in our devices were observed to contain relatively thick DOTT islands separated by regions in which the DOTT film is much thinner. In accordance with Tello and co-workers^[30], these thin regions were referred to inter grain regions (IGR). It is shown that an incomplete accumulation layer can be formed in these thin regions and thus they may be considered as preferential place for charge trapping. The experiment was performed first, by taking a topographic scan over a relatively large area and after, one line scan which crossed a few large IGRs between the DOTT grains (e.g. blue line in Fig. 3.14 (b)) was selected and surface potential was measured along this line. [See Appendix for more details.]

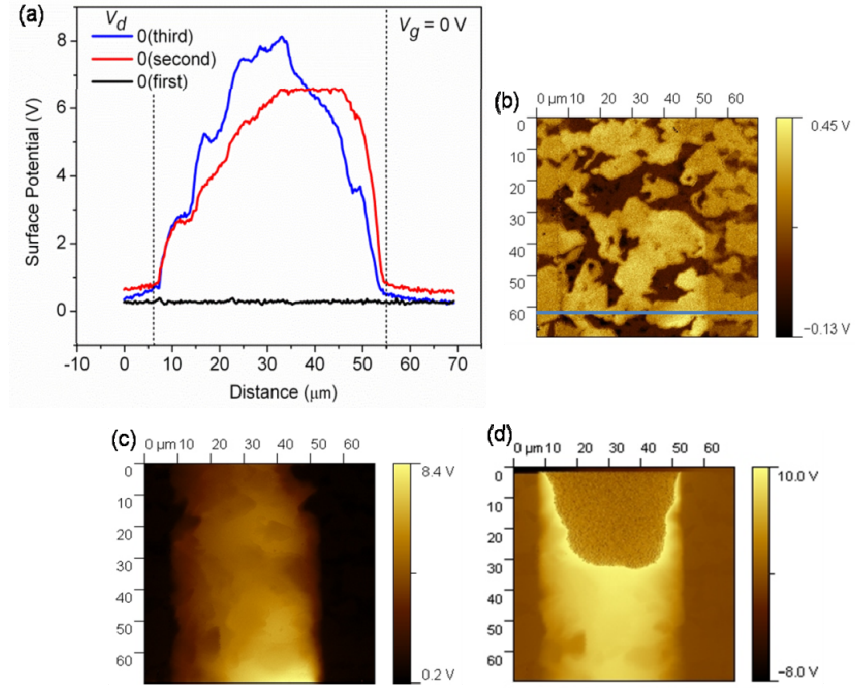


Figure 3.14 (a) Surface potential profiles (along line shown in (b); (b-d) KPFM images obtained on an untreated OTFT after polarization and switching-off the device. (b) and black): initial off-state; (c) and red): after ramping V_d down to -10 V (0.5 V steps) with $V_g = -10$ V; (d) and blue): after ramping V_g down to -20 V (2 V steps) with $V_d = -8$ V; the effect of a charged-tip is seen in the top part of the image (d) which disappeared after few minutes by continuing the scanning perhaps due to a charge compensation between the tip and the surface.

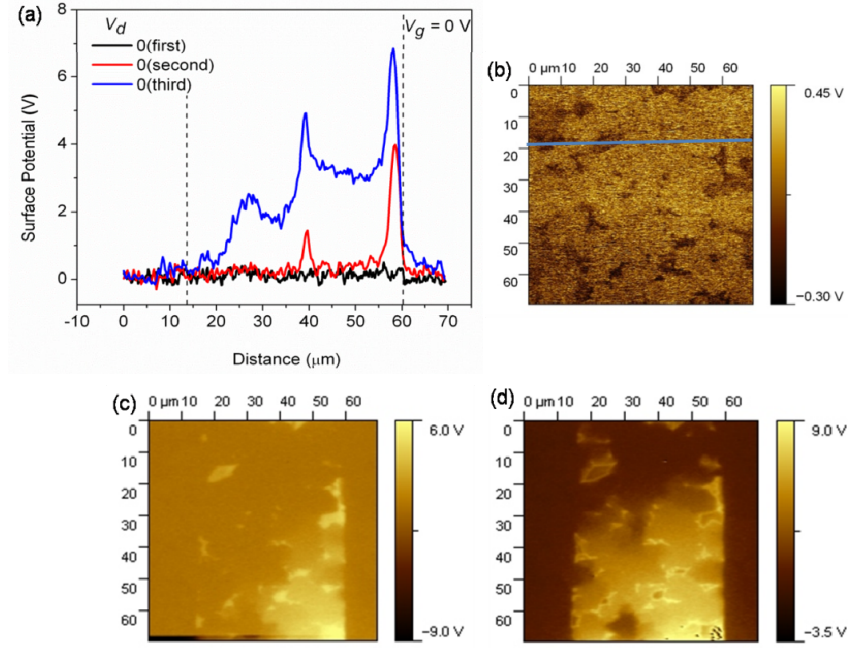


Figure 3.15 (a) Surface potential profiles along line in (b); (b-d) KPFM images obtained on a silanized OTFT after polarization and switching-off the device. (b and black): initial off-state; (c and red): after ramping V_d down to -10 V (0.5 V steps) with $V_g = -10$ V; (d and blue) after ramping V_g down to -20 V (2 V steps) with $V_d = -8$ V.

A scheme of the charge trapping process is shown in Fig.3.16. The pristine transfer curve exhibits a positive pinch-off voltage commonly observed when using SiO_2 as gate dielectric. The origin is referred to fix negative interface charges.^[31] Upon grounding all electrodes, the interface charges are compensated by mobile holes injected into the semiconductor. The interface charges are screened and the surface potential is therefore 0 V over the channel, as shown in Fig.3.16 (a).

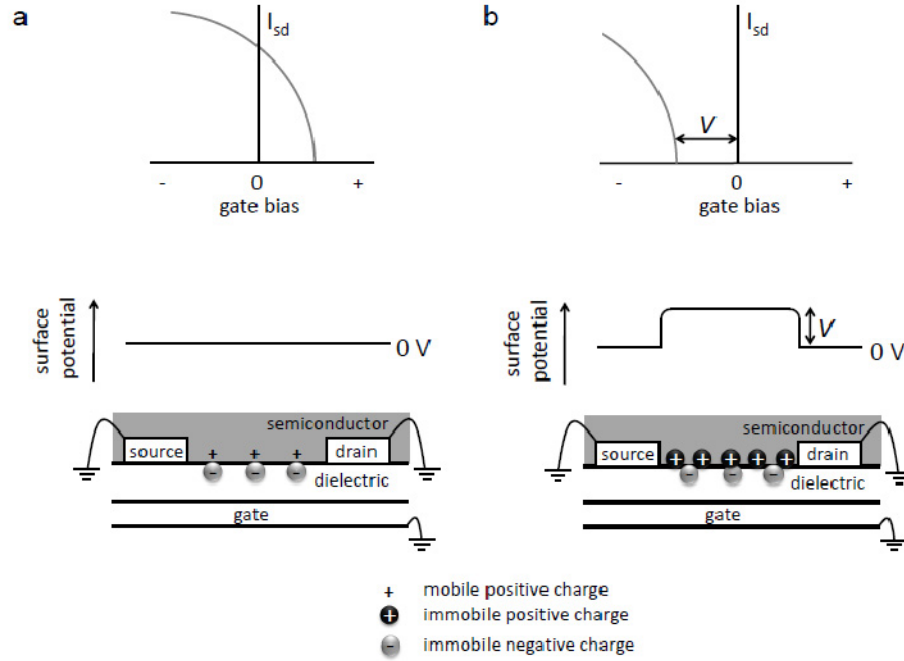


Figure 3.16 Scheme of the charge trapping process. (a) The top image shows a schematic representation of a transfer curve with a positive threshold voltage. A positive threshold voltage indicates that negative immobile charges are present in the gate dielectric which is compensated by mobile holes in the semiconductor. The resulting surface potential is then zero everywhere as shown in the bottom image. (b) Schematic representation of a transfer curve with a negative threshold voltage (top), indicating that positive charges are trapped, which give rise to a positive surface potential in between source and drain as shown in the bottom image. (From ^[13])

When a continuous gate bias is applied, the transfer curve gradually shifts to the applied gate bias, caused by trapping of charge carriers. With time, the density of positive trapped charges becomes

larger than that of the negative interface charges. As a result, the pinch-off voltage is shifted below 0 V, as shown in Fig. 3.16 (b). For a *p*-type semiconductor that does not transport electrons, when the electrodes are grounded, the immobile charges cannot be compensated. Thus, the surface potential remains non-zero and increases with the net immobile charge density and hence with the pinch-off voltage. As mentioned before, the exact molecular-level nature of these trapping sites and their location is not yet understood.^[32] KPFM cannot distinguish between charge trapping in the dielectric or in the semiconductor.

Figures 3.17(a) and 3.17(b) show the surface potential profiles obtained in these regions for the untreated and treated devices, respectively. Each point in the diagrams is an average of three surface potential values obtained along three different lines at the top, centre and bottom of the KFM images in Fig. 3.14(b) and 3.15(b).

The surface potential increases less rapidly on the treated device than on the untreated one. The larger increase of the surface potential in IGR areas for the treated device indicates that the charge traps are more likely to appear in these regions than in the crystalline ones.

The density of trapped charges was estimated from the surface potential profiles taken at $V_g = 0$ V using the equation $V_{th} = V_g + \sigma_{trap}/C$. In this equation σ_{trap} is the areal density of trapped charges and C is the gate capacitance per unit area. The difference in work function between the tip and the sample has been neglected for simplicity^[33]. Based on this equation, it is possible to obtain a map of the trapped charge density directly from the measured KFM signal. Figure 3.17(c) provides a visual comparison of the maximum of σ_{trap} in the Cryst., IGR and GB regions for both the treated and untreated devices. The larger values of σ_{trap} are obtained for the device without gate surface modification. On the other hand, the major part of the trapped charges belongs to the thin IGRs for both devices. The maximum of σ_{trap} in IGRs is calculated to be 190 nC.cm^{-2} and

110 nC.cm⁻² for the untreated and treated devices, respectively. Trapped charges reside in deep trap states without contributing to the transistor current and give rise to a shift in the threshold voltage towards more negative voltages by the amount which is corresponding to σ_{trap}/C [33]. However, the deep trapped charges can be released on long time scales, e.g. after several days, shifting back the threshold voltage towards more positive values. This effect was observed in the unmodified device while performing the microscopic measurements several days after the macroscopic measurements.

Our data show that charge trapping occurs both in the treated and untreated DOTT-based OTFTs. Apparently charge trapping is more important in the inter-grain regions and at grain boundaries than in the crystalline regions. This is consistent with the observations of Tello and co-workers [30] who showed that, while in thick pentacene grains, the potential is independent on the gate bias with minor charge trapping, in the thin IGRs, the potential varies with the gate bias, revealing the formation of an incomplete accumulation layer leading to preferential charge trapping in these thin regions. The potential variation in IGRs with gate voltage has also been observed in our study. [See Appendix]

The preferential location of the trapped charges in the IGRs may be due to their association with electronic defects in the disordered IGRs or at the crystallite edges [30].

Besides the important role of the thin IGRs in DOTT- and DOTT/C₁₀-based OTFTs, the effect of the surface modification should also be considered since it gives rise to less charge trapping densities in the different areas compared to the untreated dielectric surface [Fig. 3.15(c)]. It was reported in different studies that charge trapping at the semiconductor/dielectric interface is a possible reason for the hysteresis behaviour observed in OTFTs [14c, 34].

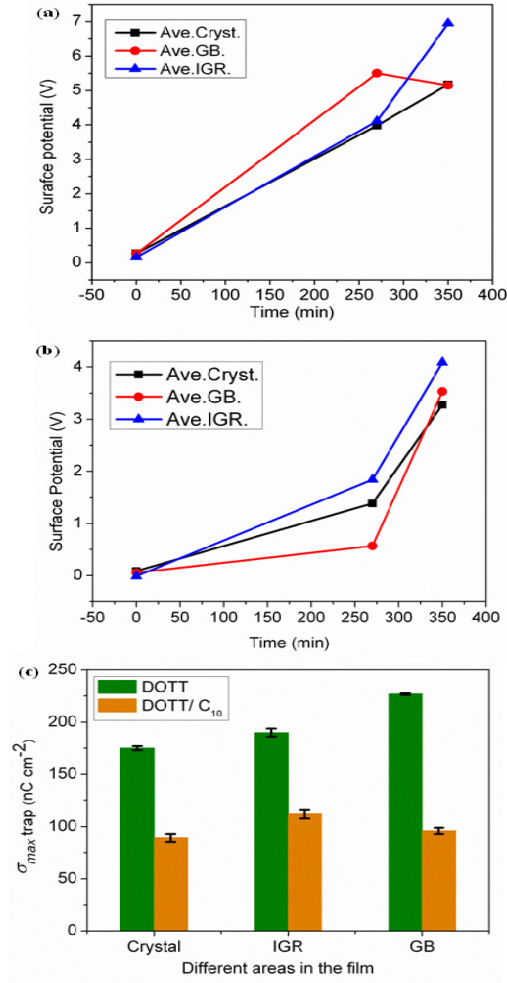


Figure 3.17 Surface potential profiles vs. biasing-time monitored for (a) the untreated and (b) the treated devices; (c) maximum of trapped charge density obtained for 3 different regions in the films of both the treated and untreated devices.

It was also shown that modifying the SiO₂ dielectric with SAMs not only favours the molecular orientation but also eliminates structural disorders which may later act as traps^[35, 36]. The water related trap formation is also reduced due to the hydrophobic character of the surface after the silanation^[37]. Ng and co-workers have shown that the treatment of a SiO₂ dielectric layer with octadecyltrichlorosilane improves the performance of an associated polyfluorene thiophene transistor not by lowering the overall trap density but by lowering instead the trapping- detrapping barrier^[38]. From the kinetic studies of trap formation, contrary to Ng observations, trap capture in our case is slower in the device with C₁₀ interface than in the device with untreated dielectric surface [Fig. 3.17(a) and 3.17(b)].

Another consequence of trapped charges is the hysteresis behaviour observed during the device operation. This hysteresis behaviour for both the treated and untreated devices was characterized as follows: V_d was first decreased stepwise (-4 V, -6 V, -8 V) and then back increased (-6 V and -4 V) at fixed V_g (-10 V). The surface potential distribution was mapped at each voltage. For the untreated device, these analyses reveal hysteresis behaviors across the channel for all the applied voltages [Fig. 3.18(a)]. For the treated device, the hysteresis behavior appeared to be less important [Fig. 3.18(b)]. At the larger value of drain voltage i.e. $V_d = -6$ V, the hysteresis decreased for the untreated device and completely disappeared on the treated device. This may indicate that larger drain voltage values induce an easier removal of the trapped charges.

To conclude, the charge trapping and hysteresis phenomena in our devices may have two main origins: first, trapping sites at the semiconductor/dielectric interface and, second, the defects in the semiconducting film localized in IGRs and at GBs. The density of trapped charges is lower in all regions of the modified device suggesting that the C₁₀ treatment has lowered the trapping sites by increasing both the hydrophobicity of the grid oxide and structural

order of the DOTT molecules (Fig. 3.13). The silanization treatment also reduced the density of IGRs that appear to be the regions in which charge trapping is the most important ^[39].

Figure 3.19(a) shows the contact (source + drain) and channel resistances as a function of gate voltage for the untreated and treated devices. The surface potential profiles were used to obtain the potential drops across individual sections of the channel [Fig. 3.10(d) and 3.11(c)]. The potential drops were divided by the appropriate drain current values (Fig. 3.9) to obtain the resistance at the contacts and across the channel ^[6a]. For the device without dielectric surface modification, contact and channel resistances remain roughly constant with increasing gate voltage. For all applied voltages, the contact resistance remains lower than the channel resistance for both devices.

This proves that the devices are not contact limited which was already suggested by the fact that the potential drops across the contacts were smaller than that across the channel. In the case of the device with C₁₀ modification of the SiO₂ surface, the contact and channel resistances both decrease when increasing the gate voltage i.e. the potential drop reduced with increasing negative gate voltage.

The reduction of the potential drop by increasing the negative gate voltage can be understood from the schematic model shown in Fig. 3.19(b). When the gate voltage increases, the number of accumulated charges (holes in this case) increases in the channel. However, some of these charges are trapped at the defects caused by structural disorder such as grain boundaries.

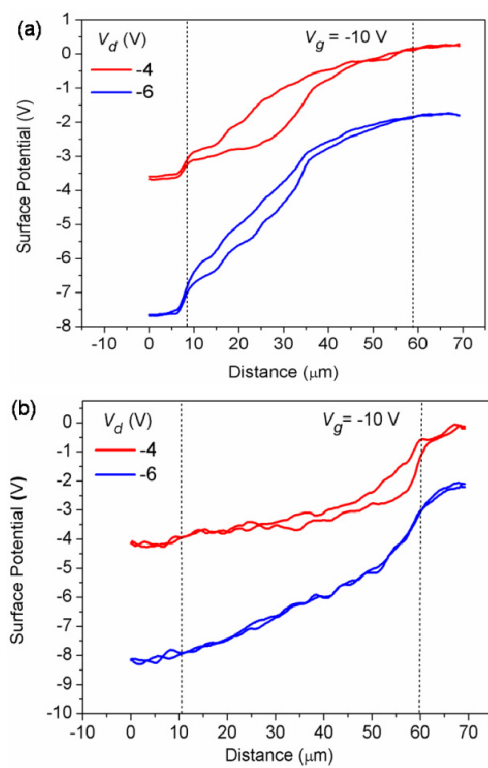


Figure 3.18 Hysteresis curves measured at two drain voltages on the untreated OTFT (a) and a silanized one (b).

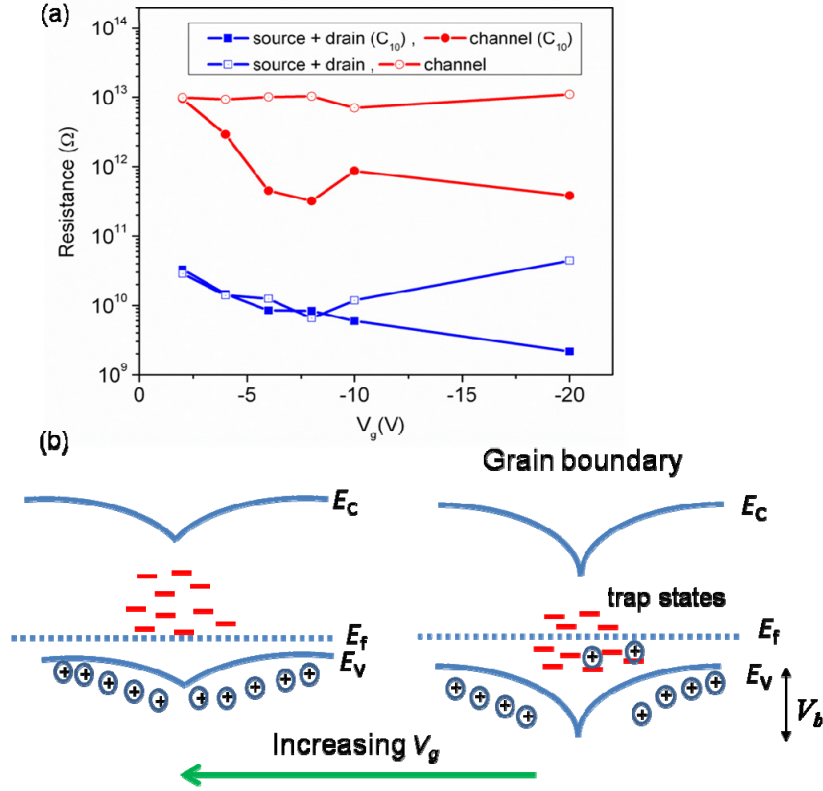


Figure 3.19 (a) Contact (source + drain) and channel resistances as a function of gate voltage for OTFTs with untreated and silanized SiO_2 ; (b) schematic model of change in potential barrier height in grain boundaries and defects with gate voltage (inspired from ^[12]).

Further increasing the gate voltage allows the trapped charges to gradually occupy the grain boundary states and as a result release the pinning of the Fermi level ^[12]. These observations also may suggest that the silane modification of the gate dielectric improved the channel conductivity by decreasing the density of the trapping states. This means that charges may be more deeply trapped in the vicinity of grain boundaries in the device without silanization. This

hypothesis, however, should be proved by activation energy studies and if this option is not available, then by dynamic measurements to obtain a filling-trap state.

In order to be more quantitative and according to the literature^[40] it is also possible to calculate the average grain boundary potential barrier height, V_b , as follow:

$$V_b = \frac{t(qN_{GB})^2}{8\varepsilon C_{ox}(V_G - V_0)}$$

Where t , N_{GB} , ε , C_{ox} , V_G and V_0 are denoted as film thickness, average trap density of the grain boundaries, dielectric constant of the film, oxide capacitance per area, gate voltage and characteristic grain boundary voltage, respectively.²

3.3.2. KPFM study on ddOD4T-based OTFTs

3.3.2.1 Size optimization

Functionalization of oligothiophenes in an endless variety and complexity implies to some advantages such as tuning the physical properties. In fact, from the semiconducting properties point of view, it has been previously shown^[41] that the presence of alkyl chains connected in the α , ω positions helps the π - π interactions between the aromatic cores and thus improves the charge mobility. On that basis, ddOD4T molecule was designed with the purpose of suppressing grain boundaries and having self-healing properties in order to improve the mobility. Although, its branched and asymmetrical alkyl

² More information on parameters (e.g. V_0) can be obtained by fitting the transfer characteristic curves (I_d - V_g) in linear regime to equation^[40]:

$$I_D = \frac{W}{L} C_{ox} \frac{\mu_G}{1 + \frac{L_{GB}}{L_G} \frac{\mu_G}{\mu_{GB}} \exp\left(\frac{qV_b}{KT}\right)} \times \frac{(V_G - V_T)V_D}{1 + \theta(V_G - V_T)}$$

chains provided a good solubility (with respect to the unsubstituted compound) and addressed a liquid crystalline character at RT ^[42], it was not the case from the enhanced π - π interactions and mobility points of view.

Figure 3.20 shows the XRR measurements of spin-coated ddOD4T films on the pristine, (a), and C₁₀ covered, (c), substrates at different temperatures.

According to the results on the pristine substrate [Fig. 3.20(a)], Annealing at high temperature and cooling to RT did not really improve the structure and organization of the film. The small correlation distance observed on the Patterson's function [Fig. 3.20 (b)] for different phases suggest that ddOD4T forms a thin and/or not well organized film on SiO₂.

However, in the case of C₁₀ covered surface, the curves for the Sm G/H and Sm F phases present broad Bragg peaks corresponding to molecular repeat distances of 36.8Å [Fig. 3.20(c)]. In the Patterson functions [Fig. 3.20(d)], we observe oscillations that range up to 30 nm for Sm G/H and Sm F phases. This indicates that the crystal average thickness is 30 nm or above. Therefore, the clearer oscillations in the pseudo- autocorrelation function and the presence of well defined peaks in the XRR spectra for the mentioned phases shows that ddOD4T films spin-coated on a silanized surface with C₁₀ SAMs will have a better organization and are more stable than films deposited on bare SiO₂.

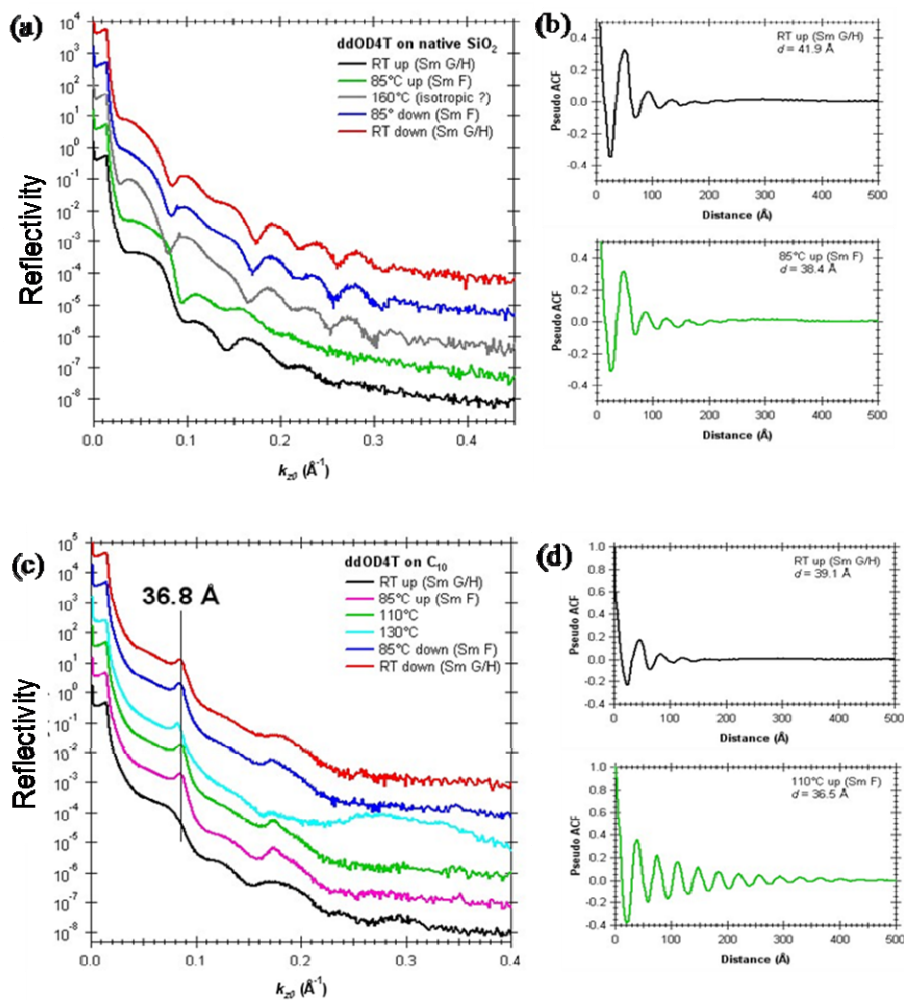


Figure 3.20 XRR analyses of ddOD4T films spin-coated on pristine (a) and C₁₀ modified (c) SiO₂ substrates. (b, d) Corresponding pseudo autocorrelation functions of the electronic density profiles at RT before and after heating. (Courtesy of the POLY group)

Adapting the film processing technique of DOTT films, ddOD4T films were also spin-coated in two steps on both pristine and C₁₀ modified SiO₂ substrates.

In addition, our first KPFM measurements ^[2] revealed that the drop-casting technique can also be convenient in ddOD4T film preparation as it leads to a smooth film formation; contrary to the two other oligothiophene molecules perhaps due to its liquid crystalline character at RT.

On that basis, we performed surface potential measurements on ddOD4T-based OTFTs prepared by both spin-coating and drop-casting methods. The results of the spin-coated films are illustrated hereafter and some examples obtained on drop-casted films are presented in appendix.

3.3.2.2 Surface potential measurement of ddOD4T-based OTFTs prepared by spin-coating

Fig. 3.21 presents topography, typical potential image and potential profiles obtained for ddOD4T on ~50μm wide-channel SiO₂ without surface modification. According to the topography [Fig. 3.21(a)], molecules have covered the channel surface properly while small grains are observed both on the channel and on the gold electrodes. The surface potential profiles have been taken along the line indicated in [Fig. 3.21(a)]. The surface potential profiles at different gate voltages ($-10\text{ V} \leq V_g \leq 0\text{ V}$ increased in 2 V steps) for a fixed drain voltage ($V_d = -6\text{ V}$) are shown in Fig.3.21(c). The vertical dotted-lines mark the geometrical edges of the source and drain located on the right and left, respectively.

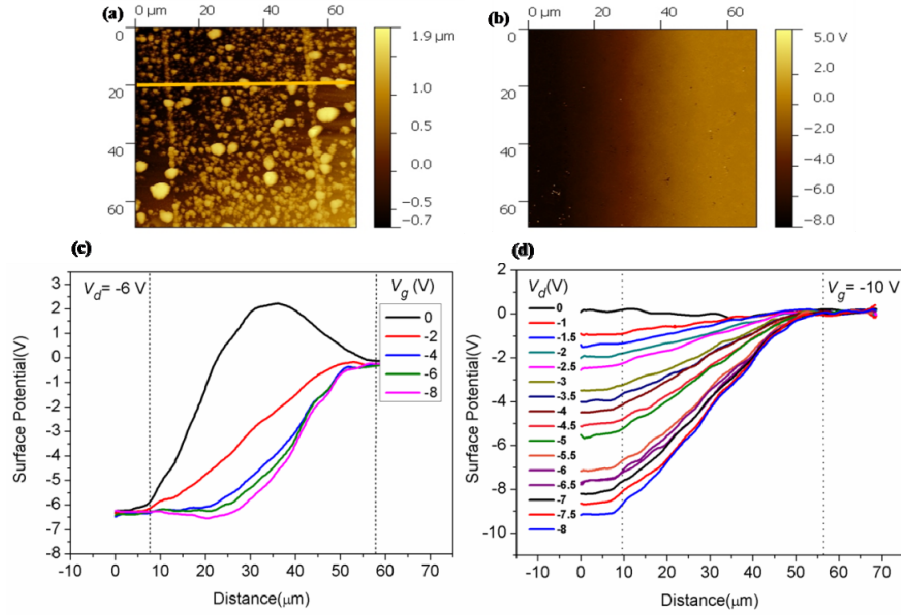


Figure 3.21 Potentiometry of ddOD4T/SiO₂ thin-film transistor ($L=50\mu\text{m}$ channel length). (a) $70\times 70\mu\text{m}^2$ topographic, (b) corresponding surface potential image at $V_d = -6.5\text{ V}$, $V_g = -10\text{ V}$; (c) Potential profiles acquired along horizontal line shown in (a) as a function of gate voltage, where $V_d = -6\text{ V}$. (d) Potential profiles as a function of drain voltage, where $V_g = -10\text{ V}$. The solid vertical lines indicate the edge between the contacts and the conducting channel.

The gate-voltage dependency of the profiles may be clearly observed. A qualitative understanding of different operation regimes of an OTFT can be already obtained from representative electric potential profiles^[43]. When the transistor is turned off, nearly the entire channel region shown between the dotted-lines, lies above the source and drain potentials. In this case, no holes can overcome the barriers and, so, can enter the channel. By decreasing the gate voltage the flat-band situation, i.e., before the injection of any mobile

carriers, can be reached. In this case, the entrance barrier at the source edge vanishes and so the gate voltage will be identical to the threshold voltage V_{th} ^[43].

Concerning the potential profiles in Fig. 3.21(c), it can be inferred that our device is in off-state at $V_g = 0$ V. In the linear regime when a steady-state is reached injected carriers accumulate at the organic layer/dielectric interface, i.e. a channel is formed. This charge accumulation leads to a slope in the potential between the source and drain and thus to an electric field which drives a current through the device^[43]. This linear regime can be seen for $|V_g| \geq |V_d|$ where the potential distribution is almost linear corresponding to an ohmic resistance in the organic channel^[44]. Fig. 3.21(d) shows the surface potential profiles at different drain voltages ($-8 \text{ V} \leq V_d \leq 0 \text{ V}$) for a fixed gate voltage ($V_g = -10 \text{ V}$) in the linear regime. A linear decrease of the measured potential is observed. This indicates that transport properties of spin-coated ddOD4T films are homogeneous on length scales larger than the resolution of our KPFM experiments. A typical surface potential image taken at $V_d = -6.5 \text{ V}$ and $V_g = -10 \text{ V}$ with respect to the source electrode, is shown in Fig. 3.21(b). It can be clearly seen how the potential distribution is uniform across the channel and how it slightly decreases from the right to the left; i.e., from the source to the drain contacts.

Figure 3.22 shows topography, typical potential image and potential profiles obtained for ddOD4T on $\sim 50 \mu\text{m}$ wide-channel SiO_2 with surface modification. i.e., the surface of SiO_2 has been covered with a self-assembled monolayer of C_{10} alkylsilane. Regarding the topography [Fig. 3.22(a)] and line profile measurements (not shown), molecules have covered the channel surface properly, while the quality and the uniformity of the film has been improved compared to the film without modification in Fig. 3.21(a). The surface potential profiles at different gate voltages ($-10 \text{ V} \leq V_g \leq 0 \text{ V}$ increased in 2 V steps) for a fixed drain voltage ($V_d = -6 \text{ V}$) are shown in Fig. 3.22(c).

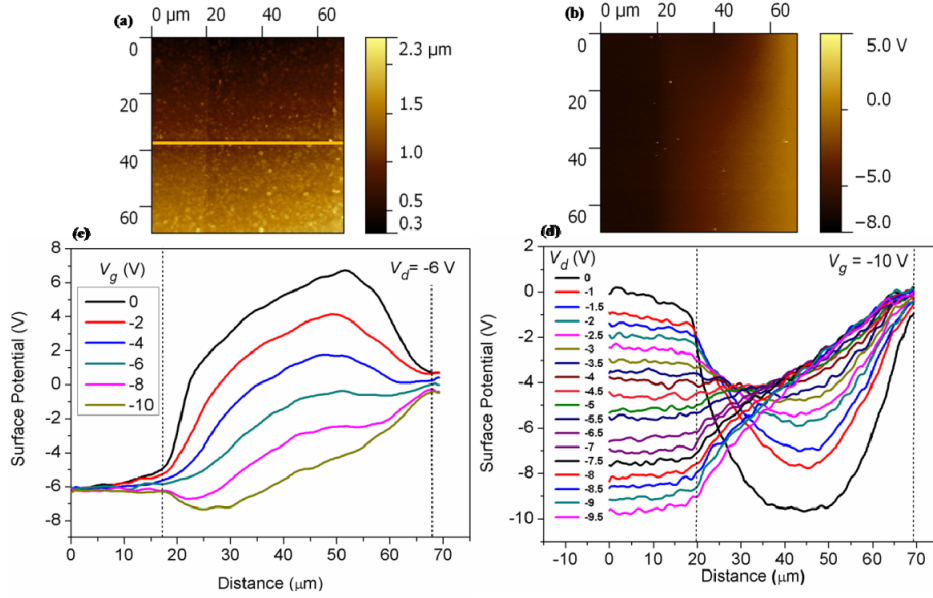


Figure 3.22 Potentiometry of ddOD4T/C₁₀/SiO₂ thin-film transistor ($L = 50 \mu\text{m}$ channel length). (a) $70 \times 70 \mu\text{m}^2$ topographic, (b) corresponding surface potential image at $V_d = -6 \text{ V}$, $V_g = -10 \text{ V}$; (c) Potential profiles acquired along horizontal line shown in (a) as a function of gate voltage, where $V_d = -6 \text{ V}$. (d) Potential profiles as a function of drain voltage, where $V_g = -10 \text{ V}$. The solid vertical lines indicate the edge between the contacts and the conducting channel.

The vertical dotted-lines mark the geometrical edges of the source and drain located at right and left, respectively. The gate voltage dependency of the profiles is presented as well as the profiles in Fig. 3.21(c). It seems that the changes in surface potential with the applied V_g is more regular than the previous case perhaps due to the effect of substrate modifications. In this respect, one can follow the device operation modes which varies from off-state at $V_g = 0 \text{ V}$ to an on-state at $V_g > -4 \text{ V}$. This can be deduced from the almost high

injecting/extracting barriers, at source/channel and drain/channel interfaces respectively, when $V_g = 0-4$ V and the vanishing of these barriers when V_g decreases to -6 V in this device. Further decreasing the gate voltage (i.e., when $|V_g| \geq |V_d|$) leads the device to enter the linear regime. In this regime, holes are initially able to enter the channel from both the source and drain sides. Therefore, both electrodes act as injecting contacts for a short period of time, i.e., until a non-vanishing source-drain electric field has been established^[43]. When a steady-state is reached injected carriers accumulate at the organic layer/dielectric interface and thus a channel is formed. This charge accumulation leads to a slope of the potential between the source and drain and thus to an electric field which drives a current through the device. This situation can be clearly seen in Fig. 3.22(d) where the device operates in linear regime and there is a distinct transition between the unsteady-state to the steady-state in this regime. In particular, for $|V_d| \leq 4$ V, we are in unsteady-state. At $V_d = 0$ the potential in the channel matches the one applied at the gate contact i.e. 10 V (black curve) which suggests that the injected carriers have not yet been accumulated at the semiconductor/dielectric interface to be able to shield the gate voltage. By decreasing the drain voltage i.e., for $|V_d| \geq 4$ V a steady-state is reached and charges accumulate in the channel which results in forming a slope of the potential between the source and drain. An image of the surface potential taken at $V_d = -6$ V and $V_g = -10$ V with respect to the source electrode, is shown in Fig. 3.22(b). The surface potential distribution is uniform across the channel and slightly decreases from source to drain electrode.

As for the DOTT-based OTFTs in the previous section, we also studied charge trapping effects for these devices. As it can be seen in Fig. 3.23 for the untreated OTFT, a positive electrostatic potential is observed in the channel after biasing the device in the on-state for an extended period of time and then switching it off, except after the first polarisation ramp that was realized with $V_g = 0$ V. For the two other polarization ramps realized with a negative bias of the gate,

large surface potential values were measured in the channel, attributed to the presence of trapped charges. The accumulation of these charges is illustrated by the KPFM images in Figure 3.23(c) & (d) and the corresponding profiles (red & blue curves).

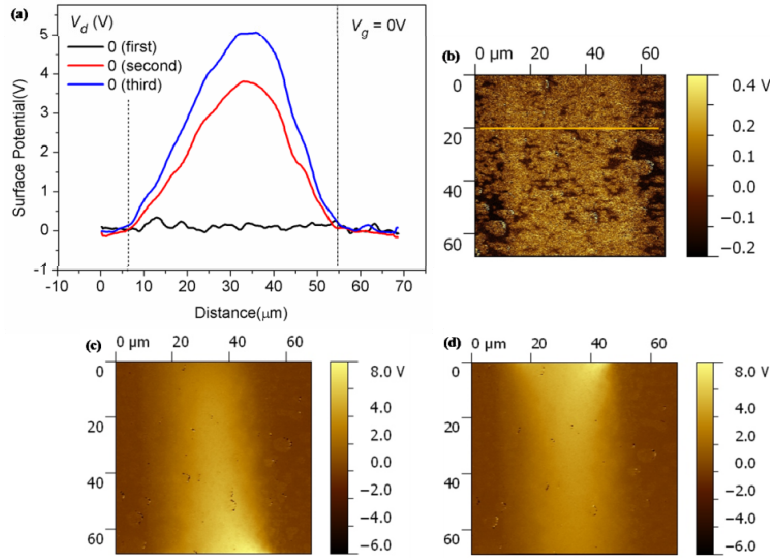


Figure 3.23 (a) Surface potential profiles (along line shown in (b)); (b-d) KPFM images obtained on an untreated OTFT after polarization and switching-off the device. (b) and black): initial off-state; (c) and red): after ramping V_d down to -8 V (0.5 V steps) with $V_g = -10$ V; (d) and blue): after ramping V_g down to -10 V (2 V steps) with $V_d = -6$ V.

Figure 3.24 presents the KPFM images and the surface potential profiles obtained on a silanized OTFT after biasing ramps in the on-state and the switching-off in the off-state. As it was the case for the untreated OTFT, a positive surface potential is measured in the channel after polarization of the device with a negative bias voltage applied to the grid, suggesting again the presence of trapped charges.

Comparing Fig. 3.23(a) and 3.24(a) indicates that charge trapping occurs along the whole channel for both devices. Moreover, in the case of the untreated device, charge trap density varies smoothly along the channel indicating a more or less homogeneous trap state density; while in the treated device charge trap density is inhomogeneous suggesting that in this case defect states especially near the source contact play a major role in charge trapping. This observation may also be explained by the probability of formation of an inhomogeneous or incomplete silane monolayer on the substrate surface during silanization process. Surprisingly, when we compare potential profiles obtained in the same conditions on the silanized and the untreated devices (Fig. 3.23 (c & blue curve) and Fig. 3.24 (c & blue curve), respectively), one clearly see that the surface potential, i.e. the amount of trapped charges is higher on the silanized device. An explanation which may account for this observation is that the morphology of the ddOD4T film itself, which is different from that of the crystalline DOTT or DH4T films, can cause higher trapping on the treated surface. These could be also the reasons of why a delay in charge accumulation and a clear transition between unsteady and steady states is observed for this system. [Fig. 3.22 (d)]

According to the topography images [Fig. 3. 21 (a) and 3. 22 (a)] , silanization has decreased the size of the grains³ of ddOD4T film, but instead increased the number of the grains which may result in more charge trapping. It should be mentioned that, within the numbers of the tested devices, based on spin-coated ddOD4T films, over half of the OTFTs showed higher amount of trapped charges for treated surfaces compared to the untreated ones.

³ The term "grain" for this compound not to be inferred as in the concept of "grain" in DH4T and DOTT, since this molecule is in smectic phase at RT.

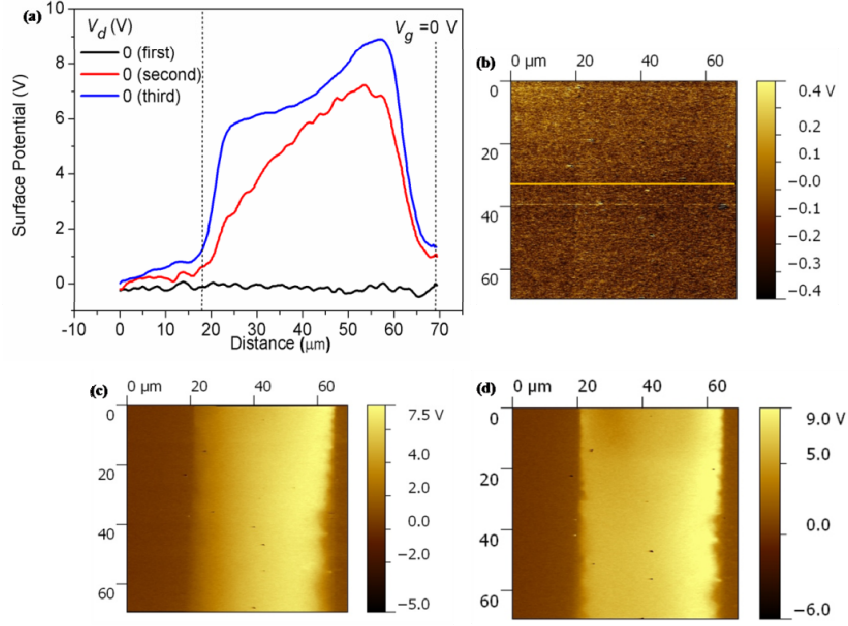


Figure 3.24 (a) Surface potential profiles (along line shown in (b); (b-d) KPFM images obtained on a silanized OTFT after polarization and switching- off the device. (b) and black): initial off-state; (c) and red): after ramping V_d down to -9.5 V (0.5 V steps) with $V_g = -10$ V; (d) and blue): after ramping V_g down to -10 V (2 V steps) with $V_d = -6$ V.

We also monitored the surface potential as a function of biasing time to study the dynamics of trapping and calculate the density of trapped charges for both treated and untreated devices. The surface potential profiles as a function of bias-stressing time have been collected in 2 different regions of the channel including: grains and inter grains. The reason of this classification was the fact that the film morphology in ddOD4T based TFTs, as can be seen in topography images, is different than that of DOTT- and DH4T- devices which more tend to form crystalline structure.

Figures 3.25(a) and 3.25(b) show the surface potential profiles obtained in these regions for the untreated and treated devices, respectively. Each point in the diagrams is an average of three surface potential values obtained along three different lines at the top, centre and bottom of the KFM images in Fig. 3.23(b) and 3.24(b).

Figure 3.25(c) provides a visual comparison of the maximum of σ_{trap} in the grains and intergrain regions for both the treated and untreated devices. The larger values of σ_{trap} are obtained for the device with gate surface modification. On the other hand, the major part of the trapped charges belongs to the grains for both devices. The maximum of σ_{trap} in grains is calculated to be 97 nC.cm^{-2} and 200 nC.cm^{-2} for the untreated and treated devices, respectively.

Figure 3.26 shows the hysteresis measurements for the treated and untreated devices. For both devices, these analyses reveal hysteresis behaviors across the channel for all the applied voltages. However, For the treated device, the hysteresis behavior appeared to be less important at $V_d = -6\text{V}$.

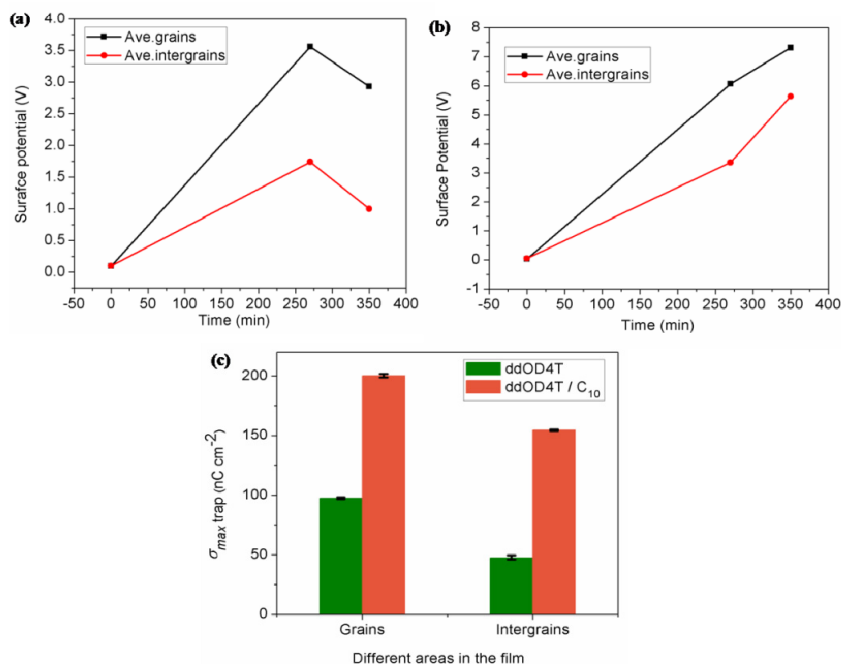


Figure 3.25 Surface potential profiles vs. biasing-time monitored for (a) the untreated and (b) the treated devices; (c) maximum of trapped charge density obtained for 3 different regions in the films of both the treated and untreated devices.

Although, the microscopic study of spin-coated ddOD4T-based TFTs showed some contradictory behaviors, such as higher charge trapping effects for silanized devices, the macroscopic measurements on drop-casted TFTs revealed the common expected behaviors that is, improved electrical properties via SAM-modified gate dielectric surfaces. As it appears in Fig.3.27, the output current of the modified device increased by about one order of magnitude compared to the pristine device. Moreover, both devices present good saturation and field-effect dependence.

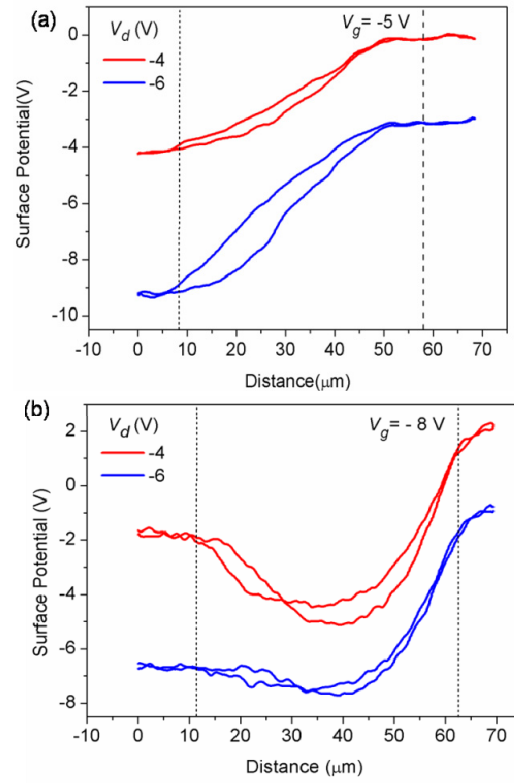


Figure 3.26 Hysteresis curves measured at two drain voltages on the untreated OTFT (a) and a silanized one (b).

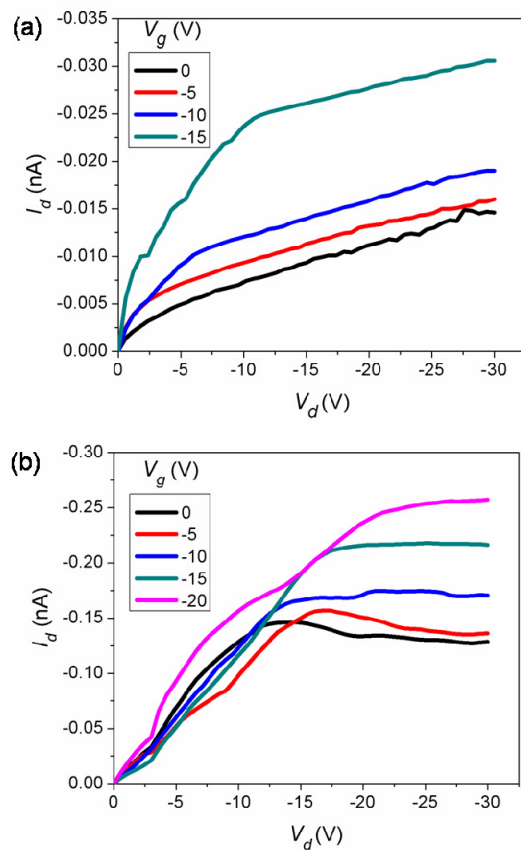


Figure 3.27 Current-voltage characteristics of drop-cast ddOD4T-based OTFTs, with 126-nm-thick SiO_2 dielectrics: Pristine (a) and coated with C_{10} (b). Both devices had Au contacts, with $W=1\text{ mm}$ and $L=50\text{ }\mu\text{m}$.

3.3.3 KPFM study on DH4T-based OTFTs

3.3.3.1 Size optimization

DH4T has been widely studied as active layer in organic transistors because of its good carrier mobility and high crystallinity^[45,45b]. In order to be compatible with large-scale applications, researches have directed their efforts towards solution-processing methods in OTFT fabrication. Initially, similar to the DOTT and ddOD4T molecules in previous sections, we investigated the film formation behavior in order to obtain appropriate conditions for KPFM measurements. Spin-coating and drop-casting were used. It has been shown either in our experiments or elsewhere that these two techniques result in different film morphologies for DH4T. DH4T films deposited by spin-coating have island morphology (Fig.3.28 (b)). In contrast, drop-casting results in very large crystals (Fig.3. 28 (a)), most probably due to a lower evaporation rate of the solvent which in turn allows for a better molecular arrangement of the material. However, a comparative XRR analysis of DH4T layers (Fig. 3.28 (c)) deposited by drop-casting (blue curve) and spin-coating (red curve) on 100-nm-thick SiO₂ suggest that there are no fundamental differences in the molecular organization of the DH4T films deposited by these techniques. In both reflectograms the Bragg peaks correspond to a specific vertical repeat distance which is equal to 28.5 Å and 29 Å for the spin-coated and drop-casted films, respectively. It is marked that the smaller intensity of the peak related to the drop-casted film is explained by the lower solution concentration (0.0075 wt %) compared to the one used for spin-coating (0.4 wt %).

As mentioned in previous sections, spin-coated crystals which are formed on top of a very thin, continuous layer are proper choice for performing microscopic measurements like KPFM; although the presence of the cracks and pores together with the smaller grain size can be the reason behind the modest macroscopic electrical performance of spin-coated DH4T films^[23].

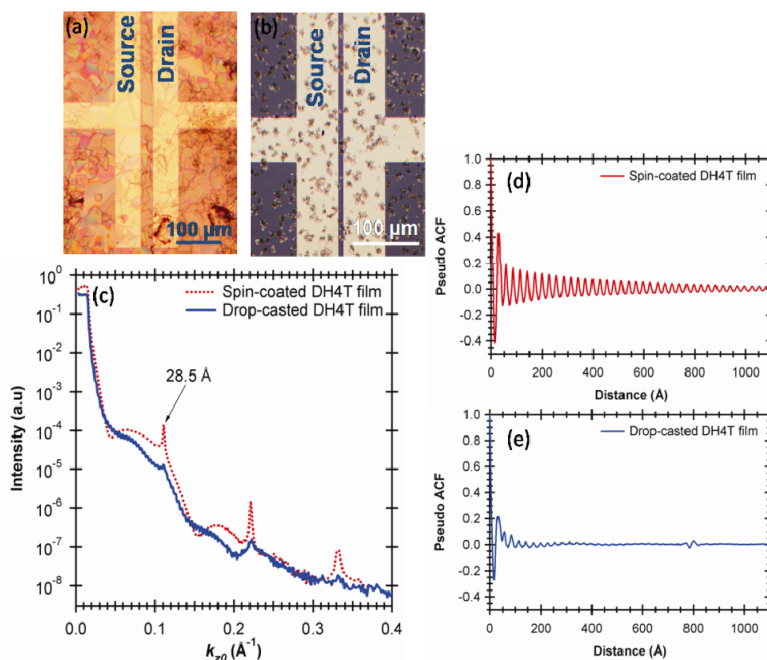


Figure 3.28 Micrographs of DH4T TFTs fabricated with T-type Pd electrodes (a,b). The film has been deposited by drop-casting (left) and spin-coating (right); XRR (c) and corresponding Patterson functions for spin-coated at 1000 rpm (d) and drop-cast (e) films of DH4T deposited on 100 nm SiO₂ pristine layers. The organic semiconductor was 80-nm-thick on both samples. (from Dana Vlad ^[23])

DH4T films were also spin-coated in one and two steps on both preheated pristine and C₁₀ modified SiO₂ substrates. As can be seen in Fig. 3.29, it is appeared that there is no significant difference between the spin-coated films in one or two steps. Hence, we fabricated our DH4T films via the one step spin-coating procedure.

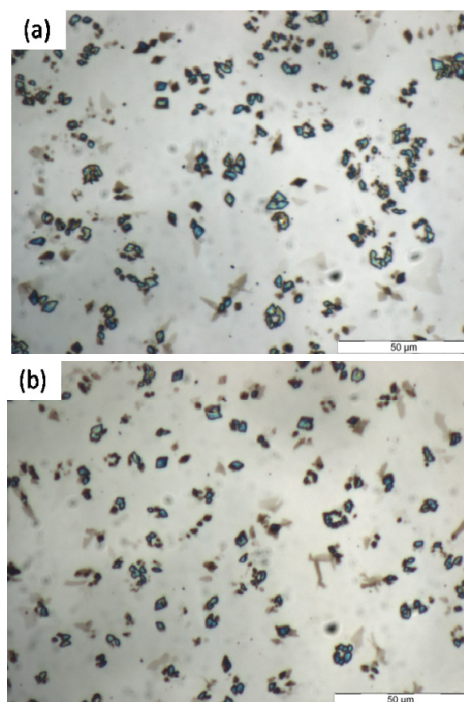


Figure 3.29 50 μm scale optical microscope images of the DH4T films from 0.4% solution concentrations deposited at different spin-coating parameters on native SiO_2 substrates at $T \sim 150^\circ\text{C}$; (a) $V_1 = 5000 \text{ rpm}$, $t_1 = 60\text{s}$, $V_2 = 5500 \text{ rpm}$, $t_2 = 60\text{s}$; (b) $V = 5000 \text{ rpm}$, $t = 60\text{s}$. The substrates were heated up to corresponding smectic phase of DH4T molecules.

3.3.3.2 Surface potential measurement of DH4T-based OTFTs prepared by spin-coating

Figure 3.30 presents AFM and KPFM results of a OTFT based on DH4T spin-coated on pristine SiO_2 (20 μm channel width). According to the topography and phase images [Fig. 3.30(a) and (b)], molecules covered the channel surface properly with a uniform and smooth film, while flat and thin crystals are observed both on the channel and on the gold electrodes. The surface potential profile measurements

have been done along the line indicated in [Fig. 3.30 (c)]. A typical surface potential image taken at $V_d = -5$ V and $V_g = -8$ V with respect to the source electrode, is shown in Fig. 3.30(c). It can be clearly seen how the potential distribution is uniform across the channel and how it slightly decreases from the right to the left; i.e., from the source to the drain contact.

The surface potential profiles at different gate voltages ($-15 \text{ V} \leq V_g \leq 0 \text{ V}$) for a fixed drain voltage ($V_d = -5 \text{ V}$) are shown in Fig.3.30 (d). The vertical dotted-lines mark the geometrical edges of the source and drain located on the right and left, respectively. The gate-voltage dependency of the profiles may be clearly observed. Regarding the qualitative understanding of the operational regimes of the OTFTs, this device is probably in on-state even at $V_g = 0 \text{ V}$ such that there is no injection barrier at the source-edge at this voltage. In addition, decreasing V_g , potential drops which first appeared at the drain-edge decreased and instead, drops increased at the source contact possibly indicating the improvement of charge injection and collection at the source and drain electrodes, respectively.

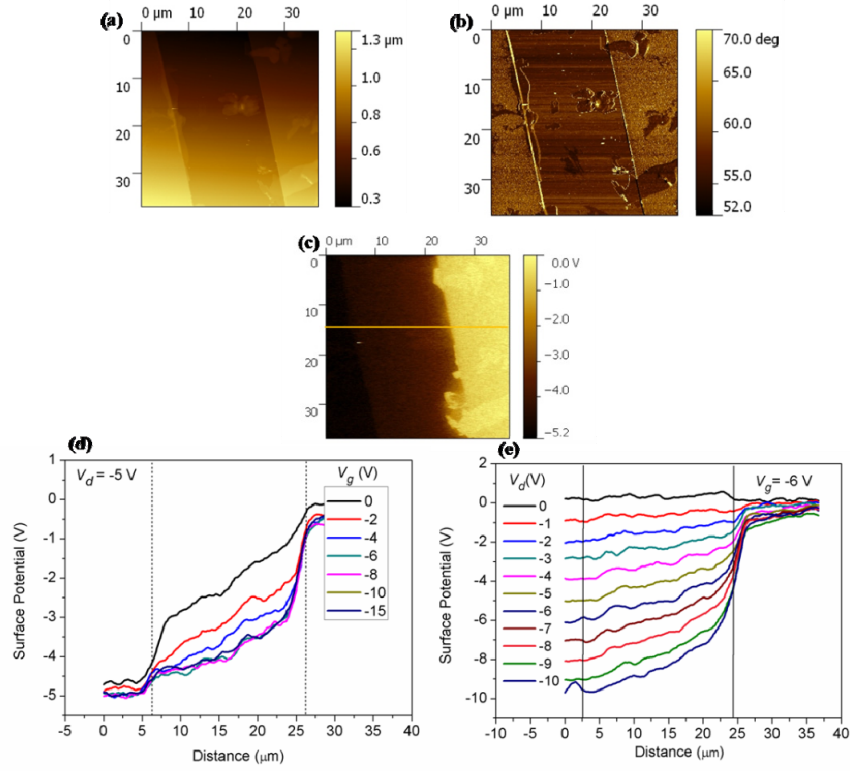


Figure 3.30 Potentiometry of DH4T/SiO₂ thin-film transistor ($L=20\text{ }\mu\text{m}$ channel length). (a) $40\times40\text{ }\mu\text{m}^2$ topographic; (b) corresponding phase image; (c) corresponding surface potential image at $V_d = -5\text{ V}$, $V_g = -8\text{ V}$; (d) Potential profiles acquired along horizontal line shown in (c) as a function of gate voltage, where $V_d = -5\text{ V}$. (e) Potential profiles as a function of drain voltage, where $V_g = -6\text{ V}$. The solid vertical lines indicate the edge between the contacts and the conducting channel.

A linear decrease of the surface potential from the source to the drain is also observable without any sharp drops inside the channel. Figure 3.30 (e) shows the surface potential profiles at different drain voltages ($-10 \text{ V} \leq V_d \leq 0 \text{ V}$) for a fixed gate voltage ($V_g = -6 \text{ V}$) in the linear regime. The surface potential varies uniformly over the entire channel and a linear decrease of the measured potential is observed. This indicates that transport properties of spin-coated DH4T films are homogeneous on length scales larger than the resolution of our KPFM experiments.

Figure 3.31 shows topography, typical potential image and potential profiles obtained for DH4T on $20\mu\text{m}$ wide-channel SiO₂ with surface modification. i.e., the surface of SiO₂ has been covered with a self-assembled monolayer of C₁₀ alkylsilane. Regarding the topography [Fig. 3.31(a)], a smooth layer has covered the channel surface completely without any further individual crystals with respect to the DH4T on pristine SiO₂, although some cracks also appeared on the surface of the film. The surface potential profiles at different gate voltages ($-15 \text{ V} \leq V_g \leq 0 \text{ V}$) for a fixed drain voltage ($V_d = -5 \text{ V}$) are shown in Fig. 3.31(c).

The gate voltage dependency of the profiles is presented in Fig. 3.31(c). Similar to the previous case, it seems that this device is also in on-state at $V_g = 0 \text{ V}$ due to the absence of the injection barriers at source-edge contact at this voltage. Further, the surface potential decreased by decreasing the gate voltage which disclosed the gate voltage dependency of profiles. An image of the surface potential taken at $V_d = -5 \text{ V}$ and $V_g = -8 \text{ V}$ with respect to the source electrode, is shown in Fig. 3.31 (b). The surface potential distribution is uniform across the channel and slightly decreases from the source to the drain electrode.

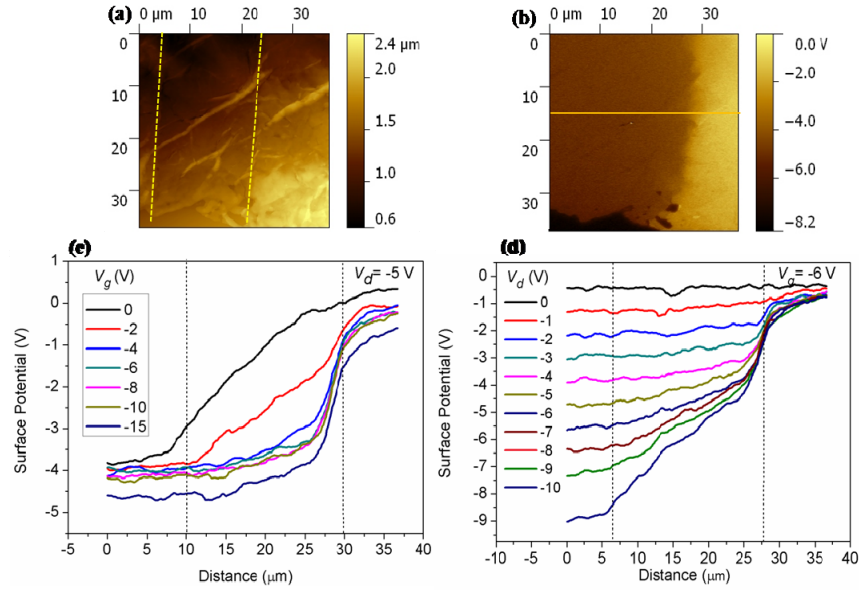


Figure 3.31 Potentiometry of DH4T/C₁₀/SiO₂ thin-film transistor ($L = 20\text{ }\mu\text{m}$ channel length). (a) $40 \times 40\text{ }\mu\text{m}^2$ topographic, (b) corresponding surface potential image at $V_d = -5\text{ V}$, $V_g = -8\text{ V}$; (c) Potential profiles acquired along horizontal line shown in (b) as a function of gate voltage, where $V_d = -5\text{ V}$. (d) Potential profiles as a function of drain voltage, where $V_g = -6\text{ V}$. The solid vertical lines indicate the edge between the contacts and the conducting channel.

Charge trapping measurements for both untreated and treated DH4T-based OTFTs revealed that the charge trapping in this molecule is less present compared to the DOTT- and ddOD4T- based OTFTs discussed in previous sections. This is evident from the surface potential values in Fig.3.32 (a) and 3.33 (a). For the case of DH4T on pristine SiO₂, there are already some trapped charges on the surface of individual crystals dispersed on top of the thin layer of DH4T film, when the device is in off state. This charge localization clearly appeared on the black profile in Fig.3. 32 (a) and Fig.3.32 (b), where the individual DH4T crystals show brighter colour corresponding to the higher surface potential and thus higher amount of accumulated charges.

However, for DH4T on silanized SiO₂, even though charge trapping in the initial off-state is observed [Fig. 3. 33 (b) and black profile in Fig. 3. 33 (a)], it appears to be more uniform and less important compared to that of DH4T on pristine SiO₂. For the two other polarization ramps realized with a negative bias of the gate, non-zero surface potential values were measured in the channel, revealing the presence of trapped charges for both untreated and treated devices. [See Fig. 3.32 (b),(c) and Fig. 3.33 (b), (c) with the corresponding red and blue profiles in Fig.3.32 (a) and 3.33 (a), respectively].

For the device with silane modification except for some points in the channel, the surface potential variations related to the trapped charges is low and not very significant.

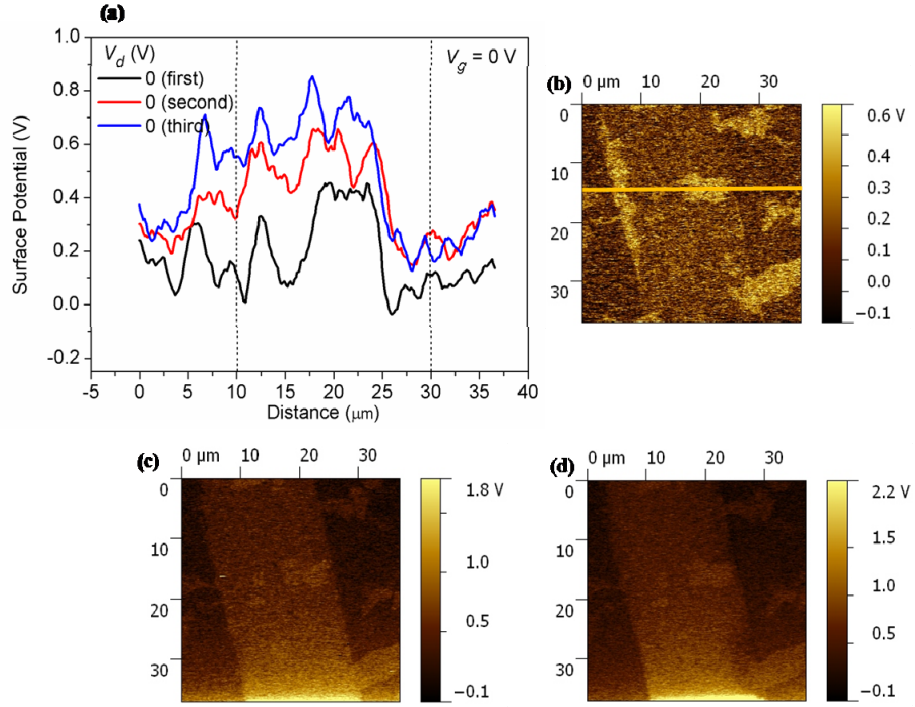


Figure 3.32 (a) Surface potential profiles (along line shown in (b); (b-d) KPFM images obtained on an untreated OTFT after polarization and switching-off the device. (b) and black): initial off-state; (c) and red): after ramping V_d down to -10 V with $V_g = -6$ V; (d) and blue): after ramping V_g down to -15 V with $V_d = -5$ V.

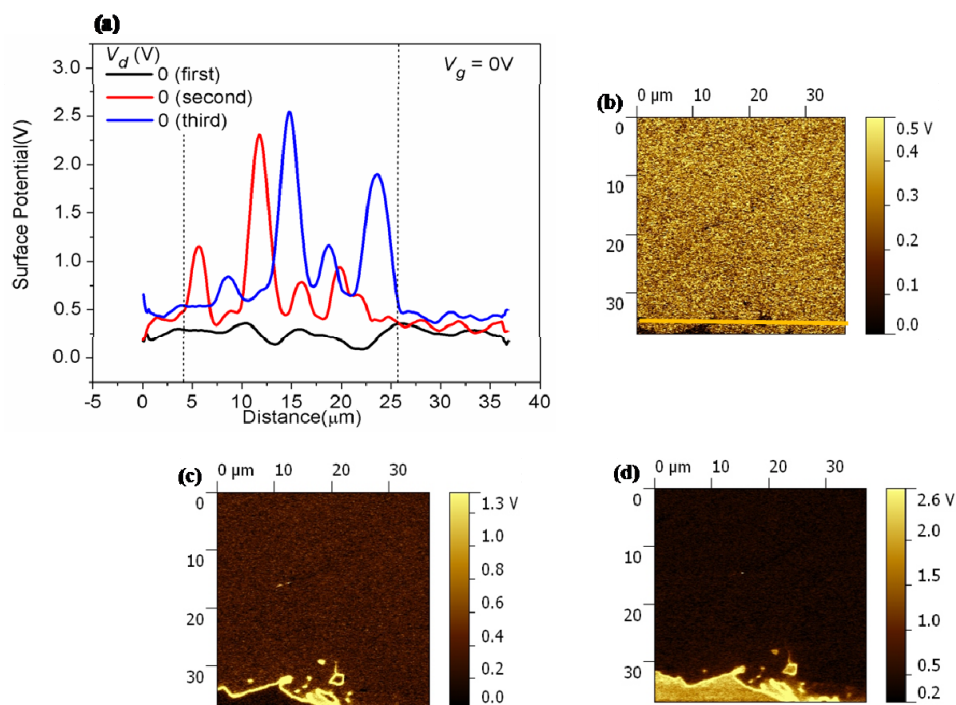


Figure 3.33 (a) Surface potential profiles (along line shown in (b)); (b-d) KPFM images obtained on an untreated OTFT after polarization and switching-off the device. (b) and black): initial off-state; (c) and red): after ramping V_d down to -10 V with $V_g = -6$ V; (d) and blue): after ramping V_g down to -15 V with $V_d = -5$ V.

Figure 3.34 (a) presents the surface potential profiles as a function of bias-stressing time on the DH4T layer in the channel in both untreated and treated devices. Since the film morphology of DH4T-based OTFTs was mostly of a smooth and uniform thin layer, the profiles were collected for the entire film. Grain boundaries and inter grain regions appearing in the DOTT-based TFTs or small grains of ddOD4T-based TFTs, are not clearly observed in the case of DH4T- based devices. Each point in the diagram is an average of

three surface potential values obtained along three different lines at the top, centre and bottom of the KFM images in Fig. 3.32(b) and 3.33(b). As it can be seen in Fig. 3.34 (a), charge trapping increased with time for both pristine and silane modified DH4T TFTs.

Figure 3.34 (b) provides a visual comparison of the maximum of σ_{trap} for both the treated and untreated devices. Both pristine and silanized devices exhibit more or less the same value of maximum of σ_{trap} : 23 nC.cm⁻² on pristine SiO₂ and 25 nC.cm⁻² on C₁₀- modified gate.

Figure 3.35 shows the hysteresis measurements for the treated and untreated devices. For both devices, these analyses reveal less hysteresis behaviors across the channel for all the applied voltages compared to the DOTT- and ddOD4T-based OTFTs.

Figure 3.36 shows an example of the macroscopic measurements on drop-casted TFTs based on DH4T molecules. Although, the output current enhancement in silanized device is not very significant in comparison with the pristine one, it shows nice field-effect behavior i.e. a clear linear and saturation regimes. The device without SAM-modification does not show saturation behavior perhaps due to some impurities or water adsorption on the surface of the conductive layer. It should also be noticed that according to our experiments the best macroscopic characteristics were obtained for DH4T-based OTFTs compared to the DOTT- and ddOD4T-based devices.

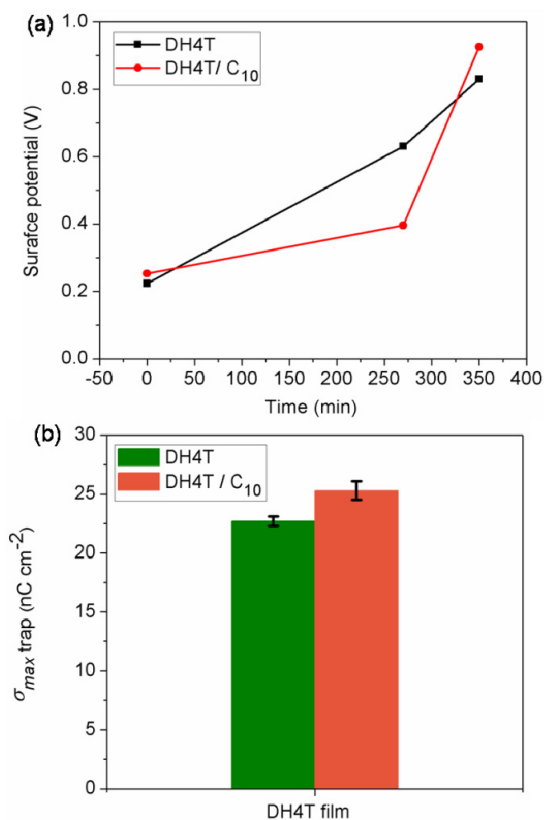


Figure 3.34 (a) Surface potential profiles vs. biasing-time monitored for the untreated and the treated DH4T-based devices; (b) maximum of trapped charge density obtained for the films of both the treated and untreated devices.

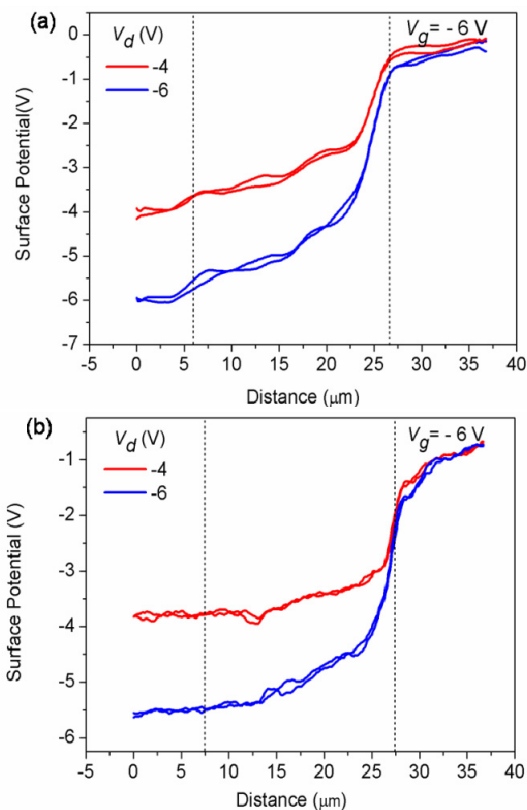


Figure 3.35 Hysteresis curves measured at two drain voltages on the untreated OTFT (a) and a silanized one (b).

This finding is consistent with the previous measurements performed in more details on these molecules which came to the conclusion that DH4T molecules exhibit better conductive properties as active layer in OTFTs^[23].

The other remark is that, the main goal of the work done in this chapter was to microscopically investigate the electrical properties of these three oligothiophene molecules and trying to find out

correlations between the morphology and electrical properties in microscopic scale. However, our efforts in performing macroscopic measurements also ended to acceptable results.

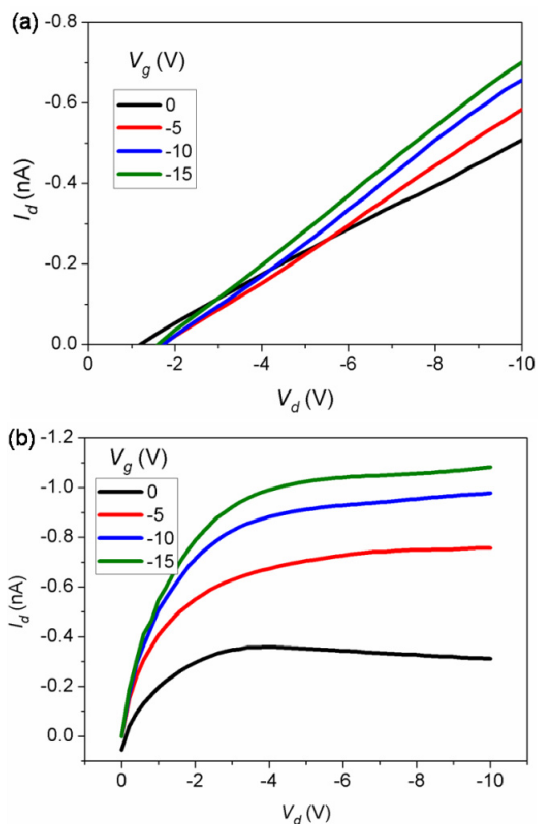


Figure 3.36 Current-voltage characteristics of drop-cast DH4T-based OTFTs, with 126-nm-thick SiO₂ dielectrics: Pristine (a) and coated with C₁₀ (b). Both devices had Au contacts, with $W = 0.1$ mm and $L = 20$ μ m.

3.4. Conclusion

In this chapter, KPFM was used to characterize simultaneously the film morphology and the electrical potential distribution on active OTFTs based on DOTT, DH4T and ddOD4T oligothiophene molecules with a native SiO_x grid or with a silanized oxide grid. Efforts were done to optimize the film morphology and structure of the active layers by modifying the film preparation process. Smaller and more densely packed crystals in addition to the more uniform films were observed on the silanized devices.

It has been shown that regarding the surface potential profiles, clear V_g and V_d dependency of the surface potential profiles were measured, in all cases. For DOTT- based OTFT on C₁₀- modified SiO₂, no sharp potential drop was observed in the channel compared to the pristine device. For ddOD4T-based OTFT on modified gate dielectric, a distinct transition between the unsteady state to steady state was observed for V_d - dependent profiles. For DH4T-based OTFTs on both pristine and C₁₀- modified SiO₂, surface potential varied smooth and uniformly over the channel and no sharp potential drop was observed.

Regarding the contact resistances, for DOTT-based OTFT on SiO₂ contact and channel resistances remained roughly constant with increasing gate voltage, while resistances both decreased when increasing the gate voltage on modified SiO₂. Moreover, the devices were not contact limited. For ddOD4T-based OTFTs, both pristine and C₁₀- modified devices were not contact limited and the potential drop decreased in the channel by increasing the gate voltage. For DH4T-based OTFTs, potential drops at the source and drain contacts were observed on both pristine and modified devices. The potential drop at the drain contact in modified device was less than drops in the pristine device.

Regarding the charge-trapping, for all systems, charge trap distribution was more homogeneous on pristine SiO₂ compared to the

C₁₀- modified SiO₂.

For DOTT-based OTFTs, charge trapping was lower on the silanized device, though charge trap distribution was inhomogeneous in the channel. Hysteresis effects appeared to be less important in the treated devices compared to the untreated ones. The origins of bias-stress effect in these devices is possibly due to the trapping sites existing both at the semiconductor-dielectric interface and close to defects in the semiconducting film mainly localized in inter-grain regions and at grain boundaries. Since the density of trapped charges was lower in all regions of the modified devices compared to the unmodified one, it can be concluded that the C₁₀ treatment improved these devices bias stress effect by lowering the trapping site density in all the regions. Better performance with C₁₀ may be due to absence of wetting layer and/or surface induced phases.

For ddOD4T-based OTFTs, charge trapping occurred for both treated and untreated devices along the whole channel. The amount of trapped charges was higher on the silanized device perhaps due to the morphology of the film. However, the less amount of the maximum of charge trapping density was measured in both pristine and silanized devices, compared to the two other molecules.

For DH4T- based OTFTs, the charge trapping appeared to be more uniform and less important on C₁₀- modified SiO₂ compared to that of DH4T on pristine SiO₂ in the initial off-state. However, for the two other polarization ramps, non-zero surface potential values were measured in the channel. Hysteresis measurements for the treated and un-treated devices revealed less hysteresis behaviors across the channel on treated device.

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** Chapter 4 **

Organic thin-film transistors on polymer gate dielectrics

Abstract

The purpose of this part is to investigate some fabrication aspects that are expected to improve the performance of DH4T-based OTFTs using polymer gate dielectrics with and without nanoparticles embedded inside. Poly (vinyl alcohol) (PVA) was used as gate insulator and was deposited by spin-coating. The PVA layers with and without SiO₂ nanoparticles were first extensively characterized. The surface properties of the nanocomposite gate dielectrics were studied by means of contact-angle and roughness measurements. The dielectric properties were characterized via capacitance and leakage-current measurements within metal-insulator-metal (MIM) structures. Then, the performances of the OTFTs were investigated by electrical measurements and KPFM microscopy.

All devices showed ambipolar behavior in the low-voltage range. However, the characteristics of the devices with PVA/SiO₂ (5 wt %) seemed to be improved compared to those with neat PVA and with PVA/SiO₂ (30 wt %). This may be due to the formation of a film with a larger capacitance and a less hydrophilic surface.

4.1. Introduction

Polymer dielectrics have recently been employed as gate insulators in OTFTs due to their simple processing via spin-coating or –casting, and easy tuning of the surface chemical properties ^[1]. It was shown that they can lead to better performances in, for e.g., pentacene-based OTFTs compared to those fabricated with SiO₂ insulators, ^[2,3] and in some cases, to ambipolar characteristics.^[4,5] Nunes et al ^[2] reported improved performance for pentacene- based OTFT on various styrene polymer dielectrics. In another study by Choongik Kim and co-workers ^[6] pentacene films were grown on bare and polymer-coated SiO₂ gate dielectrics to form field effect transistors and characterized by using AFM, X-ray diffraction (XRD) besides the electric characteristics measurements. Various polymers such as poly (vinylalcohol) (PVA), polystyrene (PS), poly (4-vinylphenol) (PVP),... were employed. It was demonstrated that the dielectric layer micro-structural properties affect the pentacene film growth mode and phase selection. It was also found that the polymer dielectric glass transition (T_g) influences the pentacene film growth mode and OTFT response.

Due to the low charge carrier mobilities of organic semiconductors and the low dielectric property of the gate dielectric, traditional OTFTs are often operated at high voltages. ^[7] This is a problem in applications which require high current output for example for switching off the OLEDs. For other applications like radio frequency identification tags ^[8], smart cards ^[9] and portable displays ^[10] low operating voltages are required. Furthermore, patchable electronics (smart patches and smart textiles) ^[11] should operate at low voltages since they are worn on the human body.

Thus, conventional OTFTs cannot yet be considered as a suitable candidate ^[12] since the field induced current is proportional to the field-induced charge density and carrier mobility. One way to solve this problem is using high dielectric constant (high- k) gate insulators ^[13] which can increase the field-induced carrier density. However,

OTFTs based on high- k materials mostly use ceramics which are then usually brittle and expensive to prepare. These materials also suffer from poor mechanical properties which make them inconvenient to be used in flexible electronics. The high-temperature annealing process used for the preparation of these high- k materials is also not compatible with plastic substrates. Therefore, it is important to develop a cheap and easy way like a solution-processable method, to fabricate gate dielectrics with both high dielectric constant and mechanical flexibility. OTFTs using an organic insulator with a high dielectric constant seem to be promising for operation at low voltages¹. Nevertheless, neat polymer materials have relatively low dielectric constant (k) which limits their use in low voltage application. In order to overcome this problem, different nanocomposite dielectrics, containing inorganic nanoparticles with a high dielectric constant (k), have been studied^[15, 16, 17, 18]. However, nanocomposite dielectrics pose their own challenges. For e.g., they generally do not have a smooth surface which is required for well-aligned organic semiconductor growth. This results in a low on/off ratio and low carrier mobility in the low voltage range. In addition, increasing the amount of inorganic particles in nanocomposite materials leads to high leakage currents in the dielectric layer due to the fact that high k materials can generate a high leakage current pass^[19].

Fang- Chung Cheng et al^[20] have reported on the fabrication of high-performance pentacene-based OTFTs with a nanocomposite dielectric layer. The dielectric layer consisted of Poly-4-vinylphenol (PVP) and high-dielectric titanium oxide (TiO₂) nanoparticles. Nanosized TiO₂ particles were dispersed in organic solvent and the

¹ For e.g., low operating voltages for p -channel OTFTs can be achieved by using polyanionic electrolytes. The resulting OTFT has operating voltages of less than 1 V and shows fast switching less than 0.3 ms in ambient atmosphere.[14.

Herlogsson, L.; Crispin, X.; Robinson, N. D.; Sandberg, M.; Hagel, O. J.; Gustafsson, G.; Berggren, M., Low-Voltage Polymer Field-Effect Transistors Gated via a Proton Conductor. *Advanced Materials* **2007**, *19* (1), 97-101.]

dielectric layer was prepared by spin coating. It was found that the OTFTs with nanocomposite dielectric layer have higher field-induced current than that of devices with neat polymer since the dielectric constant was increased (Fig.4.1). The surface roughness and the dielectric constant increased with the amount of TiO_2 nanoparticles embedded in the polymer thin films. The device with the largest amount of TiO_2 (15 wt %) showed higher leakage current than the device with the lowest amount of TiO_2 (1 wt %). In order to solve the problem of leakage, the insulator layer was covered with a poly (α -methylstyrene) (P α MS) layer. The device on-off current ratio was increased since the over-coating smoothed the dielectric surface and decreased the concentration of surface defects.

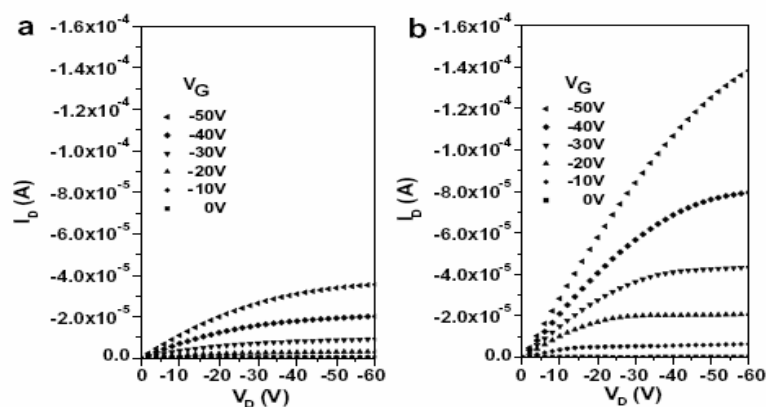


Figure 4.1 Output characteristics (drain current, I_D vs. drain voltage, V_D) of OTFTs with (a) a neat PVP insulator; (b) a composite insulator with 15 wt% TiO_2 nanocomposite insulators. (from Chen et al²⁰).

Conventional pentacene-based OTFTs are expected to exhibit p -type conduction. Nevertheless, according to recent studies [21, 5b] it is possible to also obtain n -type or ambipolar behavior in such devices. In these studies, there are two main parameters that determine the n -type conduction in pentacene-based OTFTs. The

first is the choice of suitable metal for source-drain electrodes. The second is the influence of the interface at the pentacene layer and gate dielectric.

Chua et al. ^[21] reported that the SiO₂ gate dielectric limited the *n*-type channel formation of OTFTs due to the presence of hydroxyl groups on the surface of SiO₂ which acted as electron traps. Thus, hydroxyl-free polymers such as divinyltetramethyldisiloxane-bis (benzocyclobutene) (BCB), polymethylmethacrylate (PMMA) ^[5b, 22] or polystyrene (PS) ^[23] were deposited on the surface of SiO₂ gate dielectric to isolate the electron traps in order to obtain electron conductive channels in OTFTs.

However, not all hydroxyl groups on polymeric dielectrics would trap electrons. In particular, ambipolar or unipolar (*n*-type) pentacene-based devices were demonstrated by using PVA as gate dielectric ^[4,24, 25]. J.-W. Chang et al. ^[5a] demonstrated the fabrication of pentacene-based OTFTs made with three kinds of polymer gate dielectrics (PVA, PVP or PS) and with Ca, Al or Au metals as source-drain electrodes in order to study the mechanism of the *n*-type conduction in such devices. The results showed that the hydroxyl groups of PVP limited *n*-channel formation in pentacene-based OTFTs by trapping electrons, as those of SiO₂, while the hydroxyl groups of PVA did not. This observation was explained by the difference of the dissociation constant of protons on PVP and PVA. The OTFTs with PVP gate dielectric outputted diode-like currents. The current decreased as the gate voltage increased corresponding to hole flows. No channel formation in the OTFTs was observed, although Ca electrodes (low work function ~ 2.9 eV) were used for efficient injection of electrons.

Ambipolar output characteristics for the pentacene-based OTFTs were observed with Au electrode and PVA as gate dielectric. These results could not be explained by the barrier height of charge injection from the metal to the pentacene layer. This behavior was observed in the studies by Singh et al. ^[4, 25]. The Singh's group

finding was that organic semiconductors can be ambipolar on hydroxyl-terminated dielectrics. They remarked this observation as an interesting result since it has already been suggested in the literature^[21] that surface dipoles make *n*-channel behavior less likely. Although ambipolar transistors can not be used to realize complementary circuits, they have great potential for complementary-like circuits.^[26,27] According to J.-W. Chang^[5a], “*So far, these extraordinary phenomena of OFETs with PVA are still under investigation.*”

In this chapter, we present organic transistors having acceptable capacitance gate insulators which are processable by spin-coating from solution, using water as a solvent. These prototype devices can (may) shed light on the manufacturing of cheap, simply patterned transistors that still have enough performance and the ability to operate at low voltages. The devices are based on DH4T films as semiconducting layers and have been fabricated by using inorganic SiO₂ nanoparticles embedded in PVA polymer matrix, as gate insulator layer. Rather high capacitance gate insulators and solution-processable polymer insulators could be achieved at the same time. Poly (vinyl alcohol) (PVA or PVOH) was adopted as the organic insulating polymer since it is non-toxic, cheap and commercially available polymer which has two important properties: it is soluble in water (and insoluble in organic solvents) and has already a relatively high dielectric constant ($k = 5-8$), provided the film thickness lies in the range of a hundred nanometers to several micrometers.^[28, 29] PVA and its copolymer can also be chemically and thermally cross-linked which may allow the stabilization of the layer.

4.2. Experimental part

Materials: The organic component, PVA (99% hydrolyzed grade) averaged M_w : 89.000-98.000 used in this study was purchased from Sigma-Aldrich. The inorganic component, LUDOX[®] SM colloidal silica, supplied also by Sigma-Aldrich, was an aqueous dispersion

containing 30 wt % of silica with an average particle size of 7 nm with surface area $\sim 230 \text{ m}^2/\text{g}$ and PH 9.1 Both PVA and colloidal silica were used as received from the suppliers without further purification.

Preparation of PVA and PVA/ SiO₂ nanoparticle solutions: A 30 g/L homogeneous solution of PVA was first prepared by dissolving PVA powder in boiling water and then continuously stirring for one hour. For preparing PVA/SiO₂ nanoparticle solutions, requisite amount of aqueous dispersion of colloidal silica was added to the PVA solution and continuously stirred 24 hour at room temperature to obtain a perfectly homogeneous solution. For example, in order to have PVA/ SiO₂ (5 wt %) we first dissolved 0.75g PVA powder in 25 mL flask. The amount of SiO₂ nanoparticles to be added into the polymer solution, in order to have 5 wt % concentration, was then calculated to be 0.0375g. But, as we have 30 wt% colloidal silica, the final amount of SiO₂ was calculated to be 0.125 g. ($30 \text{ wt\%} \times \text{SiO}_2 = 0.0375 \rightarrow \text{SiO}_2 = 0.125 \text{ g}$). Thus 0.125g of colloidal silica was added to the PVA solution. The same procedure was used for preparing PVA/ SiO₂ (30 wt %) solutions.

TFT fabrication: The transistors were fabricated on ITO substrates (thickness: 100 nm). The ITO substrates were washed 10 min in acetone and isopropyl alcohol and then rinsed with distilled water before being dried with nitrogen. Thereafter, the ITO substrates were patterned according to Fig.4.2. The part of the substrate intended to be etched was covered with a blue scotch and on the remaining parts, a blue resin was spin-coated (2400 rpm, 1000 rpm/s and 60s). After the spin-coating, the blue scotch was removed and the substrates were annealed for 10 min at 150°C in an oven. The substrate then immersed in fresh HCl (37%) for 5 min in order to be etched. After the etching process, the substrates were washed thoroughly with water and after drying the resistivity of the etched part was checked with a multimeter. When the reliability of the etching process was confirmed, the blue resin was removed with

acetone. In order to deposit the PVA or PVA/SiO₂ gate dielectric layers, the etched-parts and non etched- parts were separated with scotch. Afterwards, neat polymer or polymer/nanoparticle solutions were spin-coated on the etched parts. (2500 rpm, 1000 rpm/s and 60s). The resulting films with a thickness of about 165 nm, were then cured at 150°C and 80°C for an hour in air and twelve hours in vacuum oven, respectively. The TFTs device was designed as a bottom gate (ITO) and bottom-contact electrode structure. The Au source and drain electrodes were deposited through a shadow mask with a channel length (L) of 40 and 100 μm and width (W) of 7 mm in $\sim 10^{-6}$ mbar. A 2-nm-thick Cr layer was also deposited prior to gold as an adhesion promoter. Fig.4.3 (up), shows the shadow mask and the sample holder used for the electrode deposition.

Finally, DH4T was deposited by spin-coating (5000 rpm, 1000 rpm/s, 15 s) from a filtered solution in toluene (0.4 wt%). The solvent was then allowed to completely evaporate. Since PVA is hygroscopic in nature, the samples were stored inside desiccators filled with anhydrous silica gels.

Characterization method: The transmittance of the PVA and PVA/SiO₂ solutions were quantified with a UV-visible spectrophotometer (VARIAN) in the wavelength range of 200 to 800 cm^{-1} at room temperature. Contact angle with water droplets was evaluated using a Data physics OCA 20 contact angle meter.

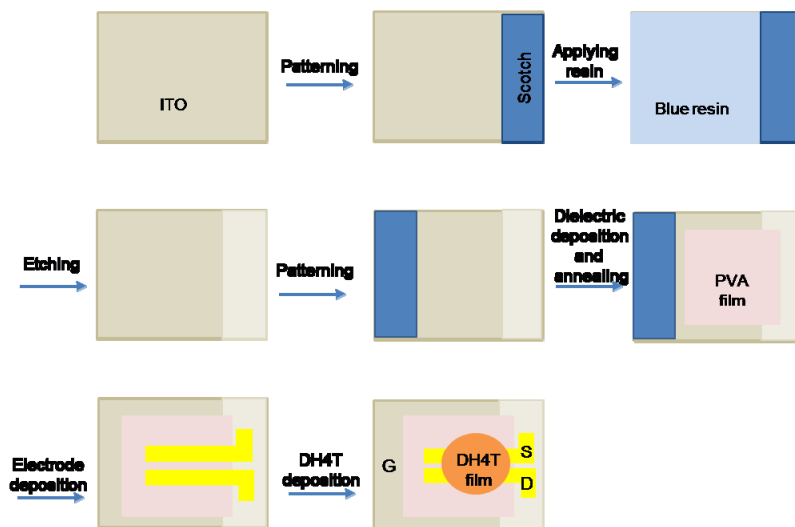


Figure 4.2 Schematic representation of the TFT fabrication approach used in this study. (S: source, D: drain and G: gate)

The surface morphologies were examined by AFM (Agilent 5500 SPM microscope). KPFM measurements were also realized with the same instrument (for more details see the previous chapter). Fig.4.3 (down) shows a device and sample holder used for KPFM measurement. The current-voltage and capacitance-voltage measurements were executed under ambient conditions using a low signal probe station with probeshield (PM8PS). IV and CV measurement unified in a single instrument. 4 SMU's with 10 fA resolution 2 SMU's with 0.1 fA resolution and CV measurement from 1 KHz to 5 MHz with 0.1 fF resolution.

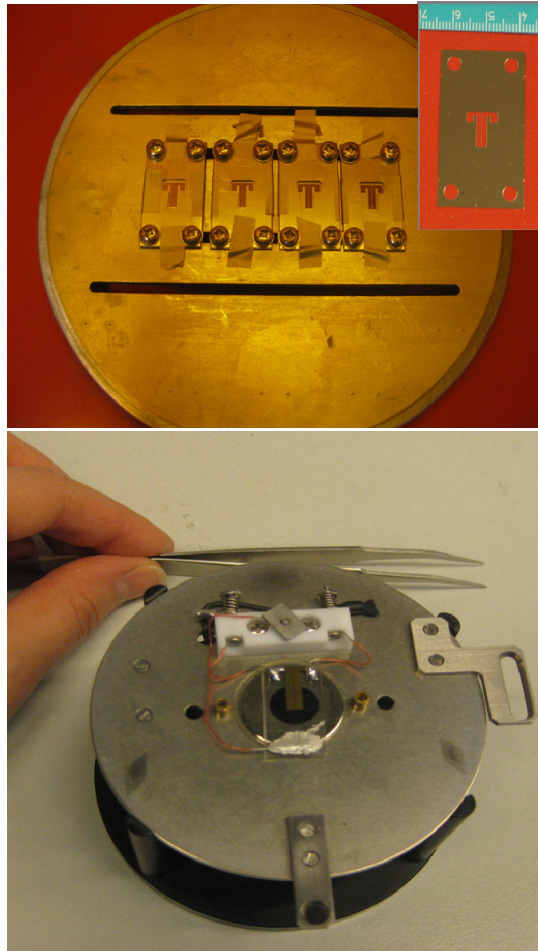


Figure 4.3 (up): Sample holder and shadow mask (inset), used for the electrode deposition; (down): An example of a device and sample holder used for KPFM measurement.

4.3. Results and discussion

4.3.1. Characterization of nanocomposite gate dielectric

4.3.1.1. Optical transparency of PVA/ SiO₂ solutions

As mentioned before, the solubility of PVA in water leads to a clear solution of polymer (Fig.4.4) and also a good dispersion of the SiO₂ nanoparticles inside the solution. Although PVA could inhibit the aggregation of the nanoparticles and keep them well dispersed in the solution, some agglomerations, was observed after rather long times. In order to avoid those precipitated nanoparticles, the clear upper parts of the solutions were used to make dielectric layers. In order to verify the presence of SiO₂ nanoparticles in the upper part of the solutions, UV-visible spectroscopic study was performed. Figure 4.4 shows the transmittance of PVA/ deionized water solutions with various loading of colloidal SiO₂. From the figure, it is evident that the transmittance drops with increasing the amount of SiO₂ nanoparticles. The decrease in optical transparencies with high loading of SiO₂ may be attributed to the variation of refractive indices of the polymer solutions with embedded SiO₂. However, all the solutions show reasonably high transparency with more than 70% in the visible wavelength transmitted.

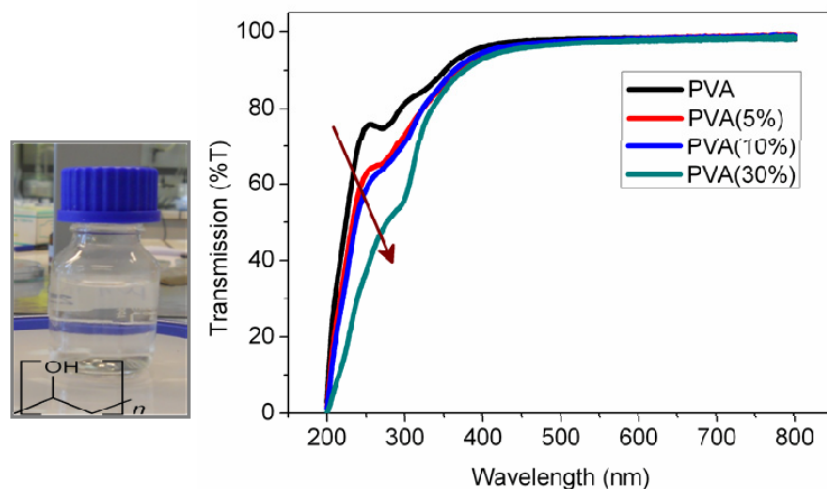


Figure 4.4 (left) A clear solution of PVA in deionized water and chemical structure of PVA; (right) UV-visible spectroscopic results of PVA-colloidal SiO_2 solutions with various amounts of SiO_2 nanoparticles. (The values in the paranthesis indicate the SiO_2 loading in wt%)

4.3.1.2. Surface properties of PVA/ SiO_2 layers

AFM images were acquired after deposition of PVA or PVA/ SiO_2 composites. The root-mean-square roughness values were measured to be about 0.8 nm for the neat PVA layer, 3.8 nm for the PVA/ SiO_2 (5 wt %) layer and 27.2 nm for the PVA/ SiO_2 (30 wt %) layer (Fig. 4.5 (d-f)). As it can be seen from the surface morphology in Fig.4.5 (d-f), the insulator roughness increased with the increasing concentration of SiO_2 blended. Particularly, the PVA/ SiO_2 (30 wt %) layer showed a grainy morphology not observed for pristine PVA and PVA/ SiO_2 (5 wt %) layers. Here grains are morphological defects, which may induce charge trapping.

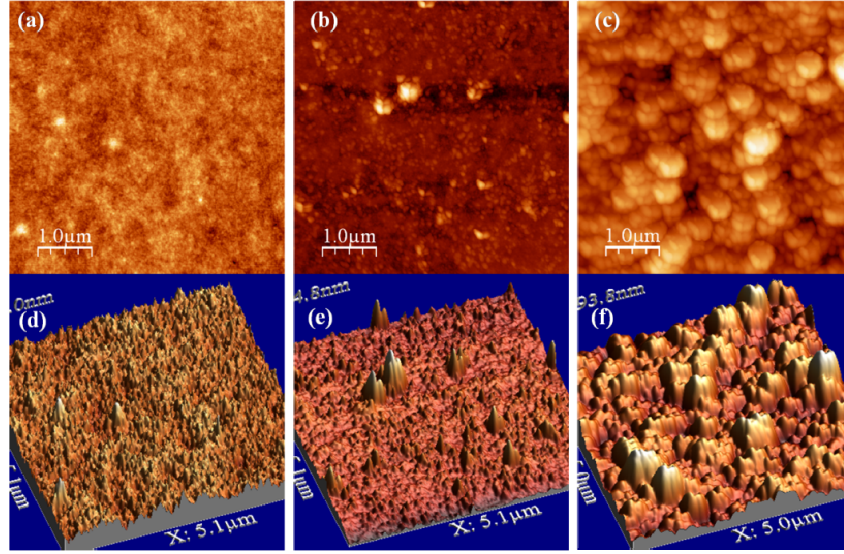


Figure 4.5 AFM images ($5 \mu\text{m} \times 5 \mu\text{m}$) of (a), (d) pristine PVA; (b), (e) PVA/ SiO_2 (5 wt %); (c), (f) PVA/ SiO_2 (30 wt %).

4.3.1.3. Dielectric properties of metal-insulator-metal (MIM) systems

One of the concerns with any gate dielectric material is the gate leakage, especially for polymer gate dielectrics ^[30]. In order to investigate this effect in our devices, current density-voltage (J - V) characteristics of pristine PVA and PVA/ SiO_2 gate insulators were measured by metal-insulator-metal (MIM) structures with ITO-insulator-Au. Fig.4.6 (a) shows the leakage current density of the pristine PVA and PVA/ SiO_2 gate dielectric layers as a function of applied bias. The leakage current at ± 1 V was about 10^{-5} for neat PVA and 10^{-3} A.cm^{-2} for two nanocomposite systems. The leakage current of nanocomposite gate dielectrics increased when increasing the concentration of SiO_2 nanoparticles in nanocomposite. The leakage problem is probably due to the structural defects induced by

the presence of SiO₂ nanoparticles.^[31, 20] This observation has been confirmed by the fact that the surface roughness of the insulators increased with the content of nanoparticles (Fig. 4.5 (d-f)).

However, according to the capacitance measurements shown in Fig.4.6 (b), the capacitance values of PVA nanocomposite dielectric layers increased compared to the neat PVA. Capacitance values of PVA, PVA/SiO₂ (5 wt %) and PVA/SiO₂ (30 wt %) are equal to about 0.21, 4.86 and 3.81 nF.cm⁻², respectively at 800 KHz. The SiO₂ nanoparticles thus indeed increase the dielectric properties of PVA.

Unexpectedly, the capacitance of the nanocomposite gate dielectrics decreased from 4.86 to 3.81 when concentration of SiO₂ in the nanocomposite increased from 5 wt % to 30 wt %.

4.3.2. Electrical characteristics of OTFTs

Conventional OTFTs need more than 15 V to be fully operational, which is incompatible with portable, battery-powered applications^[32]. Hence, taking this into account, electrical measurements in our experiments were mainly focused on low range gate and drain voltages.

Figure 4.7 plots the drain-source current versus the drain voltages swept from positive to negative values of DH4T-based OTFTs that were fabricated on neat PVA, PVA/ SiO₂ (5 wt %) and PVA/ SiO₂ (30 wt %) gate dielectrics on ITO-gate glass substrates and Au as source and drain electrodes. When the OTFT based on neat PVA were operated at negative gate voltages the *p*-channel conduction was observed, while applying positive gate voltages led to *n*-type behavior as can be seen in Fig.4.7 (b) and (a), respectively.

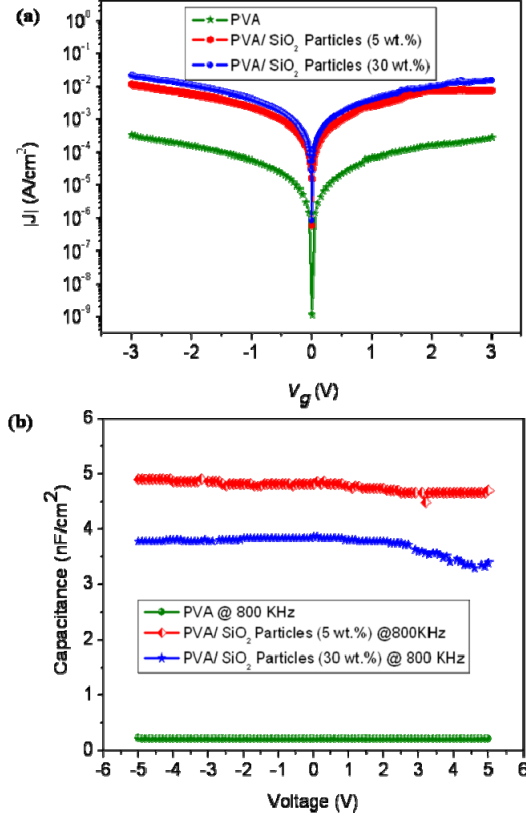


Figure 4.6 (a) Leakage current density and (b) capacitance of a pristine PVA and SiO₂ polymer composite dielectric layers.

However, the p -type output current was larger than that of n -type current. In Fig. 4.7(a), it was observed that I_d decreases as V_g increases negatively from 5 to 0, -5 and -10 (not shown in the graph) for V_d in the range of -10 to 10 V. This observation can be explained by an electron flow, but not an hole flow, contributes to the current. The field-induced positive charges compensated the conducting electrons as V_g increased. This ambipolar behavior has also been reported in literature ^[4, 5b,24].

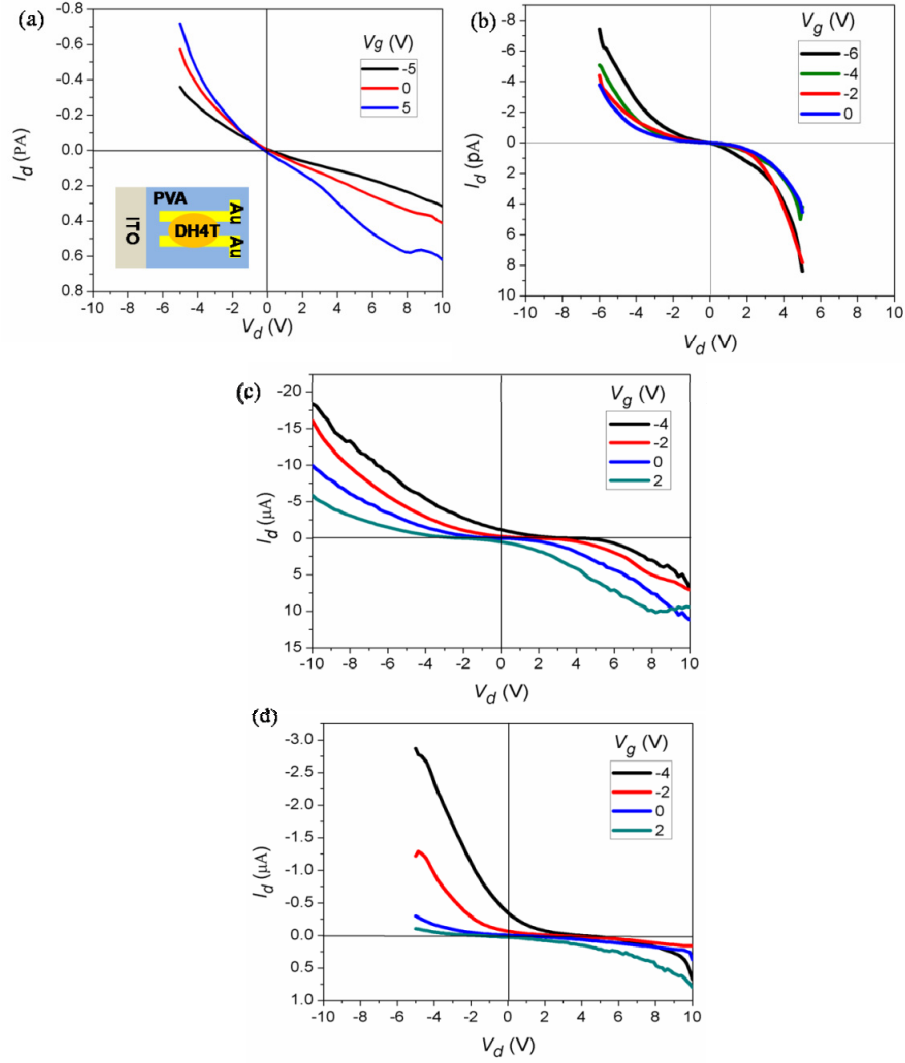


Figure 4.7. Output characteristics of ambipolar DH4T-based OTFTs on neat PVA gate dielectric in (a) n- and (b) p- channel operations. (c) on PVA/ SiO₂ (5 wt %) and (d) on PVA/ SiO₂ (30 wt %) gate dielectrics. The inset of (a) schematically depicts the structure of DH4T-based devices.

Figure 4.7(c) presents the drain-source current versus the drain voltage of a DH4T-based OTFTs which was fabricated on PVA/ SiO₂ (5 wt %) gate dielectric. Once more, we see the ambipolar behavior for these devices for the gate voltages ranged from -10 to 10 V. As for the PVA case, the *p*-type output current is larger than that of *n*-type current. However, the measured output current for the PVA/ SiO₂ (5 wt %) system is much larger than that of the PVA system i.e. (μA) currents against (*pA*). Figure 4.7 (d) presents the drain-source current versus the drain voltage of a DH4T-based OTFTs which is fabricated on PVA/ SiO₂ (30 wt %) gate dielectric. The ambipolar behavior is observed for gate voltages ranging from -10 to 10 V. As for the neat PVA and PVA/ SiO₂ (5 wt %) systems, the *p*-type output current is larger than that of *n*-type current. In addition, the output current is in the range of μA , similar to that of PVA/ SiO₂ (5 wt %) system. The increase of the drain current at low gate voltages and below the threshold voltage which is observed (e.g. Fig.4.9) is a phenomenon which has also been reported in literature. [5b, 33, 34]

Figure 4.8(a) and (b) plots the transfer characteristics of I_d vs V_g at $V_d = 5V$ for PVA/ SiO₂ (5 wt %) and PVA/ SiO₂ (30 wt %), respectively.

The properties and output currents of DH4T-based OTFTs with neat PVA and PVA/SiO₂ gate dielectrics are summarized in Table 4.1. It seems that the performance of devices based on PVA/SiO₂ gate dielectrics are improved compared to that of neat PVA. All devices exhibit ambipolar behaviors at low voltage and the *p*-type behavior is enhanced compared to the *n*-type conduction in all systems. Apparently, the better output characteristics obtained for the PVA/SiO₂ (5 wt %) devices are due to the larger capacitance and the formation of apparently less hydrophilic surfaces.

So far there are few information about the correlation of ambipolar transport [35] with the morphology of organic

semiconducting thin films at the interface between the organic layer and the gate dielectric. [36]

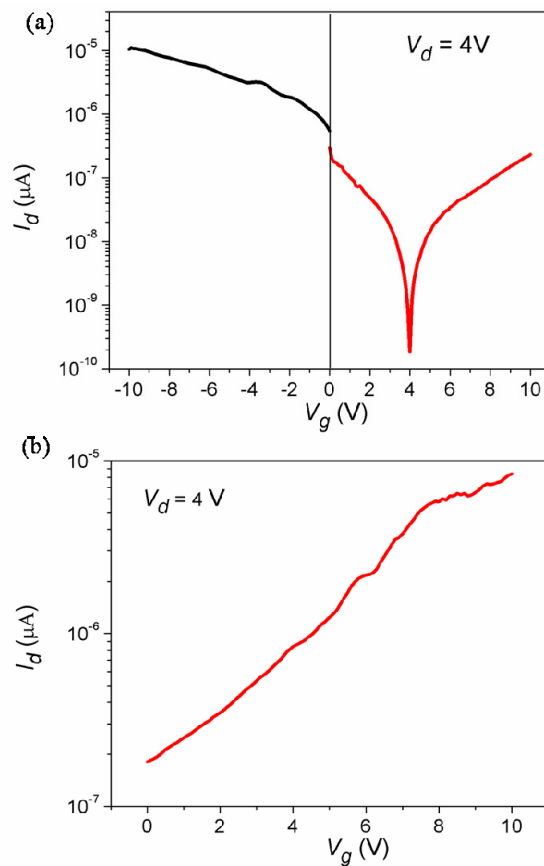


Figure 4.8. Transfer characteristics of ambipolar DH4T-based OTFT on (a) PVA/SiO₂ (5 wt %) and (b) PVA/SiO₂ (30 wt %) gate dielectrics.

Table 4.1. Properties and output current of DH4T-based OTFTs with neat PVA and PVA/SiO₂ gate dielectrics.

% of SiO ₂ -PVA	Insulator			Device	
	rms roughness (nm) for 5×5 μm	Contact angle (deg) ²	Capacity (nF/cm ²)	$ I_d $ (μA)	
				$V_d = -5$ V	$V_d = 5$ V
0	0.8	32	0.21	6×10^{-6}	0.4×10^{-6}
5	3.8	52	4.86	7	6
30	27.2	39	3.81	2.8	0.2

As mentioned before, the functional groups on polymeric gate dielectrics can be an important parameter to determine the type of accumulated charge carriers. The functionality of the hydroxyl groups on neat PVA could be different from that of the PVA/SiO₂ systems. It could be possible that embedding SiO₂ nanoparticles alter the functionality of the dielectric surface. It has been reported on the presence of reactive groups, like –OH, on the surface of different kinds of nanoparticles^[37]. Also, according to the literature^[38] PVA has the ability to form hydrogen bonds with surface hydroxyl groups of SiO₂ nanoparticles.

On that basis, the optimum characteristics observed for PVA/SiO₂ (5 wt %) may be due to a balance between the increase of the dielectric constant of the film and the decrease of charge traps on the

² This is the angle of a droplet of solvent onto a, at least, partially soluble film and should not be interpreted as a regular contact angle of a fluid of non soluble solid.

dielectric surface due to either chemical modifications and/or due to morphological modifications such as a moderate interface roughness.

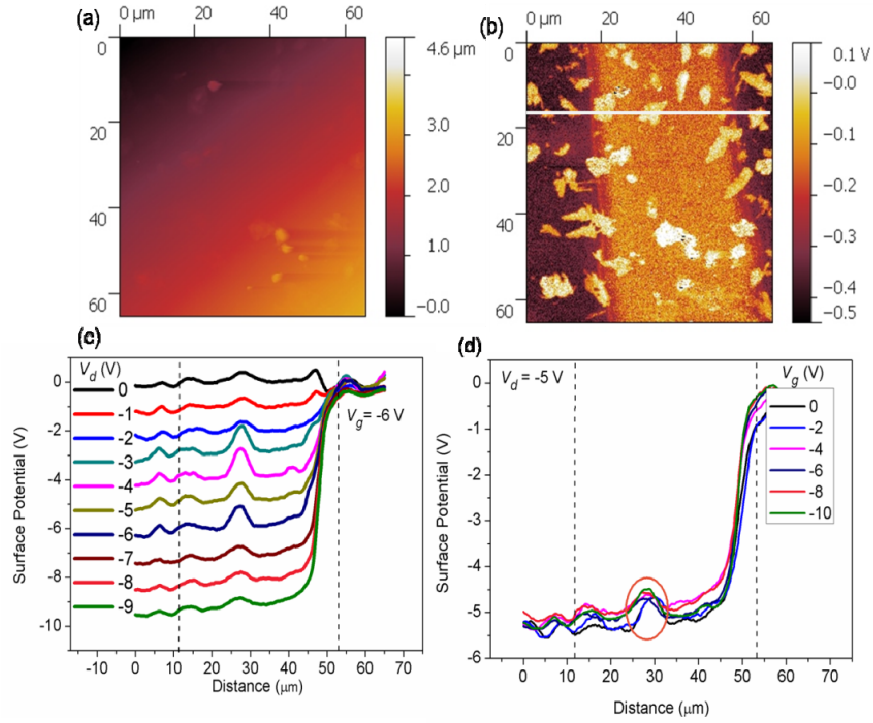
Finally, it should be mentioned that our transistors did not show saturation behavior in the low voltage range of operation, which was our interest, as mentioned before. Nevertheless, there are reports on reaching saturation regime for similar systems with neat PVA as gate dielectric at high voltages i.e. $V_g > 60$ V. ^[24, 4, 5a]

4.3.3. KPFM study of OTFTs

As it was described in the previous chapter, devices based on spin-coated films are more suited for performing microscopic measurements such as KPFM. DH4T films were thus deposited by spin coating on the polymer gate dielectrics and the Au electrodes.

Figure 4.9 shows topography, typical potential image and potential profiles obtained for a 40 μm wide-channel transistor with neat PVA gate dielectric. The surface potential profiles at various drain and gate voltages were extracted from the surface potential images along the white line indicated in Figure 4.9(b). Figure 4.9(c) shows the surface potential profiles in the channel at fixed $V_g = -6$ V with V_d varying between 0 and -9 V. Increasing potential drops are observed at the source contact with increasing V_d . However, a direct linear decrease of the potential from the source to the drain is not observed. Since the measurements were performed under ambient conditions, this result may be explained by the fact that a layer of water has been adsorbed on the surface of the film during the measurement. This water layer may screen the real surface potential. The same behaviour is also observed for the gate voltage dependent profiles in Fig. 4.9 (d). It should be noted that for good contacts, potential drops at source and drain are generally equal. According to Fig. 4.9 (d), there is a charge injection issue and is not probably asymmetric contact resistance. The surface potential profiles presented in Figure 4.9(d) were acquired at different gate voltages ($-10\text{V} \leq V_g \leq 0$ V) for a fixed drain voltage ($V_d = -5$ V).

Figure 4.9 Potentiometry of DH4T/PVA thin-film transistor (40 μm channel length). (a) $60 \times 60 \mu\text{m}^2$ topographic image; (b) corresponding surface potential image at $V_d = 0 \text{ V}$, $V_g = -2 \text{ V}$; (c) potential profiles as a function of



drain voltage, with $V_g = -6 \text{ V}$; (d) potential profiles acquired along the horizontal line shown in (b) as a function of gate voltage, with $V_d = -5 \text{ V}$; the vertical dashed lines indicate the edge between the contacts and the conducting channel.

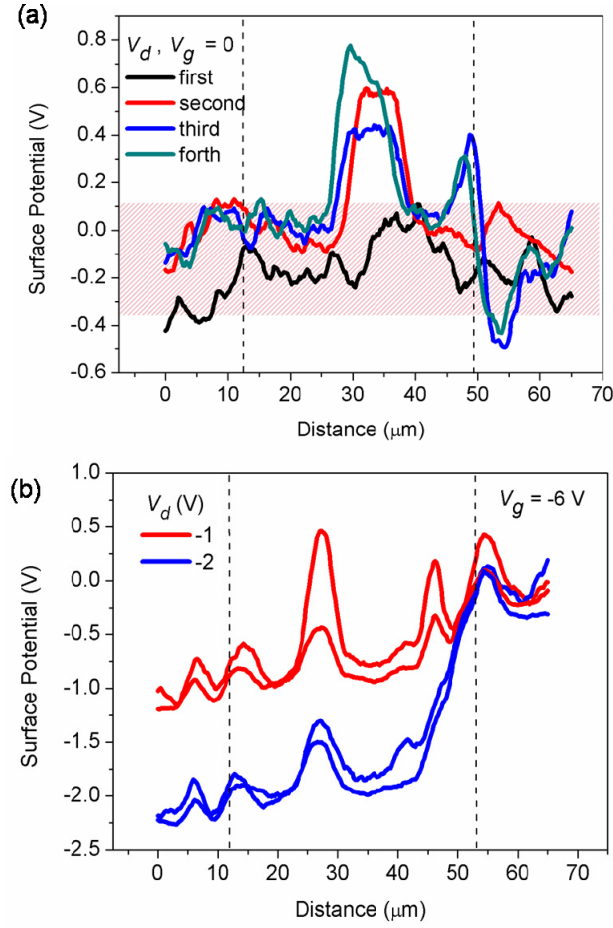


Figure 4.10 (a) Surface potential profiles of DH4T/PVA thin-film transistor (along line shown in Fig.4.12 (b)); black: initial off-state, red: after ramping V_g down to -10V (1V steps) with $V_d = 0$ V, blue: after ramping V_g down to -10V (1V steps) with $V_d = -5$ V, green: after ramping V_d down to -9 V (1V steps) with $V_g = -6$ V; (b) Hysteresis curves measured at two drain voltages on the same device.

According to Fig. 4.9 (d), apparently the charge accumulation in the channel increases with increasing the gate voltage. This is especially the case in thicker crystals as the one marked by the orange-circle in V_g -dependent profiles. The same bump is observed in the V_d -dependent profiles for the $-6\text{V} \leq V_d \leq -2\text{V}$.

In order to study charge trapping effects, KPFM measurements were realized by varying V_g and V_d according to certain protocols consisting in the progressive biasing of the devices followed by their switching off and the KPFM measurement of the surface potential. As it can be seen in Fig. 4.10 (a), a positive electrostatic potential is observed in the channel after biasing the device in the on-state for an extended period of time and then switching it off, except after the first polarization ramp that was realized with $V_g = 0\text{V}$. (surface potential measurement was along white line shown in Fig. 4.9 (b)) For the three other polarization ramps realised with a negative bias of the gate, surface potential values increase in the channel, especially in thicker crystals attributed to the presence of trapped charges.

Another consequence of trapped charges is the hysteresis behaviour observed during the device operation (Fig. 4.10 (b)). This hysteresis behaviour was characterized as follows: V_d was first decreased stepwise (-1V , -2V , -3V) and then back increased (-2V and -1V) at fixed V_g (-6V). The surface potential distribution was mapped at each voltage. These analyses reveal hysteresis behaviors across the channel for all the applied voltages, especially via the thicker crystals. At the larger value of drain voltage i.e. $V_d = -2\text{V}$, the hysteresis decreased. This may indicate that larger drain voltage values induce an easier removal of the trapped charges.

Figure 4.11 shows topography, typical potential image and potential profiles obtained for a 40 μm wide-channel transistor with PVA/ SiO_2 (5 wt %) gate dielectric. The surface potential profiles at various drain and gate voltages were extracted from the surface potential images along the white line indicated in Fig. 4.11(b). Figure 4.11(c) shows the surface potential profiles in the channel at fixed $V_g = -6$ V with V_d varying between 0 and -9 V. The surface potential profiles presented in Figure 4.11(d) were acquired at different gate voltages ($-10\text{V} \leq V_g \leq 0$ V) for a fixed drain voltage ($V_d = -5$ V). Similar to the case of PVA system, except for a sharp drop of the potential at the source/ channel interface, a linear decrease in the surface potential from source to the drain was not observed perhaps due to the water adsorption at the interface or a charge injection issue.

According to the charge trapping measurements shown in Fig. 4.12 (a), bias-stressing of this device has less effect on charge trapping. Lower amount of charges seem to be trapped after consecutive biasing or it may possible that charge trapping is dictated by the charge injection. However, even in the initial off-state there are traces of trapped charges in the device as can be seen in Fig.4.12 (a) and in Fig.4.11 (b). The device showed hysteresis behaviour for all applied voltages, especially via the thicker crystals. At the larger value of drain voltage i.e. $V_d = -2$ V, the hysteresis decreased. Maybe larger drain voltage values induce an easier removal of the trapped charges.

Figure 4.13 shows topography, typical potential image and potential profiles obtained for a 40 μm wide-channel transistor with neat PVA/ SiO_2 (30 wt %) gate dielectric.

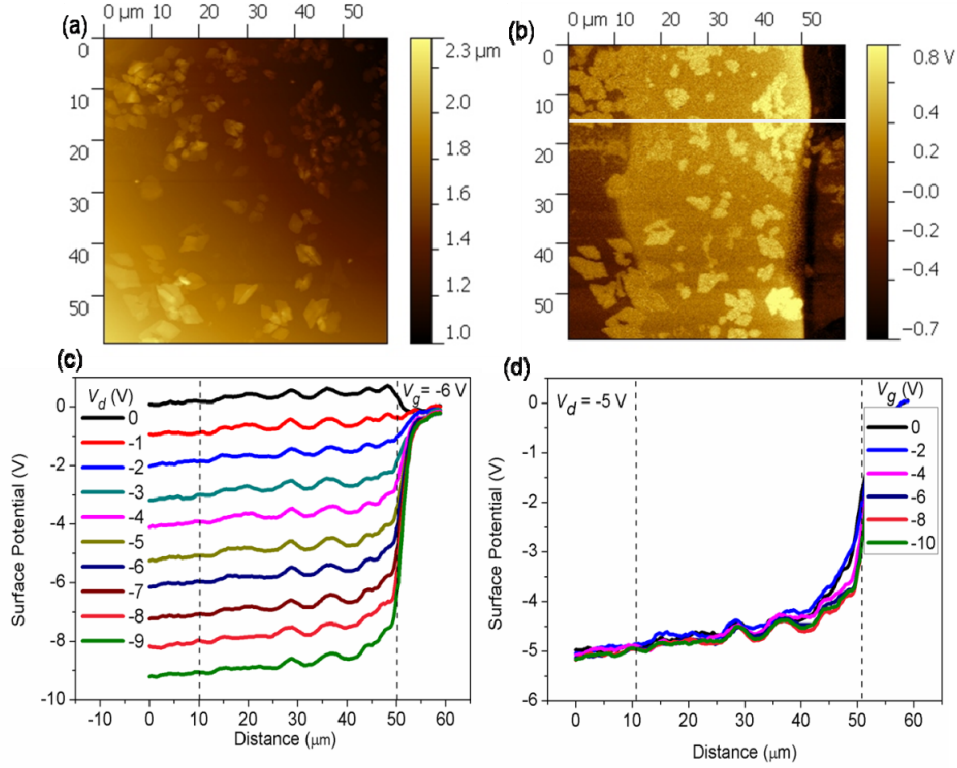


Figure 4.11 Potentiometry of DH4T/PVA/SiO₂ (5 wt%) thin-film transistor (40 μm channel length). (a) 60×60 μm² topographic image; (b) corresponding surface potential image at $V_d = 0$ V, $V_g = 0$ V; (c) potential profiles as a function of drain voltage, with $V_g = -6$ V; (d) potential profiles acquired along the horizontal line shown in (b) as a function of gate voltage, with $V_d = -5$ V; the vertical dashed lines indicate the edge between the contacts and the conducting channel.

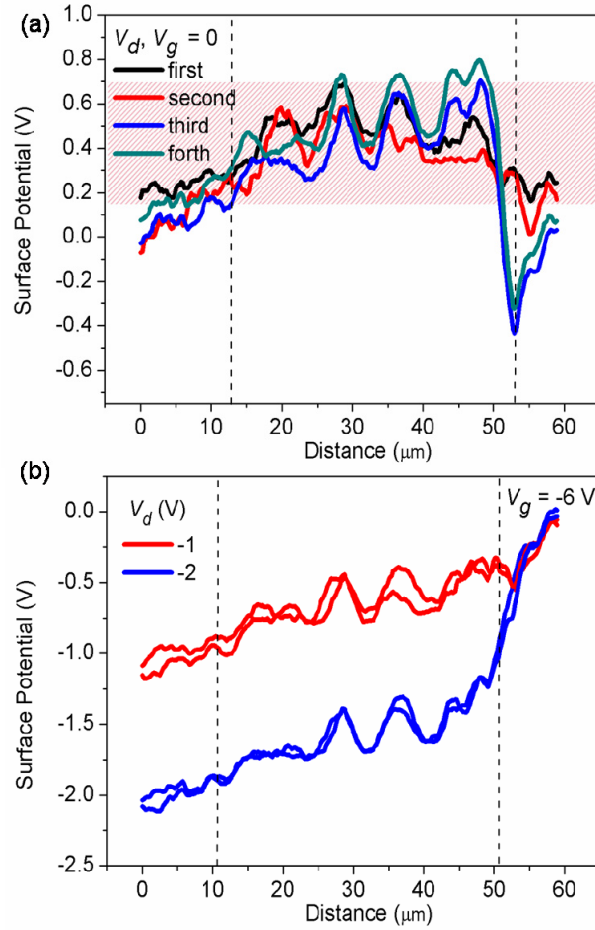


Figure 4.12 (a) Surface potential profiles of DH4T/PVA/SiO₂ (5 wt%) thin-film transistor (along line shown in Fig.4.14 (b)); black: initial off-state, red: after ramping V_g down to -10V (1V steps) with $V_d = 0$ V, blue: after ramping V_g down to -10V (1V steps) with $V_d = -5$ V, green: after ramping V_d down to -9 V (1V steps) with $V_g = -6$ V; (b) Hysteresis curves measured at two drain voltages on the same device.

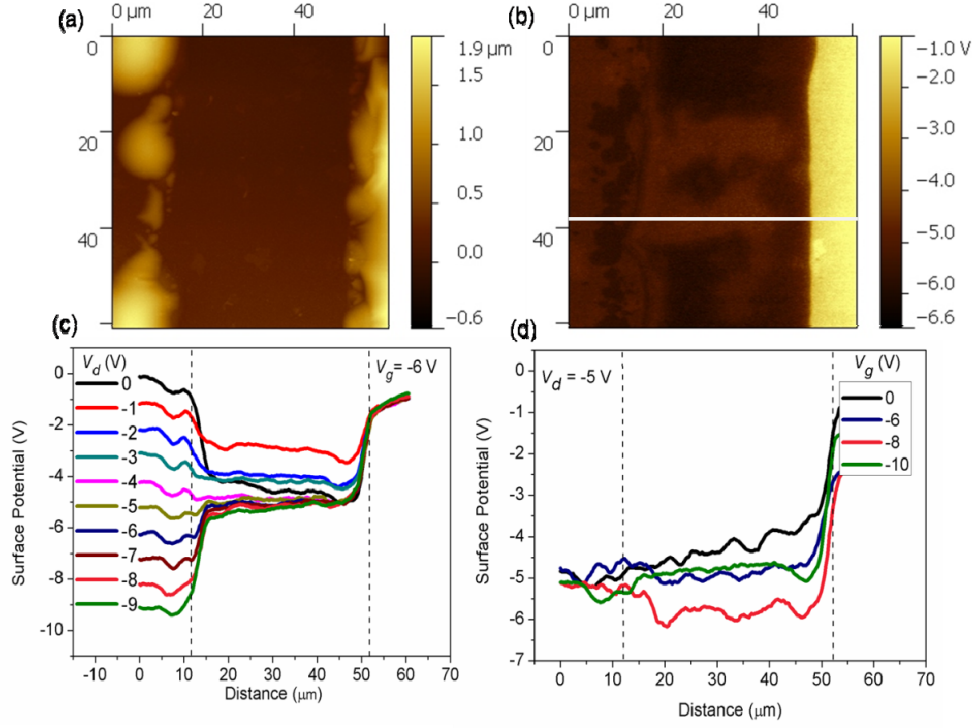


Figure 4.13 Potentiometry of DH4T/PVA/SiO₂ (30 wt %) thin-film transistor (40 μm channel length). (a) $60 \times 60 \mu\text{m}^2$ topographic image; (b) corresponding surface potential image at $V_d = 0$ V, $V_g = -6$ V; (c) potential profiles as a function of drain voltage, with $V_g = -6$ V; (d) potential profiles acquired along the horizontal line shown in (b) as a function of gate voltage, with $V_d = -5$ V; the vertical dashed lines indicate the edge between the contacts and the conducting channel.

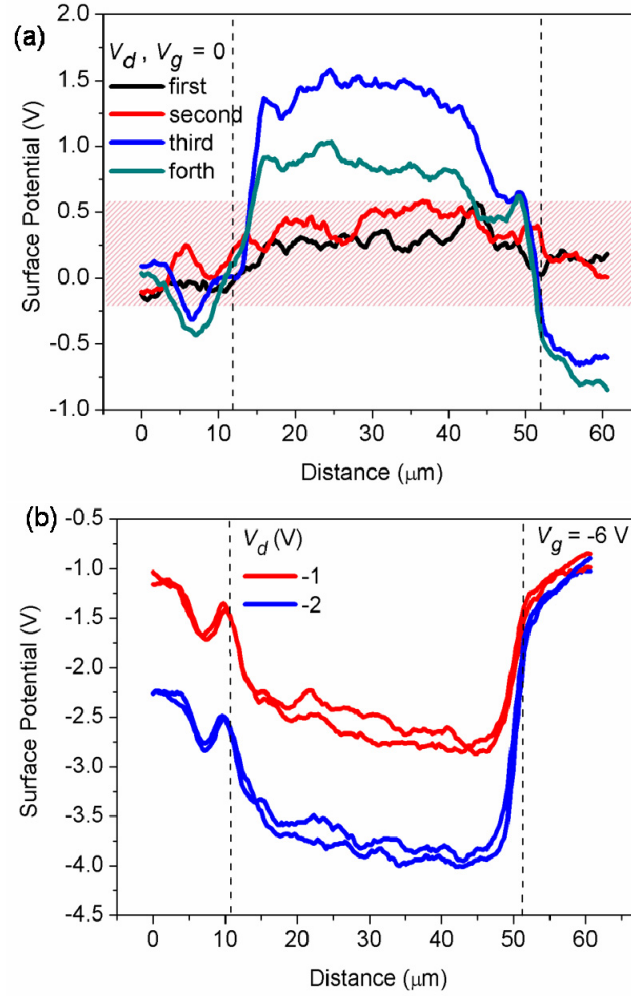


Figure 4.14 (a) Surface potential profiles of DH4T/PVA/SiO₂ (30 wt%) thin-film transistor (along line shown in Fig.4.16 (b)); black: initial off-state, red: after ramping V_g down to -10V (1V steps) with $V_d = 0$ V, blue: after ramping V_g down to -10V (1V steps) with $V_d = -5$ V, green: after ramping V_d down to -9 V (1V steps) with $V_g = -6$ V; (b) Hysteresis curves measured at two drain voltages on the same device.

According to the literature ^[39] there are generally two behaviors for each operational regimes (i.e. linear or saturation) of an OTFT: the unsteady-state to the steady-state. Devices progressively switch from the unsteady to the steady state. When a device is switched on, it is generally in an unsteady state. In this situation holes are initially able to enter the channel from both the source and drain sides; both electrodes act as injecting contacts for a short period of time until a non-vanishing source-drain electric field is established. When a steady-state is reached, injected carriers accumulate at the organic layer/dielectric interface and a channel is formed. This charge accumulation leads to a slope of the potential between the source and drain and thus to an electric field which drives a current through the device. The unsteady-state situation is seen for the PVA / SiO₂ (30 wt %) device in Fig.4.13 (c). When increasing the drain voltage, potential drops at source/ channel and drain/ channel interfaces appear indicating the presence of contact resistances. The gate voltage dependency of profiles is clearer for this device compared to the previous ones. The surface potential decreases when decreasing the gate voltage except for $V_g = -10$ V. At this voltage, the surface potential increases. This may be due to an increased accumulation.

The charge trapping measurements shown in Fig.4.14 (a), reveal that bias-stressing of this device indeed induces charge trapping. A larger amount of charges seem to be trapped after consecutive biasing compared to the initial off-state. Trapped charges appear as a large, homogeneous and positive surface potential all over the channel, contrary to the previous systems in which less trapping effects were observed. Finally, the device presents hysteresis behaviour for all applied voltages in an unsteady-state regime. At the largest values of drain voltage i.e. $V_d = -2$ V, the hysteresis decreases as was also the case for the two previous devices.

Comparing the surface potential profiles at initial off- states ($V_g = 0$, $V_d = 0$) of DH4T/PVA, DH4T/PVA/SiO₂ (5 wt%) and DH4T/PVA/SiO₂ (30 wt%) devices, shown with pink hatched area in Fig. 4.10 (a), 4.12 (a) and 4.14 (a) reveal that there are different

charge accumulation in the channel of these devices which have influenced the measured surface potential (SP). Particularly, for the device with neat PVA, surface potential has been influenced by accumulation of negative charges such that $SP < 0$. For the two other devices with embedded SiO_2 nanoparticles, $SP > 0$ at initial off-state indicates the presence of positively-charged carriers in the channel. This observation may also show that charging a neat polymer with nanoparticles can modify the semiconducting layer/ dielectric interface and thus influence electrical properties such as surface potential.

4.4. Conclusion

In this study, PVA and PVA/ SiO_2 nanocomposites were used to fabricate the gate dielectric layer of OTFTs. The electrical properties of DH4T-based OTFTs were investigated. All devices showed ambipolar behavior in the low-voltage range. However, the device characteristics on the device with PVA/ SiO_2 (5 wt %) was improved compared to the neat PVA and PVA/ SiO_2 (30 wt %) systems. This corresponds to a larger capacitance. The optimum characteristics observed for PVA/ SiO_2 (5 wt %) may be due to a balance between the increase of the dielectric constant of the film and the decrease of charge traps on the dielectric surface due to either chemical modifications and/or due to morphological modifications such as a moderate interface roughness.

Regarding the KPFM measurements, for the device with neat PVA negative surface potential, corresponding to accumulation of negative charges (electrons) was measured at initial off-state. In contrast, positive surface potentials, corresponding to accumulation of positive charges (holes) were measured for the devices with PVA/ SiO_2 . This can show how charging the polymer with nanoparticles, can modify the semiconducting layer/dielectric interface and thus influence the electrical properties such as surface potential.

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General conclusions and perspectives

The main objectives of this thesis were to *microscopically* study the morphology and electronic properties of self-assembled monolayers of semiconducting alkyl-substituted oligothiophene molecules and the morphology and electronic transport in the channel of OTFTs based on these molecules. To reach these goals, scanning probe microscopy techniques were used: STM, STS, AFM, KPFM.

First, we reported on the STM investigations of the structure of adsorbed layers of three kinds of α,α' -alkylated oligothiophenes (DH4T, DOTT and ddOD4T) on different substrates such as HOPG and MoS₂ at the liquid/solid interface or under dry conditions. First, the ability of these molecules to self-assemble on HOPG was investigated. We demonstrated that DH4T and DOTT did not form a stable molecular film on HOPG. For ddOD4T just a temporarily adsorption on HOPG was observed which resulted in fuzzy STM images. The problem was mainly solved by changing the substrate from HOPG to MoS₂. The longest oligothiophene i.e. ddOD4T did not adsorb on MoS₂ surface, perhaps due to its liquid-crystalline properties at room temperature. The two other molecules formed well ordered monolayers both at long- and short- length scales. The molecular arrangements of DH4T and DOTT were then studied with a joint theoretical/experimental approach. Our results indicated that DOTT and DH4T form well-ordered monolayers at large scales on MoS₂, with interdigitated packing while not having preferred adsorption sites and orientations. However, the formation of DH4T monolayers seemed to be more favorable than the formation of DOTT assemblies. Furthermore, the electronic properties of the self-assembled structures formed by DH4T and DOTT were probed locally with scanning tunneling spectroscopy at the solution/MoS₂ interface and under dry conditions. The acquired I - V curves revealed a clear conductance band gap. The band-gap observed for DH4T was smaller than that of DOTT, showing that the width of the *experimentally* observed band-gap depends on the number of thiophene rings in the molecule. One may conclude that chemical tailoring (number of thiophene rings and length of side chains) of the

molecules strongly determines both the electronic properties and the self-assembly of this kind of molecules.

Then, we studied the morphology and the charge transport mechanisms in the channel of OTFTs based on these three molecules without or with surface modification (silanization) of the gate silicon oxide. First, we optimized the morphology of the active layers via modifications in thin-film preparation process to make them suitable for performing KPFM measurements. Then, the structure and local electronic properties of devices under operation were investigated by AFM and KPFM, respectively. Various parameters such as V_g -dependency, V_d -dependency, hysteresis and charge trapping effects were studied. The role of the gate insulator modification with a self assembled monolayer (C_{10}) on the above properties has also been investigated. Smaller and more densely packed crystals in addition to more uniform films were observed on the silanized devices. Clear V_g and V_d dependency of the surface potential profiles were measured, in all cases. Our results, in overall, certify that factors such as molecular packing arising from the morphology optimization and nature of the substrate (silanized as opposed to pristine) can play a distinctive role in the quality of charge transport properties.

Finally, in the last chapter, organic thin-film transistors (OTFTs) based on DH4T molecules spin-coated on polymeric composite gate dielectrics, were fabricated and characterized macroscopically and microscopically. We adopted poly (vinyl alcohol) (PVA) as a gate insulator deposited by spin-coating method. The preparation and characterization of the PVA layers with and without SiO_2 nanoparticles were optimized. Several devices, showed ambipolar behavior in the low-voltage range. The device characteristics of PVA/ SiO_2 (5 wt %) seemed to be improved compared to the neat PVA and PVA/ SiO_2 (30 wt %) systems perhaps due to the formation of higher capacitance and a balance between the increase of the dielectric constant of the film and the decrease of the charge traps on the dielectric surface due to either chemical differences and/or due to morphological modifications such as an optimal interface roughness.

Regarding the KPFM measurements, for the device with neat PVA negative surface potential, corresponding to accumulation of negative charges (electrons) was measured at initial off-state. In contrast, positive surface potentials, corresponding to accumulation of positive charges (holes) were measured for the devices with PVA/SiO₂. This can also show that how charging the polymer with nanoparticles, can modify the semiconducting layer/dielectric interface and thus influence the electrical properties such as surface potential. According to the KPFM measurements, less charge trapping effects was also observed for the device with 5% SiO₂ compared to the 30% one.

This thesis was thus mainly devoted to the nanoscale characterization of semiconducting molecules and OTFTs based on them. We developed protocols and platforms which can now be applied to other molecular systems such as polymers, small molecules like other oligomers. Also, it is worth and interesting to study the existence of wetting and/or thin-film phase on silanized SiO₂, as the morphology of the semiconductor film deposited on SiO₂, can influence charge transport specially at the interface with the gate dielectric. Moreover, there are possibilities to perform more detailed experiments to study charge trapping at grain-boundaries. On that basis, measurements related to the dynamics of charge trapping or activation energy studies can be realized.

Also recently, layered MoS₂ has attracted increasing attention in the research community due its interesting electrical and optical properties, absence of dangling bonds, relatively high Earth abundance, and thermal stability up to 1,100 °C. This suggests possibilities for flexible, transparent and 2D electronic applications. Mono- and multi-layer MoS₂ nanoflakes were obtained via mechanical exfoliation^[1], solution-based chemical exfoliation^[2], and CVD based synthesis^[3]. Carrier mobility values over 200 cm²/Vs in top-gated transistors based on monolayer MoS₂^[4] and in the range 0.1-10 cm²/Vs in back-gated devices based on thin layers of MoS₂^[1, 5] were reported, showing good electronic conducting property. On

optical properties, MoS₂ exhibits direct bandgap (1.85 eV) in its monolayer and indirect bandgap (1.2 eV) in multilayer/bulk form, respectively ^[6,6b,7]. Since the material optical bandgap is determined by the physical thickness (or layer number), MoS₂ is considered to be a potentially viable candidate for photovoltaic solar cell ^[8] and photodetector ^[9] applications. There are also recent reports on molecular sensing applications ^[10,11] due to MoS₂ 2D expansion and high surface-to- volume ratio which make it sensitive to changes in its surroundings.

As it has been shown in this manuscript, self-assembled monolayers of alkyl-substituted oligothiophenes can be formed on MoS₂ due to a possibility of specific interactions between the sulfur-containing molecular adsorbate and the MoS₂ surface. On that basis, it could be possible to fabricate devices based on a double- or multi-layered combination of MoS₂ with alkyl-substituted oligothiophenes (DH4T and DOTT) or with organosilicon derivatives of α , α' - dialkyloligothiophenes which have already shown potential applications in organic bulk heterojunction photovoltaic solar cells ^[12]. Deposition of such semiconducting compounds on MoS₂ for fabrication of optoelectronic devices, may help to tune MoS₂ optic and electronic properties and thus, may improve the device performance for above mentioned applications. The devices can be investigated further microscopically, using SPM techniques such as KPFM and CS-AFM to gain more in depth knowledge about.

Concerning the polymer composite gate dielectrics which combine film-forming ability of the polymers with high-capacitance property of the nanoparticles, they are promising gate dielectric candidates for flexible organic thin-film transistors. Our preliminary results on such systems show that the performance of OTFTs based on the polymer dielectrics and DH4T molecules as conductive layer, has the potential to be improved. Infrared microscopy characterisation of the PVA and PVA/SiO₂ nanocomposite thin films, besides the chemical characterisation by for e.g., angle- resolved XPS may be

employed in order to obtain more in depth information of the possible mechanisms at the semiconducting film/ dielectric interface. There are also other parameters which can be tuned such as the optimization of the dielectric/semiconducting layer interface or the replacement with other convenient nanoparticle/polymer systems. The use of dielectric- screening by applying thin and high- k gate dielectrics such as HfO₂ for the local top-gate can also be considered as a solution to enhance the mobility in such devices. From the microscopic characterization point of view, CS-AFM could also be used as a complementary tool to investigate electronic properties of OTFTs.

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** Appendix **

KPFM measurements

As it was already discussed in chapter 3, it was observed that the Inter Grain Regions (IGRs) play important role in « charge trapping » in our DOTT-based OTFTs. This section first provides more detailed information about the essence and concept of the IGRs as well as their contribution in charge transport via the dependency of the surface potential in these regions to the applied gate voltages. (Fig.A.1)

After taking a topography scan, we selected one line crossing a few IGRs between DOTT crystals [line shown in Fig. A.1 (a)] and measured the surface potential along this line. The source and drain electrodes were grounded and the V_g was varied between 0 and -20 V. The data are plotted in Fig. A.1 (b). The two vertical dashed lines mark the source and drain electrodes. From Fig. A.1 (b) it can be seen that the surface potential for $V_g = 0$ is equal to zero both in the DOTT crystals and within the IGRs. When a negative bias is applied to the electrode, the surface potential does not vary on DOTT crystals while a surface potential dependent on the gate voltage is measured in the IGRs. As the gate voltage becomes more negative, the surface potential in IGRs drop to a minimum value for $V_g \approx -10$ V and then increases again. The fact that the surface potential does not follow exactly the applied gate bias suggests that the thin IGRs between the DOTT crystals are at least partially covered by DOTT molecules and that some holes can thus accumulate when a gate bias is applied. Nevertheless, the amount of accumulated charges is not enough to completely screen the gate bias. This result might be explained if we suppose that the DOTT film in IGRs is not continuous and thus only a partial accumulation layer can be formed there. The structure of the film might be similar to the schematic model shown in Figure A.1 (c).

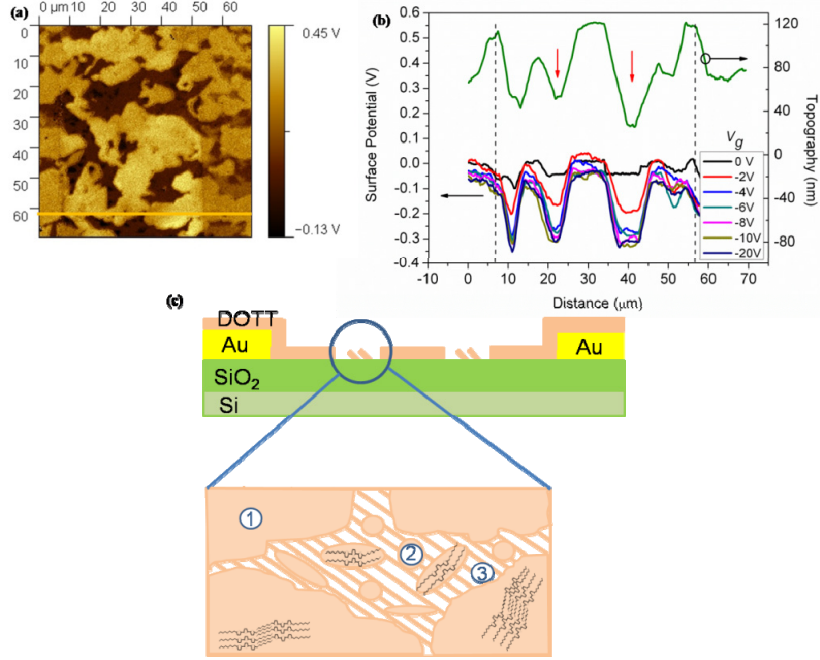


Figure A.1 (a) Topography image of the unbiased DOTT sample. (b) Surface potential profiles along line shown in (a) at various gate voltages. The corresponding topography profile is also shown. The red arrows point the places where the IGRs are. (c) Schematic cross-section of the transistor with presenting the thicker regions (DOTT crystals) and the thinner regions (IGRs); Schematic top view of the encircled area is also shown which corresponds to an inter grain region between crystalline grains (1). The proposed structure, composing relatively ordered DOTT clusters (2) and regions with no or incomplete DOTT coverage and weak connectivity (3) is shown schematically. (The Schematic is inspired from ^[1])

The film in the IGRs might consist of discontinuous areas of a very thin DOTT layer (marked as 2) and small regions with no or weak DOTT coverage (marked as 3). Therefore, an accumulation

layer can be formed in (2) while no or only an incomplete accumulation can be made in (3). The measured surface potential in the IGRs might be a weighted average of the surface potential of the regions where an accumulation is present, which is almost equal to the surface potential in DOTT crystals (marked as 1) and of the regions without any accumulation layer, which is equal to the potential of the gate electrode plus the gate voltage-independent contribution due to any fixed charges.

The surface potential becomes less negative when a more negative gate bias is applied. This suggests that the accumulation increases and thus proposes that the portions of the film which previously could not accumulate charges (mark as 3) are now able to do so. The barrier which prevents the accumulation of charges in these regions at low gate bias may also be responsible for charge trapping. These regions (mark as 3) may be associated with electronic defects at the edges of the DOTT crystallites (regions marked as 2), may thus be the preferential location for the trapped charges.^[1] As mentioned in chapter 3 in ddOD4T section, early measurements revealed that drop-casted ddOD4T devices can provide appropriate conditions in order to perform KPFM and study electrical properties, as well as the devices prepared by spin-coating as demonstrated in that chapter.

This observation was not applicable for the case of DH4T- and DOTT- based TFTs, since the drop-casted films based on these molecules showed thick crystals limiting the KPFM measurements. on Fig. A.2, A.3, A.4 and Fig. A.5 and A.6, one observes that drop-casted ddOD4T molecules on devices with different channel length and width, exhibit nice morphologies and clear electrical properties. For instance, V_g - and V_d - dependency of the surface potential profiles in the devices under operation is clearly observed. Being able to perform KPFM on drop-casted ddOD4T films may be due to the liquid-crystalline nature of this molecule at RT which allows the formation of a smooth and thin layer.

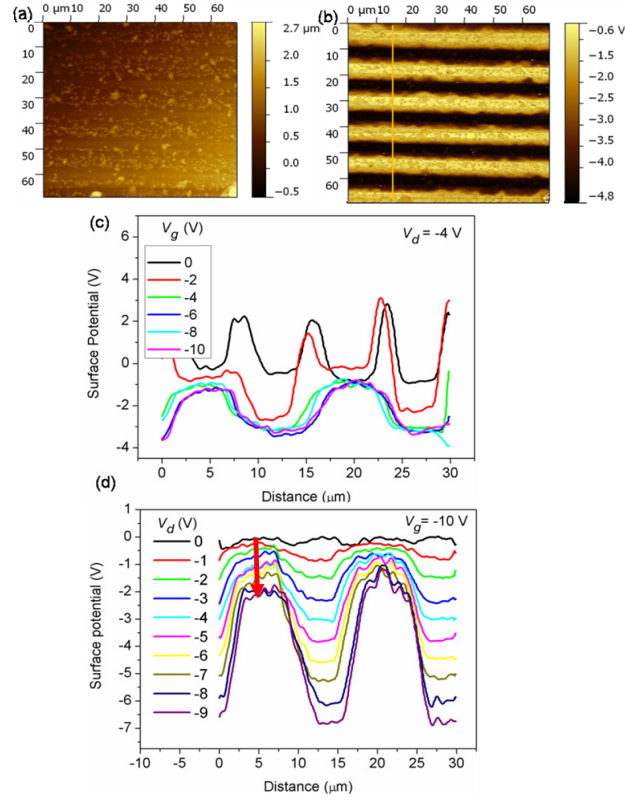


Figure A.2 Potentiometry of drop-casted ddOD4T/C₁₀/SiO₂ thin-film transistor with interdigitated source and drain electrodes ($L = 84 \mu\text{m}$, $W = 16 \text{ mm}$). (a) $70 \times 70 \mu\text{m}^2$ topographic, (b) corresponding surface potential image at $V_d = -6$ V, $V_g = -10$ V; (c) Potential profiles acquired along vertical line shown in (b) as a function of gate voltage, where $V_d = -4$ V. (d) Potential profiles as a function of drain voltage, where $V_g = -10$ V. (The deviation of the source contact surface potential from 0 to negative values, marked by the red arrow, could possibly be due to some contact issues appeared during the measurement.)

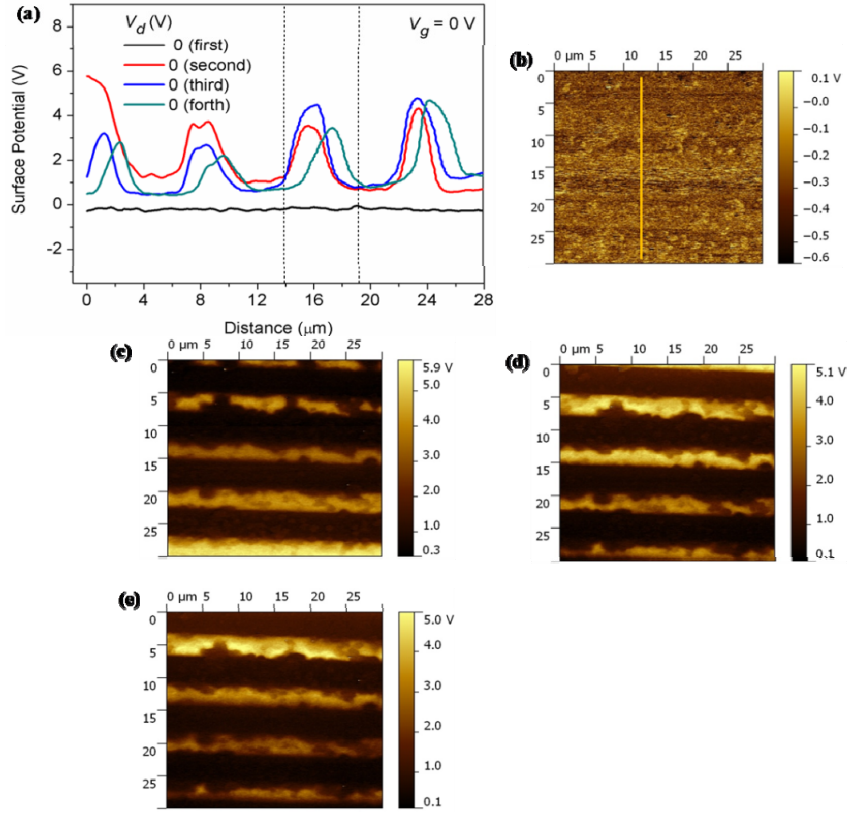


Figure A.3 (a) Surface potential profiles (along line shown in (b)); (b-e) KPFM images obtained on silanized drop-casted OTFT after polarization and switching-off the device. (b) and black): initial off-state; (c) and red): after ramping V_g down to -10 V with $V_d = 0 \text{ V}$; (d) and blue): after ramping V_d down to -10 V with $V_g = -10 \text{ V}$; (e) and green): after ramping V_g down to -10 V with $V_d = -4 \text{ V}$.

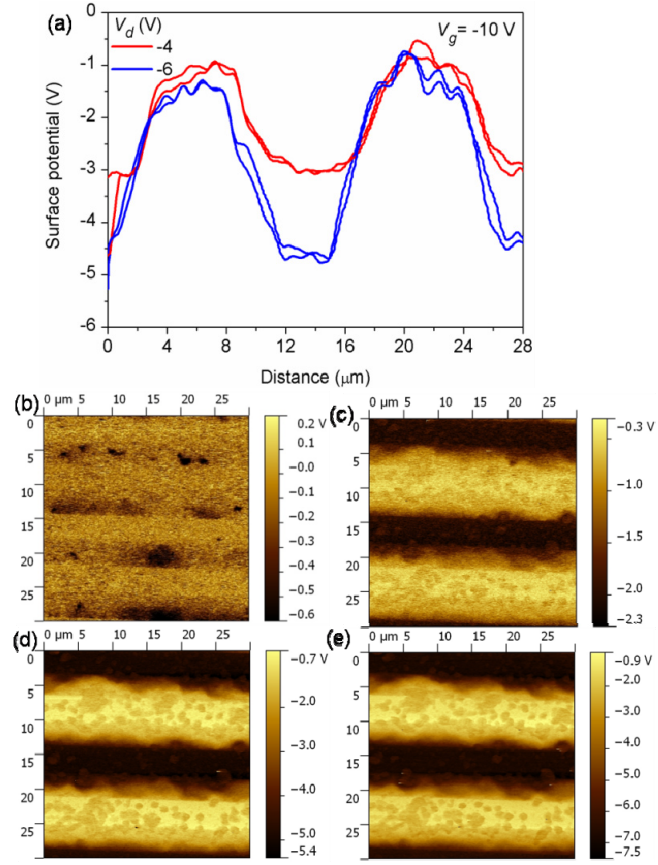


Figure A.4 (a) Hysteresis curves measured at two drain voltages on the silanized OTFT. (b-d) Surface potential images corresponding to $V_g = -10\text{ V}$ and (b) $V_d = 0\text{ V}$, (c) $V_d = -2.5\text{ V}$, (d) $V_d = -6.5\text{ V}$ and (e) $V_d = -9\text{ V}$.

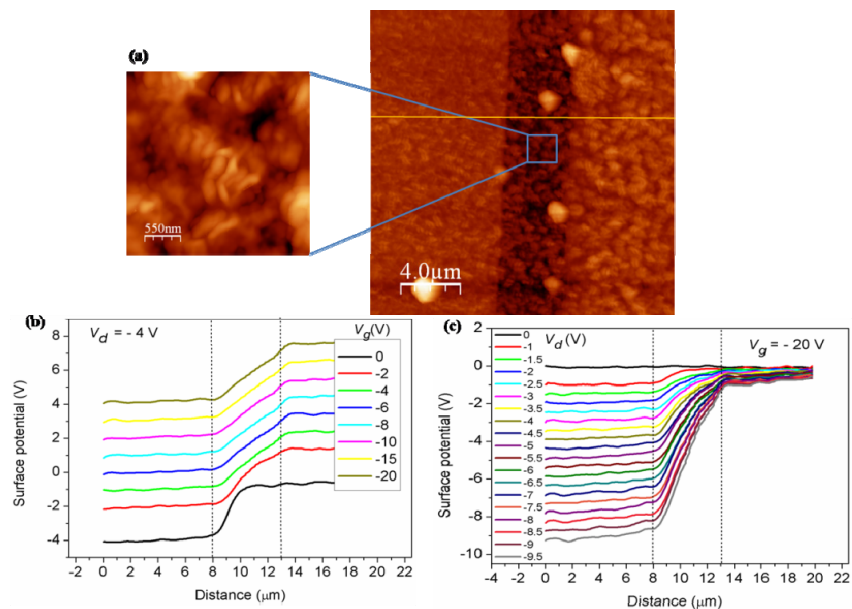


Figure A.5 Potentiometry of drop-casted ddOD4T/SiO₂ thin-film transistor ($L = 5 \mu\text{m}$, $W = 1 \text{ mm}$). (a) $20 \times 20 \mu\text{m}^2$ topographic, (b) Potential profiles acquired along horizontal orange line shown in (a) as a function of gate voltage, where $V_d = -4 \text{ V}$. (c) Potential profiles as a function of drain voltage, where $V_g = -20 \text{ V}$. (The curves in (b) are shifted for clarity.)

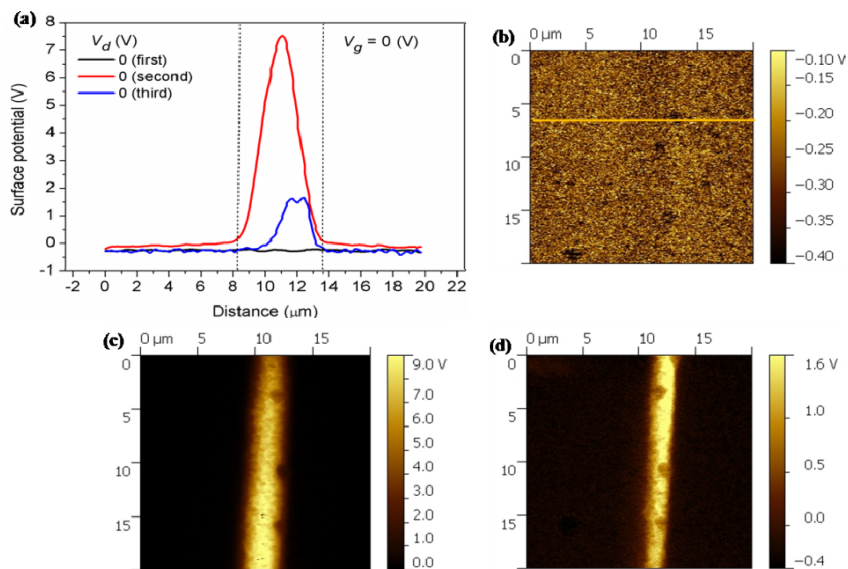


Figure A.6 (a) Surface potential profiles (along line shown in (b)); (b-d) KPFM images obtained on drop-casted OTFT after polarization and switching-off the device. (b) and black: initial off-state; (c) and red: after ramping V_g down to -20 V with $V_d = -4$ V; (d) and blue: after ramping V_d down to -10 V with $V_g = -20$ V.

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