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Extensive Electrical Characterization Methodology of Advanced MOSFETs Towards Analog and RF Applications

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ABSTRACT This *review paper* assesses the main approaches in the electrical characterization of advanced MOSFETs towards their future analog and RF applications. Those approaches are shown to be different from the traditionally used ones for the assessment of the device perspectives for digital applications. Based on the original research realized by our group over the last years, advantages and necessity of those techniques will be demonstrated on different study cases of various advanced MOSFETs, such as Fully Depleted Silicon-on-Insulator (FDSOI), FinFETs and NanoWires (NW) in a wide temperature range (from cryogenic, 4 K up to 250°C). A wide frequency band characterization (from DC up to hundred GHz range) will be positioned as a key element enabling a fair device assessment towards analog and RF applications. Importance of the "extrinsic" parasitic elements in the advanced devices is enormous, sometimes even dominating the device performance. Therefrom arises the need for a proper separate extraction and discussion of "intrinsic" versus "extrinsic" parameters.

INDEX TERMS Analog and RF figures of merit, FDSOI, FinFET, MOSFET, self-heating, S-parameters, UTBB.

I. INTRODUCTION

Enormous progress of the semiconductor technology during the last decades was mainly driven by the continuous demand for the increase of the operation speed and integration density of the complex digital circuits [1]. Another driver of the continuous progress is a demand for the reduction of the power consumption.

Aggressive device downscaling has requested the introduction of novel materials into the gate stack for its equivalent electrical thickness reduction in order to control short channel effects (SCE) while keeping leakage current low, as well as into the channel to boost carrier mobility (μ) and thus on-current and speed [1]. Hf-based dielectrics with equivalent oxide thickness (EOT) of $\sim$1 nm [2] are in use but new high-k dielectrics with k $>$ 30 and EOT down to 0.7 nm are required for further scaling [1] with La silicate appearing as a strong candidate [2]. High-μ channels consist of strained Si [3] or use different crystal orientations [4]. For the next decade, radical change to Ge and III-V materials is under discussion for p- and n-type MOSFETs, respectively. For Si CMOS analog/RF applications, other new materials (e.g., low-k for spacers) and configuration solutions (e.g., faceted Source/Drain [5]) have been introduced to lower parasitics and thus boost analog/RF performance. In addition to novel materials, emerging device architectures come into play. Planar bulk Si MOSFET is no longer considered to maintain SCE control in transistors with a gate length shorter than 14 nm [1].

Instead, two main approaches are now implemented: either 2D ultra-thin fully-depleted (FD) Silicon-on-Insulator (SOI) with ultra-thin buried oxide (BOX), so called UTBB MOSFETs [6]–[8], or 3D multiple-gate (MuG) solution with the gate partly wrapping the 3D channel or fin (i.e., either bulk- or SOI-based FinFETs [9], [10]). Gate-all-around NanoWire (NW) MOSFETs with the gate completely wrapping around the device body is widely discussed as an ultimate device with an excellent electrostatic control for (sub)-5 nm [11]–[14]. Exploitation of 3rd dimension comes as the new horizon, extending the traditional 2D scaling concept, by increasing the number of devices and their current density per μm^3 instead of μm^2. 3D sequential integration (SI) [15] is currently under great exploration. Present trends towards thin active device layers open a way to stack different layers using, e.g., wafer bonding technique. Stacked NWs [16]–[19], Si nanosheets [18], [20], 3D SI CMOS [51], [21]–[23] are widely discussed to boost the device performance.

Technological aspects and "digital perspectives" of these novel devices were widely studied under standard conditions (i.e., static/low-frequency, room temperature and nominal voltages). This, however, is not sufficient, particularly for analog/RF applications, because emerging devices present some particular "defective" behaviors that are strongly temperature and frequency dependent, related to the reproducibility, interface quality, thermal effects, parasitic elements/couplings, etc. Fair scientific benchmarking of emerging devices demands an ability to properly assess device "intrinsic" or inner parameters appropriate to different process or architectural options separately from the "extrinsic" parasitic elements related to, e.g., contacts, technical limitations, etc. Appropriate characterization methodologies to assess the inner device parameters independently of any external influence must be employed to properly explore the physical phenomena in a relation to the main Figures of Merit (FoM) for further applications. In-depth characterization linked to the physical understanding of different phenomena becomes crucial for development of reliable models required by technologists for accurate parameter extraction and process optimization, as well as by circuit designers for a fair prediction of circuit operation and performance.

This article does not target to comparatively assess different advanced MOSFETs, but rather *review* methodological approaches enabling a fair assessment of novel device architectures for their analog and RF performance. Their exploitation will be demonstrated on selected study cases of various advanced devices in wide temperature and frequency ranges, performed in our laboratory over the last years [24]–[78]. In order to be complete, important works of other groups in the domain of device assessment for analog/RF applications are also listed [3], [10], [13], [23], [79]–[94].

The paper is structured as follows: Section II introduces main Analog and RF Figures of Merit (FoM); Section III is devoted to the DC-based characterization techniques; Section IV is about wide frequency band characterization; Section V focuses on the RF characterization, and finally Section VI gives short conclusions. We would like to note that while non-linearity, distortion and noise are also of high importance for the analog/RF applications, their discussion is omitted in this article due to lack of space.

II. ANALOG AND RF FIGURES OF MERIT

Main key-factors of any analog /RF MOSFET are: intrinsic voltage gain (A_{v0}), that varies with frequency (as will be discussed in the following sections):

$$A_v = \frac{g_m}{g_d} = \frac{g_m}{I_d} \cdot V_{EA} \cdot const(f) \tag{1}$$

and cut-off frequencies f_T and f_{max}:

$$f_T \approx \frac{g_m}{2 \cdot \pi * \cdot C_{gs}} \cdot \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right) + (R_s + R_d) \cdot \left(\frac{C_{gd}}{C_{gs}} \cdot (g_m + g_d) + g_d\right)} \tag{2a}$$

$$f_{max} \approx \frac{g_m}{4 \cdot \pi * \cdot C_{gs}} \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d(R_g + R_s) + \frac{1}{2} \cdot \frac{C_{gd}}{C_{gs}}\left(R_s \cdot g_m + \frac{C_{gd}}{C_{gs}}\right)}} \tag{2b}$$

where R_s, R_d are parasitic access source and drain resistances, R_g gate resistance, C_{gd} and C_{gs} are gate-to-drain and gate-to-source capacitances.

These key-factors depend on the device Figures of Merit (FoM), such as: transconductance (g_m), drive/drain current (I_d), output conductance (g_d), Early voltage ($V_{EA} = I_d/g_d$), transconductance over drain current ratio (g_m/I_d), gate capacitance (C_{gg}), etc. Apart from the device geometry and layers' thicknesses, the FoM themselves are directly linked to inner device physics via mobility, short channel effects (SCE), body factor, etc. Furthermore, and particularly for the advanced devices, the above should be completed by parasitic resistive and capacitive elements.

If one considers applications at circuit level (e.g., amplifier), gain bandwidth product, GBW, is considered and, in turn, linked to the same device FoM (g_m/I_d and I_d):

$$GBW = \frac{g_m}{2 \cdot \pi * \cdot C_L} = \frac{g_m}{I_d} \cdot \frac{I_d}{2 \cdot \pi * \cdot C_L} \tag{3}$$

where C_L is the load capacitance.

III. DC-BASED TECHNIQUES (OR TECHNIQUES BASED ON STATIC MEASUREMENTS)

A. G_M/I_D TECHNIQUE

A very useful characterization approach which allows to have a first global appreciation of the device under study for analog application is plotting g_m/I_d as a function of normalized drain current $I_d/(W/L)$ (where W is gate width and L is gate length) [24], [28]. Such plot provides a complete view of the studied device, which is valid for different applications: from low-frequency or base-band, where high gain normalized to current and/or high precision are key FoMs, favoring device operation in weak/moderate inversion, to high-frequency application where high absolute gain is needed and therefore higher drive current is used, favoring

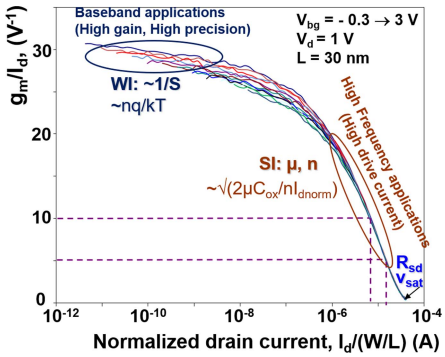

FIGURE 1. g_m/I_d vs. $I_d/(W/L)$ plot for 30 nm-long FDSOI device with different V_{bg}.

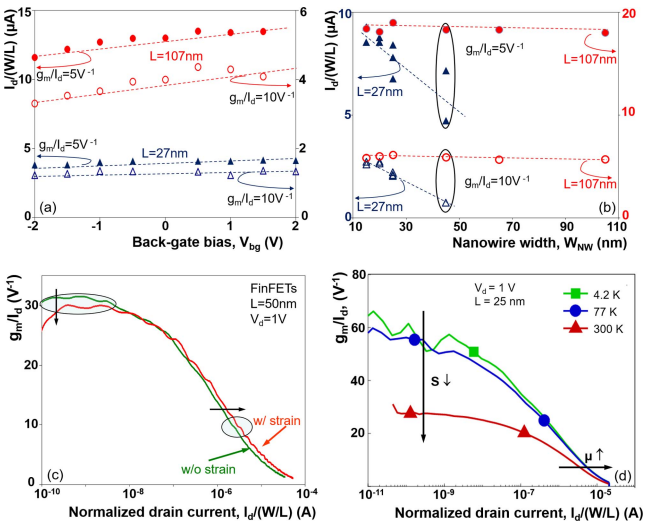

FIGURE 2. (a) Variation of $I_d/(W/L)$ in UTBB SOI MOSFET as a function of V_{bg}. V_d = 1 V [46]. (b) Variation of $I_d/(W/L)$ taken at g_m/I_d = 10 and 5 V^{-1} in NW MOSFETs as a function of NW width. V_d = 1 V [56]. (c) g_m/I_d as a function of $I_d/(W/L)$ in FinFETs with and without strain [58]. (d) g_m/I_d as a function of $I_d/(W/L)$ in FDSOI MOSFET at different temperatures [62], [64].

device operation in stronger inversion (Fig. 1). From a practical point of view, it is worth mentioning that calculating g_m/I_d as $d(\ln I_d)/dV_g$ allows to improve precision and avoid numerical errors, particularly in a range of sharp current change in weak inversion, deep subthreshold regimes.

In weak inversion regime, g_m/I_d is inversely proportional to the subthreshold swing, S. In strong inversion, it is proportional to $\mu \cdot C_{ox}/n$ (where μ is mobility, C_{ox} is gate oxide capacitance and n is body factor). Therefore, g_m/I_d versus $I_d/(W/L)$ plot is independent of threshold voltage, V_{Th}, and of its dependence on substrate/back gate (or body) bias, V_{bg}. To the first order, it is also independent of device geometry (L and W) as long as effects of small dimensions are not significant. In addition to a visual comparative appreciation of different devices in a such plot, we can fix a certain g_m/I_d value (usually = 10 and/or 5 V^{-1}, which corresponds to mid- and strong inversion, respectively, i.e., gate voltage overdrives of 200 to 400 mV typical in analog/RF circuits) and extract the corresponding $I_d/(W/L)$ values as shown in Fig. 1. This allows to link the assessed device performance to the "inner", purely physics-related parameters as μ or body factor, thus providing a fair comparison of devices issued from different technologies, featuring different dimensions and operated at different bias or temperature conditions.

Figure 2 provides some examples of the application of this technique to different devices under different conditions. Fig. 2a shows $I_d/(W/L)$ variation as a function of back-gate bias in UTBB FDSOI MOSFET [46] taken at a fixed g_m/I_d of 10 and 5 V^{-1}. Being extracted in such a way, I_d is free from effect of V_{bg} on V_{Th} and it allows us to directly link the observed improvement of I_d at positive back-gate biases to the mobility improvement. Indeed, negative V_{bg} pushes the channel towards the top Si interface with high-k gate oxide, whereas positive one attracts it towards the bottom Si interface with a SiO_2 BOX, which is less defective than high-k interface so that higher mobility is obtained [36], [46]. Figure 2b gives the example of NWs, plotting $I_d/(W/L)$ extracted at g_m/I_d of 10 and 5 V^{-1} as a function of NW width [56]. One can see that while normalized I_d is almost constant for "long" NW MOSFET, strong improvement is observed with NW width reduction in the case of "short" device. Being free from geometry and V_{Th} effect, this behavior clearly relates to the improved control of short-channel effects in the narrow NWs. It is worth pointing out that these NWs are almost square/Ω-like, with sidewall height of 10 nm that is relatively small compared to the NW width (narrowest device is 17 nm-wide only). Therefore, the usually observed [39], [83], [91] I_d (and g_m) improvement with increase of NW (or Fin) width, related to the mobility improvement when conduction is dominated by the top-plane w.r.t sidewalls, almost does not appear in these devices featuring a complex 3D conduction. More details can be found in [56].

Fig. 2c shows effect of "strain" introduced into the channel of SOI-based FinFETs on g_m/I_d versus $I_d/(W/L)$ curve [58]. One can see that while effect of strain is beneficial in the strong inversion region (due to targeted μ improvement), some degradation is observed in the weak inversion regime (due to weakened SCE control). Therefore, depending on the target application, either high-frequency/high-current, or baseband (high-precision, gain), one would choose device with strain or without, respectively. Finally, Figure 2d demonstrates effect of temperature down to 4.2 K on g_m/I_d versus $I_d/(W/L)$ plot [62], [64]. Temperature lowering is seen beneficial both in weak inversion (due to subthreshold slope improvement) and in strong inversion (due to mobility improvement), and thus for both base-band and high-frequency applications.

Apart usefulness of g_m/I_d technique for linking device performance to the physical background, the g_m/I_d technique has been recently proposed for V_{Th} extraction [41], proving its efficiency and advantages particularly for advanced devices [42]–[44], [75]. This technique extracts V_{Th} as position of extremum of g_m/I_d derivative with respect to V_g,

which was shown to coincide with the position of the extremum of the second derivative of the inversion charge (or surface potential) and thus provides the V_{Th} values linked to the device physics. Furthermore, this method was shown to be robust against mobility variation with V_g [42]; to be applicable in both linear (low V_d) and saturation (i.e., high V_d) regimes [43]; and to provide consistent physics-related values at different temperatures [44] and for different emerging devices as, e.g., Junction-Less (JL) NW FETs [75].

B. G_M – A_V ANALOG METRIC

Another useful approach allowing quick visual assessment of advanced devices for analog/RF applications is the g_m-A_v plot introduced in [46]. In this plot each point represents one device with concrete L and the group of such points for different L forms a trend. For the analog applications one wants both g_m and A_v be as high as possible, i.e., with the points moving to the right and to the top and with a steep trend-line. g_m-A_v metric for analog/RF applications can be seen as analogue to the famous I_{on}-I_{off} plot for digital applications. Using g_m-A_v plot, one can either compare different technologies, or see effect of different biases, temperature conditions, etc.

It is important to note that these plots can be generated either at a bias condition desired for the target applications (and in this case, we assess the suitability of a concrete device/process for concrete application) or at a constant gate voltage overdrive, i.e., V_g-V_{Th} (and in this case, have a link to the device physics). In the latter case, a physical and robust technique for V_{Th} extraction, as, e.g., introduced in previous section g_m/I_d technique [41]–[44], [75], is crucial.

Figure 3 gives a couple of concrete examples of g_m-A_v technique application on advanced MOSFETs. Figure 3a shows effect of NW width with a clear improvement of the device performance both in terms of g_m and A_v in "narrow" NWs comparing to their wide counterpart [56]. This is because of improved control of the SCE and "volume inversion" (i.e., when the whole Si film is inverted) operation regime in the "narrow" device. This improvement was possible to achieve since degrading effects often appearing with NW narrowing, such as, e.g., increased $R_{s/d}$, interface quality and μ reduction, were well tolerated [50]. One can also note the loss of control and performance degradation in short-channels of wide-NW devices. Figure 3b demonstrates effect of temperature on g_m-A_v metric revealing strong device performance improvement with temperature reduction. g_m values are strongly improved thanks to mobility enhancement at cryogenic temperatures, particularly in a "long"-channel devices; slight improvement of A_v is also observed (more details can be found in [56]). Effect of the back-gate bias in UTBB FDSOI is shown in Fig. 3c. It evidences that depending on the target application, one will choose either "negative" (for the high g_m and hence high frequency application) or "positive" (for the high-gain, high-precision applications) back-gate bias [51]. This trade-off derives from competing trends in the g_m and A_v responses

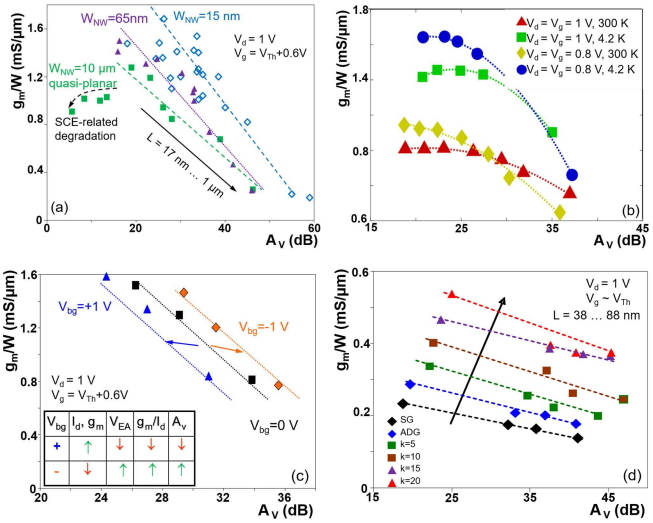

FIGURE 3. g_m - A_V metric application in the case of (a) various NW MOSFETs [56], (b) FDSOI MOSFETs at room and cryogenic temperatures [62], [64]; (c) UTBB SOI MOSFETs at different back-gate biases [57]; (d) UTBB SOI MOSFETs operating in ADG and QDG regimes [49], [50].

to the V_{bg}, e.g., "negative" V_{bg} attracting the channel to the Si/BOX interface and thus assuring higher mobility (as already mentioned above), drives it away from the control of the top gate and thus worsens control of SCE, which in turn results in degraded V_{EA} and A_v. A way to get improvement of both g_m and A_v in UTBB FDSOI devices is to simultaneously bias and sweep the top and bottom gates, as shown in Fig. 3d, in a so-called Asymmetric Double Gate (ADG) with $V_g = V_{bg}$ [48] or Quasi-Double Gate (QDG) [49], [50] with $V_{bg} = k \times V_g$ ($k>1$) regimes. In addition to the V_{Th} modulation, improved I_{on} and I_{off}, exploitable for digital applications, these regimes allow for improved g_m and I_d combined with a lower drain induced barrier lowering (DIBL) and hence higher V_{EA} and A_v, thus potentially exploitable for analog applications.

A last example of g_m-A_v application shows effect of frequency on this metric (Fig. 4) [48]. One can see improvement of g_m and degradation of A_v with frequency increase. The latter occurs because the increase (i.e., degradation) of g_d (see next section) is stronger than that of g_m, thus dominating A_v. Various non-stationary effects, such as floating body, self-heating, substrate coupling, etc. appear in different frequency ranges introducing frequency response (dependence) in g_m, g_d and hence A_v. Therefore, performance prediction based on the DC data only is clearly insufficient (and can be even misleading) for further analog/RF applications, wherefrom a quest for a detailed wide-frequency band characterization is discussed in next section.

IV. WIDE FREQUENCY BAND CHARACTERIZATION

At the beginning of this section, it is directly worth to emphasize that wide-frequency band characterization as well as RF characterization (discussed in Section V) request

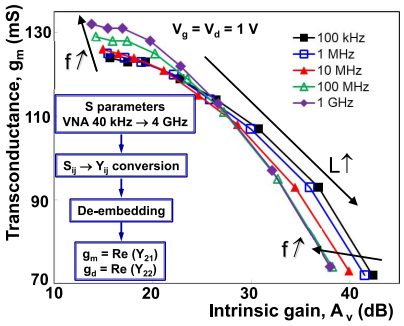

FIGURE 4. g_m-A_V metric in FDSOI MOSFETs extracted at various frequencies [54].

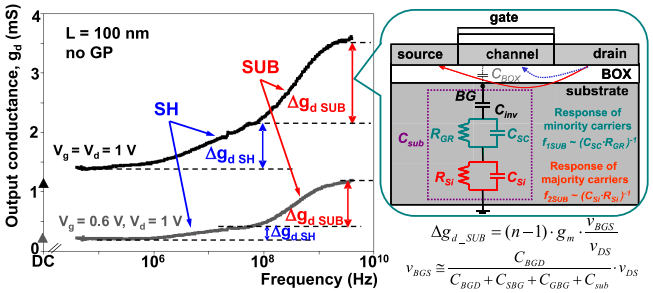

FIGURE 5. Variation of the output conductance versus frequency in UTBB SOI MOSFET [47]. Schematic figure on the right introduce the frequency response of coupling through the substrate.

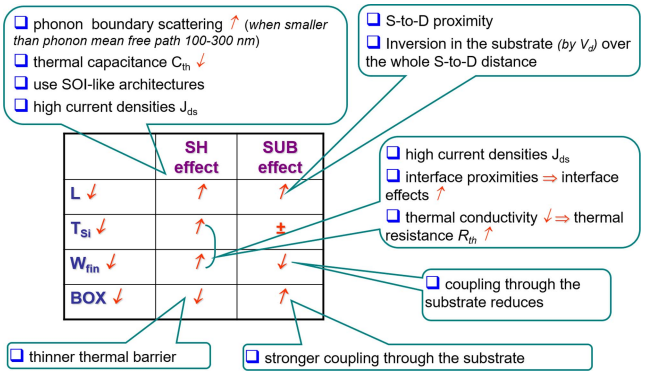

FIGURE 6. Overview of evolution of SH and substrate effects in advanced devices.

the availability of adequate test structures with coplanar waveguide (CPW) RF probe pads. As such characterization techniques open a way not only for performance assessment, but for an in-depth analysis of physical behavior, it is advised to include these specific structures in the layout of test chips, from the very beginning of the technology development.

A. NON-STATIONARY EFFECTS RESPONSE IN A FREQUENCY DOMAIN

The frequency response of the output conductance of the MOSFET can be presented in a following form:

$$g_d(f) = g_{d_{in}} + \Delta g_{d_{FB}}(f) + \Delta g_{d_{SH}}(f) + \Delta g_{d_{SUB}}(f) \quad (4)$$

Various effects contribute to the g_d frequency response: $g_{d,in}$ is an intrinsic term present in any MOSFET, constant with frequency, related to the channel length modulation and DIBL (i.e., corresponds to DC extracted value). $\Delta g_{d,FB}$ is the g_d variation related to the floating body effect. $\Delta g_{d,SH}$ is related to the self-heating (SH) effect; $\Delta g_{d,SUB}$ is related to the frequency response of the coupling through the substrate (or SUB). Other effects can be added. It is worth pointing out that Δg_d terms can have both "positive" or "negative" sign, depending on the device and its operation regime.

Figure 5 provides an example of $g_d(f)$ variation in UTBB FD SOI MOSFET without ground plane (i.e., a highly doped region implemented in the Si substrate just below the BOX to provide a back-gate contact) [47]. In practice, g_d is calculated as the real part of Y_{dd} admittance which in turn is extracted from S-parameters measured in a wide-frequency range after de-embedding [54] (see inset in Fig. 4). Floating-body effects can be to the first order neglected in such thin-film FD devices. However, both SH and SUB related transitions clearly appear in the g_d frequency response. Frequency response of SH (or dynamic SH) effect is well-known to appear because at a certain frequency, acoustic phonons (and hence lattice temperature) cannot follow a.c. excitation. Less-known frequency response of coupling through the substrate, or so-called "substrate effect", is related to the frequency variation of the substrate capacitance, C_{sub}, when, with a frequency increase, first minority (in tens-hundreds Hz range) and then majority carriers (in GHz range) in the substrate stop to follow the a.c. signal and C_{sub} decreases [27]. This can be represented, to the first order, as two RC networks. Variation of C_{sub} results in a variation of potential at Si/BOX interface which translates in a g_d variation (more details can be found in, e.g., [27]).

Figure 6 gives a synthetic overview of SH and SUB effects evolution in advanced devices detailing impact of length scaling, Si film thickness and Fin (or NW) width reduction as well as BOX thinning on these effects. One can see that in advanced deeply scaled devices both effects are strongly exacerbated. Moreover, trade-off between SH and SUB effects exist as, e.g., fin width reduction enhances SH but reduces coupling through the substrate and thus depending on the application and bias conditions one or another architectural solution can be preferential.

Figure 5 evidences a strong, 2-to-5-fold, degradation of g_d over a frequency range, which is an important bottleneck for analog applications and designers. Next to that, it is worth emphasizing that in the thin FDSOI devices with a thin BOX which did not incorporate ground plane, SUB-related transition was as strong as SH one, and at a certain regime (e.g., at lower V_g) even stronger than SH one (Fig. 5) [47]. This is because BOX thinning eases heat evacuation towards Si substrate, whereas it enhances the electrical coupling through the substrate.

From the example given in Fig. 7 one can see that the introduction of a Ground Plane (i.e., highly doped layer in the Si substrate, just underneath the BOX) allows for a strong

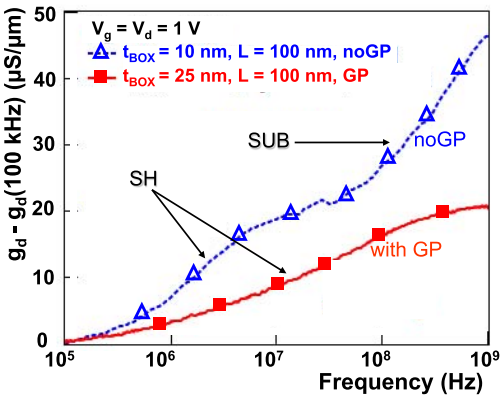

FIGURE 7. Output conductance as a function of frequency in FDSOI MOSFETs with and without ground plane [47], [54].

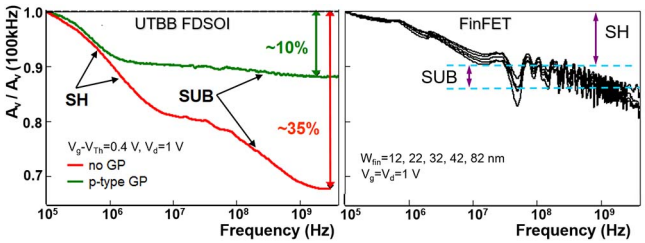

FIGURE 8. Normalized intrinsic gain as a function of frequency in UTBB FDSOI MOSFETs [45] and FinFETs [76].

reduction of the SUB-related variation of g_d [45], [54]. Thus, SH stays the main reason of analog performance degradation in advanced devices, being in UTBB FDSOI [45] or SOI-based FinFETs [76] (Fig. 8), at high bias voltage and current, i.e., power density and hence Joule heating dissipated in the device. In order to reduce SH effect, beyond using lower biases, different solutions as, e.g., optimization of device geometry, further oxide thinning, use of high thermal conductivity materials, etc. can be envisaged. Furthermore, use of a sink implemented in the back end of line (BEOL) was recently demonstrated to allow for a 20-30% improvement of SH features [74], giving additional freedom for the circuit designer optimization without the need of technological process modification.

B. SELF-HEATING ASSESSMENT

However, SH-related g_d variation in a frequency range can be seen not only as a drawback for analog design but also as a tool for extraction of SH features: thermal resistance, R_{th} and temperature rise in a channel, ΔT. Knowing the amplitude of the SH-transition, $\Delta g_{d,SH}$, low-frequency values of g_d value and temperature dependence of the drain current (dI_d/dT_a, where T_a is ambient temperature, obtained from complementary measurements), R_{th} can be extracted as:

$$R_{th} = \frac{\Delta g_{d\_SH}}{(I_d + g_{LF} \cdot V_d) \cdot dI_d/dT_a} \tag{5a}$$

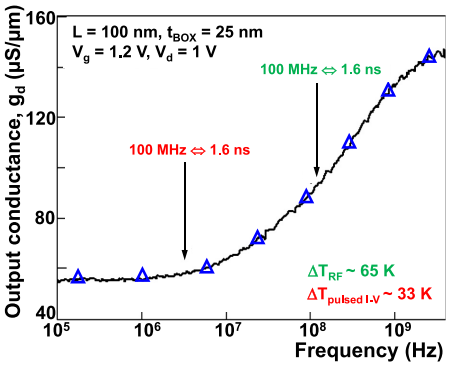

FIGURE 9. Output conductance as a function of frequency in UTBB FDSOI devices. Arrows indicate a frequency range at which RF and pulsed I-V techniques were applied for SH extraction [59].

Knowing R_{th}, channel temperature rise is then easily calculated:

$$\Delta T = R_{th} \cdot I_d \cdot V_d \tag{5b}$$

While basics of this technique were introduced a long time ago [79], its advantages become further pronounced particularly for the advanced devices, with a strongly decreased volume-to-surface ratio. This is because thermal resistance is inversely proportional to the heat evacuation surface, while thermal capacitance C_{th} is proportional to the volume available to store the heat and thus characteristic frequency f_{th} ($= 1/(2.\pi.R_{th}.C_{th})$ is inversely proportional to the volume-to-surface ratio and shifts towards higher frequencies in advanced device architectures. An example given in Fig. 9 shows that the f_{th} can reach the hundreds of MHz range in advanced FDSOI MOSFET. Alternative pulsed I-V technique widely used for the SH extraction (based on the application of the short pulses to avoid device heat) fails in this range of characteristic frequencies (or time constants). Presently, to the best authors knowledge, there is no technical solution allowing on-wafer realization of the pulse technique with well controllable pulses in the $\sim$ 1 ns range. As indicated in Fig. 9, pulsed I-V technique may strongly underestimate SH in advanced devices [59], [68]. Furthermore, this underestimation or inconsistency will be dependent on the studied device architecture, dimensions, bias and temperature conditions. For example, benchmarking of bulk and FDSOI devices in view of SH features may be wrong even in relative values, because characteristic SH frequency is lower in bulk devices (about an order of magnitude [59]) and thus pulse I-V technique can provide lesser underestimated values.

Figure 10 gives an example of comparative assessment of FDSOI vs bulk devices from the same 28 nm technology node in a wide frequency range [59]. In spite of a stronger self-heating in the FDSOI devices (Fig. 10a), they outperform the bulk counterpart (Fig. 10b) in the entire frequency range. It is worth pointing out that only wide frequency range allowed in this case a fair benchmarking: as can be seen in Fig. 10b, the improvement provided by FDSOI devices

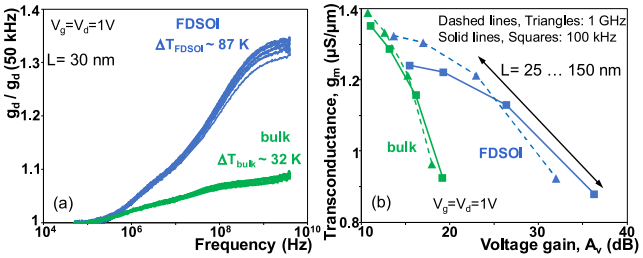

FIGURE 10. **(a) Normalized output conductance as a function of frequency in FDSOI and bulk MOSFETs. L = 30 nm. (b) g_m-A_v metric in bulk and FDSOI MOSFETs extracted at low and high frequency. L = 25 to 150 nm [59].**

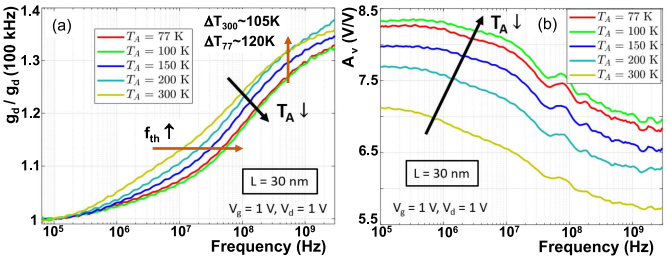

FIGURE 11. **Normalized output conductance(a) and intrinsic gain (b) as a function of frequency in FDSOI MOSFETs at different temperatures [65].**

estimated from low-frequency values (squares) is larger than that extracted from high-frequency values (triangles).

Figure 11 gives an example of wide-frequency band assessment of analog FoM with temperature reduction down to 77 K. The overall increase of analog FoM (g_m, g_d, A_v) with temperature lowering extracted from DC measurements (shown in Figs. 2 and 3) stays valid in a wide frequency range. Moreover, SH-induced degradation of analog FoM is slightly attenuated at cryogenic temperatures [65]. Thermal time constant is further reduced with temperature lowering and thus wide-frequency technique (we often cite it as "RF technique", because it requires measurements up to GHz range) for SH features extraction becomes even more relevant. It is worth to emphasize that the channel temperature is particularly different from the ambient one at cryogenic temperatures, which is crucial for modeling.

It should be pointed out that SH assessment based on equations 5, while allowing the extraction of main features, is a simplified approach. It models SH by a simple R_{th}, C_{th} thermal network. However, in real device, different heat evacuation paths co-exist (via BOX, via gate, via source/drain and vias, . . .) and thus a higher order thermal network needs to be involved for more advanced and accurate thermal representation and modeling. Detailed investigation of thermal behavior would request for a combination of experiments with simulations and modeling to allow the extraction of different R_{th}, C_{th} components related to each path. This would also request for detailed information about BEOL (back end of line) architecture (layers, thicknesses, etc.), as well as to include die-level or package-level boundary conditions. More detailed discussion is however, out of scope of this article.

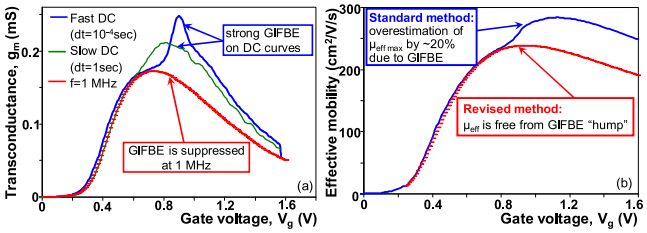

FIGURE 12. **(a) g_m-V_g curves of wide-fin FinFET (i.e., analog of PD SOI) measured at DC with short, 1 s (blue line) and long, 10 s, (green line) delay times and HF of 1 MHz (red dashes). L = 2 μm. V_d = 50 mV. (b) Effective mobility in this device extracted using standard and revised split C-V technique [38].**

C. PARAMETERS EXTRACTION

Ability to extract main device parameters, such as, e.g., threshold voltage, mobility, etc. which are "free" from the non-stationary effect is very important for the development of fair predictive models. Wide-band frequency measurements allow such possibility. Fig. 12 gives an example of the mobility extraction in partially-depleted SOI MOSFETs strongly affected by gate-induced floating body effect (GIFBE) [92] (or linear kink effect [93]) which appears as a jump in the transconductance curve, thus disturbing correct mobility extraction using standard techniques (either from maximum of g_m, or Y-function, or split C-V). Wide-band frequency characterization revealed that GIFBE effect features a characteristic frequency response with a cutoff frequency in the range of hundred kHz [78]. Figure 12a shows that in g_m extracted from a 1 MHz S-parameters measurement, this effect is suppressed. Therefrom modified split C-V technique [38] which uses integrals of g_m (instead of DC I_d in a traditional split C-V) and capacitance measured at very high frequency was proposed:

$$\mu = \frac{L^2}{V_d} \cdot \frac{\int_{V_0}^{V_g} G_m(V_g) dV_g + I_{d0}}{\int_{V_0}^{V_g} C_{gc}(V_g) dV_g} \tag{6}$$

Figure 12b demonstrates the advantages of the application of this revised technique w.r.t "standard" one in terms of the reliable values extraction: smooth mobility curve, without "overestimation" related to GIFBE is extracted.

This approach can be generalized and successfully applied to extraction of main MOSFET parameters unaffected by the non-stationary effects.

V. RF CHARACTERIZATION

When device length is scaled down, importance of parasitic components increases enormously. As we will see later in this section, parasitic elements can even dominate the device performance. This is particularly the case for advanced device architectures with thin-film, 3D geometry (as FinFETs and NWs) or stacked devices. As already mentioned in Section II, different parasitic components (Fig. 13a), as parasitic access resistances and various parasitic coupling capacitances (vulgarized in Fig. 13b along

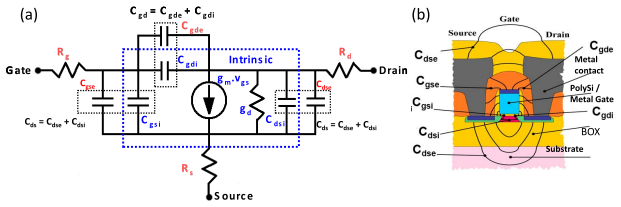

FIGURE 13. **(a) MOSFET small-signal equivalent circuit including parasitic and intrinsic components; (b) schematic representation of different parasitic capacitive coupling components.**

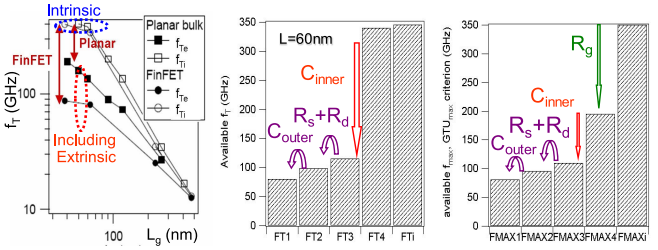

FIGURE 14. **Variation of the cutoff frequency as a function of length in FinFET and planar counterparts along with analysis of effect of different parasitic elements on the FinFET cut-off frequencies [35].**

with intrinsic capacitance components) affect the device perspectives for analog/RF applications. In advanced present technologies, the ability to separately extract "intrinsic" and "extrinsic" elements becomes crucial, because: (i) it allows to predict "intrinsically" achievable (or idealistic) device/process values, i.e., the limit one can reach with full optimization of parasitic elements; (ii) for the process/architecture optimization, it is crucial to know whether the deficiency in the performance originates from the "intrinsic device" (and thus one needs to work on optimization of interfaces, channel, μ, gate stack, etc.) or from "extrinsic parasitics" (and thus, the focus of optimization would be on spacers, access resistances, etc.). Extraction of a complete equivalent circuit (including and separating "intrinsic" and "extrinsic" components) demands S-parameters measurement in a wide frequency range up to a hundred GHz. Hence, adequate structures with RF access pads must be included in the layout from the very start of the technology development. Detailed procedure for the extraction of "intrinsic" and "extrinsic" elements of the equivalent circuit shown in Fig. 13 can be found in [61], [77]. Due to the limited space we do not provide it in this article.

Figure 14 exemplifies the above discussion in the case of FinFETs and their planar bulk counterpart [35]. "As measured" (i.e., including extrinsic parasitics) and "intrinsic" (i.e., after withdrawing of parasitic elements) values are shown. Firstly, difference between "intrinsic" and "as measured" values increases with device length reduction and is further enhanced in FinFETs w.r.t bulk counterpart. Secondly, it is interesting to point out that very similar "intrinsic" values are achievable in the case of planar and FinFET devices, whereas measurable values (i.e., those which include both intrinsic and extrinsic elements) are much lower in FinFETs comparing with the planar counterparts. Detailing various parasitic components, it was concluded that apart from the effect of R_g on f_{max}, the major degradation comes from C_{inner}, which is the sum of fringing capacitances directly linked to the FinFET 3D architecture, contributing to ∼60% of f_T and 30% of f_{max} degradation (w.r.t intrinsically achievable values). Effects from $R_{s,d}$ and C_{outer} (related to the feed connection outside the active area) were relatively small in these devices. The largest part of C_{inner} was shown to be due to the 3D coupling between source/drain side walls and the gate wrapping the fin, with some architectural optimization proposed in [76].

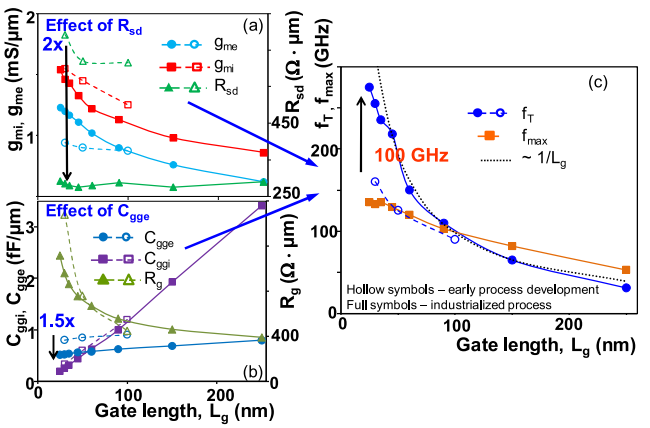

FIGURE 15. **Gate length dependence of R_{sd}, g_m, intrinsic g_m (a), R_g, extrinsic and intrinsic C_{gg} (b) and f_T, f_{max} (c) in different "generations" of FDSOI MOSFETs [55], [61].**

Figure 15 gives an example of the effect of parasitic elements on the RF performance of UTBB FD SOI devices. In this figure we show both early-stage UTBB FDSOI technology development at Leti [55] and its more mature industrial version at ST-Microelectronics [6], known as 28FDSOI [61]. One can see a strong role of parasitic elements on the device performance, particularly in "shorter" devices. Series resistance being almost constant versus L, has, nevertheless, naturally stronger impact on the g_m of shorter-L devices. Extrinsic parasitic capacitance, $C_{gg,e}$, also stays almost the same for different gate lengths, so that at it becomes higher than intrinsic component (which scales proportionally to L) and thus dominates in the total C_{gg} (Fig. 15b).

Figure 15 shows that process optimization allowed for an improvement (reduction) of both capacitive and resistive parasitic components: R_{sd} is about twice lower and $C_{gg,e}$ is 1.5 times lower in the case of the more mature version. Such reduction of parasitics results in a strong improvement of RF performance with f_T increase of ∼100 GHz. Recently, f_T values as high as 360 GHz for 30 nm-long device [69], compatible with ITRS requirements for low-power applications, were reported achievable in this technology with further device/process optimization.

Figure 16 gives another example case, namely RF performance evolution in the cryogenic temperature range, when separate extraction was important for the proper device

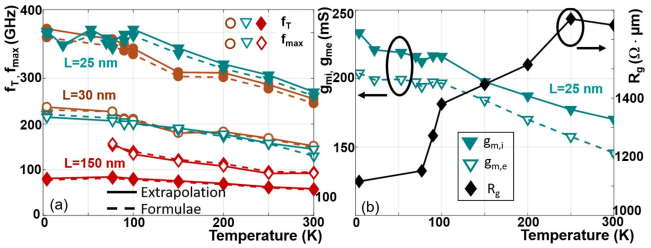

FIGURE 16. Temperature dependence of f_T, f_{max} (a) and R_g, intrinsic and extrinsic g_m (b) in FDSOI MOSFETs [64].

modeling [64]. Strong improvement of RF FoMs (∼130 and 75 GHz for f_T and f_{max}, respectively, for 25 nm-long FDSOI device) is evident with temperature reduction (Fig. 16a). This improvement was detailed to be related mainly to the mobility, and hence intrinsic g_m increase (∼40%) and additionally for f_{max} due to the R_g reduction, whereas other parasitic elements exhibited only slight temperature dependence (Fig. 16b).

VI. CONCLUSION

This article reviewed the appropriate characterization techniques and methodologies that allow fair analysis and benchmarking of advanced devices linked to the device physics and operation conditions. Wide frequency band analysis was pointed out as a key element for the fair assessment of different devices and understanding of physical phenonema impacting their behavior and performance. Separation of "intrinsic" and "extrinsic" parasitic elements and related performance impacts was emphasized to be mandatory in downscaled devices with advanced architectures, to guide both device/process optimization and parameter extraction for modeling.

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