Effect of PN Passivation on MOSFETs Performance in 28 nm FD-SOI

M. Vanbrabant[1*], M. Rack[1], A. Cathelin[2], J.-P. Raskin[1], V. Kilchytska[1]
[1]*Université catholique de Louvain, Louvain-la-Neuve, Belgium*
[2]*STMicroelectronics, Crolles, France*
[*]martin.vanbrabant@uclouvain.be

***Abstract*— This work investigates, for the first time, how the PN passivation introduced in the fully depleted silicon-on-insulator (FD-SOI) substrate below the buried oxide (BOX) to improve substrate performance for RF applications in 28 nm FD-SOI technology affects active MOSFET parameters. DC performance and low-frequency noise (LFN) of MOSFETs are studied for different substrate resistivities and implant parameters. It is demonstrated that PN passivation impacts the device performance via modification of the back-gate realization.**

Keywords- FD-SOI, interface passivation, MOSFET, substrate resistivity.

I. INTRODUCTION

Nowadays, fully-depleted silicon-on-insulator (FD-SOI) technology is a competitive platform for radio-frequency (RF) and mm-wave applications thanks to its high cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) metrics in the range of 300 to 400 GHz [1], [2] and its rich back-end-of-line options with up to 10 metal layers, including several thick layers supporting high-Q RF/mm-wave passives and interconnects. The silicon substrate becomes part of the electromagnetic environment of these passive devices and can thus be responsible for significant losses, coupling and non-linearities if the substrate resistivity is low [3]. By replacing standard resistivity substrates (with nominal resistivity ρ_{nom} = ~10 Ωcm) by high-resistivity (HR) substrates (ρ_{nom} > 1 kΩcm), these effects can be partially mitigated, though the improvements are hindered by the parasitic surface conduction (PSC) effect [4]. The *PN interface passivation* technique has then been recently developed to counter the PSC layer as an alternative solution compatible with FD-SOI process, unlike well-known *trap-rich passivation* [5]. It was first introduced in [6] showing improved *effective resistivity* of the substrate thanks to the depletion junctions between the doped P- and N-type regions locally interrupting the conductive interface and thus resulting in a strong increase in overall substrate impedance. This solution was then applied to the industrial 28 nm FD-SOI process from STMicroelectronics [7]. Assessing the RF performance of the passive elements, the optimal implant parameters/ substrates were found. Indeed, the industrially available standard 28 nm FD-SOI process, which employs standard resistivity substrate of around 10 Ωcm and usual implant parameters (for the back gate and well formation) was first characterized in terms of losses, effective resistivity (ρ_{eff}) and generated harmonics through on-wafer measurements of coplanar waveguides (CPW). Then, usual implants and several split runs with modified implant energies and doses targeting the optimal interface passivation process were considered on HR wafers (not commercial technology yet) and benchmarked against the process of reference wafer, giving insight into the critical parameters involved in this solution.

Complex RF circuits (e.g. voltage-controlled oscillator [8] and RF switches [9]) were finally developed to explore the impact of the silicon substrate resistivity on the circuit performance, which does not depend only on passive devices (e.g inductors/transformers for matching) but also on active devices. For example, in LNA design, multiple amplification stages are often used to boost the gain with several inductors/transformers for matching or trade-off gain for bandwidth [10]. Therefore, it is then crucial to evaluate the quality of each component, both passive and active one, individually to propose state of the art circuit designs.

In this work, the impact of these implant/substrate variations, originally aiming at improving passives RF performance, is investigated on active devices performance and more specifically on (i) I_d-V_{gs} characteristics, (ii) analog figures of merit and (iii) low-frequency noise behavior.

II. DEVICE DETAILS AND EXPERIMENTAL SETUP

The device used in this study is an FD-SOI low threshold voltage (LVT) nMOSFET (Fig.1) from 28 nm FD-SOI technology of STMicroelectronics featuring a gate length of 30 nm, finger width of 1 µm and 64 fingers for a total width of 64 µm (layout dimensions). This device was tape-out on standard (Std) and high-resistivity (HR) wafers with variations in the implant conditions. It is important to note that N/P-type implantation used for n-well/back-gate realization in active nFET is the same as the one used for N/P-type implantation of PN junctions under passive devices as shown in Fig. 1. Wafers description is summarized in Table I and more details about their respective RF performance (i.e. losses, effective resistivity and harmonic distortion levels) are

available in [7]. "Ref." refers to the usual implants (n- and p-wells) in the standard fabrication process which does not target PN passivation while split 1 and split 2 refer to implant variations (in energy and doses) from the usual implant conditions. In [7], W09 was identified as the one having the highest effective resistivity (540 Ωcm) among all wafers, i.e. the best one from the passives RF performance.

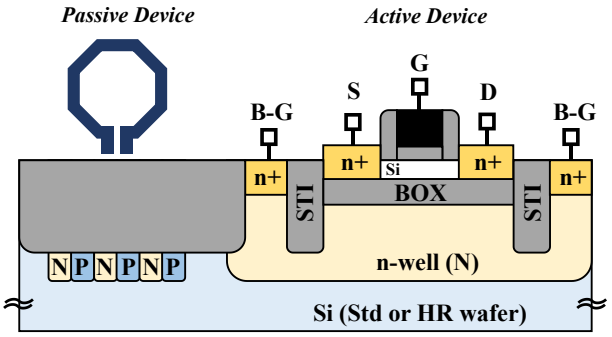

Fig. 1. Schematic (not to scale) of an LVT nFETs side by side with a passive device implemented on top of a silicon substrate with PN interface passivation solution.

TABLE I WAFERS DESCRIPTION

Wafer ID	Substrate	Implants
W01	HR	Split 1
W09	HR	Split 2
W15	HR	Ref.
W23	Std	Ref.

Both DC and LFN characterization were performed using a Keysight Advanced Low-Frequency Noise Analyzer (ALFNA) with Keysight B1500 semiconductor analyzer. To minimize external noise sources, measurements were done in a shielded probe station (MPI TS-3000). The chuck temperature was set to 25 °C for the whole measurement campaign.

III. RESULTS AND DISCUSSION

In this section, the key electrical parameters of an LVT nFET from 28 nm FD-SOI technology are studied for different substrate resistivities (i.e. Std and HR) and implant parameters. First, the impact of these changes is evidenced on I_d-V_{gs} characteristics. Analog figures of merit (FoM) are then computed and analyzed. Finally, low-frequency noise characterization is conducted on the same devices.

Measurements presented in this section were done on three dies or more (depending on the wafer, not shown) to confirm the observed trends.

A. DC Characteristics

Fig. 2 shows I_d-V_{gs} characteristics in a linear regime for different wafer splits. For reference implants, moving from Std wafer (W23) to HR wafer (W15) does not affect IV curves. However, modifications of implants (W01|W09) result in an increase of the subthreshold slope (SS) from 82 mV/dec (W15|W23) to 89 mV/dec and a threshold voltage shift ΔV_{th} of 27 mV. The threshold voltage is computed using the second-order derivative method [11], [12]. Fig. 3 shows the transconductance g_m (computed as $\partial I_d/\partial V_{gs}$) as a function of V_{gs} in linear regime with a maximum around 14 mS for all wafers.

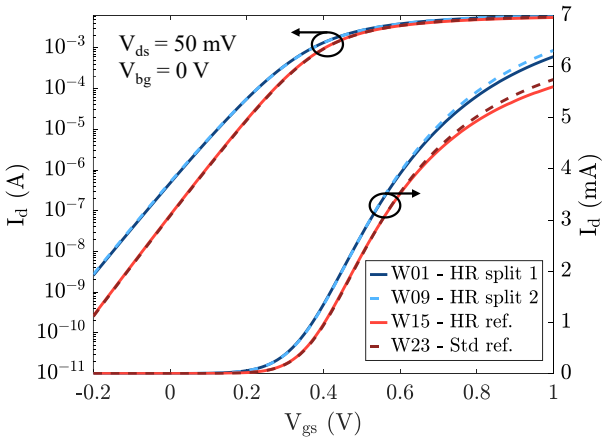

Fig. 2. I_d-V_{gs} characteristics in linear regime (V_{ds} = 50 mV) for different wafers.

In addition, V_{th} tunability with the back-gate voltage V_{bg} of split implants wafers (W01|W09) is reduced compared to "ref." implants wafers (W15|W23) as shown in Fig. 4. W01 is particularly impacted, most probably due to lower energy and doses of implants making it more subjected to substrate depletion effect [13], [14]. Indeed, in the coupling theory devised by Lim and Fossum [15], the threshold voltage rate of change with the back-gate voltage is given by

$$\Delta V_{th}/\Delta V_{bg} = -\frac{C_{si}C_{box}}{C_{ox}\left(C_{si}+C_{box}+C_{it,b}\right)} \approx -\frac{t_{ox}}{t_{box}} \quad (1)$$

Where $C_{si} = \varepsilon_{si}/t_{si}$ is the capacitance of the depleted film, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance, $C_{box} = \varepsilon_{ox}/t_{ox}$ is the BOX capacitance and $C_{it,b} = qD_{it,b}$ is the trap capacitance of the back interface. The final simplification is acceptable as the film/body capacitance is much higher than the BOX capacitance and the back-interface trap capacitance is usually low due to the high-quality silicon film/BOX interface.

At negative back-gate biases (when the BOX-nwell interface is accumulated), all wafers present similar ΔVth/ΔVbg. However, at slightly positive Vbg (i.e. ~ 1 V), the Vth tunability of the splits (W01 and W09) starts to degrade, most probably due to a depletion region forming underneath the BOX. Indeed, in the case of thin BOX and lightly doped well, a depletion region can form underneath the BOX, making the "equivalent" BOX capacitance (depletion capacitance in series with C_{box}) much lower which results in a thicker equivalent BOX ($t_{box,eq} > t_{box}$). This translates into a lower V_{th} tunability with V_{bg} as $\Delta V_{th}/\Delta V_{bg} = t_{ox}/t_{box,eq}$ is lower than Eq. 1. More complex model taking into account the BOX/well interface was developed in [16].

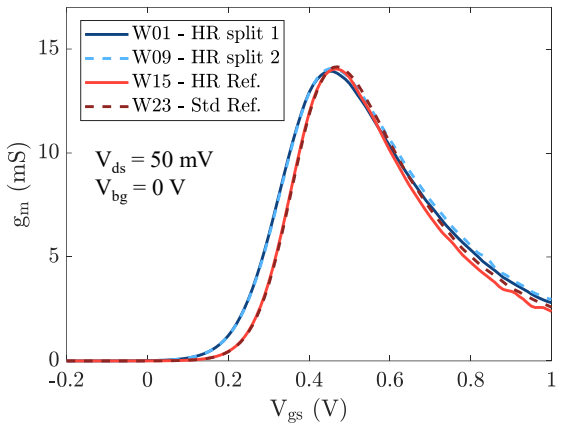

Fig. 3. g_m-V_{gs} characteristics in linear regime (V_{ds} = 50 mV) for different wafers.

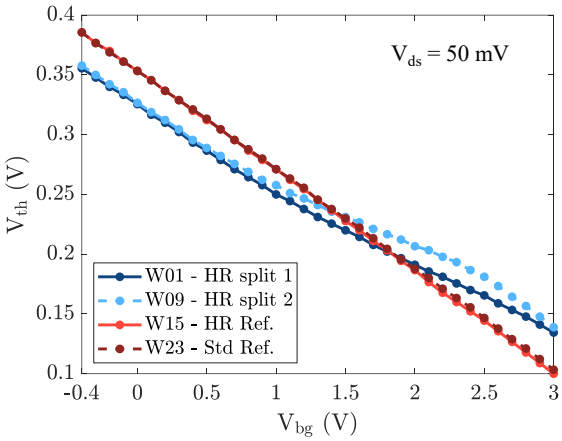

Fig. 4. Threshold voltage V_{th} vs back-gate voltage V_{bg} extracted in linear regime (V_{ds} = 50 mV) for different wafers.

B. Analog Figures of Merit (FoM)

From analog figures of merit perspective, the maximum g_m/I_d, key FoM for baseband (high-gain, high-precision) applications, decreases by 7.1% for split runs (W01|W09) with respect to "ref" ones (Fig. 5) which agrees with SS trends. For high-frequency applications where high current is required, I_d at g_m/I_d = 5 V^{-1} is increased by more than 0.3 mA for W01|W09 (Fig. 6a) while a reduction of I_d at g_m/I_d = 10 V^{-1} (around 0.5 mA) is observed for the same wafers (Fig. 6b).

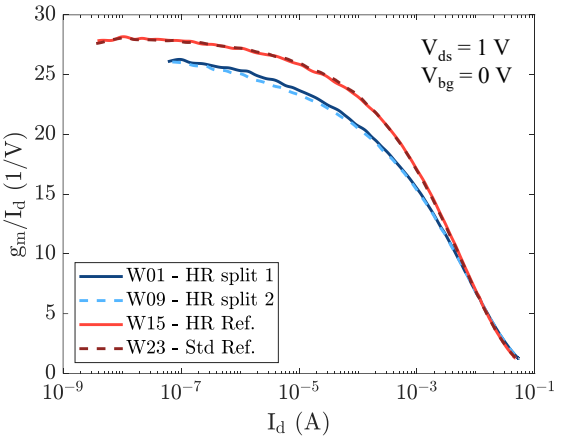

Fig. 5. g_m/I_d vs I_d at V_{ds} = 1 V for different wafers.

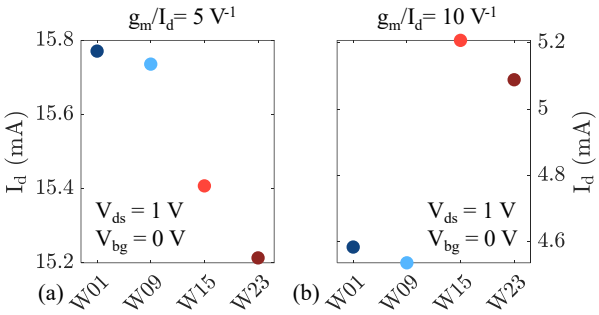

Fig. 6. I_d at (a) g_m/I_d = 5 V^{-1} and (b) g_m/I_d = 10 V^{-1} for different wafers at V_{ds} = 1 V.

Another key analog FoM of MOSFETs is the intrinsic voltage gain A_v which can be computed as the ratio between the transconductance g_m and the output conductance g_d: $A_v = g_m/g_d$. By plotting g_m vs A_v, one can quickly assess device performance under different biases or temperature conditions [17] where both g_m and A_v are desired to be as high as possible (i.e. upper right corner of the plot).

While the transconductance g_m is a bit higher for split wafers biased in saturation, their intrinsic voltage gain A_v is however lower compared to the one of "ref." implants wafers (1-2 dB) as shown in Fig. 7.

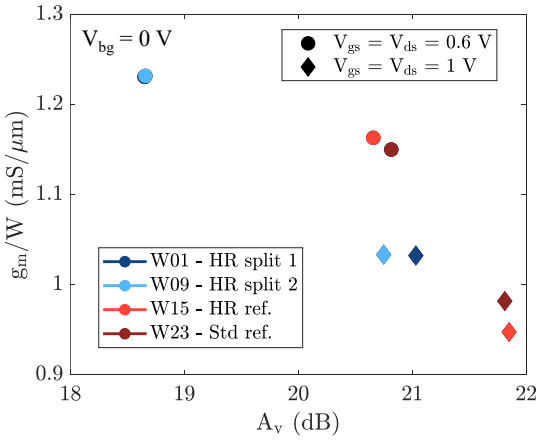

Fig. 7. g_m/W vs A_v at different V_{ds} = V_{gs} for different wafers.

C. LFN Characteristics

Fig. 8 exemplifies the noise power spectral density (PSD) S_{Id} at different fixed I_d for W23. Fig. 9 shows the normalized PSD S_{Id}/I_d^2 vs I_d at 10 Hz for different wafers. It is important to note that for both "ref." implants wafers PSD is seen to be proportional to their corresponding $(g_m/I_d)^2$, suggesting dominance of carrier number fluctuations (CNF) mechanism [18]. For split wafers W01|09, PSD follows the $(g_m/I_d)^2$ in a strong inversion regime, however, it starts to deviate from it in a weak inversion suggesting combination of different mechanisms.

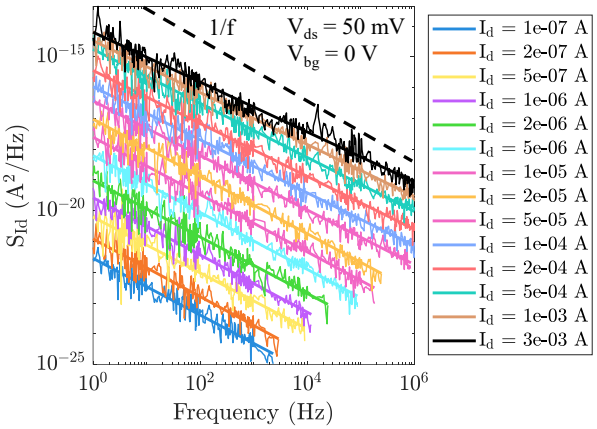

Fig. 8. Current noise power spectral density S_{Id} vs frequency at different fixed I_d for W23.

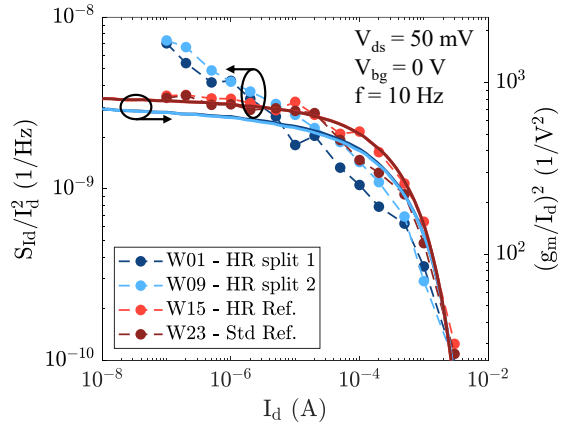

Fig. 9. Variation of normalized drain current noise S_{Id}/I_d^2 vs I_d at 10 Hz for different wafers.

IV. Conclusion

In this paper, the impact of substrate/implant variations, which was originally intended for the optimization of PN interface passivation in order to achieve good substrate RF performance, was investigated on the FD-SOI nFETs' performance. It was shown that changes in the back-gate implantation does not seriously alter the performance of the active MOSFETs. While the split runs presented slightly lower threshold voltage tunability with back-gate voltage compared to usual implant wafers, this crucial feature of FD-SOI technology is still working properly. Split wafers exhibited higher g_m (< 10 %) at the cost of a few dB lower voltage gain A_v compared to usual implant wafers, which could be favourable for the splits depending on the application. Observed changes are suggested to be mainly related to modification of the back-gate implant parameters and not to the substrate resistivity.

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