Enhanced High-Resistivity Silicon-Based Substrates for RF and mmWave FD-SOI Circuits

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Abstract

This thesis delves into the intricate advancements in mobile phone technology, where the integration of cutting-edge components such as front-end modules (FEM), RF transceivers, and systems on chips (SoCs) is critical for handling the complex demands of modern communication. These technologies ensure that mobile devices can efficiently manage and transmit signals across multiple frequency bands, while also optimizing power consumption and supporting a wide range of advanced applications.

A key focus is the role of CMOS technology, particularly the silicon substrate that not only provides mechanical support for integrated circuits but also plays a pivotal role in the electromagnetic environment surrounding RF components. The substrate's electrical properties, including permittivity and conductivity, significantly affect RF circuit performance, influencing factors like signal propagation and crosstalk. Therefore, understanding and optimizing the substrate is crucial for achieving high-performance outcomes in RF systems.

Over the past two decades, silicon-on-insulator (SOI) technology has seen remarkable progress, especially in developing substrates aimed at minimizing losses and enhancing linearity. Among these, the polysilicon trap-rich eSI™ substrate has become a cornerstone in mobile technology, used in all RF switches found in today's mobile phones. This substrate has proven successful in partially depleted SOI (PDSOI) technology, with several circuits built on it showing excellent RF performance. However, the emergence of fully depleted SOI (FDSOI) technology, which offers reduced gate lengths, higher transition frequencies, and improved power capabilities suitable for millimeter-wave applications, has introduced new challenges. Integrating the trap-rich substrate into FDSOI has proven difficult due to compatibility issues with the defect-rich polysilicon layer, leading to concerns about increased reverse current and the potential degradation of the substrate's performance under high thermal budgets. Additionally, the high cost of the trap-rich substrate poses further challenges to its widespread adoption.

This thesis explores alternative substrates that are compatible with FDSOI technology, comparing them against the trap-rich and high-resistivity substrates to assess their effectiveness. Proposed solutions include the field effect (FE) passivation technique and smart buried PN junctions, both validated through

proof-of-concept experiments at UCLouvain and successfully implemented using industrial FDSOI processes. Another promising approach developed at UCLouvain is the double-buried oxide (double-BOX) substrate, which builds on the trap-rich concept to enhance RF performance. Additionally, gold-doped silicon substrates and porous silicon are investigated for their excellent RF performance, offering viable alternatives starting from highly doped silicon substrates.

To validate these novel solutions, this thesis includes the design and evaluation of three RF circuits—switches, power amplifier, and mixers—using 22FDX® and 28FDSOI technologies. These circuits are analyzed to determine the impact of different substrates on their performance, providing a comprehensive understanding of how substrate technology influences RF circuit behavior in the context of FDSOI advancements. This work offers valuable insights into the future of mobile technology and the critical role of substrates in pushing the boundaries of RF performance.

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Introduction

Context

- Silicon technology is the most mature and cost efficient technology.
- Today, CMOS-SOI offers competitive performance, making it ideal for 5G, IoT, radar, and satellite applications.
- The new 5G technology aims to significantly improve wireless communication by increasing **data speed**, **reducing latency**, and **minimizing power consumption**.
- A key feature of the upcoming 5G technology is the use of high-frequency millimeter waves to expand available bandwidth. This requires arrays of antennas to focus the transmitted signal in specific directions. Each array is connected to RF front-end circuits, with each unit supporting between 4 and 24 antennas [1]. Ideally, these units will include components such as PAs, LNAs, switches, phase shifters, and variable gain amplifiers (VGAs) for each antenna, leading to a highly complex architecture.
- To ensure optimal system performance, careful attention must be paid to minimizing losses, coupling, and improving linearity in the front-end circuits.
- RF performance is influenced by various factors, including circuit topology, architecture, and the underlying technology. SOI is particularly well-suited for higher frequencies due to its higher integration density, better threshold voltage control, and lower substrate capacitance.

Motivation for this Work

As operating frequencies increase, the gate length of transistors must decrease. RFSOI technology with PDSOI transistors offers strong RF performance. To further enhance this technology, engineered substrate solutions have been developed and successfully integrated, transitioning from standard to high-resistivity substrates. PDSOI achieved exceptional RF performance when combined with a trap-rich polysilicon substrate, making it a promising candidate for 5G applications and mobile telecommunications.

The trap-rich substrate is one of the high quality substrates offered in the silicon market denoted as enhanced signal integrity eSI^{TM}. Beyond demonstrating low losses, low coupling and higher linearity, it shows **high integration in the PDSOI nodes** boosting the RF performances of all circuits designed atop of it. Moreover, the TR substrate is employed in practically 100 % of the switching circuits between the RF front-end and the antenna in modern day smartphone devices.

Driven by the desire to go higher in frequency and low power consuming, the FDSOI came as an innovative solution. Beyond decreasing the thickness of the box and the active silicon and offering another terminal called the back-gate contact, FDSOI demonstrates high f_t and f_{max} approaching values around 350 and 400 GHz respectively, comparable with III-V technologies. The development of such a new device puts FDSOI one step ahead compared to other architectures.

However, the **integration of the trap-rich polysilicon substrate in the FDSOI is forseen as challenging** due to the presence of below-BOX functionalities such as the back gate contact, isolations wells and diodes. Compatibility issues are predicted when wanting to implement these functionalities in a defect-rich polysilicon layer instead of the bulk silicon, it is expected that the reverse current of a biased back-gate well formed in such a polysilicon layer will be orders of magnitude larger than in a crystalline silicon material. Moreover, during an ordinary CMOS process, the trap-rich layer loses its efficiency due to the high thermal variation (recrystallization [1] effect) around 1100 °C for an average time of 2 hours.

[1] Recrystallization occurs when a polycrystalline structure comes into physical contact with a monocrystalline structure, leading the former to mimic the latter under high temperature conditions

Objectives

- Today, beyond the fact that the trap-rich substrate is considered as an expensive material, the semiconductor foundries portfolio is not offering the FDSOI nodes under polysilicon substrate option. The unique solution is the highly doped substrate with a resistivity around 20 Ω·cm.
- This work aims to provide different solutions that could be **alternatives to the trap-rich substrate** in FDSOI nodes while maintaining the high quality interface passivation BOX-SiO_2. These solutions **should be able to overcome the PSC effect** leading to low substrate loss, low coupling through substrate, higher linearity and high level integration in the FDSOI node.
- Another objective of this thesis is to **give a physical explanation to the particular behavior of each silicon based solution** under both small- and large-signal. Moreover, comprehensive simulations have been conducted using TCAD, leading to a deeper understanding of each physical phenomenon.
- Beyond giving solutions to counteract the PSC effect using passive devices, another goal of this thesis is to **assess those solutions in an industrial process**. Combining both active and passive devices through the design of a circuit gives a strong feedback on **the efficiency of this solution**.
- Another key objective of this thesis **is to design** a key part of the RF front-end module (RFFEM) that **can compete with the latest circuits** working at similar frequencies. The aim is to **improve RF circuit design by using new techniques and substrate solutions discussed in this thesis**, making sure the designed component stays relevant and competitive in the field.

Structure of the Thesis

This thesis is organized as follows:

In **Chapter 1** an overview of advancements in RF and mmWave technologies, focusing on silicon-based systems will be provided. It introduces the evolution of these technologies in modern communication systems and emphasizes the role of FDSOI, particularly 28FDSOI and 22FDX®. The importance of substrates with low losses, high resistivity, and improved linearity is discussed, alongside solutions like the trap-rich polysilicon substrate and challenges related to parasitic surface conduction (PSC). Advanced characterization and modeling techniques are highlighted to be crucial for optimizing RF performance, concluding with key challenges in RF and mmWave circuit design.

In **Chapter 2**, a detailed descriptions of various characterization and modeling methodologies will be provided. The setups for key measurements, including S-parameters, harmonic distortion will be illustrated and explained. Additionally, simulation techniques for assessing effective resistivity and harmonic distortion will be introduced. Complementary simulations focusing on quantifying the density of traps in the polysilicon trap-rich layer will also be presented. Together, these methodologies will offer a thorough framework for understanding the electrical behavior and performance of RF devices.

In **Chapter 3**, various alternative solutions to mitigate the parasitic surface conduction (PSC) will be introduced, supported by both measurements and simulations. Techniques such as field effect passivation, smart buried PN junctions, and the double-BOX substrate are explored for substrates with bulk resistivity exceeding 3 kΩ·cm. Additionally, solutions like gold-doped (Au-Si) silicon and porous silicon substrates will be discussed for highly doped bulk silicon (10 Ω·cm or lower), offering new approaches to enhance RF performance.

In **Chapter 4**, integrated circuit demonstrators designed on various substrate solutions will be presented. These circuits include RF switches, power amplifier, and RF mixers, all developed using FDSOI technology (either 22FDX® or 28FDSOI). The RF switches are optimized for operation around 6 GHz, utilizing high-power handling transistors, while the mixers and power amplifiers are designed for operation at around 28 GHz, leveraging low-threshold voltage transistors. Each circuit's performance is benchmarked against the state of

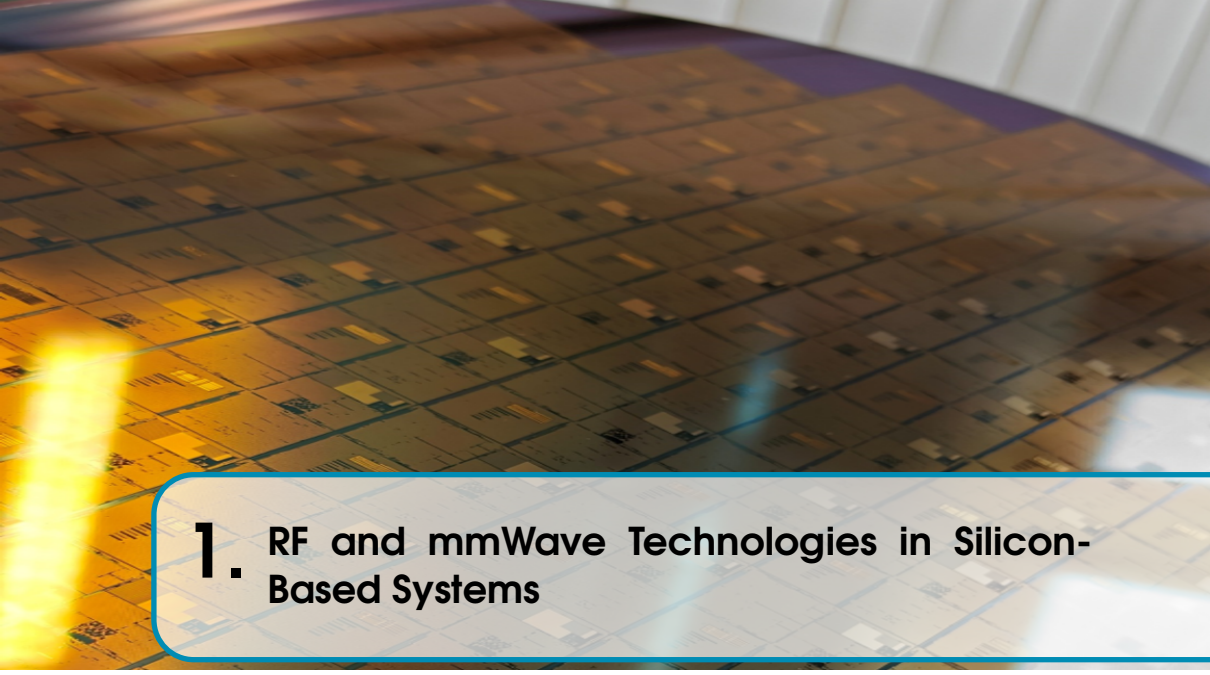
the art to provide a thorough comparison and evaluation of the advancements achieved.

The **Table 1** below presents the original scientific contributions of the author in terms of substrate solutions and RFIC design methodologies. Each contribution is highlighted and positioned relative to the current state of the art, demonstrating advancements in substrate technology and innovative design approaches. These contributions provide significant insights into the optimization of RF performance and underscore the novel methodologies introduced through this research.

Table 1: Author's contribution to the scientific community.

Topic	Contribution	Comments	Refs
Substrates	PN Junction integration	PN junctions were first demonstrated at UCLouvain as a proof of concept [2]. This thesis extends that work by integrating them into the industrial 28FDSOI process, highlighting their potential for large-scale use (see **Section 3.3**).	[3]
	Double-BOX development	The double-BOX substrate, featuring a second BOX below the trap-rich layer, has been demonstrated as an effective solution to overcome the PSC. This work is the first of its kind, originating from a patent (see **Section 3.4**).	[4]
	Au-Si bias dependency under small- and large signal	Gold-doped silicon substrates have been shown to effectively overcome the PSC. In this thesis, the research extends further by measuring and simulating the effective resistivity of the substrate as a function of applied DC bias. Additionally, the linearity of the substrate has been both simulated and experimentally measured (see **Section 3.5**).	[5]
	Traps modeling in polysilicon silicon	Starting from the measured energy levels of traps in the silicon bandgap, this thesis successfully models the trap-rich polysilicon substrate by proposing a spatial distribution and specific trap density. The resulting simulations closely align with the RF measurements conducted.	**Section 2.4**

Topic	Contribution	Comments	Refs
RFIC design	RF switches	Two types of sub-6 GHz RF switches were designed in 28FDSOI technology, utilizing advanced techniques and PN junction passivation. These designs demonstrate not only the effectiveness of PN junctions in improving passive device performance but also their potential application in complete circuit (see **Section 4.1**).	**[6]**
	Wideband power amplifier	The impact of the substrate was explored through the design of a wideband power amplifier operating in the 22-42 GHz frequency range. This amplifier was built on both a standard substrate and a high-resistivity substrate, providing insights into how substrate properties influence the performance of RF circuits.	**Section 4.2**
	RF Mixers	Two distinct 28 GHz RF mixers were designed in this work. The first mixer utilizes a conventional Gilbert cell topology, delivering high gain and a low noise figure. The second mixer introduces an innovative back-gate topology, demonstrating the feasibility of using the back-gate of an FDSOI transistor as an RF input instead of its conventional role as a DC bias point. This approach showcases the potential of modulating FDSOI transistors through the back-gate for RF mixing (see **Section 4.3**).	**[7]**



1. RF and mmWave Technologies in Silicon-Based Systems

This chapter provides a comprehensive overview of the advancements in RF and mmWave technologies, particularly in the context of silicon-based systems. Beginning with an introduction to RF and mmWave technologies, it explores the evolution and importance of these technologies in modern communication systems. Special attention is given to the role of FDSOI technology in RF and mmWave applications, focusing on the commercially available 28FDSOI and 22FDX®. The chapter further delves into the significance of substrates, highlighting the need for materials with low losses, high resistivity, and improved linearity to enhance RF performance. Solutions like the Trap-Rich Polysilicon substrate and the challenges related to the parasitic surface conduction (PSC) effect are discussed. Advanced characterization and modeling techniques are introduced as essential tools for optimizing these technologies. Finally, the chapter outlines the key challenges faced in RF and mmWave circuit design, setting the foundation for subsequent discussions on substrate and material solutions to address these challenges.

1.1 Overview of RF and mmWave Technologies

This subsection discusses the general principles, evolution, and applications of RF and mmWave technologies.

During the early stages of wireless system development, only lower-frequency bands were used due to various technical limitations. Over time, researchers began to recognize the potential of higher-frequency spectrums for more efficient transmission and reception, including radio frequencies (RF), microwaves, and millimeter waves (mmWaves). Broadly speaking, RF, microwave, and mmWave designations refer to electromagnetic waves within the frequency range of 1 MHz to 300 GHz, with corresponding wavelengths ranging from 300 meters to 1 millimeter [8, 9].

This shift toward higher-frequency bands paved the way for the ongoing development of mobile communication technologies. As seen in Table 1.1, mobile networks have progressed through various generations, starting with the introduction of 1G in 1979 and extending to the expected development of 6G in the 2030s. Each generation has introduced significant advancements in operating frequency, bandwidth, and channel capacity, enabling more sophisticated communication features and improved performance.

In 1979, the first generation (1G) of mobile communication emerged, primarily focused on analog cell phones and basic voice calling features. Operating in the 150-900 MHz frequency range, 1G provided a limited bandwidth of 30 kHz and a channel capacity of approximately 2.4 kbps. As technology progressed, 2G and 2.5G were introduced in 1991, bringing digital communication features such as SMS, MMS, conferencing, long-distance call tracking, and, later, internet access [10]. These networks operated at a higher frequency of 1.8 GHz and offered greater bandwidth (around 200 kHz) and channel capacity (approximately 64 kbps).

Table 1.1: Comparison of features of various generations of mobile communication technologies [11].

Technology	Year	Feature introduced	Frequency	Bandwidth	Channel capacity
1G	1979	Analog cell phone, calling	150-900 MHz	30 kHz	$\sim$ 2.4 kbps
2G/2.5G	1991	Digital, SMS, conference, MMS, long-distance call tracking, internet (in 2.5G)	1.8 GHz	$\sim$ 200 kHz	$\sim$ 64 kbps
3G	2001	Video call, GPS, broadband internet	1.6-2 GHz	$\sim$ 100 MHz	$\sim$ 2 Mbps
4G	2009	Super data, HD streaming	2-8 GHz	$\sim$ 100 MHz	100 Mbps
5G	2019	Internet of things, MIMO, cloud storage, cloud computing	3-30 GHz	100 $\times$ BW/unit area	10 Gbps
6G	2030s	High system capacity, global coverage, AI	110-170 GHz	Undefined for now	Up to 3 Tbps

By 2001, the third generation (3G) of mobile networks further expanded the range of services by introducing video calling, GPS, and broadband internet. Operating between 1.6-2 GHz, 3G increased the available bandwidth to 100 MHz, with a channel capacity of roughly 2 Mbps, enabling faster data transfers and improved connectivity [12]. The rise of 4G in 2009 marked a significant leap, focusing heavily on data services. This generation, operating in the 2-8 GHz frequency range, supported high-definition streaming and super data speeds [13–15], with a bandwidth of 100 MHz and a channel capacity of up to 100 Mbps.

The introduction of 5G in 2019 pushed the boundaries of mobile technology even further. 5G supports revolutionary technologies such as the Internet of Things (IoT) [16], multiple input multiple output (MIMO) [17], cloud storage [18], and cloud computing [19]. With a broad frequency range from 3-30 GHz, it offers immense bandwidth (100 times greater than that of 4G per unit area) and can achieve a channel capacity of up to 10 Gbps, providing the infrastructure necessary to support faster communication and increased data volumes.

Looking into the future, 6G is expected to be rolled out in the 2030s. This generation aims to offer high system capacity, global coverage, and enhanced integration with artificial intelligence (AI). Although specific details on bandwidth remain undefined, 6G is projected to operate at frequencies at around 110-170 GHz (D-band frequency) and could potentially offer channel capacities of up to 3 Tbps, making it a major step toward addressing the growing demands for data and connectivity [20].

Today (2024), the focus is on developing technology for 5G applications (see **Table 1.1**), which demand high bandwidth and increased channel capacity to support faster data rates and greater connectivity. To meet these stringent specifications, the design of an integrated system, commonly referred to as the RF front-end module (RFFEM), is critical. This system is responsible for efficiently handling signal transmission and reception in high-frequency ranges.

Figure 1.1 presents an architecture for an RFFEM used in today's telecommunications systems, note that green blocks will be discussed further in this thesis. This system illustrates how various components work together to process RF signals. Starting from the antenna, the incoming signal is directed through a

switch that manages signal routing. The signal is then amplified by a low-noise amplifier (LNA), which boosts weak incoming signals while minimizing noise. Before reaching the mixer, the signal passes through a band-pass filter (BPF) to isolate the desired frequency range. The mixer, with the help of a local oscillator (LO), down-converts the RF signal to an intermediate frequency (IF) for easier processing. After conversion, the signal undergoes IF filtering to further clean up the signal before it is processed in the baseband for data handling.

For the transmission side, a similar process occurs in reverse. The signal is generated at the baseband, passes through an IF filter, and is upconverted by the mixer to RF frequencies using the LO. It is then amplified by a power amplifier (PA) before transmission through the antenna. Each of these components plays a crucial role in ensuring efficient and reliable signal transmission and reception, key requirements for enabling high-speed, high-capacity communication in modern 5G networks.

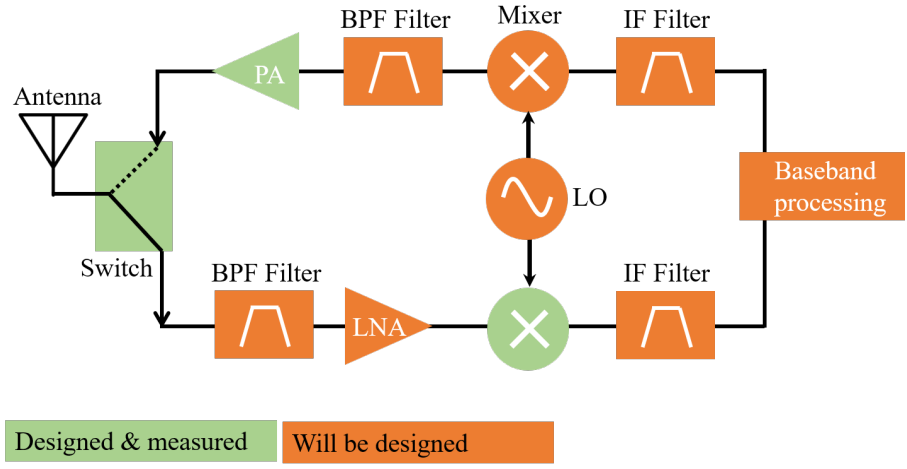


Figure 1.1: Conventional RF front-end module architecture designed for modern telecommunications systems, illustrating key components such as the PA, LNA, mixer, green circuits will be studied in this thesis.

Several circuits can be designed using various materials like Gallium Arsenide (GaAs), Gallium Nitride (GaN), and Silicon-on-Sapphire (SOS), all of which offer excellent RF performance. These materials are known for their high electron mobility, power handling capabilities, and thermal conductivity,

making them suitable for high-frequency and high-power applications. However, despite their advantages, they tend to be more expensive and less scalable compared to silicon-based technologies.

Silicon, being a more mature and cost-effective material, has led to the dominance of CMOS technology, particularly in silicon-on-insulator (SOI) processes, in the RF domain. SOI technology provides several distinct advantages. One of the key benefits is the reduced parasitic capacitance, due to the insulation layer, which improves signal speed and energy efficiency. Additionally, SOI substrates help in minimizing crosstalk between different circuit components, enhancing the isolation necessary for RF circuits. SOI technology also allows for higher transistor densities, enabling the integration of more complex circuits without compromising performance. Furthermore, SOI provides good thermal conductivity and low leakage currents, making it ideal for low-power applications. These advantages make SOI a versatile and reliable choice for RF circuits, particularly when cost and scalability are important considerations.

As a result, nearly 100 % of RF switches in present smartphones are now built on SOI technology. The combination of superior RF performance, scalability, and cost-efficiency has made SOI the industry standard for RF switches, which are critical components in modern wireless communication systems, including 5G applications. The mature manufacturing process and widespread adoption of SOI have cemented its place as the most suitable technology for designing high-performance RF circuits.

1.2 FDSOI Technology in RF and mmWave Applications

At the beginning of the 2000s, RF switches were predominantly based on partially-depleted SOI (PDSOI) technology, utilizing relatively large gate lengths, such as 0.250 µm [21], 0.180 µm [22], and 130 nm [23]. Over the years, the gate length was progressively reduced, eventually reaching 45 nm [24], in order to enable operation at higher frequencies. Alongside the reduction in gate length, other key advancements were made, such as the thinning of the buried oxide (BOX) layer.

Following these developments, fully depleted SOI (FDSOI) technology emerged as a superior alternative, offering significant advantages in terms of f_t and f_{max}[1] approaching 400 GHz [26]. Two commercially available FDSOI platforms have since become prominent: 22FDX® [27] from GlobalFoundries and 28FDSOI [28] from STMicroelectronics.

The back-gate in FDSOI technology is one of its most significant features, providing an additional degree of control over the device's performance. Unlike traditional bulk CMOS technology, where only the front-gate is used to control the electrostatics of the transistor, FDSOI incorporates a back-gate, or body-bias terminal, which allows further modulation of the transistor's characteristics. This back-gate can be used to dynamically adjust the threshold voltage and other key parameters of the transistor, providing flexibility in optimizing power consumption [29], linearity [30], or both, depending on the application requirements.

The unique aspect of FDSOI's back-gate is its wide tuning range. While body biasing is also available in planar bulk CMOS technology, the range of tuning offered by FDSOI is significantly larger, making it an excellent tool for fine-tuning RF performance. The back-gate can act as a tuning knob, adjusting parameters such as gain, linearity, and power consumption in real-time, without impacting the front-gate operation [25]. This allows designers to enhance performance across different frequency bands or operational modes, making FDSOI a highly adaptable technology for modern high-frequency applications

[1] f_t and f_{max} are the frequencies at which the short-circuit current gain and the maximum available gain, respectively, become unity. These parameters serve as general indicators of the amplification capabilities of a transistor, showing how much gain it can provide at a given frequency or the maximum frequency up to which it can effectively amplify a signal [25].

like 5G, IoT, and mmWave communications.

1.2.1 Advanced FDSOI Technology Overview/Description

Redacted Confidential Content

1.2.2 22 nm FDSOI from GlobalFoundries (22FDX®)

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1.2.3 28 nm FDSOI from ST-Microelectronics (28FDSOI)

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1.2.4 Super Low Threshold Voltage and Thick Oxide Devices in FDSOI

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1.3 Substrate Specification Needs for RF

Silicon-based technologies currently offer significant advantages in cost and volume manufacturing compared to other materials, due to the maturity of processes available on 300-mm-diameter wafers [31]. The most advanced CMOS nodes, especially SOI technology, are elevating RF figures of merit (FoMs) to unprecedented levels. This is facilitated by offering an attractive cost-effective mass market production of RF and mmWave applications such as 5G, radars [32], connected objects, and the Internet of Things (IoT) [33]. To achieve advanced telecommunication standards such as 4G and 5G, the superposition of multiple frequency bands is employed to achieve high data throughput. Circuit elements built inside the front-end-module (FEM) sense the substrate, which is an important part of the electromagnetic environment below those circuits.

Over the past decade, a variety of substrates have been proposed to improve the RF performance of circuit elements, emphasizing the critical importance of substrate selection. The choice of substrate plays a pivotal role in determining the overall efficiency and effectiveness of RF circuits. Key characteristics that a suitable substrate should possess include **low losses**, ensuring minimal energy dissipation during signal propagation, and **high effective resistivity**, typically greater than 1 kΩ·cm. Additionally, **high linearity** is essential, particularly for maintaining signal integrity under large signal conditions, where the second harmonic distortion must remain below -70 dBm at an input power of H1= 15 dBm. These attributes are crucial for achieving optimal RF performance. By carefully selecting a substrate that meets these stringent criteria, designers can significantly enhance the performance and reliability of RF circuits across a wide range of applications.

The RF performance of a substrate, as previously indicated, does not guarantee the substrate's suitability for designing circuits atop it and to be in the next generation of mobile phones. It is crucial that the substrate is **compatible with conventional industrial CMOS processes** and remains unaffected by temperature variations, as any degradation in performance could negatively impact the transistor performance of the technology employed. Another critical specification for the advanced substrate is **mechanical robustness and stability**. The chosen substrate must withstand the fabrication process, including metal deposition, oxide deposition, and chemical mechanical polishing (CMP), without being adversely affected. Furthermore, the low cost of the substrate is

another crucial specification. However, it will not be discussed further due to the lack of available information on my end.

1.3.1 The HR Substrate and the PSC as the Main Drawback

The standard substrate with a resistivity of approximately 10-20 Ω·cm is appealing due to its low cost, making it an affordable option for many applications. However, it is inadequate for RF applications because it introduces substantial losses and non-linearities, particularly in passive devices implemented on top of it. These losses can severely degrade the performance of RF circuits, as illustrated in **Figure 1.2(a)**.

In contrast, high-resistivity (HR) substrates, with a nominal resistivity exceeding 3 kΩ·cm, offer significantly improved RF performance. The higher resistivity effectively reduces coupling between different devices on the same substrate, thereby minimizing parasitic effects and signal degradation. This makes HR substrates more suitable for advanced RF applications.

However, a challenge arises with the insulating layer, often composed of SiO_2 (or, in some cases Al_2O_3 having negative oxide charges), which contains positively charged oxide charges. These charges attract electrons to the SiO_2-bulk interface, forming a conductive layer with a resistivity as low as 1 mΩ·cm. This phenomenon, known as parasitic surface conduction (PSC), leads to additional losses, as depicted in **Figure 1.2(b)**.

It is important to note that the standard substrate introduces volume losses, while the HR substrate primarily suffers from interface losses. The relatively low resistivity of standard substrates leads to significant power dissipation throughout the bulk material, affecting overall RF performance. In contrast, HR substrates mitigate these volume losses but still face challenges related to parasitic surface conduction (PSC) at the interface, which introduces losses at the SiO_2-bulk boundary.

A potential solution for addressing these interface losses is the trap-rich substrate, which will be discussed in detail later in this thesis. This innovative substrate design specifically targets the reduction of PSC and other interface-related losses. Moreover, in **Chapter 3**, solutions for bulk losses will be proposed, exploring methods to further enhance the overall RF performance of

substrates.

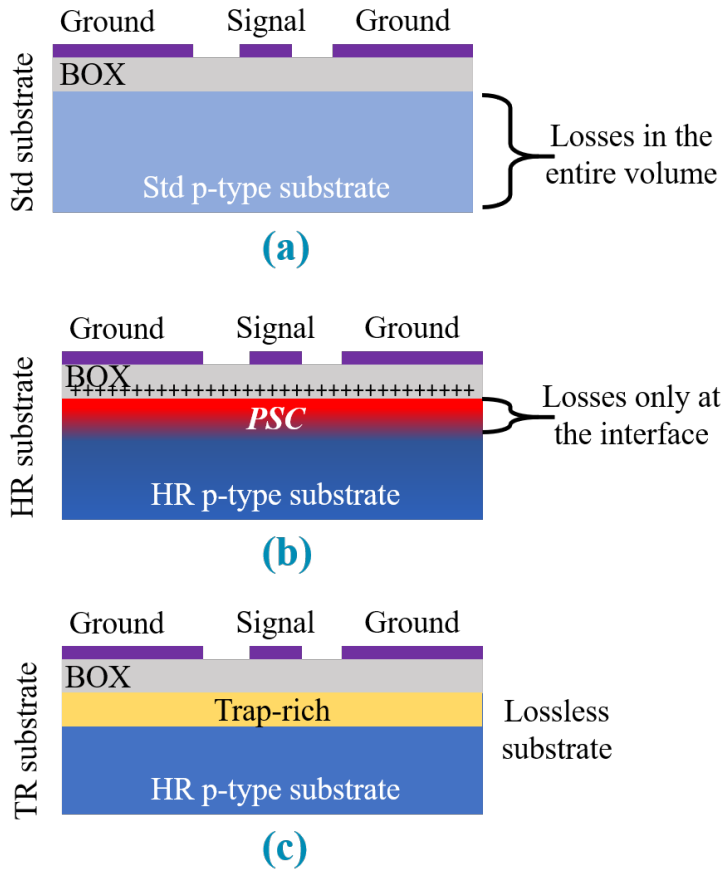


Figure 1.2: Schematic view of bulk losses in **(a)** using a low resistivity substrate (20 $\Omega \cdot$ cm), interface losses caused by the PSC in **(b)** and the conventional trap-rich substrate solution in **(c)**. The nominal resistivity of the HR bulk is usually higher than 3 k$\Omega \cdot$ cm. All the CPW lines are represented under the bias condition V_{DCLine} =0 V.

1.3.2 Trap-Rich Polysilicon the Solution to Tackle the PSC

In the realm of passive RF devices, PSC poses a significant challenge that must be addressed. To tackle the PSC effect, UCLouvain and Soitec collaborated to develop the trap-rich (TR) substrate, which incorporates a thin layer of polysilicon (ranging from 300 nm to 2 µm) between the insulating buried oxide (BOX) layer and the HR silicon bulk [34]. Leveraging the high density of trapping states in the polysilicon layer, this substrate effectively pins the Fermi level near the silicon mid-gap, with free electrons being trapped within this layer. This has been demonstrated through ATLAS TCAD simulations using two different substrates HR and TR substrates that are depicted in **Figure 1.2(b)** and **Figure 1.2(c)**, respectively.

Both substrates feature a BOX of 500 nm, and a density of positive oxide charges of 1×10^{11} cm^{-2}. Exclusively for TR substrate, a 500 nm of polysilicon layer was introduced. Moroeover, the polysilicon trap-rich layer was simulated using tail distribution for donor and acceptor traps to model the polysilicon layer according to the model given in [35] and using characteristic decay energy of 33 meV and edge band state density of 10^{22} cm^{-3} eV^{-1}. The dimensions of the CPW lines are: a signal electrode width Wc of 26 µm, a spacing between the signal and the ground electrodes S of 12 µm, and ground planar electrode width Wg of 208 µm (LineCsetC described in **Section 2.2.2**).

Figure 1.3 shows the extraction of the energy bands (valence and conduction bands) along the depth of the substrate starting from the BOX for HR substrate in **Figure 1.3(a)** and for TR substrate in **Figure 1.3(b)**. The Fermi level E_F is defined at 0 eV (definition usually used by atlas Silvaco). Moreover, the applied DC bias V_{DCLine} =0 V. For HR substrate it is shown the conduction is bent toward the Fermi level indicating a high probability of electrons in the first 1-2 µm far from the BOX. This is because of the positive oxide[2] charges that attracts electrons from the bulk leading to the creation of the PSC. After that, the Fermi level is situated around the silicon mid-gap showing that the substrate

[2]It is worth noting that in the case of BOX=SiO_2 (silicon oxide) the oxide charges are positive. But if BOX= Al_2O_3 (aluminum oxide for example) is used, the charges are negative, in this case the oxide charges will attract holes from the substrate leading to the creation of a positive PSC. In that case, it is the valence band that will bend towards Fermi level in **Figure 1.3(a)**. Those simulations and measurements are not reported in this thesis since it is not the main scope, the focus is mainly on SiO_2. Moreover, the solutions to overcome the PSC that will be discussed could be expanded to the Al_2O_3 insulating layer.

is highly resistive.

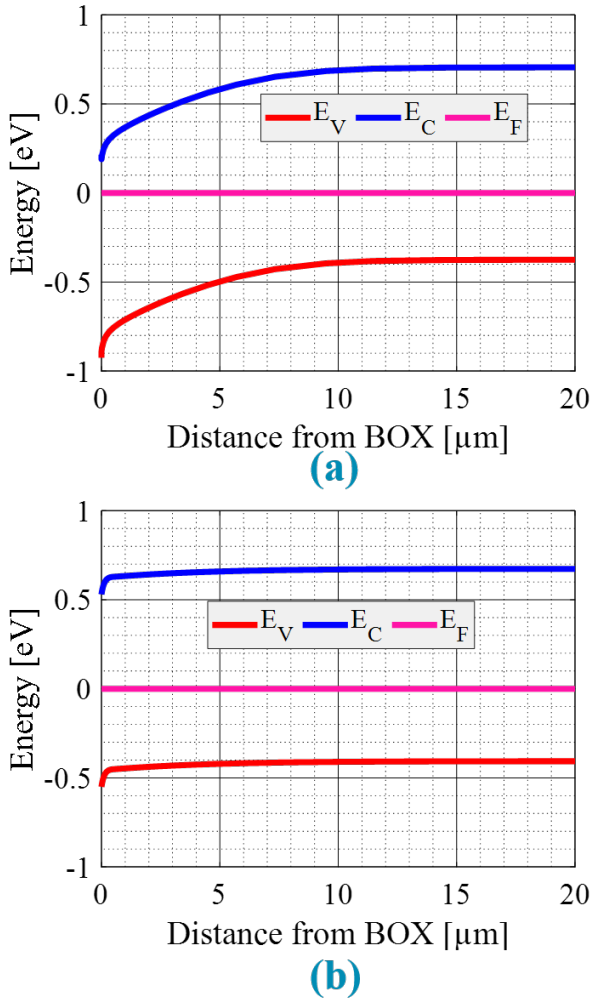


Figure 1.3: Energy bands for HR substrate with PSC in **(a)** and bands for TR substrate in **(b)** below the signal electrode of the CPW line for V_{DCLine} =0 V simulated atop of p-type silicon bulk.

On the other hand, the TR substrate in **Figure 1.3(b)** shows a Fermi level that is near silicon mid-gap at the interface and deep in the bulk silicon. This is due to the high density of traps introduced in the polysilicon trap-rich layer

that traps the carriers coming from the substrate. When applying a different DC bias on the CPW line $V_{DCLine} \neq 0$ V, the Fermi level will not change and will still near silicon mid-gap, this is called *Fermi level pinning*. Moreover, this state translates into low losses of the CPW line built atop of this substrate, high effective resistivity and high linearity. More measurements and simulations for HR and TR substrates will be shown as we go along in the next sections.

The TR substrate demonstrates excellent RF performance, boasting its effective resistivity to around 10 kΩ·cm and second harmonics below -70 dBm. Over the years, numerous passive devices such as CPW lines, inductors, and crosstalk structures have been successfully implemented on this type of substrate [36]. Additionally, the TR substrate has found considerable success in PDSOI technology. In this thesis several trap-rich like (and alternatives) solutions will be studied and described.

1.4 Advanced Characterization and Modeling Motivation

This subsection highlights the need for advanced modeling and characterization methodologies in designing high-performance RF and mmWave devices and circuits.

The development of new substrates for RF and mmWave applications necessitates precise and comprehensive characterization methods. In order to optimize the performance of advanced devices, such as those utilizing FDSOI technology or other high-resistivity substrates, accurate extraction of parameters such as effective resistivity, parasitics, and harmonic distortion is critical. These parameters are fundamental for ensuring the proper functioning of RF circuits and for achieving optimal performance in high-frequency applications.

The extraction of effective resistivity is a key step in substrate characterization. Effective resistivity is a figure of merit that gives insight into how well a substrate mitigates the PSC, a phenomenon that can significantly degrade the performance of RF components. Accurate measurement of this property requires careful setup and calibration of experimental tools. For instance, on-wafer S-parameter measurements must be meticulously conducted to see the high-frequency behavior of transmission lines and other passive components. S-parameters are essential for understanding signal propagation, losses, and impedance matching, which are crucial for high-performance RF designs. Any inaccuracies in the S-parameter measurements can lead to faulty models and thus result in a non prediction of circuit performance.

Another important aspect of substrate characterization is the ability to reproduce measurements through simulations (see **Figure 1.4**). Simulations provide an effective way to gain control over the physical effects that influence device performance, allowing for a deeper understanding of how a substrate or circuit behaves under different operating conditions. Throughout this thesis, a close correlation between measurements and simulations will be maintained. By ensuring that simulations replicate real-world measurements, it becomes easier to identify any discrepancies that may arise from model inaccuracies or unexpected physical phenomena. This, in turn, enables the optimization of both the substrate and the circuit design process.

Typically, the simulation and measurement of effective resistivity are per-

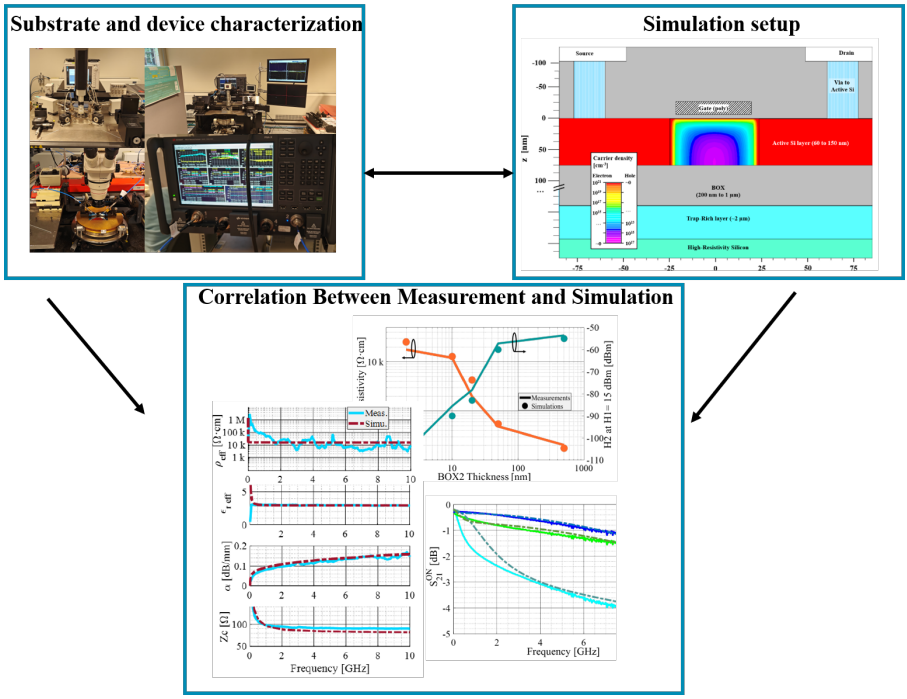


Figure 1.4: Overview of the advanced characterization and modeling workflow for RF and mmWave substrates.

formed first. Once the resistivity characteristics are well understood, the focus shifts to the simulation and measurement of harmonics, especially when coplanar waveguide (CPW) lines are fabricated. Simulating harmonics allows to understand the nonlinear behavior of substrates since they are under different condition compared to small-signal. These simulations are essential for predicting the harmonic behavior of the materials and ensuring that the CPW lines operate efficiently under real-world conditions.

On the circuit side, it's important to highlight that FET modeling has already been done extensively by foundries. Foundries provide device models that are used by circuit designers to simulate and predict the behavior of FETs within a given RF circuit. However, while these models are highly accurate, they are not without limitations. One of the major challenges today is that the substrate is often not fully considered in FDSOI technology. This oversight highlights the

need for greater accessibility to substrate parameters and models. It is crucial for silicon foundries to provide detailed and easy-to-use substrate models to ensure more accurate predictions of device performance and improve the overall design process. For instance, under different electromagnetic environment such as different handle substrate, the behavior of FETs may deviate from what is predicted by standard models. Therefore, additional characterization and model validation are required to ensure that the final circuit meets all performance specifications [37].

1.5 Challenges in RF and mmWave Circuit Design

Since modern wireless communication systems push towards higher data rates and better performance, there is a growing need for high-performance RF circuits with minimal losses, enhanced linearity, and reduced noise levels. Switches, LNAs, mixers, and PAs are key components in RFFEM design, and their performance is critical to the overall functionality of the communication system. Achieving higher performance in these components is particularly challenging in RF and mmWave frequencies, where signal integrity is more susceptible to losses, distortion, and other parasitic effects.

Traditionally, various design techniques have been explored to improve the performance of these circuits, particularly in the field of FET devices. Researchers have focused on improving transistor characteristics, such as boosting f_t and f_{max}, to enable circuits to operate at higher frequencies. Different circuit techniques have been widely studied to achieve higher gain, better linearity, and lower noise figures. However, despite these advancements in device-level design, there has been a growing interest in investigating the role of substrates in improving overall RF circuit performance.

In this thesis, the main focus is to examine whether the RF performance of circuits can be enhanced by changing the substrate. As discussed in **Section 1.3**, the substrate is a fundamental material that forms part of the electromagnetic environment surrounding the entire circuit. By exploring different substrate types, we aim to assess their impact on key performance metrics such as losses, linearity, power efficiency, and noise figures in RF circuits. Substrates with higher resistivity (HR and TR) have been shown to mitigate certain parasitic

effects like PSC, and this research seeks to determine if these substrates can meaningfully improve performance across various RF circuits.

1.5.1 Key Challenges in RF Circuits

In the design and development of RF circuits, particularly in the high-frequency domains of RF and mmWave technologies, several key challenges emerge that directly affect the performance and efficiency of these circuits. As wireless communication systems evolve and demand higher data rates **[38, 39]**, lower latency, and improved signal quality **[40]**, the design of RF circuits must meet increasingly stringent performance metrics. The primary challenges are around managing losses, improving linearity, maximizing power efficiency, and reducing noise, all critical for components such as RF switches, PAs, and mixers **[41]**.

One of the most significant challenges in RF switches (see **Figure 1.5**) is minimizing losses while simultaneously ensuring the circuit can handle high power levels. RF switches play an important role in directing signals between different paths or circuits within a communication system, and they need to do so with minimal insertion loss to preserve signal integrity. As frequency increases, even small losses can degrade the signal quality significantly, leading to lower performance in successive components such as amplifiers and mixers. Additionally, RF switches must handle high levels of power without breaking down or suffering from thermal degradation. This is particularly important in higher-frequency applications such as 5G and mmWave communications, where power levels are typically high, and device breakdowns can occur more easily. The choice of materials for the switch, as well as the substrate on which it is built, plays a crucial role in mitigating these losses and improving power handling capabilities. High-resistivity substrates been shown to reduce losses **[42, 43]** and increase the breakdown voltage, offering a potential solution to these challenges.

In PAs, the primary design challenges include maximizing saturation power and improving power added efficiency (PAE) as shown in **Figure 1.5**. The saturation power of a PA defines the maximum output power that can be delivered before the signal experiences compression. This is critical in RF circuits, where amplifiers must deliver clean, undistorted signals at high power levels. As frequencies increase, achieving high saturation power becomes more difficult

due to increasing losses and nonlinearities within the circuit. Furthermore, PAE is an important metric in evaluating how efficiently an amplifier converts DC input power into RF output power. In applications such as mobile devices and base stations, where power efficiency directly translates into battery life and operational cost, improving PAE is crucial. This is where substrate technology plays an important role—by reducing parasitics, substrates like high resistivity can help improve both PAE and saturation power in RF amplifiers.

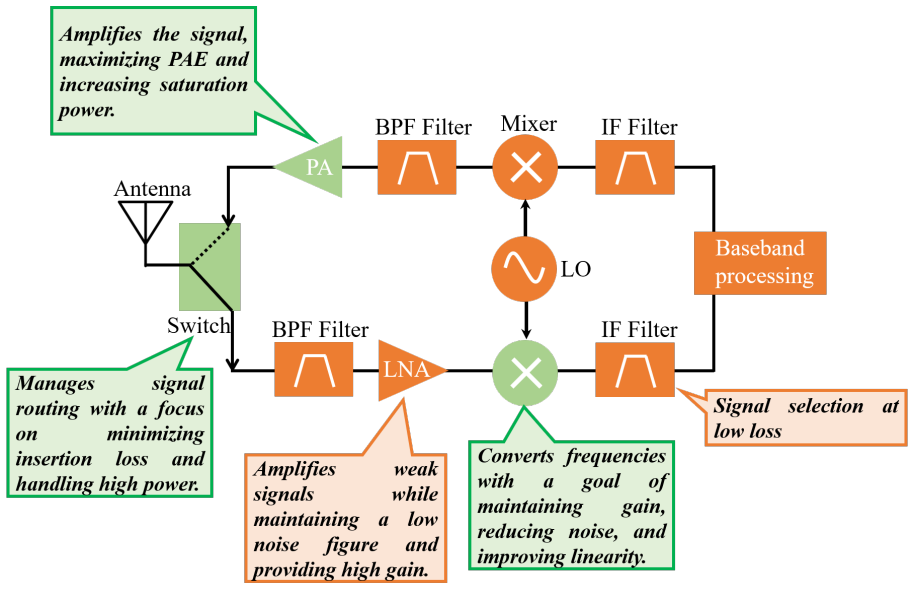


Figure 1.5: Diagram illustrating key RF circuit components, each block could show the critical performance challenges.

In RF mixers, the challenges are somewhat different but equally important. Mixers are used in RF systems to convert frequencies, typically from a higher RF frequency to a lower intermediate frequency (IF), and they need to do so with minimal loss of signal quality. The three main performance metrics for mixers are conversion gain, noise figure, and linearity (see **Figure 1.5**). Conversion gain refers to the increase in signal strength achieved by the mixer during frequency conversion, and achieving high conversion gain is essential for amplifying weak signals. At the same time, mixers need to have a low noise figur which is important for maintaining signal clarity. Linearity is another

key factor, as mixers often operate in non-linear regimes that can introduce harmonic distortion and intermodulation products, degrading the overall signal quality. Improving the linearity of mixers while maintaining high conversion gain and a low noise figure is a significant challenge, especially as the frequency increases.

1.6 Chapter Summary

This chapter introduced the fundamental concepts and the evolution of RF and mmWave technologies. It outlined the shift from the use of lower-frequency bands in the early stages of wireless systems to the exploration of higher-frequency spectrums for more efficient communication. The chapter explained the range of frequencies that classify RF, microwave, and millimeter waves, emphasizing how this shift opened the path for the advancement of mobile communication technologies.

An extensive discussion of the various generations of mobile communication technology, from 1G to the anticipated 6G systems, was presented, illustrating the progression in features, bandwidth, and channel capacity over time. Each generation of wireless technology was characterized by its increasing operational frequency, improving data rates, and growing complexity in communication protocols. Notably, 5G technology, introduced in 2019, has significantly increased bandwidth and channel capacity, making it possible to support a wide range of modern applications like the internet of things, cloud computing, and multiple-input, multiple-output technologies.

In 2024, the focus has shifted towards 5G applications, where the need for high bandwidth and increased channel capacity is paramount. To address these needs, the design of a complete RFFEM becomes essential. This chapter illustrated a typical architecture of an RFFEM, explaining the role of each component—from the antenna and switch to the mixer, LNA, and PA. The proper functioning of these circuits is crucial for achieving efficient transmission and reception of signals in high-frequency communication systems.

The chapter further discussed the importance of substrate materials in RF circuit design. Materials like GaAs, GaN, and SoS have been explored for their superior RF performance. However, SOI technology has emerged as the most cost-effective and scalable solution. SOI provides significant advantages in terms of reduced parasitic capacitance, improved thermal conductivity, and lower crosstalk.

The chapter concluded with an introduction to FDSOI technology, highlighting its significance in RF and mmWave circuit design. Initially, RF switches were designed using PDSOI with relatively large gate lengths. However, with advancements in technology, gate lengths have reduced significantly, enabling higher frequency operation. The emergence of FDSOI technology, along with the availability of 22FDX® and 28FDSOI platforms, has revolutionized RF circuit design by offering enhanced performance metrics such as higher cut-off frequencies and reduced power consumption. Additionally, the back-gate feature of FDSOI was introduced as a significant tool for fine-tuning transistor characteristics, further improving RF performance.

Throughout this chapter, the importance of substrates, device modeling, and circuit design methodologies was emphasized, laying the foundation for the advanced characterization and modeling approaches that will be explored in subsequent chapters.

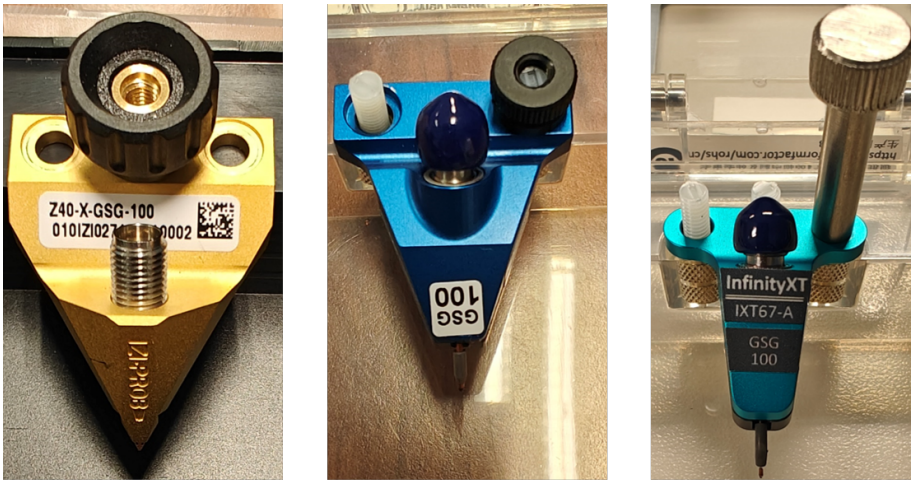


2. Characterization and Modeling Methodologies

In this chapter, various characterization and modeling methodologies will be described in detail. Different measurement setups will be illustrated and explained, including S-parameter measurements, harmonic distortion measurements. Additionally, simulation methods for assessing effective resistivity and harmonic distortion will be introduced. Complementary simulations aimed at quantifying the density of traps in the polysilicon trap-rich layer will also be presented. These methodologies will provide a comprehensive framework for understanding the electrical behavior and performance of RF devices.

2.1 Small Signal Characterization

RF probes are critical components in the testing and characterization of high-frequency semiconductor devices. These probes facilitate the measurement of electrical parameters directly on wafers, providing accurate and reliable data from DC to high-frequency ranges. Among the various types of RF probes available, the |Z| probe and the Infinity probe are notable for their performance across wide frequency ranges. The |Z| probe operates effectively from DC to 40 GHz [44], while the Infinity probe extends this capability up to 67 GHz [45]. Figure 2.1 show a photograph of the RF |Z| probe in (a) and Infinity probes in (b) and (c). It is mentioned that the |Z| probes lifetime on aluminum pads is 1,000,000 times while for Infinity 67 GHz is 250,000 times (same lifetime for Infinity XT). The maximum temperature for |Z| probes is 300 °C, for the Infinity 67 GHz is 125 °C and for the Infinity XT [46] is 175 °C (can go till 200 °C).



(a) (b) (c)

Figure 2.1: Photograph of the RF probes used for measurements in Welcome platform. (a): |Z| probe 40 GHz, (b): Infinity probe 67 GHz and (c): Infinity probes XT 67 GHz for high temperature.

Infinity probes are more fragile and more expensive compared to the |Z| probe. On the other side the Infinity probes have smaller pins, ans slightly less losses. It is estimated that the typical insertion loss at 40 GHz is 0.8 dB for |Z|

probes while 0.1 dB lesser for the Infinity. In the case of this thesis only |Z| probes and Infinity 67 GHz are used.

2.1.1 S-Parameters Measurement Setup

The RF probes previously described will be utilized with an RF prober and a vector network analyzer (VNA) for S-parameter measurements. The setup configuration is illustrated in **Figure 2.2**, ensuring careful cable connections to both the probes and the VNA. For CPW transmission lines, only 2 ports are utilized, except in the case of 3-port circuits such as RF mixers, where a third port is required. The power used to perform the measurement is -5 dBm, number of points is 801 and the average bandwidth is 300 Hz.

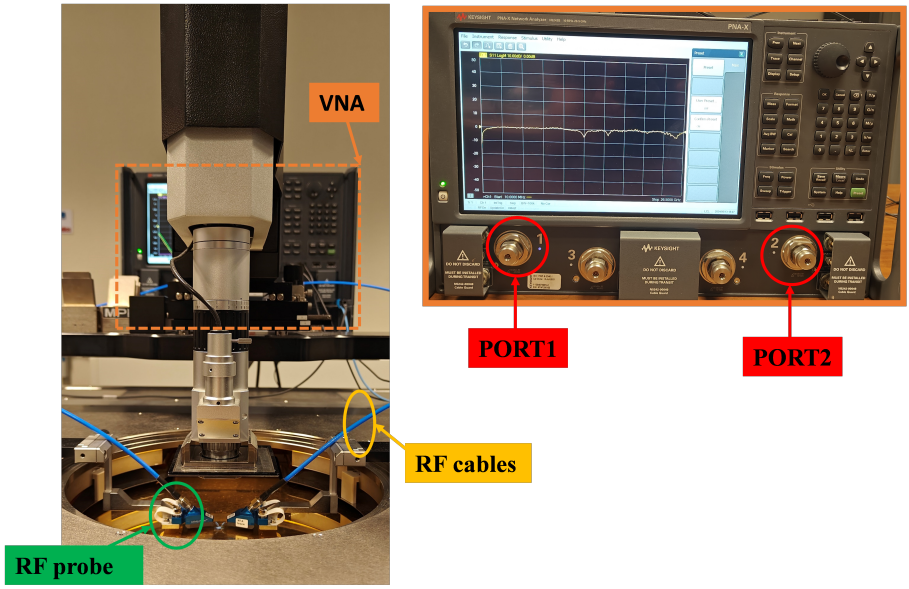


Figure 2.2: Small-signal setup used to measure the s-parameters using a VNA.

The short-open-load-thru (SOLT) calibration method is utilized to calibrate the system at the probe tips. Subsequently, measurements of the de-embedding structures, open and thru, are performed to mitigate pad parasitics using the method proposed by Gillon in [47]. Following this calibration, the CPW line of interest is measured, and the data are stored in a file. The data are then transferred from the VNA to the computer for extracting the effective resistivity,

which will be discussed in the next subsection.

2.1.2 Effective resistivity extraction

The effective resistivity is a crucial FoM for assessing RF substrates, as it directly influences the performance of passive devices and circuits operating at high frequencies. Effective resistivity serves as one of the key metrics for benchmarking substrates, representing the resistivity value if the substrate were considered entirely homogeneous, as defined in previous research [48]. This parameter is particularly important because it is frequency-dependent and can vary significantly across different substrates. For HR substrates, the effective resistivity typically is around 100 Ω·cm.

Before discussing the measurement results of various substrates, it is essential to understand the extraction method used to determine effective resistivity. The extraction process involves the analysis of S-parameters measured using a small-signal setup, as depicted in **Figure 2.2**, and one pair of the RF probes, illustrated in **Figure 2.1**. These measurements provide the necessary data to calculate the effective resistivity, offering insights into how different substrates behave under RF conditions. The following sections will outline this extraction procedure, paving the way for a comprehensive comparison of substrate performance in subsequent parts of this work.

In order to extract the effective resistivity ρ_{eff} several steps should be followed:

- **Step 1**: convert S-parameters into γ and Z_c.
- **Step 2**: convert γ and Z_c into RLGC.
- **Step 3**: convert RLGC into effective resistivity ρ_{eff}.

Step 1

The main goal is to use the measured S-parameters as inputs in the equations developed by either Eo or Dehan in order to get the values of γ and Z_c.
Eo's equations are [49]:

$$e^{-\gamma L} = \frac{1}{\left(\frac{1-S_{11}^2+S_{21}^2}{2\times S_{21}} + K\right)} \tag{2.1}$$

With:

$$K = \sqrt{\frac{((S_{11}^2 - S_{21}^2 + 1)^2 - (2 \times S_{11})^2)}{(2 \times S_{11})^2}} \tag{2.2}$$

Regarding the Z_c

$$Z_c^2 = Z_{ref}^2 \times \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \tag{2.3}$$

Dehan's equations are [50]:

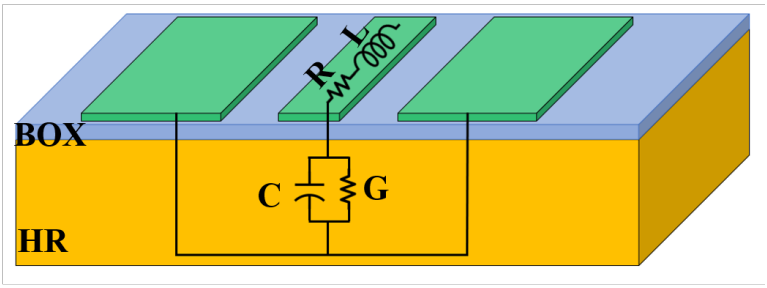
$$\gamma = 2 \times \text{atanh}\left(\sqrt{\frac{(1 - S_{11} - S_{12}) \cdot (1 + S_{11} - S_{12})}{(1 + S_{11} + S_{12}) \cdot (1 - S_{11} + S_{12})}}\right) \tag{2.4}$$

The characteristic impedance is computed as in Equation 2.3

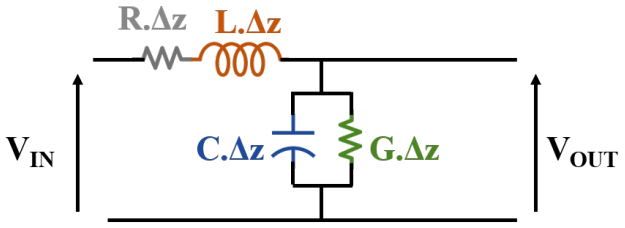
Step 2

After calculating the characteristic impedance Z_c and the propagation constant γ, these values are used to obtain the equivalent lumped elements of the CPW line. The RLGC parameters—R (series resistance per unit length), L (series inductance per unit length), C (shunt capacitance per unit length), and G (shunt conductance per unit length)—provide a distributed model of the transmission line's behavior.

RLGC parameters are crucial for analyzing the electrical characteristics of the CPW line. A detailed depiction of these RLGC parameters for the CPW line is presented in Figure 2.3.



(a)



(b)

Figure 2.3: CPW transmission line atop of a silicon substrate with RLGC component in (a). Infinitesimal length Δz of the line in (b).

It has been demonstrated in [51] and [52] that Z_c and γ could be written as a function of the RLGC through:

$$Z_c = \sqrt{\frac{j\omega L + R}{j\omega C + G}} \tag{2.5}$$

$$\gamma = \sqrt{(j\omega L + R)(j\omega C + G)} \tag{2.6}$$

Where ω is the angular frequency, and is expressed by $2\pi f$.

From Equation 2.6 and Equation 2.5 the RLGC elements are calculated using the following:

$$R = \mathrm{Re}\{\gamma Z_c\} \tag{2.7}$$

$$L = \frac{\mathrm{Im}\{\gamma Z_c\}}{\omega} \tag{2.8}$$

$$G = \mathrm{Re}\left\{\frac{\gamma}{Z_c}\right\} \tag{2.9}$$

$$C = \frac{\mathrm{Im}\left\{\frac{\gamma}{Z_c}\right\}}{\omega} \tag{2.10}$$

Moreover, the propagation constant can also be written as:

$$\gamma = \alpha + j\beta \tag{2.11}$$

Where α is the transmission line losses per unit length and β is the electrical phase delay. This equation is frequently used to extract the losses during the characterization process.

Step 3

In high-resistivity substrates, the material is inhomogeneous, featuring low resistivity near the interface and significantly higher resistivity deeper into the bulk due to the presence of positive oxide charges, as shown in **Figure 2.4(a)**.

To represent such substrates with a single resistivity value, the concept of effective resistivity is introduced, as outlined in **[48]**. The effective resistivity (ρ_{eff}) serves as an electrical parameter that characterizes the substrate's overall resistivity, assuming a homogeneous structure (see **Figure 2.4(b)**).

The extracted C and G from **Equation 2.10** and **Equation 2.9** are called measured data, they are not 100 % related to the substrate. They contain both environments on top and bottom of the CPW line, they are called C_{air} and G_{air} for the top environment, and C_{sub} and G_{sub} for the bottom environment, see **Figure 2.4**. These contributions are expressed as:

$$C_{\mathrm{data}} = C_{\mathrm{air}} + C_{\mathrm{sub}} \tag{2.12}$$

$$G_{\mathrm{data}} = G_{\mathrm{air}} + G_{\mathrm{sub}} \tag{2.13}$$

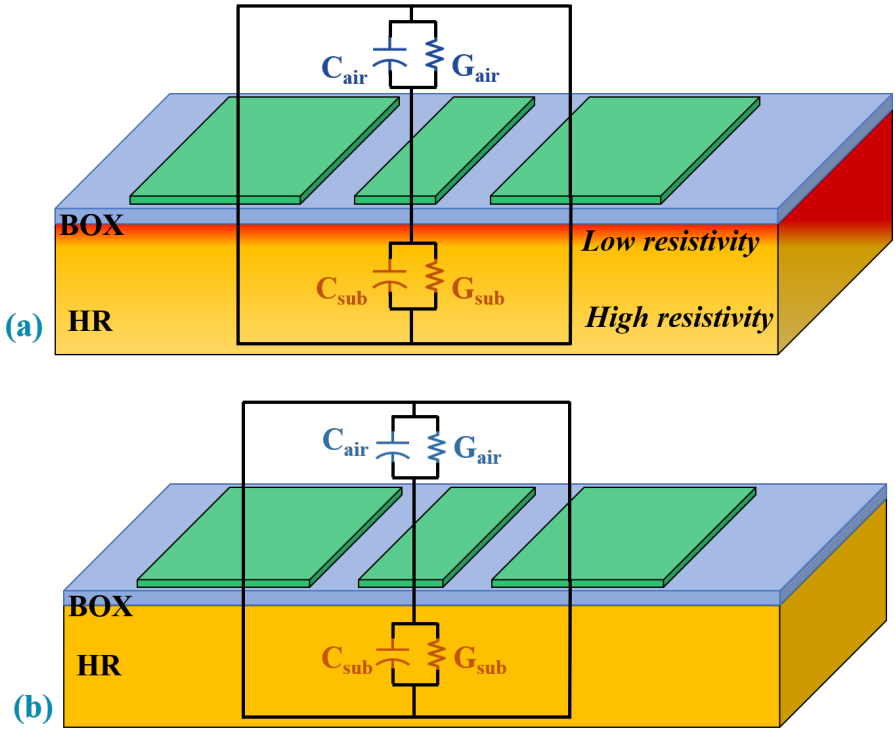


Figure 2.4: CPW transmission line atop of a real inhomogeneous substrate in **(a)** and atop of a modeled homogeneous substrate in **(b)**.

In our study, we are particularly interested in the extraction of the substrate parameters C_{sub} and G_{sub}, which represent the capacitance and conductance of the environment beneath the CPW line, respectively. This analysis assumes that the substrate material is homogeneous. Then, the two above equations are written:

$$C_{sub} = C_{data} - C_{air} \tag{2.14}$$

$$G_{sub} = G_{data} - G_{air} \tag{2.15}$$

Please note that for almost all samples in this thesis, the top material is air,

so $\varepsilon_{r,eff,air}$=1. Then:

$$C_{air} = \varepsilon_0 \varepsilon_{r,eff,air} \times F_{air}(DIMS) \tag{2.16}$$

$$G_{air} = \frac{1}{\varepsilon_{r,eff,air} \times F_{air}(DIMS)} \tag{2.17}$$

$$C_{sub} = \varepsilon_0 \varepsilon_{r,eff,sub} \times F_{sub}(DIMS) \tag{2.18}$$

$$G_{sub} = \frac{1}{\varepsilon_{r,eff,sub} \times F_{sub}(DIMS)} \tag{2.19}$$

Where F_{air} and F_{sub} are a function of the CPW geometrical dimensions and are calculated using Heinrich model in [53].

Finally, the extracted effective resistivity and effective permittivity are written as:

$$\varepsilon_{r,eff,bot} = \frac{C_{data} - \varepsilon_0 \varepsilon_{r,eff,top} \times F_{air}(DIMS)}{\varepsilon_0 \times F_{sub}(DIMS)} \tag{2.20}$$

$$\rho_{eff,sub} = \frac{F_{sub}(DIMS)}{G_{data} - \sigma_{eff,air} \times F_{air}(DIMS)} \tag{2.21}$$

The extraction of effective resistivity will be a recurring focus throughout this thesis, as it represents an important FoM for benchmarking RFSOI substrates. Effective resistivity is a key indicator of substrate performance, particularly in identifying whether the substrate is impacted by PSC and assessing the overall efficiency of RF components.

To provide a comprehensive evaluation of different RFSOI substrates, effective resistivity will typically be plotted against frequency, enabling a detailed analysis of how this parameter changes across the operating spectrum. This approach allows for an in-depth comparison of substrate performance in various RF applications.

2.2 Large-Signal Characterization

In the previous section, a small-signal setup was employed with an input power of -5 dBm to measure the S-parameters of the device, providing a linear analysis of its performance. The S-parameters were measured to understand the device's behavior under low-power conditions, which ensures that the passive device remains within its linear operating range. However, passive devices can exhibit non-linear behavior when subjected to large signals, particularly due to substrate-related effects. In this section, the focus shifts to the non-linear effects observed in a CPW line when exposed to large signal levels, specifically what is the setup used to quantify the generated non-linearities.

To observe these non-linear effects, a large signal will be injected into the CPW line, with the signal power gradually increased until reaching a maximum of 25 dBm. The experiment will use a single frequency of 900 MHz injected at the input of the CPW line, and the output will be monitored for the generation of harmonics. When passive devices, such as a CPW line, are driven with large signals, non-linear behavior often results in the creation of harmonic frequencies that were not present in the input signal. In this case, second and third harmonics will be generated at frequencies of 1.8 GHz and 2.7 GHz, respectively, corresponding to twice and three times the fundamental input frequency of f_0= 900 MHz.

As the input signal power increases, the amplitude of the harmonics H2 at 1.8 GHz and H3 at 2.7 GHz will also rise, indicating the extent of the non-linear effects present in the CPW line. By analyzing the relationship between the input power and the generated harmonic content, a deeper understanding of how the substrate influences the non-linear behavior of the passive device can be gained. Such non-linear effects are particularly important in high-power RF applications, where passive devices must operate reliably without introducing excessive distortion or unwanted harmonics.

2.2.1 Description of the HD 900 MHz On-Wafer Measurement Setup

The large-signal measurement setup used for the extraction of harmonic distortion across all substrates examined in this thesis is shown in **Figure 2.5**. Several key points of the setup are shown from **(a)** to **(g)**, each point will be explained. The main objective is to sweep the power from small-signal levels up to 24

dBm. Since the VNA[1] is unable to reach such high power levels, an RF power amplifier (PA) with a fixed gain is inserted between the output of the VNA and the input of the device under test (DUT), which in this case is a CPW line. The VNA delivers a pure signal at 900 MHz, which is ideal for this application. However, the power sweep of the fundamental is relatively low and insufficient to reach the desired high power levels (see **Figure 2.5(a)**).

After that, the signal at point **(a)** is amplified using the PA, enabling the power sweep to reach high levels around 24 dBm. However, the PA introduces harmonics at 1.8 GHz and 2.7 GHz due to its own non-linearities at point **(b)**. To ensure a clean and purified signal before it is injected into the CPW line, passive band-pass filters are used. These filters allow the 900 MHz signal to pass through while suppressing all other frequencies, resulting in the signal at point **(c)**.

When the pure signal passes through the CPW line, it generates harmonics H2 at $2f_0$ and H3 at $3f_0$ (see **Figure 2.5(d)**). These harmonics are the primary focus of this study. Before analyzing them, it is essential to ensure they are properly received by each receiver of the VNA. The signal at **(d)** is routed through the coupler via Port 4. At this point, the signal is directed to receiver D through a high-pass filter that allows only the frequencies $2f_0$ and $3f_0$ to pass. Attenuator D is set to zero since the fundamental frequency is eliminated, and the harmonic levels are not large enough to damage the VNA. Finally, the signal at **(f)** is received.

At the same time, the signal from **(d)** is directed to point **(e)** and then to **Attenuator B**. It is important to note that setting **Attenuator B** to zero could potentially damage **Receiver B** of the VNA. Therefore, attenuating the fundamental output before it reaches **Receiver B** is crucial. However, it is also important to specify an optimal attenuation value to avoid reducing the fundamental signal below the noise floor of the setup, which would make accurate measurements impossible. A careful choice of the attenuator value ensures the fundamental signal is properly measured at **(g)**.

[1] In our case, we utilize the Keysight PNA-X 26.5 GHz vector network analyzer **[54]**. This same VNA is employed for S-parameter measurements, as referenced in **Section 2.1.1**, and will also be used in the large-signal setup described here.

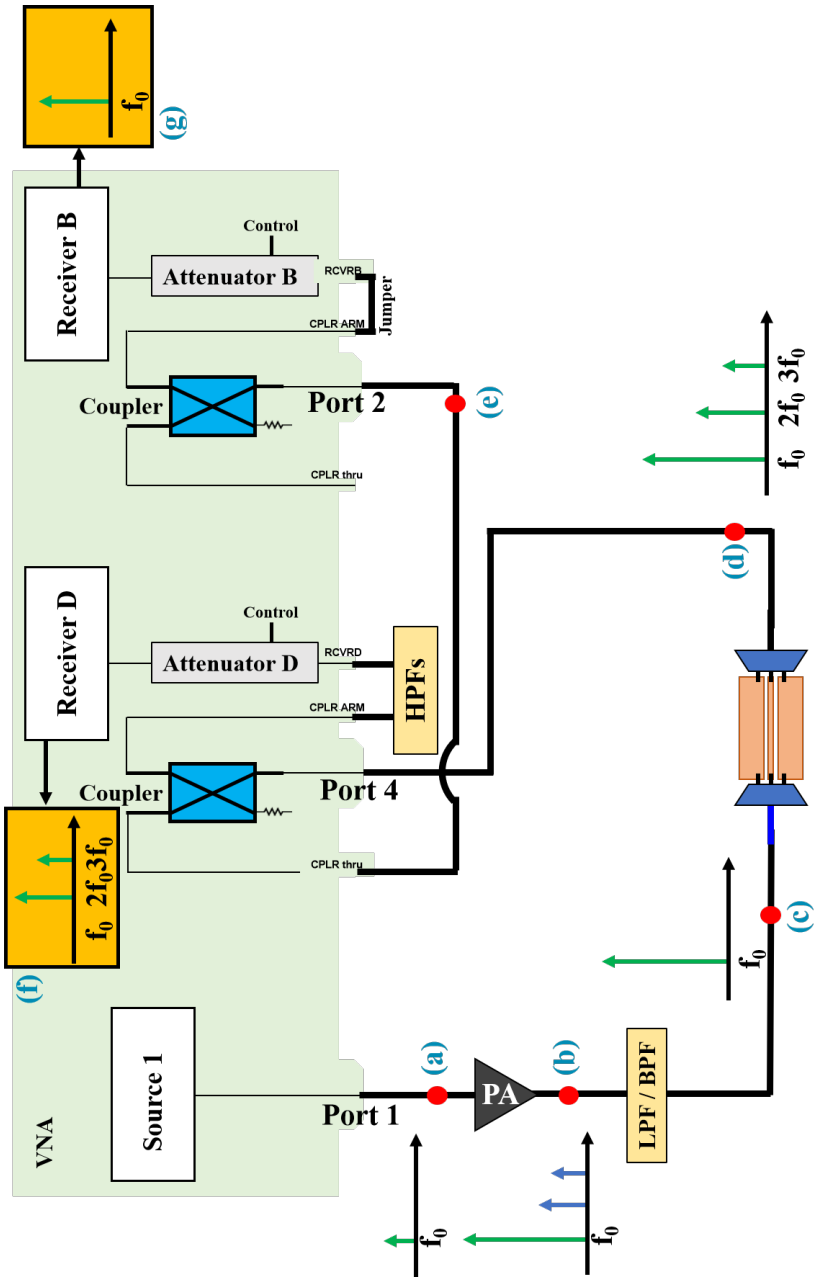


Figure 2.5: Practical setup for the on-wafer harmonic distortion measurement using an RF single-tone signal.

The measurements are performed twice. First, the input power at the DUT is swept, and the fundamental H1 is measured at receiver B. Second, the input power at the DUT is swept again to measure H2 and H3 at receiver D.

2.2.2 eSI70™, eSI80™, eSI90™ and eSI100™

Enhanced signal integrity (eSI™) refers to a trap-rich polysilicon substrate. SOITEC, a company that specializes in advanced substrate technologies, offers several types of eSI™ substrates, including eSI100™ and eSI80™. These different versions of eSI™ are included in their portfolio and address a range of performance requirements. In this subsection, we will explore what the numerical value "X" in eSIX™ represents.

SOITEC has introduced a key performance metric to quantify the substrate's effectiveness in reducing harmonic distortion. This metric involves measuring the second harmonic (H2) in relation to the output power (H1) of a CPW line at a fundamental frequency of 900 MHz. The CPW line used in the measurement is 2.1 mm long and has specific dimensions: a signal width of 26 µm, spacing between the signal and ground track of 12 µm, and a ground width of 208 µm. The measurement is conducted using a large signal setup, similar to the one described in **Section 2.2.1**. At an output power of H1 = 15 dBm and a fundamental frequency of 900 MHz, the extracted H2 value is aligned with the expected performance of the eSIX™ substrate as depicted in **Figure 2.6**. Where usually H2 at H1=15 dBm is close to -70, -80, -90 and -100 dBm.

The CPWline with the dimensions outlined above, often referred to as **LineCsetC**, is widely regarded as a standard benchmark for evaluating RFSOI substrates **[55]**. Its consistent use across various studies and industry applications stems from its ability to provide reliable and repeatable measurements that are critical for comparing different substrate technologies. For this reason, throughout this thesis, a considerable number of studies on CPWs use the LineCsetC as a reference. By maintaining the same CPW line, researchers and engineers are able to directly compare performance metrics such as harmonic generation across various substrate types, including high-resistivity substrates and trap-rich substrates.

Additionally, it has become a well-established practice to benchmark the second harmonic (H2) generated by a CPW at an output power of H1 = 15 dBm, even when the specific CPW line under test is not LineCsetC. This standardized output power is often used as a point of reference because it provides a consistent basis for comparison across different designs and materials. Benchmarking at H1 = 15 dBm allows for a better understanding of how different

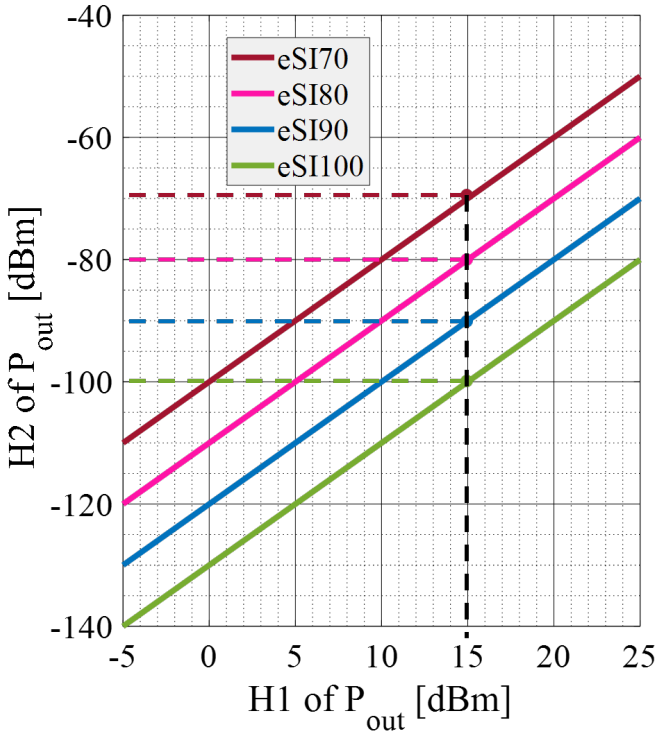


Figure 2.6: Simulated second harmonic values for various eSI™ substrates at an output power of H1 = 15 dBm with a fundamental frequency of 900 MHz.

substrates perform in high-power RF environments, which is particularly useful for applications in mmWave and 5G technologies, where harmonic distortion can severely degrade signal quality.

The combination of LineCsetC's widespread adoption and the standardized measurement of second harmonic distortion has allowed it to become a crucial tool for characterizing and benchmarking RFSOI substrates. Whether the CPW line in use is LineCsetC or a variant with different dimensions, the practice of measuring H2 at H1 = 15 dBm remains a key metric for substrate evaluation. This consistency not only enhances the comparability of results across different studies but also ensures that the substrate's ability to minimize unwanted harmonics is accurately assessed.

2.3 Conventional Trap Modeling in Polysilicon

The characteristics of polysilicon traps are of particular relevance in this study, as they play a key role in the small- and large-signal modeling of trap-rich RF substrates.

2.3.1 Continuous Trap Distribution

The total density of traps is assumed to consist of four bands: two tail bands (a donor-like valence band and an acceptor-like conduction band) and two deep-level bands (one acceptor-like and the other donor-like), all of which are modeled using a gaussian distribution [35, 56–60] and is given by:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \tag{2.22}$$

Where E is the trap energy, Ec is the conduction band energy, Ev is the valence band energy and the subscripts (T, G, A, D) stand for tail, gaussian, acceptor and donor states, respectively. Each element of the Equation 2.22 is given by the Equation 2.23 to Equation 2.26 and are graphically represented in Figure 2.7.

$$g_{GA}(E) = NGA \cdot \exp\left\{-\left(\frac{EGA - E}{WGA}\right)^2\right\} \left[cm^{-3} \cdot eV^{-1}\right] \tag{2.23}$$

$$g_{GD}(E) = NGD \cdot \exp\left\{-\left(\frac{EGD - E}{WGD}\right)^2\right\} \left[cm^{-3} \cdot eV^{-1}\right] \tag{2.24}$$

$$g_{TA}(E) = NTA \cdot \exp\left\{\frac{E - E_C}{WTA}\right\} \left[cm^{-3} \cdot eV^{-1}\right] \tag{2.25}$$

$$g_{TD}(E) = NTD \cdot \exp\left\{\frac{E_V - E}{WTD}\right\} \left[cm^{-3} \cdot eV^{-1}\right] \tag{2.26}$$

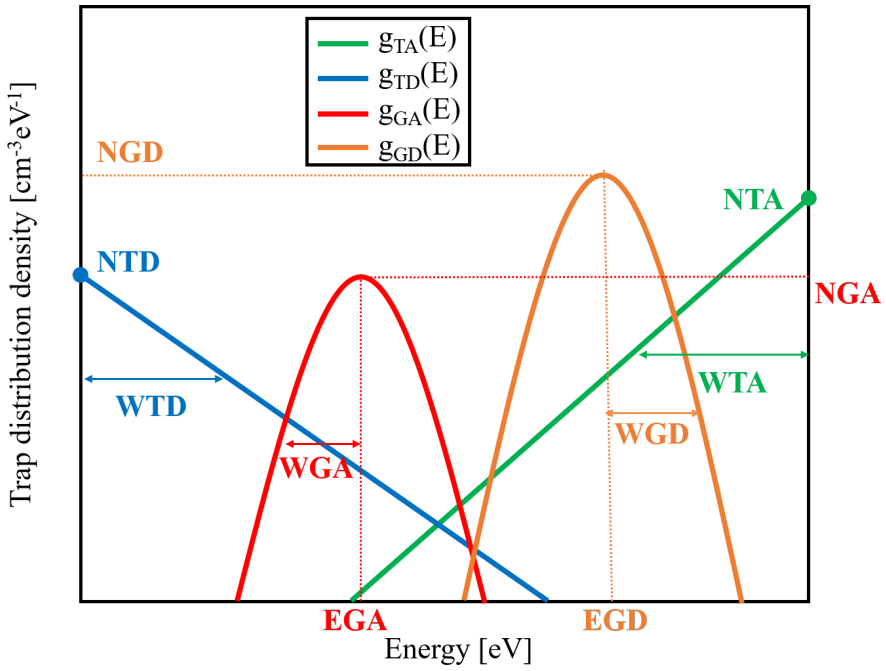


Figure 2.7: The shape of the four types of trap distributions used to model the polysilicon.

The values typically associated with NTA and NTD for polysilicon are generally in the range of 10^{20} to 10^{22} cm^{-3}eV^{-1} [56, 60], while NGA and NGD usually fall between 10^{15} and 10^{18} cm^{-3}eV^{-1}.

Table 2.1 provides the values of all parameters used from [56] to model the polysilicon trap distributions, as described by Equation 2.23 to Equation 2.26. Table 2.2 presents the capture cross-sections for electrons and holes across the four families of traps considered.

Table 2.1: Typical tail and gaussian trap distribution parameters for polysilicon, as reported in [56].

Parameter	Description	Value
NGA	Peak value of the Gaussian acceptor trap distribution $g_{GA}(E)$	$1.5 \cdot 10^{15}$ cm^{-3}/eV
EGA	Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution $g_{GA}(E)$	0.62 eV
WGA	Characteristic decay energy of the Gaussian acceptor trap distribution $g_{GA}(E)$	0.15 eV
NGD	Peak value of the Gaussian donor trap distribution $g_{GD}(E)$	$1.5 \cdot 10^{15}$ cm^{-3}/eV
EGD	Energy position from the valence band edge of the peak of the Gaussian donor trap distribution $g_{GD}(E)$	0.78 eV
WGD	Characteristic decay energy of the Gaussian donor trap distribution $g_{GD}(E)$	0.15 eV
NTA	Value of the Tail acceptor trap distribution $g_{TA}(E)$ at the conduction band edge	$1.0 \cdot 10^{21}$ cm^{-3}/eV
WTA	Characteristic decay energy of the Tail acceptor trap distribution $g_{TA}(E)$	33 meV
NTD	Value of the Tail donor trap distribution $g_{TD}(E)$ at the valence band edge	$1.0 \cdot 10^{21}$ cm^{-3}/eV
WTD	Characteristic decay energy of the Tail donor trap distribution $g_{TD}(E)$	49 meV

Table 2.2: Typical capture cross-sections of tail and gaussian-type trap distributions associated with polysilicon, as reported in [56].

Parameter	Description	Value
σ_{GAe}	Capture cross-section for electrons of the acceptor traps of the Gaussian distribution.	$2.0 \cdot 10^{-16}$ cm^2
σ_{GAh}	Capture cross-section for holes of the acceptor traps of the Gaussian distribution.	$2.0 \cdot 10^{-15}$ cm^2
σ_{GDe}	Capture cross-section for electrons of the donor traps of the Gaussian distribution.	$2.0 \cdot 10^{-15}$ cm^2
σ_{GDh}	Capture cross-section for holes of the donor traps of the Gaussian distribution.	$2.0 \cdot 10^{-16}$ cm^2
σ_{TAe}	Capture cross-section for electrons of the acceptor traps of the Tail distribution.	$1.0 \cdot 10^{-17}$ cm^2
σ_{TAh}	Capture cross-section for holes of the acceptor traps of the Tail distribution.	$1.0 \cdot 10^{-15}$ cm^2
σ_{TDe}	Capture cross-section for electrons of the donor traps of the Tail distribution.	$1.0 \cdot 10^{-15}$ cm^2
σ_{TDh}	Capture cross-section for holes of the donor traps of the Tail distribution.	$1.0 \cdot 10^{-17}$ cm^2

2.3.2 Discrete Trap Distribution

In addition to continuous trap distributions, certain materials introduce discrete traps within the silicon bandgap. As will be explored later in this thesis, elements such as gold, carbon, and germanium are known to create discrete traps, each with unique properties. Unlike continuous distributions, where traps are spread across a range of energy levels, discrete traps exist at specific energy levels within the bandgap. These traps can significantly influence the electrical behavior of devices, particularly in terms of charge trapping.

In such cases, each discrete trap can be modeled as either an acceptor or a donor, depending on whether it tends to accept or donate charge carriers. Its position is defined relative to either the valence or conduction band, depending on whether it interacts with holes or electrons as depicted in **Figure 2.8**.

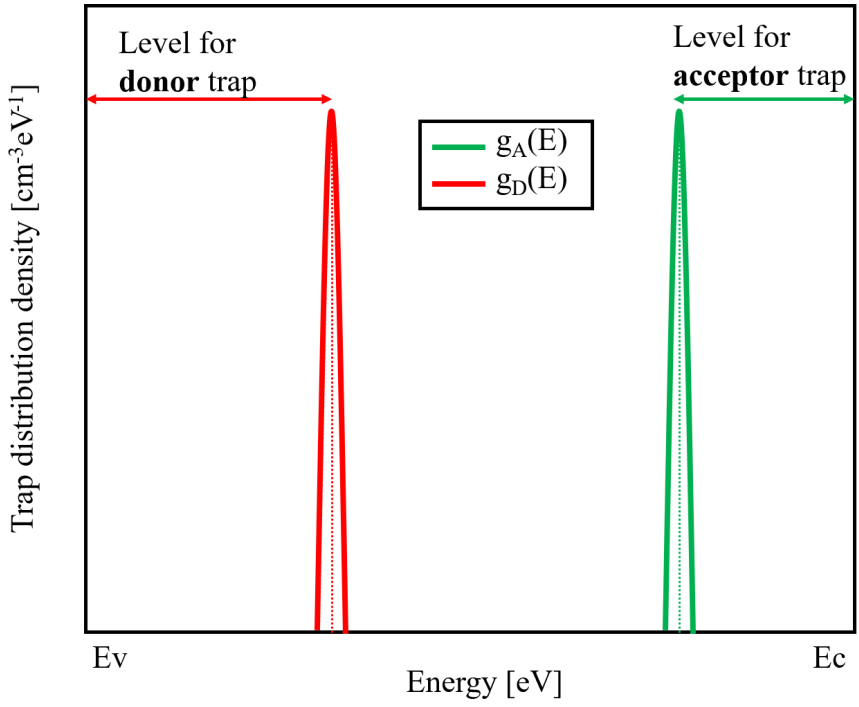


Figure 2.8: Discrete trap modeling definition as described in [56].

The two *pseudo-gaussian* distributions shown in **Figure 2.8** could be ex-

pressed using the following equation:

$$g(E) = g_A(E) + g_D(E) \tag{2.27}$$

Where $g_A(E)$ and $g_D(E)$ could be written as:

$$g_A(E) = N_A \cdot \delta(E - E_A) \left[cm^{-3} eV^{-1}\right] \tag{2.28}$$

$$g_D(E) = N_D \cdot \delta(E - E_D) \left[cm^{-3} eV^{-1}\right] \tag{2.29}$$

It is worth noting that the representations of $g_A(E)$ and $g_D(E)$ with finite widths, as shown in Figure **Figure 2.8**, are provided to aid the reader's comprehension. These visualizations are meant to illustrate the concept of energy distributions for acceptor-like and donor-like traps in the material. However, in the TCAD Atlas simulations, these distributions are not modeled with finite widths but are instead treated as Dirac delta functions, as described by **Equation 2.28** and **Equation 2.28**. This simplification in the simulation assumes that the traps are localized at specific energy levels without any spread.

So far, only one donor and one acceptor trap have been considered. However, certain materials, such as porous silicon, which will be discussed later in this thesis, introduce multiple discrete acceptor traps and multiple discrete donor traps. In these cases, the formulation presented in **Equation 2.27** will need to be adjusted to account for the presence of multiple discrete trap levels, both donor- and acceptor-like:

$$g(E) = k \cdot g_A(E) + m \cdot g_D(E) \tag{2.30}$$

Where k is the number of discrete acceptor traps and m is the number of discrete donor traps.

2.4 Polysilicon Modeling Using PICTS method

The method described in Section 2.3 is based on measurements of polysilicon used in TFT transistors. It provides a good model for the trap-rich substrate, as will be further discussed in this thesis. However, the quantification of traps in an undoped polysilicon trap-rich layer used for RF applications has not yet been performed. In this section, after quantifying the activation energy of traps in the polysilicon trap-rich layer using the photo-induced current transient spectroscopy (PICTS) measurement method[2], a model of the polysilicon is presented. This model incorporates the measured trap activation energy and is then fitted to both small- and large-signal measurements of the CPW line.

2.4.1 PICTS Measurement Method

Figure 2.9(a) shows the schematic view of the setup in order to extract the PICTS signal. The sample is put on the thermal stage inside cryostat. The light is provided using light emitting diodes (LED) of a given wavelength λ (λ= 940 nm in this paper). DC generator is used to provide a pulse signal V_p in order to illuminate the sample during the filling time t_p. Those three parameters λ, V_p and t_p are characterizing the LED. The sample is a Schottky diode that is always reverse-biased through a DC bias V_R is applied to the front side of the studied sample. When the sample is not illuminated the decreasing current depicted in Figure 2.9(b) is saved, where t_0 (5 ms) is the cut-off time and T_w (100 ms) is the measurement time. The first order of the sine coefficient of the fast Fourier transform (FFT) is considered at each temperature in order to build the PICTS spectrum as in [68] (Figure 2.9(c)). The temperature is swept from 150 to 300 K in heating-up mode [61].

[2]The working principle of begins with cooling the semiconductor sample to a low temperature. The sample is then illuminated with a light pulse or a continuous light source, which excites electrons from deep-level traps in the bandgap into the conduction band, creating a non-equilibrium condition. After the illumination is switched off, the sample is allowed to return to equilibrium as electrons are recaptured by the deep-level traps. During this process, transient currents are generated as the charges (electrons or holes) move back and recombine. These transient currents are measured over time using sensitive electronic equipment. The process of illumination and transient current measurement is repeated at various temperatures. As the temperature increases, the emission rate of the trapped charges rises due to thermal activation, enabling the observation of different trap energy levels. More details about the PICTS measurement method can be found in [61–67].

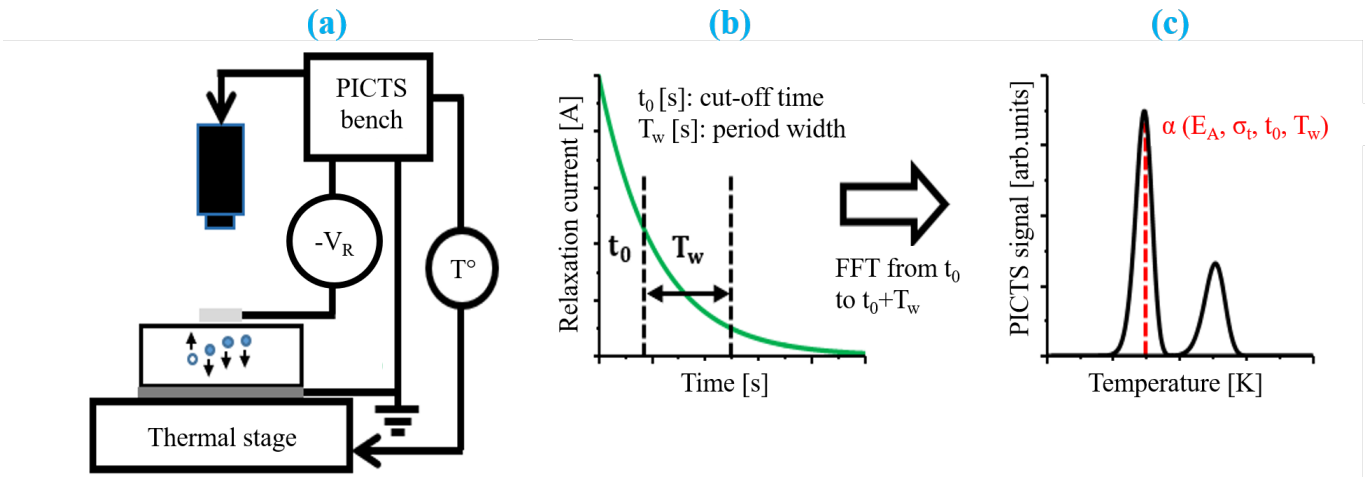


Figure 2.9: Schematic of the PICTS setup testbench used in this paper, in **(a)** the thermal stage is varied between 150 and 300 K, the sample is always reverse biased by V_R and the sample is illuminated using a LED. After extraction of the relaxation current versus time in **(b)**, the PICTS signal is deduced through fast Fourier transform in **(c)** **[61]**.

2.4.2 Substrates Description

Figure 2.10(a) illustrates the substrates utilized for RF characterization (fabrication and SRP are performed at Cea-Leti) and the method employed for the spreading resistivity profile (SRP) in **Figure 2.10(b)**. Three HR Si wafers served as the handle silicon substrate, followed by a two-step low pressure chemical vapor deposition (LPCVD) polysilicon deposition process. Initially, a 1 µm layer without chemical and mechanical polishing (CMP) was deposited, succeeded by a 0.65 µm layer with CMP. The sample labeled A0 underwent no annealing, while samples A900 and A1100 were annealed for two hours each at 900 and 1100 °C, respectively, to explore the effects of annealing steps commonly found in conventional CMOS process flows.

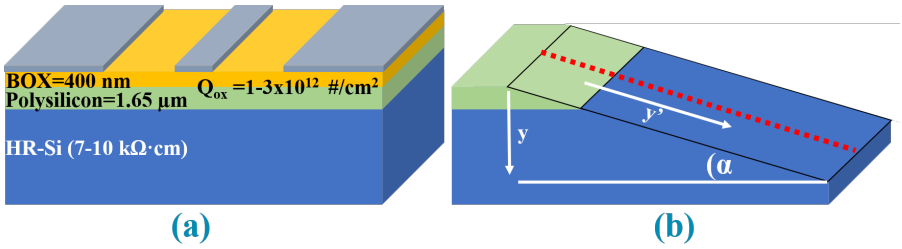


Figure 2.10: (a) 3D-view of the fabricated CPW lines, **(b)** bevel angle along which the SRP was performed.

Subsequently, a 400 nm insulating layer of SiO_2 was deposited on each wafer, followed by the deposition and patterning of a 1 µm-thick aluminum layer to define a 2.1 mm-long CPW line. The CPW line features the following geometry: a signal track width Wc of 26 µm, a spacing S of 12 µm between the signal and ground electrodes, and ground electrode width Wg of 208 µm. The density of positive oxide charges Qox was extracted using CV measurements (performed at UCLouvain) and is estimated to be around 1-3 $\times$ 10^{12} cm^{-2}. SRP was conducted along a bevel angle of 16° along the y' axis as depicted in **Figure 2.10(b)**.

Figure 2.11 displays the SRP measurements (performed at Cea-leti) of the substrates A0, A900, and A1100 as described earlier. A significant variation in local resistivity within the polySi layer is observed, likely attributable to contaminations.

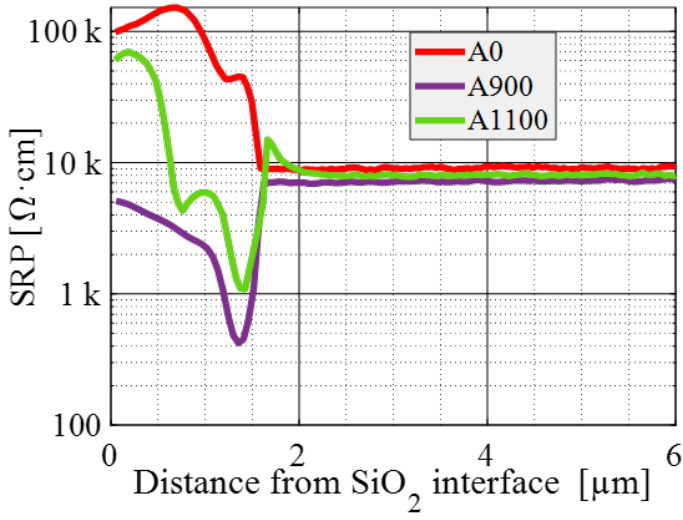


Figure 2.11: Resistivity profile as a function of the depth in the different trap-rich substrates: A0 not annealed, A900 and A1100 annealed, respectively, at 900 and 1100 °C.

Figure 2.12 illustrates boron (green color) and phosphorus (blue color) contaminations extracted via secondary ion mass spectroscopy (SIMS) for the three studied substrates. Sample A0 (**Figure 2.12(a)**) exhibits minimal contamination, with only two peaks of boron impurities at approximately 3×10^{15} cm^{-3} at depths of 0.65 µm and 1.65 µm. Substrate A900 (**Figure 2.12(b)**) displays a boron contamination of approximately 5×10^{14} cm^{-3} across the entire polysilicon layer, while it is approximately 3×10^{15} cm^{-3} for A1100. . It is important to note that the detection threshold for boron (Bth) is around 3×10^{13} cm^{-3}, and for phosphorus (Pth) is around 1.5×10^{15} cm^{-3}, exclusively due to the measurement setup. Boron and phosphorus impurities originate from the intrinsic doping of the handle Si substrate, as well as contaminants in the furnaces and clean room environment. During the annealing steps, impurities diffuse and redistribute within the polysilicon layer.

2.4.3 Polysilicon Discrete Traps Modeling

Various methods have been employed over the past 20 years to quantify trap activation energy levels, including Deep Level Transient Spectroscopy (DLTS)

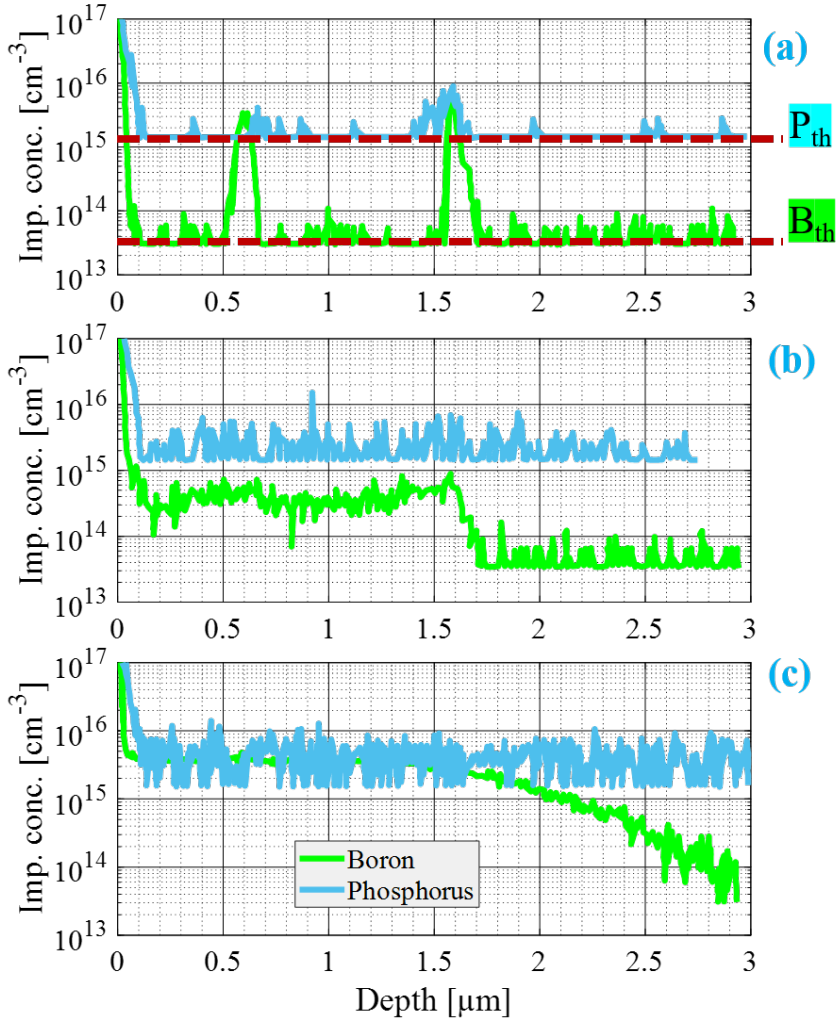


Figure 2.12: Phosphorus and boron impurity concentration (imp. conc.) as a function of the depth in the polysilicon layer for the substrates **(a)** A0, **(b)** A900 and **(c)** A1100. The red dashed lines show the detection threshold for boron and phosphorus.

and PICTS methos. PICTS has demonstrated its efficiency in extracting trap positions within the silicon bandgap, particularly for gold-doped silicon substrates **[61]**. Same method was performed on the previously described substrates and

the spectrum results are shown in **Figure 2.13**.

Figure 2.13 displays the PICTS spectrum signal for the substrates A0, A900, and A1100. The entire spectrum, depicted in black, is modeled by one or multiple discrete traps in a manner that the sum of all peaks can replicate the measured spectrum **[61]**. There are five discrete levels of traps that can be considered to replicate the spectrum of the three silicon-based substrates A0, A900 and A1100. These trap levels, denoted as P1, P2, P3, P4, and P5, have peaks at temperatures of 269 K, 257 K, 242 K, 230 K, and 215 K, respectively. From this experiment, it can be concluded that there is no change in the activation energy of traps during the annealing of the polysilicon. The parameters σ_n, σ_p, activation energy of the traps Ea and the extraction methods are summarized in **Table 2.3**[3].

Table 2.3: Activation energies, their associated parameters and extraction methods for the three analyzed substrates: A0, A900 and A1100.

	T_{peak} [K]	E_A [eV]	σ_n [cm^2]	σ_p [cm^2]	Type
P1	269	0.485	1.0×10^{-15}	3.3×10^{-16}	Acceptor
P2	257	0.474	1.6×10^{-15}	5.2×10^{-16}	Donor
P3	242	0.42	5.3×10^{-16}	1.7×10^{-16}	Donor
P4	230	0.334	5.3×10^{-16}	1.7×10^{-16}	Donor
P5	215	0.31	5.3×10^{-16}	1.7×10^{-16}	Donor

The PICTS method has proven effective in extracting the activation energies associated with traps present within the polysilicon layer, as evidenced in **[61]**. This technique offers valuable insights into the energy levels of individual traps, facilitating a deeper understanding of their behavior within the semiconductor material.

[3]The main focus of this part of the thesis is to utilize the PICTS measurements and their modeling, which were conducted at CEA-Leti by another researcher. While the measurements themselves are not the primary focus of this thesis, they play a crucial role in supporting the analysis and modeling of the trap-rich polysilicon layer presented here.

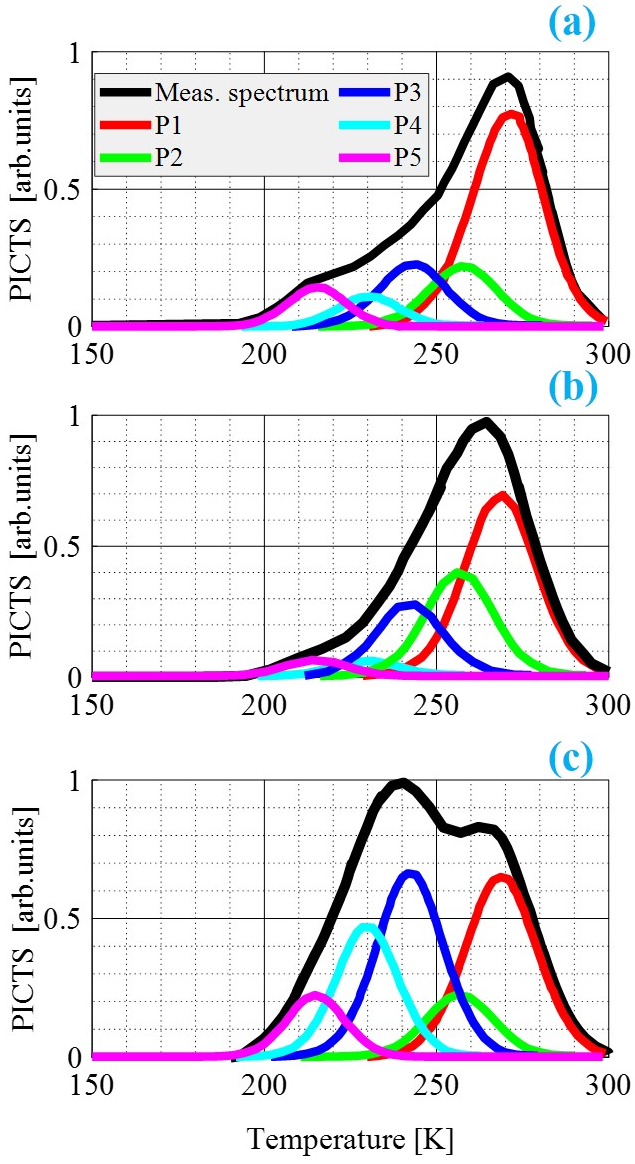


Figure 2.13: Spectrum of the studied samples in black and their activation energy modeling (P1-P5): **(a)** A0, **(b)** A900, and **(c)** A1100.

However, while PICTS excels in characterizing activation energies, determining the density and spatial distribution of traps using this method presents significant challenges. PICTS primarily focuses on analyzing transient current signals generated by trap states within the material. While these signals provide valuable information about the energy levels of traps, they offer limited insights into trap density and spatial distribution throughout the semiconductor structure. Additionally, factors such as device geometry, material composition, and measurement conditions can further complicate the interpretation of PICTS data in relation to trap density and distribution.

To address these challenges and gain a more comprehensive understanding of trap behavior, complementary techniques such as computer simulations become essential. In the subsequent section of this paper, Atlas Silvaco simulation software is used in order to propose trap density and spatial distribution within the polySi layer.

2.4.4 Spatial Traps Distribution

To evaluate the impact of the trap-rich (TR) layer on the RF behavior of the substrates, Atlas Silvaco TCAD simulations were conducted for the CPW line illustrated in **Figure 2.14**.

The simulations were performed under specific conditions: the density of positive oxide charges Q_{ox} in the buried oxide was set to 3×10^{12} cm^{-2} , and the polySi layer was modeled based on the trap positions within the silicon bandgap, as detailed in **Table 2.3** Additionally, the simulator accounted for the presence of unwanted contaminations, such as boron and phosphorous, introduced into the polySi region, as illustrated in **Figure 2.12**.

An essential aspect of the simulations was the depiction of trap density throughout the thickness of the polysilicon layer, as shown in **Figure 2.15**. These simulations provided insights into how the presence and distribution of traps within the polySi layer influence the RF behavior of the substrates.

Figure 2.15 illustrates the distribution of acceptor traps in the Y direction within the polySi region. Only the distribution of acceptor traps is presented, while the distribution of other types of traps can be inferred using the ratio described in **Figure 2.13**. The modeling of the traps considers a constant density at specific depths of 0.15, 0.35, 0.65, 1.1, and 1.65 µm.

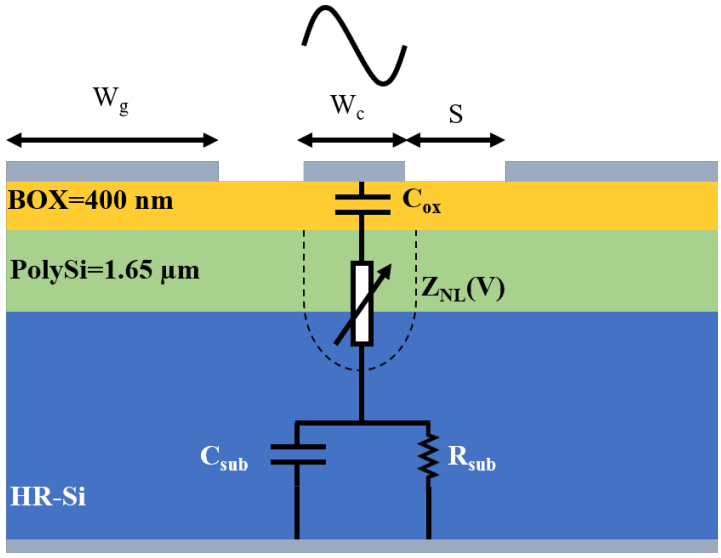


Figure 2.14: Simplified equivalent circuit of a CPW line under small- and large-signal excitation. The impedance Z_{NL} is the non-linear impedance modelled during the large-signal excitation. This impedance is in series with capacitance and resistance of the bulk substrate.

The spatial distribution in **Figure 2.15** is proposed based on several iterations aimed at accurately fitting the measurements of SRP, effective resistivity, and linearity. These iterations are critical for refining the model to ensure it closely reflects the experimental results. Furthermore, it is important to note that the recrystallization effect is expected to be more pronounced at the polySi-bulk interface than at the BOX-polySi interface. Consequently, it becomes essential to identify a decreasing trend in the trap density along the Y direction, from the polySi-bulk interface toward the BOX.

For substrate A0, the distribution exhibits a decrease from 4×10^{18} cm^{-3} to 1×10^{17} cm^{-3}. This diminishing trend can be attributed to a low recrystallization process occurring during polysilicon deposition at approximately 625 °C. Recrystallization occurs when a polycrystalline structure comes into physical contact with a monocrystalline structure, leading the former to mimic the latter under high temperature conditions [69]. It is noteworthy that monocrystalline

structures have lower trap densities, hence the reduced densities observed closer to the bulk silicon (where y=0 represents the SiO_2-polysilicon interface, and y=1.65 µm denotes the polySi-Si bulk interface).

Substrate A900 exhibits a distribution ranging from 3.5×10^{18} cm^{-3} to 4×10^{15} cm^{-3}. At the SiO_2-polysilicon interface, the traps density is nearly identical to that of A0, at around 3×10^{18} cm^{-3}, indicating minimal impact from the recrystallization process in this region. However, beyond 0.65 µm, the traps density drops below 1×10^{16} cm^{-3}, indicative of a highly recrystallized region with fewer traps.

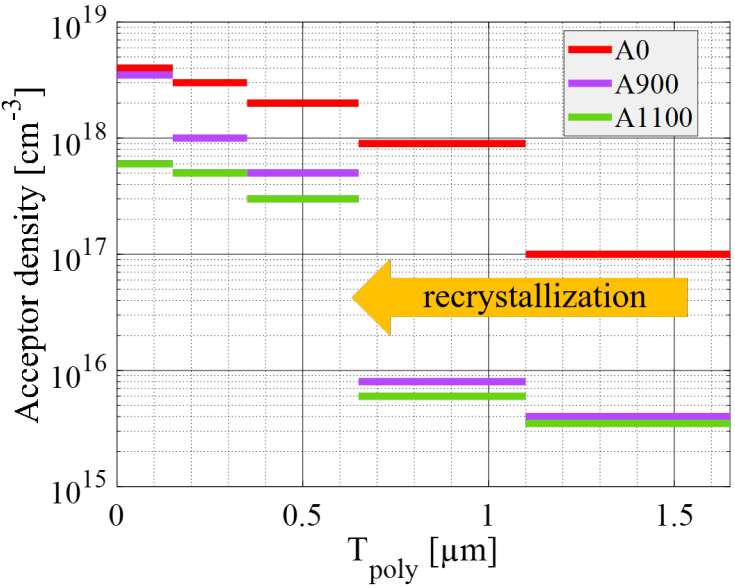


Figure 2.15: Spatial distribution of the traps in the polySi layer for acceptor traps versus the distance from the insulating layer for the studied substrates A0, A900 and A1100.

Substrate A1100 demonstrates a distribution spanning from 6×10^{17} cm^{-3} to 3.5×10^{15} cm^{-3}. Near the polySi-bulk interface, the traps density is comparable to that of A900, attributed to recrystallization effects. Conversely, at the SiO_2-polySi interface, the density decreases to approximately 6×10^{17} cm^{-3}, which is five times lower than A900. This decline is attributed to the gradual reduction in traps density induced by the recrystallization process, progressing

from right to left (from the bulk side towards the SiO_2 interface).

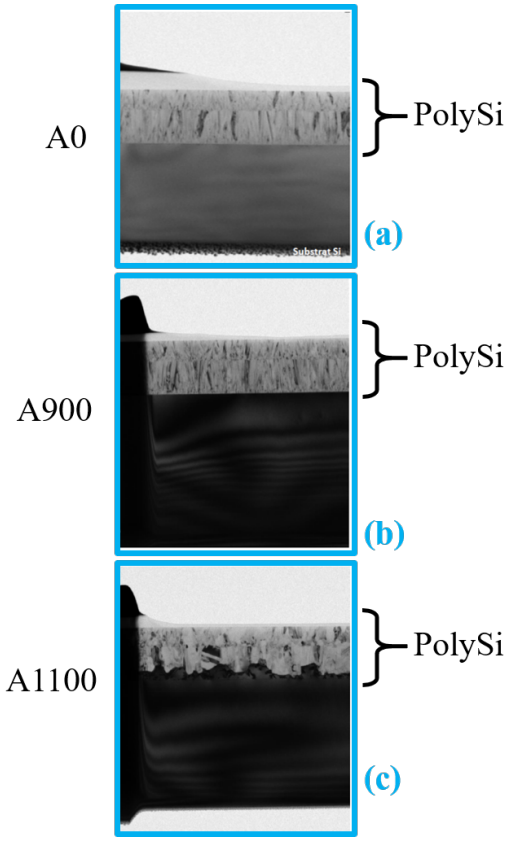


Figure 2.16: TEM images of a trap-rich sample subjected to different thermal annealing steps.

The recrystallization is visible to the naked eye in **Figure 2.16**, where the polysilicon exhibits larger grain sizes for the A1100 compared to the A900, which shows smaller grains but at a higher density.

2.4.5 Polysilicon RF Performance Simulations

Throughout this part of this thesis, careful consideration has been given to several key parameters to comprehensively model the substrate:

- The substrate's bulk resistivity has been set at approximately 8 $k\Omega \cdot cm$;
- Positive oxide charges have been quantified, with Q_{ox} values ranging from 1 to 3×10^{12} cm^{-2};
- The presence of contamination in the various substrates has been examined, as illustrated in **Figure 2.12**;
- Trap positions within the silicon bandgap have been precisely determined and presented in **Table 2.3**;
- A spatial distribution and density of traps within the polySi layer have been proposed, providing valuable insights into trap behavior, as depicted in **Figure 2.15**;
- Additionally, passive device CPW transmission lines have been constructed on each substrate to facilitate further analysis, as shown in **Figure 2.14**;

In the subsequent subsections, the RF figures of merit, including SRP, effective resistivity, and harmonic distortion, were measured and analyzed for each substrate. Simulations were also conducted to comprehensively model the substrate's behavior. The alignment of simulations with measured data was successfully demonstrated by utilizing information obtained from previous sections, thereby deepening the understanding of substrate characteristics and RF performance.

Fitting of the SRP Profile

Figure 2.17 displays the measured (solid line) and simulated (dashed line) SRP as a function of the distance from the insulating layer. For substrate A0, the polySi resistivity remains above 100 $k\Omega \cdot cm$ up to 0.5 µm, then decreases to around 8 $k\Omega \cdot cm$ at 1.65 µm. This decline is attributed to the absence of traps in the silicon bulk.

Substrate A900 exhibits a dip around 1.3 µm-deep, with a local resistivity of 400 $\Omega \cdot cm$, where the simulations align closely with the measurements. This dip is attributed to phosphorus contamination in the polysilicon region. However, significant discrepancies between measurements and simulations are observed at the SiO_2-polysilicon interface, possibly due to unreliable measurements for this substrate. Given that all substrates have uniform thicknesses and

substrate A1100 exhibits high resistivity at 0 µm, substrate A900's resistivity should fall between 60 and 100 kΩ · cm.

Substrate A1100 displays two dips at 0.7 and 0.4 µm, with local resistivities of 4.3 and 1 kΩ · cm, respectively, fitting well with simulations. Both phosphorus and boron contaminations are present in this substrate, contributing to these observed dips.

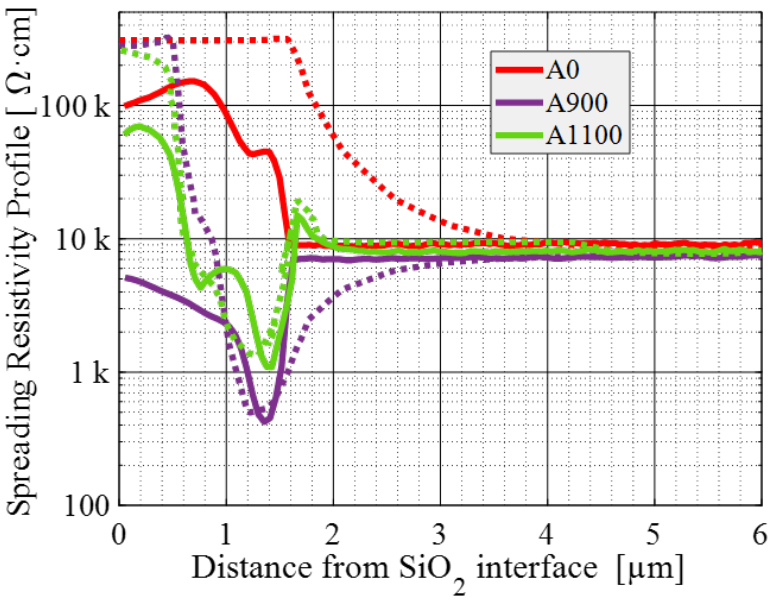


Figure 2.17: Measured and simulated local resistivity as a function of the depth in the polySi region for the studied substrates A0, A900 and A1100. Measurements are in solid line while the simulations are in dashed lines.

Fitting of the Effective Resistivity

To extract the effective resistivity of the studied substrates, small-signal measurements were conducted using a 2-port Performance Network Analyzer (PNA)-X and a pair of Ground-Signal-Ground (GSG) |Z| probes with a 100 µm-pitch. The S-parameters of the CPW (2 ports device) were measured and utilized to extract the equivalent RLCG (resistance inductor capacitor conductance) model of the CPW line. This model was then employed to derive the effective resistivity.

Measurements were carried out for various DC bias points applied to the central conductor of the CPW line relative to a 0 V reference voltage, which was set at both the wafer back-side substrate contact and the lateral ground lines of the CPW.

Figure 2.18 illustrates the extraction of the effective resistivity above the slow-wave mode as a function of the applied DC bias voltages for the three different substrates. The simulations closely align with the measurements. Substrate A0 exhibits an effective resistivity of approximately 30 $k\Omega \cdot cm$ across the entire DC bias range, with the Fermi level deeply pinned within the silicon mid-gap.

Substrate A900 demonstrates an effective resistivity of around 12 $k\Omega \cdot cm$ throughout the DC bias range, with the Fermi level pinned near the silicon mid-gap. This can be attributed to a lower density of traps compared to substrate A0 (see **Figure 2.15**).

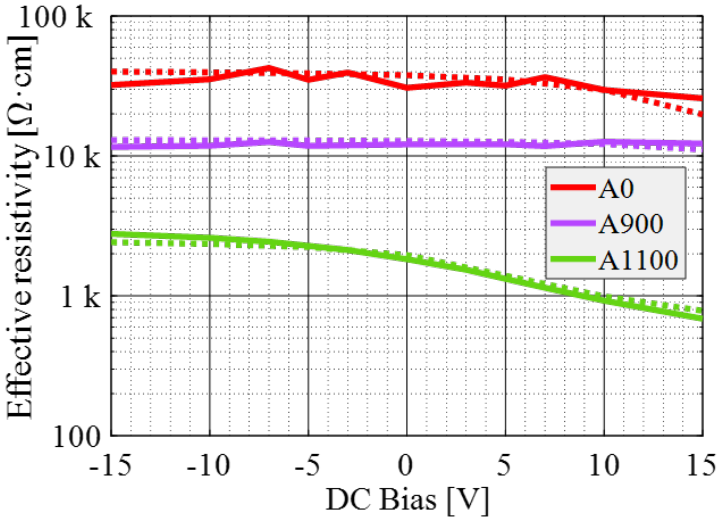


Figure 2.18: Measured and simulated effective resistivity as a function of the applied DC bias for the different substrates (measurements in solid line while the simulations are in dashed line). The effective resistivity was extracted at 2 GHz.

Substrate A1100 displays a varying effective resistivity, ranging from 1.8 k$\Omega \cdot$cm to 687 $\Omega \cdot$cm, depending on the bias. Unlike in the cases of substrates A0 and A900, the Fermi level in A1100 is not pinned. Positive bias points affect much more the effective resistivity, reducing it to 687 $\Omega \cdot$cm. Overall, the density of traps for A1100 is lower compared to A900 and A0 due to the partial recrystallization effect in polySi.

Fitting of the Harmonic Distortion

To assess the linearity of the CPW lines described above, a harmonic distortion (HD) setup was implemented using a single tone of 900 MHz injected into one port of the CPW line (with power ranging from -15 to 24 dBm). Subsequently, the first (H1 at 900 MHz), second (H2 at 1.8 GHz), and third (H3 at 2.7 GHz) harmonics were measured at the second port of the CPW line. **Figure 2.19** illustrates the level of the second harmonic at an output power of 15 dBm as a function of the applied DC bias. Simulations were conducted using the model outlined in **[36]**

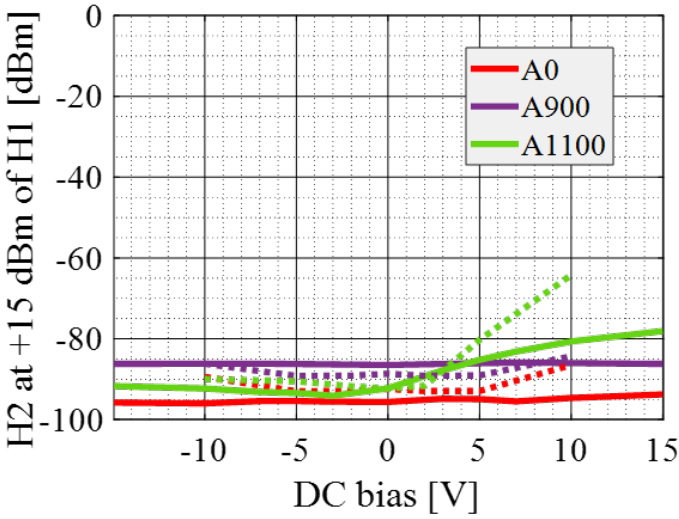


Figure 2.19: Measured and simulated second harmonic at 1.8 GHz at an output power of 15 dBm (at 900 MHz) as a function of the applied DC bias. Measurements are in solid line while the simulations are in dashed line.

Substrate A0 exhibits an H2 level of -95 dBm, similar to conventional

eSI100^{TM} substrate from SOITEC, and remains independent of bias due to the deep pinning of the Fermi level within the silicon bandgap. A900, with lower trap density, yields an H2 level of around -86 dBm, also independent of bias, with the Fermi level pinned near the silicon bandgap. A1100, with even lower trap density, demonstrates variation ranging from -78 to -91 dBm, with the Fermi level unpinned. This aligns with the effective resistivity, which is relatively low (around 1 k$\Omega \cdot$cm) at a bias of 10 V (see **Figure 2.18**).

2.4.6 Discussion

This part underscores the gradual decrease in the trap-rich layer's efficiency during the conventional CMOS process, primarily attributed to contamination and recrystallization, leading to effective resistivities nearing 687 $\Omega \cdot$cm. Despite this, these values continue to yield satisfactory RF performance for passives built on such substrates. Moreover, while a dependency on linearity is observed for the A1100 substrate, it closely aligns with the commercially available eSI80^{TM} at a 15 V DC bias point. Additionally, the A1100 substrate exhibits H2 levels that are 10 dB more linear than the eSI80^{TM} at a 0 V DC bias point at an output power of 15 dBm, showcasing its superior performance. Notably, the second harmonic H2 of the A1100 substrate is 40 dB lower than that of the high-resistivity substrate (not shown in this part) suffering from the PSC effect, highlighting the efficiency of the TR substrate in mitigating harmonic generation.

Currently, the TR substrate finds widespread utilization in the most advanced silicon foundries and is well-integrated into PDSOI technology. This integration has spurred RF designers to develop RF front-end module circuits atop this substrate. A diverse array of RF circuits, including switches **[42, 43]**, power amplifiers **[70]**, low-noise amplifiers **[71]**, and integrated circuits **[72]**, have been successfully designed and implemented on trap-rich substrates, further highlighting the versatility and efficacy of this technology in modern RF design.

Through PICTS measurements, the energy position of traps within the polySi bandgap was successfully extracted using a specialized setup. It was revealed that this type of polySi employed for RF applications harbors five discrete energy levels within the silicon bandgap.

Accounting for unwanted contamination in the trap-rich layer of annealed substrates, the density and spatial distribution of traps were modeled using TCAD software from Silvaco. It was demonstrated that the annealing process induces gradual recrystallization of the polySi layer, thereby reducing the density of traps in the trap-rich layer.

Simulations of the CPW transmission line on conventional SOI substrates were conducted, incorporating comprehensive data from the polySi region. By aligning the simulations with measurements of resistivity profiles, effective resistivity, and harmonic distortion, the efficacy of modeling the trap-rich layer using discrete traps was illustrated.

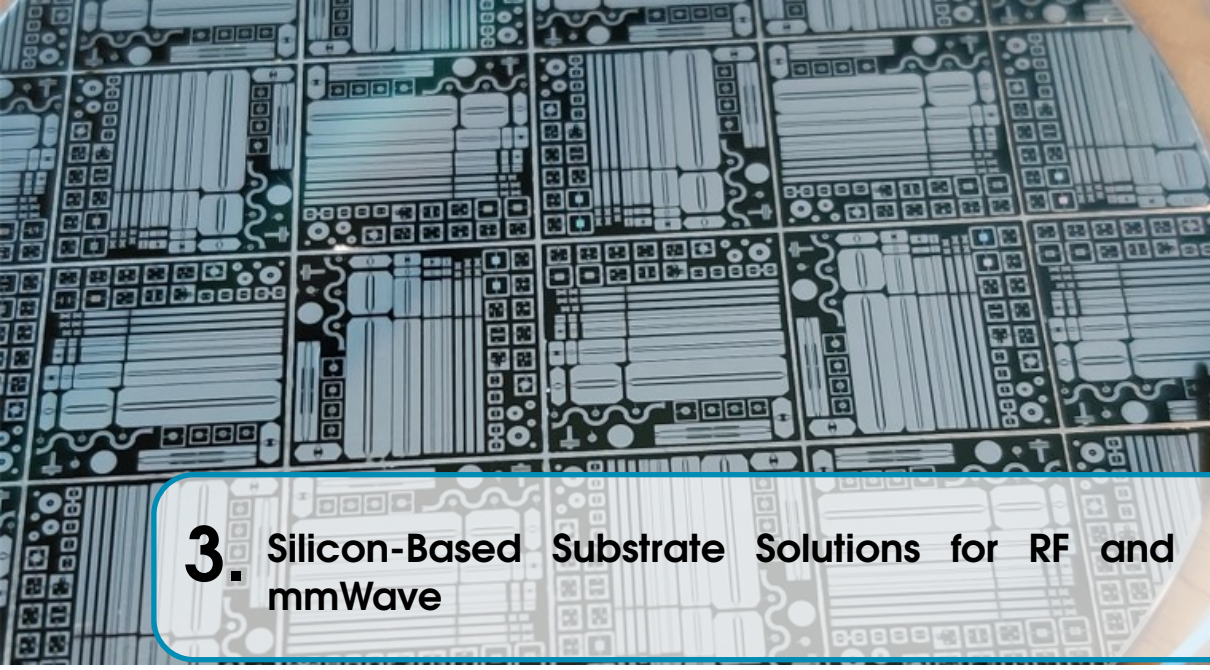
The modeling of the polysilicon layer, based on trap measurements in the silicon bandgap, offers a more realistic approach compared to the traditional continuous distribution modeling derived from TFT transistors. It is important to emphasize that polysilicon in TFTs is typically doped, whereas the polysilicon used in RF applications is undoped, making these two materials significantly different. Furthermore, while Gaussian and tail distributions of traps are often assumed, no direct measurements have been conducted to confirm this. This makes the modeling approach in this work more robust and consistent, as it relies on an experimental method called PICTS, providing direct measurement of trap characteristics.

2.5 Chapter Summary

This chapter outlined the methods that will be employed throughout this thesis. It detailed the process of extracting effective resistivity and explained how the DC bias is applied to the CPW line. Following this, the setup for large-signal measurements was described in detail, including the relevant methodologies used to simulate and fit the substrate measurements. The combined experimental and simulation approaches provide a comprehensive framework for characterizing and understanding the behavior of the substrates under high-power conditions.

A key focus of this chapter was on the methodologies used to study both continuous distributions of traps and discrete trap levels within the substrate. These trap characteristics, which significantly affect the performance of RF devices, were thoroughly explored. The PICTS measurements provided a unique opportunity to characterize trap energy levels, and these findings formed the basis for further simulations using the TCAD tool. By incorporating precise simulation parameters, such as the dimensions of the CPW line, trap energy levels, unwanted contamination it was possible to estimate the density and spatial distribution of the traps in the undoped polysilicon layer. This has been done through fitting the simulations to the measured data such as SRP, effective resistivity and harmonic distortion. These insights are critical for understanding how the substrate influences RF performance, especially in terms of signal distortion and non-linear behavior.

Overall, this chapter provided a comprehensive overview of the experimental and simulation methodologies that will guide the research presented in this thesis. The detailed setups for large-signal measurements, trap characterization, and specific RF circuits, such as switches (see **Appendix B**) and mixers (see **Appendix C**), establish the groundwork for the upcoming chapters, where these techniques will be applied to analyze and optimize the performance of RF devices on advanced substrates.



3. Silicon-Based Substrate Solutions for RF and mmWave

In this chapter, several alternative solutions to overcome the PSC will be presented through measurements and simulations. Solutions such as field effect passivation, smart buried PN junctions and double-BOX substrate are used when the resistivity of the bulk substrate is higher than 3 kΩ·cm. While solutions such as gold-doped (Au-Si) silicon and porous silicon substrates are used when the starting bulk silicon is highly doped (10-20 Ω·cm or lower).

3.1 Strategies for Reducing Losses in Silicon Substrates

In RF and mmWave circuit design, minimizing both interface (in high-resistivity substrates) and bulk losses (in low-resistivity substrates) is essential to achieving optimal performance, especially in applications where signal integrity, linearity, and power efficiency are critical. High-resistivity substrates are commonly used to reduce parasitic effects, but they often encounter challenges such as the PSC effect at the Si-SiO_2 interface, which degrades RF performance by creating unintended conductive paths. Furthermore, bulk losses, which stem from high carriers within the substrate, also contribute to increased signal attenuation and reduced linearity.

This section gives an overview of the strategies and advanced methodologies that have been developed to mitigate these losses effectively. It explores innovative solutions targeting the Si-SiO_2 boundary to suppress the PSC effect and minimize interface-related degradation. Techniques such as field-effect passivation, PN junctions and the use of trap-rich layers are discussed, as they have shown promise in increasing the effective resistivity of the interface and enhancing RF signal linearity. Additionally, methods that address the bulk substrate, including gold-doped or porous silicon substrates, are reviewed for their potential to maintain high resistivity and reduce losses throughout the substrate's volume.

3.1.1 Solutions for Interface Losses (FE/PN Junctions/DB)

Interface passivation is a key approach for reducing losses at the Si-SiO_2 interface, which is a common source of performance degradation in HR substrates. There are several techniques that will be discussed in this thesis to address these losses:

- **Field Effect Passivation Technique**: This method involves applying a DC bias to increase the impedance at the Si-SiO_2 interface, thereby mitigating the PSC effect. By controlling the charge distribution at the interface, the parasitic conduction is suppressed, leading to improved signal integrity and enhanced linearity. Further details on the implementation of this method in advanced RF technologies will be explored in Section 3.2.

- **Smart Patterns of PN junctions**: Another effective solution for mitigating interface losses is the strategic use of PN junctions. By leveraging the depletion regions formed between the P-type and N-type regions of the silicon substrate, the electric field near the Si-SiO_2 interface can be disrupted. This interruption in the electric field helps to reduce the flow of free carriers at the interface, which in turn minimizes the PSC effect. As a result, signal integrity is enhanced, and substrate losses are significantly decreased. This technique will be discussed in more depth in **Section 3.3**, where its impact on RF performance is demonstrated.

- **Double-BOX substrate**: An innovative solution involves the use of a double-BOX substrate, which introduces a second insulating layer between the polysilicon layer of a conventional trap-rich substrate and the silicon bulk. By incorporating a thin insulating layer, as thin as 20 nm, the traps in the polysilicon can effectively mitigate the PSC effect, resulting in reduced substrate losses and enhanced performance. Additionally, this extra insulating layer helps to minimize harmonic generation within the substrate, which is crucial for preserving signal integrity in high-frequency applications. Further analysis and validation of this technique, through both simulations and measurements, are provided in **Section 3.4**, demonstrating its ability to significantly reduce substrate losses.

3.1.2 Solutions for Bulk Losses (Au-Si/Porous)

While interface losses are a primary concern, bulk substrate losses also play a significant role in degrading the performance of RF circuits. Several methods have been developed to passivate the bulk of the substrate, focusing on increasing the effective resistivity and reducing free carrier mobility within the silicon. The following bulk passivation techniques are examined:

- **Gold-Doped Silicon Substrate (Au-Si)**: Gold doping is a widely studied method for enhancing the resistivity of silicon substrates. In this technique, gold atoms are introduced into the bulk of the silicon substrate, where they act as trap centers for free carriers. These traps capture both donor-like and acceptor-like carriers, effectively reducing the number of mobile charge carriers in the substrate. By increasing the local resistivity at each point within the substrate, gold-doped silicon significantly improves the linearity of the RF device. This method will be explored in

detail in Section 3.5, where the effects of gold doping on the performance of RF passives are presented.

- **Porous Silicon**: Similar in function to gold-doped substrates, porous silicon offers an alternative method for increasing substrate resistivity. Unlike gold doping, porous silicon is created through an electrochemical process called anodization, which damages the crystalline structure of the silicon. This process introduces a high density of traps into the bulk substrate, effectively increasing the resistivity and reducing losses. The introduction of these traps prevents free carriers from traveling through the substrate, thereby mitigating both bulk and interface losses. Porous silicon substrates have shown great potential in improving the linearity and performance of RF circuits, and this technique will be thoroughly discussed in Section 3.6.

3.2 Field Effect in an Industrial 28 nm FDSOI Process

3.2.1 Proof of Concept

In this section, a passivation technique based on substrates fabricated in UCLouvain to overcome the PSC effect using a DC bias is demonstrated through RF measurements, which relies on locally depleting the interface, making it highly resistive. This is achieved by biasing a dedicated undoped polysilicon layer implemented below RF passive devices and above the Si bulk interface. Similar concepts have been proposed in [73, 74], and in this work we further expand on the concept using a full-sheet of a polysilicon layer below the passive devices. Furthermore, it is important to highlight that this Field Effect local passivation solution is fully compatible with all CMOS technologies, including both bulk-CMOS and fully-depleted FDSOI. This stands in contrast to the conventional trap-rich substrate eSI^{TM}, which is exclusively compatible with PDSOI technology at the wafer scale. Thanks to this field-effect passivation scheme, significantly improved linearity and reduced substrate losses are demonstrated.

Field Effect Operating Principle

The working principle of the field effect technique is based on a structure similar to the metal-oxide-semiconductor (MOS) structure. In our case the resistive-electrode layer is used as top electrode, making it possible to control the InsL-bulk interface by varying the applied DC bias V_p, consequently changing the impedance value at this interface. When a 0 V DC bias is applied, a PSC is present due to the positive oxide charges. If a positive DC bias is applied, the PSC is enhanced since more electrons from the substrate are attracted to compensate for the charges created by the positive applied DC bias. Conversely, if a negative bias is applied, holes are attracted to the InsL-bulk interface, leading to the creation of a hole-based PSC. It is important to note that sweeping the DC bias from accumulation to inversion (in a p-type substrate) is synonymous with sweeping the Fermi level from the valence band to the conduction band.

The main purpose of this technique is to find the optimum applied DC bias ($V_p = V_{opt}$) that positions the Fermi level near the silicon mid-gap. When that optimum condition is reached, the free carriers created by the positive oxide charges are compensated by a slightly negative applied DC voltage. This results in a high-resistivity interface at the InsL-bulk junction, as depicted in **Figure 3.1**.

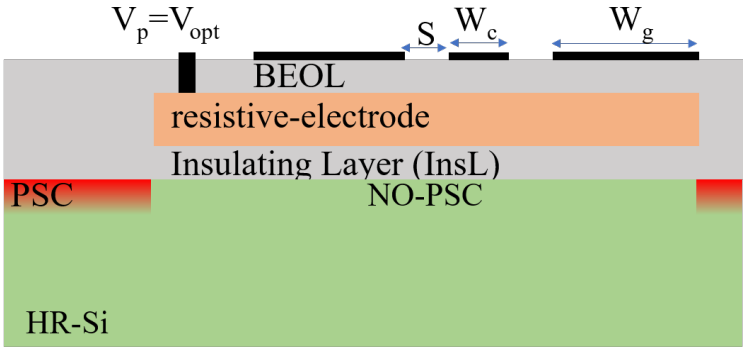


Figure 3.1: Operating principal of the field effect biasing technique in order to overcome the PSC effect, the applied DC bias $V_p = V_{opt}$ is at depletion region.

By comparing both TR and FE substrates, it is evident that both feature an undoped polysilicon layer. However, their usages are completely different. In the TR substrate, the polysilicon serves as a trapping network where electrons are compensated due to the high density of traps. On the other hand, the polysilicon in the FE substrate acts as an electrode that is biased to create accumulation, depletion, and inversion at the InsL-bulk interface, thereby increasing or decreasing the impedance at the interface. Another difference is that the polysilicon in the TR substrate is distributed throughout the entire silicon wafer, whereas in the FE substrate, it is used locally, only beneath passive components.

Substrates Description

CPW lines with 2.1 mm length have been fabricated at UCLouvain on various substrates. The substrates utilized include (see **Figure 3.2**): **(a)** high resistivity (HR) substrate, **(b)** trap-rich (TR) substrate to benchmark the new solution that will be described in this paper featuring an insulator oxide thickness of 200 nm and a trap-rich layer made of polysilicon $T_{trap-rich}$=500 nm, which is exclusively compatible with PDSOI technology. The third substrate is **(c)** field-effect (FE) substrate, featuring an insulator oxide thickness of 200 nm, an insulating layer (InsL) thickness of 100 nm and a highly resistive electrode with a thickness $T_{resistive-electrode}$ of 500 nm as illustrated in **Figure 3.2(c)** made of undoped polysilicon.

The dimensions of the CPW lines are: a signal electrode width Wc of 26 µm, a spacing between the signal and the ground electrodes S of 12 µm, and ground planar electrode width Wg of 208 µm. For all samples, the bulk silicon is p-type and has a nominal resistivity of 10 kΩ·cm, and the metal line is 1 µm-thick aluminium.

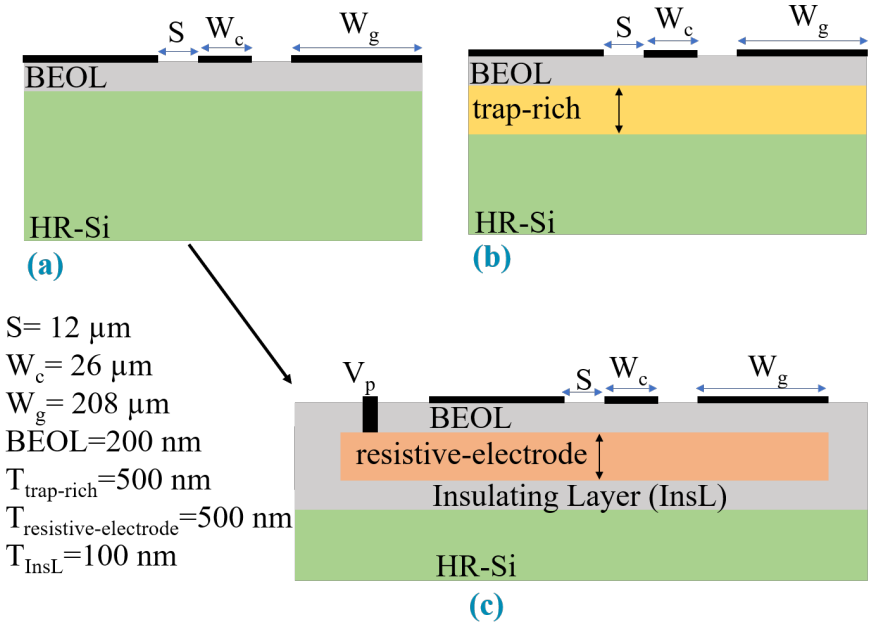


Figure 3.2: The three different fabricated substrates: **(a)** HR, **(b)** TR, and **(c)** field effect (FE) substrate with a DC bias (V_p) connected to the resistive electrode layer.

The polysilicon-based resistive-electrode (see **Figure 3.2(c)**) might already be available in a CMOS technology, offering an alternative to purchasing a substrate with a built-in trap-rich layer across the entire wafer (refer to **Figure 3.2(b)**). Additionally, it is feasible to use the field effect (FE) solution by employing the HR substrate as the starting material (indicated by the arrow in **Figure 3.2**.

Effective Resistivity Measurements

The small-signal measurements of the CPW line were carried out using an Agilent 2-port Performance Network Analyzer (PNA)-X, in conjunction with a pair of ground-signal-ground (GSG) Infinity probes with a 100 µm pitch. A DC needle probe is used to apply the V_p in the case of the Field Effect substrate. Then, S-parameters were measured and subsequently used to derive the equivalent RLCG model of the line. These parameters enable the extraction of the effective resistivity.

Figure 3.3 shows the measured losses and extracted of the effective resistivity as a function of frequency of the CPW line atop the three silicon-based substrates described above. The voltage values shown in the figure are the DC bias points applied to the resistive electrode called V_p as shown in **Figure 3.1** and is swept from -10 V to 1 V. The HR substrate exhibits the lowest effective resistivity, reaching 60 Ω·cm at 10 GHz as depicted in **Figure 3.3(b)**. This is due to the positive oxide charges attracting electrons to the BEOL-bulk interface, leading to the formation of the PSC. This results in increased losses, which exceed 0.6 dB/mm at 10 GHz (see **Figure 3.3(a)**). On the other hand, TR substrate shows an effective resistivity of around 10 kΩ·cm at 2 GHz (see **Figure 3.3(b)**). It mitigates the PSC effect by leveraging the traps generated by the grain boundaries within the 500 nm-thick trap-rich layer situated between the insulating layer (SiO_2) and the high-resistivity silicon bulk. This results in low transmission line losses, reaching 0.3 dB/mm at 10 GHz (see **Figure 3.3(a)**).

For the field effect substrate, when applying V_p = -10 V, an effective resistivity of around 100 Ω·cm is observed (see **Figure 3.3(b)**), which is very low and close to the value of the HR substrate. This is expected because at this DC value, holes are attracted to the surface, creating an accumulation (hole-based PSC). The Fermi level at the InsL-bulk interface is close to the valence band, resulting in high losses (see **Figure 3.3(a)**) close to HR substrate. By increasing the V_p value towards a positive value, it is possible to achieve an effective resistivity of around 4 kΩ·cm at 5 GHz when V_p = -2 V. This indicates that the Fermi level is near the silicon mid-gap (strong depletion point is reached), resulting in low insertion loss of around 0.3 dB/mm, close to the TR reference substrate (see **Figure 3.3(a)**).

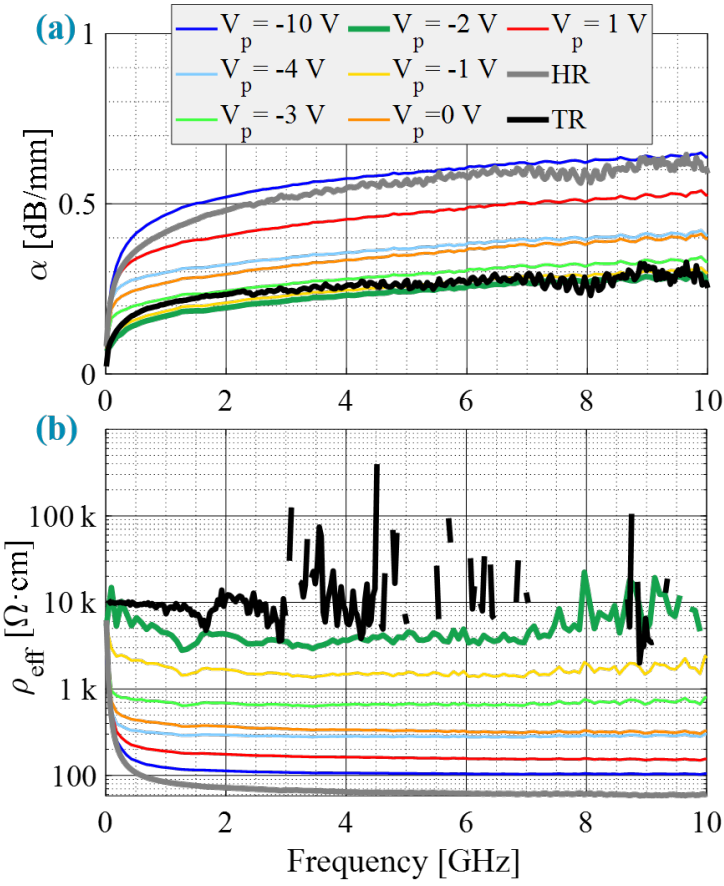


Figure 3.3: **(a)** Measured insertion loss of the CPW line and **(b)** extracted effective resistivity of the three studied substrates. The values from -10 V to 1 V are the DC biases (V_p) applied to the resistive electrode layer.

Increasing the value of V_p above -2 V gradually decreases the effective resistivity from 4 kΩ·cm to 100 Ω·cm. This occurs because the Fermi level shifts from the mid-gap towards the conduction band, increasing the density of electrons below the InsL. Whereas, the PSC is enhanced at V_p = 1 V (in positive bias), resulting in high losses (0.6 dB/mm at 10 GHz) along the CPW line.

Large Signal Measurements

large-signal measurements were conducted by injecting a single-tone frequency of 900 MHz into port 1 of the CPW line, with power ranging from -6 to 25 dBm. Subsequently, measurements of the fundamental (H1 at 900 MHz), second (H2 at 1.8 GHz), and third (H3 at 2.7 GHz) harmonics were taken at the output (port 2) of the CPW using setup in **Section 2.2.1**.

Figure 3.4 shows the second (H2 at 1.8 GHz) and third (H3 at 2.7 GHz) harmonics versus the output power of H1. The second harmonic for the HR substrate demonstrates around -43 dBm at an output power of H1=15 dBm, indicating high non-linearity due to the PSC effect. The large signal applied to the signal electrode modulates free carriers, significantly changing the resistivity at the InsL-bulk interface.

In contrast, the TR substrate shows a value of around -81 dBm at an output power of H1=15 dBm (eSI80™ substrate). This substrate is highly linear, thanks to the trap-rich layer that significantly reduces the density of free carriers.

For the Field-Effect substrate, it is possible to achieve very low values of the second harmonic when V_p = -2 V, which correlates well with the high effective resistivity (see **Figure 3.3(b)**). At this DC bias point, H2 = -85 dBm is reached at an output power of H1=15 dBm, which is close to the performance of the commercially available trap-rich eSI90™ substrate.

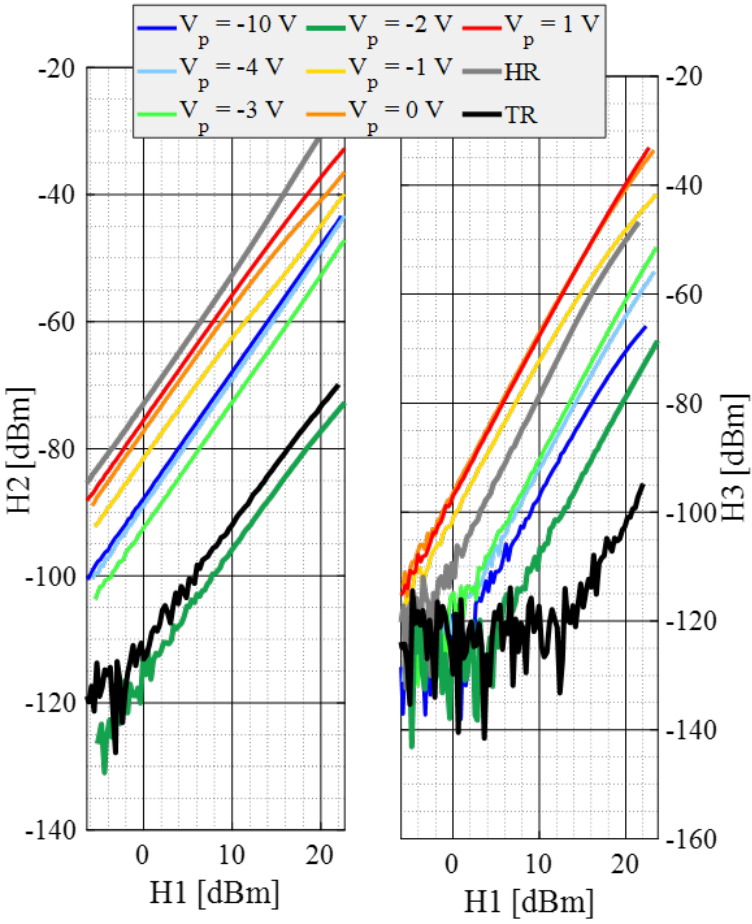


Figure 3.4: Measured second H2 (left) and third H3 (right) harmonics at 1.8 and 2.7 GHz, respectively, for the three studied silicon based substrates.

Small- and Large-Signal Correlation

Figure 3.5 presents the measured effective resistivity extracted at 5 GHz and the second harmonic at 1.8 GHz extracted at an output power H1= 15 dBm, both versus the resistive-electrode applied DC bias V_p.

As explained above, applying -10 V results in highly non-linear behaviour and low effective resistivity due to the hole-based PSC. Conversely, applying 1

V enhances the electron-based PSC and also considerably reducing the effective resistivity. It is worth noting that the nonlinearities in silicon-based substrates are based on the variation of the local resistivity at the InsL-bulk interface. When free holes/electrons are present at the interface due to the PSC effect (case V_p=-10 V or V_p= 1 V), they are modulated by the large signal applied to the CPW line, varying the local resistivity by orders of magnitude [36, 75]. This leads to high harmonics generation (higher than 60 dB at an output power of H1= 15 dBm).

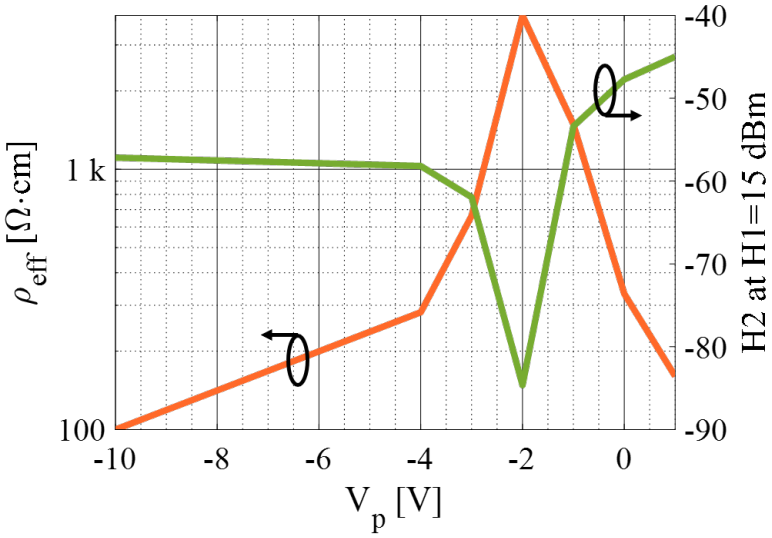


Figure 3.5: Measured effective resistivity extracted at 5 GHz (left) and the second harmonic H2 at 1.8 GHz extracted at an output power H1= 15 dBm (right) versus the resistive-electrode applied DC bias.

On the other hand, when the interface InsL-bulk is in state of strong depletion, all free carriers are compensated (Vp = -2 V), no free carriers are available in the whole substrate leading to low variation of the local resistivity, consequently low harmonics. This correlates well with high effective resistivity as depicted in **Figure 3.5**.

3.2.2 Measurements Using Commercial 300 mm Wafer

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3.2.3 Benchmarking

Redacted Confidential Content

3.3 PN Junctions in an Industrial 28 nm FDSOI Process

This technique was patented by UCLouvain in 2019 [76] and is able to achieve high RF performance. This is done by interrupting the PSC by introducing several implants of N and P type junctions below the insulating layer of the SOI structure. It takes benefit from the depletion region that happens between the neighboring P and N wells (see **Figure 3.6(b)**). The main contribution of this work in this kind of substrate is to extend the proof of concept to an integrated industrial technology 28 nm FDSOI from STMicroelectronics.

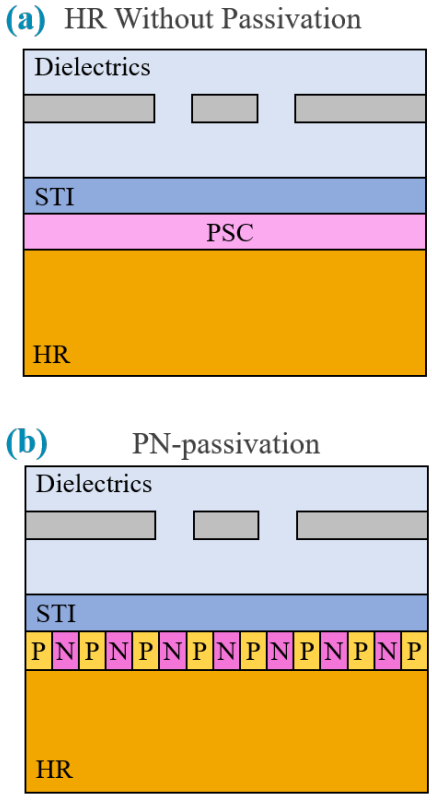


Figure 3.6: Schematic of the HR substrate in **(a)** and the perfect implementation of the PN junction in **(b)**.

3.3.1 Measurements Using Commercial 300 mm Wafer

The prototypes fabricated and measured at UCLouvain [2] have demonstrated that the implementation of PN junctions below the insulating layer are able to reach an effective resistivity higher than 3 kΩ·cm and a second harmonic can reach a values around -67 dBm at an output power of H1= 15 dBm. After that in [77] CPW lines were studied in a short loop technology with 2 metal layers, where the effective resistivity reaches values around 2 kΩ·cm. Moreover, HD measurements at 900 MHz are shown versus applied DC bias voltage. It has been shown that the PN junctions substrate is bias independent. Moreover, in [78] PNlines and PNgrid are studied in the 22FDX® technology from GlobalFoundries.

In this work, the extraction of effective resistivity and the measurement of the linearity of CPW lines, using PNlines and PNgrid passivation techniques, are integrated within the 28FDSOI technology. Furthermore, the dependence of these parameters on DC bias is thoroughly examined, offering a comprehensive analysis of the substrate's performance within this advanced technology.

Implementation of the PN Junctions

Two patterns of PN junctions are considered in this work: PNlines and PNgrid, as depicted in **Figure 3.7**. The PNlines configuration should be implemented perpendicular to the electric field (i.e., parallel to the CPW line tracks, as shown in **Figure 3.7(a)**). This alignment ensures that a high-impedance region is formed between the signal and ground tracks. The dimensions of the P and N regions are 315 nm wide, which is the minimal value allowed by the technology, while the length depends on the CPW line (760 µm in our case).

When the signal is in the P region, the Fermi level is close to the valence band, whereas in the N region, the Fermi level is near the conduction band. Consequently, the Fermi level must traverse the mid-gap, leading to resistivity values as high as 1 MΩ·cm. It has been demonstrated in [3] that when the pitch is tight (315 nm), a higher effective resistivity is achieved compared to a relaxed pitch (> 315 nm). This is primarily due to the fact that the electric field is interrupted more frequently in the tight pitch configuration than in the relaxed one. Moreover, the P and N regions are smaller in the tight pitch configuration, further contributing to the higher effective resistivity.

The second pattern is the PNgrid, the idea is to create multiple P and N regions in a square shape in order to create more resistive regions than PNlines. However, due to the DRC rules it is not possible to make them adjacent (like in PNlines case), this is why a small gap is made between P and N and is 234 nm. It is not possible to make smaller dimensions of the PNgrid because DRC rules of minimum area will appear, this explains the fact that squares of dimensions 350 nm $\times$ 350 nm are not used.

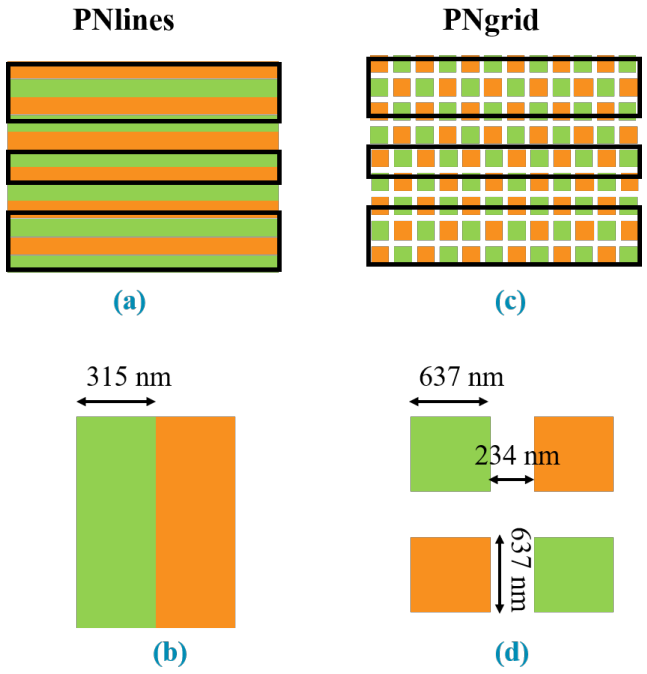


Figure 3.7: Implementation of the PNlines in **(a)** and the dimensions in **(b)**, PNgrid scheme in **(c)** and its dimensions in **(d)**. The black shapes in **(a)** and **(c)** show the CPW line implemented using the metal layers of the technology while the green and orange colors show the P and N regions implemented below the STI.

Influence of PN Implants Parameters

Ideally the P and N regions are like in Figure 3.6(b), but it is challenging to get those results since the control of the implants is required. Table 3.1[1] shows the wafer splits with their different energies of P and N. Moreover, the value of the effective resistivity has been measured for each wafer on a 760 µm CPW line with the following dimensions: Ws= 13.5 µm, S= 16.65 and Wg=111.6 µm. The CPW line is stacked M1LB.

When the N type implants are deeper than the P type implants, parasitic Nwell-to-Nwell coupling occurs, leading to a lower effective resistivity. This creates an unintended PSC due to the implants, which is observed in wafers A, B, and E. However, when the energy of the P type implants is increased to 110 %, a high effective resistivity is achieved, indicating that the N and P implants are balanced. This scenario is demonstrated in wafer C, where both implants are properly aligned, minimizing parasitic effects and expected to be similar to Figure 3.6(b).

Moreover, similar high resistivity results can be obtained with P type implants at 100 % energy and N type implants at 90 % energy, as seen in the case where a well-balanced implantation results in an effective resistivity of 540 Ω·cm (Figure 3.6(b)). This suggests that fine-tuning the implant energies can optimize the balance between N and P implants, thereby achieving the desired electrical properties without inducing unwanted parasitic coupling.

In the subsequent sections of this study, wafer D is extensively measured and analyzed. This wafer is selected as the most representative wafer for RF characterization due to its optimal balance of implant parameters and high effective resistivity.

[1]The energy implants shown in Table 3.1 are for a dose of 50 %. We also have the same split for a dose of 100 %. However the results of effective resistivity are lower than the ones shown in this thesis. This is expected, because the width of the depletion region (W) in a PN junction is given by the following simplified equation:

$$W \propto \sqrt{\frac{1}{N_A} + \frac{1}{N_D}}$$

Where N_A and N_D are the density of acceptors and donors, respectively. When N_A and N_D are increased the depth of the depletion region decreases. This leads to decreased effective resistivity of the CPW, those results could be found in [3].

Table 3.1: RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy. Effective resistivity is extracted at 30 GHz.

Wafer	Energy P [%]	Energy N [%]	ρ_{eff} [$\Omega \cdot$ cm]	Remark
A	90	100	150	N too deep relative to P
B	100	100	200	N too deep relative to P
C	110	100	500	Good balance with deeper P
D	100	90	540	Good balance with shallower N
E	100	110	61	N too deep relative to P

Effective Resistivity Measurements In the 28 nm FDSOI technology

Figure 3.8(a) presents the extracted effective resistivity as a function of frequency[2] for HR substrate without passivation, PNgrid and PNlines. The HR substrate shows a value of 30 Ω·cm because it suffers from PSC and the interface STI-bulk is expected to have high positive oxide charges. When the PNlines are implemented, the effective resistivity is 400 Ω·cm at 5 GHz indicating that the PSC is interrupted. When using PNgrid, a modest value of 300 Ω·cm is reached, which is unexpected. Since P implants are deeper than N, *maybe* there are some connections between the P regions (no connection between the N regions since they are shallow implants). Another suggestion is that the dose and energies are not adapted.

If the effective resistivity is categorized into ρ_x and ρ_y, where the x-direction is perpendicular to the PN lines and the y-direction is parallel to them, then ρ_x is expected to reach a high value, as previously explained. Conversely, ρ_y will be low due to facilitated electric field coupling through the very low resistivity

[2]Please note that other types of characterization, specifically regarding the effect of temperature on silicon-based substrates such as HR, trap-rich, PN junction substrates, and gold-doped silicon substrates, are reported in [79]. In this thesis, the effective resistivity versus frequency is presented exclusively at room temperature, whereas in [79], the effective resistivity is analyzed versus frequency at various temperature points. These temperature-dependent analyses are not included in this thesis, as they are not central to its primary focus.

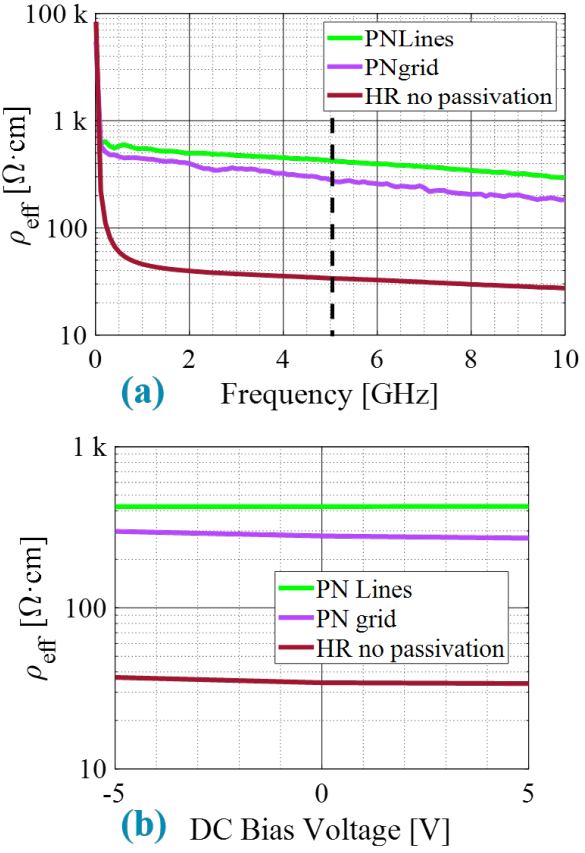


Figure 3.8: Extracted of the effective resistivity as a function of frequency in **(a)** and extracted effective resistivity as a function of the applied DC bias at 5 GHz in **(b)**. The designed CPW lines are stacked M1LB.

of the P and N regions. Thus, the effective resistivity in the context of PN lines is considered **directional**. This necessitates a co-design approach between the RF device and the PN lines. It is crucial to consistently ensure that the electric field is interrupted in scenarios involving crosstalk, inductors, filters, and even switch design to mitigate unwanted interactions.

On the other hand, the PNgrid does not require special attention when being implemented below RF devices, as it is expected to create high-resistivity

regions in both 2D directions.

Figure 3.8(b) presents the effective resistivity extracted at 5 GHz as a function of the applied DC bias. Both the PNlines and PNgrid demonstrate bias independence, reaching values of 400 and 300 Ω·cm, respectively. The HR substrate also shows bias independence in the range of -5 V to 5 V, due to the presence of a high density of positive oxide charges, which causes the depletion region at values lower than -5 V.

Large Signal Measurements In the 28 nm FDSOI technology

Large-signal measurements were conducted using a single-tone frequency of 900 MHz injected into one port of the CPW line, with power ranging from -4 to 25 dBm. Subsequently, measurements of the fundamental (H1 at 900 MHz), second (H2 at 1.8 GHz), and third (H3 at 2.7 GHz) harmonics were taken at the second port of the CPW. The setup is well described in **Section 2.2.1**.

Figure 3.9(a) shows the measured second and third harmonics as a function of the output power H1 at 900 MHz. Due to the PSC the HR substrate is non linear and shows a value of H2 around -52 dBm at an output power of H1=15 dBm. By using the PNgrid passivation, 4 dBm are gained due to the increased effective resistivity of the substrate. 8 dBm of H2 could be gained compared to HR substrate when PN lines are used. This correlates well with effective resistivity in **Figure 3.8(a)**.

Figure 3.9(b) shows the extracted second harmonic H2 at an output power of 15 dBm versus the applied DC bias on the CPW line. The HR substrate is bias dependent due to the compensation of charges created by the applied DC bias. On the other side, PNgrid is more linear than HR and is bias independent. PNlines are around 4 dBm more linear than PNgrid which correlates well with effective resistivity in **Figure 3.8(b)** and also to measurements of PNlines in **[77]**.

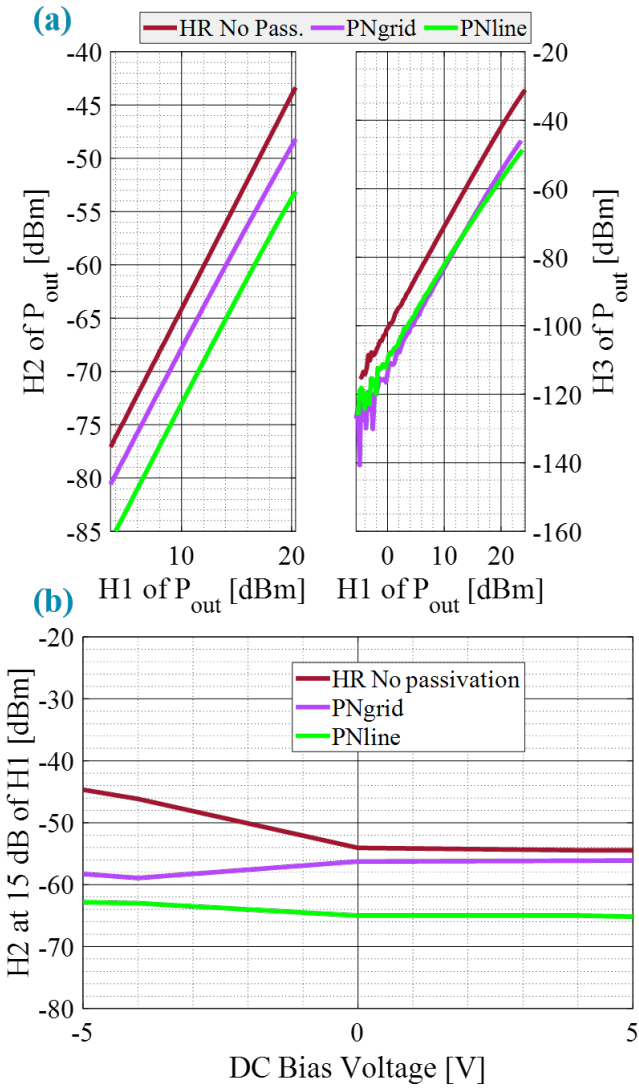


Figure 3.9: Measured second H2 (left) and third H3 (right) harmonics at 1.8 and 2.7 GHz, respectively, versus the output power H1 for HR without passivation, PNgrid and PNlines in **(a)** and second harmonic (H2) as a function of applied DC bias extracted at an output power of H1=15 dBm in **(b)**.

3.3.2 Benchmarking

Several advantages of using the PN substrate can be highlighted. First, both PN line and PN grid patterns increase the effective resistivity compared to the high-resistivity (HR) substrate without passivation. Additionally, the PN substrate is demonstrated to be compatible with FDSOI technology. Since PN junctions are created through implantation rather than by depositing or etching a physical layer (such as a metal or active layer), there is no limitation on the maximum density of PN junctions within this technology. This makes possible to make the PN junctions below the whole circuit when designing the RF circuit.

However, implementing PN lines requires careful consideration to ensure that the PN regions effectively impede the propagation of the electric field. This complexity can be mitigated by using the PN grid, which is straightforward to implement. The concept involves copying and pasting the PN grid pattern beneath the passive device[3]. This efficiency makes PNgrid pattern a practical choice for rapidly deploying substrate solutions in a given designs.

One challenge of using PN junctions is the requirement for multiple iterations during the fabrication process to determine the optimal balance of implantation energy and dose. This balancing is necessary to achieve the desired electrical characteristics and performance outcomes. Multiple fabrication runs are often needed to fine-tune these parameters, which can increase development time and cost. Despite this drawback, the benefits of using PN substrates in terms of enhanced performance and compatibility with FDSOI make it as a reliable solution to remove PSC and to replace the trap-rich substrate.

Table 3.2 shows a comparison of the performance of PN substrate to the reference HR with PSC, the commercially available POR substrate (10 Ω·cm) and commercial trap-rich substrate eSI80^{TM}. Please note that the POR, HR, PNLines, and PNgrid substrates represent measurements from a CPW line integrated within the 28FDSOI technology, all originating from the same fabrication run. The CPW line is 760 µm in length, with dimensions of Ws= 13.5 µm, S= 16.65 µm and Wg=111.6 µm.

[3]The implementation of the PN grid involves copying and pasting a cell containing four implants (2P and 2N) in both the x and y directions. Once the cell is prepared (DRC clean, which typically takes about 3 hours), implementing the PNgrid takes approximately one minute for a 760 µm CPW line.

In contrast, the eSI80^{TM} substrate is fabricated by SOITEC and processed at the Winfab facility at UCLouvain and its measurements were conducted on a LineCsetC CPW line (see **Section 2.2.2**).

Table 3.2: PN substrates RF performance comparison to the HR without passivation, POR substrate and eSI80^{TM} references.

Substrate	ρ_{eff} at 2 GHz [$\Omega \cdot$ cm]	ρ_{eff} Bias Dependency	H2 at H1=15 dBm [dBm]
POR	10	YES	-30
HR	40	YES	-52
eSI80^{TM}	10 k	NO	-80
PNlines	**500**	**NO**	**-57**
PNgrid	**400**	**NO**	**-62**

3.4 Double-Buried Oxide (DB) Substrate

As it has been noted in the beginning of this thesis, the integration of the trap-rich substrate is foreseen as challenging due to the presence of below-BOX functionalities such as the back gate contact, isolations wells and diodes. Forming these wells in a trap-rich type substrate is expected to lead to high leakage currents from the biased back gates to the substrate, facilitated by recombination centers associated to the traps of the polysilicon [80–82].

In order to overcome the reverse current leakage, one solution that will be studied in this thesis is to introduce an insulating layer of SiO_2 between the trap-rich layer and the bulk silicon called double-BOX (DB) substrate as depicted in Figure 3.10(c).

It has been demonstrated in two patents [83] and [84] from International Business Machine (IBM) that this new substrate can be manufactured in a semiconductor foundry using the Smart-Cut® process.

However, no studies have used this substrate within the scientific community for RF applications, raising several scientific questions: Is there a PSC between BOX2 and the bulk silicon? Is the polysilicon trap-rich layer capable of compensating for the charges created by Qox1, Qox2, and possibly Qox3? All answers to those questions will be in this subsection.

3.4.1 Proof of Concept

2.1 mm-long CPW lines have been designed on top of three types of substrates: (a) high-resistivity (HR), (b) conventional trap-rich (TR) and (c) double-BOX substrates (DB) as depicted in Figure 3.10.

UCLouvain Fabrication Process

Substrates illustrated Figure 3.10 are fabricated at Winfab (UCLouvain). Basic HR wafers are cleaned using Piranha solution (3:1: H2SO4:H2O2 for a duration of 20 min at 110°C). After the Piranha cleaning, all the wafers were dipped in dilute HF solution (1:50, HF: Deionized water) to remove the native oxide. The insulating layer (silicon dioxide, SiO_2) BOX2 was thermally grown at a temperature of 900°C. Several samples were fabricated with various thicknesses of that BOX2 layer. Next, for all samples, 500 nm (T_{poly}) of polysilicon was

deposited by low pressure-chemical vapor deposition (LPCVD), followed by, 200 nm of SiO_2, by PECVD. This oxide layer emulates the combined presence of the BOX1 layer along with the first insulating layers of the back-end of line (BEOL) dielectrics. Finally, a 1-µm-thick Aluminum layer was deposited on the backside of the Si wafer using E-gun evaporation. After each growth and deposition, the thicknesses were mapped by ellipsometry over the wafer.

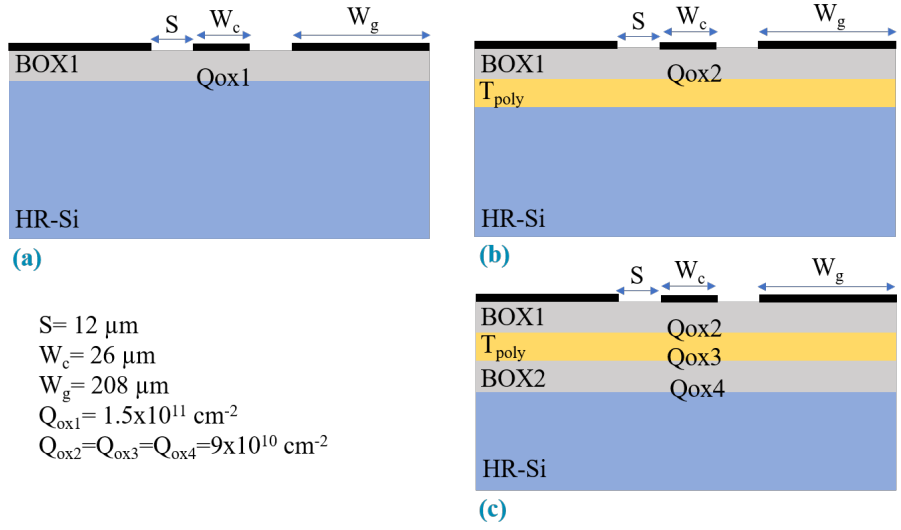


Figure 3.10: The different substrates fabricated: **(a)** HR, **(b)** TR, and **(c)** DB substrate with different BOX2 thicknesses of 2, 10, 20, 50 and 500 nm.

The dimensions of the CPW lines are: the width of signal track Wc = 26 µm, the spacing between the signal and the ground plane S = 12 µm and the width of the ground line Wg = 208 µm. For all samples, the bulk silicon is p-type and has a nominal resistivity of 10 kΩ·cm. The metal is 1 µm-thick aluminum.

The DB substrates have different BOX2 thicknesses: 2, 10, 20, 50 and 500 nm. The small-signal measurements of the CPW line were performed using 2-port Performance Network Analyzer (PNA)-X and a pair of ground signal ground (GSG) 100 µm-pitch |Z| probes.

Simulations are performed using Silvaco TCAD software, and accurately accounting for the effects of oxide charges Qox in the insulating layers, along

with those of interface and volume traps in the polysilicon layer. The interface oxide charge Qox1 was extracted as 1.5×10^{11} cm^{-2} for the HR substrate from the measurements of the metal-oxide-semiconductor (MOS) capacitance versus applied DC voltage (CV measurements[4]). At the SiO_2-polysilicon interface Qox2 was extracted as approximately 9×10^{11} cm^{-2} for the DB and TR samples through simulations fitting of the RF measurements using the modelling methodology described in [36, 75]. The polysilicon layer was simulated using tail distributions[5] for donor and acceptor as in [35]. The simulated DB structures include three semiconductor-insulator interfaces are Qox2, Qox3 and Qox4, as depicted in Figure 3.10.

Effective Resistivity Measurements

Figure 3.11 shows the extracted effective resistivity as a function of frequency for HR, TR and DB substrates, at V_{DCline} = 0 V. The HR substrate has a low effective resistivity of around 80 Ω·cm at 2 GHz due to the PSC effect. A conductive layer below the insulating layer is formed which makes the substrate's electrical properties non-homogeneous. The TR substrate has an effective resistivity higher than 10 kΩ·cm at 2 GHz. The traps from the polysilicon layer capture the electrons attracted to the Si-SiO_2 interface and pin the Fermi level near mid-gap [75] (i.e. the interface is in a highly resistive state).

[4]The CV measurements were conducted under dark condition using a PM8PS prober and B1500 semiconductor analyzer, with a hot-plate temperature control system allowing for precise measurements at elevated temperatures. The frequency ranges from 1 kHz to 1 MHz and temperature from 25 to 150 °C as in [85].

The density of oxide charges is computed using the equation from [86]:

$$Q_{ox} = \frac{(\Phi_{MS} - V_{FB}) \times C_{ox}}{q}$$

Where Φ_{MS} is the metal-semiconductor work function difference between the aluminum and the silicon, V_{FB} is the flatband voltage, C_{ox} is the oxide capacitance in F/cm^2 and q is the elementary charge constant of 1.6×10^{-19} C.

[5]In the case of the simulations performed for the double-BOX substrate, continuous distributions (see Section 2.3.1) were used, as the analysis of this substrate was conducted before the implementation of the PICTS method. It is important to note that the simulation, fabrication, and measurements of the double-BOX substrate were completed prior to the introduction of PICTS measurements.

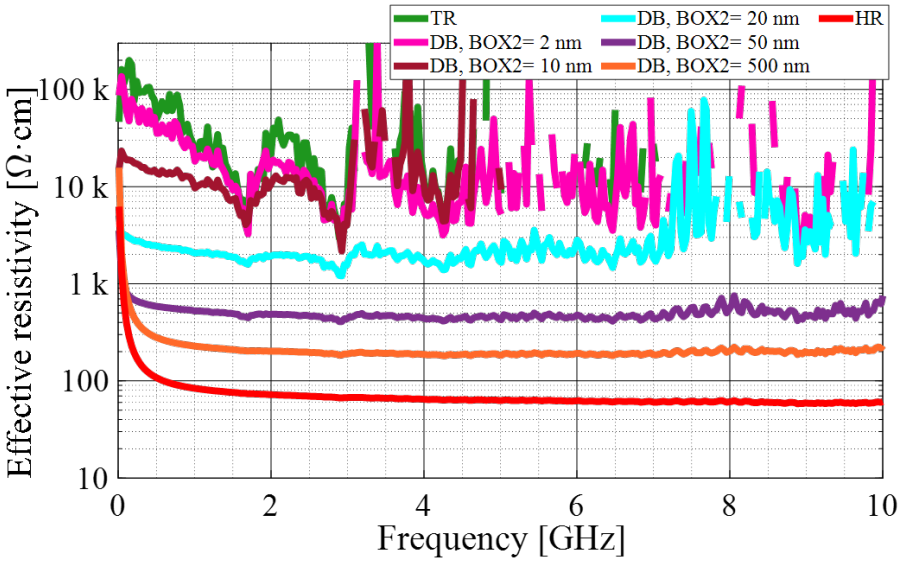


Figure 3.11: Measured effective resistivity as a function of the frequency for the TR, HR and DB substrates with different BOX2 thicknesses.

The DB substrate with 2 nm of BOX2 shows an effective resistivity close to that of the reference TR wafer. In that case, even with the presence of the 2 nm-thick BOX2 layer in between the bulk and the polysilicon, the traps are able to compensate the electrons created by the fixed oxide charges and passivate the BOX2-Si interface. This is confirmed by TCAD simulations, that reveal a robust passivation of the below-BOX2, particularly for thin BOX2 layers (see **Figure 3.12(a)**).

The DB substrates with 10 nm and 20 nm of BOX2 achieve effective resistivity metrics of 10 kΩ·cm and 2 kΩ·cm at 2 GHz, respectively. With the increase in BOX2 thickness, the trap-rich polysilicon layer becomes further away from the BOX2-bulk interface, and the passivation is less effective.

Then, the DB substrates with BOX2 thicknesses of 50 nm and 500 nm show 400 Ω·cm and 200 Ω·cm, respectively. The decrease in effective resistivity for these samples is due to the traps in the polysilicon being electrostatically far from the Si-SiO_2 interface. The traps are not able to compensate the PSC effect

locally (see **Figure 3.12(b)**), and the RF performance results resemble more those of the HR reference sample than those of the TR reference sample.

Figure 3.12 presents the electron concentration across the entire substrate in two dimensions. The implemented CPW has the dimensions specified for a LineCsetC and is simulated atop two different substrates: a DB with a BOX2 thickness of 2 nm in **Figure 3.12(a)** and a DB with a BOX2 thickness of 500 nm in **Figure 3.12(b)**. It is evident that with a BOX2 of 2 nm, there is a very low electron density at the BOX2-bulk interface, as shown in **Figure 3.12(a)**. Conversely, when BOX2 is 500 nm, an electron density of approximately 10^{16} cm^{-3} is observed, indicating the presence of a PSC layer at the BOX2-bulk interface.

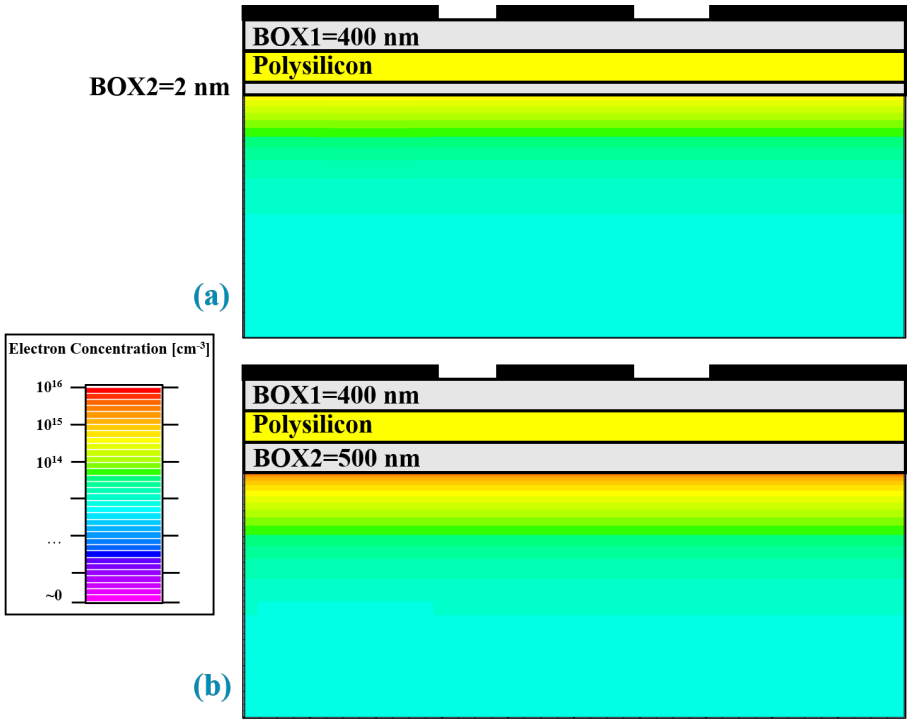


Figure 3.12: Electrons concentration simulation in 2D for CPW line implemented in ATLAS silvaco for a DB substrate with a BOX2 of 2 nm in **(a)** and for the same substrate with a BOX2 of 500 nm in **(b)**.

Large signal measurements

Large-signal measurements were performed using a single tone (H1) at 900 MHz injected into one port of the CPW line with its power swept from -25 to 25 dBm. The fundamental (H1), second (H2) and third (H3) harmonics were measured at the second port of the CPW.

Figure 3.13 shows the measured power of the second and the third harmonics versus the fundamental output power H1 at 900 MHz frequency.

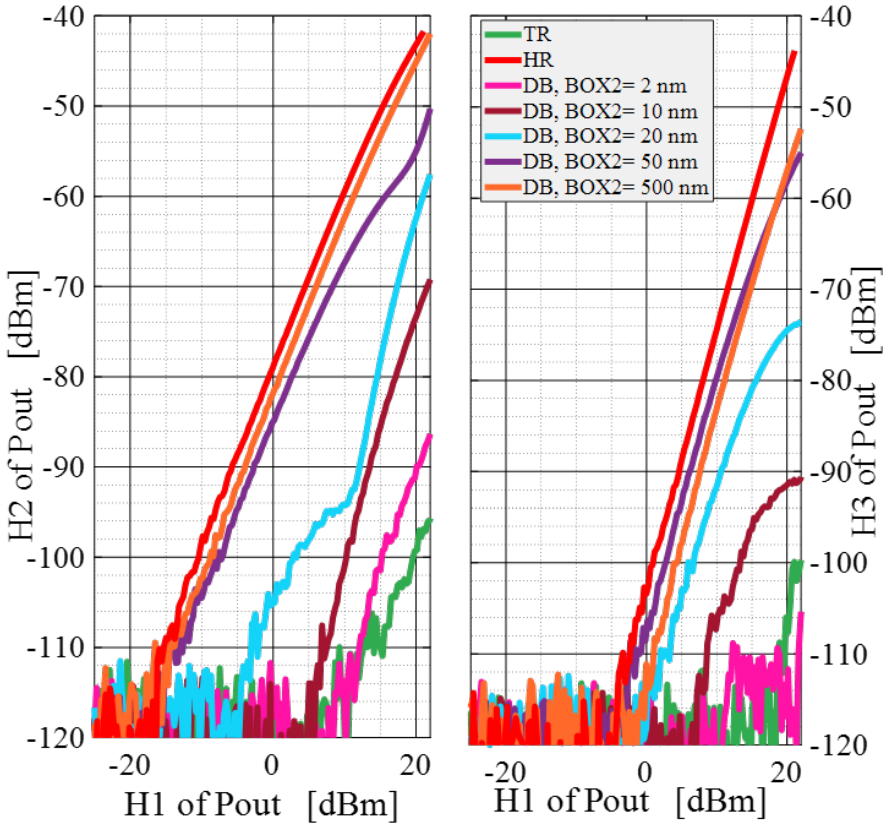


Figure 3.13: Second and third harmonics versus fundamental H1 output power at 900 MHz, for the studied substrates HR, TR and DB with different BOX2 thicknesses.

The HR is the least linear substrate due to the PSC effect and shows -50 dBm of H2 at a fundamental output power H1 of 15 dBm. The large signal applied to the CPW line modulates a large amount of free carriers at the Si-SiO_2 interface, and this translates to a high power of harmonics [87].

The TR is the most linear substrate because of the traps in the polysilicon that ensure a low quantity of free carriers in the substrate, and consequently, a low variation of the local resistivity below the signal line at RF frequencies [36, 75]. This low variation translates to a low harmonic level for the TR substrate. The DB substrate with a BOX2 of 2 nm shows a H2 power around 10 dB higher than the TR. The thicker the BOX2 layer, the more free carriers are at the Si-SiO_2 interface to be modulated by the large-signal stimulus.

Effective Resistivity and H2 Dependence

Figure 3.14 shows both the effective resistivity extracted at 2 GHz and the second harmonic H2 (extracted at an output power H1= 15 dBm) for the different BOX2 thicknesses, under the condition V_{DCline} = 0 V. It illustrates how the effective resistivity and linearity strongly depend on the thickness of the BOX2. When the free carriers are less than 10 nm away from the polysilicon, the interface BOX2-polysilicon is well passivated and effective resistivities higher than 10 kΩ·cm are achieved thanks to the Fermi level below the signal line being deep in the bandgap. When the traps are far away from the Si-SiO_2 interface (more the 20 nm), the traps are not able to overcome the PSC effect, and this translates into a low effective resistivity and higher non-linearity. TCAD simulation results are overlaid in Figure 3.14, and demonstrate very good agreement to the measured data.

It is important to note that simulations of the effective resistivity and second harmonic have been performed but are not included in this thesis. The reason for this omission is that variations in the thickness of BOX1 do not affect the state of the BOX2-Si interface. The BOX1 layer only determines the proximity of the CPW line to the BOX2-Si interface, which is the primary interface of interest. As such, variations in BOX1 thickness are not critical for the conclusions drawn in this study.

Similarly, simulations exploring the impact of varying the thickness of the polysilicon layer are not presented here. This is because no significant variation

in results was observed for polysilicon thicknesses ranging from 500 nm down to 50 nm. It is worth noting that no simulations have been conducted for polysilicon layers thinner than 50 nm. Furthermore, measurements for substrates with a thin polysilicon layer are not available, thereby limiting the validation of such simulations experimentally.

So far, it has been demonstrated that the double-BOX substrate works correctly as a prototype. The next challenge is to determine whether a semiconductor foundry can successfully reproduce this type of substrate, and how the RF performance of these substrates would be affected. Moreover, the objective includes assessing how the RF performance of the double-BOX substrate, with thickness of BOX2 at 500 nm, would be influenced when the thickness of this latter is reduced. Reducing the thickness of the polysilicon layer is of high importance for semiconductor foundries as it reduces the production cost of the substrate. These aspects will be discussed in the following subsection, exploring both the effective resistivity and linearity of the fabricated passive devices.

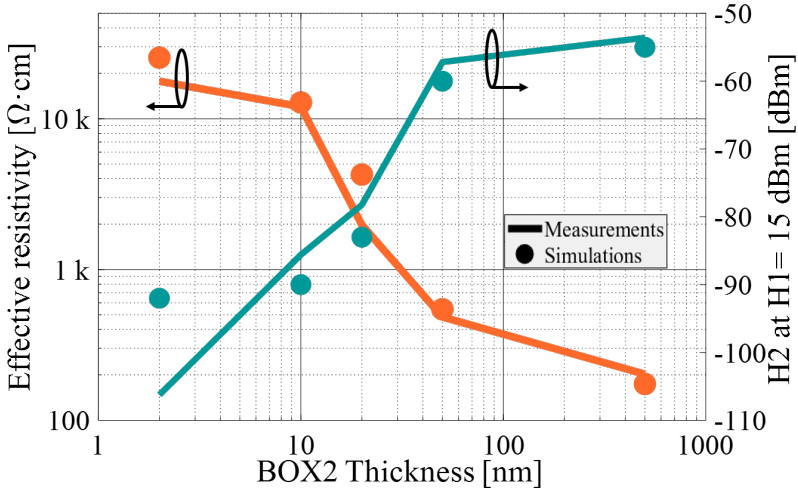


Figure 3.14: Measured and simulated effective resistivity (left axis) and second harmonic power (right axis) as a function of the BOX2 thickness of the DB substrates.

3.4.2 Measurements Using Commercial 300 mm DB Wafer

2.1 mm-long CPW lines have been designed on top of two types of substrates: (i) high-resistivity substrate and (ii) double-BOX substrates (DB) as depicted in **Figure 3.10**. The thickness of BOX1= 400 nm[6], thickness of polysilicon Tpoly= 200 nm, BOX2= 5 nm, the bulk is p-type (high-resistivity > 1 kΩ·cm)[7].

Effective Resistivity as a Function of Applied DC Bias

The small-signal measurements of the CPW line were performed using 2-port Performance Network Analyzer (PNA)-X and a pair of ground signal ground (GSG) 100 µm-pitch |Z| probes. **Figure 3.15** shows the measured effective resistivity as a function of the applied voltage with extraction conducted at 5 GHz for the HR and DB (polySi) substrates.

In the case of the HR substrate, the effective resistivity exhibits bias dependency, fluctuating between 600 and 200 Ω·cm, significantly lower than the nominal resistivity of the bulk (1 kΩ·cm). The lack of pinning of the Fermi level at the interface results in charges generated by the applied DC bias being compensated by carriers originating from the bulk. This bias dependency is attributed to the accumulation, depletion, and inversion effects at the SiO_2-bulk interface.

The DB (polySi) substrate exhibits bias independence, with the effective resistivity around 2.5 kΩ·cm. Despite the presence of a thin insulating layer of 5 nm, the traps within the polysilicon trap-rich layer effectively compensate for the electrons generated by both positive oxide charges and the applied DC voltage. This leads to efficient passivation of the BOX2-bulk interface and the pinning of the Fermi level.

[6]It is worth noting that in this study, the BOX1 layer has a thickness of 400 nm, compared to 200 nm in the previous section. The choice to use a BOX1 thickness of 400 nm in this study was primarily driven by practical considerations from the foundry. This change in thickness was implemented because variations in the thickness of BOX1 do not influence the state of the BOX2-Si interface, which is the primary focus of this investigation.

[7]Substrates have been fabricated by Watech Electronics CO from China. It is worth noting that the substrates in **Figure 3.10** are from UCLouvain, but in this part **Section 3.4.2**, Watech collegues have fabricated one HR of reference similar to one in **Figure 3.10(a)**, and a double-BOX similar to the one in **Figure 3.10(c)**, no polysilicon trap-rich of reference has been provided.

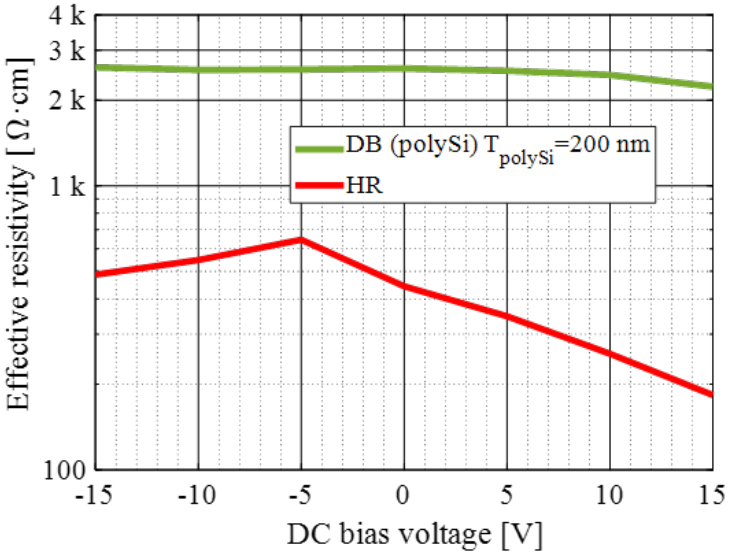


Figure 3.15: Effective resistivity as a function of the applied DC bias for undoped trap-rich layer in the double-BOX substrate and HR reference at 5 GHz. (the DB substrate has a BOX1= 400 nm, Tpoly=200 nm, and BOX2= 5 nm).

Moreover, The DB substrate demonstrates bias independence because the potential across the substrate is primarily dropped down over BOX1 and effectively compensated at the BOX1-polysilicon interface. TCAD simulations in **Figure 3.16** illustrate the evolution of the bias along the Y direction for the DB substrate, with parameters BOX1= 400 nm, Tpoly= 200 nm, and BOX2= 5 nm.

Both +5 and -5 V DC bias points are applied to the electrode signal reference to 0 V. Additionally, the inset in **Figure 3.16** shows that the energy bands (valence and conduction) at the interface BOX2-bulk are flat, this potential does not significantly affect the substrate due to the compensatory effect provided by the polysilicon trap-rich layer. The ionization/de-ionization of numerous trap states within the polysilicon layer in response to the applied DC potential ensures minimal variation in the Fermi level at the BOX2-Si interface.

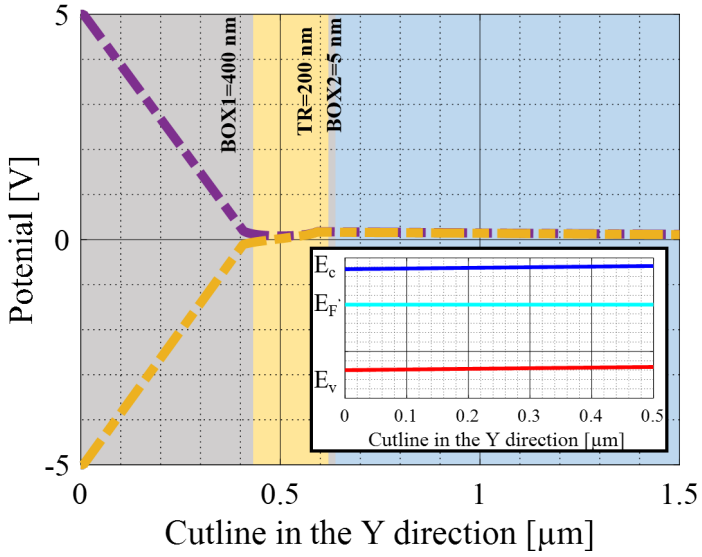


Figure 3.16: Potential along the Y direction of the CPW line below the signal electrode when V_{DCline}= 5 V and V_{DCline}= -5 V bias points are applied on it reference to 0 V. The inset provides the energy bands starting from BOX2=5 nm.

The simulation depicted in **Figure 3.17** illustrates the potential distribution for another DB substrate, not characterized within this study but referenced in our previous work [4], with BOX2=500 nm. This simulation provides valuable insights into the substrate behavior when the traps within the trap-rich layer are positioned further away from the interface.

The simulations indicate that when the traps are electrostatically distant from the trap-rich layer, their ability to compensate for the charges induced by the applied DC bias is significantly compromised. This conclusion is supported by the observed potential at the BOX2-bulk interface, where the conduction band is seen to be bent towards Fermi level (see inset **Figure 3.17**).

Although the effective resistivity remains low for this substrate, its bias independence is maintained due to the entire potential being dropped across BOX1 and effectively compensated at the BOX1-polysilicon interface.

This disparity underscores a fundamental distinction between an ordinary HR substrate and a DB substrate featuring a thick BOX2. While the latter exhibits bias independence owing to the compensation mechanism across BOX1, the former lacks this characteristic due to differences in trap positioning and charge compensation dynamics.

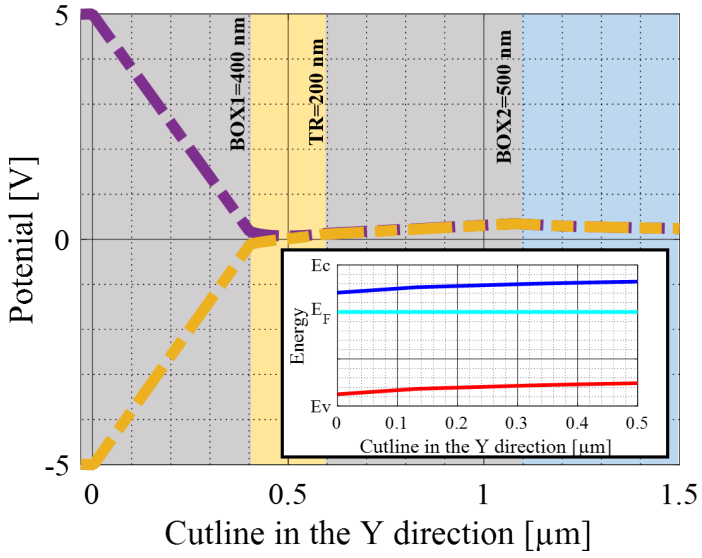


Figure 3.17: Potential along the Y direction of the CPW line below the signal electrode when V_{DCline}= 5 V and V_{DCline}= -5 V bias points are applied on it reference to 0 V. The inset provides the energy bands starting from BOX2=500 nm.

Second Harmonic as a Function of Applied DC Bias

Applying a large signal to a passive device induces modulation of the free carriers in the semiconductor substrate by the electric field, thereby causing variations in the substrate impedance over time [36, 75]. These fluctuations result in nonlinear behavior of the device. To assess such effects, large-signal measurements were conducted using a single-tone frequency of 900 MHz injected into one port of the CPW line, with power ranging from -14 to 25 dBm. Subsequently, measurements of the fundamental (H1 at 900 MHz), second (H2

at 1.8 GHz), and third (H3 at 2.7 GHz) harmonics were taken at the second port of the CPW.

In **Figure 3.18**, the second harmonic (H2) level at an input power of 15 dBm is depicted against the applied DC bias points for the HR and DB (polySi) substrates. The HR substrate exhibits bias dependency, with variations from -68 to -38 dBm, indicating high non-linearity attributed to the PSC effect and unpinned Fermi level.

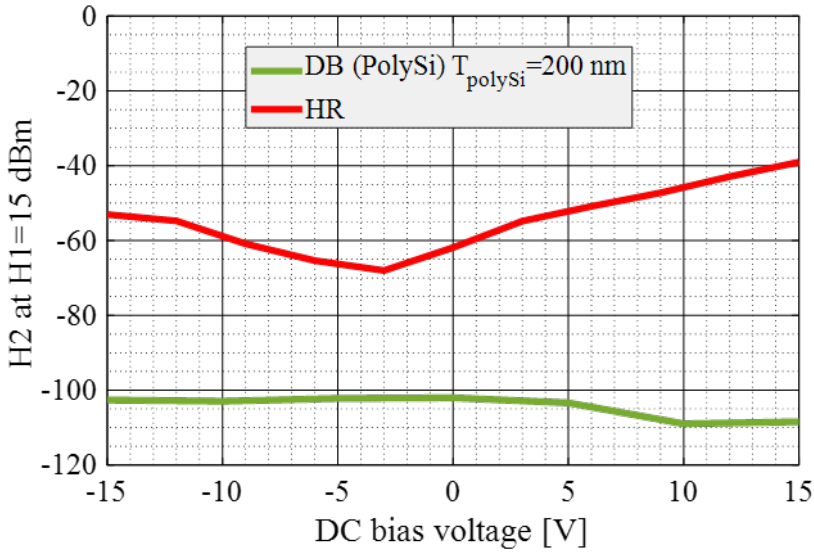


Figure 3.18: Power of the second harmonic extracted at an input power of H1=15 dBm as a function of the applied DC bias for undoped trap-rich layer in the double-BOX substrate and HR substrate. (the DB substrate has a BOX1= 400 nm, Tpoly=200 nm, and BOX2= 5 nm).

Conversely, the DB (polySi) substrate, owing to its traps within the polysilicon, demonstrates minimal bias dependency and boasts a 40-dB improvement over HR substrates at V_{DCline} = 0 V. Moreover, it shows a value of around 100 dBm similar to the commercially available eSI100^{TM}. It aligns well with its effective resistivity trend (refer to **Figure 3.15**).

3.4.3 Undoping/Doping the Polysilicon Layer

Typically, the primary objective of doping a semiconductor is to reduce its resistivity, achieved through dopants like Boron and Phosphorus. This decrease in resistivity is attributed to the proximity of the energy levels of these dopants to either the conduction or valence band. However, for RF and millimeter-wave applications, high resistivity semiconductor materials are necessary. To enhance the resistivity of doped or undoped semiconductors, one approach involves doping with deep-level atoms that create energy levels near the silicon mid-gap [88]. Prior studies have demonstrated that doping the silicon substrate with gold atoms significantly increases the effective resistivity [5].

It is crucial to carefully select atoms compatible with conventional CMOS processes. Candidates such as Carbon and Germanium atoms are well-suited for use in semiconductor foundries. Moreover, it is anticipated that these atoms can mitigate the effects of recrystallization in the polysilicon trap-rich layer. Consequently, the polysilicon layer can maintain the density of trap states even under high thermal budgets [89] (e.g., 2 hours at 1100 °C). This resilience is vital for ensuring consistent performance of semiconductor devices, particularly in high-temperature environments characteristic of semiconductor manufacturing processes.

Historically, the activation energies associated with carbon (C) and germanium (Ge) atoms have been documented in [90]. Carbon atoms introduce traps at two energy levels: the first is situated 0.25 eV away from Ec (the conduction band), while the second lies 0.27 eV distant from Ev (the valence band). Conversely, Ge atoms generate traps at energy levels of 0.27 eV and 0.5 eV, both far from Ec.

In this subsection, the efficiency of doping the trap-rich layer with carbon atoms is investigated and quantified. Through measurements and analysis, the impact of carbon doping on the performance and characteristics of the double-BOX trap-rich layer is evaluated. This exploration aims to elucidate the potential benefits of carbon doping in enhancing semiconductor materials for RF and millimeter wave applications.

Measurements were performed as in **Section 3.4.2** using the same material, also the same dimensions and length of the CPW line. Two wafers were

measured, both having identical structures, i.e., BOX1 = 400 nm, polysilicon thickness T_{poly} = 180 nm, and BOX2 = 5 nm. The bulk resistivity is higher than 1 k$\Omega \cdot$cm. The difference between the two wafers is as follows: (i) one has a low density of carbon dopants (C $< 0.5\%$) in the polysilicon layer, and (ii) the other has a high density of carbon dopants (C $= 1\%$).

Effective Resistivity Versus DC Bias

Figure 3.19 depicts the effective resistivity as a function of the applied DC bias for the two DB substrates with extraction conducted at 5 GHz. Since both DB substrates have 5 nm of BOX2, they overcome the PSC effect exhibiting effective resistivity higher than 1 k$\Omega \cdot$cm. The effective resistivity of the highly doped DB (polySi C $= 1\%$) substrate surpasses that of the lowly doped DB (polySi C $< 0.5\%$) substrate by 450 $\Omega \cdot$cm. This difference is attributed to the presence of carbon atoms, which create additional traps in the polysilicon trap-rich layer, resulting in a slight difference of the effective resistivity[8].

A similar study was conducted using Ge atoms in place of C atoms, highlighting the difference between highly doped and slightly doped Ge. This difference is approximately 800 ohms, as detailed in **Appendix E**.

In this section, the effective resistivity as a function of frequency is not presented because the conclusions drawn would be identical to those discussed in the previous section. Repeating similar analyses and results would not contribute additional value or insights to the study. Therefore, to avoid redundancy and maintain clarity, this section focuses on effective resistivity as a function of applied DC bias rather than revisiting findings already established earlier.

[8]The undoped double-BOX substrate described in **Section 3.4.2** was not included in the figure due to its different polysilicon thickness of 200 nm, whereas the doped substrates have a thickness of 180 nm. This discrepancy makes a direct comparison between the undoped and doped substrates unreliable. To ensure a valid comparison, it is crucial that all substrates have same polysilicon thickness. Thus, only substrates with identical polysilicon thickness were considered in the analysis.

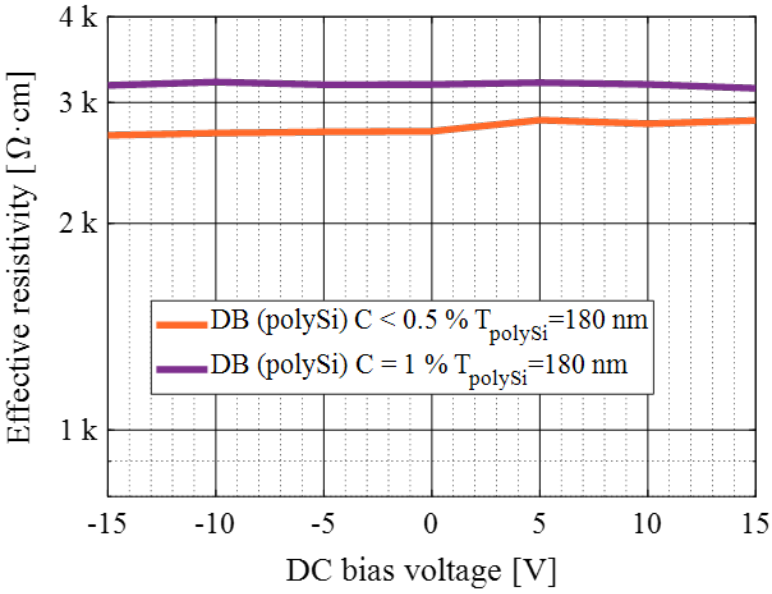


Figure 3.19: Effective resistivity as a function of the applied DC bias for doped trap-rich layer in the double-BOX substrates using carbon atoms. Extraction was conducted at 5 GHz.

Second Harmonic Versus DC Bias

In **Figure 3.20** the second harmonic power levels at an input power of H1=15 dBm are depicted against the applied DC bias for the DB substrates analyzed herein. Notably, both the DB (polySi C $<$ 0.5%) and DB (polySi C $=$ 1%) substrates exhibit bias independence, with the former hovering around -97 dBm and the latter at approximately -101 dBm. This 4 dB discrepancy between the lightly and heavily doped substrates underscores the role of additional carbon trapping centers within the polysilicon trap-rich layer, influencing harmonic generation dynamics.

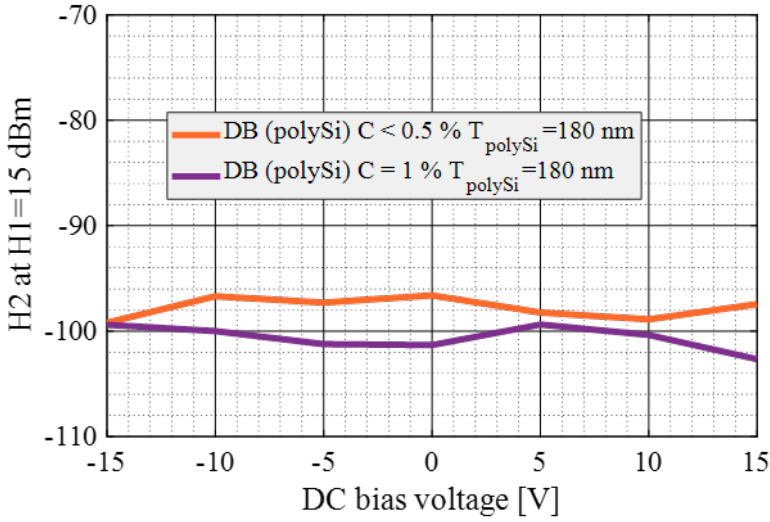


Figure 3.20: Power of the second harmonic extracted at an input power of H1=15 dBm as a function of the applied DC bias for carbon-doped trap-rich layer in the double-BOX substrate.

In this subsection, the efficiency of double-BOX substrates employing polysilicon trap-rich layer is demonstrated through measurements of CPW transmission lines. Simulations illustrate that the DB with polySi exhibits bias independence, as the DC bias applied is absorbed by the BOX1-polysilicon interface.

Based on the findings of this paper, reducing the polysilicon layer thickness from 200 nm to 180 nm and heavily doping it with carbon atoms offers triple benefits: (a) thinner polysilicon thus reducing substrate cost; (b) carbon atoms mitigate the effects of recrystallization in the polysilicon trap-rich layer, enhancing robustness against temperature fluctuations during conventional CMOS process as mentioned in [89]; and (c) gain in effective resistivity while maintaining high substrate linearity, remaining below or near 100 dBm of the second harmonic at 1.8 GHz.

It is expected that during annealing, the process naturally attempts to repair defects in the polysilicon layer. However, the presence of C and Ge (same study similar to the doping of polysilicon with Ge instead of Carbon are shown in

Appendix E) atoms creates additional traps that counteract this defect-repairing effect, ensuring that the trap-rich layer maintains its high trap density.

Overall, doping the polysilicon trap-rich layer increases the effective resistivity of the substrates and reach values three times higher than the nominal resistivity of the bulk. Moreover, it lowers its harmonics to reach a value of the H2 around -100 dBm at an input power of 15 dBm which is close to the commercially available eSI100^{TM}.

3.4.4 Benchmarking

One of the primary advantages of double-BOX substrates is that they completely eliminate current leakage from the polysilicon layer to the silicon bulk due to the presence of the thin BOX2. This isolation is particularly advantageous for applications in RF and digital domains, as it minimizes unwanted crosstalk and losses (high effective resistivity and linear see Table 3.3). Additionally, the double-BOX structure allows for the application of both positive and negative DC biases on the back-gate of the FDSOI transistor, providing greater flexibility in circuit design and operation.

The double-BOX substrate is also less sensitive to re-crystallization after annealing, which is a significant benefit during the CMOS process. By doping the substrate with carbon and germanium, its efficiency can be further enhanced, which delays the re-crystallization process. Well-designed double-BOX substrates are capable of delivering excellent RF performance, which is crucial for the development of high-quality RF passive components. This capability makes the double-BOX substrate a promising candidate for advanced RF applications.

Despite its advantages, the double-BOX substrate comes with certain drawbacks. One notable disadvantage is its higher cost compared to conventional trap-rich substrate. This increased expense is primarily due to the additional processing step required to integrate the double-BOX structure. To mitigate this cost, it is essential to reduce the thickness of the polysilicon layer, which can help lower manufacturing expenses while maintaining the substrate's performance.

Another significant challenge is the difficulty of integrating double-BOX substrates into commercially available technologies such as 22FDX® and 28

nm FDSOI. This integration challenge arises because adopting the double-BOX substrate would necessitate changes in the doping profiles of the channel and modifications to existing fabrication recipes. Such changes could disrupt established manufacturing processes and require substantial re-engineering efforts, which may not be feasible or cost-effective in the current commercial landscape.

Table 3.3: Double-BOX RF performance comparison to the HR, TR eSI80^{TM} and TR eSI100^{TM} references.

Substrate	**ρ_{eff} at 2 GHz** $[\Omega \cdot cm]$	**ρ_{eff} Bias Dependency**	**H2 at H1=15 dBm** [dBm]
HR	100	YES	-50
eSI80^{TM}	10 k	NO	-80
eSI100^{TM}	40 k	NO	-100
Double-BOX	**$>$ 10 k**	**NO**	**-100**

3.5 Gold Doped Silicon Substrate (Au-Si)

A new concept called deep level doping compensation was introduced in order to increase the resistivity of SOI substrate, consequently reducing the PSC effects by introducing a high density of traps in the entire silicon substrate thickness [91].

Elemental gold (Au) is used to compensate for background free carriers in low resistivity Czochralski silicon substrates by creating deep level traps within the Si band gap, thereby enhancing the substrate's resistivity [88]. Gold is introduced into the Si via an ion-implantation process, followed by a high-temperature annealing procedure to activate the dopant and achieve an optimum level of compensation.

The material chosen for doping the silicon in this work is gold, because it can be used for both n-type and p-type silicon in contrast to other dopants that only introduce either donor or acceptor traps centers. It has been reported in [92] that gold atoms introduces equal concentrations of donor and acceptor levels and since Au atoms act as recombination centers in silicon, they generate a pair of energy levels; acceptor state at ionisation energy of 0.54 eV from conduction band and donor state at ionisation energy of 0.33 eV from valence band[9]. Doping with gold does not require exact control of the quantity of dopants to achieve the resistivity needed, and also the gold is among most studied materials in the litterature [93–95]. Other materials could be used such as Co, Pd, and Ag as dopants to increase substrate resistivity Table 3.4.

Table 3.4: Substitutional position of energy levels of other atoms than Au.

Atom	Donor level at Ec-	Acceptor level at Ev+
Co	0.89	0.82
Pd	0.84	0.90
Ag	0.75	0.55
Au	0.78	0.56

[9] In the Table 3.4, the donor level is defined relatively to the conduction band E_c, while acceptor level is defined relatively to the valence band E_v. There is no rule that imposes the definition. Conversly, it is possible to define the donor level relatively to the E_v, and the acceptor level to the E_c

3.5.1 Deep Level Trap Compensation

Doping silicon is a common way that is used today, the most known doping are boron and phosphorus. They create only one energy level in the silicon bandgap, that is to close to the valence or conduction band. Having dopants that are too close to one of the bands are called shallows dopant. On the other side, dopants that create energy level far from the bands are called deep level dopants. Those definitions of shallow and deep dopants have not been well defined in the scientific community.

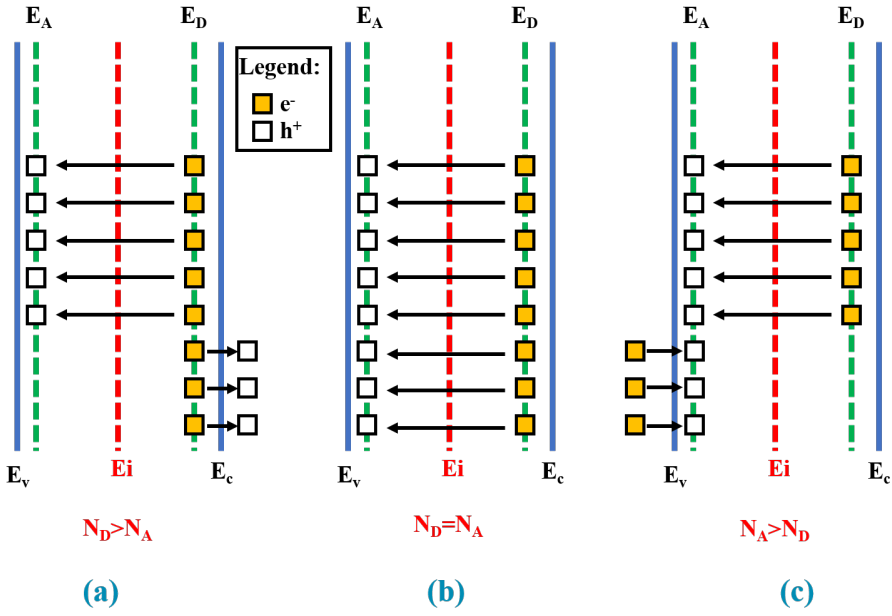


Figure 3.21: Shallow trap compensation effect in silicon for **(a)**: $N_D > N_A$, **(b)**: $N_D = N_A$ and **(c)**: $N_A > N_D$

.

When shallow donors and acceptors are simultaneously present in the silicon bandgap, two trap levels E_D[10] are created (created by the shallow donor)

[10] In this thesis: E_D stands for shallow donor energy level, E_A for shallow acceptor level, E_{DD} for deep donor energy level and E_{DA} for deep acceptor energy level. E_c is the conduction band and E_v is valence band.

close to E_c, and E_A (by the shallow acceptor) close to E_v thus the compensation will happen. Electrons from the E_D will be captured by the traps from E_A [96] (see Figure 3.21).

The resultant type of silicon is determined by the concentration of dopants. If the donor concentration N_D significantly exceeds the acceptor concentration N_A, the substrate becomes n-type. Conversely, if the acceptor concentration is much larger, the substrate becomes p-type. But, when N_D=N_A, full compensation happen and no free carriers are available in the silicon.

Figure 3.22(a) shows an explanation of a compensation of the donors by deep acceptors while the Figure 3.22(b) shows the compensation of the acceptors by deep donors.

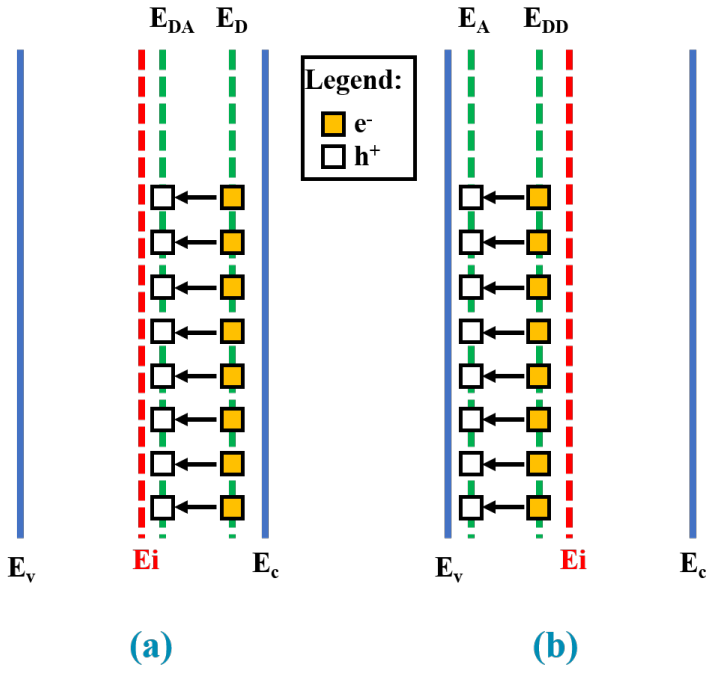


Figure 3.22: Shallow trap compensation effect in silicon for (a): shallow donor and deep acceptor levels and (b): shallow acceptor and deep donor levels.

Compensation happens always between acceptors and donors whatever their position is in the silicon band-gap. Electrons from E_D are first exited to conduction band and then, fall down to the E_{DA} and recombine by holes (see **Figure 3.22(a)**). In the case of gold atoms, both EDA and EDD are present in the silicon band-gap. It is important to note that the E_{DA}, E_{DD}, E_A and E_D are generated by the atoms, and the density of thoses traps/dopants depends on the dose implanted. Moreover, in the case of gold atoms, both E_{DD} and E_{DA} are present in the silicon bandgap (see **Table 3.4**), which is similar to the case in **Figure 3.22(a)**.

3.5.2 Deep Traps in the Silicon

One advantage of using gold as a dopant is that the precise quantity does not need to be tightly controlled. **Figure 3.23** shows the calculated resistivity at room temperature of boron-doped silicon as a function of donor trap concentration for several generic donor levels. All the curves of generic donors reach a maximum of around 600 kΩ·cm when the ionised donors compensate the boron concentration, Fermi level is then around silicon mid-gap. After the maximum, the over-compensation hapens due to the excess of ionised donors making the substrate n-type.

Theoretically, it is possible to compensate the boron dopants using donor traps at various positions in the silicon band-gap such as Phosphorus where it creates a donor level at E_c - 0.045 eV. However, when the trap is at E_c - 0.045 eV, exactly 1×10^{14} cm^{-3} is needed to achieve resistivities higher than 10 k$\Omega \cdot$cm. Conversely, using a donor at E_c - 0.7 eV allows for more flexibility in the donor density, achieving resistivities higher than 20 k$\Omega \cdot$cm with doping densities between 5×10^{14} cm^{-3} and 9×10^{17} cm^{-3}.

Gold atoms have a donor trap level at E_c - 0.78 eV as depicted in **Table 3.4**, which is close to the donor level at E_c - 0.8 eV in **Figure 3.23**, explaining the choice of gold in this study.

It is worth knowing that the data in **Figure 3.23** are calculation (not measurements), doping gold above around 1×10^{17} cm^{-3} is not physically possible due to the maximum solubility of gold in silicon **[97]**.

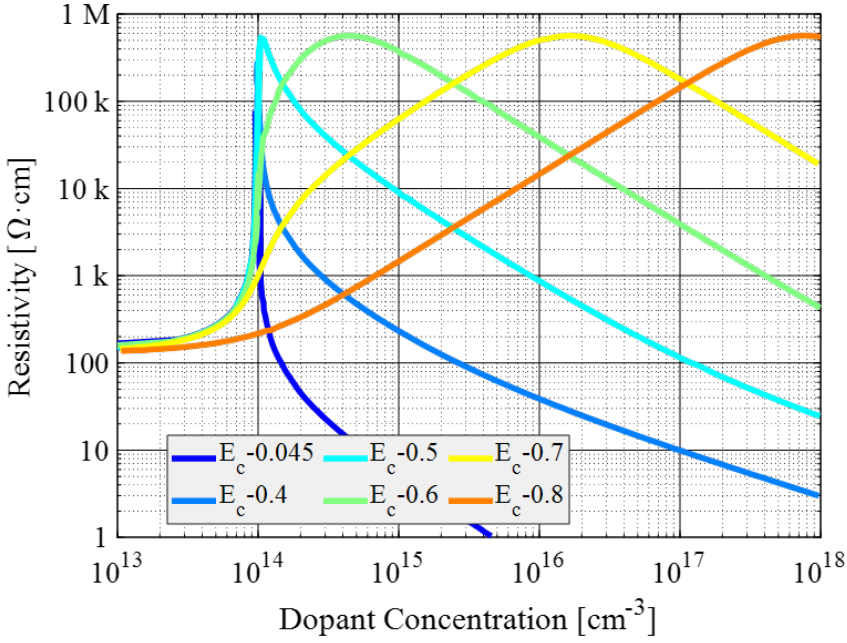


Figure 3.23: Calculated resistivity of p-type silicon with a boron concentration of 1×10^{14} cm^{-3} doped with generic donors exhibiting various ionization energy levels. From [88].

3.5.3 Au-Si Substrate Fabrication Process

6-inch Czochralski-grown silicon wafers with a (100) crystal orientation were selected as the starting materials. These n-type, phosphorus-doped wafers have an average thickness of 675 µm and a nominal resistivity ranging from 50 to 60 Ω · cm. To protect against implantation damage and prevent out-diffusion of gold during the subsequent annealing process, a 20 nm-thick sacrificial oxide layer was grown on top of the wafers using a dry oxidation process in a Tempress furnace at 1000 °C for 15 minutes.

Au atoms were introduced at the backside of the wafers with a dose of 4×10^{13} cm^{-2} at an energy of 100 keV (see **Figure 3.24(a)**) using ESPRC ion-implantation facility located at the University of Surrey. Once implanted, the wafers were treated under annealing condition of 950 °C for 1 hour in

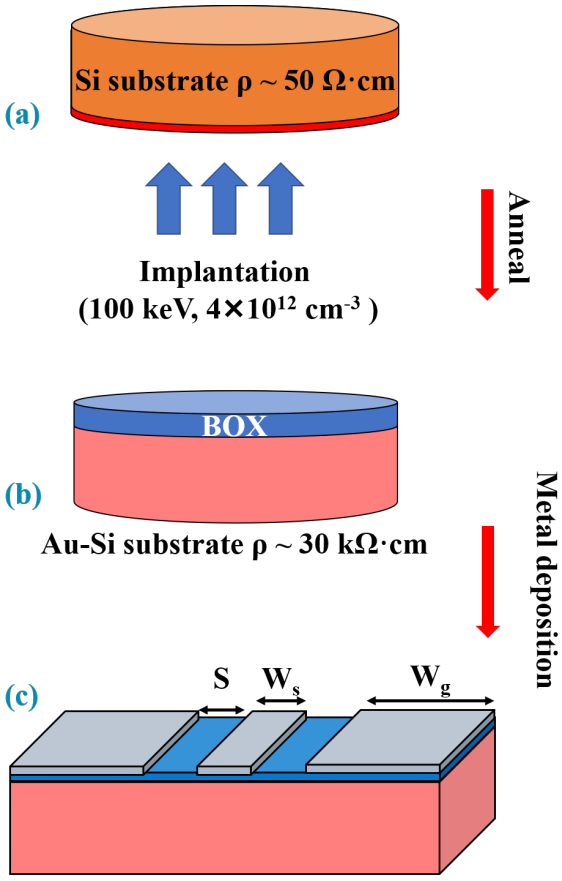


Figure 3.24: Fabrication process of the Au-Si substrate beginning with a standard resistivity substrate: implantation in **(a)**, activation in **(b)**, and CPW line fabrication in **(c)**.

Argon environment to activate the Au dopants. The implantation details and annealing temperature were optimised values obtained in **[98]**. Accordingly, the combination of this particular implantation dose and annealing temperature provides the highest resistivity enhancement (see **Figure 3.24(b)**).

The substrate has an insulating layer with thickness of BOX = 200 nm that was deposited using low-pressure chemical vapor deposition (LPCVD). The 50 Ω CPW line was defined as: W_c = 26 µm (central signal conductor width), S

= 12 µm (signal-to-ground line spacing) and W_g = 208 µm (ground conductor width) as depicted in **Figure 3.24(c)**.

3.5.4 Electrical Characterization

Deep level compensation technique has showed its capabilities to improve the RF performance of the substrate by reducing attenuation from 0.8 dB/mm to 0.3 dB/mm [99], for CPW fabricated on gold-doped silicon and standard silicon, respectively. Resistivities around 100 k$\Omega \cdot$cm have been achieved for gold-doped silicon substrate [98]. It was also shown that this technique can suppress the PSC effects [91], however the non-linearities of the gold-doped silicon substrate and its performances under large RF signal have not been reported in the literature yet.

Effective Resistivity as a Function of Frequency

Figure 3.25 demonstrates the effective resistivity versus frequency for 3 si-based substrates, Au-Si, eSI80^{TM} and HR substrate, all the substrates have the same BOX thickness that is 200 nm.

The HR substrate suffers from PSC: the effective resistivity is therefore low as expected, and shows a value of around 40 $\Omega \cdot$cm at 4 GHz. This low value translates to an increase in the CPW line's RF losses. The eSI80^{TM} substrate effectively mittigates the PSC effect and its effective resistivity is reletively high around 10 k$\Omega \cdot$cm at 4 GHz. The Au-Si substrate shows better performances than TR, with an effective resistivity reaching a value of more than 15 k$\Omega \cdot$cm at 4 GHz and translates into low losses of the passive devices designed atop it[11].

The gold atoms in substitutional sites create traps in the bandgap of the silicon, deep donors and deep acceptors at EC- 0.78 eV (0.78 eV below conduction band) and EV + 0.58 eV (0.58 eV above valence band), respectively. The traps created by gold atoms capture free charges in the silicon bulk, the Fermi level at the Si-SiO_2 interface is located near the mid-gap, thereby increasing the overall resistivity.

[11] Several passive devices have been characterized such as one port inducor, band-pass filter and crosstalk atop of Au-Si, TR and HR substrates. They are not reported here, please refer to [5] for more details.

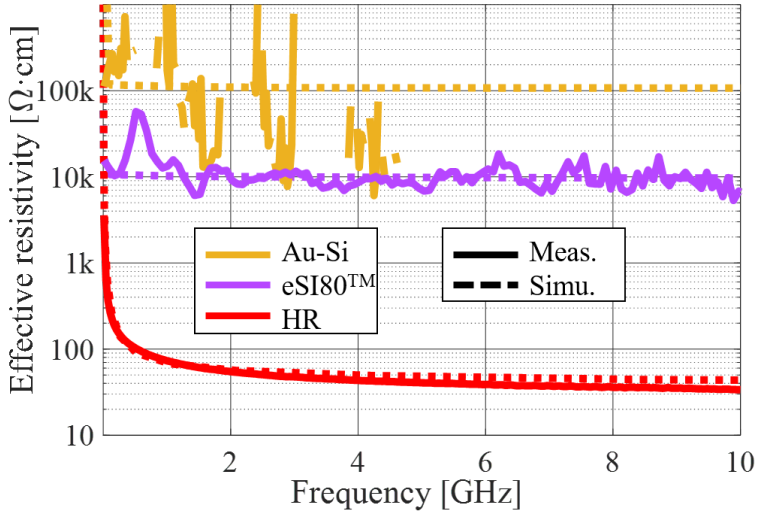


Figure 3.25: Measurement and simulation results of the effective resistivity extracted from CPW lines designed on the three different substrates at 0 V DC bias.

Effective Resistivity as a Function of Applied DC Bias

To better understand the behavior of the substrates, we extracted the effective resistivity as a function of the DC bias points of the CPW line which is depicted in **Figure 3.26**. The effective resistivity of the HR substrate is bias dependent, as we can see it is around 40 $\Omega \cdot$ cm for positive bias points and around 130 $\Omega \cdot$ cm for negative bias points. When applying a positive DC bias we create more electrons below the signal electrode, so that enhance the PSC effect, therefore we register low effective resistivity. When we apply a negative DC bias, we are creating holes below the signal electrode, this leads to the creation of a depletion region between the signal and ground electrodes. The electric field will face a high resistive region between the signal and ground electrodes, so the effective resistivity is relatively high compared to when we apply a positive DC bias.

For the eSI80^{TM} substrate, the effective resistivity is bias independent and is around 10 k$\Omega \cdot$ cm. The bias independency is due to the traps created by the polysilicon, so when electrons (or holes) are generated in the substrate

by applying a positive (or negative) DC bias, they are captured by the traps and do not participate to conduction, or alter the effective resistivity. In the Au-Si substrate, the effective resistivity is high but also shows some bias dependency. This is because the traps created by gold are sufficient to counter the oxide charges, but not to counter the high number of carriers induced by the application of several Volts of DC bias.

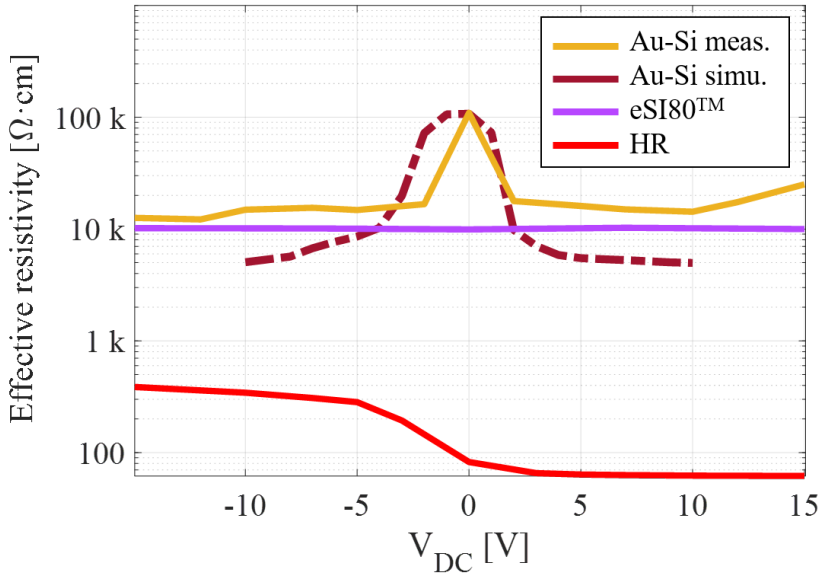


Figure 3.26: Extraction of the effective resistivity as a function of DC bias for the Si-based substrates at 2 GHz.

Harmonics at 0 V DC bias

The harmonics H2 and H3 measured at the output of the CPW line are plotted versus fundamental output power H1 in **Figure 3.27** for the Si-based substrates described above at 0 V DC bias. It is shown that the HR substrate presents high harmonic distortion and shows a value of the second harmonic of -53.37 dBm at an input power of 15 dBm due to its low effective resistivity (around 40 $\Omega \cdot$cm). The TR substrate shows better linearity compared to HR (H2 = -80 dBm at an input power of 15 dBm) due to its higher effective resistivity (around 10 k$\Omega \cdot$cm). The Au-Si shows a second harmonic of -111 dBm at an input power of 15 dBm because of its high effective resistivity compared to TR.

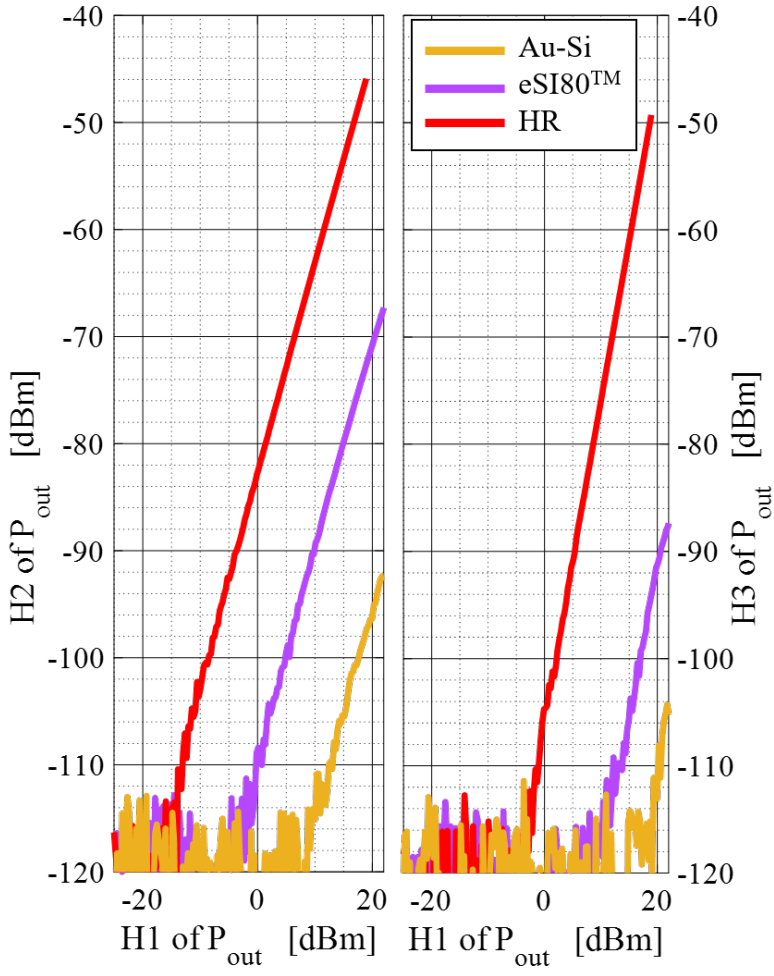


Figure 3.27: Measured H2 (left) and H3 (right) for CPW line built on Au-Si, HR and eSI80^{TM} substrates versus fundamental H1 output power at 900 MHz and at 0 V DC bias.

Harmonics as a Function of Applied DC Bias

The variation of the second harmonic (H2) at an output fundamental power H1 = 15 dBm with the applied DC bias for the described substrates is depicted in

Figure 3.28. While TR is almost bias independent (variation in a small range between -80 and -81 dB), the HR shows high H2 values and is strongly bias dependent varying from -14 to -54 dBm over the measured DC bias range. For the Au-Si substrate the harmonic distortion (HD) is quite low at 0 V (-105 dBm), however large degradations in H2 are observed at the other DC bias points (variation between -65 and -90 dBm). Simulations of the Au-Si agree quite well with measurements.

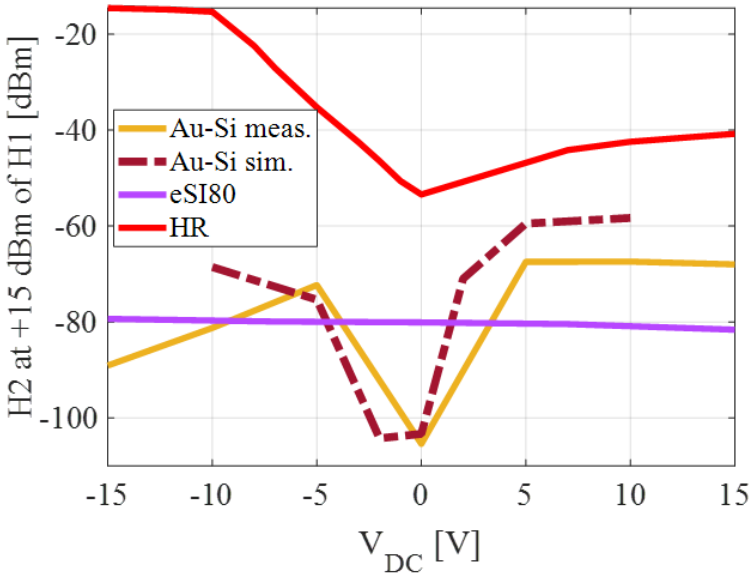


Figure 3.28: Measured variation of the second harmonic at H1 = 15 dBm with the applied DC bias for the three different substrates.

Fermi Level Localization

In order to explain the behavior of Au-Si under large signal, we simulated the Fermi level below the signal electrode of the CPW line just at the Si-SiO_2 interface and was represented in Figure 3.29 as a function of the applied DC bias. Moreover, the Equation 3.1 shown the space charge density extracted from Poisson's equation:

$$\rho = q \times (p - n + N_D - N_A + \rho_p - \rho_n) \tag{3.1}$$

Where q is the elementary charge, p and n the hole and electron concentrations, respectively. N_D, N_A, ρ_p and ρ_n are donor impurities, acceptor impurities, trapped holes and electrons, respectively. It is well known that the HR substrate does not contain traps in the silicon bandgap ($\rho_p = \rho_n = 0$), so the applied DC bias is compensated by a large variation of in free carriers consequently a large variation in the Fermi level as shown in **Figure 3.29**. For the TR substrate the Fermi level is pinned near the mid-gap thanks to the polysilicon layer that introduces high trap density, so the applied DC bias is compensated by activating and deactivating the acceptor(ρ_n) and donor(ρ_p) traps, the value of ρ in the **Equation 3.1** will remain almost constant whatever the value of the applied DC value.

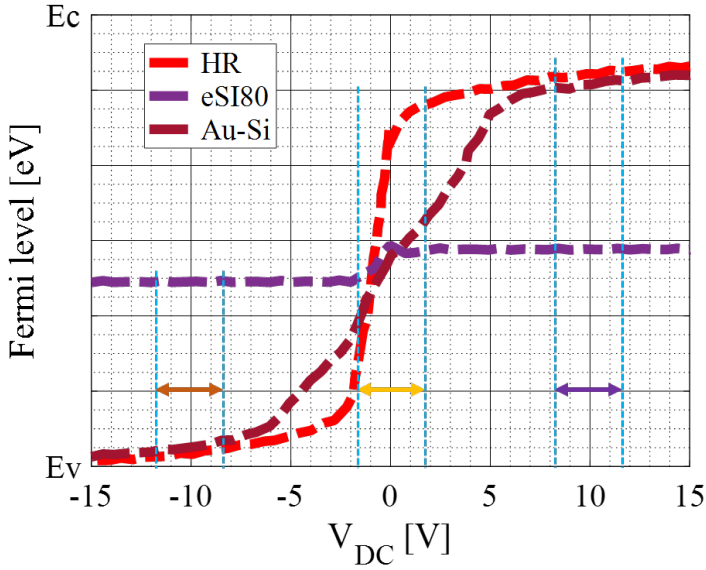


Figure 3.29: Variation of the Fermi level as a function of the DC bias points for Si-based substrates.

The Au-Si substrate shows a different Fermi level behavior comparing to HR and TR. Around 0 V DC bias, when a large signal (15 dBm) is applied (a sine wave of 2 × 1.7 V peak to peak), the Fermi level will oscillate between Ev + 0.62 eV and Ev + 0.4 eV (yellow arrow), the traps are able to compensate this DC bias variation by donor and acceptor traps. In contrast, at 10 V DC bias,

when the same large signal is applied, a high density of electrons is generated in the substrate the Fermi level will oscillate near the conduction band between Ev + 0.98 eV and Ev + 1.01 eV (purple arrow), this is because the traps density is not large enough to compensate the applied DC bias. The same for -10 V DC bias, where we will have a high density of holes and the traps can not compensate this amount, consequently the Fermi level oscillate between Ev + 0.01 eV and Ev + 0.06 eV (brown arrow).

The position of the Fermi level near the mid-gap allow us to say that the linearity of the substrate is high enough, however when its position is close to one of the bands there will be an excess of free carriers that will be modulated by the applied signal thus lower linearity, leading to a low harmonic distortion for 0 V and higher harmonic for other DC bias points.

Impedance Seen by the CPW Line

The non-linearities of the studied substrates are described using an impedance network at the Si-SiO_2 interface. As shown in **Figure 3.30** , Zsignal represents the impedance below the signal electrode and Zsig-gnd is the impedance at the Si-SiO_2 interface between signal and ground electrodes.

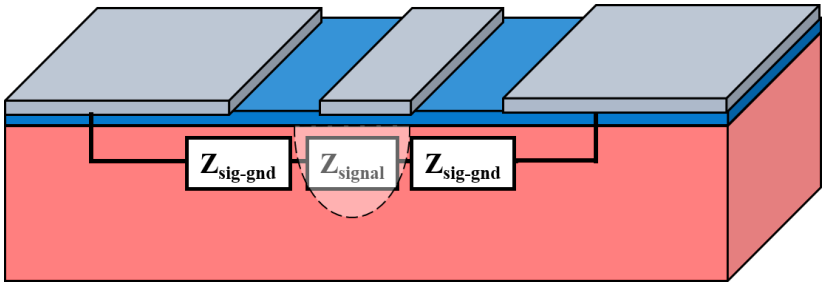


Figure 3.30: Substrate modeling using the impedance seen by the CPW line.

The HR substrate presents a highly non linear impedance Zsignal (very low impedance) that is in series with very low impedance Zsig-gnd due to the large quantity of electrons (PSC effect), thus the overall impedance is low, so the substrate is non-linear. In contrast to HR, the TR substrate shows a high Zsig-gnd impedance as it overcomes the PSC effect, and relatively low variation below the signal electrode (Zsignal) as shown in **Figure 3.29**, so the overall

impedance seen by the CPW line is high and can not be influenced by the large signal applied to it. This explains the high linearity of the TR substrate and its bias independence.

The non-linear behavior of the substrate beneath the central CPW line on the Au-Si substrate is similar to that on HR, as **Figure 3.29**. The interface Fermi level is not pinned by the traps as in the TR case, so we have a highly nonlinear impedance Zsignal. However, in the Au-Si substrate this non-linear impedance (Zsignal) comes in series with a highly resistive impedance Zsig-gnd, and so its contribution to the overall CPW shunt impedance is attenuated, and as a result the harmonic distortion is significantly lower than for HR. Table. I summerizes the linearity (variations) of Zsignal and the value of the series impedance Zsig-gnd (the overall impedance linearity is the sum of the two latters) of the CPW line lying on the Si-based substrates.

3.5.5 Benchmarking

The Au-Si substrate several advantages, notably its low cost due to the use of standard resistivity substrates. Additionally, it introduces traps throughout the entire thickness of the substrate, making it suitable for various applications in integrated passive devices (IPDs) **[100, 101]**. This method enables the design of integrated filters in silicon, as demonstrated in **[102]**, and can also be used for impedance matching networks and quadrature couplers **[103]**. Furthermore, it is applicable for variable attenuators in mmW applications **[104]**, where gold has been used as a contact material. Since high-resistivity (HR) substrates are employed with contacts to the BOX, the phenomenon of PSC is present. It is important to highlight that standard resistivity substrates with gold doping can be utilized instead of HR with PSC. Gold can also be used to design circuits such as passive phase shifters **[105]**, including LC phase shifters or transmission line phase shifters. Morover, AuSi can be used to fully encapsulated semi-insulating silicon-on-insulator (SOI) substrates **[97]**, where it is expected to prevent the diffusion of gold into the active layer.

However, there are notable drawbacks. The gold is not CMOS-compatible due to the high diffusion rate of gold atoms. Moreover, it is not suitable for use in CMOS foundries since any airborne gold particles could reach the transistor channel, degrading its performance by reducing mobility through trapping phe-

nomena.

It is worth highlighting that the Au-Si substrate demonstrates very good RF performance reaching high effective resistivity close to that of the eSI100^{TM} and similar value of H2 power level at 0 V (see Table 3.5). Even if its linearity is bias dependent, it demonstrates around 20 dB improvement compared to the HR substrate at different bias point (15 V for example).

Table 3.5: **Au-Si** RF performance comparison to the HR and TR eSI80^{TM} eSI100^{TM} references.

Substrate	ρ_{eff} at 2 GHz [$\Omega \cdot$ cm]	ρ_{eff} Bias Dependency	H2 at H1=15 dBm [dBm]
HR	100	YES	-50
eSI80^{TM}	10 k	NO	-80
eSI100^{TM}	40 k	NO	-100
Au-Si	**40 k**	**YES**	**-100**

3.6 Porous Silicon Substrate

Another substrate that mitigates the PSC effect is the porous silicon substrate, which has been proposed and studied for several decades. This material is created from a highly doped silicon substrate through the electrochemical dissolution of bulk crystalline silicon [106, 107]. The process involves the anodic etching of silicon in a hydrofluoric acid-based solution, which results in the formation of a porous network with a high surface area.

Porous silicon (PSi) is distinguished by its very low effective permittivity, achieving values 3 to 4 times lower than those of conventional silicon-based substrates. This significant reduction in permittivity leads to decreased capacitive coupling and crosstalk between adjacent devices [108–111], which are critical factors in high-frequency and RF applications.

At UCLouvain, high-quality PSi has been developed using either standard resistivity (10-20 Ω·cm) substrates [112] or heavily doped substrates (1 mΩ·cm) [113]. For industrial CMOS processes, the PSi fabricated from standard resistivity 20 Ω·cm substrates is the most suitable due to its low cost.

Usually, PSi is fabricated in a pre-process, meaning it is fabricated first, followed by the deposition of silicon buried oxide, and then metallic CPW lines are deposited atop it. However, due to its lack of mechanical robustness, it is difficult to implement the conventional CMOS process on this fragile substrate.

In [114], a post-process porous silicon method was introduced. The idea is that once the passive devices are fully processed, porosification from the back side of the wafer is performed, targeting passive devices. However, it is expected that the HF electrolyte used during the process will not only etch the monocrystalline silicon but also the insulating layer, leading to the undermining of the entire structure. To overcome this issue, a thin etch-stop layer resistant to HF is introduced below the BOX and the silicon bulk during the pre-process, forcing the HF to etch exclusively the silicon bulk, as demonstrated in **Figure 3.31**.

Significant efforts have been made by the scientific community in processing porous silicon for various domains such as optics and RF applications. However, comprehensive modeling of this substrate remains an area that has

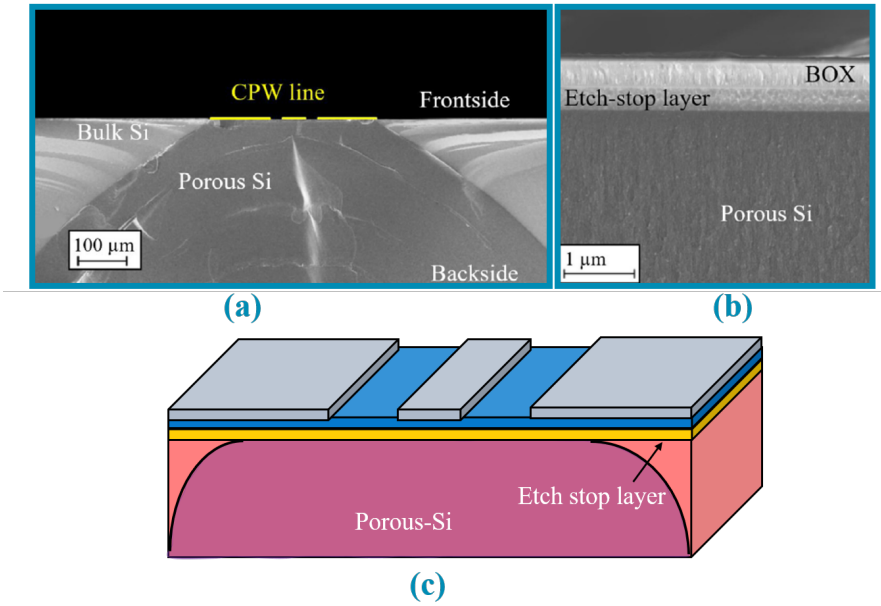


Figure 3.31: Cross-sectional view of post-process porous silicon substrate **(a)** over full substrate thickness and **(b)** magnified view at the frontside of the wafer. Both images obtained from scanning electron microscopy (SEM). **(c)** schematic view of the post-process porous silicon.

not been fully explored.

The primary contribution of this thesis is the detailed modeling of porous silicon substrates and their simulation using ATLAS Silvaco. This work includes predicting the effective resistivity and harmonic response of the material through the quantification of traps within the substrate. By providing a robust model, this research aims to bridge the gap between the physical properties of porous silicon and its practical applications, offering valuable insights for future technological advancements.

3.6.1 Fabrication Process

Several recipes for porous silicon for RF applications are available. In this thesis, one type of porous silicon is introduced and is pre-processed. A 380

µm-thick heavily doped p-type silicon 3-inch wafer from SIL'TRONIX with a resistivity ranging from 0.6 to 0.8 m$\Omega \cdot$cm serves as the initial substrate. Prior to processing, the wafer undergoes a cleaning procedure using nitrogen gas flow, and a thin layer of sacrificial material is removed. Similar to [115], porous silicon (PSi) is then prepared through anodization in a solution with a 3:1 volume ratio of HF (49%) to ethanol. The etch cell has a radius of 3 cm, and the growth of porous silicon is isotropic. SEM picture of the resulted substrate and the porosified region and the schematic view are depicted in Figure 3.32.

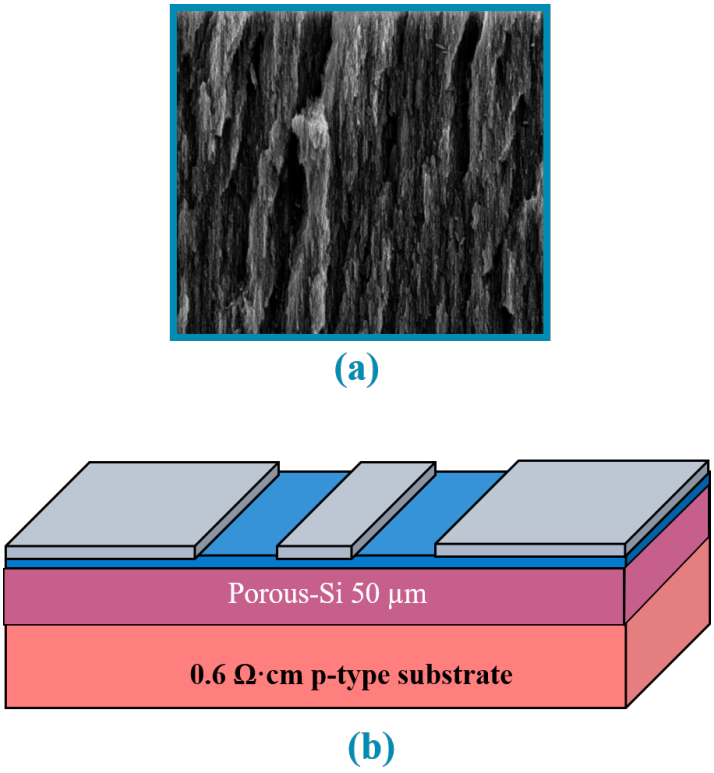


Figure 3.32: Micro-photograph of the porous silicon fabricated in Winfab (UCLouvain) in (a), and in (b) a schematic view of the pre-process porous silicon.

3.6.2 Discrete Levels of Traps in the Porous Silicon

Extensive research has been conducted worldwide to understand the fundamental properties of porous silicon. A major discovery came in 1990 when it was found that highly porous silicon could emit visible photoluminescence at room temperature. This finding led to significant interest in the material, and since then, its structural, optical, and electronic properties, including trapping effects, have been thoroughly studied [116].

As discussed throughout this thesis, trapping phenomena play a crucial role in RF applications by pinning the Fermi level, which in turn reduces losses and improves linearity. In porous silicon, it is expected that traps originate from the chemically degraded (broken) monocrystalline silicon network. Unlike trap-rich substrate, where the Fermi level is pinned thanks to the traps in a thin 1.65 µm polysilicon layer, porous silicon introduces trapping centers located much deeper within the substrate, around 50 µm into the substrate volume. This is characteristic of pre-process porous silicon. However, in the case of post-process porous silicon, the entire substrate thickness becomes porosified, resulting in trapping centers being distributed uniformly throughout the entire volume. These traps are primarily located along the pore walls [112].

To model these traps, it is essential to determine their density and position within the silicon band-gap. One effective technique for achieving this is optically charging spectroscopy (OCS), which has been employed to identify the position of traps related to defects created by the porous silicon structure. This method, as demonstrated in [117], enables a precise understanding of the traps' positions within the silicon band-gap, providing valuable insights into their impact on the material's electronic properties.

Optically charging spectroscopy (OCS)[12] is a zero-bias method utilized to investigate trapping levels in high resistivity materials. The sample is polarized

[12]The OCS method closely resembles the PICTS technique, as both methods require the sample to be cooled and subsequently illuminated. Following illumination, the sample is heated while the resulting discharging current is measured. Despite these procedural similarities, a key distinction exists between the two methods: the OCS technique does not require the application of a bias, whereas the PICTS method necessitates an applied DC bias. This difference makes the OCS method simpler in terms of experimental setup, as it eliminates the need for external biasing equipment, while PICTS relies on the bias to capture charge carrier dynamics under specific conditions.

by illumination at sufficiently low temperatures. Photo-generated electron-hole pairs diffuse into the sample, and if trapping centers are present within the material or on its surface, these non-equilibrium carriers are captured and prevented from being released into the conduction and/or valence bands, for more details about the measurement method please refer to [118–120].

After using the OCS measurement method on fresh samples, it has been concluded in [117] that a the porous silicon contains 5 discrete levels of traps that are named A, B, C, D, and E. Where A: at Ev + 0.29 eV, B: at Ev + 0.37 eV, C: at Ev + 0.41 eV, D: at Ev + 0.47 eV and E: at Ev + 0.61 eV as depicted in Figure 3.33. Similar studies have been performed by same authors in [121, 122] demonstrating same results.

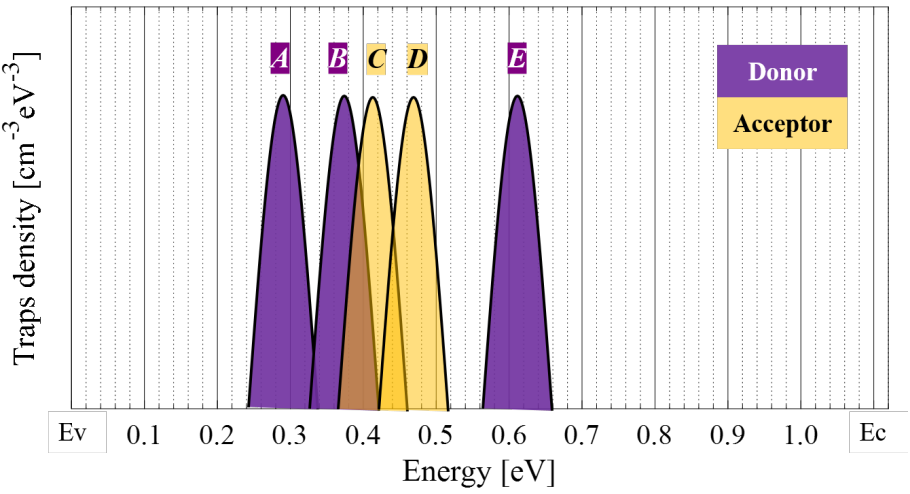


Figure 3.33: Position of the trapping centers in the silicon band-gap for porous silicon fabricated starting from 10-12 $\Omega \cdot$cm as measured by [117].

3.6.3 Characterization of the Recent Porous in UCLouvain

Small- and large-signal measurements have been performed on the described pre-process porous silicon using CPW line having the dimensions 26, 12, 208 μm for width of the central track, spacing between the signal and ground, and width of the ground, respectively.

The simulations were conducted using Atlas Silvaco. The modeling of the porous silicon was performed by considering a 50 μm thickness of semiconductor material, with a relative permittivity of 3. The spatial distribution of traps throughout the 50 μm volume was assumed to be constant, with trap positions as indicated in **Figure 3.33**. Several iterations were carried out to refine the trap density, adjusting it to match experimental measurements, and it was ultimately set to 5×10^{17} cm^{-3}.

Figure 3.34 shows the measured and simulated CPW line parameters (**(a)**: effective resistivity, **(b)**: effective permittivity, **(c)**: losses of the CPW line and **(d)**: impedance characteristic of the CPW line) where the simulations agree well with measurements.

The value of the characteristic impedance Z_c is around 90 Ω, which is expected due to the reduced capacitance of the transmission line. Since:

$$Z_c = \sqrt{\frac{L}{C}} \tag{3.2}$$

When the capacitance of the line C is reduced, the value of the characteristic impedance Z_c increases. The total losses are dominated by the metallic losses of the CPW and are considerably reduced.

The effective permittivity is around 3, a very low value compared to HR and TR substrates, where it is around 11. This low permittivity leads to reduced coupling through the substrate.

The effective resistivity of the porous silicon is fluctuating around 10 kΩ·cm (due to the conductance that it close to zero), it is expected that the traps in the porous region will disable the effect of oxide charges and the effect of the carriers from a heavily doped bulk silicon substrate.

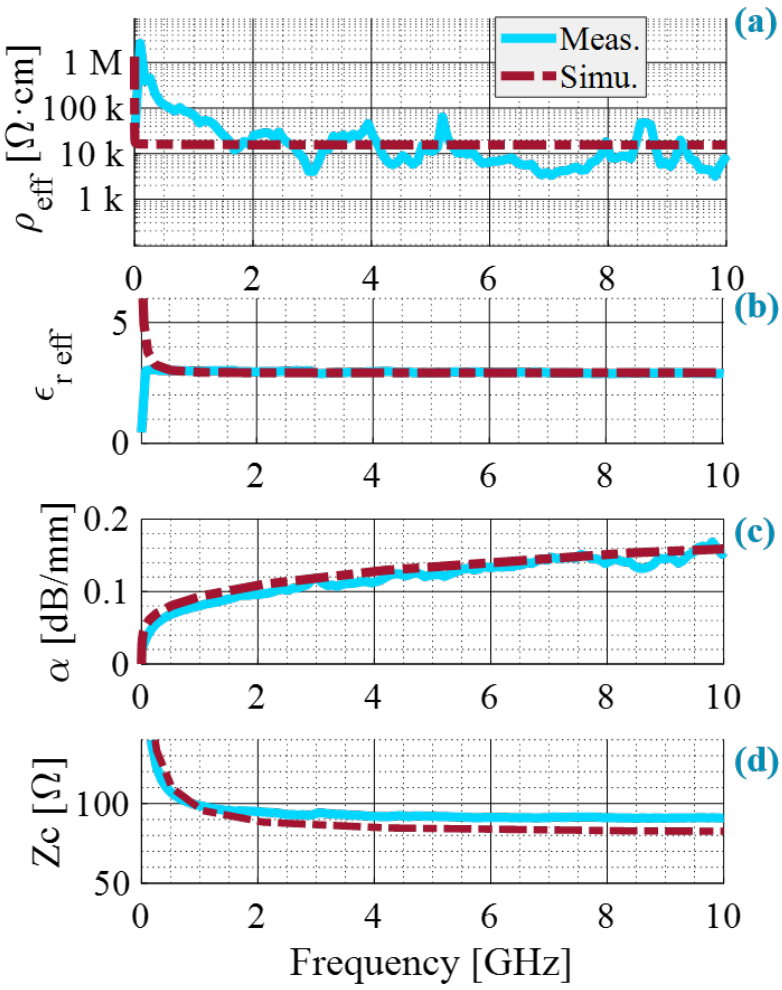


Figure 3.34: Measured and simulated of the **(a)**: effective resistivity, **(b)**: effective permittivity, **(c)**: losses of the CPW line and **(d)**: impedance characteristic of the CPW line.

Figure 3.35 shows the measured and simulated effective resistivity at 2 GHz versus the applied DC bias.

The measurements indicate a bias-independent value of ρ_{eff} around 10

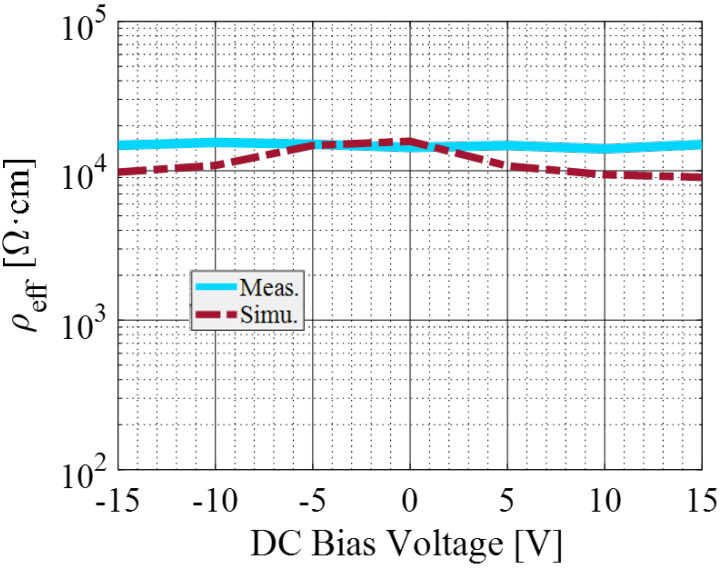


Figure 3.35: Measured and simulated of the effective resistivity at 2 GHz versus applied DC bias between the signal track and the ground.

kΩ · cm. This is attributed to the fact that the Fermi level below the CPW line is completely pinned near the silicon mid-gap. The traps inside the porous silicon (PSi) are not only able to counteract the positive oxide charge and free carriers from the bulk but also the charges created by the applied DC bias.

Figure 3.36 shows the measured and simulated of the second (H2 at 1.9 GHz) and third (H3 at 2.7 GHz) harmonics versus the fundamental power output H1 (f_0 at 900 MHz) for the porous silicon described above[13].

The simulations closely match the measurements. The third harmonic is around 150 dBm at an output power of H1= 15 dBm, the second harmonic is at -130 dBm which is 30 dB more linear than the commercially available

[13]Measurements of the second harmonic (H2) as a function of the applied DC bias were not conducted in this work due to time constraints. However, based on the demonstrated bias independence of the effective resistivity, we are confident that H2 would also remain unaffected by DC bias. Since the second harmonic response is closely tied to the substrate's resistivity profile, which has been shown to be stable across various bias conditions, we hypothesize that H2 will exhibit similar bias independence.

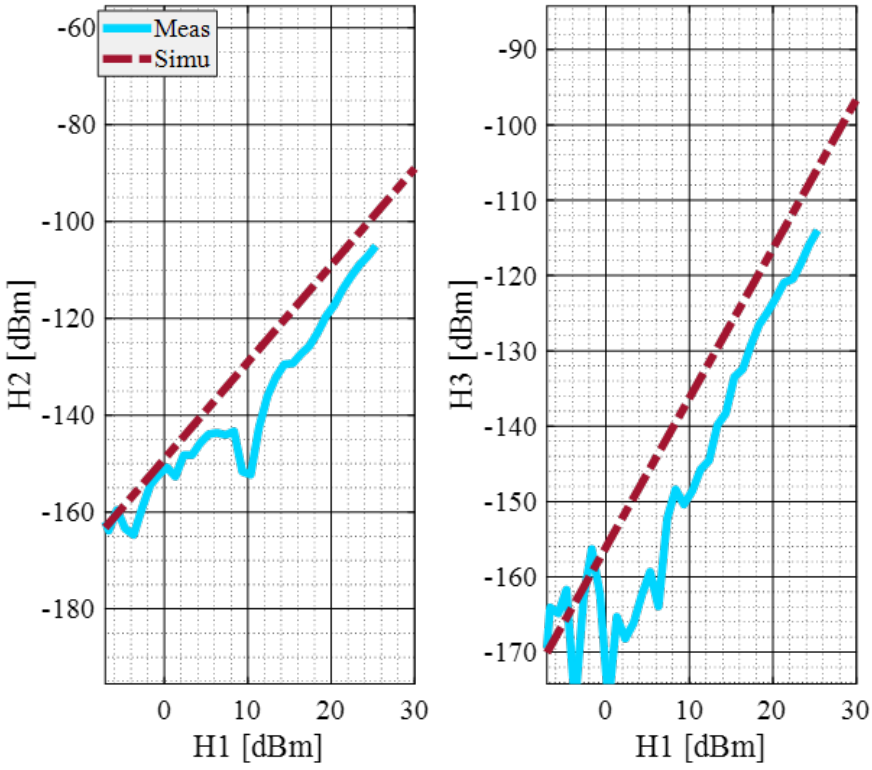


Figure 3.36: Measured and simulated of the second (H2 at 1.9 GHz) and third (H3 at 2.7 GHz) harmonics versus fundamental (f_0 at 900 MHz) for the porous silicon. (Incize's low noise setup has been used).

eSI100^{TM} manufactured by SOITEC. This very low value of H2 is attributed to the high density of trapping centers originating from the porous walls. Since almost no free carriers exist within the 50 µm below the CPW line, the porous layer resists to the modulation by the large RF signal.

Moreover, the slight dip observed in the measurement of H2 is not related to measurement at an input power of H1=10 dBm, and remains unexplained. Further detailed investigation is required to identify the root cause of this dip.

3.6.4 Discussion

The model described in this thesis serves as a starting point for further efforts in modeling substrates. It is based on the assumption that all porous silicon recipes worldwide are identical. However, it is evident that recipes for porous silicon differ from one to another, whether starting from p++ or a standard substrate, or even from pre-process to post-process. It is possible that the traps change position from one recipe to another, which is a current topic of investigation.

Nonetheless, the only effective way to model porous silicon is based on the work done in [117]. Moreover, we are convinced that the only reliable methods to quantify the traps are optical or thermal techniques (OCS or PICTS), as our CV measurements on porous or trap-rich substrates have shown that it is impossible to shift the Fermi level by applying a DC bias (a sweep was performed between -100 and 100 V, and the CV curve still flat).

These scientific results will further encourage the scientific community to invest efforts in the comprehensive characterization of this high performance substrate. It is worth noting that the best approach is to fabricate multiple porous silicon recipes and forms. Each wafer should then be characterized to extract the traps within the porosified region. Following this, an RF prober should be used to extract the Figure of Merit (FoM) of the substrate.

Furthermore, measurements indicate that the second harmonic H2 = -130 dBm at an output power of H1 = 15 dBm. Despite the lack of robustness in this substrate, it exhibits remarkable linearity, much better than that of trap-rich silicon. Its H2 is 30 dB lower than that of eSI100™ when H1 = 15 dBm.

3.6.5 Benchmarking

Porous silicon offers several advantages and drawbacks that have been studied extensively. One of the primary benefits of the porous silicon substrate is its low cost. Additionally, it possesses a very high effective resistivity, similar to that of trap-rich silicon substrate (see Table 3.6). The second harmonic is 30 dB lower than the most advanced eSI100™, due to the high density of traps contained within the 50 µm thick porous region.

However, the reproducibility of the same recipe is challenging, sometimes

even within the same wafer. The mechanical strength of PSi is very low, making it necessary to use robust |Z| probes for measurements and to make contact as delicately as possible. Despite its promising properties, the porous silicon substrate is not yet a mature technology, having been discovered only in 1990. Furthermore, it has been shown in [123] that the thermal conductivity of porous silicon is 3-5 orders of magnitude lower than that of bulk silicon. This thermal conductivity further decreases as the substrate's porosity increases.

Table 3.6: **Porous silicon** RF performance comparison to the HR and TR eSI80^{TM} eSI100^{TM} references.

Substrate	**ρ_{eff} at 2 GHz** [$\Omega \cdot$ cm]	**ρ_{eff} Bias Dependency**	**H2 at H1=15 dBm** [**dBm**]
HR	100	YES	-50
eSI80^{TM}	10 k	NO	-80
eSI100^{TM}	40 k	NO	-100
Porous	**10 k**	**NO**	**-130**

3.7 Heat Dissipation Through Silicon Substrate

The thermal conductivity of silicon substrates is a critical parameter that has attracted significant attention, especially in determining whether the substrate effectively dissipates heat or not. In this work, substantial efforts have been devoted to the electrical characterization of the substrate. However, it is equally crucial to consider the impact of substrate self-heating, which plays a significant role in the performance and reliability of silicon-based devices.

In **Figure 3.37** (from **[124]**), the thermal conductivity of silicon is presented as a function of doping concentration, ranging from 10^{13} to 10^{20} cm^{-3} for a boron-doped silicon substrate at 23 °C. The results, as shown in the plot, reveal that the thermal conductivity of a standard silicon substrate with a resistivity of 15 $\Omega \cdot$cm is nearly identical to that of a high-resistivity substrate with a resistivity of 1.5 k$\Omega \cdot$cm. The data demonstrate that thermal conductivity remains almost constant up to a doping concentration of approximately 10^{17} cm^{-3}. This behavior indicates that in lightly doped silicon, the thermal conductivity is not significantly affected by the doping level. As a result, both standard silicon substrates and high-resistivity substrates have similar heat dissipation abilities up to a doping concentration of 10^{17} cm^{-3}. However, beyond this doping level, the thermal conductivity decreases significantly. This drop is caused by higher doping levels, which increase the scattering of heat-carrying particles, known as phonons.

In the range of this study, the substrates used have resistivities ranging from 1.6 $\Omega \cdot$cm to 1.5 k$\Omega \cdot$cm (HR substrate). Within this range, no significant effects have been observed, indicating that the substrate resistivity does not noticeably impact the outcomes under the studied conditions.

It is clearly demonstrated that for doping concentrations above 10^{18} cm^{-3} , the resistivity of the silicon substrate becomes very low, which leads to a reduction in thermal conductivity and an increase in substrate losses. However, it is important to note that the substrate also exhibits high linearity in this doping range. This linearity arises because, in highly doped substrates ($> 10^{18}$ cm^{-3}), the substrate's response is not significantly influenced by variations in the large signal applied to it.

In silicon substrates, the generation of harmonics is primarily governed

by variations in local resistivity due to the applied signal. In highly doped substrates, the resistivity is already extremely low, and as a result, any applied large signal has minimal impact on its local resistivity. Specifically, when a negative bias is applied to the signal electrode (as in the case of a CPW line), holes are attracted toward the electrode. Conversely, when a positive bias is applied, minority carriers are drawn toward the electrode. In both cases, the net effect is that the local resistivity of the substrate remains unchanged, rendering the substrate unaffected by the applied large signal.

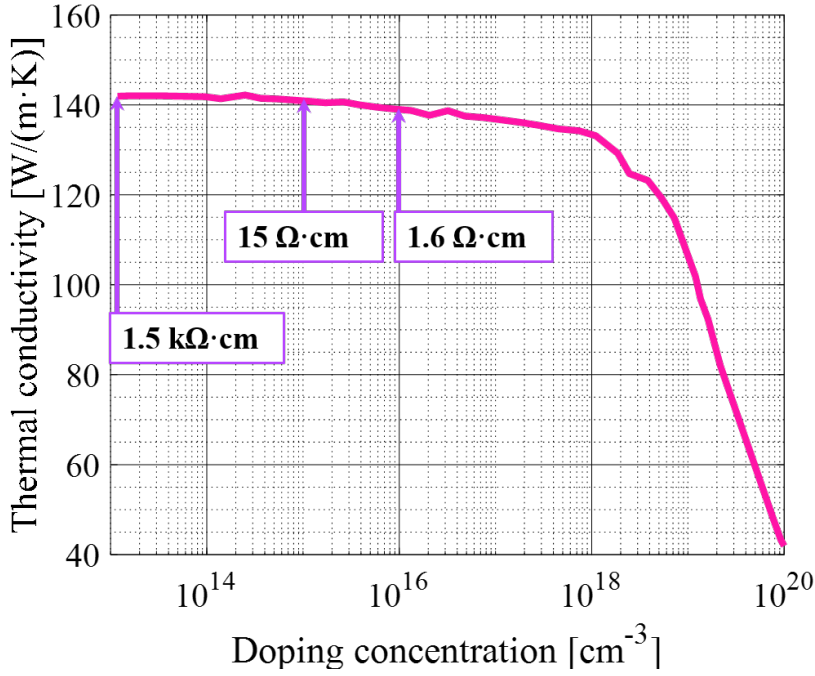


Figure 3.37: Experimental results of thermal conductivity at room temperature (23 °C) in silicon material p-type from [124].

This behavior highlights an important tradeoff: although the highly doped silicon substrate suffers from low thermal conductivity and increased substrate losses, it demonstrates excellent linearity. The lack of resistivity variation under large signal conditions significantly suppresses the generation of harmonics.

Table 3.7: General benchmarking of substrates with the advantages and drawbacks of each solution.

Substrate	Advantages	Drawbacks
PN junctions	• Medium RF performance • FDSOI compatible • No maximum density	• Multiple fabrication runs are often needed to fine-tune the dopants that should be balanced
Double-BOX	• No current leakage to the substrate • Used for RF and digital applications • Allows for the application of both (+) and (-) biases on the back-gate of the FDSOI	• High cost compared to eSI™ • Could not be integrated in today's FDSOI process
Au-Si	• Low cost • High RF performance* • Can be used for IPDs	• CMOS incompatibility • Bias dependent
Porous	• Low cost • High RF performance*	• Low mechanical strength • Not mature technology • Low thermal conductivity compared to bulk

*:Please note that the term "high RF performance" is used broadly here, referring to both high effective resistivity and lower harmonics when compared to an eSI substrate.

3.8 Chapter Summary

In this chapter, a range of innovative and novel substrate solutions are presented to address the PSC effect, as illustrated and summarized in **Table 3.7**. These solutions offer compelling alternatives to the mainstream commercially available trap-rich eSI substrate, which is limited to compatibility with PDSOI technology.

First, it has been demonstrated through a proof of concept that it is possible to integrate the field effect scheme into a commercially available 28FDSOI technology. This approach has shown increased effective resistivity and linearity compared to the high-resistivity substrate.

Second, to avoid the maximum density limitations imposed by the DRC rules for FE passivation, PN implants can be used through the shallow trench isolation (STI). Careful consideration of the energy and dose is necessary to achieve a good balance between the two implants, preventing parasitic connections between similar implants. The PN grid pattern offers simplicity and achieves good RF performance in terms of effective resistivity and linearity, avoiding the need for co-design between RF devices and electric field orientation.

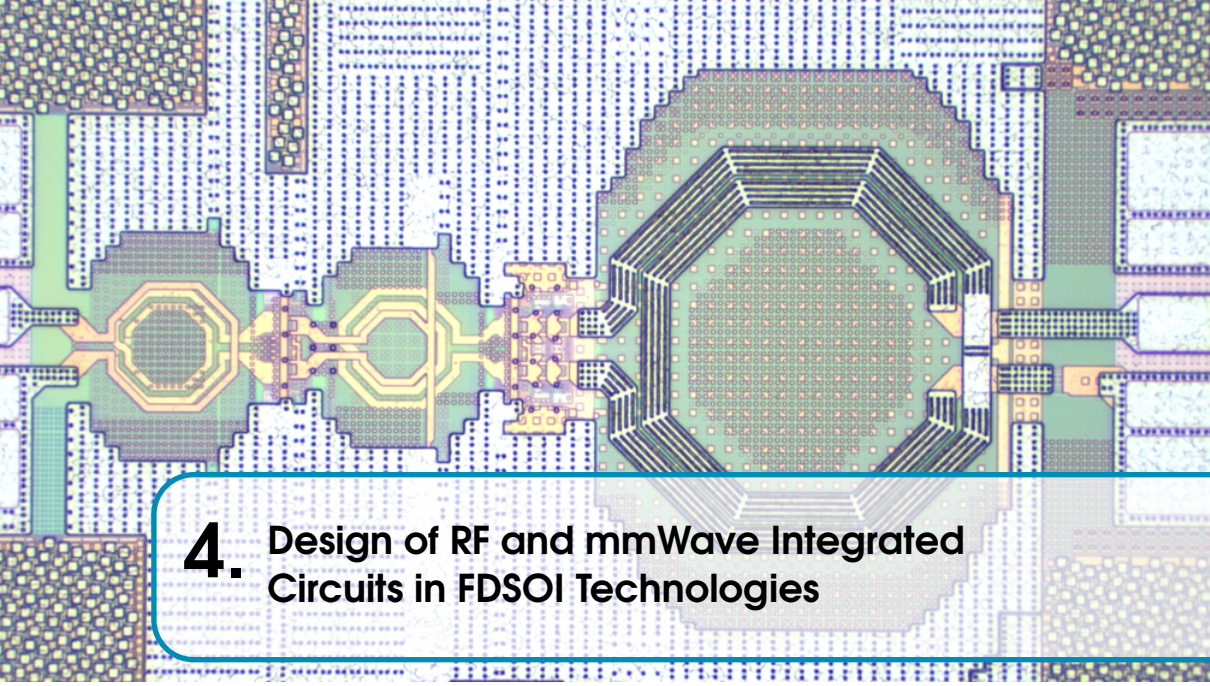
Subsequently, the double-BOX substrate is proposed as a solution for the next generation of FDSOI technology. Proof of concept and TCAD simulations demonstrate that traps in the polysilicon layer can compensate for charges at the BOX2-bulk interface when the latter is thinner than 20 nm. The RF performance of the double-BOX substrate is comparable to the trap-rich substrate in terms of effective resistivity and harmonics. Further work is needed to integrate this type of substrate into industrial technology.

Additionally, measurements and TCAD simulations show that it is possible to eliminate both substrate and interface losses through deep level compensation. The main idea is to introduce traps throughout the substrate volume, compensating for free carriers created by the PSC. However, these traps do not compensate the charges created by the applied DC bias, explaining the variable linearity behavior of the gold-doped silicon substrate (Au-Si). Since gold atoms are highly diffusive, this approach is unsuitable for CMOS foundries, as it is expected to reduce

carrier mobility within the transistor channel.

The last substrate, known as porous silicon, introduces traps electrochemically throughout the substrate volume, similar to the Au-Si substrate. It exhibits excellent RF performance in terms of linearity (better than eSI) and losses. Several fabrication recipes have been developed in the literature, particularly at UCLouvain. However, no modeling has been proposed. In **Section 3.6**, a preliminary model is proposed based on measurements of other porous silicon substrates with different fabrication methods. This serves as a starting point for modeling porous silicon.

Today (2025), the two commercially available FDSOI technologies are 28FDSOI and 22FDX®, both of them are using standard resistivity substrate (10-15 Ω·cm). In **Chapter 4**, for the first time, circuit designs will be integrated with high-resistivity substrates, including FE and PN implants. This opportunity allows us to measure the effect of the substrate at the circuit level. Moreover, it will enable us to observe how circuit figures of merit (FoM) depend on substrate variations.



4. Design of RF and mmWave Integrated Circuits in FDSOI Technologies

So far in this work, a comprehensive characterization of CPW transmission lines on various substrate solutions has been carried out. In this chapter, the design of the individual circuits that make up the complete RF front-end module is presented. Two advanced FDSOI technologies are employed: 28FDSOI from STMicroelectronics and 22FDX® from GlobalFoundries.

As depicted in **Figure 4.1** the RF mixers are designed on a standard silicon substrate with a resistivity of approximately 10 Ω·cm, while the PA is implemented on both standard and high-resistivity substrates (1900 Ω·cm). The RF switches are designed on multiple substrate configurations, as detailed in **Section 3.2** and **Section 3.3**. These configurations include the standard substrate, high-resistivity substrate without passivation, high-resistivity substrate with field-effect passivation, and high-resistivity substrate with PN junction passivation. Each of these substrate choices has been investigated to assess its impact on key performance metrics such as insertion loss, linearity, and power handling capability in RF switch designs.

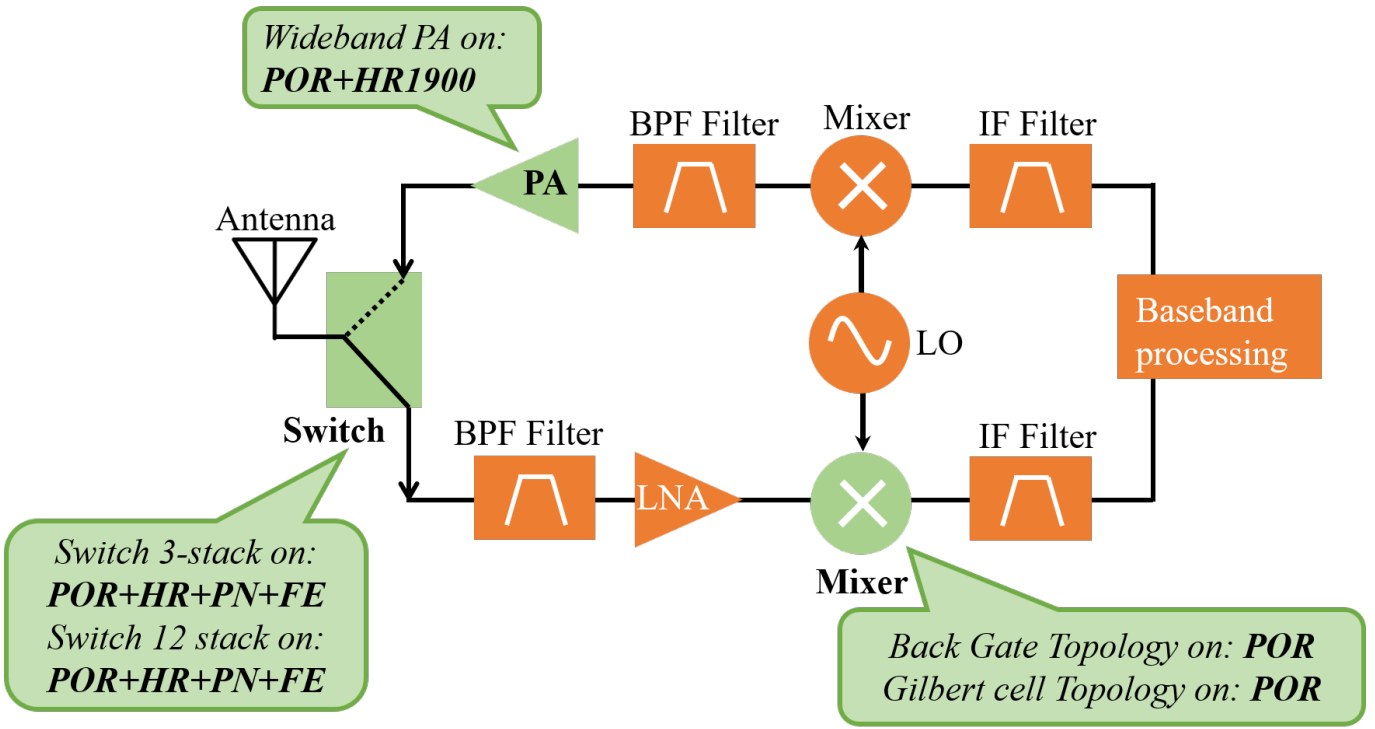


Figure 4.1: Block diagram of an RFFEM showcasing key components such as the PA, switches, and mixers, along with the various substrates on which they are designed, as will be explored in this thesis.

4.1 DC-6 GHz SPDT Switches with 43 dBm Handling in 28FDSOI

Two types of DC-6 GHz single-pole double-throw (SPDT) switches were designed and fabricated using ST's 28FDSOI technology. The first design utilizes stacks of three FETs, targeting a power handling capacity of 30 dBm, while the second design incorporates stacks of twelve FETs, aiming for 42 dBm. Both designs are significantly affected by the substrate. When implemented on surface-passivated high-resistivity substrates, the designs show notable improvements in insertion loss compared to the same devices on standard resistivity substrates. Specifically, the three-stack design achieves a 0.6 dB improvement at 5 GHz. For the twelve-stack design, the active area of the transistors is approximately 30 times larger than that of the three-stack design, resulting in a much greater substrate impact and an insertion loss improvement of 2.5 dB at 5 GHz.

4.1.1 Stacked Series-Shunt Topology Design

The mainstream single ended[1] series-shunt topology is used because of its simplicity and can cover low frequencies with less chip area [127] as depicted in Figure 4.2.

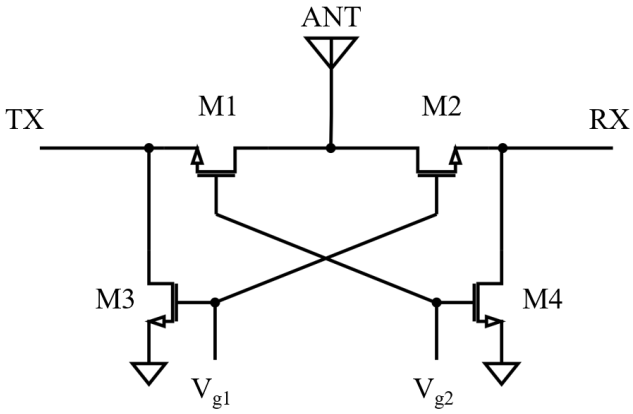


Figure 4.2: Schematic of series/shunt type single-ended T/R switch.

[1]It has been demonstrated in [125, 126] that a differential SPDT switch topology, which is mirrored from the single-ended series SPDT shown in Figure 4.2, can achieve 3 dB higher power handling compared to the single-ended version.

Series transistors M1 and M2 are complementary and perform switch functions for TX and RX as follow: When M1 and M4 are ON, the signal flows from TX to antenna through M1, while the undesired signal RX is grounded through. Conversely, when M2 and M3 are ON, the signal flows from RX to antenna through M2, and the undesired signal is grounded via M3. V_{g1} and V_{g2} are the DC bias points controlling the transistors gate. Compared to the series topology, the series-shunt topology offers better isolation but results in higher insertion loss [128].

The design of the 3-stack switch to target 30 dBm power handling uses transistors known as GO2 (EGV-LVT-N-FET) and implement a thick gate oxide recommended by the foundry for RF switches. Gate lengths of 100 nm and finger width of 2.5 µm are chosen (225 fingers for the series arm). Each transistor can either be biased in an ON state using front- and back-gate voltages of Vg1=1.8 V and Vbg1= 3 V, or to an OFF state using Vg1=-1.8 V and Vbg1=0 V (see Table 4.1). In order to force the RF signal to flow from source to drain and control the transistors, the gate and back-gate nodes of all transistors are biased through R_g and R_{bg} resistors where R_g=R_{bg} = 10 kΩ.

Moreover, a 10 kΩ drain source resistor R_{sd} is connected to each FET in both the series and shunt branches, this is done in order to ensure that the voltage across each FET in OFF state is evenly distributed as shown in [129].

Table 4.1: ON and OFF states considered for the 3- and 12- stack switches and their corresponding voltages.

	ON state	OFF state
Vg1 [V]	1.8	-1.8
Vbg1 [V]	3	0
Vg2 [V]	-1.8	1.8
Vbg2 [V]	0	3

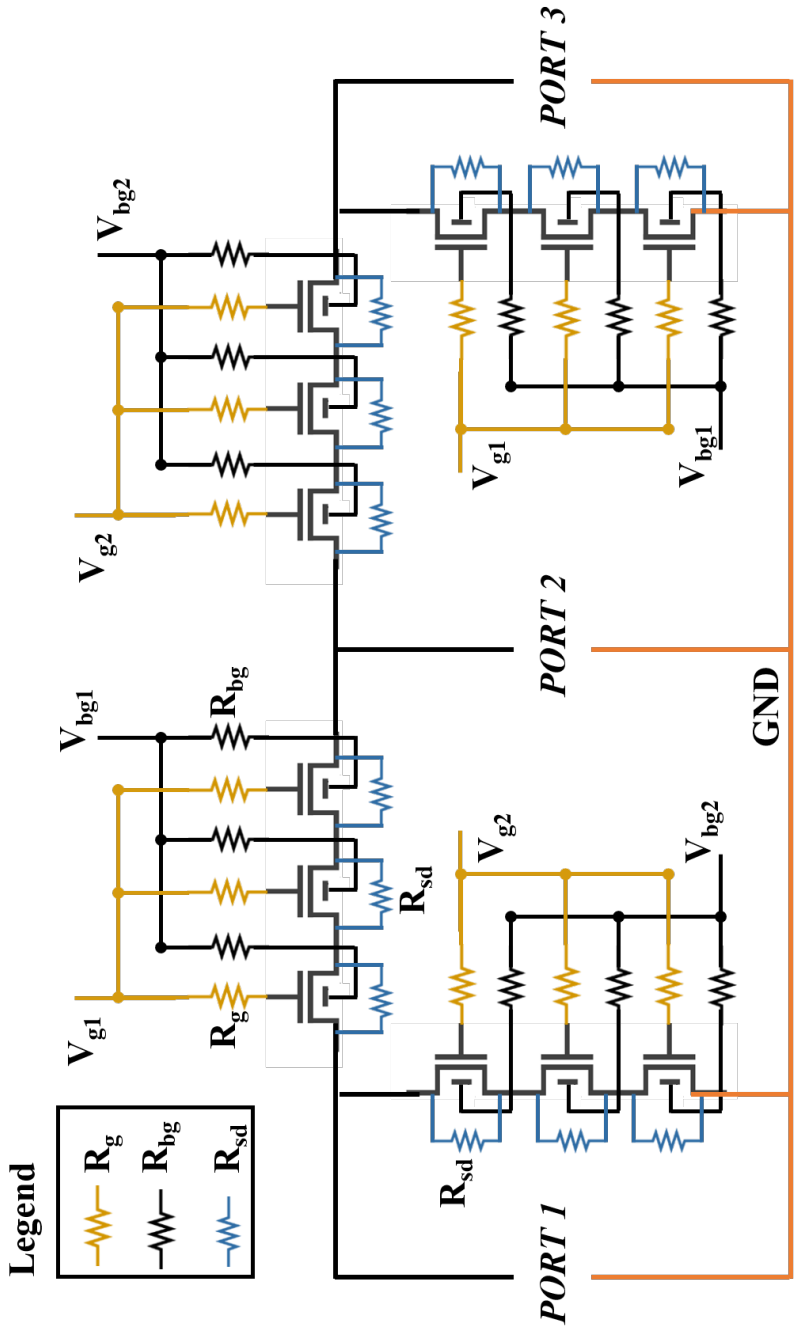


Figure 4.3: Schematic of the designed 3-stack switch in 28FDSOI technology.

4.1.2 12- and 3-stack SPDTs with same Ron×Coff

For sub-6 GHz applications, which require high power handling, a 12-stack switch is presented. Both switches (3-stack and 12-stack) are **geometrically** designed to achieve the same Ron×Coff metric, ensuring comparable performance in terms of the trade-off between on-resistance and off-capacitance. The 12-stack design is derived directly from the 3-stack configuration, as illustrated in **Figure 4.4**.

In **Figure 4.4(a)**, the 3-stack switch is a conventional SPDT having the PORT2 serve as pole while PORTS 1 and 3 are the throws. The switch has 3 series FETs and 3 shunt FETs. Considering the stacked series transistors in the ON state, depicted in a red circle of **Figure 4.4(b)**, the total branch resistance (Ron) is 3A, where A is the ON-series resistance of a single FET. In order to build the 12-stack series branch with the same total Ron (and hence similar insertion losses as the 3-stack switch if we neglect the losses in the metallic interconnections), its FETs are designed to have an ON-series resistance of A/4 (see **Figure 4.4(c)**). This is achieved by using 4 parallel FETs having the same geometry as those used in the 3-stack switch (see **Figure 4.4(d)**).

The dimensions of each FET for the two switches are listed in **Table 4.2**.

Table 4.2: Transistors Dimensions in the Branch of the Two Designed RF Switches.

	3-stack	12-stack
N	3	12
Wser [µm]	562.5	2250
Wsh [µm]	62.5	250

Due to these design choices, the 3-stack and 12-stack switches are expected to yield similar small-signal performances (S-parameters) if substrate parasitics are negligible. In terms of large-signal performance, the 3-stack design targets above 30 dBm of power handling, while the 12-stack targets close to 40 dBm.

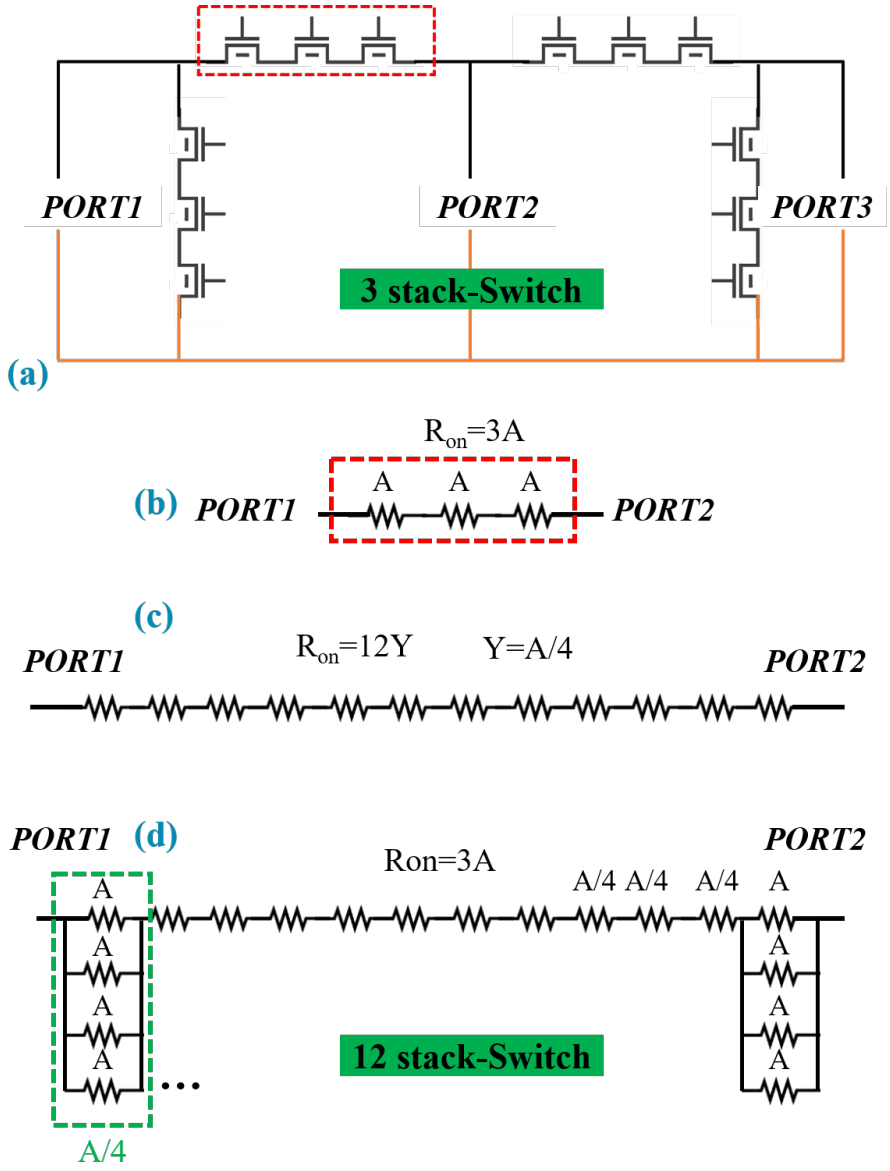


Figure 4.4: Description of the 12-stack switch series branch design starting from a 3-stack switch.

4.1.3 Implementation of the Passivation Techniques for RF Switches

Redacted Confidential Content

4.1.4 Small Signal Measurements

Small-signal S-parameter measurements were performed using an Agilent 4-port Performance Network Analyzer (PNA)-X, three ground signal ground (GSG) infinity probes with 100 µm pitch and 4-point DC probe as depicted in Figure 4.5. The switches were built on three different substrate types termed as:

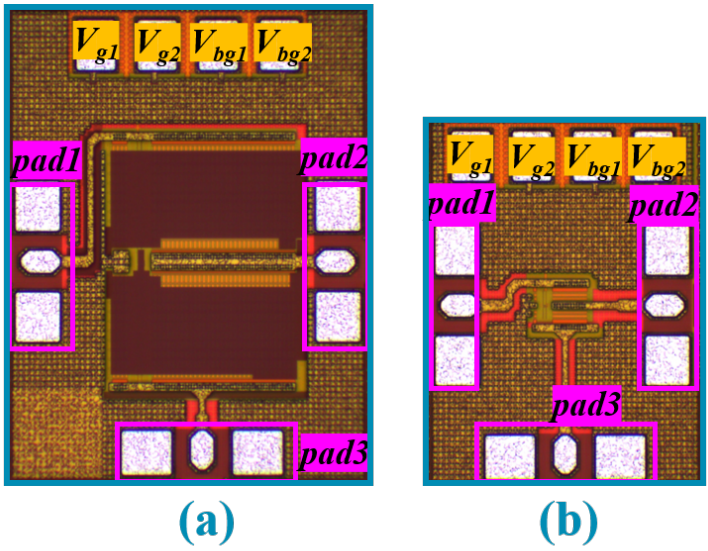


Figure 4.5: Photograph of the designed RF switches (a): 12- and (b): 3 -stack. The active area of the 12-stack is 0.152 mm², for the 3-stack is around: 0.005 mm².

standard substrate (bulk resistivity at 10 Ω·cm), high resistivity (HR) substrate (bulk resistivity above 1 kΩ·cm) without passivation and HR substrate with FE passivation and PN junction passivation. Each circuit on every substrate was measured three times to reduce measurement errors and remove uncertainties.

4.1.5 Substrate Effect on the Designed 3-Stack Switch

Figure 4.6 shows the S_{21} (left) and S_{23}/S_{21} (right) for the 3-stack switch designed on different substrates. The 3-stack switch on standard substrate demonstrates 1.22 dB insertion loss at 5 GHz. The same circuit atop of HR substrate without passivation shows 0.68 dB insertion loss at 5 GHz. However, even if the HR substrate reduces substrate losses, the PSC remains around the tran-

sistors. This is why using the HR substrate with the FE passivation technique further reducing losses by 0.07 dB at 5 GHz, while maintaining high isolation between all the ports (i.e., below 20 dB). The PN lines are not affecting the substrate probably, the number of depletion regions are not enough to increase the impedance in such a small area.

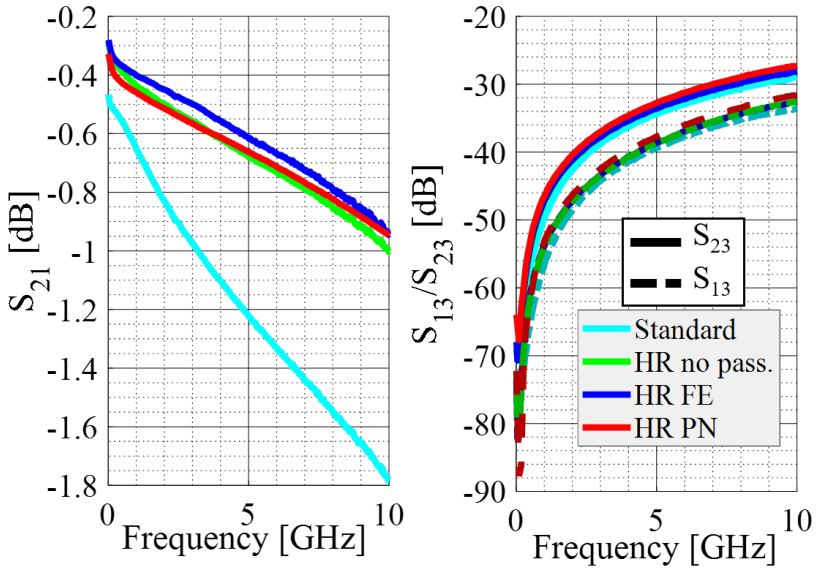


Figure 4.6: Measured S-parameters for the 3-stack switch built on top on standard, HR substrate without passivation, HR with FE passivation, and HR with PN juntions.

4.1.6 Substrate Effect on the Designed 12-Stack Switch

Figure 4.7 shows the S_{21} (left) and S_{23}/S_{21} (right) for the 12-stack switch designed on the previously described substrates. The 12-stack switch on the standard resistivity substrate shows around 3.5 dB insertion loss at 5 GHz. Changing from standard to HR without passivation improves the insertion loss to 1.36 dB at 5 GHz. After that the PN lines improves with 0.2 dB, since the switch is larger, the switch senses more the depletion regions created by P and N regions around the FETs. Using the FE passivation technique, the 12-stack switch insertion loss are 0.91 dB at 5 GHz. The isolation between the non-connected ports remains lower than 20 dB for all the described substrates.

The insertion loss of the switch across different substrates shows a strong correlation with the extracted effective resistivity, as reported in **Section 3.2** and **Section 3.3**. The POR demonstrates the highest losses because of 10 Ω·cm effective resistivity, then the HR is better with 30 Ω·cm, after that the PN lines further improve performance with 500 Ω·cm. The best performance is achieved with the FE passivation, which has an effective resistivity of 1 kΩ·cm.

The substrate effect is more pronounced in the 12-stack compared to the 3-stack, and this effect is caused by the much larger surface occupied by the FETs of the 12-stack switch. Due to its higher power handling, it should be noted that the 12-stack switch is a more appropriate circuit for mobile communications.

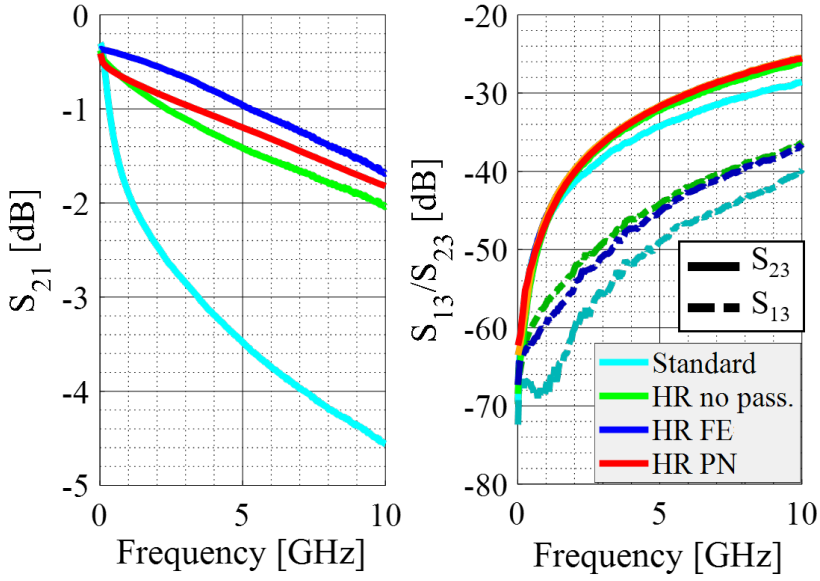


Figure 4.7: Measured S-parameters for the 12-stack switch built on top on standard, HR substrate without passivation, HR with FE passivation, and HR with PN juntions.

4.1.7 12- and 3-Stack Comparison

Figure 4.8 shows the insertion loss comparison of the 3- and 12- stack switches on each substrate. It is shown that the gap between the two switches gradually

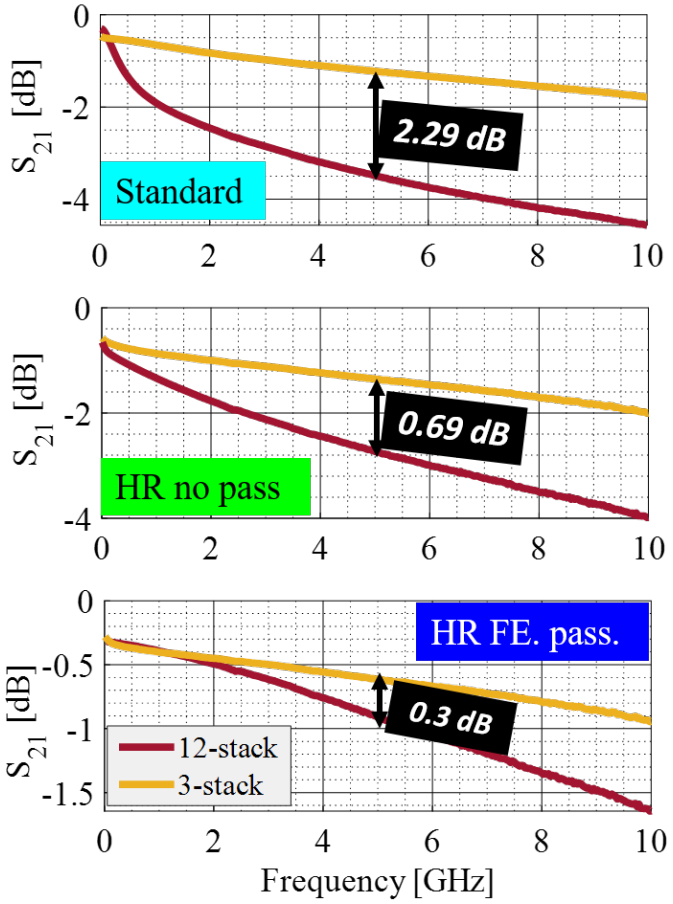


Figure 4.8: Comparison of the S_{21} between 3- and 12-stack switches on **(a)**: standard substrate, **(b)**: HR substrate without passivation and **(a)**: HR with FE passivation.

decreases as the interface is well passivated going from a gap of 2.29 dB for standard substrate, to 0.69 dB for HR without passivation and then finally to a gap of only 0.3 dB for the HR with advanced passivation. Theoretically, the 3-stack and 12-stack switches are expected to have very similar performance if there are no substrate parasitics or associated losses at all. This is achieved at 2 GHz but not at 5 GHz, where a (modest) gap of 0.3 dB is present.

For any substrate, the FETs in 12-stack switch will always be expected to suffer from higher substrate-parasitics than those in the 3-stack design, since the area occupied by the FETs in the 12-stack is more than 30 times larger than that occupied by the FETs in the 3-stack.

The gap in the S-parameter results between the two designs could theoretically be reduced to zero if substrate parasitics could be totally removed. The fact that the substrate-parasitics' influence reduces down to 0.3 dB at 5 GHz when comparing the two designs highlights that a high effective resistivity is well achieved for the effective substrate material around the FETs of the fabricated switches.

4.1.8 Substrate Modeling for FDSOI

The current FDSOI process is manufactured on silicon wafers with standard resistivity (approximately 10 Ω·cm), which are known to cause significant losses, non-linearity, and complicated substrate coupling modeling. Enhancements to the RF quality of the substrates used in FDSOI technology are viewed as an appealing opportunity for short-term technological advancements. In this subsection, the simplest model will be introduced to effectively represent the substrate.

A model is proposed to ensure coherence between the measurements and simulations. Furthermore, it is crucial to highlight that the effective resistivity varies depending on the selected substrate. This variation can significantly impact the overall performance and behavior of the RF circuits. Therefore, understanding and accurately modeling the substrate's properties are essential for predicting and optimizing the performance of high-frequency electronic devices. This model aims to provide a more comprehensive understanding of how different substrates influence effective resistivity and, consequently, the performance of the RF system.

Figure 4.9 presents the 28FDSOI transistor cross-section used in the design of the described switches. Where the buried oxide BOX is modelled by C_{ox}, the depletion region between the back-gate and the silicon substrate is modeled by C_{dep}. The silicon bulk substrate is modeled by the two elements R_{Si} and C_{Si}. In the schematic, Node Y is located below the N-well of the back-gate, representing the connection point within the transistor structure. Node X, on

the other hand, is connected to the ground, which is provided by the GSG probe through the ground tiling[2] of the circuit.

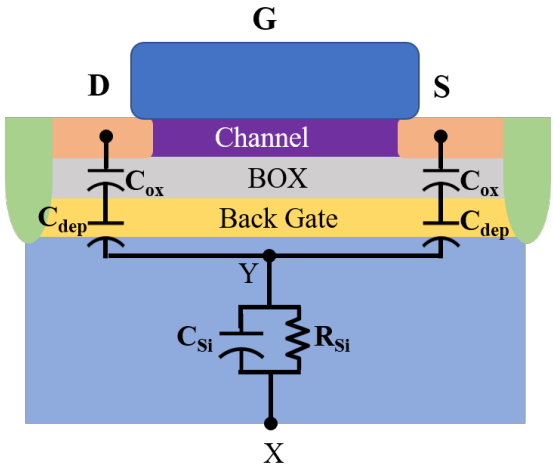


Figure 4.9: Proposed model to evaluate the behavior and effect of the different studied substrates.

The mathematic expression of C_{ox}, the capacitance between the drain and the back-gate is given by:

$$C_{ox} = \frac{\varepsilon_r \varepsilon_0 A}{T_{ox}} \tag{4.1}$$

Where ε_r is the relative permittivity of silicon dioxide that is around 3.9, ε_0 is the permittivity of air estimated at 8.85×10^{-12} F m^{-1}, A is the area of the source or drain region estimated at 0.12×2.5 µm² and T_{ox} is the buried oxide thickness given by the technology that is around 25 nm.

The mathematic expression of C_{dep}, the capacitance between the highly doped back-gate and the doped silicon bulk is given by:

[2]Ground tiling refers to the metal structures that serve as the ground plane in the layout. However, rather than being a solid, continuous sheet of metal, the ground plane is typically represented by a mesh or grid-like structure with small holes or gaps. This mesh ensures proper grounding while adhering to all DRC, which are essential for ensuring the manufacturability and reliability of the circuit.

$$C_{dep} = \frac{\varepsilon_r \varepsilon_0 A}{T_{dep}} \tag{4.2}$$

Where T_{dep} is the thickness of the depletion region and is given by the equation:

$$T_{dep} = \sqrt{\frac{2\varepsilon_r \varepsilon_0 V_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{4.3}$$

Where q is the elementary charge that is equal to 1.6×10^{-19} C, N_A and N_D are the number of acceptor and donor atoms, respectively. V_{bi} is the built in voltage and is given by the following formula:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A \times N_D}{n_i^2}\right) \tag{4.4}$$

The value of V_{bi} is approximately around 0.7 V for a PN junction as demonstrated in [130]. T_{dep} is estimated around 1 µm for an assumed N_A $=10^{15}$ cm^{-3} and N_D=10^{18} cm^{-3} (assumed values)[3].

The objective of this model is to determine the values of R_{Si} and C_{Si}. Given that C_{Si} remains constant—its value being directly proportional to the permittivity of the silicon substrate—the primary focus is on accurately determining the varying values of R_{Si}. Since R_{Si} is directly related to the substrate's resistivity, our task is to identify the specific resistivity values that best match the experimental measurements. This approach involves fitting R_{Si} to observed data, enabling a more accurate representation of the substrate's electrical properties within the model.

[3]The exact doping levels of the back-gate in this technology, particularly for the GO2 transistor, have not been disclosed, as these values are considered confidential. As a result, precise information on the doping concentrations are not available for direct analysis. Due to this confidentiality, an estimation has been provided, based on the general knowledge of similar technologies and typical doping levels that are commonly employed in such transistors. This estimation is used to guide the modeling and analysis efforts, though it is acknowledged that this approach introduces some uncertainty. The use of estimated values allows for continued progress in understanding the behavior of the GO2 transistor within the constraints of the available data.

The values of C_{dep} and C_{ox} are utilized in Cadence software, as illustrated in Figure 4.9. These capacitances are connected in series, which means that the overall capacitance is predominantly influenced by C_{dep}, given that the depletion layer thickness (T_{dep}) is much greater than the oxide layer thickness (T_{ox}). As a result, C_{dep} plays a more significant role in determining the equivalent capacitance (C_{eq})[4].

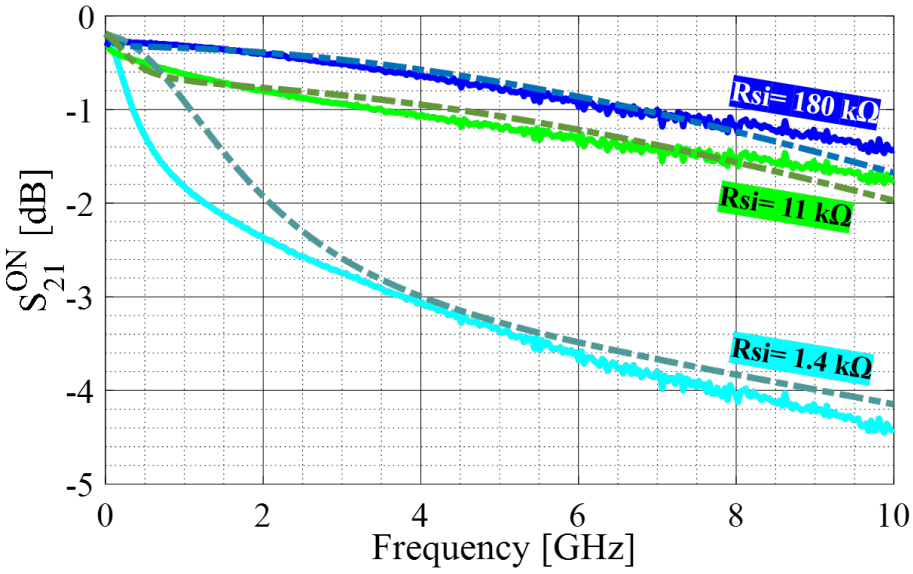


Figure 4.10: Measurements and simulations correlation of the insertion loss of the 12-stack switch built atop of the POR, HR and FE substrates. Measurements are in solid line while the simulations using the described model are in dashed.

By setting the value of C_{Si} to 5 fF, it becomes possible to align the simulation results with experimental measurements, as shown in Figure 4.10. When R_{Si} is set to 180 kΩ, the substrate model closely matches the characteristics of the FE substrate. Subsequently, with R_{Si} set to 11 kΩ, the high-resistivity (HR) substrate with parasitic surface conduction (PSC) is simulated. For the

[4]Where C_{eq} is C_{dep} in series with C_{ox} given by the equation:

$$C_{eq} = \frac{C_{dep} \times C_{ox}}{C_{dep} + C_{ox}}$$

When C_{ox} is much larger than C_{dep}, $C_{eq} \approx C_{dep}$.

POR substrate, a value of R_{Si} equal to 1.4 kΩ is used for modeling. However, a discrepancy is observed at low frequencies for the POR substrate, which may be attributed to the potential mis-estimation of C_{ox} and C_{dep}. These capacitances are critical in accurately representing the substrate's behavior, and any inaccuracies in their values could lead to a misalignment between the simulated and actual performance, particularly in the low-frequency range.

So far, using the modeling approach described above, the substrate has been represented by simple R_{Si} and C_{Si} elements, applied uniformly across the entire substrate. In this model, the substrate is considered homogeneous, which aligns with the concept of effective resistivity. To determine the resistivity[5], the value is calculated using the equation **Equation 4.5**:

$$R_{Si} \times C_{Si} = \rho_{Si} \times \varepsilon_{Si} \tag{4.5}$$

ρ_{Si} based on switch measurements in **Equation 4.5** will be named $\rho_{eff,switch}$, while the effective resistivity measured using CPW lines in **Section 3.2** and **Section 3.3** will be named $\rho_{eff,CPW}$.

$\rho_{eff,switch}$ of the FE substrate has been calculated to be 924.5 Ω·cm, while the $\rho_{eff,switch}$ for the HR substrate without passivation is determined to be 56 Ω·cm. For the POR substrate, the calculated $\rho_{eff,switch}$ is 7 Ω·cm. These calculated values closely correspond to the $\rho_{eff,CPW}$ measurements reported in **Section 3.2** and **Section 3.3** as shown in **Table 4.3**.

Table 4.3: Comparison between the measured effective resistivity on the CPW line, and effective resistivity sensed by the designed switch.

	Measured $\rho_{eff,CPW}$ $[\Omega \cdot cm]$	Measured $\rho_{eff,switch}$ $[\Omega \cdot cm]$
POR	10	7
HR	30	56
HR-FE	1 k	925

[5] C_{Si} is set to 5 fF, ε_{Si} is set to 11.8 and R_{Si} is 1.4 kΩ for POR, 11 kΩ for HR and 180 kΩ for FE substrate.

The close agreement between the calculated and measured values validates the accuracy of the modeling approach, confirming that the simplified model effectively takes into account the resistive characteristics of the different substrates.

4.1.9 Measurements of Power Handling in RF Switches

Redacted Confidential Content

4.1.10 Benchmarking

In the context of RF switch design on different substrates, the table **Table 4.4** offers a comprehensive benchmarking of various RF switches operating in the DC-6 GHz frequency range, highlighting key performance metrics such as P1dB, insertion loss, isolation, and chip area. The comparison spans a range of technologies, topologies, and design approaches from 2003 to 2024, providing a broad perspective on the evolution of RF switch performance over time.

The P1dB of 43 dBm achieved in this work compares favorably with values reported in previous designs, which range from 31 dBm to 40 dBm. For example, the switch designed using 130 nm SOI technology reported by **[131]** has a P1dB of 39 dBm, which, while respectable, still falls short of the performance achieved in this work. The 43 dBm P1dB indicates that the 12-stack switch can handle significantly higher power levels before entering compression, making it particularly well-suited for high-power RF applications where maintaining linearity at high power is crucial.

In terms of insertion loss, the 3- stack switch achieves a value of 0.6 dB, which is competitive with the other designs in the table, especially given the higher frequency range of operation. For instance, the 130 nm GaN RF-SOI switch reported in **[132]** has an insertion loss of 0.6 dB, which matches the performance in this work but does so at the expense of using a different material system. Additionally, the isolation achieved in this work is 30 dB, which is on par with other high-performance designs. Good isolation is critical for reducing interference and crosstalk, ensuring that signals are effectively blocked when the switch is in the OFF state. This level of isolation, combined with low insertion loss, underscores the overall efficiency and effectiveness of the 3-stack switch design.

The switch presented in this work utilizes a 28FDSOI process on HR for the first time, which represents a significant advancement in semiconductor technology compared to many of the earlier works listed in the **Table 4.4**. For instance, several earlier designs are based on 250 nm and 180 nm SOI technologies (e.g., references **[21, 133]**), which inherently suffer from larger parasitic capacitances and less precise control over the channel. The transition to a 28 nm FDSOI node provides this work with enhanced insertion loss, isolation, linearity and power handling of the switches.

Table 4.4: State of the art comparison with DC-6 GHz RF Switches.

Work	Technology	Type	Topology	Stacked [FETs]	Freq [GHz]	IL [dB]	Iso [dB]	Area [mm^2]	P1dB [dBm]	Year
[21]	250 nm SOI	SPDT	Series-Shunt	1	5	1	46	NA	12	2003
[133]	180 nm SOI	SPDT	Dynamic bias	20	5	0.75	39	0.012	33	2007
[134]	130 nm SOI	SPDT	Series-Shunt	10	DC-6	0.8	10	NA	35	2017
[135]	180 nm SOI	SPDT	Negative bias	NA	DC-6	0.7	20	0.58	39.5	2022
[136]	130 nm SOI	SP6T	Series-Shunt	NA	DC-3.5	0.95	20	1.23	36	2006
[131]	130 nm SOI	SP4T	Series-Shunt	9	DC-3	0.7	20	0.49	39	2020
[137][1]	RF-CMOS	SPDT	NA	NA	DC-9	0.38	28	NA	30#	2021
[132]	130 nm GaN-RFSOI	SPDT	Series	2	DC-6	0.6	13	NA	36	2023
[138]	500 nm GaAs	SPDT	Series-Shunt	1	3-6	0.4	34	0.84	40*	2024
[139]	130 nm SiGe-BiCMOS	SPDT	Series-Shunt	3	DC-6	0.8	NA	NA	31	2022
This work	28 nm FDSOI on HR substrate	SPDT	Series-Shunt	3	DC-6	0.6	30	0.4	32.7	2024
			Series-Shunt	12		1	30	0.54	43	2024

*: fundamental=4 GHz, #: $P_{0.1}$dB, NA: not available,X[1]: Industrial product.

In summary, the RF switches presented in this work demonstrate clear advancements over earlier designs, particularly in terms of power handling (P1dB), insertion loss, and isolation, while also maintaining a compact chip area. The use of advanced 28FDSOI technology, combined with a Series-Shunt topology, 12 stacked FETs and FE passivation solution, positions this switch as a leading solution in the field of RF switches, offering superior performance in key metrics that are critical for high-power and high-frequency applications. This work sets a new benchmark for RF switch performance and showcases the continued evolution and optimization of SOI-based RF technology.

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4.2 24-43 GHz Power Amplifier with 19 dBm Psat in 22FDX®

A high-power switch is typically employed to manage the power output from the power amplifier. The primary role of the power amplifier is to boost the low-power RF signals produced by the transmitter to a level adequate for over-the-air transmission to a receiver. This amplification is vital as it directly impacts the communication range, signal strength, and overall performance of the wireless system. Additionally, the power amplifier must maintain a linear response to prevent signal distortion, which can cause interference with neighboring channels and diminish the quality of the transmitted signal. Ensuring this linearity is crucial for preserving signal integrity, especially in systems using complex modulation schemes, where any distortion can significantly affect data rates and reliability.

As demonstrated in [140], the RF performance of a power amplifier (PA) can be tuned by applying a DC bias to the back-gate of each differential pair of transistors at a specific frequency. Furthermore, it has been shown that the average output power and efficiency can be optimized by adjusting the back-gate bias, with the optimal value depending on (i) the signal bandwidth, (ii) the carrier frequency, and (iii) the target error-vector-magnitude (EVM) value. However, the impact of the substrate on power amplifiers operating at such high frequencies has not been studied. Substrate studies have been conducted on various passive devices and advanced circuits, such as LNAs [141] and VCOs [142, 143] in FDSOI technology, but not on power amplifiers.

The primary objective of this thesis is to evaluate the RF performance of the designed power amplifier on two different substrates: a POR substrate with a resistivity of 10 Ω·cm and high-resistivity substrate with a nominal resistivity of 1.9 kΩ·cm. Additionally, this section aims to address several key questions: Does the substrate influence the RF performance of the PA? If so, to what extent? Are there additional benefits for designers beyond improvements in Pout, Psat, and PAE? These questions will be thoroughly explored and answered in this section.

4.2.1 Power Amplifier Overview

Figure 4.11 illustrates the architecture of a balanced power amplifier operating in the 24-39 GHz frequency range. The design comprises two main stages: the driver stage and the power stage, each separated by interstage matching

networks. The signal first enters through an input matching network, which includes a balun (Balun 1) that balances the input signal before feeding it into the driver stage. The driver stage amplifies the signal, which then passes through another balun (Balun 2) in the interstage matching network, ensuring proper signal transfer to the power stage. The power stage further amplifies the signal, which is then fed through an output matching network containing a third balun (Balun 3) to ensure efficient delivery of the amplified signal to the output.

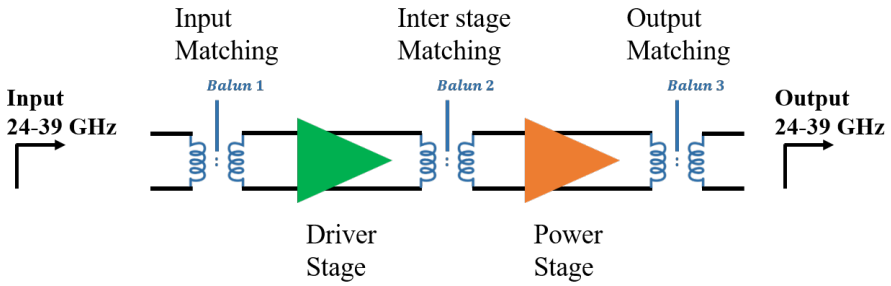


Figure 4.11: Schematic view of the designed power amplifier.

The differential configuration of this power amplifier offers several advantages over single-ended designs. Notably, it improves linearity by canceling even-order harmonics, as outlined by Cripps (2006) [144], and enhances stability through the use of baluns, as discussed by Maas (2003) [145]. Additionally, by combining the outputs of two amplifiers, this design achieves higher overall output power, as described by Grebennikov (2021) [146]. Moreover, differential amplifiers typically exhibit wide bandwidth characteristics, making them highly suitable for broadband applications, as demonstrated by Vendelin (2021) [147]. These advantages make the differential power amplifier a robust choice for high-frequency and broadband RF applications.

The design of the wideband power amplifier (24-43 GHz) is closely based on the one presented in [25] operating in deep class AB, with the primary difference being the reworked driver stage to enhance performance. In the previous design, the driver stage was built with a standard FET configuration, whereas in this work, the driver stage employs a differential architecture with FETs that are twice the width. The main objective of this modification was to improve the linearity of the driver stage, thereby preventing early compression. The only parts designed in this thesis are the input matching, interstage matching,

and driver stage. The power stage and output balun are identical to those in [25].

4.2.2 PA Driver Stage Redesign

In this section, a detailed design of the reoptimized power amplifier will be presented. This will include a comprehensive description of the different parts.

Figure 4.12 shows a detailed schematic of the double stage with an input RF signal frequency at 24-44 GHz. In order to simplify reading of the schematic, the Driver stage is in gray and the power stage is in green while the different matching networks between the different parts are in blue. As said earlier in this part, the power stage and the output matching are the starting material of the design if the PA. They are exactly the same as in [25].

First, let's discuss the driver stage. The FETs M0n and M0p are identical, each with a total width of 80 µm, a gate length of 20 nm, and 80 fingers, with each finger being 1 µm long. These dimensions are expected to allow the driver stage to deliver higher power before reaching compression, compared to the design in [25]. Regarding the neutralization capacitor Cn1, when the drain voltage undergoes a large swing, it generates a feedforward current through Cgd to the gate of M0n or M0p, which weakens the gate voltage and reduces the transistor's overall gain [148]. To address this, Cn1 of 34 fF is placed between the gate and drain of the opposite transistor to compensate for Cgd, enhancing isolation and significantly improving the circuit's stability [149]. For reference, neutralization capacitances are also used in low-noise amplifiers to improve the overall gain, as demonstrated in [150].

The next step in the design process is to create the interstage matching network. To achieve this, a load-pull simulation was performed using Cadence. The primary objective of this simulation is to determine the optimal impedance that should be presented at the output of the driver stage to ensure maximum power transfer. Load-pull simulations generate two key contours on the Smith chart: one representing the optimum power output and the other representing the optimum power added efficiency (PAE). By analyzing these contours, designers can identify the best impedance conditions to balance both power output and efficiency.

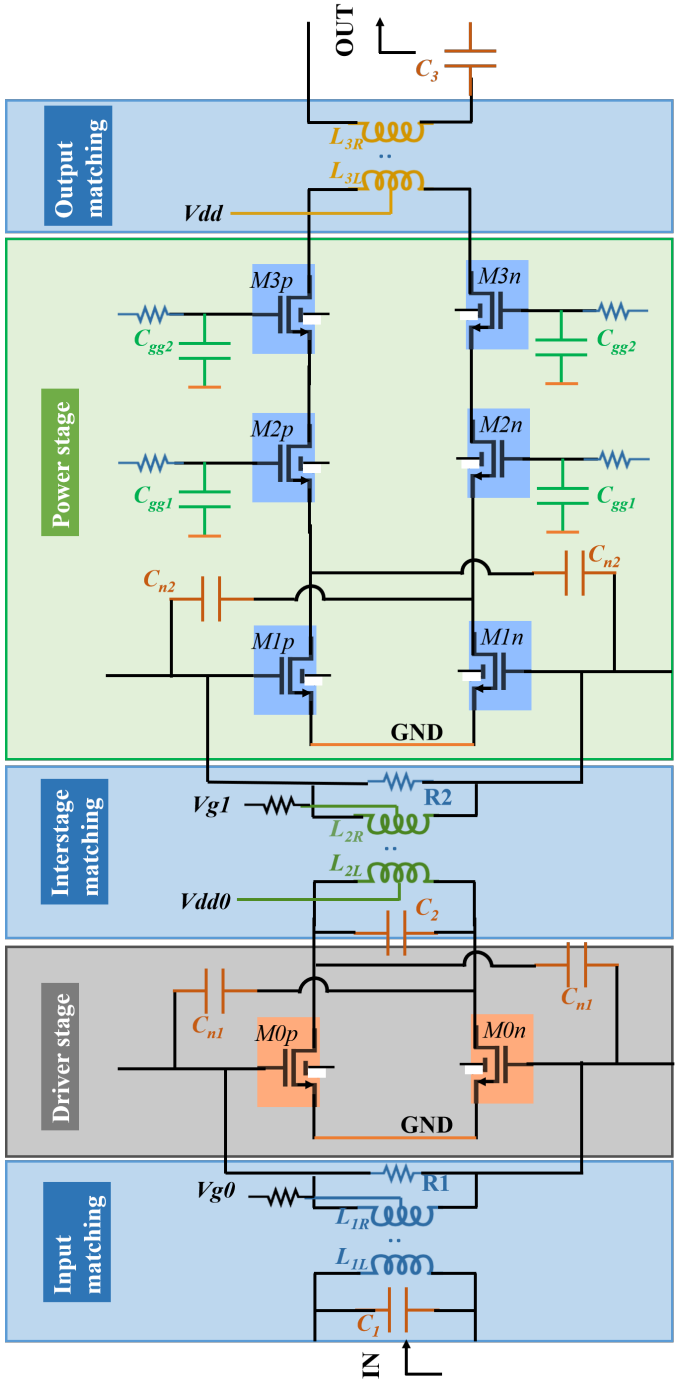


Figure 4.12: Schematic diagram of the designed power amplifier, where the output stage and output balun are exactly the same as [25]. The driver stage is in grey color, power stage in green, and the matching between different parts of the PA are in blue color.

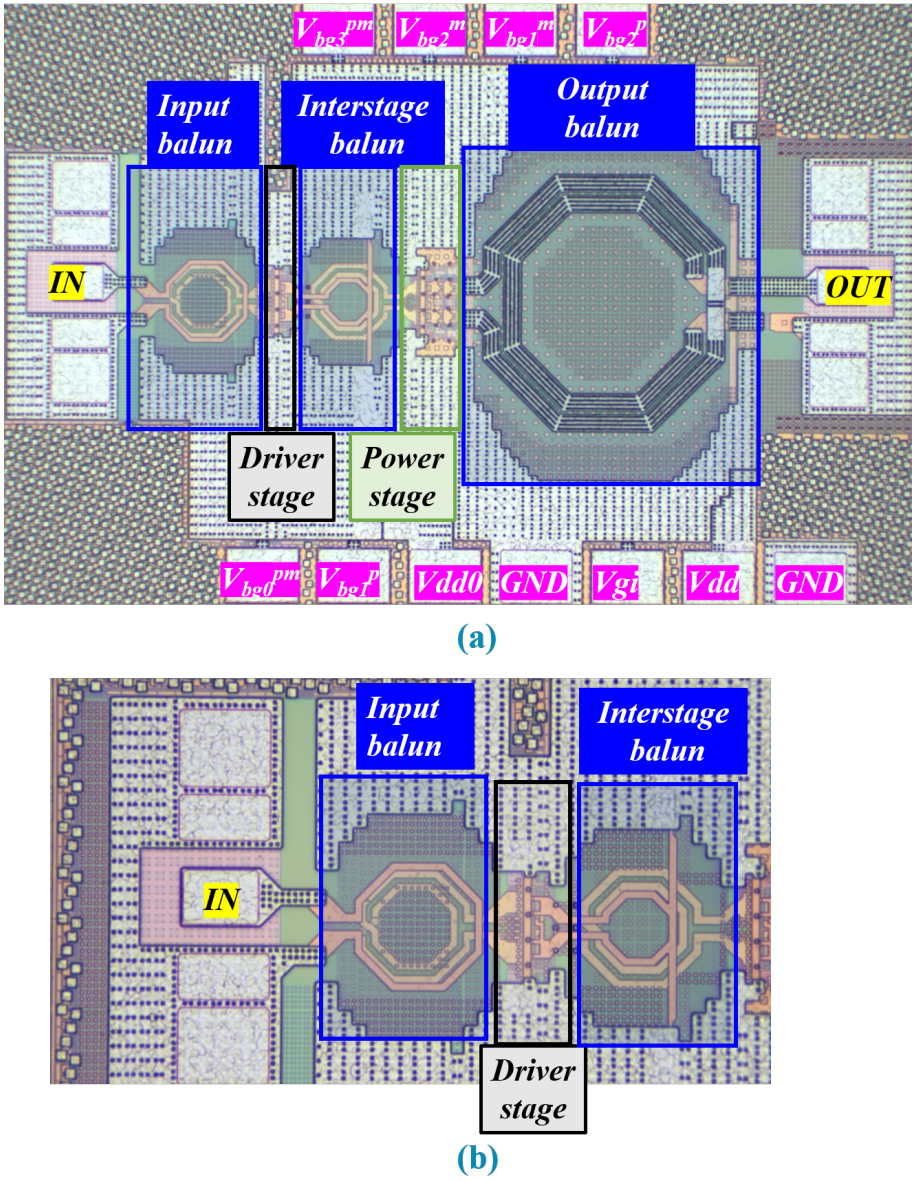


Figure 4.13: Layout views of the fabricated PA: **(a)** Full layout of the PA, highlighting the input, interstage, and output baluns, along with the driver and power stages. The various biasing and supply voltages are also labeled for reference, 520 × 800 µm without pads. **(b)** Layout showing the zoom of input and interstage baluns, along with the driver stage, for a detailed view of components. colour code of is the same as in **Figure 4.12**.

Several simulations were performed at key frequencies of 28, 32, and 39 GHz. In this design, the equivalent output impedance at the driver stage Z_{out} is $R = 34\ \Omega$ in parallel with a capacitance of 72 fF. This impedance needs to be transformed into 80 fF in series with $R = 4.5\ \Omega$ to match the load impedance Z_{load}. The matching network is designed accordingly, incorporating inductances and capacitances to achieve the desired impedance transformation for maximum power transfer (see **Figure 4.14(a)**).

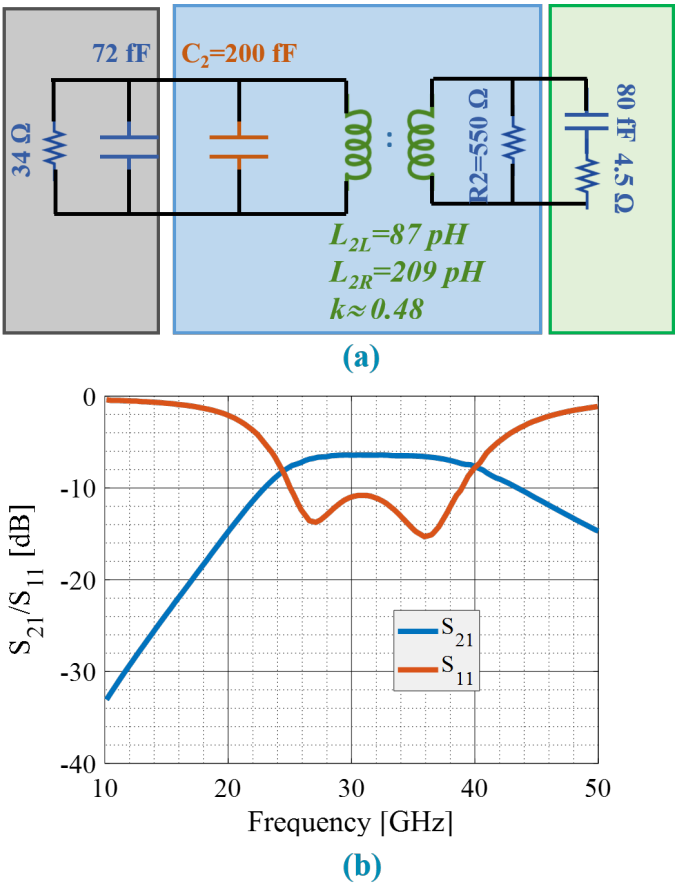


Figure 4.14: Interstage matching with the values implemented in the design in **(a)** and simulations results showing the reflection and transmission parameters of the interstage matching in **(b)**.

Figure 4.14 illustrates the design of the interstage matching network. In **(a)**, the blue section represents the matching network, the grey section corresponds to the driver stage, and the green section indicates the input of the power stage. The matching network was optimized using the ADS optimizer, with the inductors set to values of 87 pH (drawn on QB layer: second metal layer from the top) and 209 pH (drawn on QA layer: third metal layer from the top) for the left and right sides of the balun, respectively. The capacitor C2 was set to 200 fF, and the resistor R2 = 550 Ω.

These component values were validated through simulations using the PDK, as depicted in **Figure 4.14(b)**, where the S-parameters are plotted as a function of frequency. The results confirm that the interstage matching is effective, with the driver stage being well-matched to the input of the power stage over the frequency range of 24-40 GHz, exhibiting approximately 6 dB of insertion loss. The higher losses are primarily due to the R2 resistor. In narrowband matching networks, inductors and capacitors are typically used to create a resonance at a specific frequency, which maximizes power transfer at that frequency. However, this sharp resonance can lead to poor matching outside the resonance frequency, resulting in a narrow bandwidth. By introducing R2 into the network, the resonance is effectively damped. This damping flattens the resonance peak, thereby reducing the network's sensitivity to frequency variations. As a result, the matching network becomes less frequency-dependent and more broadband. However, this also affects the gain and leads to power being dissipated in the resistor. This trade-off was carefully considered during the design process.

The next step involves applying a similar procedure as used for the interstage matching to design the input matching network. The goal here is to match the 50 Ω RF input pad to the input impedance of the driver stage. The input impedance of the driver stage is characterized by a resistance of 6.1 Ω in parallel with a capacitance of 73 fF, whereas the RF input pad is represented by a simple 50 Ω resistance.

Figure 4.15(a) shows the design of the input matching network with the implemented component values. The balun is constructed with a primary inductor of 188 pH on the QB layer, while the secondary inductor, implemented on the QA layer, has a value of 430 pH with a coupling coefficient k=0.59. Below that, in **Figure 4.15(b)**, the S-parameters simulations are presented, demonstrating a decent wideband matching from 23 to 44 GHz. The minimum

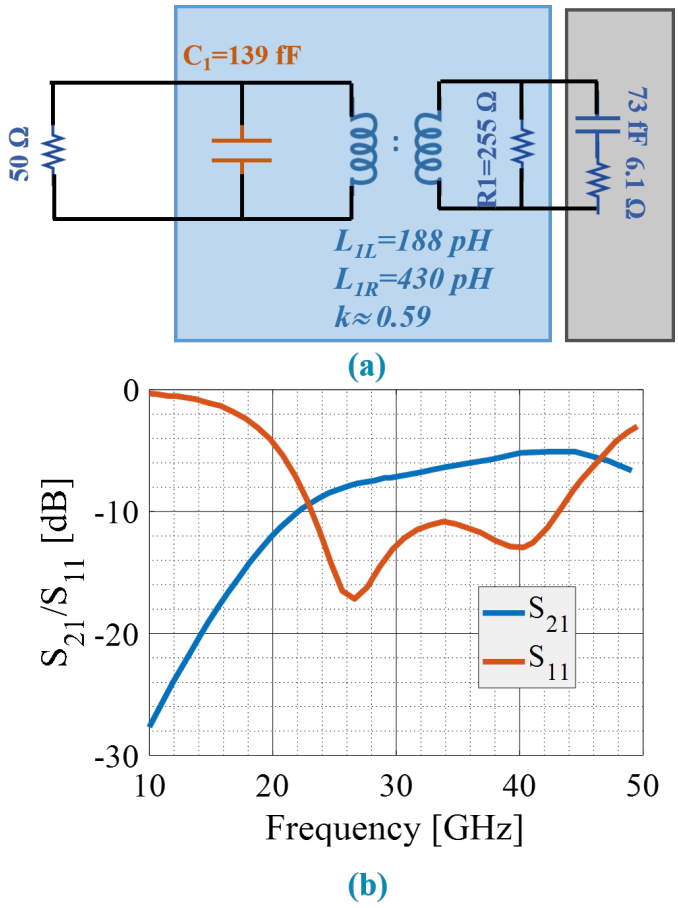


Figure 4.15: Input matching with the values implemented in the design in **(a)** and simulations results showing the reflection and transmission parameters of the input matching in **(b)**.

loss observed is -5.5 dB, occurring around 40-44 GHz. This relatively high loss is primarily due to the presence of the resistor R1, highlighting the trade-off between wideband matching and insertion loss, as discussed earlier.

4.2.3 RF Measurements on Highly Doped Substrate

RF measurements have been conducted on the designed power amplifier (PA) fabricated on a standard substrate. These measurements are crucial for multiple reasons. First, they serve to validate the accuracy of the model provided in the PDK (Process Design Kit), ensuring that the simulation models correspond well to the actual performance of the fabricated device. Additionally, the RF measurements are aimed at evaluating the performance of the power amplifier in terms of key parameters such as matching and gain. Proper impedance matching is critical for maximizing power transfer and minimizing reflections, which can significantly impact the efficiency and overall performance of the power amplifier. Furthermore, specific measurements of the PAE and output power Pout will be performed at selected key frequencies. These measurements are particularly important for assessing the PA's efficiency in converting DC power into RF power.

Gain and Matching

Figure 4.16 shows the measured and simulated input matching S_{11} (and output matching S_{22}) in **(a)** and gain of the power amplifier in **(b)** as a function of frequency. In both figures, the simulations align well with the measured results. However, in **Figure 4.16(a)**, a slight shift is observed around the 24-44 GHz range. Based on the S_{11} values, it can be concluded that the power amplifier is well-matched across the 24-44 GHz frequency range, as a return loss of -10 dB is achieved throughout this range.

The S_{22} values observed in both measurements and simulations are consistently below 0 dB, which indicates good impedance matching at the output of the amplifier. In amplifier design, maintaining S_{22} below 0 dB is crucial because it helps prevent negative resistance at the output, which could lead to instability. A low S_{22} value is therefore desirable for ensuring that the amplifier operates stably across all conditions. This observation is further supported by the measured stability factor K_f (see **Figure 4.17(a)**) which remains above 1 across the entire frequency range, confirming the amplifier's stability.

The gain in **Figure 4.16(b)** shows a value higher than 20 dB in the entire frequency range 24-44 GHz with a maximum gain at 25 and 26.5 GHz of almost 30 dB.

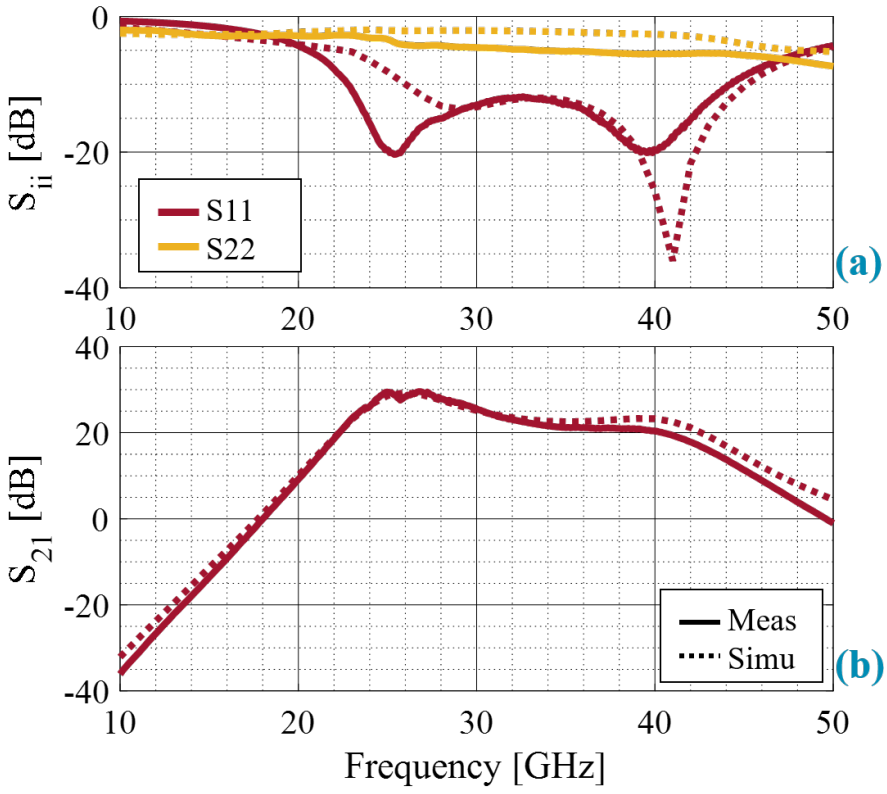


Figure 4.16: Matching between the input pad and the input stage of the PA in **(a)** and the gain of the PA in **(b)**.

Stability of the PA

To ensure that an RF circuit operates correctly, the stability factor must be thoroughly analyzed and checked at each step of the design process. An unstable power amplifier can lead to oscillations and potential damage to the circuit. For an amplifier to be considered stable, two conditions must be met: (i) the Rollett stability factor K_f is lager than 1 and (ii) the magnitude of the determinant Δ should be less than 1 (in small-signal conditions).

The stability factor K_f (Rollett factor) is calculated using the equation from [151] as follow:

$$K_f = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{4.6}$$

Where:

$$\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \tag{4.7}$$

Figure 4.17 shows the measured stability factor K_f in **(a)** and the absolute of determinant Δ in **(b)** as a function of the frequency

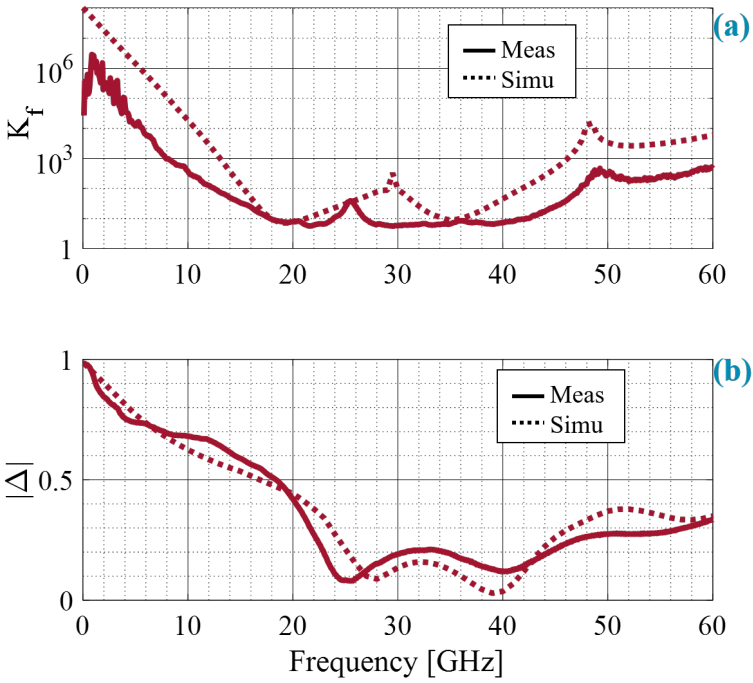


Figure 4.17: Measured and simulated of the stability factor K_f **(a)** and measured and simulated of the determinant $|\Delta|$ in **(b)**.

The simulations presented in **Figure 4.17** closely follow the shape of the measurements, and the results are quite similar. There is a slight shift that could be related to the S_{11} matching, as shown in **Figure 4.16(a)**. Despite this minor discrepancy, the Rollett stability factor remains consistently above 1 across the entire frequency range measured. Additionally, the absolute value of the determinant is maintained below 1. These two conditions confirm that the designed power amplifier is unconditionally stable, ensuring reliable operation without the risk of oscillations.

One key area of improvement for the power amplifier (PA) in this work is its stability. In [25], it was observed that while the PA's determinant Δ was below 1, fulfilling one of the requirements for stability. However, the Rollett stability factor K_f was below 1 in the frequency range of 23 to 29 GHz. This low K_f value indicated that the amplifier was potentially unstable within this frequency band[6]. In this work, efforts were made to address this instability by ensuring that both stability criteria $-\Delta < 1$ and $K_f > 1-$ are met across the entire operating frequency range.

4.2.4 Substrate Impact on IC Design

After confirming that the power amplifier on the POR substrate is stable, operates correctly, and provides measurements that align well with the simulations, we can now proceed to explore how changing the substrate affects the PA's performance. By altering the substrate into the high resitivity substrate with 1900 Ω·cm, we aim to investigate the impact on key parameters such as stability and overall efficiency, and to understand how different substrates might enhance or limit the PA's capabilities.

Substrate Simulation Method

Since the primary focus of this thesis is the effect of the substrate, it is important to detail how the simulations are conducted within the integrated circuit. In conventional design methodologies, the substrate is either shielded or its impact is accounted for in the IC design through electromagnetic (EM) simulations of passive components and interconnects. These simulations typically rely on an EM stack provided in the technology's process design kit (PDK). This EM stack generally models the substrate as a homogeneous layer with fixed permittivity and resistivity values.

However, as discussed in **Chapter 3**, the substrate is not inherently homogeneous. It often consists of regions with varying resistivities, particularly in the

[6]The PA demonstrated in [25] was not unstable under the 50 Ω conditions for which it was initially designed and tested. However, for real-world applications, this alone is not sufficient. In practice, variations in load impedance, often caused by changes in antenna impedance, can occur. Therefore, the PA must be robust enough to handle such variations, maintaining both stability and performance in diverse operating conditions.

case of high-resistivity (HR) substrates. In HR substrates, for example, the PSC effect creates a non-homogeneous environment beneath the buried oxide (BOX) layer. This non-uniformity significantly influences the electrical behavior of the substrate, necessitating more detailed modeling to accurately capture its impact on the IC performance.

To account for the vertical resistivity profile variations, ATLAS Silvaco is employed as it solves semiconductor transport equations using Finite Element Methods. This approach is applied to the three substrates under study to obtain a 2D resistivity profile at all points within the substrate. These simulations take into consideration oxide charges, traps, and other material and interface parameters, allowing for the extraction of precise vertical resistivity profiles for each substrate, as shown in **Figure 4.18(a)**.

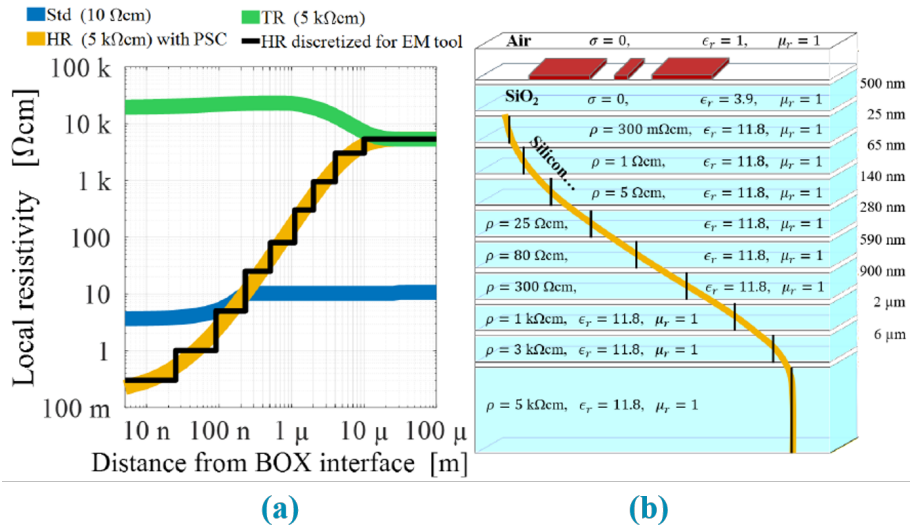


Figure 4.18: Typical vertical resistivity profiles within the semiconductor volume beneath the BOX layer for the three SOI substrates in **(a)** . An example of profile discretization is illustrated for the HR substrate. **(b)** shows an illustration of the material stack definition used in EM solver tools to account for the non-uniformity of a HR substrate affected by the PSC effect. From **[152]**.

However, since TCAD software (like ATLAS Silvaco) is limited to 2D simulations, it is primarily used for structures that are uniform in the third dimension, such as CPW lines. Extending its application to arbitrary structures, such as inductors, becomes significantly more challenging. To address this, an EM simulation tool such as Momentum ADS from Keysight is used for RF design. These tools solve Maxwell's equations to model electromagnetic propagation and are better suited to handle complex structures.

For a more comprehensive simulation approach, it is possible to combine the EM simulations with the resistivity profiles obtained from ATLAS Silvaco. In this combined method, the non-uniform resistivity profiles generated by TCAD simulations are discretized into a finite number of uniform layers for use in the EM simulation. For instance, in the case of the HR substrate, the vertical resistivity profile obtained from ATLAS Silvaco (illustrated by the orange curve in **Figure 4.18(b)**) is discretized into a series of nine uniform silicon layers with varying resistivities (depicted by the black curve). By stacking these nine material layers, the non-uniformity of the HR substrate is approximated, allowing its electrical behavior to be represented more accurately.

This approach is not limited to the HR substrate but is similarly applied to configure the material stacks and simulate the electrical behavior of the Std and TR substrates. By integrating the detailed resistivity profiles from TCAD into the EM simulations, the substrate's non-uniform properties and their impact on device performance can be better captured, enhancing the fidelity of the overall simulation process.

It is important to note that Momentum, a simulation tool from Keysight, is available as a plugin for Cadence Virtuoso, which is the primary IC design platform used by most semiconductor foundries.

PA on High Resistivity Substrate

Figure 4.19(a) presents the maximum PAE at each frequency for the designed PA on both the POR and HR substrates. HR-1900 is a high-resistivity substrate that, despite its classification, exhibits a relatively low effective resistivity and is impacted by PSC. Additionally, simulations were performed on a substrate with characteristics similar to a trap-rich substrate, which has an effective resistivity of approximately 3 kΩ·cm. The simulations align well with the measurements

above 30 GHz, but this is not the case below 30 GHz. This discrepancy is likely due to the driver stage, which is not sufficiently linear, causing it to compress too early and thus limiting the power stage from reaching its full potential. Additional measurements were conducted at Vdd =2.7 V instead of 2.4 V, showing improved performance above 30 GHz. However, below 30 GHz, the results remained unchanged, reinforcing the assumption that the driver stage is not adequately optimized [7]. Aside from the mismatch observed below 30 GHz, the PAE can be improved by approximately 6 % at 35 GHz simply by switching the substrate from POR to HR-1900. The 6 % improvement in PAE results in lower power dissipation as heat (since a greater portion of the DC power is converted into useful RF output power, and less is wasted as heat) from the PA as given by the equation from [153]:

$$P_{Dissipated} = P_{DC} \times (1 - PAE) \tag{4.8}$$

However, when transitioning from the HR-1900 substrate to the HR-3 k substrate, the PAE gain is more modest (slight increase in power dissipation), with only a 1 % improvement.

Figure 4.19(b) illustrates the output power extracted at the point of maximum PAE[8].

At 35 GHz, the power amplifier built on the POR substrate achieves a maximum PAE of 25.5 %. This efficiency translates to an output power of 17.85 dBm at the same frequency. However, when the substrate is switched from POR to a high-resistivity substrate, the PAE significantly improves to 32.4 %. This improvement in efficiency corresponds to an increased output power

[7] One of the primary objectives of this project was to design a power amplifier with high efficiency and stability. We successfully achieved the design of the PA, meeting the required performance criteria. Additionally, the amplifier was made stable across the targeted frequency range, ensuring reliable operation. However, despite these successes, the goal of making the driver stage fully linear was not achieved. The driver stage exhibited early compression, indicating that further optimization is necessary to enhance its linearity and fully realize the potential of the overall amplifier design.

[8] Typically, the measurements we extract are presented as a function of the Pin. For instance, when analyzing the PAE as a function of Pin, we first identify the maximum PAE and note the corresponding Pin value at that point. Once we have this specific Pin value, we refer to the curve of Pout versus Pin. By using the Pin value obtained from the PAE curve, we can then determine the corresponding Pout by locating it on the Pout versus Pin curve. This process allows us to accurately relate the efficiency performance to the actual output power delivered by the amplifier.

of 18.4 dBm at 35 GHz. The change in substrate from POR to HR-1900 not only enhances the efficiency but also boosts the output power. The higher PAE indicates that the amplifier is converting more of the DC input power into RF output power, with less energy lost in the substrate since it is the only variation between the two measured PAs.

Moreover, simulations of the HR-3 k substrate show a very modest improvement in PAE compared to the HR-1900 substrate, with an increase of about 1 % at 35 GHz. This minor enhancement has translated to almost no gain in output power.

The 1 % lower PAE for the HR-1900 substrate compared to the HR-3 k substrate, despite having the same Pout, can be attributed to higher internal losses within the HR-1900 substrate created by the PSC effect. This could be explained as follow:

The PAE equation is defined as:

$$\mathrm{PAE} = \frac{\mathrm{P_{out}} - \mathrm{P_{in}}}{\mathrm{P_{DC}}} \tag{4.9}$$

Where $\mathrm{P_{out}}$ is the RF output delivered to the load, $\mathrm{P_{in}}$ in the RF input power and $\mathrm{P_{DC}}$ is the total DC power consumed by the amplifier.

The total DC power is used to generate the RF output power and some power will be lost within the power amplifier due to parasitics. So one can write that:

$$\mathrm{P_{DC}} = \mathrm{P_{out}} + \mathrm{P_{loss}} \tag{4.10}$$

For the HR-1900 substrate, the losses in the substrate are mainly due the PSC effect as mentioned in **Chapter 3**, the PAE can be written as:

$$\mathrm{P_{DC,HR\text{-}1900}} = \mathrm{P_{out,HR\text{-}1900}} + \mathrm{P_{loss,PSC}} \tag{4.11}$$

For the HR-3k substrate, which is the trap-rich substrate, the PAE can be written as:

$$\mathrm{P_{DC,HR\text{-}3k}} = \mathrm{P_{out,HR\text{-}3k}} + \mathrm{P_{loss,no\text{-}PSC}} \tag{4.12}$$

Since the PA atop both substrates demonstrates almost same output power P_{out} as shown in **Figure 4.19**:

$$P_{out} = P_{out,HR\text{-}1900} = P_{out,HR\text{-}3k} \tag{4.13}$$

Using **Equation 4.13** and **Equation 4.10** in **Equation 4.9**:

$$PAE_{HR\text{-}1900} = \frac{P_{out} - P_{in}}{P_{out} + P_{loss,PSC}} \tag{4.14}$$

$$PAE_{HR\text{-}3k} = \frac{P_{out} - P_{in}}{P_{out} + P_{loss,no\text{-}PSC}} \tag{4.15}$$

The **Equation 4.15** and **Equation 4.14** demonstrate that the PAE differs between the two substrates, despite both amplifiers delivering the same output power. This discrepancy in PAE, with a modest 1 % lower efficiency observed in the HR-1900 substrate, can be attributed to the higher DC power dissipation in this substrate. The increased dissipation is primarily due to the parasitic surface conduction (PSC) effect.

In the HR-1900 substrate, the PSC effect leads to additional conductive paths within the substrate, which increases the overall power loss. These losses reduce the amount of DC power available for effective RF amplification, thereby lowering the PAE. In contrast, the trap-rich (TR) substrate or a very high-resistivity substrate, such as the HR-3k, exhibits fewer such parasitic effects, resulting in lower internal losses and higher efficiency. This explains why, even with almost the same P_{out} the PAE is higher in the HR-3k substrate compared to the HR-1900 substrate.

Below 38 GHz, the benefits of using the HR substrate become even more evident. There is a noticeable improvement in overall output power across the frequency range when compared to the POR substrate. Specifically, by switching to the HR substrate, an approximate gain of 0.5 dB in output power is observed. While this gain might seem modest, it is significant in RF and microwave applications.

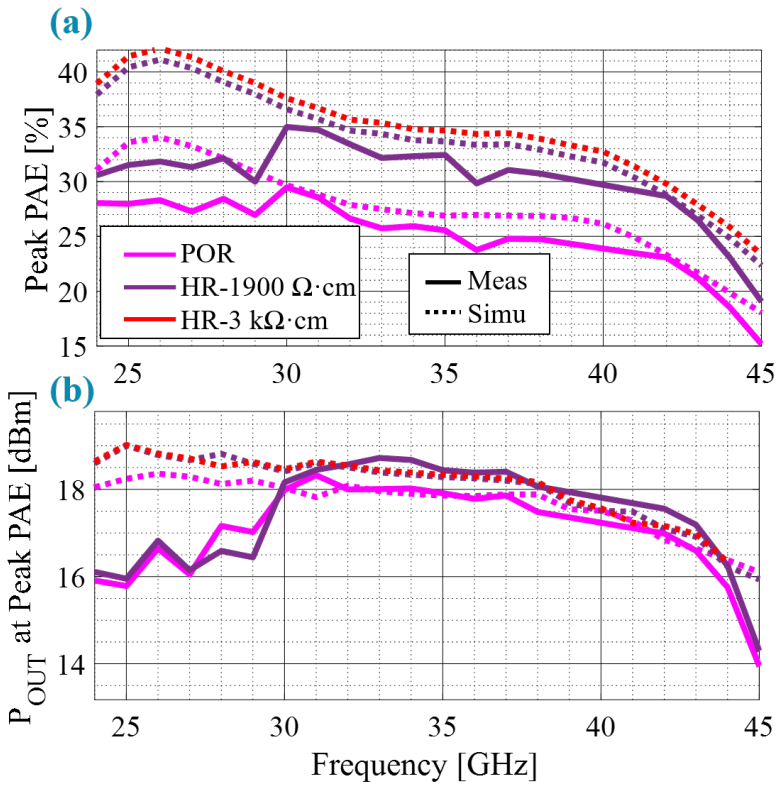


Figure 4.19: Extracted maximum PAE as a function of frequency **(a)** and output power at peak PAE **(b)**.

When a HR substrate is used, it acts as a low-loss substrate, characterized by fewer free carriers. This reduction in free carriers minimizes the energy lost within the substrate, allowing more of the DC power to be converted into RF output power rather than being dissipated as heat or other forms of loss. As a result, the amplifier becomes more efficient, reflected in an improved PAE.

Figure 4.20 illustrates the measured and simulated output power at saturation P_{SAT} for two PAs designed on different substrates: HR-1900 and POR. Additionally, simulations were performed for a PA on the HR-3 k substrate. The P_{SAT} values are plotted against frequency, covering the range from 25 to 45 GHz. It is evident that the simulations align well with the measurements above

30 GHz for both the HR-1900 and POR substrates.

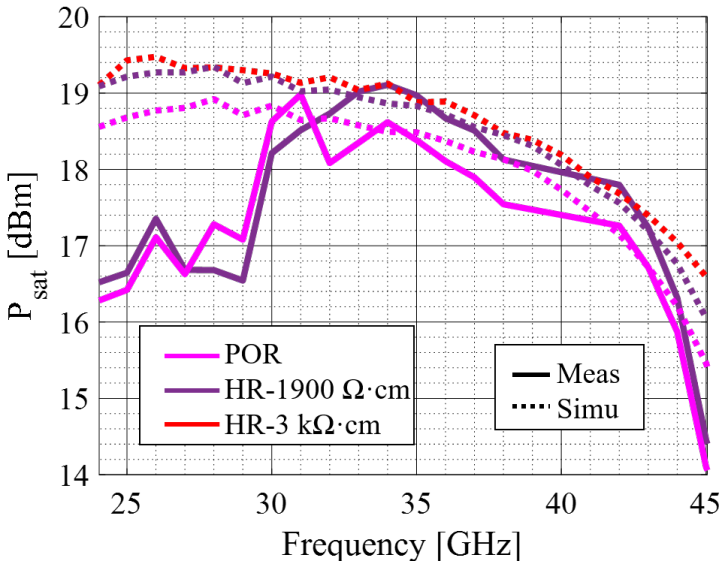


Figure 4.20: Output power of the two manufactured designed PAs in saturation. In addition, the red curve presents the simulation of a virtual PA atop of HR substrate without PSC effect.

The overall trend shows that both substrates reach their peak P_{SAT} values around 34 GHz, with the POR substrate achieving 18.5 dBm and the HR-1900 substrate slightly higher at 19 dBm. When comparing these two substrates, the HR-1900 consistently demonstrates higher P_{SAT} across most of the frequency range. This suggests that the high-resistivity HR-1900 substrate is more effective in supporting higher output power at saturation, likely due to its lower loss characteristics and fewer free carriers in the bulk. These properties reduce energy dissipation within the substrate, leading to more efficient power transfer and, consequently, higher output power. Moreover, the free carriers in the HR-1900 substrate result in reduced parasitic effects compared to the POR substrate. This reduction in parasitic effects further minimizes energy losses, improving the overall performance of the amplifier. As a result, the HR-1900 substrate consistently delivers higher output power across a broad frequency range.

Switching from the HR-1900 substrate to the HR-3 k substrate, however, leads to only a very modest improvement in P_{SAT}. This small gain is likely due to the elimination of the PSC effect, which slightly enhances the efficiency and output power, but does not result in a significant difference compared to the HR-1900 substrate.

Distributed Balun on High Resistivity Substrate

The improvement in the output power of the power amplifier, approximately 0.5 dB, raises an important question: which specific element of the power amplifier contributes to this improvement? Based on previous results in **Section 4.1**, it has been demonstrated that the substrate significantly impacts large-surface switches. This observation leads to the hypothesis that the output balun, a critical component of the power amplifier, is also considerably influenced by the substrate properties.

To investigate this hypothesis, the output balun was isolated from the rest of the power amplifier for standalone characterization. This approach enables a focused study of the balun's performance without interference from other circuit elements. A photograph of the standalone output balun, as shown in **Figure 4.21**, reveals its configuration. The standalone output balun was tested on both the POR and HR substrates to evaluate how substrate characteristics affect its performance.

It is evident (from the photograph in **Figure 4.21**) that the dimensions of the distributed balun are significantly larger compared to the RF pads used in the setup. This substantial size highlights the balun's role as a large, distributed structure that is likely to exhibit substrate-dependent behavior. Understanding this dependency is crucial, as it allows for the identification of the substrate's influence on the overall performance of the power amplifier, particularly in terms of output power. By characterizing the standalone balun on different substrates, valuable insights can be gained into the substrate's effect and how it contributes to the observed improvements in output power.

It is important to highlight that the distributed balun (referred to as balun 3 in **Figure 4.11**) significantly impacts both the output power and the efficiency of the power amplifier. This balun operates under high-power conditions, making

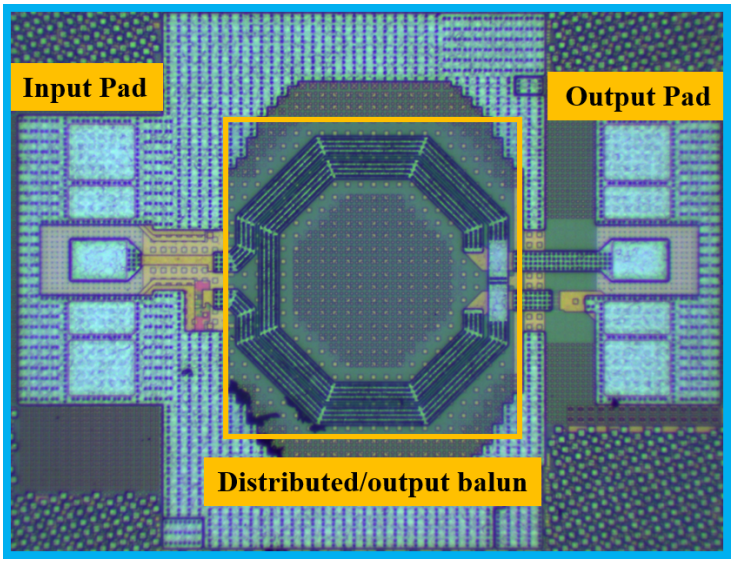


Figure 4.21: Photograph of the standalone output matching network structure, measured on both studied substrates: POR and HR-1900. The dimensions of the distributed balun given in the yellow area is around 310×290 µm.

it particularly sensitive to losses, mismatches, and inefficiencies. Even a small loss in Balun 3 can significantly reduce the output power delivered to the load, impacting the overall efficiency and linearity of the amplifier.

Furthermore, the interstage matching transformer is more critical than the input balun because it directly affects the signal transfer to the power stage. Losses or mismatches in the interstage balun can reduce the signal strength delivered to the power stage.

Figure 4.22 presents the reflection coefficient S_{11} in **(a)** and the transmission coefficient S_{21} in **(b)** of the measured distributed balun on both POR and HR-1900 substrates. At 37 GHz, the losses of the balun on the POR substrate are 4.6 dB, whereas on the HR substrate, the losses are 4.2 dB. The maximum difference between the two substrates is 0.4 dB, indicating an improvement with the HR substrate. This improvement could partially explain the enhanced total output power observed in the power amplifier.

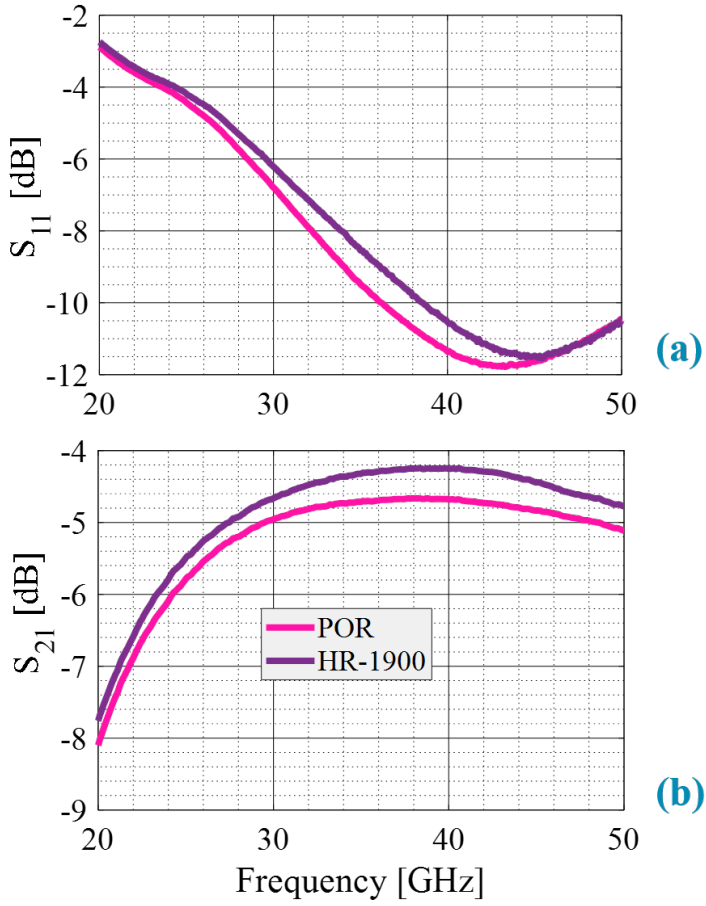


Figure 4.22: Measured reflection coefficient (S_{11}) of the standalone distributed balun in **(a)** and transmission coefficient (S_{21}) in **(b)** for both POR and HR-1900 substrates.

The matching network in the power amplifier is specifically designed to maximize output power under large-signal operating conditions, where the power amplifier exhibits nonlinear behavior. This optimization is achieved by tuning the load impedance to an optimal value that enables the PA to deliver maximum power. The determination of this optimal load impedance is carried out using load-pull simulations, which account for the nonlinear characteristics of the PA.

However, when the same matching network is used with the standalone balun, the situation changes significantly. The standalone balun operates as part of a linear system, where the maximum power transfer is governed by the principle of conjugate matching. In this case, the load impedance is adjusted to match the complex conjugate of the source impedance for optimal performance. This approach is fundamentally different from the load-pull optimization used in the nonlinear PA, where the impedance is specifically adjusted to maximize power under large-signal conditions rather than achieving a simple conjugate match.

Overall, the matching network in the PA is tailored to optimize the nonlinear behavior of the amplifier, ensuring maximum power delivery. When used with the standalone balun, however, the absence of the nonlinear load-pull effects from the PA causes the matching network to function in a purely linear system, resulting in performance characteristics dictated by conjugate matching. This absence of the optimized impedance environment is the primary reason why the standalone balun does not achieve proper matching (see **Figure 4.22(a)**).

4.2.5 Benchmarking

Table 4.5 presents a comparative analysis of state-of-the-art SOI power amplifiers operating close to 28 GHz frequency. Using 22FDX® technology, the design reported in this thesis employs a distributed balun architecture, which is particularly well-suited for wideband high-frequency operation.

In terms of frequency range, this work operates between 24 and 43 GHz, which is one of the broadest ranges presented in the table. This range is notably wider than narrow-band designs, such as those in references that operate within 28 GHz or 27 GHz. This broader range demonstrates the versatility of the design and its capability to address a variety of applications within the mmWave spectrum.

In terms of gain, this work achieves a range of 18–30 dB, making it competitive with other designs in the table. For instance, some designs report gains around 21 dB, while others achieve up to 26.1 dB. The high gain achieved by this work ensures strong signal amplification across its wide operational bandwidth, making it particularly suitable for applications requiring both high gain and wideband operation.

The maximum PAE for this work ranges from 26 to 35 %, which is among the highest efficiencies reported in the table. While a few designs achieve PAEs as high as 42, 45 %, the efficiency of the design reported in this thesis is well-balanced with its gain and bandwidth, demonstrating its ability to deliver strong performance while maintaining power efficiency thanks to HR substrate.

This work achieves a saturation power Psat of 17–19 dBm, which is comparable to other designs operating in the same frequency range. For instance, the work in [154] reports a Psat of 18–20.7 dBm, while others, such as [155] and [156] , demonstrate Psat values in the range of 17.4–17.8 dBm and 17.9–20.4 dBm, respectively. Although some designs, like [157] , achieve a higher Psat of 23.3 dBm, this work offers a balanced combination of Psat, efficiency, and bandwidth, making it an excellent choice for applications prioritizing wideband operation.

Table 4.5: State of the art SOI power amplifiers operating close to 28 GHz.

Work	Technology	Architecture	Supply [V]	Frequency [GHz]	Psat [dBm]	Gain [dB]	PAEmax [%]	Year
[154]	28 nm FDSOI	Broadband balanced	2	22-42	18-20.7	21-23	20-34.9	2023
[155]	28 nm FDSOI	Adaptive bias control	2	28-34	17.4-17.8	13.8	37.8-42.5	2021
[158]	22 nm FDSOI	2 stacked diff.	1.6	28	21	23.5	31.5	2022
[159]	22 nm FDSOI	Doherty	2.4	28	22.5	26.1	28.5	2021
[157]	45 nm PDSOI	Current combining	2.4	28	21.7	27	27.1	2020
[160]	45 nm PDSOI	Mixed signal Doherty	2.4	27	23.3	19.1	40.1	2019
[156]	22 nm FDSOI	Distributed balun	2	24-42	17.9-20.4	17.5-20	35-45	2020
[161]	22 nm FDSOI	RC feedback 1-stage diff.	2	19.1-46.5	12.9-14.6	13.4-16.4	15.2-26.1	2022
[140]	22 nm FDSOI	Distributed balun	1.8	24-44	16.6-18.6	17.4-27.7	27.2-36.4	2024
This Work	22 nm FDSOI	Distributed balun	2.4	24-43	17-19	18-30	26-35	2024

This work demonstrates a well-balanced performance profile, with a saturation power of 17–19 dBm, a gain of 18–30 dB, a PAE of 26–35 %, and an industry-leading operational bandwidth of 24–43 GHz. Compared to other designs in the table, it offers a unique combination of high efficiency, competitive saturation power, and wideband capability thanks to the HR substrate.

Aside from designing a stable power amplifier (PA) that meets the two fundamental requirements of stability ($K > 1$ and $\Delta < 1$), it has been shown that the HR-1900 substrate offers only a modest improvement of 0.5 dB in output power compared to the PA built on a POR substrate. In addition to the output power improvement, the HR-1900 substrate also offers a 6 % increase in PAE. This improvement in PAE is important because it reduces heat generation within the PA. When the PA operates more efficiently, less DC power is wasted as heat, which not only enhances the longevity of the amplifier components but also simplifies thermal management in the PA.

However, despite the benefits of increased PAE, designers typically prioritize output power over PAE in the context of PA design. The primary role of the PA in a front-end module is to generate a high power level to effectively transmit the signal through the switch. Higher output power directly contributes to better signal transmission, ensuring that the signal reaches its intended destination with sufficient strength. Therefore, while improvements in PAE are valuable, the focus often remains on maximizing output power to meet the primary functional requirements of the PA.

When considering the design of a complete transceiver on a high-resistivity substrate within the same chip, the benefits extend beyond just the PA. Since other critical components such as the switch, LNA, and VCO are significantly improved by using an HR substrate, integrating the PA on the same HR substrate could further enhance the overall gain and performance across the entire transceiver chain. The integration of the PA with other components that benefit from the HR substrate, like the switch, LNA, and VCO, would likely result in better overall system efficiency. This approach leverages the modest but valuable improvements in output power and efficiency, contributing to the superior performance of the entire system.

4.3 28 GHz Down-Conversion Mixer in 22FDX®

In this section, our study focuses on downconversion RF mixers, which are integral components in the receive path of a given front-end module. Historically, the Gilbert cell has been the predominant topology for mixer design, especially over the past decade. However, recent advancements have led to the introduction of various alternative mixer topologies, each tailored to meet the specific demands of different receiver (RX) or transmitter (TX) architectures.

Initially, a detailed explanation of the operation of the Gilbert cell mixer will be provided, followed by the design, fabrication, and measurement of its performance. The Gilbert cell is widely used due to its balanced operation and superior linearity, making it a foundational element in mixer design.

Following this, a novel topology, known as the back-gate mixer, will be introduced, which has recently been proposed to the scientific community. This topology offers several advantages, particularly in terms of mixing using a single FET. However, certain drawbacks must also be considered, such as the high power injection required for the back-gate.

4.3.1 Gilbert Cell: From Fundamentals to Performance Evaluation

It has been demonstrated in [151] that a mixer can be simply realized as shown in Figure 4.23(a). In this configuration, when the V_{LO}, is in the ON state, the output signal V_{IF} is equal to the input RF signal V_{RF}. Conversely, when V_{LO} is OFF, the output is V_{IF}=0. This mechanism essentially allows the mixer to act as a switch, turning the RF signal on and off at the rate of the LO frequency.

When the switching is abrupt, this operation can be viewed as the multiplication of the RF signal V_{RF} with a square wave in the time domain, as illustrated in Figure 4.23(b). In the frequency domain, this multiplication translates into a convolution of the RF signal, which typically consists of a band of frequencies centered around f_{RF}, with the Fourier series of the square wave.

The fast Fourier transform of the square wave is a series of Dirac delta functions (impulses) at odd multiples of the f_{LO}. As a result, the RF signal, originally centered around f_{RF}, is shifted and replicated around f_{LO} and its harmonics, as shown in Figure 4.23(d). This process effectively mixes the RF

signal with the LO signal, translating it to different frequency bands. This frequency shifting is the core function of the mixer, enabling the downconversion.

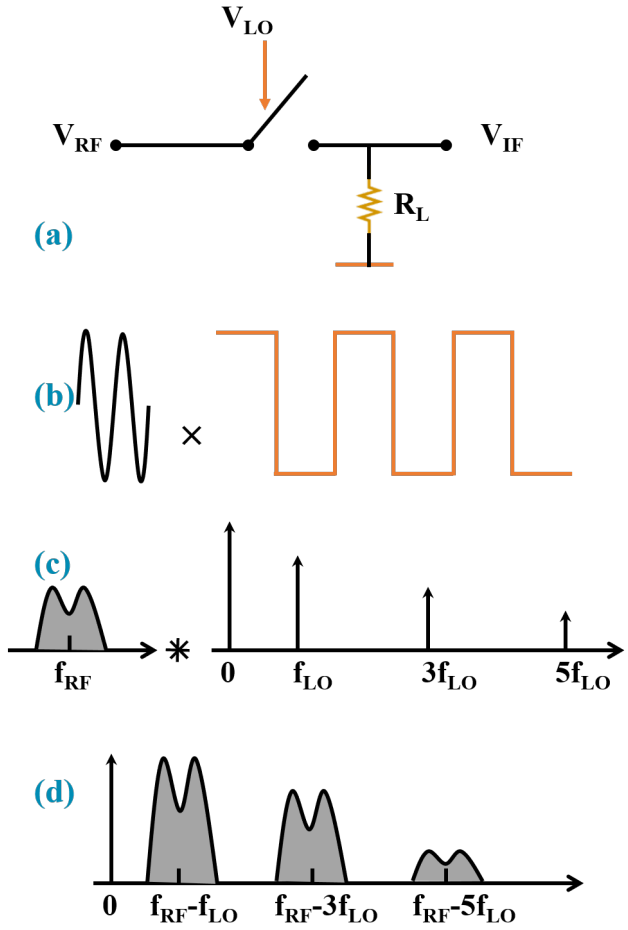


Figure 4.23: Mixer principal working using simple elements in (a), then in time domain in (b), then if frequency domain in (c) and mixing result in (d).

Noise Figure and Linearity of Mixer Correlation

The design of mixer depends generally on low noise amplifier figures of merit. It has been demonstrated in [162] that for a given system with multiple circuits in cascode, the overall noise figure NF_{total} is given by the equation:

$$NF_{total} = NF_1 + \frac{G_1 \cdot (NF_2 - 1)}{G_1} + \frac{G_1 \cdot G_2 \cdot (NF_3 - 1)}{G_1 \cdot G_2} + \cdots \tag{4.16}$$

Where NF_i and G_i are the noise figure and gain of a single stage. This formula is commonly used when designing an LNA with multiple stages. The total noise figure is not the product of the noise figure of each stage, it is always given by Friis formula in **Equation 4.16**.

Let's consider a simple sytem with an LNA (with a gain G_{LNA} and a noise figure NF_{LNA}) followed by a mixer (G_{Mixer} and NF_{Mixer}), then the NF_{toal} given by **Equation 4.16** is:

$$NF_{total} = NF_{LNA} + \frac{NF_{Mixer} - 1}{G_{LNA}} \tag{4.17}$$

Equation 4.17 illustrates how the noise contribution from the mixer appears reduced when the low-noise amplifier (LNA) preceding it has a high gain. However, this does not imply that the mixer should be designed with a high noise figure. Instead, the equation suggests that a high-gain LNA can mitigate or "mask" the noise generated by the mixer to some extent, improving the overall noise performance of the system. Nevertheless, it's important to emphasize that the mixer should still be designed with careful consideration of its noise performance. Relying solely on the LNA's gain to compensate for a noisy mixer is not an optimal design strategy, as this could lead to suboptimal performance in scenarios where the LNA's gain is insufficient to fully suppress the mixer's noise. Therefore, both the LNA and mixer should be optimized to achieve the best possible noise performance in the overall system.

Regarding the P1dB compression point (which is the point where the gain decreases by 1 dB from its linear gain), the P1dB of the whole system is given by **Equation 4.18** from [163]:

$$\frac{1}{P1dB_{total}} = \frac{1}{P1dB_1} + \frac{1}{G_1 \cdot P1dB_2} + \frac{1}{G_1 \cdot G_2 \cdot P1dB_3} + \cdots \tag{4.18}$$

By considering the system of LNA (with a compression point $P1dB_{LNA}$) and a mixer ($P1dB_{Mixer}$), the **Equation 4.18** will become:

$$\frac{1}{P1dB_{total}} = \frac{1}{P1dB_{LNA}} + \frac{1}{G_{LNA} \cdot P1dB_{Mixer}} \tag{4.19}$$

Equation 4.19 demonstrates that the overall $P1dB_{total}$ of a system is primarily determined by the stage with the lowest P1dB. This relationship underscores the importance of careful co-design between the mixer and the low-noise amplifier (LNA) when setting system specifications [151]. Since the P1dB of the system is limited by its weakest link, it is crucial to consider the impact of each component within the RF chain. The interdependence between the LNA and mixer highlights the need to optimize both stages to achieve a balanced performance.

4.3.2 Conversion Gain in Mixers

An RF mixer with high gain is of high importance since it helps to amplify the RF signal while suppressing the noise contributed by the stages that follow the mixer in the signal chain. Since the mixers converts an RF signal at frequency f_{RF} to another frequency f_{IF}, the conversion gain (instead of gain) is defined as:

$$CG = \frac{V_{IF} \text{ at } f_{IF}}{V_{RF} \text{ at } f_{RF}} \tag{4.20}$$

Where V_{RF} is the voltage of the RF signal and V_{IF} is the voltage of the output signal.

In this thesis, the focus is specifically on active mixers, which are characterized by their ability to provide a conversion gain greater than 1. This is possible because active mixers utilize an applied DC supply power, which enhances the signal strength during the frequency conversion process. The use of a DC bias enables the active components, such as transistors, to amplify the signal, resulting in a net gain.

It is worth noting that it is also possible to implement passive mixers, which do not require a DC supply for operation. In passive mixers, the frequency conversion is achieved using passive components, such as diodes or switches, without any active amplification of the signal. As a result, instead of achieving a conversion gain (CG), passive mixers typically exhibit a conversion loss (CL). This means that the output signal after frequency conversion is weaker than the input signal. Passive mixers are often chosen for their simplicity and lower power consumption.

Thus, the distinction between active and passive mixers lies in the use of a DC bias and the resulting performance characteristics. While active mixers can amplify the signal and provide conversion gain due to their active nature, passive mixers, lacking this DC bias, lead to conversion loss.

4.3.3 Port-to-Port Feedthrough

Feedthrough refers to the unintended coupling or leakage of signals between different ports of a mixer. As discussed earlier, the LO signal is typically a large signal at a frequency f_{LO}. The primary objective in mixer design is to ensure that the power LO does not leak to RF or IF ports. In practical simulations or measurements, it is possible to evaluate the feedthrough between all the ports. However, since the RF and IF signals are generally much smaller in amplitude compared to the LO signal, they are less likely to couple to other ports. The main concern is that the large-signal LO could influence the RF and IF ports, leading to undesirable signal mixing or interference. This LO feedthrough can create spurious signals, reduce the signal-to-noise ratio, and degrade the linearity of the mixer.

4.3.4 Noise Figure of a Mixer

The noise figure (NF) of a mixer quantifies the additional noise introduced by the mixer during the frequency conversion process, compared to an ideal, noiseless system. It measures how much the signal-to-noise ratio (SNR) degrades as the signal passes through the mixer. This makes the noise figure a crucial parameter for assessing the performance and efficiency of RF and microwave systems. The noise figure is often expressed in decibels (dB) as:

$$\text{NF (dB)} = 10 \cdot \log_{10}\left(\frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}\right) \tag{4.21}$$

Where SNR_{in} is signal-to-noise ratio at the input of the mixer and SNR_{out} is signal-to-noise ratio at the output of the mixer.

Physically, a noise figure of 0 dB means an ideal mixer that does not introduce any additional noise. A higher noise figure indicates that the mixer adds more noise, reducing the quality of the output signal.

4.3.5 Third-Order Intercept Point (IP3)

The third-order intercept point (IP3) is an essential parameter for evaluating the linearity of RF mixers and their ability to process large signals without introducing significant distortion. It quantifies the point at which the power of the third-order intermodulation products equals the power of the desired signal, serving as a hypothetical measure of the mixer's behavior under non-linear conditions.

Throughout this thesis, only simulations of the third-order intercept point (IP3) are performed using Cadence Virtuoso. These simulations utilize two tones for the RF signal, specifically at 28 GHz and 28.3 GHz, with a local oscillator (LO) frequency of 21 GHz. The fundamental output power brought to the baseband corresponds to the intermediate frequency (f_{fund}) and is calculated as follows:

- For the first RF tone:

$$f_{\text{IF}} = f_{\text{RF1}} - f_{\text{LO}} = 28 - 21 = 7 \text{ GHz} \tag{4.22}$$

- For the second RF tone:

$$f_{\text{IF}} = f_{\text{RF2}} - f_{\text{LO}} = 28.3 - 21 = 7.3 \text{ GHz} \tag{4.23}$$

The third-order intermodulation power brought to the baseband appears at f_3, which is derived from the nonlinearity of the mixer:

- For the first intermodulation product:

$$f_3 = 2f_{RF2} - f_{RF1} - f_{LO} = 2 \times 28.3 - 28 - 21 = 7.6\,\text{GHz} \quad \textbf{(4.24)}$$

- For the second intermodulation product:

$$f_3 = 2f_{RF1} - f_{RF2} - f_{LO} = 2 \times 28 - 28.3 - 21 = 6.7\,\text{GHz} \quad \textbf{(4.25)}$$

The IP3 is often represented graphically to illustrate the relationship between input power, output power, and intermodulation distortion in RF systems. Specifically, it is depicted as the point where two extrapolated lines meet. The first line represents the power of the desired fundamental signal, which increases linearly with the input power at f=f_{fund}. This linear behavior indicates the ideal operation of the system, where output power is directly proportional to input power without significant distortion.

The second line represents the power of the third-order intermodulation products at f=f_3. These unwanted distortion components are generated due to the system's inherent nonlinearity. Unlike the fundamental signal, the power of these intermodulation products grows at a faster rate—specifically, 3 dB for every 1 dB increase in input power.

The IP3 is a theoretical point at which these two lines intersect. It signifies the input power level where the power of the third-order intermodulation products would become equal to the power of the desired signal. In practice, this point is inexistent because no real device can operate linearly up to this level. Instead, as the input power increases, the device reaches its saturation point before the IP3 is physically reached. Beyond this saturation point, the system's behavior deviates significantly from the linear approximation used to define the IP3 **[151]**.

4.3.6 Single Balanced Gilbert Cell Mixer

Figure 4.24(a) shows the conventional single ended Gilbert cell mixer. M1 FET converts the input RF signal to a current (it is also called transconductor), M2 an M3 FETs are interrupting the RF signal ideally, this is why they are called switching pair FETs. R1 and R2 convert the output currents to voltage.

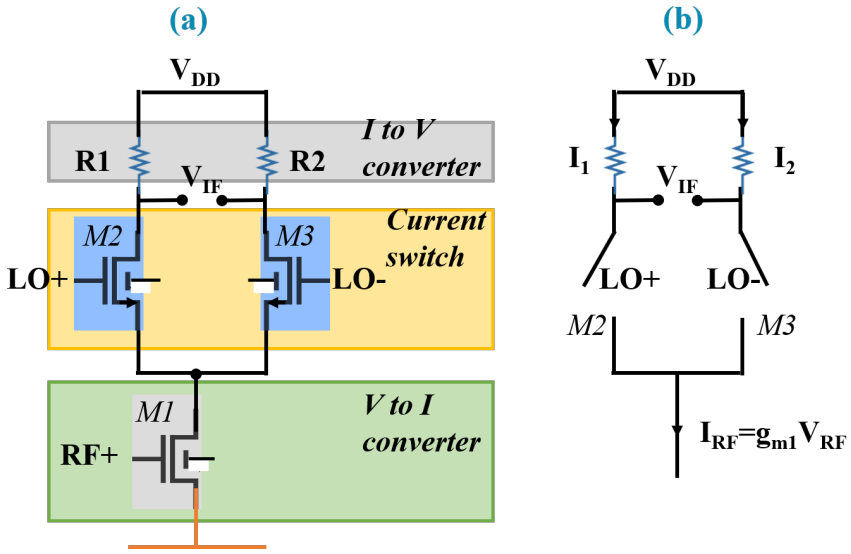


Figure 4.24: Schematic of the single balanced Gilbert cell mixer topology in (a). Equivalent circuit of the mixer in (b).

M1 generates a small-signal drain current I_{RF} proportional to $g_{m1} \cdot V_{RF}$ while the LO signal induces abrupt switching. Considering that M2 multiplies the I_{RF} current by a square wave S(t), and M3 multiplies the I_{RF} current by a square wave $S\left(t - \frac{T_{LO}}{2}\right)$ since LO+ and LO- are complementary we will have:

$$I_1 = I_{RF} \cdot S(t) \tag{4.26}$$

$$I_2 = I_{RF} \cdot S\left(t - \frac{T_{LO}}{2}\right) \tag{4.27}$$

By considering R1=R2=R, then:

$$V_{out} = R \cdot (I_2 - I_1) \tag{4.28}$$

By replacing the currents from **Equation 4.26** and **Equation 4.27** in **Equation 4.28** we will get:

$$V_{out}(t) = I_{RF} \cdot R \left[S\left(t - \frac{T_{LO}}{2}\right) - S(t) \right] \tag{4.29}$$

The square wave in time domain becomes a consecutive direacs in frequency domain with first amplitude at f_{LO} is $\frac{4}{\pi}$. Then we write:

$$V_{out}(t) = I_{RF}(t) \cdot R \cdot \frac{4}{\pi} \cos \omega_{LO} t + \cdots \tag{4.30}$$

Since $I_{RF}(t) = g_{m1} \cdot V_{RF} \cdot \cos(\omega_{RF})t$, then the IF signal will written as:

$$V_{IF}(t) = \frac{2}{\pi} \cdot g_{m1} \cdot R \cdot V_{RF} \cdot \cos\left(\omega_{RF} - \omega_{LO}\right) t \tag{4.31}$$

The conversion gain is therefore equal to:

$$CG = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} \cdot g_{m1} \cdot R \tag{4.32}$$

The conversion gain depends on the sizing of the FET M1 and to the resistance load. The M1 FET is sized according to the overdrive voltage V_{OV} that gives the good IP3. It is worth noting that the g_{m1} is limited by the current imposed by the identical FETs M2 and M3. The value of g_{m1} is given by:

$$g_{m1} = \frac{2I_{D1}}{V_{GS1} - V_{TH1}} \tag{4.33}$$

Moreover, the resistor R is limited by the maximum allowable voltage accross it. The linearity of active mixers is largely determined by the overdrive voltage of the input transistor M1. A higher overdrive voltage allows the transistor to operate in a more linear region of its transfer characteristics, which reduces

distortion and improves the linearity of the mixer. However, increasing the overdrive voltage also increases the current through the transistor, which can lead to higher power consumption and potentially increased noise. The FET M1 imposes direct trade-off between the non linearity and total noise.

$$\text{IP3} \propto V_{GS1} - V_{TH1} \tag{4.34}$$

On the other hand, the noise is given by:

$$\overline{V_{n,in}^2} = \frac{\text{Constant}}{2I_D} \cdot (V_{GS} - V_{TH}). \tag{4.35}$$

Increasing the gain of the mixer often necessitates minimizing the overdrive voltage of the transistor M1. By making the overdrive voltage as small as possible, the transistor operates closer to its threshold voltage, which can significantly reduce the total noise contribution of the mixer. However, this approach comes with a trade-off: while the noise performance improves, the linearity of the mixer tends to decrease substantially. The reduced overdrive voltage limits the transistor's ability to handle large signal swings, leading to higher distortion and, consequently, lower linearity.

On the other hand, increasing the overdrive voltage enhances the linearity of the mixer. A higher overdrive voltage allows the transistor to operate further into the linear region of its transfer curve, which improves its ability to process large signals without significant distortion. This results in a highly linear mixer, capable of maintaining signal integrity even with large input signals. However, this comes at the cost of reduced gain and increased total noise. The higher overdrive voltage typically requires higher current through the transistor, which can increase thermal noise and reduce the overall gain of the mixer.

4.3.7 Gradual LO Transitions

In **Equation 4.32** it has been supposed that the current produced by the LO power is square wave. Since the LO signal injection is a sine wave, at a given moment both switching pairs are on OFF state and probably reducing the conversion gain during that short time except if LO is a square wave. **Figure 4.25** shows the effect of gradual LO transition, where during the ΔT the gain is reduced, because the FETs are not a perfect switches.

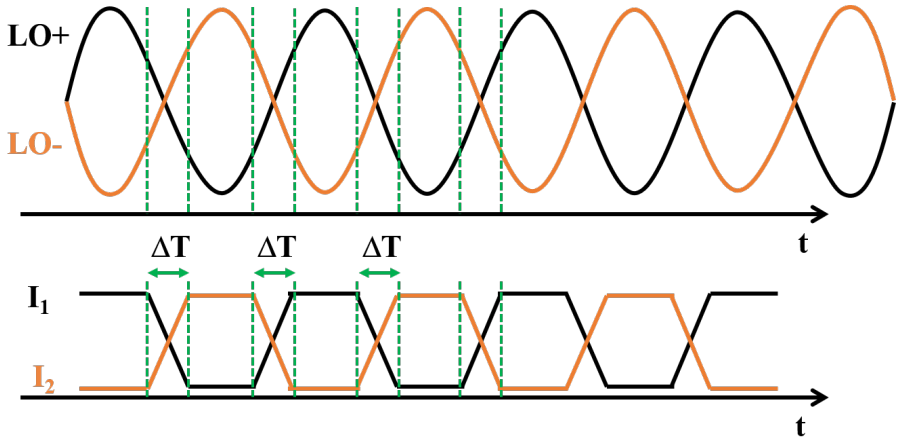


Figure 4.25: Demonstration of the time where the conversion gain is reduced because the current is not square wave.

If we consider equilibrium voltage overdrive, $(V_{GS} - V_{TH})_{eq}$ as the quiescent operating point (where the switching pair is not influenced by an input signal). ΔT is given by [151] as:

$$\Delta T = \frac{(V_{GS} - V_{TH})_{eq}}{5 \cdot V_{p,LO} \cdot \omega_{LO}} \tag{4.36}$$

Where $V_{p,LO}$ is the maximum (peak) value of the LO signal. In this case, Equation 4.32 is reduced to:

$$CG = \frac{2}{\pi} \cdot g_{m1} \cdot R \cdot \left(1 - \frac{2\Delta T}{T_{LO}}\right) \tag{4.37}$$

$$CG = \frac{2}{\pi} \cdot g_{m1} \cdot R \cdot \left[1 - \frac{(V_{GS} - V_{TH})_{eq}}{5 \cdot \pi \cdot V_{p,LO}}\right]. \tag{4.38}$$

This equation demonstrates that the conversion gain depends not only on the load resistance and size of M1 but also on the large signal applied by V_{LO}. It shows that the conversion gain decreases if the LO amplitude is not sufficiently large compared to the equilibrium overdrive voltage.

4.3.8 Active Load and TIA to Improve Mixer Performance

So far in this thesis, the design flow has been described. Using this information, it is possible to design an RF mixer for a given frequency. The performance of a mixer can be enhanced by adding various elements, such as increasing linearity by using a resistor or an inductor at the source of the RF FETs, applying dynamic current injection [164], or increasing gain through negative resistance generation [165], current reuse technique [166]. In this thesis, an active load and a transimpedance amplifier are employed to enhance the mixer's performance.

Active Load (AL)

Figure 4.26 shows an active load circuit composed of the PMOS FETs M7 and M8. Its main objective is to enable a high-gain mixer.

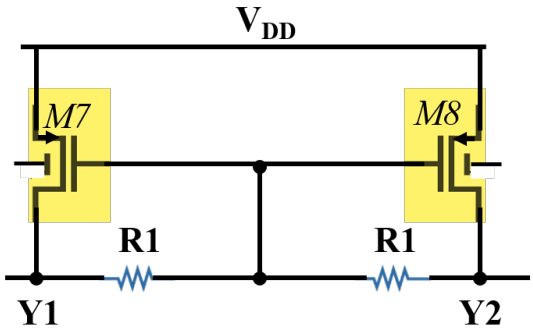


Figure 4.26: Schematic of the active load used in RF mixers.

These FETs are connected in a way that allows them to provide high small-signal resistance to the differential signals present at nodes Y1 and Y2. The two FETs are replacing the resistors in a simple RF circuit. Since they are transistors, they can provide a much higher small-signal resistance than a resistor would, particularly when biased in the sub-threshold. This is demonstrated through the small-signal output resistance of a MOSFET in saturation that is given by:

$$r_o = \frac{1}{\lambda \cdot I_D} \tag{4.39}$$

Where r_0 is the output resistance of the PMOS transistor, λ is the channel-length modulation parameter and I_D is the drain current of the FET. Since r_0 is inversely proportional to λ and I_D, the FETs M7 and M8 can provide a high resistance especially when I_D is low.

Biasing M7 and M8 in sub-threshold mode increases the V_{GS} helping the FET to maintain high resistance while drawing minimal current, thereby improving the efficiency and gain of the circuit. Moreover, it has been shown in **[167]** that the FETS M7 and M8 *self-regulate* the potential at the nodes Y1 and Y2. This regulation prevents the degradation of conversion gain, especially at high LO levels.

The high value of the resistor R1 is used in order to ensure that the output voltages Y1 and Y2 remain balanced and the differential operation of the circuit is not disrupted by common-mode voltage fluctuations. Moreover, the feedback loop adjusts the gate voltages of M7 and M8 ensuring that the common-mode voltage at Y1 and Y2 is stable.

Transimpedance Amplifier (TIA)

The transimpedance amplifier (TIA) is used to convert an input current signal into a corresponding output voltage is shown in **Figure 4.27**.

In this configuration, both the PMOS and NMOS transistors (M9 and M10, respectively) contribute to the total transconductance, which is the sum of their individual transconductances $g_{m,total} = g_{m,M9} + g_{m,M10}$. This approach increases the efficiency and gain of the amplifier compared to single-transistor designs. The medium value of the resistor R2 (50-700 Ω) is fixing the gain of the TIA.

The small-signal gain of the transimpedance amplifier is expressed as:

$$G = \frac{V_{out}}{I_{in}} = R_2 \tag{4.40}$$

This equation indicates that the transimpedance gain is directly determined by the value of the feedback resistor R2. The feedback mechanism ensures that the input current is converted into a proportional output voltage, with the

feedback resistor defining the proportionality.

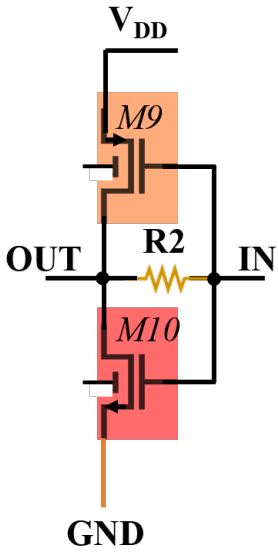


Figure 4.27: Schematic of the transimpedance amplifier (TIA) used in RF mixers.

The TIA is commonly used to maintain sufficient overall conversion gain concerning the LO power and to achieve a broadband IF characteristic [168, 169].

Throughout this thesis, both active load and transimpedance amplifier techniques are used to enhance circuit performance. It is worth noting that, depending on the design requirements, it is possible to use one of these techniques instead of both. Additionally, several other enhancement techniques have been proposed in the literature, as referenced in [151], including current-source helpers, enhanced transconductance methods, and low flicker noise mitigation strategies, which can further improve circuit efficiency and performance.

4.3.9 Gilbert Cell Topology: Circuit Design

Due to the superior isolation, enhanced gain, and improved noise figure provided by the double-balanced mixer compared to the single-balanced topology, the double-balanced topology has been adopted and designed throughout this thesis to optimize RF performance and ensure superior results in terms of signal integrity and overall efficiency.

Figure 4.28 shows a detailed schematic of the double balanced Gilbert cell mixer with an input RF signal frequency at 28 GHz, LO frequency at 21 GHz and IF frequency at 7 GHz. The voltage to current stage uses 2 nMOSFETs M1 and M2 super-low threshold voltage with a gate length of 20 nm and a total FET width of 75 µm with 60 finger, 1.25 µm width of each finger. A relaxed contact poly-pitch is used (CPP$\times$2), which increases f_t and f_{max}, reduces the source and drain extrinsic resistances, this is used for all FETs in this design. 20 nm gate length demonstrates a good trade-off between high RF performance and reliability. Then the switching quad composed of M3, M4, M5 and M6 are with same FET type with half of the width of the RF stage. They are 37.5 µm FET total width and 30 fingers with 1.25 µm each finger. It is worth noting that the dimensions of the switching quad is half the one from RF stage, because in DC, the M1 FET will receive half current from M3 ad the other half from M4.

The active load is based on the R1 resistors with 5 kΩ each and are used in polysilicon. The pMOSFET M7 and M8 have a total width of 25 µm and 58 fingers and each finger is 430 nm width, they were chosen in such a way to have a good compromise between the linearity and the gain.

The TIA is formed using a 500 Ω resistor, an unsilicided N+ diffusion resistor within the SOI is chosen due to its low inductance and validated high-frequency model. Second, as the resistor width decreases for a fixed resistance value, the length also decreases. Since the reactance of the resistor significantly increases with larger dimensions, the minimum width of 360 nm is selected. pFETs M9 and M11 are with a total width of 75 µm, 55 fingers and 1.36 µm of finger width. nFETs M10 and M12 are with a total width of 72.5 µm, 58 fingers and 1.25 µm of finger width.

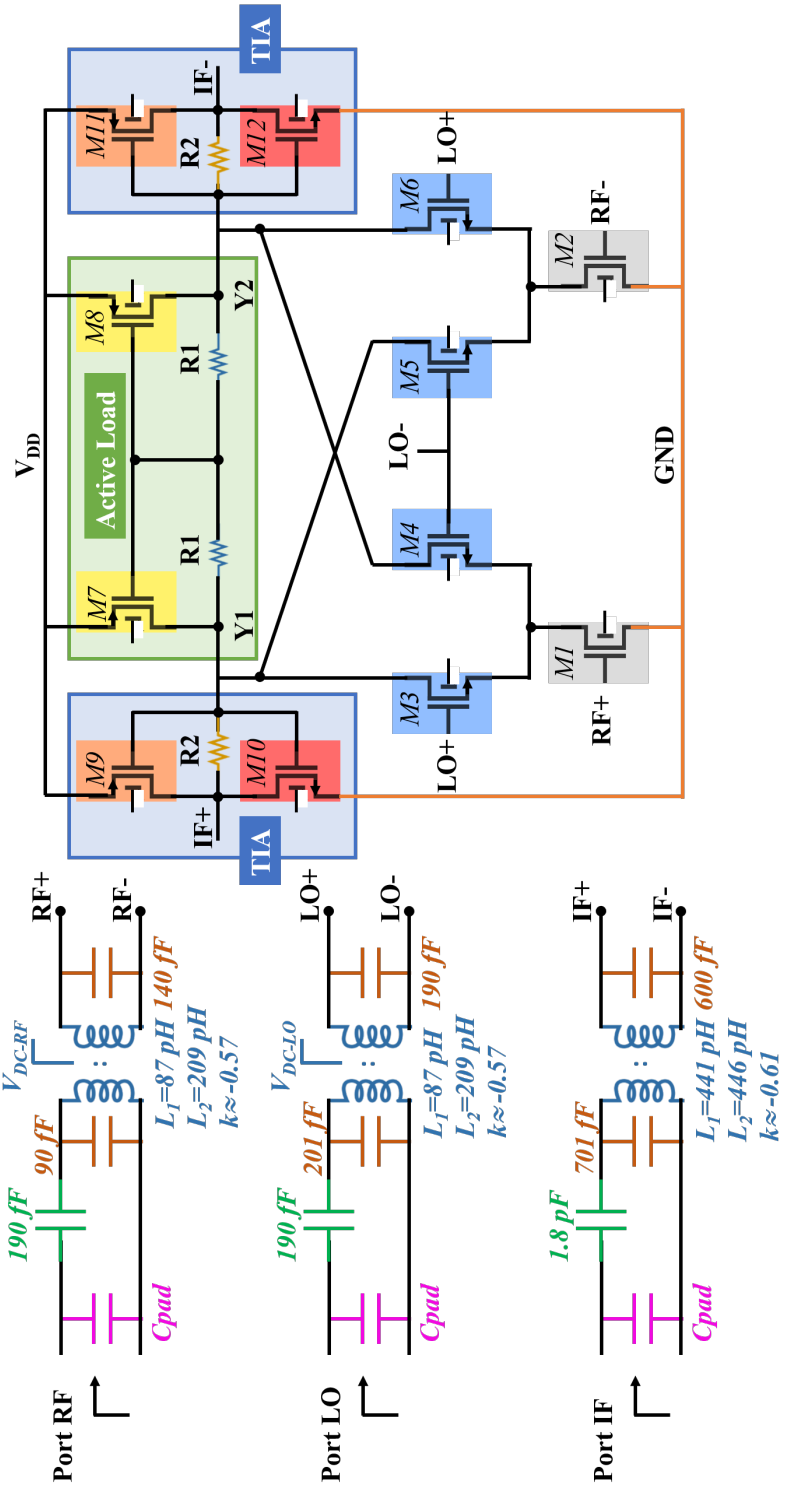


Figure 4.28: Schematic diagram of the Gilbert cell topology down-conversion mixer using an active load and a transimpedance amplifier. The baluns at 3 different frequencies are also shown. Design made for a POR substrate.

The generation of differential signals RF+, RF-, LO+, LO-, IF+ and IF- is achieved through the use of integrated baluns designed to operate at each specific frequency. Interleaved baluns are employed, meaning they are placed on a single metal layer just before the last metal layer. This configuration was chosen to maximize the distance from the substrate. At the RF port, the interleaved balun consists of inductors L1= 87 pH and L2=209 pH with a coupling factor k=0.57. This configuration is optimized to convert the RF signal from a single-ended input to a differential output, with the appropriate impedance matching required for RF signal. A bias DC V_{DC-RF} is 400 mV. The capacitors 190 fF, 90 fF and 140 fF are used in order to allow compensation of the inductive part by the capacitive part in the smith chart to 28 GHz frequency. Particularly the 140 fF helps to have the two signals out of phase (180°).

At the LO port, the interleaved balun consists of inductors L1 = 87 pH and L2 = 209 pH, identical to the configuration used at the RF port with a bias V_{DC-RF}=0.6 V. The primary objective was to identify the optimal capacitances that would compensate for the inductive reactance, thereby positioning the impedance at the center of the Smith chart at 21 GHz. This goal was achieved by employing shunt capacitances to precisely balance the inductive components. Specifically, capacitors with values of 201 fF, and 190 fF were strategically selected to introduce the necessary complementary capacitive reactance, effectively neutralizing the inductive reactance and achieving the desired impedance match.

At the IF port, the interleaved balun is configured with inductors L1 = 441 pH and L2 = 600 pH, featuring a coupling factor of k = 0.61. This specific configuration is designed to accommodate the relatively low frequency of 7 GHz, necessitating larger inductor values compared to those used at the RF and LO ports. To effectively convert the differential signal (out of phase) from the double-balanced mixer into a single-ended output, capacitors with values of 701 fF, 1.8 pF, and 600 fF are employed. These capacitors are carefully selected to ensure proper phase alignment and signal conversion. Additionally, a single pad with a capacitance of approximately 65 fF is used in the design.

4.3.10 Gilbert Cell RF Measurements

In this section, we will present and thoroughly discuss both the small-signal and large-signal measurements of the designed mixer. The small-signal measurements will focus on evaluating the S-parameters of each port and impedance matching across the intended frequency range. On the other hand, the large-signal measurements will explore the mixer's performance under higher power of the LO.

S-Parameters Measurements

Figure 4.29(a) is a photograph of a designed down-conversion mixer, showcasing its layout and highlighting key components.

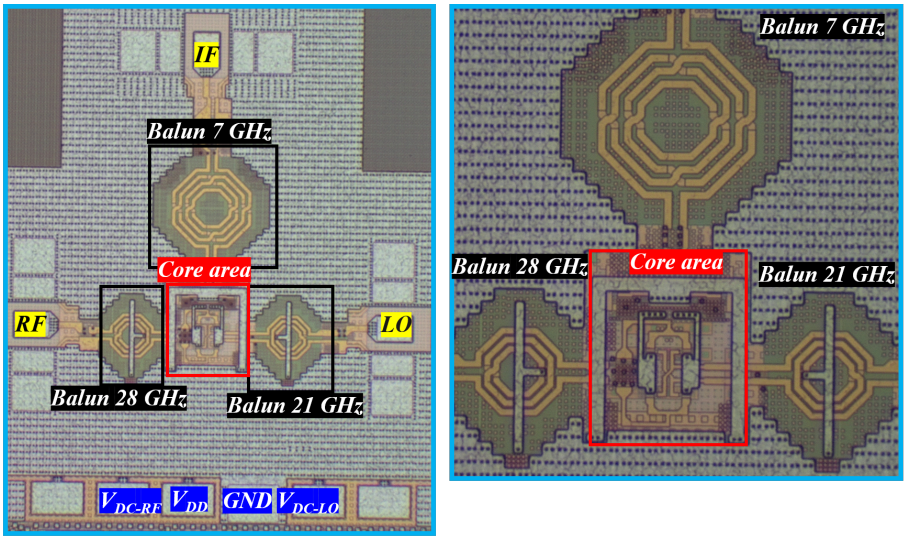


Figure 4.29: Photograph of the designed down-conversion mixer in (a). The total area, including the baluns and excluding the pads is 0.150 mm² in (b). The core active area (highlighted in blue) is 0.008 mm².

At the center of the layout, marked with a red outline, is the *core area* of the mixer. This is the active region where the FETs described above are including the active load and the TIA. Surrounding the core area are three baluns, each

designed for different frequency bands, which are critical for converting single-ended signals into differential signals.

The Balun 28 GHz, located at the bottom-left, handles the RF input at 28 GHz. The Balun 21 GHz, located at the bottom-right, is used for the LO signal at 21 GHz. The Balun 7 GHz, located at the top-center, manages the IF output at 7 GHz. These baluns are interleaved structures, each optimized for their specific operating frequency to ensure efficient signal conversion and impedance matching. The baluns occupy significant portions of the chip area.

At the bottom of the figure, various power supply and ground connections are depicted. The V_{DC-RF} and V_{DC-LO} are connected to the center tap of the baluns. The V_{DD} is fixed at 0.9 V, and the GND pads are so small that they cannot be seen with the naked eye.

S-parameters measurements are calibrated with a Short-Open-Load-Thru (SOLT) calibration performed on an impedance standard substrate to move the reference plane at the probe tips. The measured S-parameters plotted in **Figure 4.30** demonstrate that the mixer is well matched at the LO port at 20.8 to 22 GHz, at the RF port from 27 to 29.5 GHz, and at the IF port from 6.5 to 9.0 GHz.

Simulations align closely with measurements, even at frequencies above 30 GHz, demonstrating that the baluns and the finely tuned capacitances described earlier are in good agreement with the measured results. This correlation indicates that the design choices, including the selection of baluns and the precise tuning of capacitances, effectively yield accurate and reliable performance across the targeted frequency range.

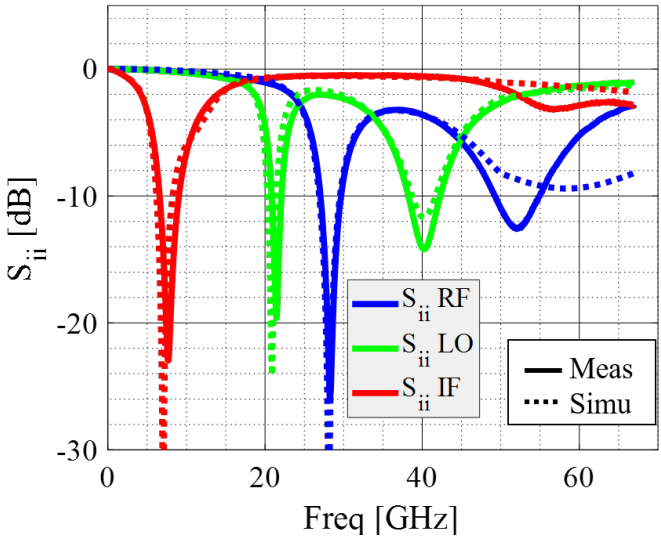


Figure 4.30: Measured and simulated small-signal reflection coefficients for each port of the Gilbert cell topology mixer, evaluating the circuit's matching performance in medium power mode (refer to **Table 4.6**).

Conversion Gain With Respect to LO Power

Large-signal measurements are performed to extract the mixer's FoMs. After calibrating the power of the PNA to the probe tips, an input RF signal at -30 dBm and 28 GHz was injected to the mixer. Then, a power sweep of the LO signal (at 21 GHz) was performed using a separate source from the VNA, while the IF port is connected to one of the VNA's receivers.

Figure 4.31 shows the measured and simulated conversion gain as a function of the LO power P_{LO}, at an RF input power of -30 dBm, measurements agree well with simulations. It is worth noting that the curves in colors are simulations of the mixer atop of POR substrate, while the black dashed curve is the simulation of the mixer atop of HR substrate without PSC effect, having a nominal resistivity of 3 kΩ·cm. The simulation using HR-3 k substrate is performed only for the mixer at Vdd=0.9 V.

Different circuit operating points are possible through the choice of a given power budget. At low LO power, the switching quad FETs are working cor-

rectly in their linear region. They are able to switch between the ON and OFF state, the gain increases with respect to the LO power. At around P_{LO}=-2 dBm, the conversion gain reaches its maximum. At this maximum, the LO power is at an optimal level that fully switches the mixer without pushing it to the saturation. At this point, the mixer is working at the best of its performance. When the LO power continues to increase, the FETs are no more working in the triode region, generating non linearities. Moreover, it pushes the FETs towards the saturation region. In the saturation region, the drain current becomes less sensitive to changes in the drain-source voltage.

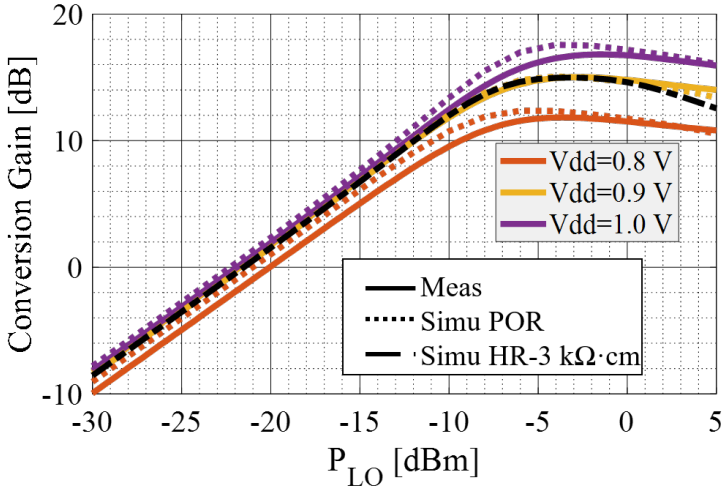


Figure 4.31: Measured and simulated conversion gain versus LO power. P_{RF} = -30 dBm, f_{RF} = 28 GHz, f_{LO} = 21 GHz, f_{IF} = 7 GHz. The black dashed curve is the simulation of the mixer in medium power mode atop of HR substrate without PSC.

The black curve[9], representing the simulation of the same mixer on an HR substrate, closely mirrors the performance observed with the POR substrate, indicating that the substrate has a very minor impact on the mixer's performance. The gain reaches its peak between -6 and 0 dBm of LO power. However, a slight decrease in gain is observed at P_{LO} = 5 dBm for the HR-3k substrate,

[9] In the next figures, the back dashed curves refers always for a simulation of the mixer atop of HR substrate without PSC effect

while the gain for the POR substrate tends to remain flat.

It is possible to adjust the RF mixer performance through the power supply, this has been summarized in Table 4.6. Three modes could be considered, low power mode with 17 mW power consumption, medium power with 30 mW and high power with 41 mW. This table illustrates the trade-offs between power consumption and conversion gain in the RF mixer.

Table 4.6: The three operational modes of the mixer are described in terms of their respective gain characteristics.

	Power [mW]	Max CG [dB]	Vdd [V]	V_{DC-RF} [V]
Low Power	17	11.8	0.8	0.36
Medium Power	29	15	0.9	0.4
High Power	41	16	1	0.42

Conversion Gain With Respect to the RF Power

By selecting P_{LO}=-2 dBm as the operating drive level for the mixer, the LO power is fixed to ensure that the mixer operates at its maximum conversion gain. This specific LO power level is chosen to provide the highest possible gain without overdriving the mixer. Once the LO power is set, the input RF power P_{RF} will be swept to measure the compression point of the mixer, as demonstrated in Figure 4.32. The compression point, which indicates the RF input level at which the mixer's gain begins to compress, will be determined through this process.

Measurements are in good agreement with simulations across the three operating modes of the designed mixer. The conversion gain was plotted as a function of RF power, ranging from -30 dBm to -7 dBm, at an LO power of -2 dBm. The results indicate that, for the three modes, the gain remains stable at 17 dB, 15 dB, and 11.7 dB for power supply voltages of 1V, 0.9V, and 0.8V, respectively. This consistent gain is maintained up to around P_{RF}=-13.5 dBm , which marks the 1 dB compression point. The 1 dB compression point indicates the RF input power level at which the gain starts to drop by 1 dB, signaling the

onset of nonlinear behavior in the mixer.

The mixer simulated on the HR-3k substrate shows results closely matching those of the mixer built on the POR substrate.

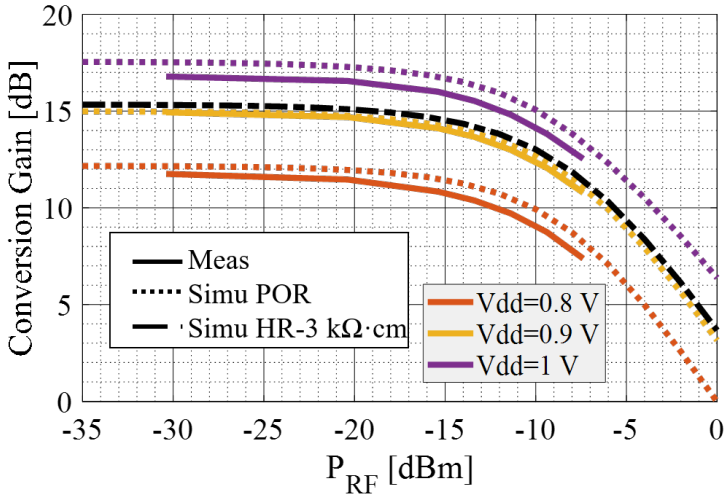


Figure 4.32: Measured and simulated conversion gain versus RF signal power. f_{RF} = 28 GHz, P_{LO} = -2 dBm, f_{LO} = 21 GHz. The black dashed curve is the simulation of the mixer in medium power mode atop of HR substrate without PSC.

Conversion Gain With Respect to the RF Frequency

By selecting P_{LO}=-2 and P_{RF}=-30 dBm, the bandwidth of the RF frequency response of the mixer can be observed. **Figure 4.33** illustrates the measured conversion gain as a function of the RF frequency, ranging from 24 GHz to 31 GHz. The measurements align closely with the simulation results, demonstrating that the 3-dB bandwidth for the three operating points of the mixer is approximately 26.5 GHz to 29.5 GHz.

It should be noted that the Gaussian shape of the curves is likely attributed to impedance matching rather than to losses from other sources. The mixer rejects the power at 24 GHz because the circuit is not optimally matched at 24 GHz, unlike at 28 GHz where proper matching allows for better power transfer.

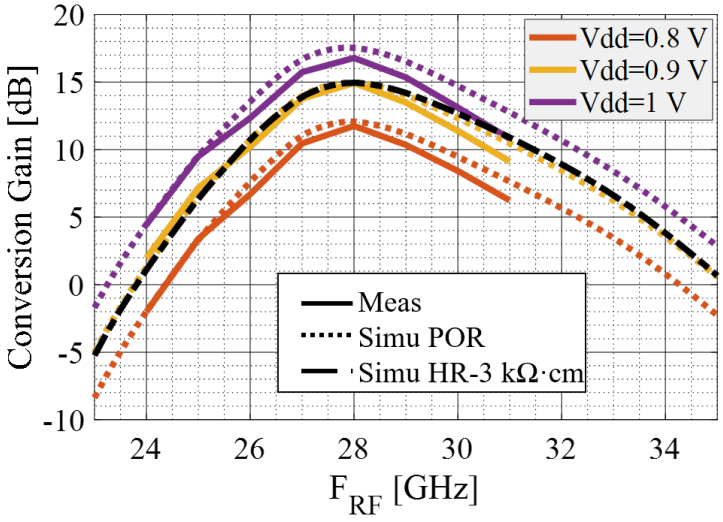


Figure 4.33: Measured and simulated conversion gain versus RF signal frequency. P_{RF} = -30 dBm, P_{LO} = -2 dBm, f_{LO} = 21 GHz. The black dashed curve is the simulation of the mixer in medium power mode atop of HR substrate without PSC.

Moreover, this behavior suggests that the matching network is optimized at around 28 GHz frequency range, which correlates well with **Figure 4.30**.

Simulation of the IP3 as a function of the LO power

In **Figure 4.34**, the simulated IP3 point is illustrated, with the input IP3 (IIP3) shown on the left and the output IP3 (OIP3) on the right, plotted against the input LO power at a fixed RF power of -30 dBm (at 28 GHz) for the three operating modes. It is shown that at P_{LO} = -2 dBm, the coordinates of the IP3 point for the medium power mode are (IIP3 = -3 dBm, OIP3 = 12 dBm). This value is considered low, as referenced in **Table 4.9**, and could be improved by adjusting the operating point of the mixer towards P_{LO} = 3 dBm. At P_{LO} = 3 dBm, an IIP3 value of approximately 9 dBm is achieved. However, this adjustment would result in increased RF power consumption and a slight reduction in conversion gain by about 1 dB. Additionally, if a highly linear mixer is required, an IIP3 of 17 dBm can be attained by increasing the DC supply to 1 V (41 mW) and the LO power to 5 dBm.

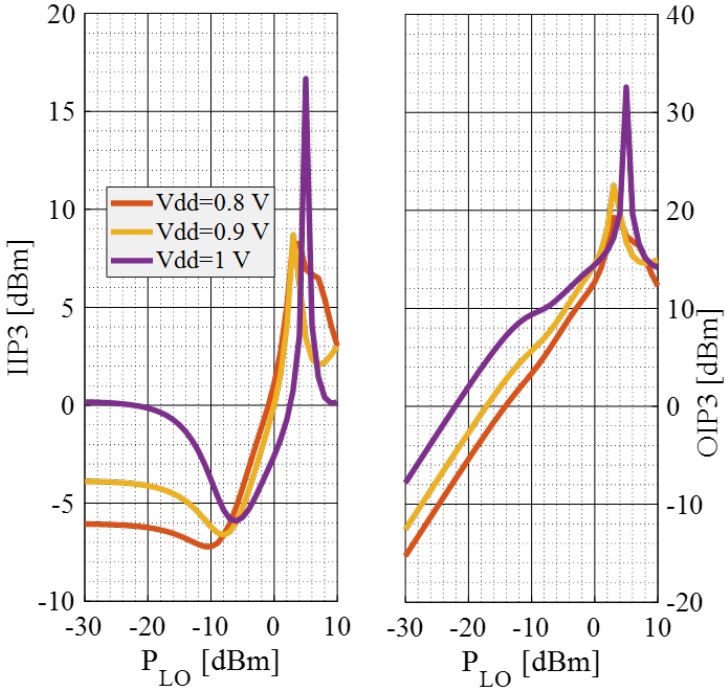


Figure 4.34: Simulated Intercept Point coordinates (on POR substrate) as a function of the LO power, Input IP3 on the left and Output IP3 on the right, P_{RF} = -30 dBm, f_{RF} = 28 GHz.

Typically, signals above 0 dBm are considered large signals. To generate such a large signal and achieve the desired high linearity, an integrated medium power amplifier (like in **[170, 171]** for example) circuit would be required at the input of the LO port of this mixer. This amplifier would ensure that the mixer operates at P_{LO} = 5 dBm (or higher) which enables to take benefit from the highly linear option.

Simulation of the Noise Figure as a Function of Frequency

Figure 4.35 illustrates the simulated noise figure of the designed mixer as a function of the IF frequency, using P_{LO} = -2 dBm and P_{RF} = -30 dBm. The mixer, across its three operating modes, demonstrates similar noise figure

performance. Additionally, in the IF range between 5.5 and 8.5 GHz—which corresponds to an RF range of 26.5 to 29.5 GHz, where the highest gain is observed in Figure 4.33—the noise figure remains below 9.5 dB. Specifically, at an IF of 7 GHz, the noise figure reaches 8.5 dB in the medium power mode, which is considered low for state-of-the-art RF mixers, as referenced in Table 4.9.

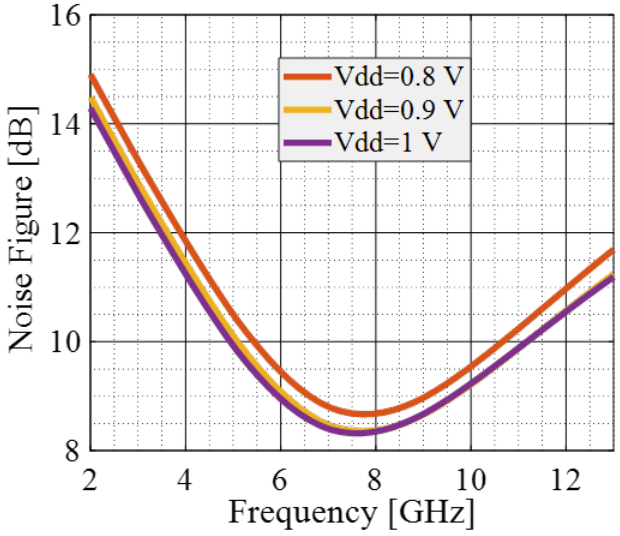


Figure 4.35: Simulated of the Noise Figure (on POR substrate) as a function of the IF frequency at P_{LO} = -2 dBm and P_{RF} = -30 dBm.

Simulation of the Feedthrough Between the Ports

The unwanted coupling of frequencies from one port to another, known as feedthrough, specifically from LO to IF and from LO to RF, is summarized in Table 4.7.

In other words, the LO to RF feedthrough refers to how much of the LO power leaks into the RF port, potentially mixing those frequencies. The primary objective is to minimize this feedthrough to the lowest possible level. As shown in Table 4.7, the LO to RF feedthrough is simulated at -66 dB, while the LO to IF feedthrough is measured at -55 dB across the three operating modes.

Table 4.7: Feedthrough from large signal LO port to either RF or IF ports for P_{LO} = -2 dBm, P_{RF} = -30 dBm on POR substrate.

	LO to RF [dB]	LO to IF [dB]
Low Power	-66	-56
Medium Power	-67	-55
High Power	-66	-55

Figure 4.36 presents the RF to LO feedthrough on the left and the RF to IF feedthrough on the right. The curves for the three operating modes of the mixer are shown to be quite close. The RF to LO feedthrough remains below -60 dB, while the RF to IF feedthrough is approximately 10 dB higher.

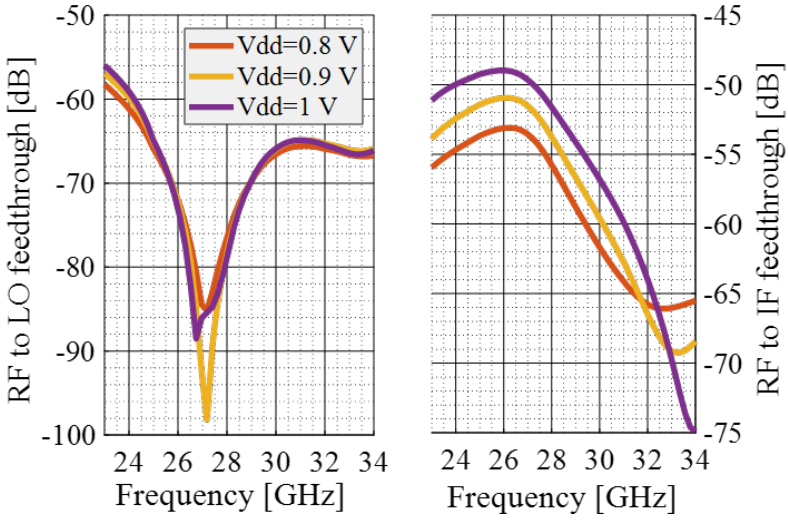


Figure 4.36: Simulated feedthrough from RF to LO port on the left, and simulated RF to IF feedthrough on the right.

4.3.11 Concept of Dual-Gate Excitation

In this part, a 28 GHz to 7 GHz down-conversion (similar to the Gilbert-cell) mixer was designed, fabricated and measured using GlobalFoundries' 22FDX® technology. This node offers advanced fully-depleted (FD) silicon-on-insulator (SOI) devices with ultra-thin body and BOX (UTBB) with back-gate terminal accesses. The mixer is based on a double-balanced topology, which offers excellent port isolation, and includes active loads and a transimpedance amplifier stage, that contribute to improving mixer conversion gain and linearity, respectively. The major novelty in the proposed circuit is the use of the back-gate as an analog input terminal to which the LO signal is injected.

It is important to highlight that a previous physical study was conducted using Multiple Independent Gate FinFETs (MIGFETs), where a physical model was developed in Spice3, as reported in [172, 173]. However, this study was limited to simulations of a double-balanced mixer with a resistive load, operating at an RF frequency of 1.8 GHz and an LO frequency of 1.6 GHz. Additionally, only transient simulations and the input and output spectra were provided to demonstrate the mixing function.

In this thesis, this technique has been extended to an industrial, commercially available technology 22FDX®, utilizing a model of an industrial MOSFET. The work has been expanded to function at higher frequencies, specifically at an RF frequency of 28 GHz and an LO frequency of 21 GHz. Moreover, a full characterization of the mixer has been performed, including both on wafer measurements and simulations, to thoroughly evaluate its performance and comparison to the state o the art CMOS RF mixers.

A double-gate excited device is illustrated in Figure 4.37, configured in a common-source loaded with a resistor R at the drain. This configuration is fundamental yet powerful for understanding the mixing behavior of signals applied to both gates V_{RF} and V_{LO}. The interaction between these two signals within the transistor, particularly through its non-linear characteristics, is what facilitates the mixing process. In this setup, the FET operates in a non-linear region where the superposition of the RF and LO signals leads to the generation of wanted harmonics. These products are the mixed frequencies, typically the sum and difference of the RF and LO frequencies, which are the desired outputs in a mixer.

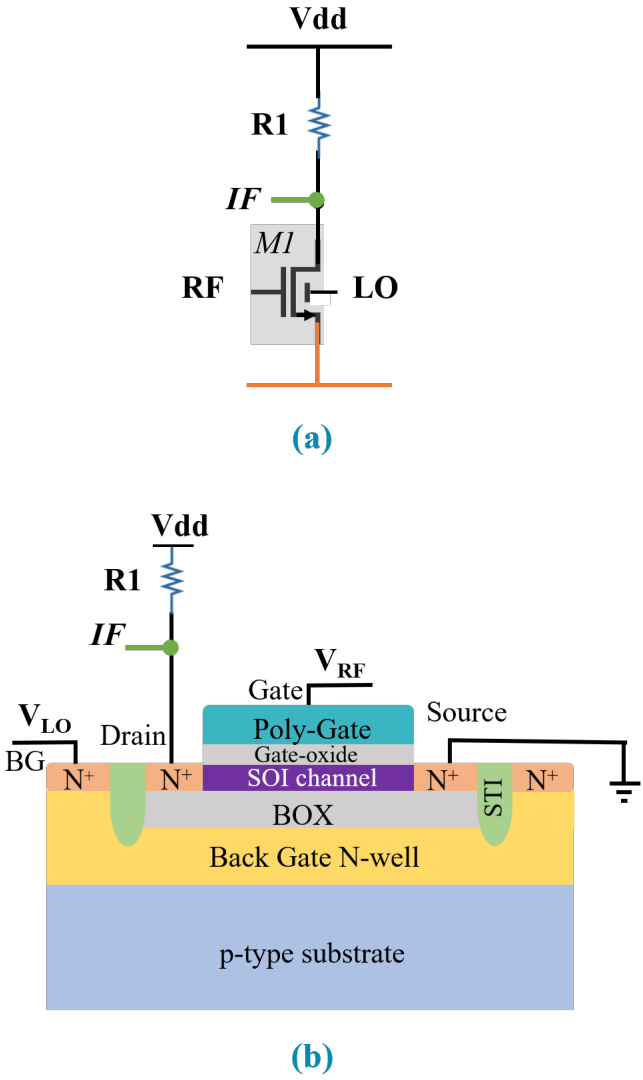


Figure 4.37: Basic mixing cell with dual-gate excitation: **(a)** shows the schematic diagram of the mixing cell, and **(b)** presents the cross-sectional view of an SLVT-NFET UTBB FDSOI device.

For this simple branch circuit, we can write the following equation for the

drain current:

$$I_{ds} = \frac{V_{dd} - V_{ds}}{R} = \frac{V_{dd} - V_{IF}}{R} \tag{4.41}$$

Considering the time-varying RF signal terms, we write:

$$i_{ds} = -\frac{v_{ds}}{R} = -\frac{v_{IF}}{R} \tag{4.42}$$

Neglecting parasitic elements, the FET's RF drain current can be written as:

$$i_{ds} = \frac{\partial^2 i_{ds}}{\partial v_{gs} \partial v_{bgs}} \cdot v_{gs} \cdot v_{bgs} + g_{mb} \cdot v_{bgs} \tag{4.43}$$

Where g_{mb} represents the transconductance due to v_{bgs} and $\frac{\partial^2 i_{ds}}{\partial v_{gs} \partial v_{bgs}}$ represents the variation of the current i_{ds} when modulated by both v_{gs} and v_{bgs} (g_m represents the transconductance due to v_{gs}).

We can write then:

$$i_{ds} = \frac{\partial^2 i_{ds}}{\partial v_{RF} \partial v_{LO}} \cdot v_{RF} \cdot v_{LO} + g_{mb} \cdot v_{LO} \tag{4.44}$$

In our case, to implement a mixer, a large-amplitude LO signal will excite the device's back-gate so that it strongly modulates the FET's characteristics (g_m) in time with the LO signal. The device's threshold voltage will then be pulsed in time with $v_{LO}(t)$. The g_{mb} term is not considered to be dependent on $v_{RF}(t)$ for our application, since the RF signal at the front-gate is considered to be of infinitesimally small-amplitude. Combining **Equation 4.42** and **Equation 4.44** we can then write:

$$v_{IF} = -R \cdot \frac{\partial^2 I_{ds}}{\partial v_{RF} \partial v_{LO}} \cdot v_{LO} \cdot v_{RF} - R \cdot g_{mb} \cdot v_{LO} \tag{4.45}$$

The second term on the right-hand side of **Equation 4.45** is a signal term at a frequency of f_{LO} (it is usually undesirable at the IF port, and can be avoided

using a double-balanced topology, that shall be considered for the full mixer).

The first term however is a multiplication of a term at frequency f_{RF} (voltage v_{RF}) by a term at frequency f_{LO} (the term $g_m(f_{LO})$). It then contains a spectrum of frequencies described by: $f_{RF} + k \cdot f_{LO}$. Where k can take a value of either -1 or +1.

In this work, we wish to use such a mixing principle to design a down-converter, and we are then specifically interested in the signal component of v_{IF} at the frequency of $f_{RF} - f_{LO}$ which is the case for k = -1.

The conversion gain of a mixer is defined as the amplitude of the IF signal relative to the RF input's amplitude at a given LO input power. It will then be proportional to the first term of the right-hand side of **Equation 4.45**, so we can write:

$$CG = \frac{v_{IF}}{v_{RF}} \propto R \cdot g_m(v_{LO}) \tag{4.46}$$

The CG in **Equation 4.46**[10] is then maximized by appropriately biasing the device's front gate (FG) and back gate (BG). The device is carefully biased to set the optimal operating point, ensuring that both gates contribute effectively to the mixing process. Additionally, the appropriate v_{LO} signal is provided, with the correct amplitude and phase, to achieve the desired mixing efficiency.

After demonstrating that the mixing effect can be achieved using a single FET, the next subsection will explore how the biasing of the front and back-gate is selected to optimize performance.

[10] The conversion gain is given in [172] by:

$$CG = \frac{1}{\pi} \cdot g_m \cdot R_L$$

Which is close to our detailed equations.

4.3.12 Biasing of the Mixing FET

Single FET simulations were performed using the PDK models of mmWave SLVT transistors in order to maximize this $g_m(v_{LO})$ term towards achieving high mixer conversion gain. The results are given in **Figure 4.38**, that plots the device front-gate transconductance g_m for various front- and back-gate DC biasing conditions, for a Vds fixed to 0.5 V.

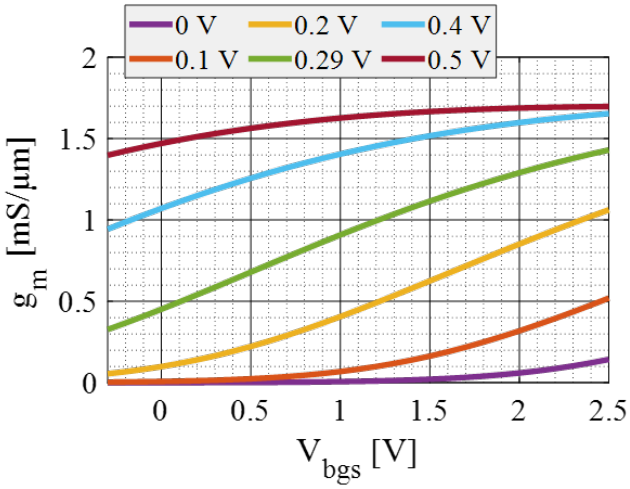


Figure 4.38: g_m of the front-gate vs back-gate voltage for multiple front-gate biases, at Vds = 0.5 V.

The back-gate voltage is biased within the range of -0.3 V to +2.0 V. Setting the DC back-gate bias near +1.0 V allows for the greatest possible swing in the applied v_{LO} signal. This optimal biasing maximizes the modulation of the FET's behavior by enabling the LO signal to fully drive the device. The front-gate DC bias should then be carefully selected such that the device's current and g_m are strongly modulated by the LO signal at the back-gate. The curves of **Figure 4.38** show that a front-gate DC bias close to 0.29 V results in the $g_m(V_{bg})$ function with the strongest slope over the -0.3 V to +2.0 V range.

The analysis shown in **Figure 4.38** is performed at a Vds of 0.5 V. Similar analysis was performed at other Vds bias points. Overall, 0.5 V is chosen, as it is a good compromise between $g_m(V_{bg})$ sensitivity and DC power consumption. For these reasons, we set the DC operating points of each double-gate excited

FET of the mixer topology to Vds = 0.5 V, Vgs = 0.29 V and Vbg = 1.0 V.

A double-balanced differential topology, shown in **Figure 4.39**, is chosen towards high port isolation between one-another. In this topology, the v_{IF+} and v_{IF-} signals do not contain any term proportional to $g_{mb} \cdot v_{LO}$, though that is the case in single-balanced or single-branch topologies (see second term in **Equation 4.45**). In the double-balanced circuit, a virtual ground is then enforced at the LO frequency at nodes IF+ and IF- by circuit's symmetrical design, resulting in very high isolation of the IF port from the LO signal (which can be of substantially higher power than the RF and IF signals).

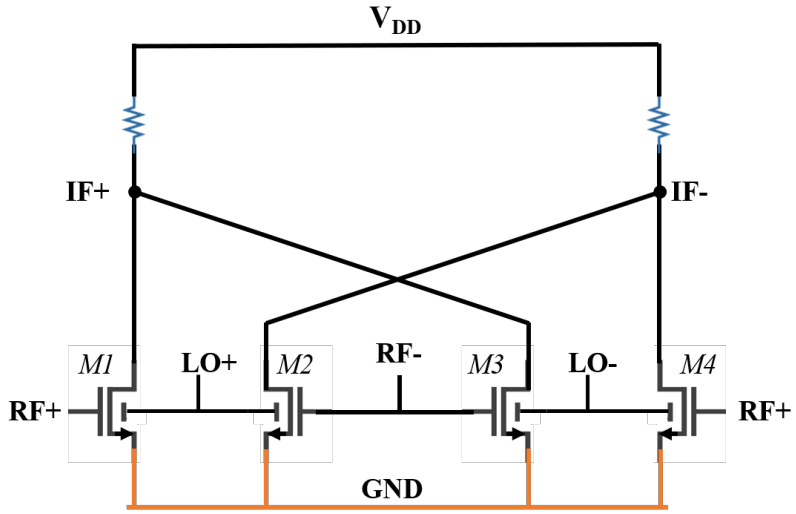


Figure 4.39: Double-balanced mixer back-gate topology, fully differential at all three ports with a basic resistive load.

In this topology, the conversion gain remains proportional to the sensitivity of the device's transconductance to the back-gate excitation signal, $g_m(v_{bg})$, as indicated by the first term of **Equation 4.45**.

4.3.13 Back Gate Topology: Circuit Design

Figure 4.40 shows a detailed schematic of the double balanced back gate topology mixer with an input RF signal frequency at 28 GHz, LO frequency at 21 GHz and IF frequency at 7 GHz. All the transistors have a gate length of 20 nm

that length demonstrates a good trade-off between high RF performance and reliability. A relaxed contact poly-pitch is used (CPP×2), which increases ft and fmax, reduces the source and drain extrinsic resistances, this is used for all FETs in this design. The mixing stage formed by the SLVT-NFETs M1, M2, M3, and M4 are handling the differential RF and LO inputs with a total width of 37.5 µm and 30 fingers with 1.25 µm each finer. The biasing of the front gate and back gate are used as demonstrated in **Section 4.3.12**.

The active load consists of R1 resistors, each with a value of 5 kΩ, fabricated in polysilicon. The pMOSFETs M5 and M6 were designed with a total width of 72.5 µm, distributed across 58 fingers, with each finger having a width of 1.25 µm. These dimensions were carefully selected in such a way to get 0.5 V DC bias points at the nodes Y1 and Y2 (see **Section 4.3.12**).

The transimpedance amplifier is constructed using a 200 Ω resistor, specifically an unsilicided N+ diffusion resistor within the SOI, chosen for its low inductance and validated high-frequency performance. To achieve the desired resistance while minimizing reactance, the resistor was designed with a minimum width of 360 nm, as reducing the width for a fixed resistance value also reduces the length, thereby limiting the increase in reactance associated with larger dimensions. The pFETs M7 and M9 are designed with a total width of 75 µm, distributed across 55 fingers with each finger being 1.36 µm wide. Similarly, the nFETs M8 and M10 have a total width of 72.5 µm, divided into 58 fingers, with each finger having a width of 1.25 µm.

The generation of differential signals RF+, RF-, LO+, LO-, IF+ and IF- is accomplished through the use of integrated baluns, specifically designed to operate at each corresponding frequency. Interleaved baluns are utilized, which are placed on a single metal layer just below the final metal layer. This placement was chosen to maximize the distance from the substrate, thereby reducing substrate parasitic effects.

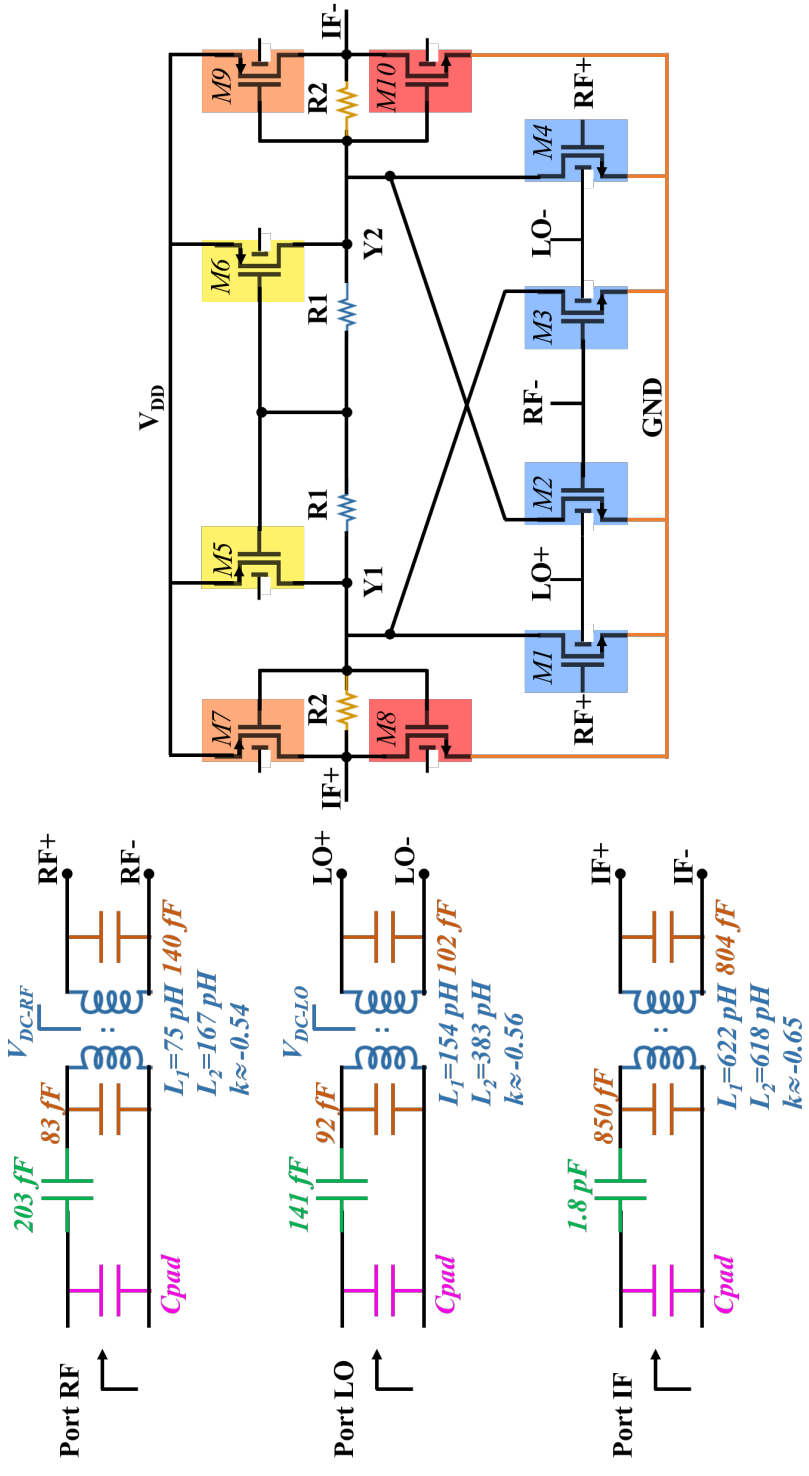


Figure 4.40: Schematic diagram of the back-gate topology down-conversion mixer using an active load and a transimpedance amplifier. The baluns at 3 different frequencies are also shown. Design made for a POR substrate.

At the RF port, the interleaved balun consists of inductors L1= 75 pH, L2=167 pH with a coupling factor k=0.54. This configuration is optimized to convert the RF signal from a single-ended input to a differential output, ensuring proper impedance matching for the RF signal. The bias voltage V_{DC-RF} is set to 290 mV. Capacitors of 203 fF, 83 fF, and 140 fF are employed to compensate for the inductive reactance, allowing the overall impedance to be tuned to 28 GHz on the Smith chart.

At the LO port, the interleaved balun is consisting of inductors L1=154 pH and L2= 383 pH , with a bias voltage V_{DC-RF}= 1 V. The primary objective was to determine the optimal capacitances that would effectively compensate for the inductive reactance, thereby centering the impedance on the Smith chart at 21 GHz. This was accomplished by using shunt capacitors to balance the inductive components precisely.

At the IF port, the interleaved balun is configured with inductors L1=622 pH and L2=618 pH, featuring a coupling factor k=0.61. This specific configuration is designed to accommodate the relatively low frequency of 7 GHz, which necessitates larger inductor values compared to those used at the RF and LO ports. To effectively convert the differential signal, which is out of phase, from the double-balanced mixer into a single-ended output, capacitors with values of 850 fF, 1.8 pF, and 804 fF are employed. These capacitors are carefully selected to ensure proper phase alignment and efficient signal conversion.

4.3.14 Back Gate Topology Mixer Measurements

In this section, both the small-signal and large-signal measurements of the designed back-gate topology mixer will be presented and thoroughly discussed, with corresponding simulations performed for each figure of merit. The small-signal measurements will be focused on the evaluation of the S-parameters of each port and the assessment of impedance matching across the intended frequency range. Meanwhile, the large-signal measurements will explore the mixer's performance under higher LO power conditions. Simulations will be conducted alongside these measurements to provide a comprehensive comparison and validate the mixer's performance metrics.

S-Parameters Matching

Figure 4.41 presents a photograph of a designed down-conversion mixer, showcasing the key components and areas within the layout that is quite similar to the Gilbert cell mixer designed in **Figure 4.29**. At the heart of the design is the core area, which is highlighted in red and labeled as the core area. The design incorporates three baluns, each serving a specific purpose within the mixer. The first balun, operating at 7 GHz, is positioned near the top center of the layout and is connected to the IF output. The second balun, designed for 28 GHz, is located towards the center-left, adjacent to the RF input. The third balun, operating at 21 GHz, is found towards the center-right, near the LO input. These baluns play a critical role in the conversion of signals within the mixer.

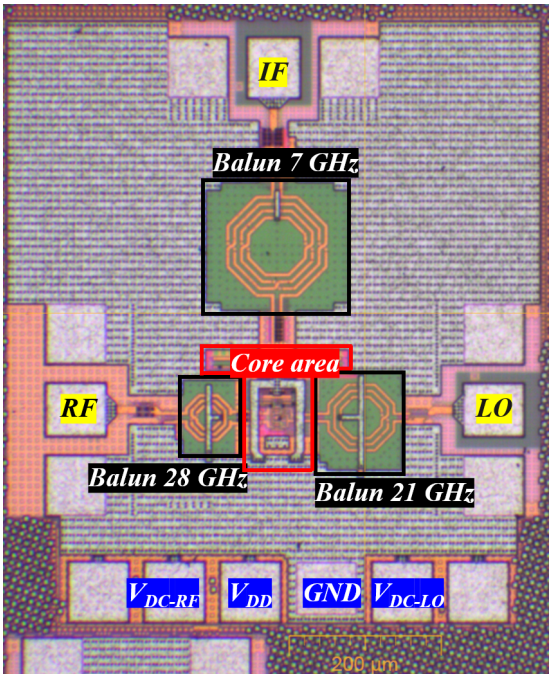


Figure 4.41: Photograph of the designed down-conversion mixer. The total area, including the baluns and excluding the pads is 0.150 mm². The core active area (highlighted in blue) is 0.008 mm².

At the bottom of the layout, several pads are visible, labeled as V_{DC-RF}, V_{DC-LO} and V_{DD} used to bias the mixer.

S-parameters measurements are calibrated with a Short-Open-Load-Thru calibration performed on an impedance standard substrate to move the reference plane at the probe tips. The measured S-parameters plotted in **Figure 4.42** demonstrate that the mixer is well matched at the LO port at 21 GHz, at the RF port from 25 to 29 GHz, and at the IF port from 5.5 to 8.5 GHz.

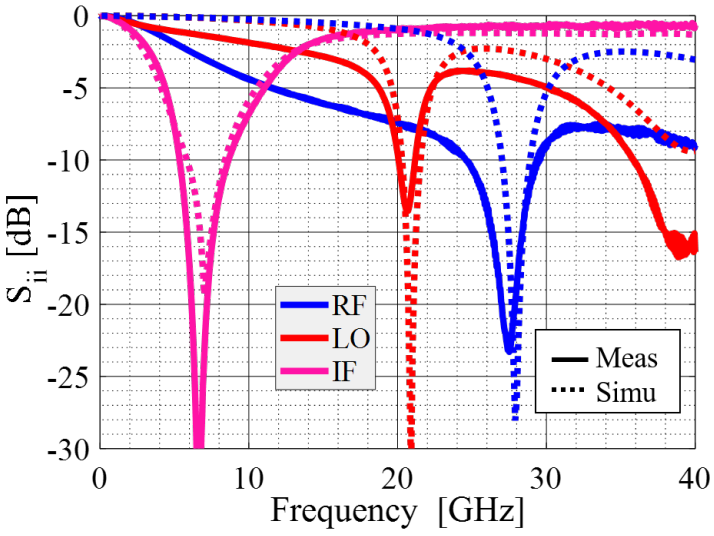


Figure 4.42: Measured and simulated reflection coefficients for each port of the back-gate topology mixer, evaluating the circuit's matching performance on the POR substrate.

Large-signal measurements were carried out to determine the mixer's FoMs. The process began with calibrating the PNA's power to the probe tips. An RF signal at -30 dBm and 28 GHz was then applied to the mixer's input. Following this, the LO signal at 21 GHz was subjected to a power sweep using a separate source from the VNA, while the IF port was connected to one of the VNA's receivers.

Conversion Gain as a Function of the LO Power

Figure 4.43 illustrates the measured and simulated conversion gain as a function of LO power P_{LO}, with the RF input power set to -30 dBm. Simulations agree

well with measurements below 10 dBm. At low LO power, the power applied to the back-gate of the FETs ensures they operate correctly within their linear region, effectively switching between the ON and OFF states. Consequently, the gain increases proportionally with the LO power. At P_{LO}=10 dBm, the conversion gain reaches its maximum, At this maximum, the LO power is at an optimal level that fully switches the mixer without pushing it to the saturation. At this stage, the mixer is functioning at its peak performance, with all components working in harmony to achieve maximum gain of around 3.5 dB.

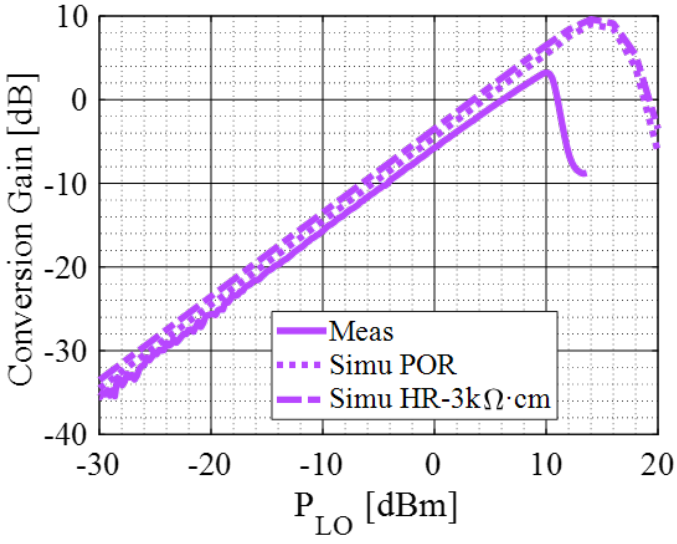


Figure 4.43: Measured (on POR substrate) and simulated conversion gain versus LO power for the back-gate topology mixer. P_{RF} = -30 dBm, f_{RF} = 28 GHz, f_{LO} = 21 GHz, f_{IF} = 7 GHz.

However, a discrepancy is observed between the measurements and simulations within the P_{LO}=10 and P_{LO}=14 dBm. This deviation may be attributed to the modeling of the back-gate under high power conditions. It is crucial to note that the back-gate is typically recommended for use as a DC input, primarily to adjust the threshold voltage of the FETs [30, 174–176]. In this study, however, an RF signal was applied to the back-gate, which may have introduced complexities that are not fully captured by the existing RF or high

power models. The observed mismatch between the measured and simulated data could thus stem from inaccuracies in the RF modeling of the back-gate or from the limitations of the high power modeling in this context. This issue remains under investigation by the research group, as further analysis is needed to fully understand the underlying causes.

Conversion Gain as a Function of the RF Power

Figure 4.44 illustrates the measured and simulated conversion gain as a function of the RF power P_{RF}, a at two different LO power levels: P_{LO}=10 dBm where the mixer achieves its maximum gain, and P_{LO}=-2 dBm, for comparison with the Gilbert cell topology.

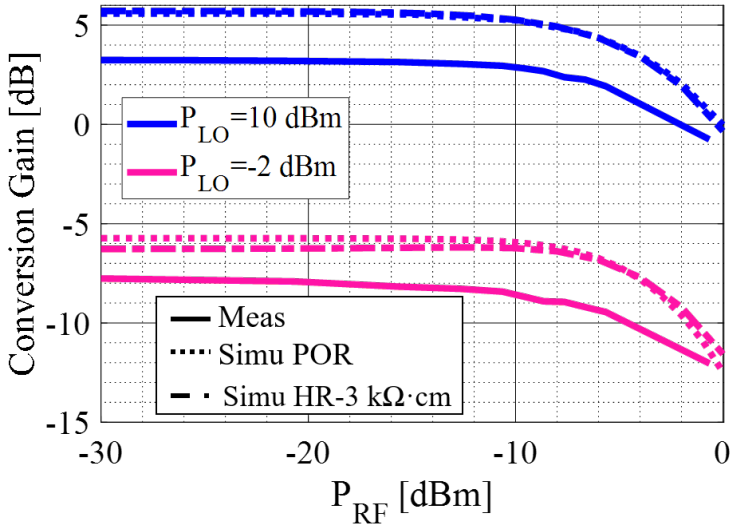


Figure 4.44: Measured and simulated conversion gain versus RF signal power. f_{RF} = 28 GHz, P_{LO} = 10 dBm or P_{LO} = -2 dBm, f_{LO} = 21 GHz.

In both driving LO power, the value of the 1 dB compression is reached approximately at P_{RF}=-6 dBm which is 6 to 7 dB better than Gilbert cell topology. However, as shown in Figure 4.44 the gain at P_{LO}=-2 is -7 dBm, which is 22 dB lower than the Gilbert cell topology at medium power configuration.

Conversion Gain as a Function of the RF Frequency

Figure 4.45 illustrates the measured and simulated conversion gain versus the frequency of the RF a P_{RF}=-30 dBm and LO power P_{LO}= 10 dBm and P_{LO}= -2 dBm. The gain at both LO power levels is not flat, as the mixer is optimized for matching around 28 GHz. Additionally, the 3-dB bandwidth in both cases ranges from 27 to 30 GHz.

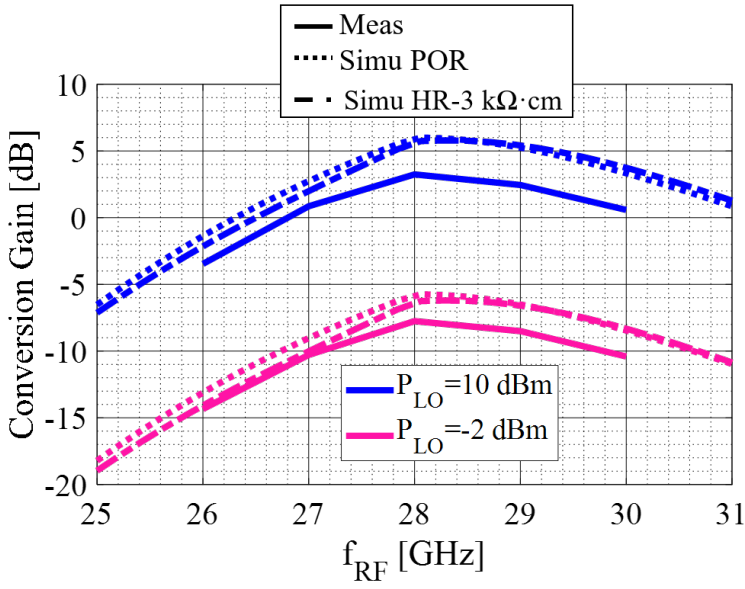


Figure 4.45: Measured and simulated conversion gain versus RF signal power. f_{RF} = 28 GHz, P_{LO} = -2 dBm and P_{LO} = 10 dBm, f_{LO} = 21 GHz.

Simulation of the IP3 as a function of the LO power

In **Figure 4.46**, the simulated IP3 point is illustrated, with the input IP3 (IIP3) shown on the left and the output IP3 (OIP3) on the right, plotted against the input LO power at a fixed RF power of -30 dBm (at 28 GHz). At P_{LO}= 10 dBm an IIP3 of 15 dBm is reached which is a high value compared to the state of the art RF mixers around 28 GHz. At this point an OIP3 =14 dBm is reached. The IIP3 value will decrease when decreasing the value of the LO driving power to P_{LO}= -2 dBm where 5 dBm is reached. This value is 4 dB better than the Gilbert cell topology (see **Figure 4.34**).

On the other hand, if a highly linear mixer is required (IIP3 > 15dBm), , it can be achieved using the Gilbert cell topology at P_{LO}= 5 in high power mode (Vdd= 1 V). However, this approach results in significant DC power consumption, around 41 mW. In contrast, the back-gate topology, while consuming higher LO power at P_{LO}=10 dBm, offers lower DC power consumption at 26 mW. These trade-offs highlight that the specifications of the mixer are heavily dependent on the design of the LNA, underscoring the point previously discussed in **Section 4.3.1**.

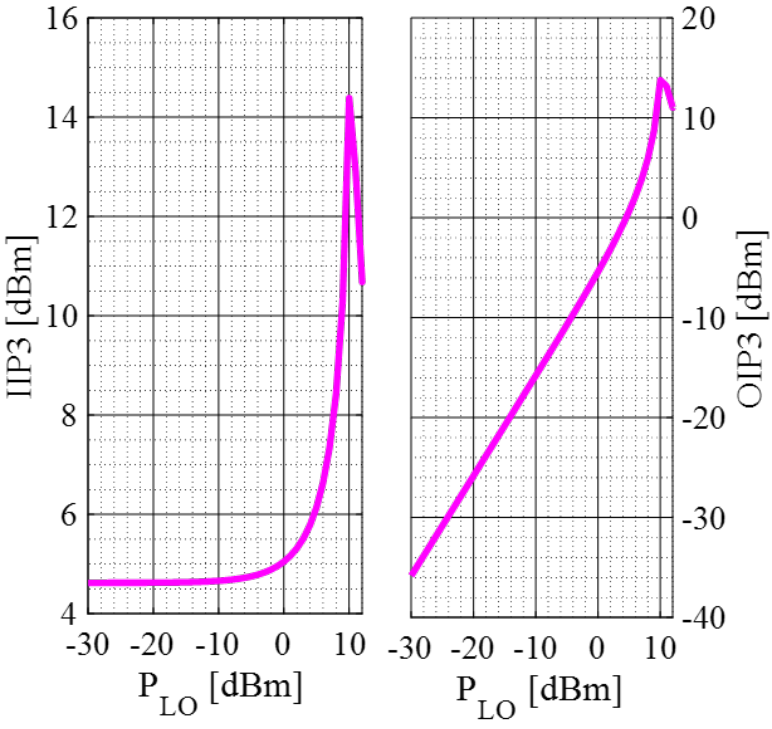


Figure 4.46: Simulated Intercept Point coordinates as a function of the LO power for the back-gate topology mixer, Input IP3 on the left and Output IP3 on the right, P_{RF} = -30 dBm, f_{RF} = 28 GHz.

Simulation of the Noise Figure as a Function of Frequency

Figure 4.47 illustrates the simulated noise figure of the designed mixer as a function of the IF frequency, using P_{LO} = -2 dBm and P_{LO} = 10 dBm. The results clearly show that at P_{LO} = -2 dBm, the worst noise figure achieved is 25 dB, which is 10 dB worse than when P_{LO} = 10 dBm.

It is important to note that in **[177]** (designed in 130-nm SiGe BICMOS technology at similar frequencies), a noise figure of 23 dB was achieved with -12 dB gain but with P1dB=6 dBm. On the other hand, the Gilbert-cell topology shows a noise figure around 8 dB, which is 17 dB better than the back-gate topology at the same P_{LO} = -2 dBm.

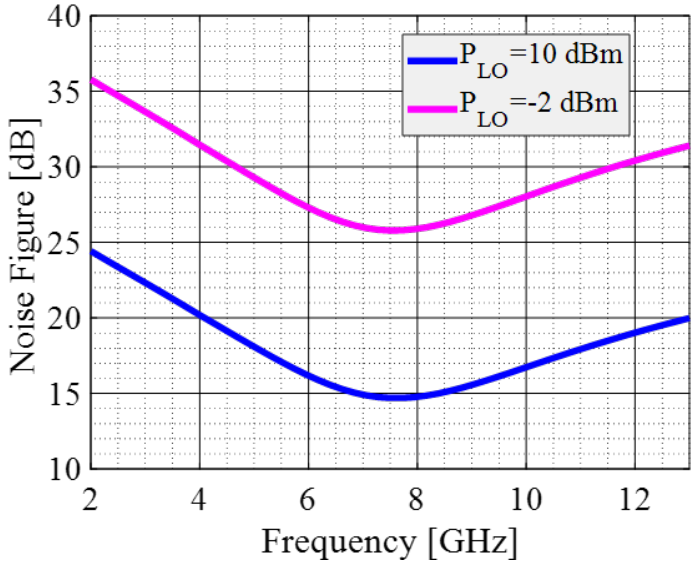


Figure 4.47: Simulated of the Noise Figure as a function of the IF frequency at P_{LO} = -2 dBm and P_{LO} = 10 dBm for same P_{RF} = -30 dBm.

Simulation of the Feedthrough Between the Ports

The feedthrough from LO to RF and IF ports are summarized in **Table 4.8** for both P_{LO} powers. The feedthrough LO-IF for the back-gate topology is 50 dB, which is 6 dB higher than the Gilbert cell topology.

Table 4.8: Feedthrough from large signal LO port to either RF or IF ports.

	LO to RF [dB]	LO to IF [dB]
P_{LO}=10 dBm	-47	-51
P_{LO}=-2 dBm	-46	-50

Moreover, the LO-RF feedthrough is 20 dB higher compared to the Gilbert cell topology. This could be explained by the fact that during the mixing process in the Gilbert cell, the LO signal is interrupted by the capacitances C_{gs2} and C_{dg1} (see **Figure 4.48(b)**), which help to reduce coupling.

In contrast, in the back-gate topology, the mixing occurs within the same channel, with both the LO and RF signals modulating the channel simultaneously (see **Figure 4.48(a)**). Since there are no capacitances present to mitigate the coupling, the mixing mechanism itself within the same FET leads to higher feedthrough[11].

The feedthrough is expected not to affect the circuit designs described in this thesis since the two frequencies 21 and 28 GHz are quite far compared when mixing is directly to the baseband. In that case for example the frequencies 28 and 27.9 GHz will be used. In that case, the feedthrough can affect the performance of the Mixer by mixing unwanted signal at 27.9 GHz with the wanted signal at 28 GHz.

[11] The feedthrough is not expected to significantly impact the circuit designs described in this thesis, as the two frequencies, 21 GHz and 28 GHz, are sufficiently far apart compared to scenarios where mixing occurs directly to the baseband. In such a case, for example, frequencies like 28 GHz and 27.9 GHz might be used. In that situation, the feedthrough could adversely affect the performance of the mixer by allowing an unwanted signal at 27.9 GHz to mix with the desired signal at 28 GHz.

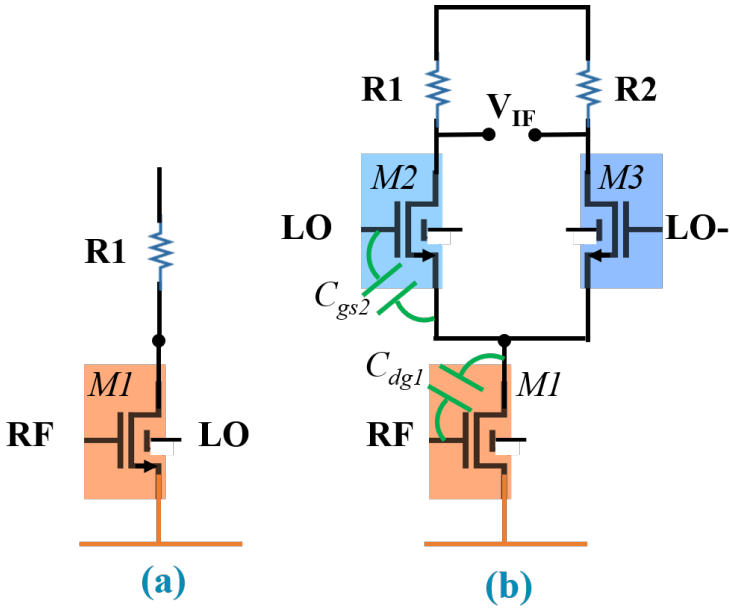


Figure 4.48: Schematic diagram showing that the mixing process in the case of the back-gate topology is happening in the same FET making the feedthrough higher **(a)** and the case where the mixing process is in different FETs, the feedthrough is reduced through C_{gs2} and C_{dg1} in **(b)**.

4.3.15 Discussion: Gilbert Cell Topology And Back-Gate Topology

In addition to demonstrating the mixing concept of the back-gate topology, the choice of the appropriate topology is heavily influenced by the design specifications and the LNA configuration. When comparing the two mixers separately, the Gilbert cell topology offers better feedthrough performance than the back-gate topology, primarily because, in the back-gate design, mixing occurs directly within the channel. In contrast, the Gilbert cell topology benefits from capacitors that effectively block unwanted signals. Furthermore, the Gilbert cell topology exhibits a lower noise figure compared to the back-gate topology, and it achieves this performance at lower LO power levels.

Moreover, the Gilbert cell topology demonstrates a conversion gain exceeding 12 dB, which remains stable across an LO power range from -4 to 5

dBm. In contrast, the back-gate topology achieves a maximum gain of only 3.5 dB. However, the back-gate topology exhibits an IIP3 that is higher or equal to 4.5 dBm over a wide P_{LO} range from -30 to 12 dBm, with notably stable IIP3 performance between -30 and 0 dBm. For applications requiring high linearity, the back-gate topology can achieve an IIP3 of 14 dBm with a DC power consumption of 26 mW at P_{LO}=10 dBm. In contrast an even higher IIP3 of 17 dBm can be reached using lower LO power P_{LO} with high power mode Gilbert cell topology while maintaining a high conversion gain of 16 dB, though at an increased DC power consumption of 41 mW. The Gilbert cell mixer designed in this thesis, with some adaptations, could potentially meet the specifications required for the transceiver designed in [178] used in mobile communications. It has been specified that the required conversion gain for the mixer in RX mode is -7 dB, with a noise figure of 7.5 dB, and an IIP3 of 19 dBm.

4.3.16 Benchmarking

Table 4.9 provides a comprehensive comparison of various state-of-the-art down-conversion mixers operating close to 28 GHz compared to the designed mixers back-gate topology and improved topology of the Gilbert cell. The two mixers designed in this thesis utilizes 22FDX® technology, one of the most advanced semiconductor processes available in the market (2024). This technology is known for its high performance and power efficiency, placing our design at a distinct advantage compared to other designs.

In terms of gain, the Gilbert cell topology (GCT) achieves a conversion gain of 15 dB. This is a strong performance metric compared to other works. Although some other designs, such as the one cited in [179], achieve higher gains of up to 24.5 dB, our work gain still competitive and outperforms many designs that show lower or even negative gain values.

The NF of Gilbert cell is estimated to 8 dB, which is close to some of the lower-noise designs in the table. For example, the [179] design achieves a noise figure as low as 7.8 dB and [167] achieving 7 dB, indicating superior performance in minimizing noise and maintaining signal integrity.

Regarding DC power consumption, the back-gate topology consumes 26 mW, positioning it as one of the more power-efficient designs in the table. This

is particularly notable when compared to designs like **[180]**, which consumes 390 mW.

While the back-gate topology requires the highest LO power at 10 dBm, the Gilbert cell demonstrates a significantly lower value of -2 dBm, which is the third lowest in the entire table. In terms of 1 dB compression, the back-gate is also linear, with a measured P1dB= -6 dBm compared to the Gilbert cell at P1dB= -13 dBm. Both of these values are around the midpoint of the table. Regarding IIP3, higher values such as those in **[181–183]** exceed 20 dBm. The back-gate topology follows, and the Gilbert cell topology is also capable of achieving up to 17 dBm of IIP3, depending on the LO power level used.

Table 4.9: State of the art active down conversion mixers operating close to 28 GHz.

Work	Technology	Gain [dB]	NF [dB]	f_{RF} [GHz]	f_{IF} [GHz]	P_{DC} [mW]	P_{LO} [dBm]	f_{LO} [GHz]	P1dB [dBm]	IIP3 [dBm]	Area [mm^2]
[177]	130 nm SiGe	-12.9	23.3	24-28	3	29.7	6	25	8.5	NA	2.94
[181]	180 nm CMOS	-4.5	NA	23-25	NA	16	5	NA	-5	23	0.72
[179]	180 nm CMOS	24	7.8	22-26	DC-1.7	35	0	24.6	-20	NA	0.39
[184]	90 nm CMOS	10	NA	21-27	NA	38.1	NA	NA	NA	-8.5	0.98
[182]	90 nm CMOS	-3.2	NA	23-30	DC-3.5	10	1	26.5	0	21	0.6
[168]	90 nm CMOS	0	16	20-50	0.1	6	0	NA	-1	9.5	0.48
[183]	45 nm SOI	-0.5	15.3	28	12	24	2	16	-0.2	20	0.78
[180]	45 RFSOI	-12	15	8-30	DC-8	390	0	NA	7	NA	0.85
[167]	22 nm FDSOI	12	7-12	25-31	DC-3	25	0	28	-14.8	NA	0.64
[185]	22 nm FDSOI	-2.6	NA	26.7-29	DC	38	-8	28	-2.5	NA	0.24
[186]	22 nm FDSOI	7.8	12-16	24-34	DC-4	1.28	-8	30	-7	4.8	0.24
This Work[1]	22 nm FDSOI	3.5	15*	26-30	5-9	26	10	21	-6	15*	0.55
This Work[2]	22 nm FDSOI	15	8*	27-30	6-9	30	-6 to -2	21	-13	-2*	0.59

This Work[1]: mixer with back gate topology. This Work[2]: mixer with conventional Gilbert cell topology,*: simulated.

4.4 Chapter Summary

In this chapter, several critical RFSOI circuits were designed using FDSOI technology on various high-resistivity substrates for the first time. The primary objective was to thoroughly investigate the impact of substrate properties on the performance of RFSOI front-end components. By leveraging different high-resistivity substrates, this work aimed to explore how variations in substrate characteristics, such as resistivity and parasitic effects, influence the overall performance, including parameters like linearity, efficiency, and power handling.

The substrate significantly influences the performance of the switch, particularly when the switch has a large surface area. This thesis demonstrates that switches with relatively smaller surface areas are less impacted by substrate effects, whereas those with larger areas are more susceptible. Upgrading from a POR substrate to HR substrate proves beneficial, as it increases the effective resistivity from 10 Ω·cm to approximately 100-200 Ω·cm—an order of magnitude improvement. Although HR substrates are prone to PSC effect, it has been shown that techniques such as field-effect passivation and the incorporation of PN junctions in the RF circuits can effectively mitigate these parasitics. Moreover, using an HR substrate reduces nonlinearities associated with the substrate, thereby enhancing the power handling capabilities of the stacked switch.

The power amplifier, a crucial circuit in the TX chain front-end, is significantly influenced by the substrate. In this thesis, a high-resistivity substrate, in addition to the POR substrate, was used, leading to several performance improvements. Specifically, the PAE increased by 5-7 % in the 30-40 GHz frequency range. The higher PAE results in less power being dissipated as heat in the substrate and more power being converted into useful RF output power. Additionally, a slight increase of 0.4-0.5 dB in output power at the point of maximum PAE was achieved with the HR substrate compared to the POR substrate. While these differences may seem modest, it is important to emphasize that changing the substrate from POR to HR in a front-end module impacts not just a single circuit but all circuits within the module. When all the circuits, including the switch, LNA, PA, and VCO, are placed on an HR substrate, the cumulative benefits across the entire system can be significant.

The RF mixers designed solely on POR substrates in 22FDX® technology were presented in this thesis, with no study conducted on substrate effects. It has been demonstrated that the back-gate of a FET can be used not only as a DC input but also as an RF input, allowing for channel modulation by a frequency different from that applied to the front gate. However, when comparing a conventional Gilbert cell mixer topology to the back-gate topology, several drawbacks of the back-gate approach were identified, including increased feedthrough, noise, and challenges in achieving high conversion gain. Due to the 25 nm thick BOX layer that separates the back-gate from the FET's channel, the maximum conversion gain in the back-gate topology was achieved only at an input power of 10 dBm applied to the back-gate. This 10 dBm input power is significant and typically requires the use of a power amplifier, which in turn increases power consumption in the front-end module.

In contrast to the back-gate topology, the conventional Gilbert cell architecture easily achieves high gain with an LO power around -2 dBm. Additionally, it has been shown that this topology can be utilized in various power consumption modes, offering flexibility depending on the application's requirements. High linearity is also achievable through careful control of the LO power. Furthermore, the Gilbert cell topology maintains a relatively low noise figure of 8.5 dB at 7 GHz, which is a favorable characteristic for mixers.

Overall, the substrate is not always the definitive factor for improving the RF performance of a given circuit. In this chapter, it is demonstrated that the substrate plays a crucial role in the case of RF switches, particularly in the series-shunt topology, where it can be considered a first-order element for enhancing circuit performance. This finding aligns with the fact that 100 % of RF switches in modern smartphones are implemented on trap-rich substrates, as seen in PDSOI technology.

Conversely, the substrate's influence can be less pronounced in other circuit types, as shown in the case of the power amplifier. Here, the substrate is considered a second-order factor, having a more moderate effect on the RF performance of the circuit. Beyond this, simulations presented in this thesis reveal that the substrate plays a minimal role in

in the performance of RF mixers, leading to the conclusion that the mixer topology studied here is substrate-independent. This highlights the need for a case-by-case evaluation of the substrate's impact, as its importance varies significantly depending on the specific circuit topology and application.



5. Conclusion and Perspectives

Conclusion

Summary

Throughout this thesis, several key aspects related to substrate technologies and their impact on RF circuit design are thoroughly examined from various perspectives.

First, the importance of accurate substrate characterization, and subsequently, the circuits built upon them, is pointed out. It has been demonstrated that reliable conclusions can only be drawn when precise measurement techniques are applied. Thanks to the advanced measurement methods found at UCLouvain, key tools such as the S-parameter small-signal setup and the harmonic distortion measurement setup were used to obtain important measurements. In addition to these measurements, the role of modeling and simulations has been shown to be an essential complement to experimental RF characterization, particularly for the quantification of traps in the polysilicon trap-rich layer. This modeling plays a complementary role alongside the PICTS measurements, highlighting the importance of using both measurement an simulations for comprehensive substrate analysis.

Second, several substrate types are analyzed beyond the conventional trap-rich, HR, and standard substrates. Innovative substrate solutions such as FE, PN junctions, and double-BOX substrates are presented as proofs of concept. These novel substrates are shown to have the potential to migrate from small-scale research settings (such as a 3-inch wafer in a basic clean-room) to commercially viable products. Moreover, alternative substrate solutions like Au-Si and porous silicon, which begin from highly doped starting materials, are presented as promising future technologies. The study of these substrates, enabled by accurate measurement and modeling techniques detailed in **Chapter 2**, provides a robust foundation for exploring new substrate solutions in RF applications.

In **Chapter 4**, several critical circuits within the front-end-module are designed and tested in sub-6 GHz bands for RF switches and PA, with mixers operating around 28 GHz. By employing the techniques outlined in **Chapter 3**, a significant substrate impact was observed, particularly for the RF switches. It was demonstrated that by upgrading the substrate from low resistivity to high resistivity substrate, low-loss RF switches could be achieved using the

3-stack design, while high power handling was achieved using the 12-stack switch. Additionally, the use of high-resistivity substrates in the PA resulted in a 0.5 dB improvement in output power and a 5 % increase in PAE. However, the substrate influence on mixers was minimal, as no significant effect was observed during the simulations using HR substrates.

Aside from designing a conventional Gilbert cell mixer topology, an innovative topology is introduced, showcasing the use of the FDSOI technology's back-gate as an RF input. While typically recommended as a DC bias input by the foundry, this work explores its novel application for RF signal processing. The exploration of this unique design further underlines the flexibility and potential of FDSOI technology in RF circuit design, offering new pathways for future innovations.

Discussion

Need for Further Traps Quantification

Over the last two decades, extensive research has been conducted on trap-rich substrates, such as eSI™, which are known to contain traps that significantly enhance RF performance. Understanding and accurately measuring the density of these traps, along with their precise position within the silicon bandgap, is becoming increasingly important. In this thesis, a complementary approach combining PICTS measurements with simulations was employed to explore the position of these traps. Discrete traps were identified in the polysilicon trap-rich layer, and a comprehensive model was developed. This study opens the door to further exploration of trap-rich materials and their potential impact on RF performance.

However, only one type of trap-rich substrate has been analyzed so far, and there is a strong belief that the density and characteristics of traps could vary with the use of different materials, such as amorphous silicon instead of polysilicon. Additionally, the density of traps is likely to change depending on the specific processing conditions or recipes used during fabrication. This work lays the groundwork for further studies aimed at understanding how varying the material composition and processing techniques can influence trap density and, in turn, RF performance.

Porous silicon should also be added to the list alongside polysilicon and amorphous silicon. A modeling approach for porous silicon was proposed in this thesis, and comparing these trap-based materials would benefit the scientific community, providing a deeper understanding of their unique characteristics.

Assessing Substrate Impact on RF Circuit Performance

Throughout this thesis, it has been demonstrated that the substrate significantly influences passive devices. Building upon this understanding, this work extends the analysis to combine both active and passive devices within the design of key elements of the RF front-end module, namely switches, power amplifiers and mixers. However, the impact of the substrate is not uniform across all these components, likely due to the specific architectures of the designed circuits.

In particular, this thesis establishes that the substrate plays a critical role in RF switches, especially in the series-shunt topology, where it functions as a first-order element in enhancing circuit performance. This conclusion is consistent with the observation that 100 % of RF switches in modern smartphones utilize HR substrates, as seen in PDSOI technology.

In contrast, the substrate influence is less pronounced in certain circuit types, as illustrated by the power amplifier. In this case, the substrate is considered a second-order factor, having only a moderate impact on RF performance with 5 % improvement in PAE and 0.5 dB gain in the output power using HR substrate. However, it is expected that implementing a balanced PA with a hybrid coupler on an HR substrate could elevate the substrate role to a first-order factor in improving performance. This expectation arises from the significant size of the hybrid coupler, which measures approximately 550 × 140 µm.

Furthermore, simulations performed in this work demonstrate that the substrate has minimal influence on the performance of RF mixers. It is important to note that these findings are based solely on simulations across different substrates for mixers and should be interpreted cautiously, without strong conclusions. This leads to the conclusion that the mixer topology studied here is largely substrate independent. Further experimental validation and testing would be necessary to confirm the true extent of the substrate's impact on mixer performance in practical applications.

These findings underscore the necessity of a case-by-case evaluation of the substrate's impact, as its influence can vary significantly across different circuit topologies and applications. The substrate's role is not uniform—what works for one type of circuit or application may not necessarily apply to another.

Substrates: Present Status and Future Directions

Today, if a performance increase is required in RF applications, it can be achieved through the use of high-resistivity substrates in an industrial process. Two promising approaches to improve substrate performance are field effect passivation and PN junction implant passivation. However, each of these techniques comes with its own limitations. FE passivation faces the drawback of maximum density area constraints, making it impractical for implementation across an entire wafer. On the other hand, PN junctions, while not limited by

density, are challenging due to the iterations required to balance them properly. PNlines, in particular, are more complex and time-consuming to implement, as they require precision and complex design. Therefore, PNgrid is recommended as a more practical solution, as it is geometry-independent and easier to implement in comparison to PNlines.

Looking towards near-term substrate solutions, the double-BOX substrate presents a promising option. This substrate offers performance close to that of a conventional trap-rich substrate and could serve as an excellent choice for upcoming technologies. Passive devices implemented atop this substrate have been studied throughout this thesis, and it would be of great interest to explore how an entire technology could be designed on top of this *special advanced* trap-rich substrate. Its near-TR performance suggests that it could be an ideal candidate for further industrial adoption in the coming years.

In the more distant future, porous silicon has the potential to become the next revolutionary substrate material. While it currently faces challenges related to mechanical robustness, due to its fragile nature, its excellent RF performance makes it an attractive candidate for further research. As the industry moves forward, there is a growing expectation that efforts will be directed toward enhancing the mechanical strength of porous silicon, enabling it to become a viable option for future substrates. If this challenge is solved, porous silicon could offer unparalleled performance benefits, positioning it as a next-generation substrate solution for high-frequency RF applications.

Germanium in CMOS Substrate Engineering

Indeed, gold atoms are generally undesirable in CMOS foundries due to their fast diffusion rates [187]. If gold diffuse into the transistor channel, it would significantly reduce carrier mobility, effectively degrading the performance of the FET.

On the other hand, carbon and germanium, which exhibit lower diffusivity compared to gold, are commonly used in conventional CMOS processes [188, 189]. For example, germanium is used to enhance transistor mobility [190]. Since carbon and germanium are accepted in CMOS foundries, they can be considered as potential doping materials for increasing the resistivity of standard silicon substrates. Using these elements to dope the entire volume of the

substrate is expected to result in higher resistivity, benefiting the performance of devices fabricated on such substrates. However, doping the entire substrate volume may lead to increased manufacturing costs. As a cost-effective alternative, a high-resistivity substrate can be used as a base, with localized germanium implants introduced beneath passive devices to enhance performance.

Perspectives

Several relevant future research directions can be identified from the discussions in this thesis.

Measurements Field

Complete RF Mixer Setup Measurements

Simulations for the RF mixer have already been completed, yielding valuable insights into its performance. Furthermore, measurements of the conversion gain versus LO power, frequency, and the P1dB have already been conducted, which is a significant achievement (see **Section 4.3**). However, it remains crucial to develop a measurement setup to validate the remaining simulation results for IIP3, NF, and feedthrough.

Measuring the third-order input intercept point IP3 (IIP3 and OIP3) presents a challenge due to the requirement for three signal sources. It is anticipated that the setup will involve VNA capable of generating two tones at 28 GHz and 28.3 GHz, while a second VNA (or signal generator) will be used to generate the LO signal at 21 GHz. Although this configuration may appear complex and somewhat crowded, it is a necessary approach to make the measurement. For the noise figure measurements, a spectrum analyzer will be required. The setup is expected to be similar to the NF measurement setup used for the LNA, which simplifies the process. Once the configuration is properly established, obtaining the NF measurements should be straightforward, requiring only the necessary time and resources to complete.

Looking ahead, IIP3 will be measured to assess linearity, the noise figure will be measured to evaluate noise performance, and feedthrough will be measured to determine the extent of unwanted signal leakage between ports. These measurements are essential for confirming the accuracy of the simulations and ensuring that the RF mixer meets the required performance specifications.

Substrate Level

Enhancing Substrate Maturity

To evaluate the thermal stability of the double-BOX substrate, comprehensive temperature tests will be conducted to determine its robustness to conven-

tional CMOS process. It is expected that the substrate will exhibit enhanced robustness, particularly when doped, making it suitable for high-performance applications since no contact exists between the polysilicon trap-rich layer and the monocrystalline silicon. Additionally, the PICTS method will be employed to quantify the traps present in porous silicon. This analysis will investigate whether the characteristics of these traps depend on the fabrication recipe used, with the ultimate goal of developing an accurate model of the substrate's properties.

Looking ahead, there is potential to integrate the double-BOX substrate into the next generation of FDSOI technology, possibly at the 10 nm node, to leverage its superior electrical isolation and thermal characteristics. Furthermore, transistors will be manufactured and measured using the double-BOX substrate to assess its impact on performance metrics such as mobility and threshold voltage.

Circuit Level

Substrate Option During Circuits Design

During the design process, it is essential to include the substrate as a key parameter in parasitic extraction (PEX) and method of moments (MoM) simulations. By doing so, the substrate's influence on circuit performance, especially in RF designs, can be accurately modeled and accounted for. This approach provides a more realistic representation of the electrical behavior of the circuit, ensuring that substrate effects such as parasitic capacitances and resistances are properly evaluated.

Incorporating the substrate as a design parameter enables designers to optimize device layouts more effectively. By minimizing parasitic effects caused by substrate interactions, overall circuit performance—such as signal integrity, linearity, and efficiency—can be significantly improved. This strategy is particularly critical for advanced semiconductor technologies, where substrate interactions become more pronounced and can strongly impact the circuit's electrical characteristics, as demonstrated throughout this thesis.

Application of Linearization Techniques

In circuit design, one of the most critical figures of merit is linearity, partic-

ularly in power amplifiers. Several techniques have been proposed to enhance the linearity of PAs, as discussed in [151]. These include methods such as feedforward linearization, Cartesian feedback, predistortion techniques, and envelope feedback techniques. While these methods have been widely studied and demonstrated to be effective at lower frequencies, their behavior and effectiveness at higher frequencies, such as 28 GHz, 77 GHz, or even 140 GHz, remain an open area of exploration. Investigating the performance of these linearization techniques at such high frequencies is particularly relevant for advanced driver-assistance systems (ADAS) applications, where circuit performance is pushed to its limits.

Similarly, in the case of LNAs, noise-cancelling techniques have been employed successfully to reduce noise at lower frequencies, such as around 6 GHz, as shown in [191, 192]. However, it is crucial to evaluate whether these noise-cancelling methods remain effective and practical when applied to higher frequencies, such as those used in ADAS applications. Frequencies in the range of 77 GHz or 140 GHz present unique design challenges, including increased parasitic effects and reduced device gain, which could impact the performance of these techniques.

Alternative Mixer Architectures

Throughout this thesis, it has been shown that the mixer architecture used is largely substrate-independent. However, it is worthwhile to explore alternative mixer architectures, such as mixers with degenerative inductors, to better see substrate effects and potentially enhance performance. The primary goal of this alternative architecture is to improve the linearity, particularly the IIP3. This is achieved by introducing an inductor between the source and ground of the RF FETs in a Gilbert cell mixer.

The inclusion of the degenerative inductor lowers the conversion gain of the mixer but significantly enhances its linearity. It is expected that this type of mixer architecture will be more sensitive to substrate variation. This makes it an ideal candidate for investigating how different substrate characteristics, such as POR and HR, influence the mixer's performance.

Wideband Designs for ADAS Applications

In this thesis, the focus has been on narrowband mixers. As a natural pro-

gression, it would be advantageous to investigate the development of wideband mixers operating in the 130-150 GHz range. Specifically, the goal could be to achieve an intermediate frequency of 100 MHz from an RF input signal at 140 GHz. This approach would result in a wideband mixer capable of covering the 130-150 GHz RF range with a direct conversion to baseband.

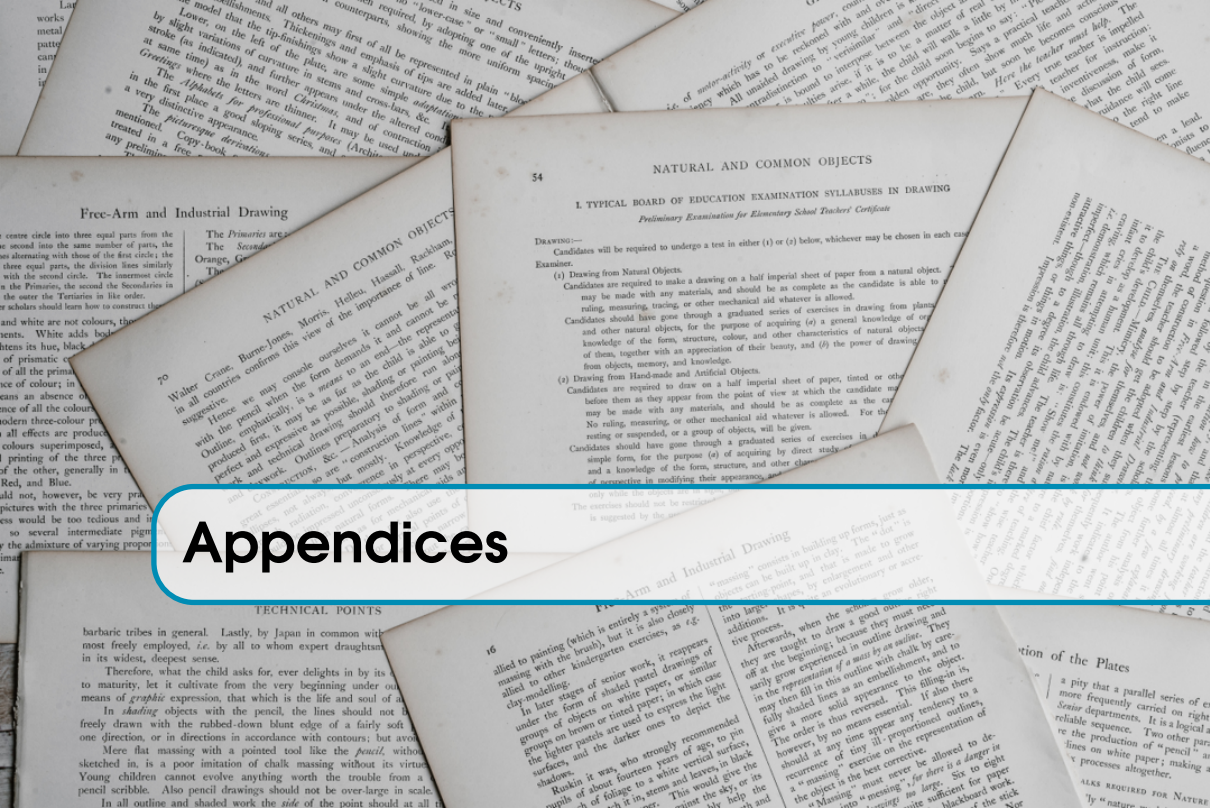
To facilitate this transition, the design of a wideband LNA spanning the 130-150 GHz frequency range is critical. The primary role of this LNA would be to integrate seamlessly with other components—such as the switch and mixer—to form the receiver (Rx) section of the RF front-end module. Additionally, the design of a DC-150 GHz SPDT switch could be undertaken to support the wideband receiver architecture. The complete receiver chain, comprising the switch, LNA, and mixer, is intended for use in advanced driver-assistance system (ADAS) applications, as described in [193].

Toward Transceiver Design

It is important to understand that possessing individual components—such as the switch, LNA, and mixer—does not imply a straightforward connection between them. Each of these blocks is usually matched to 50 Ω pads for testing purposes. Successful integration necessitates careful impedance matching between the output of one block and the input of the next. For example, the output of the LNA must be properly matched to the input of the mixer. However, the actual impedances of these connections often differ from 50 Ω and are not naturally matched to this standard. Therefore, meticulous design and tuning are required to ensure optimal performance and minimal signal loss across the entire system. Achieving this integration involves adjusting the matching networks to facilitate seamless signal flow and maximize the efficiency of the RF front-end module.

Appendices

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Appendices

A Effective Resistivity Summarized

Figure 5.1 provides a clear and concise demonstration of the process for extracting the effective resistivity and effective permittivity of a silicon substrate using S-parameters. This method is crucial for understanding the electrical properties of the substrate, which play a key role in determining the performance of RF and microwave circuits. The procedure is divided into three well-defined and systematic steps (see Figure 5.1).

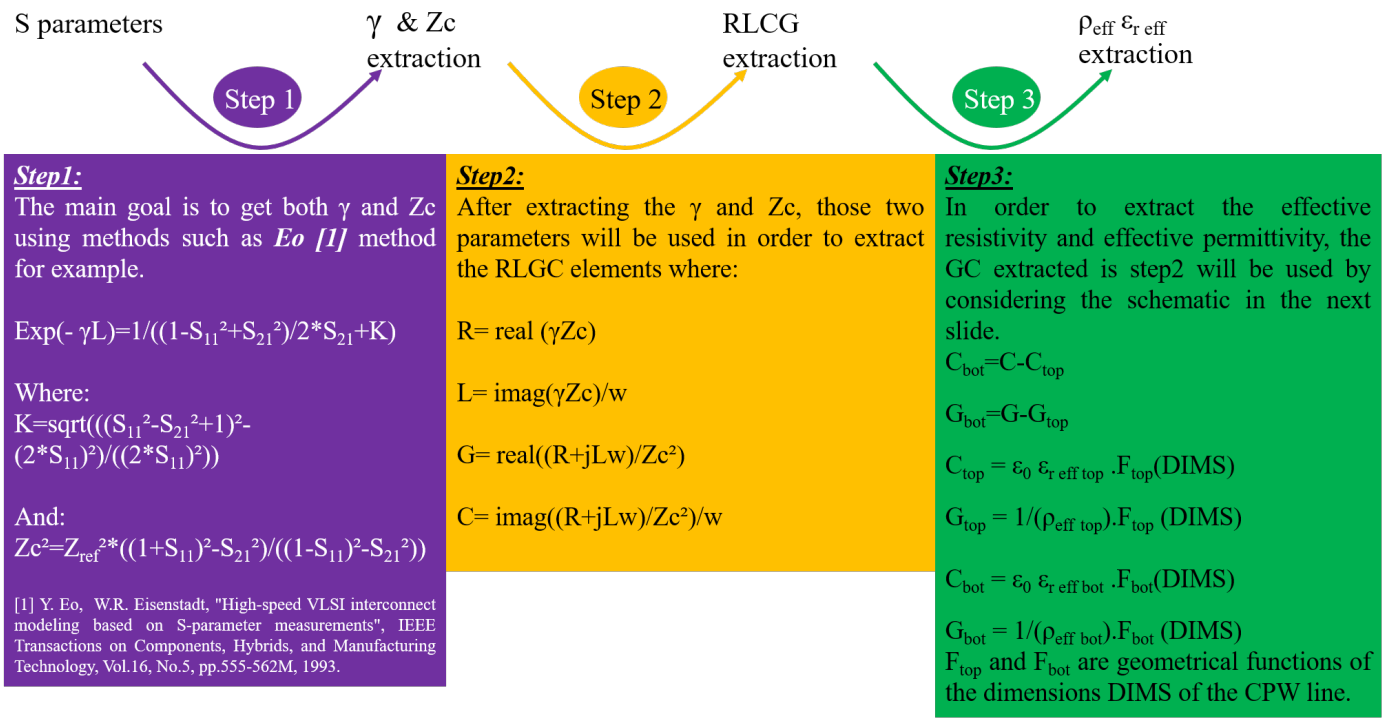


Figure 5.1: The steps of the extraction of the effective resistivity summarized in one page.

B P1dB Setup Measurements for RF switches

Having a setup for on-wafer measurements of the P1dB (1 dB compression point) for RF switches is crucial for evaluating their performance in high-frequency applications. P1dB indicates the power level at which the switch's linearity begins to degrade, resulting in a 1 dB reduction in gain. This metric is vital for understanding the switch's behavior under large-signal conditions and assessing its suitability for use in RF front-end modules, where maintaining signal integrity is essential. On-wafer measurements allow for direct testing of devices without packaging, providing faster feedback and more accurate insights into device performance.

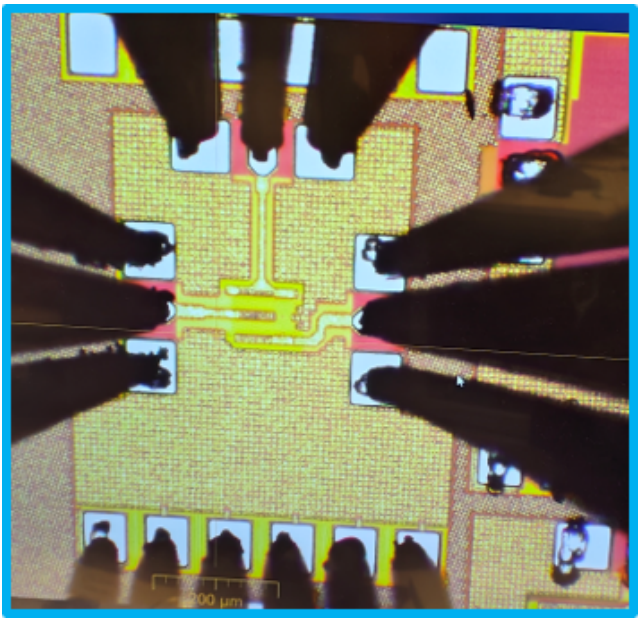


Figure 5.2: 3-stack switch under large-signal measurements.

B.1 Setup Description

Figure 5.3 shows the measurement setup performed by Incize to extract the P1dB metric of the two RF switches analyzed in this thesis. The entire setup is capable of delivering around 49 dBm at the input of the DUT, corresponding to nearly 80 W of RF power.

The process begins with a signal generator producing a small, pure RF signal at 900 MHz, as depicted in **Figure 5.3(a)**. This initial signal is then amplified by a high-power PA, which boosts the signal to the desired high-power level. However, due to the non-linear behavior of the PA, unwanted harmonics are generated, as illustrated in **(b)**.

To prevent these harmonics from interfering with the measurement and to avoid them being mistaken for harmonics generated by the DUT, a band-pass filter is employed to clean the signal. This filter removes the harmonics produced by the PA, ensuring that the signal remains clean and pure, as shown in **(c)**.

The RF switch under test is in its ON state, which mimics the behavior of a CPW line, a topic that will be discussed in more detail later in this thesis. The clean signal from **(c)** is injected into the RF switch. The output signal at **(d)** will exhibit a slight reduction in the fundamental frequency at f0, primarily due to the internal losses of the switch, as well as harmonics generated by the non-linear behavior of the RF switch.

To separate the fundamental signal from the harmonics, a passive device called a diplexer is used. The diplexer acts as a frequency-selective filter, allowing signals from two distinct frequency ranges to pass through different ports without interference. The fundamental frequency is routed to point **(f)**, where it is measured using a power meter. On the other side, the second and third harmonics (H2 and H3) are directed to point **(e)**, where they are measured using a spectrum analyzer.

The measurements were started by sweeping the input power from 0 dBm, gradually increasing until the point where the gain decreased by approximately 4-5 dB. At that point, the system was stopped to prevent potential damage to the RF switch. To ensure reliable results, each switch was measured twice on the same die. Consistency between the two measurements was confirmed by obtaining the same curve, ensuring repeatability and accuracy in the results.

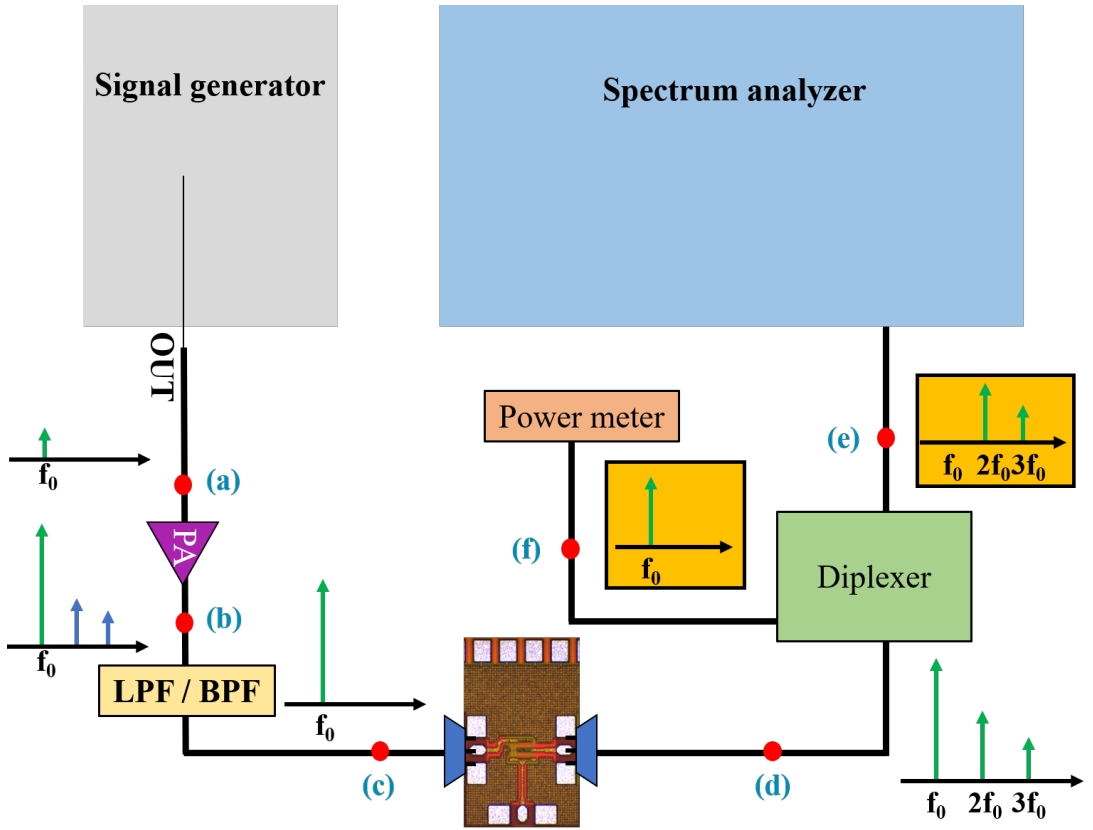


Figure 5.3: Practical implementation of the high-power large-signal on-wafer measurement setup used for measuring the P1dB of RF switches.

This setup operates in continuous wave mode, which can be harsh on the circuits due to the constant high-power exposure. Typically, it is recommended to use a 5 % duty cycle to minimize stress on the components. The continuous wave mode can lead to excessive heat generation and increased wear on the devices, whereas reducing the duty cycle helps to limit the power-on time, allowing the circuits to cool down between pulses and thus ensuring greater reliability and longevity during testing.

C Large Signal Measurements for RF mixers

In this section, we will describe the procedure for on-wafer measurements of RF mixers. The primary goal is to measure the output power at the intermediate frequency (IF) while sweeping the LO power, with the RF power and LO frequency held constant. By capturing the IF output power as a function of the LO power, we can gain valuable insights into the performance of the mixer, including its conversion gain, linearity, and dynamic range. This measurement approach will allow us to fully characterize the mixer's behavior under real operating conditions.

C.1 Setup description

Since the mixer is a somewhat exotic circuit, unlike more common components like PAs and LNAs, it features two inputs—RF input and LO input—and one output, the IF. This setup makes its measurement process a bit more complex and demanding. The test configuration typically requires the use of three GSG probes for the RF, LO, and IF connections, along with an additional DC probe for biasing actives. This combination of multiple inputs and outputs, along with the need for precise alignment of the probes are depicted in **Figure 5.4**.

The primary objective in this setup is to fix the RF power at -30 dBm and the RF frequency at 28 GHz. Meanwhile, the LO power is swept over a range, and the output from the IF port is recorded. This process allows us to observe how the LO power influences the mixer's performance at a constant RF input. By analyzing the output at the IF port, we can gain insights into the conversion gain.

First, power calibration is performed for both the RF cable (black) and the LO cable (red) to ensure that the power at the end of each cable is correctly recognized by the VNA. This step allows the VNA to account for any losses along the cables, ensuring that the power being dealt with is accurately represented at the output of the cables. By performing this calibration, proper power levels are established for the subsequent mixer measurements.

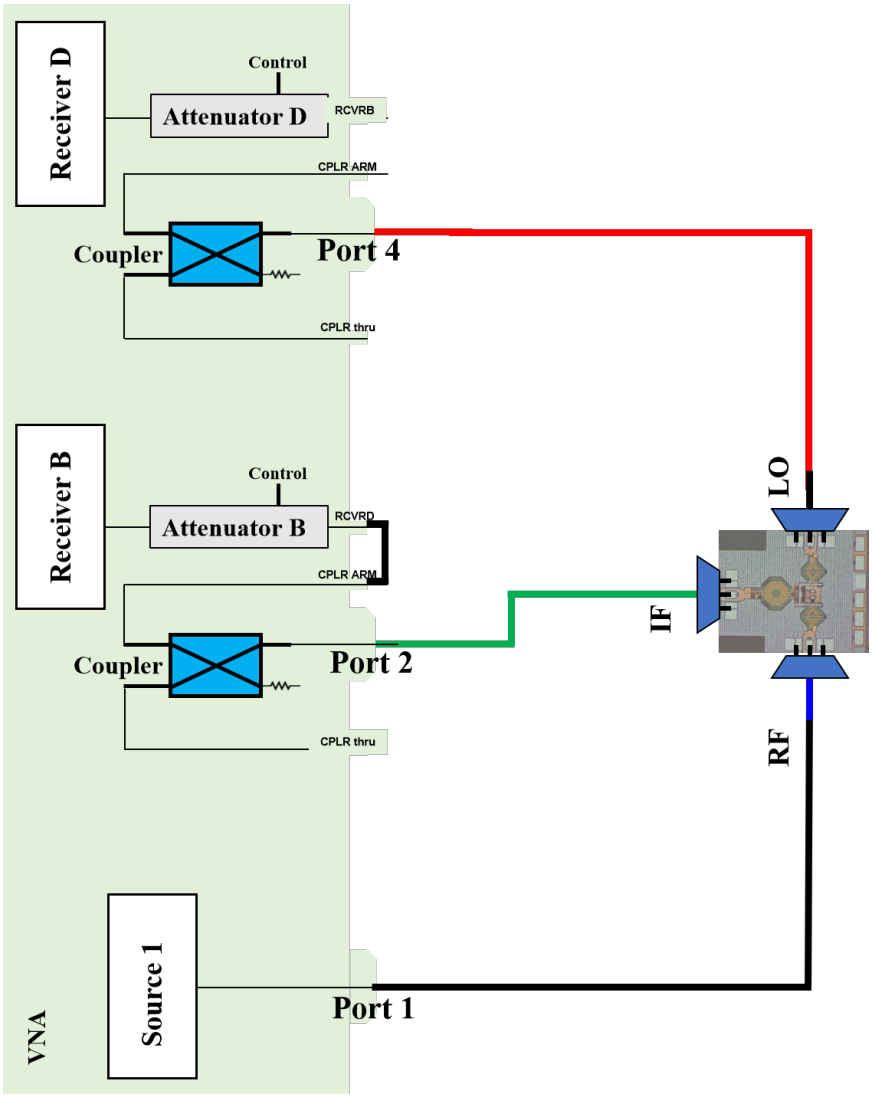


Figure 5.4: Practical implementation of the RF mixer on-wafer measurement setup.

After that, it is necessary to specify the appropriate frequencies to the VNA, as indicated in Table 5.1, referred to as the frequency offset channel. It should be noted that the primary port, which is the LO port, must be set to sweep in power. This ensures that the VNA operates with the correct frequency settings for both the RF and LO inputs, allowing accurate measurement of the mixer's performance as the LO power is varied.[1]

Table 5.1: Table from the VNA displaying the frequency of each port of the RF mixer.

	Mode	Sweep type	Settings
Primary		Power sweep	f_{LO}=21 GHz
Source	Un-coupled	Power sweep	f_{RF}=28 GHz
Receiver	Un-coupled	CW time	f_{IF}=7 GHz

To ensure that both the RF and LO signals are injected at the same time, they must be turned on simultaneously. This synchronization can be controlled through the power and attenuator settings in the VNA (see Table 5.2). It should be noted that since Port 2 and Port 3 are turned off, the values set for these ports are irrelevant and do not impact the measurement process.

Table 5.2: Powers and attenuators window from the VNA displaying that RF and LO signals are in ON state.

Name	State	Port power [dBm]	Start power [dBm]	Stop power [dBm]
Port1	**ON**	-5	-30	-30
Port2	OFF	-5	-10	-10
Port3	OFF	-5	-10	1
Port4	**ON**	-5	-30	5.5

[1]The RF power will also be swept, but initially, the output power at the IF port will be measured as a function of LO power (P_{LO}) in a single channel. When sweeping the RF power, a second sweep will be performed, generating multiple curves of IF output power versus P_{LO}. Each curve will represent a different RF input power.

So, far the performed measurements have their reference at the end of the cable not at the probe tips, then the measurements performed have some probe losses that should be added/removed. Since LO and RF signals are inputs then:

$$P_{LO_DUT} = P_{LO_measured} - IL_{probe_at_21G} \tag{5.1}$$

$$P_{RF_DUT} = P_{RF_measured} - IL_{probe_at_28G} \tag{5.2}$$

Since IF signal is an output then:

$$P_{IF_DUT} = P_{IF_measured} + IL_{probe_at_7G} + IL_{cable_at_7G} \tag{5.3}$$

D Creating Trap-Rich Substrate Without Polysilicon

This appendix aims to provide insight into the feasibility of creating a trap-rich layer in an SOI substrate without the need to deposit an additional semiconductor layer. This approach leverages the ability to induce traps within a high-resistivity (HR) substrate by deliberately disrupting the SiO_2-bulk interface with specific atoms.

Atoms such as carbon (C) and nitrogen (N) can be introduced into the silicon band-gap, where they act as trap centers. The effectiveness of this process depends on the energy and dose of the implanted atoms, which directly influence the creation and density of these traps. As a result, the effective resistivity of the substrate can be modified, leading to the formation of various types of trap-rich substrates. This method offers a versatile and potentially more integrated solution for enhancing the performance of RFSOI substrates by tailoring the trap-rich layer within the existing substrate structure.

Simulations are performed on a CPW line having the following dimensions 26, 12, 208 µm for the width of the central track, spacing between the signal and ground electrodes, and width of the ground track , respectively. Moreover, the impurities (C and N) are introduced at 50 nm below the insulating layer.

D.1 Doping With C atoms

Figure 5.5 presents the effective resistivity as a function of applied DC bias, with each curve corresponding to different densities of carbon implants ranging from 10^{16} to 10^{20} cm^{-3}. It is worth noting that the C atoms introduce two energy levels in the silicon bandgap: the first is situated 0.25 eV away from Ec (the conduction band), while the second lies 0.27 eV away from Ev (the valence band) **[90]**.

As shown in **Figure 5.5**, carbon implant densities around 10^{16} cm^{-3} do not significantly impact the PSC, leaving the electrons at the SiO_2-bulk interface largely unaffected. However, as the implant density increases beyond this threshold, the effective resistivity begins to rise gradually. At densities around 10^{19} cm^{-3}, an effective resistivity of 10 $k\Omega \cdot cm$ can be achieved, which is considerably high and advantageous for RF applications.

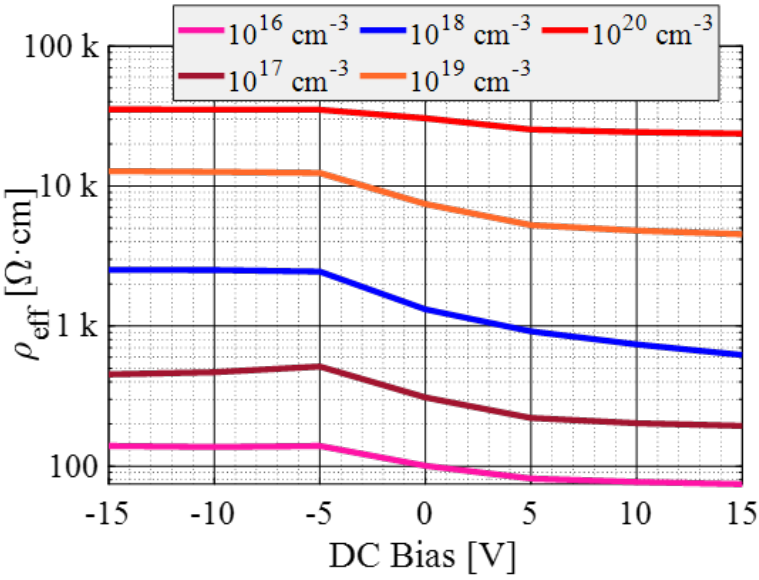


Figure 5.5: Simulation of the effective resistivity for HR substrate with C implantation at different doses extracted at 2 GHz.

D.2 Doping With N atoms

Similar to the substrate doping using C atoms, the nitrogen N atoms introduces several energy level where 3 are donors and are far from the valence band 0.22, 0.48 and 0.71 eV and 2 acceptor levels 0.18 eV and 0.34 eV far from the conductance band as given in [90].

Figure 5.6 presents the effective resistivity as a function of the applied DC bias, measured at 2 GHz for an HR substrate doped with nitrogen N atoms within the 50 nm region below the insulating layer. When the density of N atoms is around 10^{16} cm^{-3}, the parasitic surface conduction (PSC) persists and is not overcome. However, as the density increases to 10^{17} cm^{-3}, the effective resistivity shows a significant increase, though it becomes highly dependent on the applied DC bias, with resistivity values varying between 2 k and 600 Ω · cm. When the density of N atoms exceeds 10^{17} cm^{-3}, the effective resistivity stabilizes at a bias-independent value of 2 kΩ · cm, indicating that the Fermi level is pinned near the silicon midgap. In this scenario, the traps introduced by the N atoms effectively compensate for the charges induced by both PSC and

the applied DC bias, resulting in a fixed value of effective resistivity.

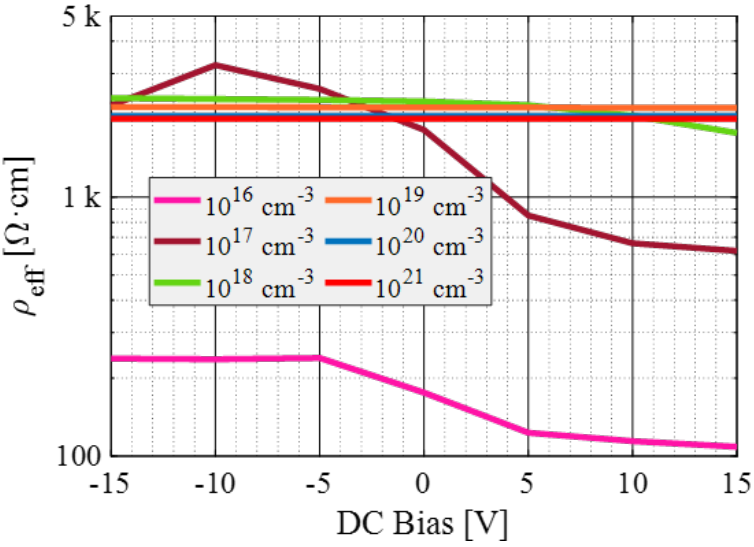


Figure 5.6: Simulation of the effective for HR substrate with N implantation at different doses extracted at 2 GHz.

E Double-BOX Substrate Doping With Germanium

This part is complementary to the Section 3.4.3.

Continuing from the doping of the double-BOX substrate with carbon atoms, this section presents the results of doping the double-BOX substrate with germanium (Ge) atoms. Ge atoms generate traps at energy levels of 0.27 eV and 0.5 eV, both far from Ec. The measurements were performed identically to those in Section 3.4.2. To evaluate the effects of Ge doping, 2.1 mm-long CPW (coplanar waveguide) lines were designed and fabricated on two types of substrates: one with low Ge doping (DBJH10) and the other with high Ge doping (DBJH9), as illustrated in Figure 5.7.

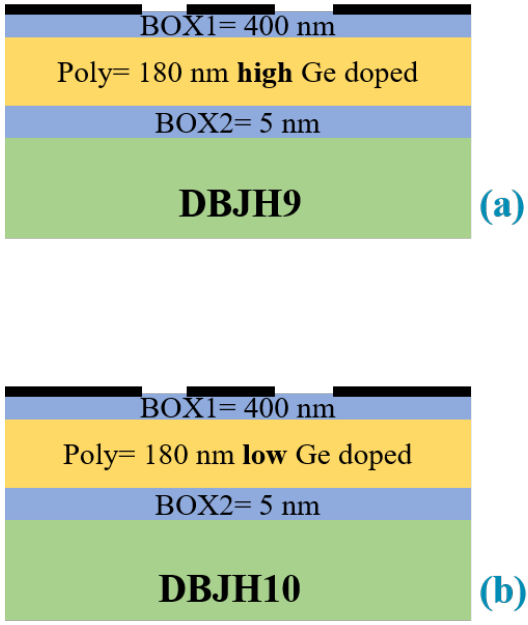


Figure 5.7: Schematic view of the two Ge-doped polysilicon substrates in this part named as DBJH9 in (a) and DBJH10 in (b).

E.1 Small-Signal Measurements

Small-signal measurements of the CPW lines were conducted using an Agilent 2-port Performance Network Analyzer (PNA)-X, along with a pair of ground-

signal-ground (GSG) |Z| probes featuring a 100 µm- pitch.

Figure 5.8 shows the extracted effective resistivity as a function of the DC bias applied to the CPW line. Both substrates exhibit high effective resistivity, exceeding 2 kΩ · cm, which is twice the resistivity of bulk silicon substrates. This improvement is attributed to the traps present in the polysilicon layer and those introduced by the Ge atoms, which help mitigate the PSC effect, thereby restoring the nominal resistivity.

In addition, since the effective resistivity remains high and bias-independent, it indicates that the Fermi level is pinned near the silicon mid-gap. Furthermore, the lowly Ge-doped substrate (DBJH9) exhibits an effective resistivity of approximately 2.7 kΩ · cm, while the highly Ge-doped substrate (DBJH10) shows a higher value of around 3.5 kΩ · cm. The 800 Ω · cm improvement in effective resistivity is attributed to the increased number of traps in the polysilicon layer created by the Ge atoms, which leads to a slight shift of the Fermi level toward the silicon mid-gap.

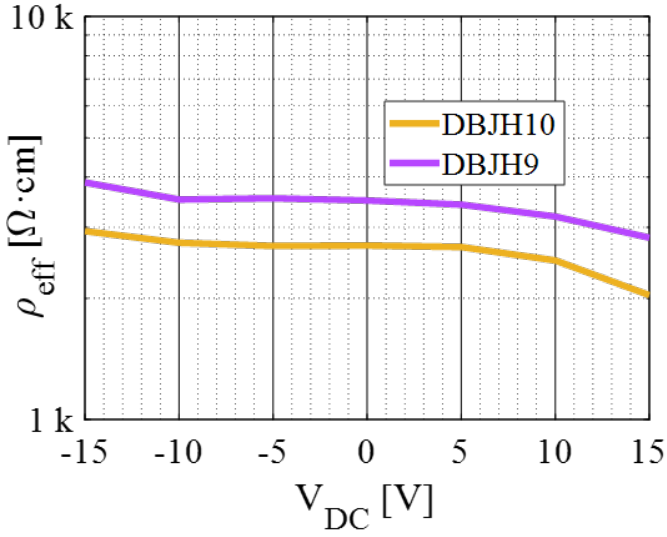


Figure 5.8: Measured of the effective resistivity as a functio of the applied DC bias on the CPW line extracted at 5 GHz.

E.2 Large-Signal Measurements

Large-signal measurements were conducted using a single-tone frequency of 900 MHz injected into one port of the CPW line, with power ranging from -14 to 25 dBm. Subsequently, measurements of the fundamental (H1 at 900 MHz), second (H2 at 1.8 GHz), and third (H3 at 2.7 GHz) harmonics were taken at the second port of the CPW.

Figure 5.9 presents the measured second (left) and third harmonic (right) levels as a function of the fundamental frequency H1 at 900 MHz. The third harmonic level is observed to be 10 dB higher in the DBJH10 substrate (lowly Ge-doped) compared to the DBJH9 substrate (highly Ge-doped). Additionally, the second harmonic H2 is visibly higher for the DBJH10 substrate than for the DBJH9 substrate.

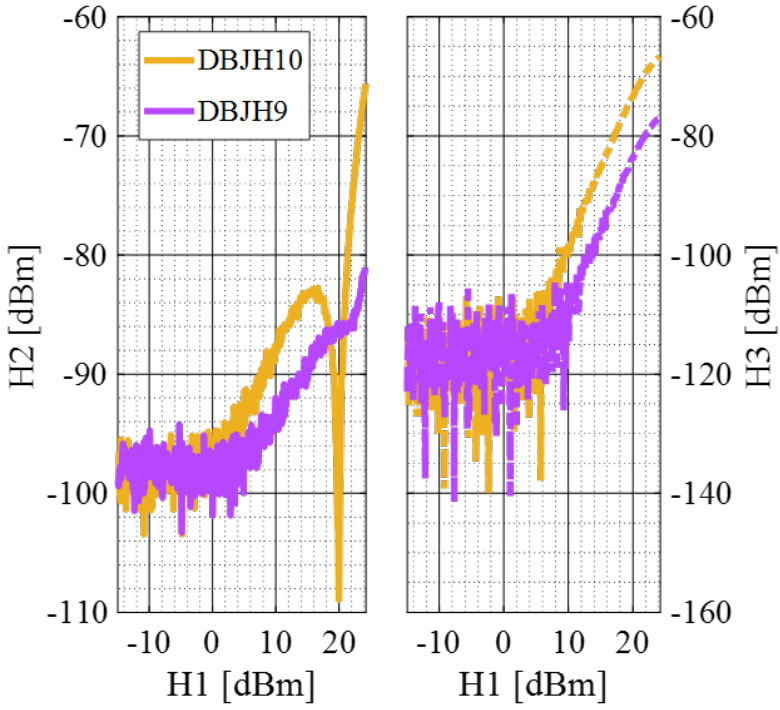


Figure 5.9: Schematic view of the two Ge-doped polysilicon substrates in this part.

It is important to note that the pronounced dip observed in the DBJH10 curve, and the less pronounced dip in the DBJH9 curve, are not due to measurement errors. This is a physical phenomenon typically seen in doped or contaminated polysilicon trap-rich substrates. These dips are dependent on the applied DC bias, although their exact physical origin remains unclear at this time. Ongoing research within the group is currently focused on investigating the underlying mechanisms responsible for this phenomenon.

Figure 5.10 shows the extracted of the second harmonic as a function of the applied DC bias[2] on the CPW line.

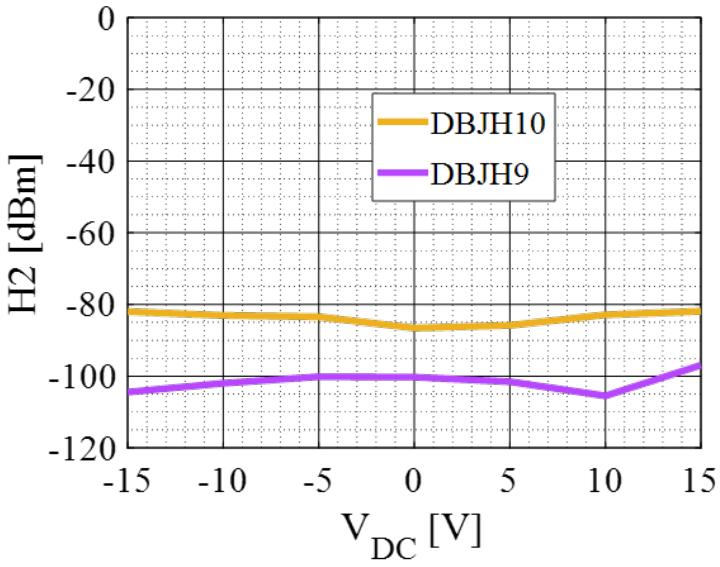


Figure 5.10: Measured of the second harmonic (H2) power at H1= 15 dBm versus the applied DC bias for doped trap-rich layer with Ge atoms in double-BOX substrate.

Both substrates are bias independent because the Fermi level is pinned near silicon midgap which correlates well with the effective resistivity in **Figure 5.8**. The DBJH10 (low Ge-doped) shows a value around -81 dB and the DBJH9

[2]The extraction process involves determining the H2 level at 24 dBm output power, followed by drawing a line with a slope of 2. Subsequently, the H2 value at 15 dBm output power was extracted at each bias point.

(high Ge-doped) shows around 20 dB improvement. This improvement is related to the traps created by the Ge-atoms that are higher in DBJH9 than in DBJH10.

Germanium and Carbon atoms have been demonstrated to increase the resistivity of the polysilicon trap-rich layer in an SOI substrate. Additionally, these atoms can be utilized in the double-BOX substrate to enhance the density of traps within this layer. Increasing the number of traps in the trap-rich layer is crucial for mitigating the effects of recrystallization during high-temperature CMOS processes. During annealing, the process naturally attempts to repair defects in the polysilicon layer. However, the presence of Ge and C atoms creates additional traps that counteract this defect-repairing effect, ensuring that the trap-rich layer maintains its high trap density.

F Fast Fourier Transform of the Square Wave

If the square wave can be expressed mathematically as:

$$x(t) = A \cdot \mathrm{sgn}\left(\sin\left(2\pi \cdot f_{LO} \cdot t\right)\right) \tag{5.4}$$

where f_{LO} is the fundamental frequency of the square wave.

The square wave can be decomposed into a Fourier series, which is the sum of its harmonic components:

$$x(t) = \frac{4A}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \cos\left(2\pi \cdot n \cdot f_{LO} \cdot t\right) \tag{5.5}$$

Here, n represents the odd harmonics (1, 3, 5, etc.).

The Fourier transform $X(f)$ of the square wave is given by:

$$X(f) = \frac{4A}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \delta\left(f - n \cdot f_{LO}\right) \tag{5.6}$$

This expression indicates that the square wave in the time domain corresponds to a series of delta functions in the frequency domain, located at the odd harmonics of the fundamental frequency f_{LO} . Each delta function is weighted by the amplitude $\frac{4A}{\pi n}$.



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