Novel mmWave NMOS Device for High Pout mmWave Power Amplifiers in 45RFSOI

Sameer H. Jain
Globalfoundries Inc
Hopewell Jn, NY,USA
sameer.jain@globalfoundries.com

Dimitri Lederer
Université catholique de Louvain
Louvain-la-Neuve, Belgium
dimitri.lederer@uclouvain.be

Arvind Kumar
Globalfoundries Inc
Hopewell Jn, NY, USA
arvind.kumar@globalfoundries.com

Sudesh Saroop
Globalfoundries Inc
Hopewell Jn, NY, USA
sudesh.saroop@globalfoundries.com

Chris Prindle
Globalfoundries Inc
Hopewell Jn, NY, USA
chris.prindle@globalfoundries.com

P. Srinivasan
Globalfoundries Inc
Malta, NY, USA
srinivasan.purushothaman@globalfoundries.com

Wen Liu
Globalfoundries Inc
Essex Jn, VT, USA
wen.liu@globalfoundries.com

Ravi Achanta
Globalfoundries Inc
Hopewell Jn, NY, USA
ravi.achanta@globalfoundries.com

Erdem Kaltalioglu
Globalfoundries Inc
Hopewell Jn, NY, USA
erdem.kaltalioglu@globalfoundries.com

Stephen Moss
Globalfoundries Inc
Essex Jn, NY, USA
stephen.moss@globalfoundries.com

Greg Freeman
Globalfoundries Inc
Hopewell Jn, NY, USA
greg.freeman@globalfoundries.com

Paul Colestock
Globalfoundries Inc
Santa Clara, CA, USA
paul.colestock@globalfoundries.com

***Abstract*—The adoption of 5G mmWave is upon us, with major cell phone companies having introduced phones with mmWave capabilities and major US cellphone providers building their infrastructure out. Parts manufactured using Globalfoundries 45RFSOI technology have made significant traction in the infrastructure space. A good part of the success of this technology is based on the excellent high frequency performance of the thin oxide device, the high resistivity substrate and the high voltage support enabled by the use of stacking in SOI technologies. In this paper we introduce a new transistor developed to improve the output power of mmWave power amplifiers (PA). It demonstrates ~ 1.2X increase in maximum voltage, reduced linear mode resistance and ~20% increases in f_{MAX} to >400 GHz**

Keywords—millimeter-wave (mm-wave), 5G, power amplifier (PA), silicon On Insulator (SOI), ADNFET and CMOS

I. INTRODUCTION

Historically, silicon based MOS transistors with their lower carrier mobility have had worse high frequency performance than bipolar devices. Through continued gate length scaling, the high frequency performance now rivals that provided by bipolar technologies and is sufficient to support the needs for mmWave applications. The trade-off has been a reduction in the maximum voltage supported by the FET and hence the maximum output power from power amplifiers designed using this technology. The use of phase array antennas in 5G though reduces the output power required from individual amplifiers to a range that CMOS technologies can support. Even so, the output power provided by current CMOS technologies is at the lower end of what is desired and there a clear need for devices that can increase the output power.

45RFSOI is a technology based on high performance partially depleted 45nm SOI CMOS technology [1], featuring a high resistivity trap rich (TR) substrate and a RF optimized BEOL with 3um thick Cu metal levels. Multiple papers have demonstrated PAs in 45RFSOI with a saturated output power (Psat) ranging from 23-25dBm [2]-[4] using the RVT device and a stacked FET architecture. In this paper we report the electrical results of a new FET (ADNFET) developed to further improve the output power of mmWave PAs.

I. DEVICE STRUCTURE AND ELECTRICAL PERFORMANCE

A. Device Structure and Objectives

General wisdom suggests that there is limited benefit in increasing the FET cut-off frequencies (ie f_T and f_{MAX}) above a certain threshold (~ 3-4X the operating frequency). Thus for 5G applications (24 → 48 GHz) a f_T or f_{MAX} above 200 GHz is expected to be sufficient to design a good PA. The P_{sat} of the PA is then tied to the maximum (V_{max}) and minimum (V_{min}) voltages that the FET can swing between. The V_{max} of a MOSFET is limited by reliability considerations (TDDB and HCI). Internal sizings show that the V_{max} for the RVT NFET under 5G NR modulation is limited by hot carrier injection (HCI). The V_{min} is driven by the linear mode resistance of the FET.

This paper reports on a new device (the ADNFET) that was designed to improve PA output power by optimizing the above parameters while maintaining sufficient high frequency performance. The source and drain junctions, the channel doping and the gate length were optimized to give reduced

linear mode resistance (V_{min}), increased maximum voltage support (HCI based V_{max}), all while still keeping the f_T above 200 GHz. In addition the gate resistance of the device was reduced improving f_{MAX} >400 GHz. Finally, the ADNFET is offered at 3 different designed gate length (Ldes): 32, 40 and 48 nm to enable ease of designing. The device is built at double the minimum technology gate pitch (380nm) to maximize the stress benefits of the technology and minimize parasitic capacitances. In this paper we primarily compare the performance of the ADNFET using the 45RFSOI RVT NMOS (an industry leading device) as a benchmark [2], [3]. Data for both devices is reported at same gate pitch and Wdes=1um, since that is the typical width we expect will be used in actual PA designs. It is worth noting that better performance for key metrics like f_T, f_{MAX} have been observed for alternate layouts but are not reported here in the interest of reporting relevant data.

B. DC performance

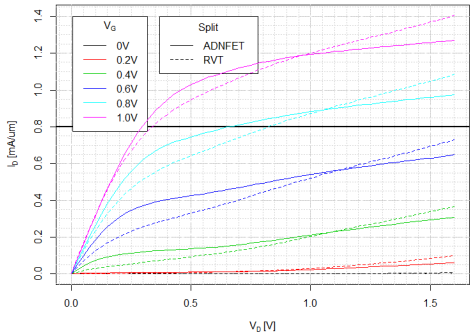

Fig. 1: Id-Vd of RVT NFET (dashed) vs ADNFET (solid) Ldes=40 nm.

Fig. 1 compares the I-V characteristics of the ADNFET with Ldes=40nm (solid line) with the RVT device (dashed lines). The ADNFET shows a lower resistance in the linear mode and significantly improved output conductance (g_{ds}) in saturation. As a figure of merit, we measured the drain voltage (Vd) for a fixed gate voltage (Vg=1.0 V) that results in a fixed current (Id=0.8 mA/um) -- we call it V_{min}, reflecting the minimum voltage encountered as the PA output voltage swings through its minima). We observe a ~20mV drop in the V_{min} for the ADNFET.

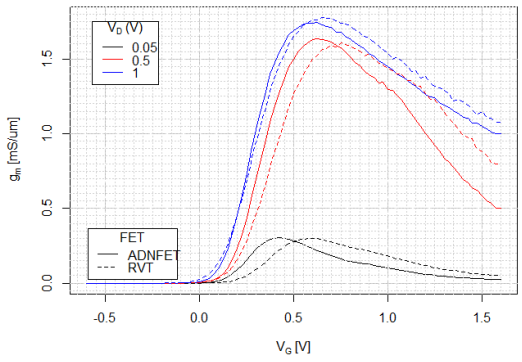

Fig. 2: Comparison of the g_m of RVT vs ADNFET (Ldes=40 nm).

Fig. 2 shows that the transconductance (*gm)* of the two devices is very comparable. The combination of similar g_m and improved g_{ds} results in an improvement of ~2X in g_m/g_{ds} for the ADNFET device (see Fig. 3).

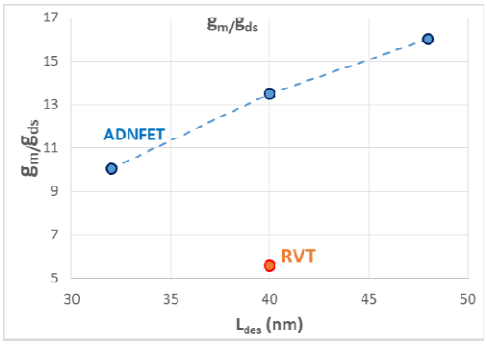

Fig. 3: peak g_m/g_{ds} for RVT vs ADNFET for Vd=1.0 V.

C. RF performance

In this section we take a look at the high frequency performance of the ADNFET.

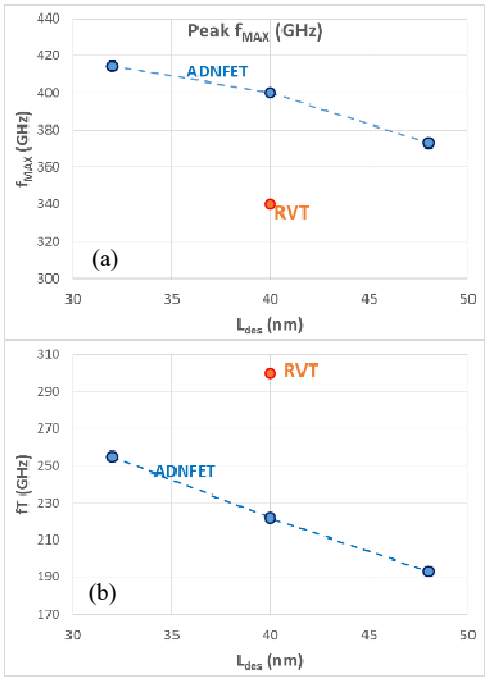

Fig. 4: Comparison of (a) peak f_{MAX} and (b) peak f_T RVT NFET vs ADNFET

Fig. 4(a) shows the ADNFET f_{MAX} to be greater than 400 GHz. The f_{MAX} for the device is comparable to the best reported for any CMOS technology [5], [6]. This is achieved through a combination of the excellent g_m and g_{ds} of the device, low external resistance and a significant reduction in the gate resistance of this device (see Fig. 5). The f_T (Fig 4(b)) of the ADNFET drops some compared to the RVT device but is >200 GHz for the Ldes=40nm device and the availability of the shorter gate length devices offer designers options for a higher frequency device if needed.

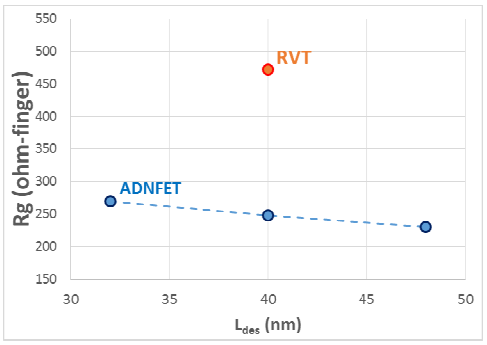

Fig. 5: Gate resistance (R_g) for RVT vs ADNFET.

Fig. 6 (a) and (b) show the Common Source (CS) and Common Gate (CG) Maximum Stable Gain (MSG) of the ADNFET vs the RVT device respectively. While the CS MSG of the devices are fairly comparable, in the CG mode, the ADNFET offers significantly better gain due to the superior g_m/g_{ds}. The combination of ADNFET in the CS and the CG of a cascode results in improved overall gain for a PA.

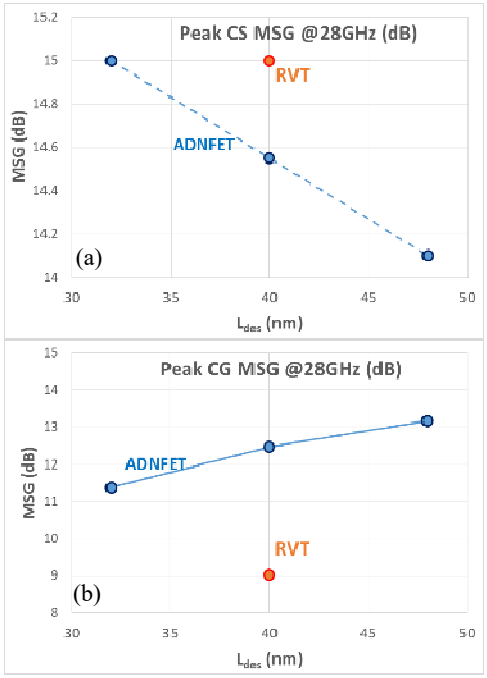

Fig. 6: Comparison of the (a) peak common source and (b) peak common gate MSG of the RVT vs the ADNFET.

While the device was designed with a PA application in mind, we see it may work very well in an LNA application too. We have already seen the excellent g_m and g_{ds}. In addition, Fig. 7 shows that the reduced gate resistance leads to an improvement in the noise figure for the device compared to the RVT device.

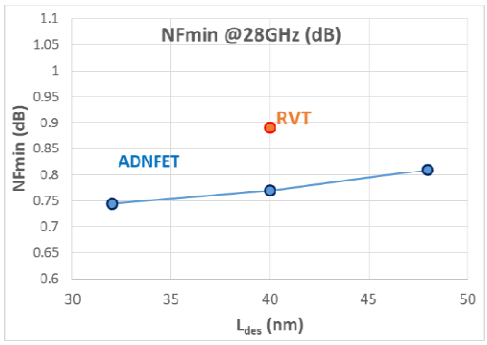

Fig 7: RVT vs ADNFET NFmin

D. *Reliability*

As mentioned earlier, key to increasing the output power of a PA is increasing the Vdd that the PA can support which translates to improved reliability for the devices comprising the PA. Internal evaluations suggest that FETs in a PA undergo maximum stress when the gate voltage swings low resulting in a high Vds across the device.

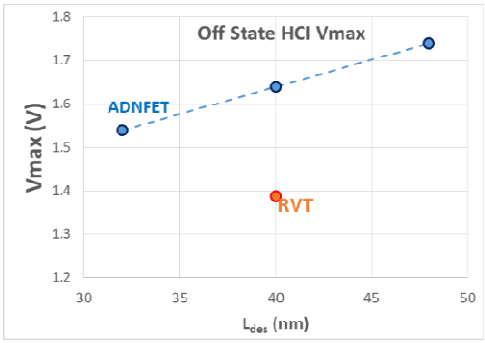

Fig 8: Off State HCI comparison between RVT and ADNFET.

Fig. 8 shows the OFF state HCI V_{max} of the ADNFET vs the RVT device. While the exact stress seen in the device depends on the way the PA is designed and operated, the OFF state HCI (maximum Vd @ Vg=0 V that results in 10% Idsat shift at 125ºC) is a good metric of the ability of the device to withstand high voltages during PA operation. We observe as much as a 22% increase in the HCI V_{max}. This improvement in the reliability of the device is also observed during RF stress under a continuous wave (CW) condition at 28 GHz.

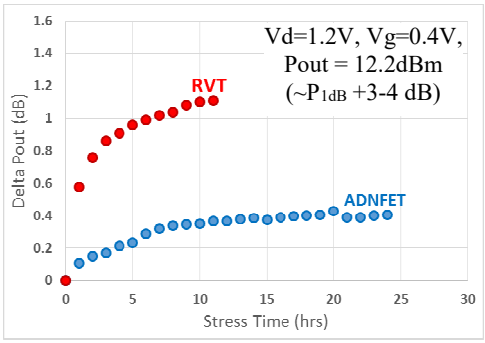

Fig 9: Comparison of the Psat degradation of the RVT and the ADNFET when stressed at high DC and RF CW stress conditions.

Fig. 9 shows a comparison of the P_{sat} degradation of the ADNFET vs the RVT device when stressed using a CW signal at 28GHz. Both devices were biased with the same bais conditions. The input and output impedances of the device were individually tuned using a load-pull (LP) tuner to maximize peak power added efficiency (PAE). Fresh devices were then stressed at a fixed output power of 12.2 dBm (close to or above the Psat of the devices) and the shift in Psat was measured as a function of the stress time. It is worth noting that this is a highly accelerated stress with the peak voltages reaching more than 2X the applied Vdd. The ADNFET shows significantly lower degradation in Psat compared to the RVT device. It is clear that the ADNFET demonstrates reduced degradation under both DC and RF stresses.

E. Large signal and Power Amplifier results

Finally, we report on the large signal performance of the devices in a common source configuration at 28 GHz. As before the devices were tuned to optimize the maximum PAE during the LP testing. Shown in Fig. 10 (a) is a comparison of the P_{1dB} of the RVT vs the ADNFET. We observe as much as a 2 dB increase in P_{1dB} when the Vdd is increased by ~ 20% (what we consider an equivalent reliability point). The peak PAE is similar to slightly improved (see Fig. 10 (b))

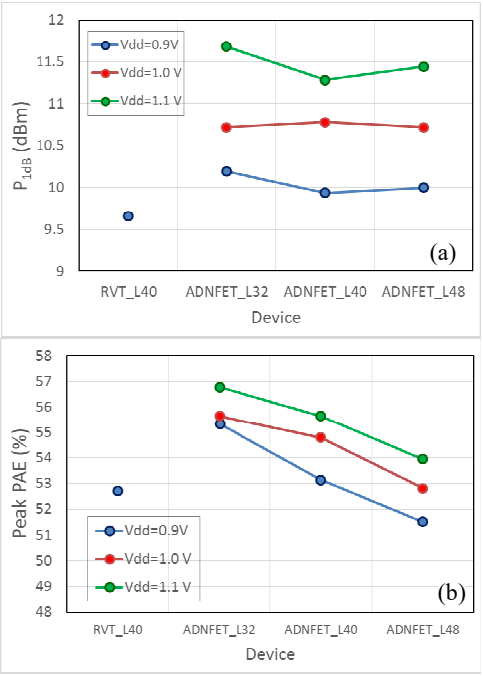

Fig 10: Large signal (a) P_{1dB} and (b) peak PAE for RVT (Vd=0.9V) vs ADNFET (L=32, 40 and 48 nm, Vdd=0.9, 10 and 1.1V).

A PA designed using the ADNFET was reported [7], demonstrating P_{sat}=18.9 dBm and peak PAE=45% using a differential pair 2-stack cascode topology. These are some of the best results reported for a simple differential pair PA design. In contrast to previous reported results, these were reported at a Vdd that showed minimal degradation during a ruggedness stress test.

II. Conclusion

This paper reports on the ADNFET, a new device custom designed for mmWave PA applications. It features excellent high frequency performance, a 20% improvement in voltage handling capability (V_{max}) and reduced V_{min} (through reduced external resistance). This improvement translates into demonstrated improvements in P_{1dB} and maximum PAE at a power cell level and was used to design a reliable PA with best in class P_{sat}, gain and PAE. It also features excellent g_m/g_{ds}, reduced gate resistance and NFmin making it a promising candidate for LNA applications.

Acknowledgements

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