3-D Simulation of Multiple-Gate Devices.

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Abstract
With transistors shrinking, problems such as short-channel effects are becoming a normal occurrence. In order to reduce this increase, and to obtain higher current drive, a good alternative is to implement the use of multiple-gate fully depleted SOI-MOSFET transistors. In this paper, we will show that these novel devices are able to overcome most of the problems and optimized operation can be obtained in the DC and AC regimes.

Introduction
Following the prediction of the Roadmap of the Semiconductor Industry Association (SIA) [1], MOS transistors will have gate lengths down to 25 nm by 2007 with the 65 nm nodes. For this technology node we expect degradation of transistors performances by short channel effects (SCE). Recent results published in [2] show that multiple-gate structures pose an exciting alternative to reduce the SCE. In the subthreshold region of operation, these multiple-gate devices have outstanding subthreshold swing (S) and low drain-induced barrier lowering (DIBL) values. Fig. 1 shows the various multiple-gate devices studied in this work. These multiple-gate MOS structures have been simulated with 3-D Atlas numerical software. The following models were considered; energy balance, physical models accounting for electric field dependent lifetime, transverse field dependent mobility, SRH recombination/regeneration and bandgap narrowing and carrier statistics.

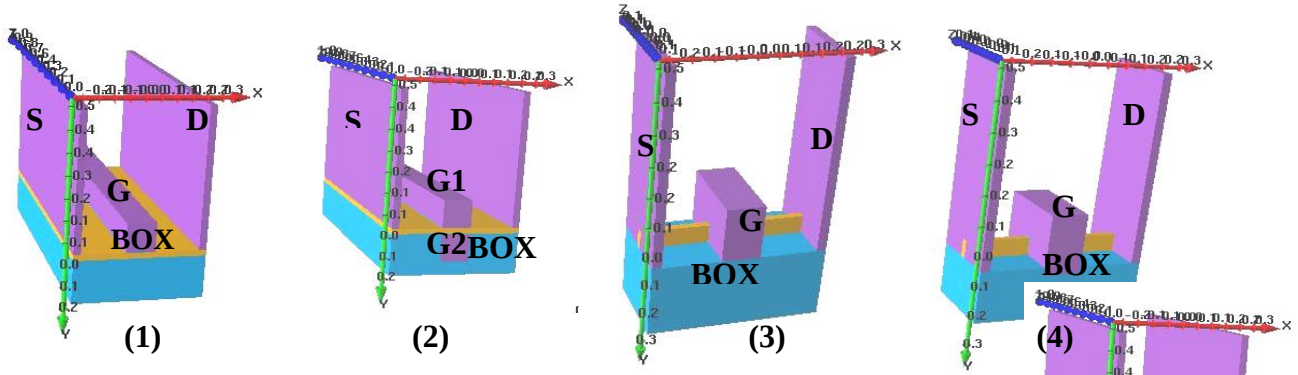

Figure 1: (1) Single-gate (2) Double-Gate (3) Triple-Gate and (4) Pi-Gate

Results and Conclusion

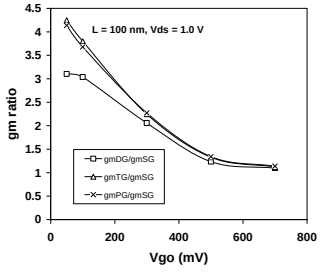

Fig. 2: g_m ratio for the various multiple gate and SG devices extracted at V_{ds} = 1.0 V.

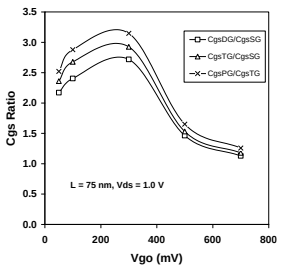

Fig. 3: Various C_{gs} ratio for various multiple gate and SG devices at V_{ds} = 1.0 V.

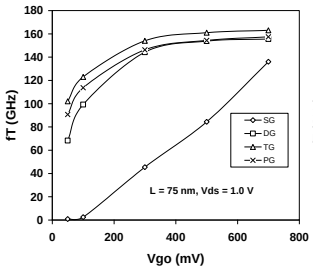

Fig. 4: f_T extracted for the multiple gate and SG devices extracted at V_{ds} = 1.0 V.

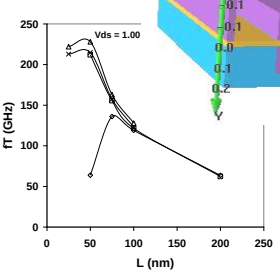

Fig. 5: f_T values for various multiple gate and SG devices extracted at V_{ds} = 1.0 V.

In Fig. 2, 3, 4 and 5, it is clear that the multiple gate devices show much superior properties compared to the SG devices. This improvement is noticed in both DC and AC operation modes. Multiple gate MOS devices exhibit great high frequency performances especially at low gate voltage overdrive (V_{go}) thanks to the voume inversion or quasi volume inversion regime. These devices are potential candidate for future consideration in the challenge to build smaller and faster devices.

References
[1] http://public.itrs.net/, The International Technology Roadmap for Semiconductors, 2001
[2] Jean-Pierre Colinge, "Multiple-gate SOI MOSFET's", Solid-State Electronics, Elsevier Ltd., 2004