Traps and Radio-Frequency Characterization of Polysilicon Layer on High Resistivity Silicon Substrate

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***Abstract* — In this work, radio-frequency and traps properties of unintentionally doped polycrystalline silicon (polySi) deposited by low pressure chemical vapor deposition (LPCVD) on high resistivity silicon (HR-Si) substrate are characterized. Both volume (i.e. inside polySi) and interface traps (i.e. near polySi/HR-Si) are detected by photo-induced current transient spectroscopy (PICTS). A thermal budget of 900°C during 2 hours is sufficient to observe trap densities reduction near the polySi/HR-Si interface, affecting the RF performance of the fabricated substrates.**

Index Terms — Radio-Frequency (RF), effective resistivity (ρ_{eff}), second harmonic power (H2), figure of merit (FoM), photo-induced current transient spectroscopy (PICTS), trap-rich (TR), polycrystalline silicon (polySi), grain boundary (GB), low pressure chemical vapor deposition (LPCVD), boron contamination.

I. Introduction

The formation of the parasitic surface conduction (PSC) layer below the silicon dioxide (SiO_2) of a Silicon-on-Insulator (SOI) structure is detrimental for the SOI radio-frequency (RF) behavior as it decreases the substrate effective resistivity (ρ_{eff} [Ω.cm]) [1] while increasing the power of the harmonic distortions (H2, H3 [dBm]) which are two important RF figures of merit (FoM) [2], [3], [4]. This PSC layer can be induced by the presence of positive oxide charges Q_{ox}^{+} inside the SiO_2, the metal-semiconductor work function ϕ_{ms}, or simply due to the application of a DC bias on the top part of the SOI substrate. Introduction of traps through the deposition of a trap-rich (TR) layer – usually made of unintentionally doped polycrystalline silicon (polySi) – between the SiO_2 and the high-resistivity Si (HR-Si) handle wafer is an efficient solution to prevent the formation of this PSC by the mechanism of Fermi level pinning (FLP) [5], [6], [7], [8].

From a technological point of view, two parameters can limit the efficiency of the TR layer. The first one is unwanted contamination (especially boron) by the environment of the clean room during the layer deposition. The second obstacle is that the TR layer should be thermally stable enough to prevent recrystallization during the SOI wafer manufacturing thermal-steps [9], [10].

Even if there is a lot of interest in this material, trap properties like trap energy level introduced by such deposition process are not well known. This is due to the presence of FLP, high traps concentration and low carrier density, preventing the use of capacitive or electrical injection based techniques, such as thermal admittance spectroscopy [11] or deep level transient spectroscopy (DLTS) [12]. To overcome this problem, we applied photo-induced current transient spectroscopy (PICTS) to characterize such resistive layers [13], [14]. In PICTS, traps are filled by illumination following which the relaxation current is monitored to extract traps parameters such as the activation energy E_A [eV] and the capture cross-section σ_t [cm^2].

In this paper, we focus on a non-industrial TR layer (made of polySi) obtained by low pressure chemical vapor deposition (LPCVD) and study the effect of annealing on the extracted traps. Prior to this PICTS study, we introduce the morphology analysis of the deposited polySi, unwanted doping and the resistivity depth profile. These complementary studies are helpful in order to interpret ρ_{eff} and H2 results for the fabricated polySi/HR-Si substrates.

II. Experimental Details

A. Samples preparation

The substrates were prepared in the clean room facilities of CEA-Leti (Grenoble, France). Unintentionally doped polySi was deposited by LPCVD using SiH_4 as precursor, at 620°C and 220 mTorr on p-type HR-Si substrates with nominal resistivity

$\rho_{Si} \approx 5.5$ kΩ.cm (corresponding to $N_A \approx 3.25 \times 10^{12}$ at.cm^{-3}). Due to equipment constraint, polySi was obtained by two deposition steps: a first layer of 1 µm-thick followed by a second one of 0.65 µm, for a total thickness $t_{polySi} = 1.65$ µm. Then, polysilicon surface was planarized using chemical-mechanical polishing (CMP). The samples were then annealed at 900°C (T900) for 2 hours in N_2 in order to test the thermal stability of the structure. Two references were used: T0 with no anneal, and HR0 without TR nor anneal.

For RF measurement, a 400 nm-thick silicon dioxide was deposited by plasma enhanced chemical vapor deposition (PECVD) of tetraethyl orthosilicate (TEOS) at 480°C on top of the wafers. Then, Coplanar Waveguide (CPW) line structures – made of Al with a thickness of approximately 0.75 µm – were patterned. An illustration of the RF structure is shown in **Fig. 1**(a) (front view) and (c) (top view). The width of the central line S is equal to 26 µm, two planar ground lines G are of 280 µm-wide each and the distance between S and G lines equals 12 µm. The total length of the CPW structure is 2 mm. The CPW structures were fabricated at Winfab clean room facilities from UCLouvain.

Schottky barrier diodes (SBD) were prepared for PICTS measurement by thermal evaporation of a 10 nm-thick Ti semi-transparent [15], [16] circular contact using an MEB550 evaporator from Plassys. Surface cleaning was performed using solvents, Standard Clean 1 (SC-1) and hydrofluoric acid. Then, the samples were mounted on a ceramic (Al_2O_3) substrate. Silver paste was used for the back electrical contact, after surface scratching with a diamond tip. A representation of the samples (without ceramic substrate) is shown in **Fig. 1**(b).

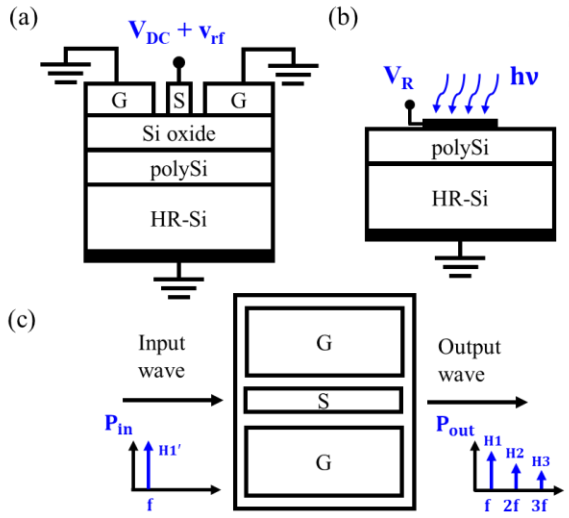

Fig. 1. Representation of the structures (side view) used for (a) RF and (b) PICTS measurement. (c) Illustration on the principle of RF measurement for the extraction of harmonic distortion.

B. Set-up description

RF measurements (ρ_{eff} and H2) were performed at UCLouvain (Louvain-la-Neuve, Belgium) using a PNA-X 2-port vector network analyzer (VNA) from Keysight. During measurement, a sine wave with an input bias of $V_{DC} + v_{rf}$ [V], frequency f [Hz] and power P_{in} [dBm] is applied at the input of S line while G lines were grounded (**Fig. 1**(a) and (c)). V_{DC} is the DC and v_{rf} the AC voltage of the input signal. Substrate non-linearity was extracted through the second harmonic component H2 (2 x f) of the output signal of power P_{out} [dBm] at the end of the CPW lines for $P_{in} = 15$ dBm and f = 900 MHz.

PICTS measurement was performed using an FT1030 Fourier DLTS system from PhysTech where the sample is introduced inside a cryostat. The tested material is submitted to a reverse bias V_R (**Fig. 1**(b)). Two light emitting diode (LED) from Thorlabs – whose beam was focused with an optical column – are employed to generate electron-hole pairs inside the sample. Three parameters characterize each LED: the wavelength λ, the pulse voltage V_P and the filling time t_p. LED illumination power is an increasing function of V_p. For the first LED, λ is equal to 430 nm (corresponding to a photon energy E_{ph} of 2.88 eV) and V_p can vary from 0 to 5 V (corresponding to a maximum optical power of 600 mW). For the second LED, λ is 940 nm ($E_{ph} = 1.32$ eV) and V_p ranges between 0 and 10 V (1,000 mW). Also, the number of photons received in the sample for each λ was not evaluated. For this study, we fixed $V_p = 1$ V when λ = 940 nm and 5 V for 430 nm.

The relaxation current is recorded between times t_0 and $t_0 + T_w$, t_0 being the cut-off time and T_w the measurement period. Finally, a Fast Fourier Transform (FFT) algorithm is employed to extract the different Fourier coefficients a_n and b_n [17]. In this paper, PICTS spectra are represented using b_1 coefficient with $t_0 = 5$ ms and $T_w = 100$ ms. Each measurement was performed between 50 and 300 K, in heating up mode. More information about the PICTS set up can be found in [18]. Like for DLTS, in a PICTS spectrum, traps electrical responses manifest as peaks whose temperature position depends on associated E_A and σ_t. Contrary to DLTS, there is no simple formula to relate peak amplitude to trap concentration N_t so we did not extract the trap density.

To assess polySi morphology, transmission electron microscopy (TEM) observations were performed by Serma Technologies (Grenoble, France) with a Tecnai Osiris (S/TEM 200 kV) from FEI. Boron and phosphorus contaminations were checked by Probion Analysis using an IMS 6f secondary ion mass spectrometer (SIMS) from Cameca. Finally, polysilicon resistivity and carrier polarity profiles as a function of depth were obtained from scanning resistance profiling (SRP) measurement realized by Solecon Laboratories (Reno, USA).

III. RF Performances of Fabricated Substrates

The effective resistivity ρ_{eff} (a) and the second harmonic power H2 (b) as a function of V_{DC}, measured for HR0, T0 and T900 samples, are shown in **Fig. 2**.

Regarding HR0 sample, ρ_{eff} is only equal to 35 Ω.cm despite using a HR-Si substrate with a nominal resistivity $\rho_{Si} \approx 5.5$ kΩ.cm (a). H2 (b) varies between -50 and -60 dBm for -15 V ≤ V_{DC} ≤ 15 V. Those high values are due to the presence of the PSC layer below the buried oxide, conductive enough to strongly degrade the substrate resistivity and linearity seen by CPW lines.

For the sample including a TR layer (HR0 → T0), ρ_{eff} attains a value of 23 kΩ.cm (a) and H2 decreases to -95 dBm (b). Moreover, H2 becomes nearly bias independent. This is due to the presence of the TR layer preventing the formation of the PSC layer.

After the 900°C anneal (T0 → T900), ρ_{eff} decreases by nearly a factor of two (a) while H2 rises by 10 dB (b). Both quantities are independent of V_{DC} between -15 and 15 V.

Those RF FoMs are discussed in the following sections, based on TEM, SIMS, SRP and PICTS measurement results.

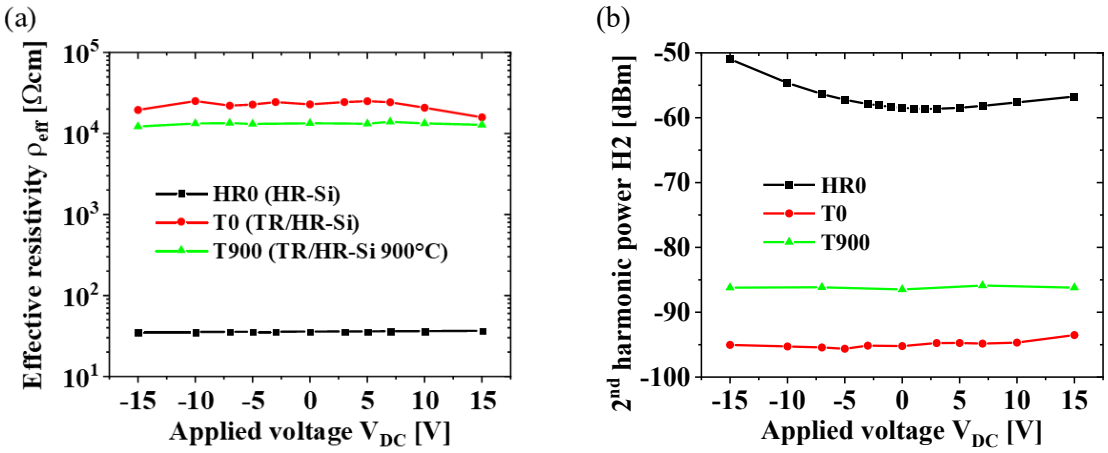

Fig. 2. (a) Effective resistivity ρ_{eff} and (b) second harmonic power H2 as a function of applied voltage V_{DC} for samples HR0, T0 and T900. In (b), measurement parameters were P_{in} = 15 dBm and f = 900 MHz.

IV. Physical and Electrical Properties of Polysilicon Layer

A. PolySi morphology

Fig. 3 depicts the TR layer morphology obtained by TEM imaging for TR/HR-Si samples (T0 and T900). As can be observed in (a), grains inside the polySi are columnar with an average width of 100 nm. In (b), we notice no major change in the morphology of polySi.

This result aligns with Raman spectroscopy measurements (not shown), which reveal a crystalline-to-amorphous ratio of approximately 78% / 22% for the as-deposited sample (T0), and 83% / 17% for the annealed sample (T900). These values indicate that the deposition temperature used for T0 is already sufficient to produce a highly crystalline film, with only a modest increase in crystallinity observed after annealing. Consequently, the microstructure of both polySi layers is very similar, as confirmed by TEM images (**Fig. 3**). For both samples, the amorphous fraction observed by Raman spectroscopy is likely associated with structural disorder at grain boundaries.

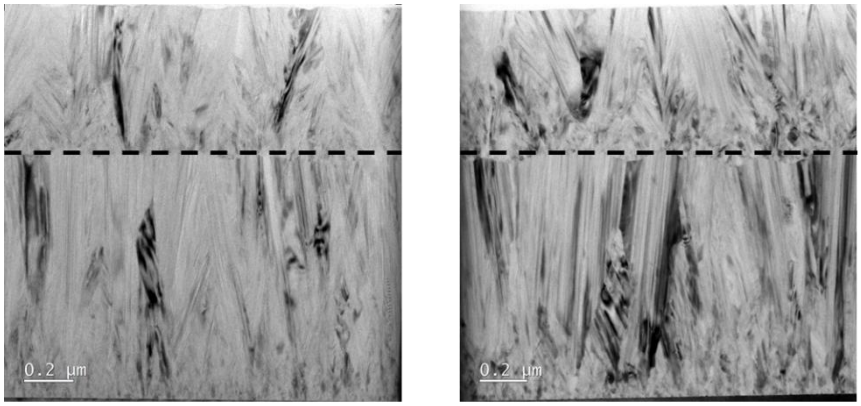

Fig. 3. TEM pictures of the LPCVD polySi for (a) T0 and (b) T900 samples. Scale: 0.2 µm. Dashed lines: polySi/polySi interface.

B. Boron and phosphorus contamination

The diffusion of unwanted (a) boron and (b) phosphorus atoms into the polysilicon layer during annealing has been characterized and is shown in **Fig. 4**. The boron (phosphorus) SIMS detection threshold is equal to 3 x 10^{13} (1.4 x 10^{15}) at.cm^{-3}.

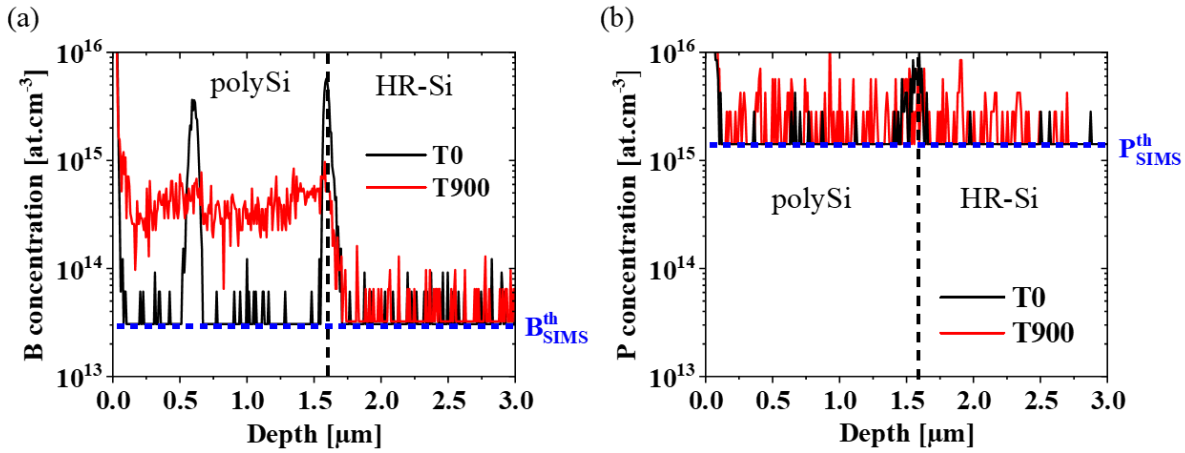

Fig. 4. SIMS concentration of (a) boron and (b) phosphorus as a function of depth for T0 and T900 substrates. Undesirable integrated B dose for each sample is 5.9 x 10^{10} (T0) and 6.7 x 10^{10} at.cm^{-2} (T900). P dose was not estimated. Dashed lines: polySi/HR-Si interface.

In **Fig. 4**(a), for T0, we observe two boron peaks with 5 x 10^{15} at.cm^{-3} of concentration near 0.6 and 0.6 µm, respectively. The location of those two peaks should be related to the polySi deposition in two steps. The boron contamination source originates from the cleanroom's filtration system. During the 900°C annealing step (T900), boron diffuses into the polySi, reaching a concentration of 4 x 10^{14} at.cm^{-3}. Both T0 and T900 were contaminated with similar boron doses: 5.9 x 10^{10} and 6.7 x 10^{10} at.cm^{-2}, respectively.

Phosphorus SIMS results are more difficult to analyze because of the higher SIMS detection threshold (**Fig. 4**(b)). Nevertheless, it can be seen that phosphorus contamination is also present at the polySi/HR-Si interface (and possibly at the polySi/polySi interface) for T0. During the 900°C annealing step (T900), phosphorus also diffuses into the polySi (inset of **Fig. 4**(b)) even if the final P concentration is difficult to assess.

C. PolySi resistivity

SRP measured for T0 and T900 is shown in **Fig. 5**. Before annealing, polySi resistivity increases from 10^4 Ω.cm near the polySi/HR-Si interface to approximately 10^5 Ω.cm close to the surface. This high polySi resistivity, despite the observed boron peaks at the interfaces (**Fig. 4**(a)) means either that introduced boron is electrically inactive or that all dopant-generated carriers have been captured by traps.

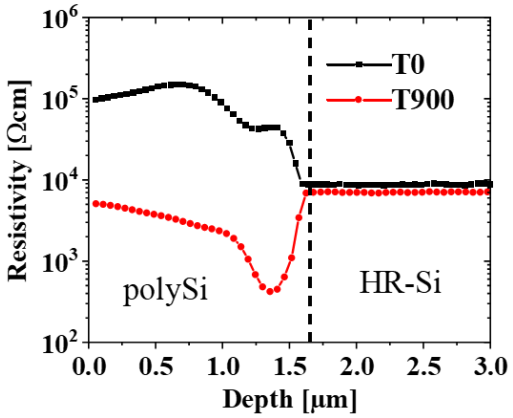

Fig. 5. Resistivity as a function of depth for T0 and T900 substrates. Dashed lines: polySi/HR-Si interface.

After the 900°C anneal, polySi resistivity falls by at least one order of magnitude and becomes lower than that of HR-Si. The highest drop is located near a depth of 1.35 µm, close to the polySi/HR-Si interface, where ρ ≈ 420 Ω.cm. It is worth mentioning that the conductivity type measured during SRP (hot probe, not shown) is *p*, meaning that boron contamination is more important than phosphorus one in that sample.

V. Traps Properties of the PolySi Layer

A. PICTS spectrum study of T0 sample

1) Traps detection and spatial localization

The PICTS spectrum, measured from t_p = 50 µs to 20 ms when V_R = 10 V and λ = 940 nm, is shown in **Fig. 6**. At least two peaks are present: 1P whose maximum is located near 269 K and αP lying near 140 K. A third peak (2P) is also present at the low temperature shoulder of 1P. Spectrum saturation is reached at around t_p = 10 ms (inset of **Fig. 6**). 1P and 2P peaks are likely related to discrete levels inside polySi bandgap (see discussion in Section V.A.2). We believe that αP originates from a trap with an energy level continuously distributed in the gap and its maximum moves to lower temperatures (from 160 to 140 K) when t_p increases (inset of **Fig. 6**).

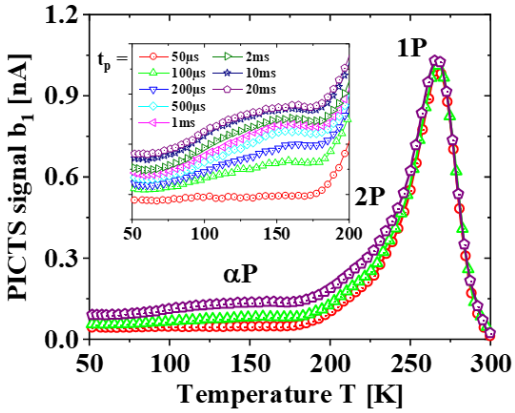

Fig. 6. Effect of t_p on PICTS spectrum of T0 sample. Inset: focus on peak αP between 50 and 200 K. Measurement conditions are V_R = 10 V, λ = 940 nm and V_p = 1 V.

The spatial localization of traps can be studied by varying λ during the measurement. This is illustrated in **Fig. 7** for two wavelengths: 430 and 940 nm, at t_p = 20 ms (for saturation conditions). We observe that 1P and 2P peaks are detected, whatever illumination conditions. This is not the case for αP, visible only when λ = 940 nm. This difference can be explained by the different light penetration depths α^{-1} in polySi, associated to each LED. When λ = 940 (430nm) nm, α^{-1} is close to 6 µm (100 nm) in polySi [19] (inset of **Fig. 7**). Since $\alpha_{940nm}^{-1} \gg t_{polySi}$, carriers are photo-generated throughout the entire TR layer. In the second case, $\alpha_{430nm}^{-1} \ll t_{polySi}$ and electron-hole pairs are only present in the upper part of the polySi layer.

It means that 1P and 2P peaks are associated to polySi volume traps, while αP, detected only when λ = 940 nm, seems to be associated with one of the two interfaces: polySi/polySi or polySi/HR-Si. It cannot be related to an HR-Si bulk defect since it was not detected on a bare HR-Si substrate (not shown). As it will be demonstrated in Section VI, we can suppose that this signal comes from the polySi/HR-Si interface.

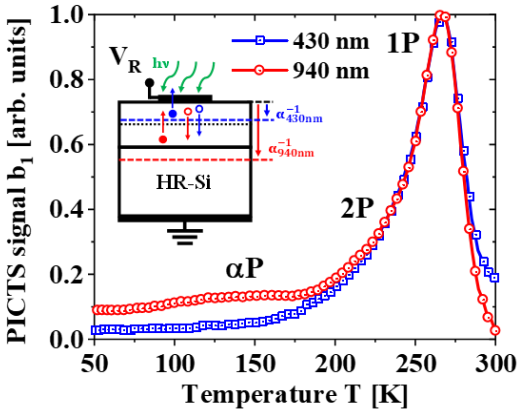

Fig. 7. Effect of λ on the PICTS spectrum of T0 sample when V_R = 10 V and t_p = 20 ms. Inset: illustration of the penetration depths α^{-1} inside the polySi/HR-Si structure.

2) Traps parameters extraction and modeling

For sufficiently low t_p, it is possible to separate 1P and 2P contributions. This is illustrated in **Fig. 8** when λ = 430 nm, V_p = 5 V and t_p = 20 µs. Associated Arrhenius plots for those defects are shown in the inset and extracted traps parameters are reported in **Table 1**. Because both carrier types are injected during PICTS measurement, there is an ambiguity concerning the captured carrier type for each trap (i.e. whether one is an electron or a hole trap). Consequently, we indicated both σ_n for electron and σ_p for hole traps. 1P (2P) associated trap has an activation energy of 0.49 (0.40) eV and $\sigma_n = 10^{-15}$ (5.3×10^{-16}) cm^2.

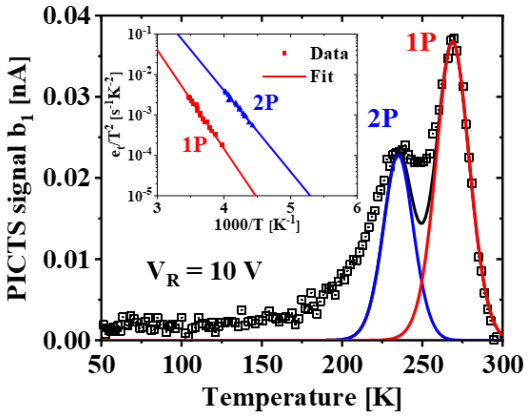

Fig. 8. PICTS spectrum of T0 sample when V_R = 10 V, λ = 430 nm and t_p = 20 µs. Two peaks: 1P and 2P are visible from 200 to 300 K and their Arrhenius plot are shown in the inset. Peak modeling using the discrete trap model of [17] is also presented.

In **Fig. 8**, we observe that 1P peak is well modeled with a discrete trap model from [17]. 2P is too broad to be represented by a single level in the polySi bandgap. It could mean that 2P associated trap is not discrete but has a larger energy distribution in the gap (e.g. Gaussian distribution [20], [21]). Another possibility is that 2P is linked to a sum of closely spaced discrete levels. We think the second hypothesis is valid because it is possible to model PICTS spectra between 200 and 300 K using the same set of discrete trap levels.

This result is shown in **Fig. 9** on two spectra measured for t_p = 20 µs and 1 ms when λ = 430 nm. In all fitted curves, only the amplitude of each peak is allowed to change, the position for each peak is the same for all curves. Four peaks, named 1P, 2Pa, 2Pb and 2Pc, are sufficient to model the spectrum. Fitting parameters are summarized in **Table 1**. Peak 2P was separated in three peaks called 2Pa, 2Pb and 2Pc. 2Pb was modeled with the same trap parameters (E_A, σ_t) as 2P. We made the hypothesis that 2Pa and 2Pc's capture cross-sections were the same and equal to σ_t^{2P}, which yields E_A^{2Pa} = 0.38 eV, E_A^{2Pb} = 0.41 eV and E_A^{2Pc} = 0.44 eV.

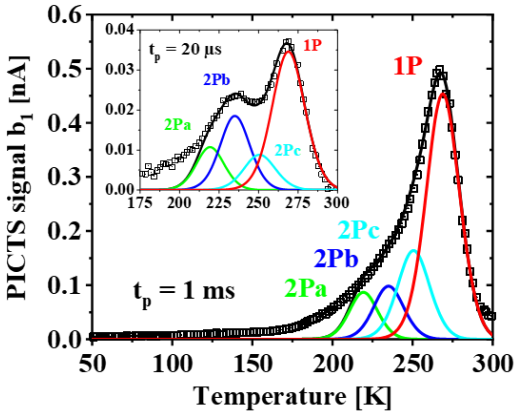

Fig. 9. Curve fitting of T0 PICTS spectrum from 200 to 300 K for t_p = 20 µs (inset) and 1 ms when λ = 430 nm. Four discrete peaks (1P, 2Pa, 2Pb and 2Pc) are used to model the spectrum.

	Extraction method	T_{peak} [K]	E_A [eV]	σ_n [cm^2]	σ_p [cm^2]	Localization
1P	Arrhenius plot	269	0.485 ± 0.015	1.0 ± 0.1 x 10^{-15}	3.3 ± 0.2 x 10^{-16}	polySi
2P	Arrhenius plot	≈ 235	0.399 ± 0.015	5.3 ± 0.3 x 10^{-16}	1.7 ± 0.1 x 10^{-16}	polySi
2Pa	Curve fitting	219	0.38	5.3 x 10^{-16}	1.7 x 10^{-16}	polySi
2Pb	Curve fitting	235	0.41	5.3 x 10^{-16}	1.7 x 10^{-16}	polySi
2Pc	Curve fitting	251	0.44	5.3 x 10^{-16}	1.7 x 10^{-16}	polySi

Table 1. Traps parameters associated with T0 and T900 samples. T_{peak} is only valid when t_0 = 5 ms and T_w = 100 ms.

B. Evolution of detected traps with anneal

The effect of anneal on the PICTS spectrum of LPCVD polySi is shown in **Fig. 10** for (a) T0 and (b) T900 when V_R = 10 V and λ = 940 nm. Filling time was chosen in such a way that bulk traps (from 200 to 300 K) are saturated. Curve fitting for the different discrete levels are also shown, using traps parameters of **Table 1**.

T900 spectrum envelope is also well modeled using the discrete traps parameters determined for T0 sample. Only relative peak intensities in each spectrum have changed. This suggests that neither the annealing process nor contamination (**Fig. 4**) altered the trap signature of the detected traps (i.e. the peak position), meaning that these are the same defects. This is corroborated by the similar saturation times observed for both volume traps – around 80-100 µs for both samples – indicating that the capture cross-section of these traps did not change during annealing. However, the reduction in peak intensities implies that the annealing process has affected the concentration of the traps.

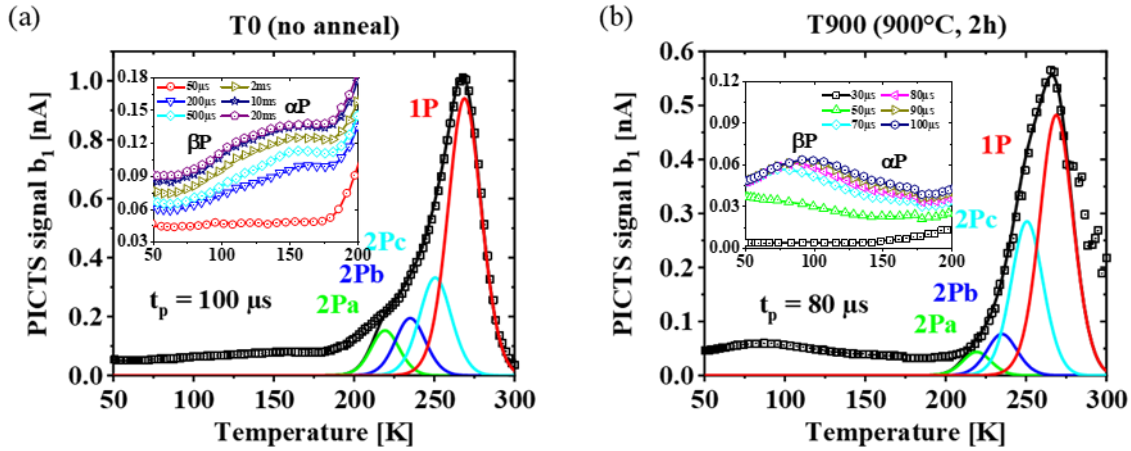

Fig. 10. PICTS spectra measured on (a) T0 and (b) T900. Other measurement conditions are V_R = 10 V and λ = 940 nm. Curve fitting for 1P, 2Pa, 2Pb and 2Pc is also shown. Inset: evolution of (a) T0 and (b) T900 polySi/HR-Si interface traps contribution as a function of t_p.

The evolution of interface traps (T < 200 K) with anneal is illustrated in the insets of **Fig. 10**. In (a), a large peak labeled αP is observed and saturates for a t_p close to 10 ms. In (b), αP is significantly reduced and another defect, labeled βP, is dominant near 100 K. The peak position of βP shifts by about 30 K between t_p = 50 and 100 µs, meaning it should also be a trap with energy continuously distributed in the gap [22], [23].

From the relative intensities observed in both spectra, it is likely that βP was already present in the T0 sample but masked by the much stronger αP signal. In T900, βP reaches an amplitude of approximately 0.06 nA, while in T0, the total PICTS signal in the same temperature range is around 0.11 nA, suggesting a possible superposition of αP and βP. In T0, αP likely extends down to at least 100 K and the peak saturation time is that of αP, around 10 ms, whereas βP saturates near 80 µs in T900 – two order of magnitude lower.

These observations indicate that the interface traps are composed of at least two distinct defects: αP and βP. The annealing process affects them differently: αP shows a stronger reduction in intensity after the 900°C treatment than βP, suggesting a different origin or passivation mechanism. It would be valuable to study the exact energy distribution of αP and βP, as was done for volume traps 1P and 2P.

The annealing result presented in **Fig. 10** is particularly noteworthy because no apparent morphological modification was observed within the polySi volume, or at the polySi/polySi and polySi/HR-Si interfaces in the TEM images shown in **Fig. 3**. Further insight into the nature and passivation mechanisms of these traps would require a more detailed investigation, including variations in process conditions (e.g., polySi deposition parameters, annealing conditions, or other fabrication-related steps), and/or correlation with complementary characterization techniques.

VI. Discussion

A. About the origin of detected volume traps

In the literature, the electrical activity of grain boundaries (GB) inside Si has been studied by several means:

- in a polySi, where GBs are naturally present [24], [25], [26], [27], [28];
- on a bi-crystal with a unique GB [29], [30], [31];
- on two bonded Si with different crystallographic orientations creating also a unique GB [32], [33].

In the first case, depending on the size of the electrodes relatively to the grain size, it is possible to isolate the electrical contribution of a unique GB [24], [25]. Otherwise, the trap activity consists on a sum of the different GBs participating in the monitored current [26], [27], [28].

Several studies show that the origin of GB electrical activity is complex and depends on both intrinsic and extrinsic parameters [34], [35]. Intrinsic parameters are related to the structure of the GB itself: GB plan orientation and misorientation angle. Those two parameters define the electronic structure of the GB through the presence of dangling and distorted bonds. Dangling bonds introduce deep levels inside the Si bandgap. Distorted bonds do not directly introduce deep levels but can attract contaminants (e.g. Fe, Au or Cu) by acting like a potential well. Those contaminants, with their associated deep levels, will give an extrinsic contribution to the GB electrical activity [30], [36], [37].

By comparing our results in the inset of **Fig. 8** with the literature associated to GBs or deposited polySi, it was found that 1P trap signature could correspond to the level signature detected by [24] for a particular GB structure (Σ9 in [24]) inside polySi. This defect is a hole trap with an activation energy of 0.51 eV and a capture cross-section associated to holes of 2.7×10^{-15} cm^{-2}. By careful TEM investigations, [38] also highlighted the importance of both Σ3 twins (or nanotwins) and Σ9 grain boundaries to the substrate RF performances. Even if no correspondence was found for the other detected levels in the literature, a plausible hypothesis for the remaining detected levels in T0 (and T900) is that they are related to different grain or twin boundaries structures as there are no other sources of defects.

B. About T0 and T900 RF performances

T0 RF performances are explained through polySi deposition that introduces several deep levels (1P, 2Pa, 2Pb and 2Pc peaks) inside the Si bandgap. Those traps pin the Fermi level inside the TR layer in close vicinity with those defects' energies. This prevents the formation of the PSC layer that strongly degrades both ρ_{eff} and H2 FoM (**Fig. 2** for HR0). Moreover, because of FLP, both ρ_{eff} and H2 are nearly independent of the applied V_{DC}.

After 900°C anneal, the trap density is still sufficient to ensure FLP, as demonstrated by H2's independence to V_{DC} (**Fig. 2**). Observed RF performance degradation can be explained by combining SIMS (**Fig. 4**), SRP (**Fig. 5**) and PICTS (**Fig. 10**) data. SIMS shows uniform boron contamination in the TR layer. SRP exhibits a stronger resistivity reduction close to the polySi/HR-Si interface than in the polySi volume, suggesting a larger trap density reduction near the polySi/HR-Si interface. PICTS measurements revealed that both volume and interface traps densities inside the polySi layer were reduced. Those observations support the idea that αP and βP peaks originate near or at the polySi/HR-Si interface, and not from the polySi/polySi one. Moreover, [38] also shows a distinct family of defects composed of nanosized grains (< 100 nm) just above the polySi/HR-Si interface, contrasting with the larger grains (ranging from 100 nm to 1 µm) present in the polySi volume. Maybe it is possible that those nanosized grains annealed faster than the larger grains, degrading SRP resistivity close to the interface.

T900 RF performance can thus be understood by separating the TR contribution in two parts:

- Inside polySi, near to the TR/oxide interface: volume traps density is still high enough for FLP, despite introduced contamination, and ensures that both ρ_{eff} and H2 are V_{DC} independent (**Fig. 2**);

- Close to the polySi/HR-Si interface: interface traps and volume traps densities are not important enough to counterbalance free holes coming from boron doping and a conductive layer is present. This conductive layer leads ρ_{eff} (H2) to lower (higher) values.

A similar result was observed in [39], [40] for a boron contaminated polySi (after anneal) and was reproduced by RF simulations considering both FLP inside the TR layer and the presence of a conductive layer at the TR/HR-Si interface.

VII. Conclusion

Several TR/HR-Si RF substrates with different thermal budgets and contamination levels have been characterized by associating different measurement techniques giving complementary information on the polySi layer such as morphology (TEM), contamination (SIMS), resistivity (SRP) and traps (PICTS).

By varying light penetration depth, two traps' populations were detected by PICTS: deep levels near the polySi/HR-Si interface and deep levels inside the polySi volume. Trap parameters (E_A and σ_t) were determined by both peak position and curve fitting. Detected levels were attributed to different grain boundaries obtained by the polySi deposition process. For interface traps, a 900°C anneal is sufficient to observe an important density reduction of this defect population. A similar result was also observed by SRP measurement. This non-uniform trap density reduction, in addition to boron and phosphorus contamination, explains TR/HR-Si RF performances for different annealing steps (no anneal and 900°C, 2 hours).

To conclude, we showed that PICTS gives complementary results to the usually applied TEM, SIMS and SRP techniques to help us explain TR/HR-Si RF behavior. PICTS non-quantitative aspect for N_t determination could be overcome by curve fitting between RF measurement and TCAD simulation.

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References

[1] D. Lederer et J.-P. Raskin, « Effective resistivity of fully-processed SOI substrates », *Solid-State Electron.*, vol. 49, nº 3, p. 491-496, mars 2005, doi: 10.1016/j.sse.2004.12.003.
[2] A. C. Reyes, S. M. El-Ghazaly, S. J. Dorn, M. Dydyk, D. K. Schroder, et H. Patterson, « Coplanar waveguides and microwave inductors on silicon substrates », *IEEE Trans. Microw. Theory Tech.*, vol. 43, nº 9, p. 2016-2022, sept. 1995, doi: 10.1109/22.414534.
[3] D. C. Kerr, J. M. Gering, T. G. McKay, M. S. Carroll, C. R. Neve, et J.-P. Raskin, « Identification of RF Harmonic Distortion on Si Substrates and its Reduction Using a Trap-Rich Layer », in *2008 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, janv. 2008, p. 151-154. doi: 10.1109/SMIC.2008.44.
[4] Y. Wu, S. Gamble, B. M. Armstrong, V. F. Fusco, et J. A. C. Stewart, « SiO2 interface layer effects on microwave loss of high-resistivity CPW line », *IEEE Microw. Guid. Wave Lett.*, vol. 9, nº 1, p. 10-12, janv. 1999, doi: 10.1109/75.752108.
[5] H. S. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, et J. A. C. Stewart, « Low-loss CPW lines on surface stabilized high-resistivity silicon », *IEEE Microw. Guid. Wave Lett.*, vol. 9, nº 10, p. 395-397, oct. 1999, doi: 10.1109/75.798027.
[6] D. Lederer et J.-P. Raskin, « New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity », *IEEE Electron Device Lett.*, vol. 26, nº 11, p. 805-807, nov. 2005, doi: 10.1109/LED.2005.857730.
[7] C. Roda Neve et J.-P. Raskin, « RF Harmonic Distortion of CPW Lines on HR-Si and Trap-Rich HR-Si Substrates », *IEEE Trans. Electron Devices*, vol. 59, nº 4, p. 924-932, avr. 2012, doi: 10.1109/TED.2012.2183598.
[8] L. Zhu *et al.*, « RF performance of passive components on state-of-art trap rich silicon-on-insulator substrates », in *2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, avr. 2016, p. 1-2. doi: 10.1109/VLSI-TSA.2016.7480530.
[9] C. R. Neve *et al.*, « RF and linear performance of commercial 200 mm trap-rich HR-SOI wafers for SoC applications », in *2013 IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, janv. 2013, p. 15-17. doi: 10.1109/SiRF.2013.6489417.
[10] L. Zhu *et al.*, « Effects of Low Boron Concentration on Electrical Properties of Commercial Trap-Rich High Resistivity SOI Substrate », *ECS J. Solid State Sci. Technol.*, vol. 7, nº 2, p. P35, janv. 2018, doi: 10.1149/2.0061802jss.
[11] D. L. Losee, « Admittance spectroscopy of impurity levels in Schottky barriers », *J. Appl. Phys.*, vol. 46, nº 5, p. 2204-2214, mai 1975, doi: 10.1063/1.321865.
[12] D. V. Lang, « Deep-level transient spectroscopy: A new method to characterize traps in semiconductors », *J. Appl. Phys.*, vol. 45, nº 7, p. 3023-3032, juill. 1974, doi: 10.1063/1.1663719.
[13] G. M. Martin et D. Bois, « A New Technique for Spectroscopy of Deep Levels in Insulating Materials - Application to Study of Semi-Insulating GaAs », *Electrochem. Soc.*, vol. 78, p. 32-42, janv. 1978.
[14] Ch. Hurtes, M. Boulou, A. Mitonneau, et D. Bois, « Deep-level spectroscopy in high-resistivity materials », *Appl. Phys. Lett.*, vol. 32, nº 12, p. 821-823, juin 1978, doi: 10.1063/1.89929.
[15] A. Axelevitch, B. Gorenstein, et G. Golan, « Investigation of Optical Transmission in Thin Metal Films », *Phys. Procedia*, vol. 32, p. 1-13, janv. 2012, doi: 10.1016/j.phpro.2012.03.510.
[16] G. W. Hyung *et al.*, « Flexible Top-Emitting Organic Light-Emitting Diodes Using Semi-Transparent Multi-Metal Layers », *J. Nanosci. Nanotechnol.*, vol. 12, nº 7, p. 5444-5448, juill. 2012, doi: 10.1166/jnn.2012.6232.
[17] S. Weiss et R. Kassing, « Deep Level Transient Fourier Spectroscopy (DLTFS)—A technique for the analysis of deep level properties », *Solid-State Electron.*, vol. 31, nº 12, p. 1733-1742, déc. 1988, doi: 10.1016/0038-1101(88)90071-8.
[18] E. Vandermolen *et al.*, « Characterization and role of deep traps on the radio frequency performances of high resistivity substrates », *J. Appl. Phys.*, vol. 129, nº 21, p. 215701, juin 2021, doi: 10.1063/5.0045306.

[19] Y. Laghla et E. Scheid, « Optical study of undoped, B or P-doped polysilicon », *Thin Solid Films*, vol. 306, nº 1, p. 67-73, août 1997, doi: 10.1016/S0040-6090(97)00247-2.
[20] P. Omling, L. Samuelson, et H. G. Grimmeiss, « Deep level transient spectroscopy evaluation of nonexponential transients in semiconductor alloys », *J. Appl. Phys.*, vol. 54, nº 9, p. 5117-5122, sept. 1983, doi: 10.1063/1.332733.
[21] A. Das, V. A. Singh, et D. V. Lang, « Deep-level transient spectroscopy (DLTS) analysis of defect levels in semiconductor alloys », *Semicond. Sci. Technol.*, vol. 3, nº 12, p. 1177, déc. 1988, doi: 10.1088/0268-1242/3/12/005.
[22] K. Yamasaki, M. Yoshida, et T. Sugano, « Deep Level Transient Spectroscopy of Bulk Traps and Interface States in Si MOS Diodes », *Jpn. J. Appl. Phys.*, vol. 18, nº 1, p. 113, janv. 1979, doi: 10.1143/JJAP.18.113.
[23] N. M. Johnson, « Energy-resolved DLTS measurement of interface states in MIS structures », *Appl. Phys. Lett.*, vol. 34, nº 11, p. 802-804, juin 1979, doi: 10.1063/1.90650.
[24] J. Chen, E. Cornagliotti, E. Simoen, E. Hieckmann, J. Weber, et J. Poortmans, « A deep level transient spectroscopy study on the interface states across grain boundaries in multicrystalline silicon », *Phys. Status Solidi RRL – Rapid Res. Lett.*, vol. 5, nº 8, p. 277-279, août 2011, doi: 10.1002/pssr.201105225.
[25] T. Mchedlidze, M. Nacke, E. Hieckmann, et J. Weber, « On the capability of deep level transient spectroscopy for characterizing multi-crystalline silicon », *J. Appl. Phys.*, vol. 115, nº 1, p. 012006, janv. 2014, doi: 10.1063/1.4837997.
[26] W.-S. Kim, D. H. Kim, D. W. Kwak, D. W. Lee, Y. H. Lee, et H. Y. Cho, « Analysis of Deep-Level Defects on Proton Implanted Polycrystalline Silicon Thin Films Using Photoinduced Current Transient Spectroscopy », *Jpn. J. Appl. Phys.*, vol. 49, nº 12, p. 125802, déc. 2010, doi: 10.1143/JJAP.49.125802.
[27] P. C. Srivastava, J. C. Bourgoin, F. Rabajo, et J. Mimila Arroyo, « Transient capacitance spectroscopy in polycrystalline silicon », *J. Appl. Phys.*, vol. 53, nº 12, p. 8633-8638, déc. 1982, doi: 10.1063/1.330403.
[28] K. Knobloch, W. Seifert, et M. Kittler, « Application of scanning deep level transient spectroscopy for characterisation of multicrystalline silicon », *Mater. Sci. Eng. B*, vol. 42, nº 1, p. 254-259, déc. 1996, doi: 10.1016/S0921-5107(96)01717-5.
[29] A. Broniatowski, « Measurement of the grain-boundary states in semiconductors by deep-level transient spectroscopy », *Phys. Rev. B*, vol. 36, nº 11, p. 5895-5905, oct. 1987, doi: 10.1103/PhysRevB.36.5895.
[30] R. Rizk, X. Portier, G. Allais, et G. Nouet, « Electrical and structural studies of copper and nickel precipitates in a Σ=25 silicon bicrystal », *J. Appl. Phys.*, vol. 76, nº 2, p. 952-958, juill. 1994, doi: 10.1063/1.357773.
[31] Y. Ohno *et al.*, « Nanoscopic mechanism of Cu precipitation at small-angle tilt boundaries in Si », *Phys. Rev. B*, vol. 91, nº 23, p. 235315, juin 2015, doi: 10.1103/PhysRevB.91.235315.
[32] M. C. Wagener, M. Seacrist, et G. Rozgonyi, « Evaluation of Hybrid-Orientation (110)/(100) Direct Silicon Bonded Interfaces », *ECS Trans.*, vol. 11, nº 3, p. 25, sept. 2007, doi: 10.1149/1.2778647.
[33] X. Yu, J. Lu, et G. Rozgonyi, « Deep-level transient spectroscopy study on direct silicon bonded (110)/(100) interfacial grain boundary », *Semicond. Sci. Technol.*, vol. 23, nº 12, p. 125005, oct. 2008, doi: 10.1088/0268-1242/23/12/125005.
[34] C. R. M. Grovenor, « Grain boundaries in semiconductors », *J. Phys. C Solid State Phys.*, vol. 18, nº 21, p. 4079-4119, juill. 1985, doi: 10.1088/0022-3719/18/21/008.
[35] J.-L. Maurice, « On the origin of the electrical activity in silicon grain boundaries », *Rev. Phys. Appliquée*, vol. 22, nº 7, p. 613-621, juill. 1987, doi: 10.1051/rphysap:01987002207061300.
[36] R. Bakowskie, H. von Wenckstern, D. Lausch, M. Müller, K. Petter, et M. Grundmann, « Thermal admittance spectroscopy of multicrystalline silicon wafers and solar cells », in *Proceedings of the 24th EU-PVSEC*, 2009, p. 2100-2.
[37] X. Yu *et al.*, « Effect of Au contamination on the electrical characteristics of a “model” small-angle grain boundary in n-type direct silicon bonded wafer », *J. Appl. Phys.*, vol. 108, nº 5, p. 053719, sept. 2010, doi: 10.1063/1.3471817.
[38] L. Ding, J.-P. Raskin, G. Lumbeeck, D. Schryvers, et H. Idrissi, « TEM investigation of the role of the polycrystalline-silicon film/substrate interface in high quality radio frequency silicon substrates », *Mater. Charact.*, vol. 161, p. 110174, mars 2020, doi: 10.1016/j.matchar.2020.110174.
[39] M. Rack, F. Allibert, et J.-P. Raskin, « Modeling of Semiconductor Substrates for RF Applications: Part I—Static and Dynamic Physics of Carriers and Traps », *IEEE Trans. Electron Devices*, vol. 68, nº 9, p. 4598-4605, sept. 2021, doi: 10.1109/TED.2021.3096777.
[40] M. Rack, F. Allibert, et J.-P. Raskin, « Modeling of Semiconductor Substrates for RF Applications: Part II—Parameter Impact on Harmonic Distortion », *IEEE Trans. Electron Devices*, vol. 68, nº 9, p. 4606-4613, sept. 2021, doi: 10.1109/TED.2021.3096781.