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Total Ionising Dose effects in commercial 4H-SiC MOSFETs

V. Kotagama, A.B. Renz, K. Melnyk, V. Kilchytska, D. Flandre, V.A. Shah, M. Antoniou, P.M. Gammon

***Abstract*— This work presents a comparative analysis of total ionizing dose (TID) effects in modern commercial 4H-SiC MOSFETs, including both planar and trench-gate architectures from five manufacturers: onsemi, STMicroelectronics, Infineon, and two generations of ROHM devices. Devices rated at 650–750 V were exposed to gamma irradiation up to 500 krad using a Cobalt-60 source at gate biases of –5 V, +5 V, and +15 V, simulating space-relevant operating conditions. Threshold voltage shifts (V_{TH}) as large as –12 V were observed in trench-gate devices, with the ROHM Gen 3 MOSFET exhibiting a V_{TH} shift from +4.5 V to –7.5 V, converting the device to normally-on. In contrast, planar devices showed better resilience, with STMicro's planar MOSFET maintaining V_{TH} above +0.5 V under all test conditions and a maximum ΔV_{TH} of only –2.5 V. Secondary effects included up to 0.5 mA of drain leakage at drain-source voltage > = 50 V and on-resistance reductions of up to 28%, correlating with increased gate overdrive. Capacitance measurements revealed gate-source capacitance increases up to 366% and decreases up to 36% in trench devices. Post-irradiation annealing up to 300 °C enabled near-complete V_{TH} recovery in planar devices, while the trench devices showed only partial recovery, indicating deeper or more stable trap states. Extracted oxide trapped charge densities reached up to >4×10^{12} cm^{-2} in trench devices. These results underscore the influence of device structure, gate bias, and interface quality on radiation tolerance, with planar MOSFETs offering superior robustness for space-grade SiC power electronics.**

***Index Terms*—TID, MOSFET, commercial, 4H-SiC, Radiation**

I. Introduction

4H-silicon carbide (SiC) is now an established semiconductor for producing high-performance power electronics, exploiting its wide bandgap (WBG), high thermal conductivity, and high critical electric field [1]. These attributes enable SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) to operate at higher voltages, temperatures, and switching frequencies than traditional silicon (Si) devices, resulting in improved power converter efficiency and power density in electric vehicles, renewable energy systems, and industrial power converters [2, 3]. With the growing demand for radiation-hardened power devices in aerospace and deep-space missions, SiC MOSFETs have gained increasing attention for space-grade electronics [4]. The material's intrinsic properties suggest a strong potential for radiation tolerance, particularly under single-event effect (SEE) stress – an effect caused by a large quantity of charge deposited within the device, during a single energetic particle strike in space [5]. However, commercial terrestrial SiC devices have not been optimized for this purpose, with several studies having shown single-event burnout occurring at blocking voltages between 150 to 200V, significantly below their 1200V rating [6, 7].

Alongside the instantaneous destructive SEE effects, electronic devices in space are subjected to a cumulative radiation dose known as total ionizing dose (TID). TID primarily dictates the operational lifetime of these devices, as their electrical parameters gradually shift with increasing dose [8, 9]. TID effects primarily involve permanent charge trapping at oxide interfaces, making gate structures in devices such as MOSFETs and IGBTs particularly sensitive regions. For commercial SiC MOSFETs, both planar and trench devices exhibit varying degrees of radiation vulnerability, with degradation in key parameters such as threshold voltage, on-resistance, and gate leakage current observed across different device architectures and processing methods [10, 11].

The SiC/SiO_2 interface within a MOSFET is known to have an interface state density (D_{it}) one to two orders of magnitude higher than that of equivalent Si devices [12, 13], degrading channel mobility (and hence increasing resistance) and subthreshold behavior [14-17]. Under TID, degradation arises mainly from positive charge captured in near-interfacial oxide/border traps, which are strongly influenced by oxide thickness, interface quality, and applied gate bias rather than from D_{it} alone [18]. Upon irradiation, positive charge progressively accumulates in the gate oxide, which distorts the local electric field. In Si MOS devices, this build-up leads to the generation and activation of interface traps, thereby increasing D_{it} and positive trapped oxide charge [19]. This in turn results in increased leakage current as the MOSFET conducts at lower gate voltages. Simultaneously, elevated D_{it} reduces carrier mobility in the inversion channel, degrading device transconductance and overall efficiency, seen in prolonged space missions [8, 20].

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Previous studies [21] have shown that some of these effects, particularly the interface charge accumulation and trap activation may be partially reversible through post-irradiation annealing at elevated temperatures, which allows for charge relaxation and partial recovery of interface states.

This work presents a comparative study of TID-induced degradation in the current generation of commercial planar and trench SiC MOSFETs, from several manufacturers. Radiation dose, recovery time and post-irradiation annealing are all investigated to analyze charge trapping behavior and the potential for performance recovery.

II. Methodology

Five commercially available 650–750 V SiC MOSFETs from four different manufacturers were selected. Listed in Table 1, planar devices from onsemi and STMicroelectronics are compared to three different trench MOSFET designs, a first-generation asymmetrical design from Infineon and two generations of symmetrical design from ROHM. All devices were in TO-247 packages. Cross section depictions of all device types tested are in Fig.1.

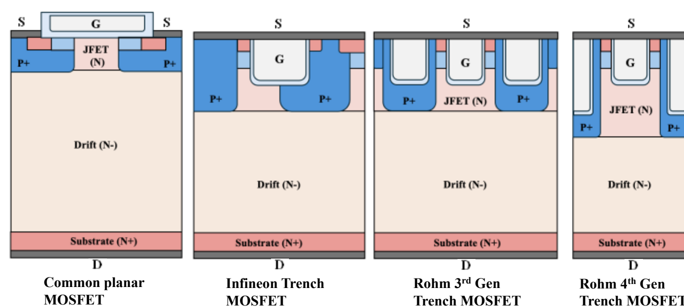

Fig.1. Cross sectional drawings of the four device types under investigation.

TABLE I

THE MOSFET DEVICES UTILIZED, WITH THEIR VOLTAGE RATING (V_{DSS}) AND ON-STATE DRAIN-SOURCE RESISTANCE ($R_{DS(ON)}$) PER THEIR DATASHEETS, AND THRESHOLD VOLTAGE (V_{TH}) AND ACTUAL BREAKDOWN VOLTAGE PER ELECTRICAL MEASUREMENTS.

Supplier / Part no.	Type	V_{DSS}	V_{BD}	$R_{DS(on)}$	V_{TH}
onsemi / NTHL045N065SC1	Planar	650 V	840	32 mΩ	2.71
STMicro / SCTW35N65G2V	Planar	650 V	860	67 mΩ	3.04
Infineon / IMW65R072M1H	Trench	650 V	820	72 mΩ	4.54
ROHM (G3) / SCT3080ALG	Trench	650 V	1260	80 mΩ	4.54
ROHM (G4) / SCT4045DEHR	Trench	750 V	970	45 mΩ	3.86

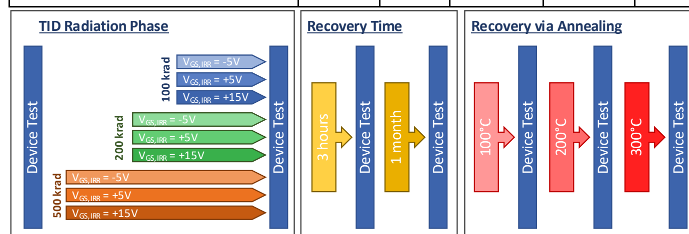

Fig.2. Summary of the testing undertaken. 27 devices were tested per manufacturer; three at each $V_{GS,IRR}$ step and radiation dose.

Fig.2. summarizes the testing methodology. In the first stage, all 27 of each device type were individually characterized at room temperature using a Keysight B1505A power device analyzer. At every characterization stage, each MOSFET's output and transfer characteristics were recorded along with its drain and gate leakage current. Threshold voltage (V_{TH}) is determined from the transfer characteristics by subthreshold slope measurements, per each datasheet. On-state drain-source resistance ($R_{DS(on)}$) is determined from the output characteristics under the gate voltage and drain current conditions specified in the respective device datasheets. Capacitance-voltage (C-V) measurements recorded the input, output and reverse transfer capacitance at 1MHz, from which, the gate-source capacitance (C_{GS}), gate-drain capacitance (C_{GD}) and drain-source capacitance (C_{DS}) are determined from commonly sourced associations [22].

This initial test, prior to irradiation, highlighted similarities and differences between the MOSFETs under test. Measured $R_{DS(on)}$ and V_{TH} values were consistent with their datasheet values, shown in Table 1. Where ROHM do not publish typical V_{TH} values, the values measured for the Gen 3 and Gen 4 devices were, respectively, 4.54 and 3.86 V. With the other trench device from Infineon also having a measured V_{TH} of 4.54 V, it is notable that these values exceed the planar MOSFETs' V_{TH} values of 2.71 and 3.04 V for the onsemi and STMicro devices, respectively. Measured up to -200 V, none of the devices had a drain-source leakage above the SMU's 100 pA compliance level. The same is true for gate-source leakage measured up to 22 V. Also listed in Table 1 are the device's rated voltage (V_{DSS}), and their actual measured breakdown voltage (V_{BD}). It is notable and relevant the differences in headroom (V_{BD}-V_{DSS}) in the dataset, the ROHM Gen 3 having the most headroom at 610 V.

After the initial characterization, the devices were split between nine identical PCB test boards, allowing three of each device to be tested under irradiation at a constant gate-source voltage ($V_{GS,IRR}$) of –5 V, +5 V, and +15 V, up to a total cumulative dose of 100, 200 and 500 krads. The drain-source voltage is held at 0 V (grounded) for all devices during the irradiation phase. Gamma irradiation was conducted using a Cobalt-60 source at a constant dose rate of 4.6 krad/hr, with cumulative exposure up to 500 krad, following European Space Agency (ESA) guidelines for space-grade electronics qualification [23]. After receiving the appropriate dose, the devices were stored and transported under dry ice in accordance with MIL-STD-883-1 standards [24].

After irradiation, the devices were left unbiased in ambient for one month, with testing occurring at regular intervals (hours, days, and months after). Given the stability of electrical measurements in this time period, only the data sets taken 3 hours and one-month post-irradiation are presented here.

Finally, annealing was performed on a hotplate at temperatures of 100 °C, 200 °C and 300 °C under floating conditions, each for an hour, with electrical characterization occurring at room temperature after cooling.

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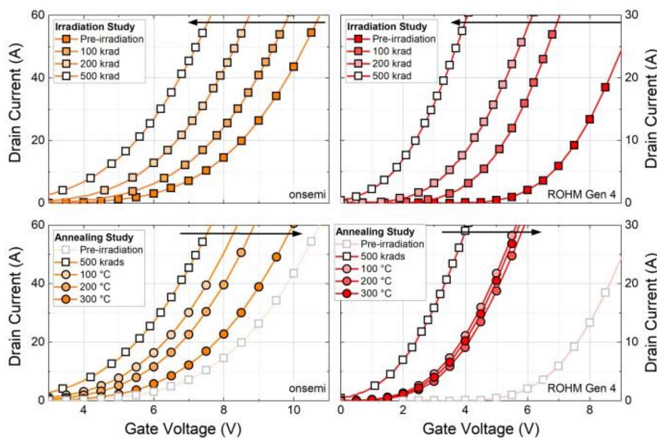

Fig.3. Transfer characteristics showing (top) cumulative radiation dose up to 500 krad, and (bottom) post-irradiation annealing for the onsemi planar and ROHM G4 trench MOSFETs, held at $V_{GS,IRR}$=15 V.

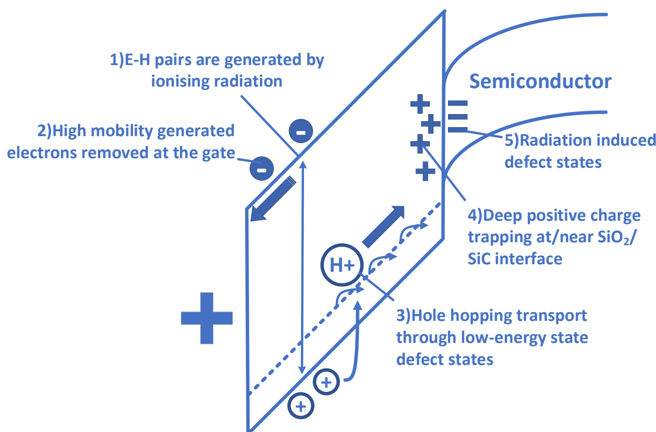

Fig.4. Band diagram of charge trapping at typical SiO_2/semiconductor interface in a NMOS device with positive gate bias [8, 9, 25, 26].

III. Radiation-Induced Charge Mechanisms and Electrostatic Impact

In Fig.3, the upper panels show the evolution with dose of the transfer characteristics of the onsemi planar and ROHM Gen 4 trench MOSFETs, tested with $V_{GS,IRR}$=15 V. They both display the effect of positive charge build-up in the oxide, resulting in a negative V_{TH} shift.

In Fig.4, the charge trapping mechanism is summarised for MOS devices. Upon exposure to ionizing radiation, the gate oxide absorbs energy and generates electron–hole pairs. The high-mobility electrons are quickly swept toward the gate electrode by the local electric field, while the much slower holes migrate toward the SiC/SiO_2 interface via field-assisted hopping between localized states [8, 9, 25, 26]. During this migration, holes interact with hydrogenated bonds within the oxide, such as Si–H or O–H, breaking them and releasing neutral hydrogen atoms. These then diffuse toward the interface, where they influence the formation or passivation of interface traps by altering the bonding structure at the semiconductor–oxide boundary [27-30]. Simultaneously, a fraction of the radiation-generated holes becomes trapped at intrinsic or radiation-induced defect sites within the oxide. These defects such as oxygen vacancies or Si dangling bonds act as efficient hole traps, contributing to the net build-up of fixed positive charge near the interface [8, 9, 26].

This accumulation of radiation-induced positive charge effectively pre-biases the semiconductor surface, resulting in a negative shift in the threshold voltage. The trapped charge introduces an internal electric field that enhances band bending at the interface, raising the surface potential (ψ_s) even in the absence of gate bias. Consequently, less external gate voltage is required to induce inversion, thereby reducing V_{TH}. From an electrostatic perspective, the positive charge acts to partially replicate the function of the gate electrode, accelerating the onset of channel formation. This behaviour is a well-documented signature of total ionizing dose (TID) effects in MOSFETs and is observed across both Si and SiC technologies [7, 16].

Following irradiation, the devices were stored under ambient conditions and periodically re-characterized over the subsequent month. In previous studies of Si/SiO_2 interfaces, partial recovery of threshold voltage has been attributed to the slow tunnelling of trapped holes out of shallow oxide traps [7, 15]. However, no significant recovery was observed in the present SiC MOSFETs under ambient conditions, suggesting a predominance of deep or more stable oxide traps.

In contrast, the lower panels of Fig. 3 demonstrate that low-temperature annealing, up to 300 °C, is effective in reversing a portion of the radiation-induced degradation. These anneals provide sufficient thermal energy for trapped holes to escape from defect states via thermally activated emission mechanisms.

IV. V_{TH} Shift and Estimating Q_{OT}

Threshold voltage was extracted from the transfer characteristics of all the device tests pre- and post-irradiation. This data is plotted in the top panel of Fig.5 while in the bottom panel, radiation-induced threshold voltage shift (ΔV_{TH}) is plotted. As per Fig.3, a consistent trend in V_{TH} is seen across all devices and biases, initially decreasing with increasing dose, with several devices reaching negative V_{TH} by 500 krad. For the onsemi and Rohm Gen 3 devices, fractional V_{TH} recovery occurs after 3 hours recovery time in air, but no other recovery is seen across the dataset up to one month after exposure. With anneals of increasing temperature to 300 °C, the Rohm devices partially recover, while the recovery is almost total in all three others.

Clear trends appear when comparing between devices. The planar MOSFET variants are the most resilient at any applied voltage. The threshold voltage remaining above zero under all conditions for the STMicro device, its maximum ΔV_{TH} being –2.5 V (at $V_{GS,IRR}$=5 V, 500 krads). For the onsemi device, the threshold voltage remained positive while $V_{GS,IRR}$=-5 V and was 0 V at $V_{GS,IRR}$ =15 V and 500 krads. However, at $V_{GS,IRR}$=5 V and 500 krads, a ΔV_{TH} of -4.5 V resulted in a negative threshold voltage. This means that the device is no longer a normally-off MOSFET, becoming normally-on, which could be unsafe for many applications.

The trench devices fared worse, by comparison. Like the planar MOSFETs, at $V_{GS,IRR}$=-5 V, the ΔV_{TH} of the Infineon trench MOSFET is <1 V, its V_{TH} remaining positive under all doses. However, for both the ROHM devices and the Infineon

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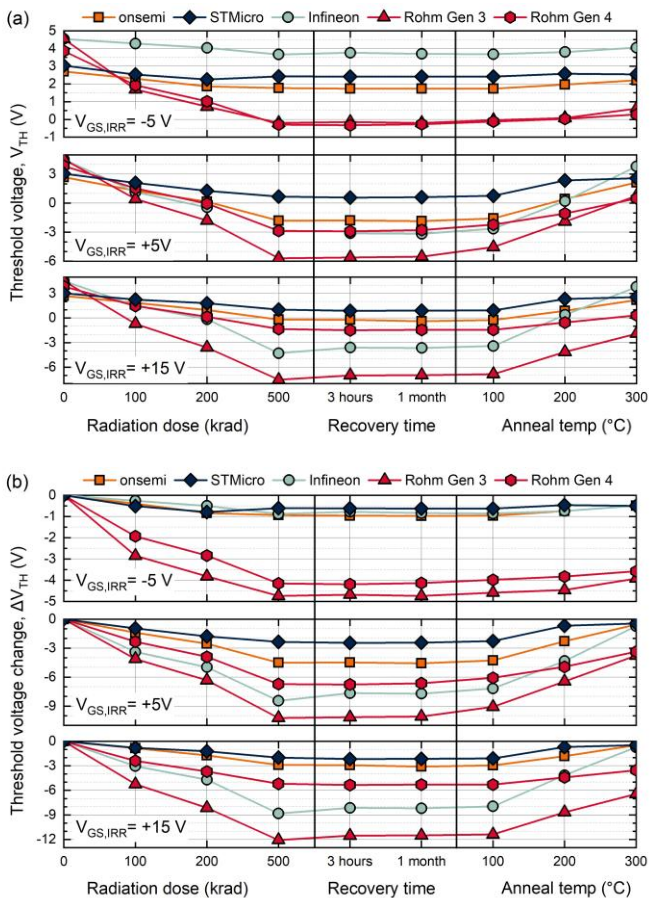

Fig.5. Comparison of a) average absolute threshold voltage and b) average threshold voltage shift from pre-irradiation for MOSFET dataset at a $V_{GS,IRR}$ of -5, 5, and 15V.

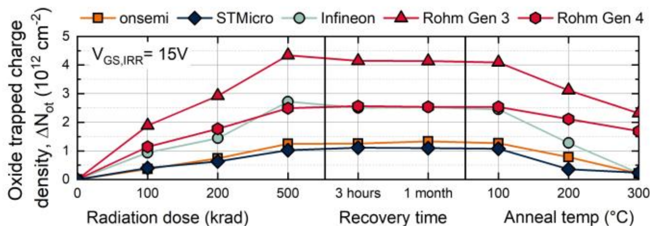

Fig.6. Comparison of oxide trapped charge density (ΔN_{ot}), that accumulates during radiation, as derived from ΔV_{TH} for the MOSFET dataset taken with a $V_{GS,IRR}$ of 15V.

device under positive bias, a 500 krad dose results in a large, negative V_{TH}. In the worst case, the ROHM Gen 3 device, biased at 15V and exposed to a 500 krad dose, had a V_{TH} of -7.5 V, which is 12 V lower than its pre-irradiation state.

Across all data, the ΔV_{TH} became increasingly negative with dose, while the presence of a positive $V_{GS,IRR}$ is notably worse than a negative $V_{GS,IRR}$. However, it did not follow that $V_{GS,IRR}$=15 V was always more deleterious than the 5V, though it is for the ROHM Gen 3 device. For the onsemi Rohm Gen 4 and STMicro devices however, the lower bias of 5V produced the greater ΔV_{TH}. A +5 V gate bias during irradiation may be more effective than +15 V for trapping hole charge due to its proximity to the devices' threshold voltage. In this bias range, the oxide electric field is optimally oriented to drive holes toward the SiC/SiO_2 interface while still allowing efficient trapping in pre-existing or radiation-induced defect states. At $V_{GS,IRR}$=+15 V, the device is driven into strong inversion; although the oxide field is even larger, the presence of an inversion layer may screen the field or influence trapping dynamics.

Post-irradiation, there is minimal change in V_{TH} during the post-recovery phase, while the devices are left in air at room temperature for one month. The low temperature annealing (100, 200, and 300°C) has an effect for all the devices however. For the onsemi and STMicro planar, and Infineon trench MOSFETs, there is near full recovery back to initial threshold voltage values, at 300°C of post-irradiation annealing. However, it is noted that approximately -0.5V of ΔV_{TH} remains for all in-situ gate biases for these devices once exposed to 500 krad. Both ROHM trench MOSFET exhibit only partial recovery. This limited response may be due to permanent interface damage caused by radiation-enhanced hydrogen motion, which can generate new interface traps (e.g., Si dangling bonds) [9, 20, 31]. Alternatively, a significant fraction of the positive charge may be trapped in deep or metastable oxide states, which are less thermally responsive. Further recovery might be achievable with longer, or higher-temperature, annealing.

It is possible to derive the total oxide trapped charge density that accumulates during radiation (ΔN_{ot}), given $\Delta V_{TH} = -\Delta Q_{ot}/C_{ox}$, where $\Delta Q_{ot} = q\Delta N_{ot}$ and $C_{ox} = \varepsilon_{ox}/t_{ox}$. ΔQ_{ot} is the radiation induced increase in total oxide trapped charge, ε_{ox} is the oxide (SiO_2) permittivity, C_{ox} is oxide capacitance calculated using oxide thickness (t_{ox}) estimates from commercially available sources [32]. Elsewhere, N_{ot}, has been estimated in commercial devices, without irradiation, to be approximately 3.5×10^{12} cm^{-2} [33], while ΔN_{ot} has been estimated to saturate at 3.3×10^{12} cm^{-2} [34]. This is in good alignment with experimental results herein. In the worst case, shown in Fig.6, for $V_{GS,IRR}$= +15 V and 500 krads, ΔN_{ot} ranged from 1-1.3×10^{12} cm^{-2} for the planar devices, to 2.5×10^{12} cm^{-2} for the ROHM Gen 4 and Infineon trench MOSFET variants, while the ROHM Gen 3, with a relatively thick oxide, is alone at 4.3×10^{12} cm^{-2}.

In this work, using commercial devices with many unknown parameters, it is not possible to accurately separate contributions to the total oxide charge N_{ot} from interface charge (N_{IT}), fixed charge (N_F), oxide trapped charge (N_A) or any other contributions. However, previous work [18] suggests that any incremental N_{IT} increase is likely to be small compared to N_A, as the primary driver of ΔV_{TH}. While dedicated D_{it} extraction was not possible, the subthreshold slope remained unchanged within experimental repeatability across all doses and devices, indicating no measurable D_{it} change over the dose range studied [14]. Consequently, while any interface-trap occupancy effect on ΔV_{TH} is implicitly included in the reported ΔN_{ot}, it is more likely that a change in trapped charge near the interface is the major contributor, in line with the theory of Fig 4.

V. SECONDARY EFFECTS OF RADIATION INDUCED V_{TH} SHIFT

The negative threshold voltage shift has an impact on other device characteristics. For any device in which the threshold voltage has become negative, a substantial drain-source current will now be able to pass through the device, when it ought to be in its blocking state. In many applications, the SiC MOSFET

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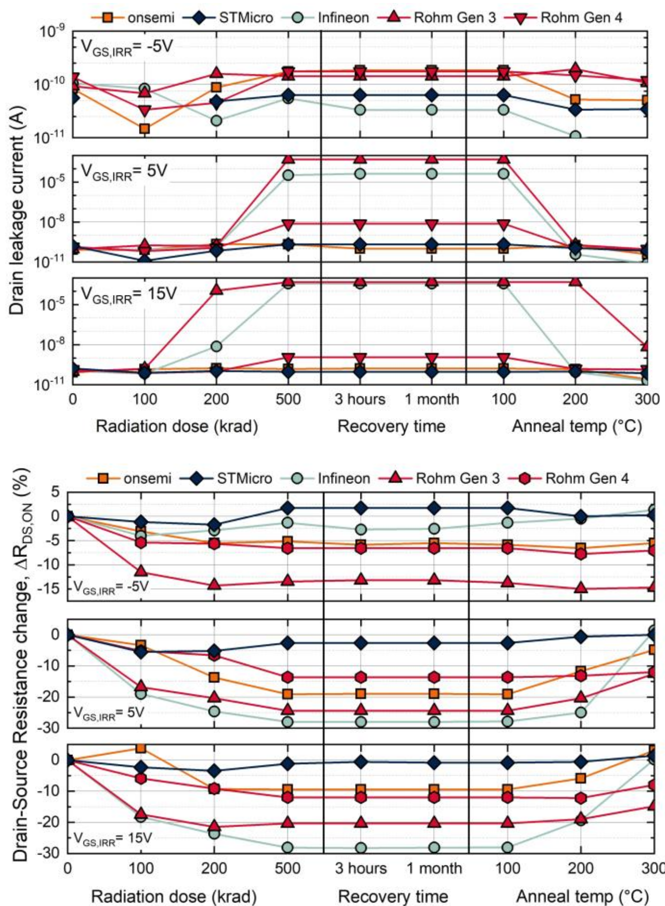

Fig.7. Top. Representative drain leakage measured at V_{DS}= 50 V, V_{GS}=-5V, and below, percentage on-resistance shift from pre-irradiation. Both datasets show results with $V_{GS,IRR}$=-5, 5, and 15V of in-situ gate bias and cumulative radiation dose up to 500 krad.

gate will be held at -5V during the off-state. Hence, in the top panel of Fig. 7, the drain-source I_{DS} is shown for V_{DS}= 50 V and V_{GS} = -5 V at each testing point. As might be expected, for those devices whose V_{TH} has shifted below, or close to -5 V, a substantial I_{DS} is present. This can be seen to affect the trench gated ROHM Gen 3 and Infineon devices the most; after 500 krad with $V_{GS,IRR}$=15 V, the leakage current of each device reaches the SMU's compliance (0.5 mA) before the 50 V drain voltage condition. These effects are seen to be reversible, the leakage reducing in line with V_{TH} increases post-annealing.

Gate leakage was also measured with V_{DS} = 0 V, under all test conditions. but no change was observed from pre-irradiation values below the equipment noise base of 100 pA. This means that any possible variation could not be resolved within the instrument's sensitivity. This indicates an absence of intrinsic gate oxide damage and reinforces the interpretation that the dominant TID mechanism is positive charge trapping in the oxide or at the oxide-semiconductor interface.

The results of percentage resistance shift from pre-irradiated values, $\Delta R_{DS(on)}$, are shown in the bottom panel of Fig. 7. The same general trends are observed, $R_{DS(on)}$ decreasing with radiation dose then recovering after annealing. At every measurement point, the resistance was measured using the same supplier-recommended V_{GS}. As a result, as V_{TH} decreases, the effective overdrive voltage (V_{GS}-V_{TH}) increases, enhancing channel conductivity and thereby $\Delta R_{DS(on)}$. This explains the correlation between ΔV_{TH} and $\Delta R_{DS(on)}$.

However, notable differences emerge when comparing ΔV_{TH} and $\Delta R_{DS(on)}$ trends across the device types. For example, following exposure to 500 krad with $V_{GS,IRR}$= +15 V, the Infineon device shows a 28% reduction in $\Delta R_{DS(on)}$, whereas the ROHM Gen 3 and Gen 4 devices exhibit smaller reductions of 20% and 12%, respectively. This occurs despite the ROHM Gen 3 device exhibiting a larger increase in gate overdrive than the Infineon device—by more than 3 V. Similarly, the onsemi device suffers a greater relative increase in $\Delta R_{DS(on)}$ than its modest ΔV_{TH}, when compared to either ROHM device.

One possible explanation is that the channel resistance constitutes a smaller proportion of the total $\Delta R_{DS(on)}$ in the ROHM devices, making threshold-related changes less impactful. Supporting this interpretation, is the higher V_{BD} of the ROHM devices, as shown in Table 1, implying they have wider or more lightly doped drift regions to support this voltage. This would result in a higher drift resistance, thereby reducing channel contribution to the total resistance.

A second explanation may lie in differences in interface charge and trap distribution. Devices with different D_{IT} (interface trap density) profiles may experience varying levels of mobility degradation under irradiation, even for similar ΔV_{TH}.

VI. Capacitance Responses

Representative plots of C_{DS}, C_{GS}, and C_{GD} against voltage are shown for the onsemi planar and ROHM G4 trench MOSFETs in Fig. 8 at all gate biases up to 500 krad. These were derived from input, output, and reverse transfer C-V_{DS} measurements, taken with a gate voltage of -5 V. Both C_{GS}, and C_{GD} represent the combined capacitance of the gate oxide and the depletion region formed in the semiconductor beneath. The application of a gate voltage of -5 V means that at low V_{DS}, the p-channel, under the gate, should be in accumulation prior to radiation. Similarly, the n-type JFET regions surrounding the gate should be in depletion. As the V_{DS} is ramped up to 10 V in the onsemi device, or 5V in the ROHM Gen 4 device, the depletion regions that expand laterally from the p-source, across the JFET regions, meet and merge in the centre of the JFET region. This can be seen in all the C-V plots, as when they merge, they combine to form a uniform planar depletion region within the drift region of reduced total area, and hence a jump to lower capacitance.

The results of Fig.8 reveal contrary effects of increasing positive charge accumulation in the gate dielectric. This is most noticeable at voltages below the aforementioned transition point in the C-V_{DS} responses. For instance, with V_{DS}=0.1 V applied to the onsemi device, following 15V/500 krads of exposure, the extra positive charge within the gate reduces the depletion region within the n-type JFET region, so increasing the gate-drain capacitance dramatically, by 111%. This is depicted in the bottom panel of Fig.8. For the ROHM Gen 4 trench device, the capacitance increase is 366%, the effect likely having been magnified by having a gate trench with a larger gate-to-JFET surface area. Above 10V, after the JFET region becomes fully depleted, minimal differences between

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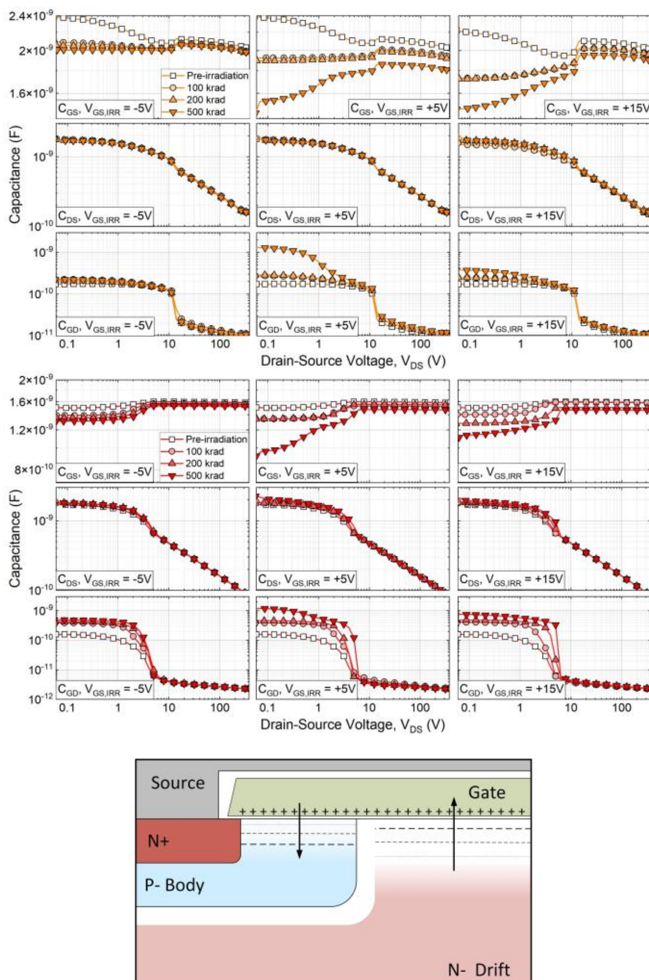

Fig.8. Representative gate-source, drain-source, and gate-drain capacitance with -5, 5, and 15V in-situ gate bias with cumulative radiation dose up to 500 krad for (top) the onsemi planar MOSFET and (middle) ROHM Gen 4. Measurement taken with -5V applied at gate. Bottom, a planar MOSFET gate showing the contrary effects of increasing positive gate charge, represented by the arrows, on the depletion regions in the p- channel and the JFET.

the C_{GD} values are seen as the gate oxide has a weak influence compared to the large V_{DS} bias.

By contrast, increased radiation induced gate charge brings about a reduction in C_{GS}. Depicted again in Fig 8, this occurs as described previously in section 1A, bringing about increased depletion at lower gate voltages, and hence lower capacitance. Given the relatively high doping of the p-channel and p-body compared to the n-JFET, the change in C_{GS} is less. With V_{DS}=0.1 V applied following a 15V/500 krads exposure, C_{GS} decreases by 36% in the onsemi device, and 27% in the ROHM Gen 4 trench device. Less affected by the depletion region expanding through the JFET and drift region, a negative change in C_{GS} remains, in both cases, up to V_{DS}=325 V.

The drain to source capacitance, C_{DS} is the least affected by charge in the gate, and little difference can be seen pre-and post-radiation.

VII. Comparisons within the SiC dataset

Fig. 9 compares the threshold voltage shift (ΔV_{TH}) of five SiC MOSFET technologies before and after radiation exposure

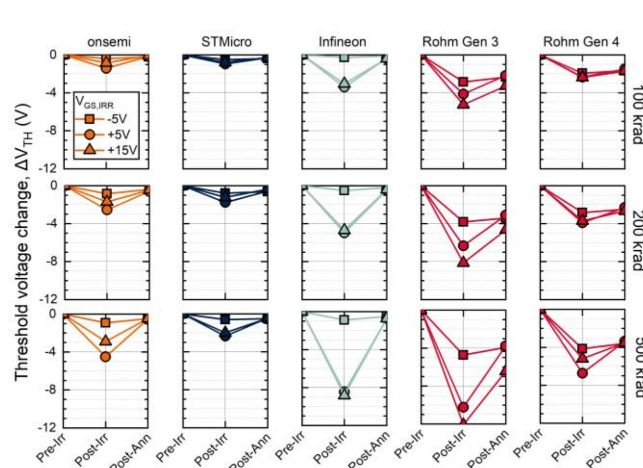

Fig.9. The average ΔV_{TH} for every device tested, under every condition. Each panel contains ΔV_{TH} for $V_{GS,IRR}$=-5, +5 and +15V, recorded pre-irradiation, post-irradiation and post 300°C anneal. The three rows represent data from 100, 200 and 500 krad doses. Device types align by column.

at 100, 200, and 500 krad, under the three $V_{GS,IRR}$ conditions (–5 V, +5 V, +15 V), and following a 300 °C anneal. As previously discussed, a clear bias dependence is observed, with the largest negative ΔV_{TH} typically occurring at $V_{GS,IRR}$ = +5 V, for all devices except the ROHM Gen 3.

Comparing device architectures, planar MOSFETs exhibit greater resilience to TID effects than trench-gate designs. The STMicroelectronics planar device shows exceptional stability, with minimal ΔV_{TH} even at 500 krad across all bias conditions. This may be due to its relatively thin gate oxide, which limits the volume available for charge trapping. The onsemi planar device also demonstrates moderate threshold shifts and good recovery. In contrast, the older trench devices—ROHM Gen 3 and Infineon—exhibit significant ΔV_{TH}, exceeding –8 V at 500 krad with $V_{GS,IRR}$=+5 V or +15 V bias. This degradation may be partly attributable to their thicker gate oxides, which lead to greater charge storage.

However, the more recently released ROHM Gen 4 device, despite having the second thinnest oxide, still shows a significant ΔV_{TH}. This suggests that trench gate structures may be inherently more susceptible to radiation-induced charge trapping due to geometric factors such as gate sidewall orientation, longer vertical channel length, or processing artefacts including trench wall roughness and subsurface damage from etching.

The annealing response further highlights differences between technologies. Both planar devices and the Infineon trench MOSFET show near-complete recovery of pre-irradiation V_{TH} following the 300 °C anneal, consistent with the release of thermally unstable trapped charge. By contrast, the ROHM Gen 3 and Gen 4 devices exhibit significant residual ΔV_{TH}, with only a weak correlation to radiation dose and virtually no dependence on irradiation bias. While further recovery with longer or higher-temperature anneals cannot be ruled out, the persistence of this shift suggests the presence of permanent defects or a population of deep, stable oxide traps not readily annealed at 300 °C.

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Notably, irrespective of total irradiation dose and $V_{GS,IRR}$, each device recovers to a similar final threshold voltage following the 300 °C anneal. This convergence suggests that the residual fixed charge in the partially recovered trench devices is generated primarily at low doses (∼100 krad), and remains thermally stable even as the total dose increases.

VIII. Comparisons with Si MOS devices

The fundamental physics of TID degradation in SiC MOSFETs are rooted in the same oxide-trapping phenomena long established in Si MOS technologies. However, the magnitude and spatial distribution of charge trapping differ substantially due to intrinsic material and structural differences between Si and 4H-SiC, as well as differences in oxide thickness and interface quality. Understanding these parallels and divergences provides valuable context for interpreting the present results and for guiding future hardening strategies in SiC technology.

As discussed earlier, the main mechanism for positive charge trapping induces a negative shift in V_{TH}, an increase in subthreshold leakage, and potential transconductance degradation.

These qualitative trends are entirely consistent with the bias dependencies previously observed in Si MOS transistors. Literature showed that positive gate bias enhances hole trapping through field-assisted transport, while negative bias suppresses it by reversing the oxide field [35]. The bias sensitivity observed in the tested SiC MOSFETs, where the positive irradiation bias produces the largest ΔV_{TH} in many SiC devices and parallels the electric-field dependence of oxide charge build-up documented in Si technologies [36].

It was notable that for several of the SiC MOSFETs irradiated, a positive bias of +5 V produced a larger negative ΔV_{TH} than at +15 V bias. Based on extensive findings in the Si MOS literature, such behaviour may arise from partial in-situ neutralization of oxide-trapped charge under high electric field conditions [37-39]. Two principal mechanisms were identified for this neutralization process: (1) the tunnelling of electrons from the silicon into pre-existing or radiation-induced oxide traps [40], and (2) the thermal emission of electrons from the oxide valence band into these traps [40, 41]. Both pathways act to compensate positively charged hole traps within the oxide and thereby mitigate the net threshold-voltage shift. At higher positive bias, the enhanced oxide field can therefore promote electron injection or field-assisted recombination, effectively counterbalancing the positive charge build up during irradiation. A similar but more pronounced version of this behaviour termed ‘super-recovery’ has been reported in Si MOS devices, where strong bias during or immediately after irradiation leads to an apparent over-recovery or even positive ΔV_{TH} shift [42]. The occurrence and magnitude of this field-assisted recovery in SiC remains highly dependent on device-specific parameters such as oxide thickness, dielectric quality, interface state density, and gate design, making its quantitative contribution difficult to isolate without dedicated time-resolved experiments of self-made test structures.

Similarly, the post-irradiation annealing behaviour in SiC mirrors that of Si MOSFETs. In both material systems, trapped holes in shallow or near-interfacial states can be thermally released through tunnelling or recombination during low-temperature annealing. The partial to full recovery of ΔV_{TH} observed in the present SiC data up to 300 °C thus represents the same thermally activated hole emission that has been extensively characterized in Si devices [43].

IX. Conclusion

This study presents a comprehensive evaluation of TID effects in modern commercial SiC MOSFETs, encompassing both planar and trench architectures. Across five devices from major manufacturers, trench MOSFETs consistently exhibited greater vulnerability to radiation-induced degradation, most notably in threshold voltage shift when compared to their planar counterparts. These shifts are driven predominantly by positive charge trapping in the gate oxide or at the SiC/SiO_2 interface and were strongly influenced by in-situ gate bias during irradiation. In several cases, particularly under +5 V and +15 V bias, threshold voltage shifts were large enough to render devices permanently-on, posing reliability and safety risks in power applications.

Secondary effects of this threshold shift were also observed, including increased drain leakage under typical off-state gate conditions and reduced on-resistance due to increased gate overdrive. However, measurable gate leakage remained unchanged across all irradiation conditions when V_{DS} = 0 V, suggesting that no intrinsic damage occurred in the gate oxide. This reinforces the interpretation that TID effects are primarily electrostatic in nature, dominated by oxide and interface charge trapping rather than dielectric degradation.

Post-irradiation annealing at temperatures up to 300 °C enabled partial to near-complete recovery in most devices, though ROHM trench MOSFETs exhibited persistent degradation, implying the presence of deeper or more stable trap states. Capacitance measurements revealed complementary changes in gate-drain and gate-source capacitances, consistent with shifting depletion regions due to trapped charge.

These findings underscore the importance of tailoring oxide quality, interface engineering, and bias management for radiation-sensitive environments. While planar SiC MOSFETs demonstrate relatively robust behaviour under TID stress, trench devices—despite other performance advantages—require further process-level hardening to ensure long-term reliability in aerospace and other radiation-exposed applications.

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