C-V Measurement and Modeling of Double-BOX Trap-Rich SOI Substrate

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1. Introduction

High-resistivity (HR) Silicon-on-Insulator (SOI) substrates with trap-rich (TR) layer (Fig. 1(a)) are widely used for RF chips. The trap-rich layer is a polysilicon film that captures free carriers and thus eliminates the parasitic channel at BOX-substrate interface and enables the substrate to retain its high nominal resistivity, which leads to lower losses and improved linearity [1, 2]. However, partial re-crystallization and impurity contamination in the trap-rich layer affect the local resistivity and, hence, the RF performance [3]. To solve these problems, a new structure named double-buried-oxide (D-BOX) TR substrates was proposed by UCLouvain and SOITEC, as shown in Fig. 1(b) [4]. This structure incorporates a second thin buried oxide (BOX2) beneath the TR layer, preventing direct contact between the TR layer and the silicon substrate. In this paper, we characterize the D-BOX structure through capacitance-voltage (C-V) measurements. The presence of the BOX2 eliminates the impact of the bulk depletion layer on C-V performance, simplifying the analysis. The D-BOX structure also enables the characterization of TR layer at wafer level.

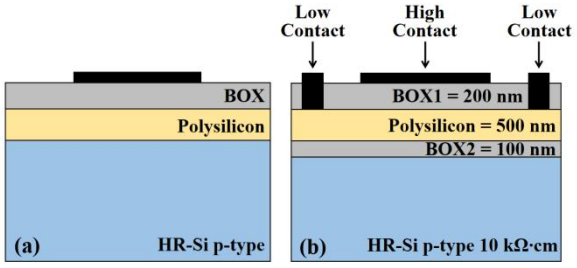

Fig. 1. Cross-section of (a) the HR SOI substrate with TR layer and (b) the D-BOX TR substrate.

2. Device Fabrication and Experimental Setup

The D-BOX TR substrate was fabricated at UCLouvain. The BOX2 layer was first thermally grown at 900℃ on top of the silicon substrate, followed by polysilicon and BOX1 layers deposited by LPCVD and PECVD, respectively. Finally, an Al layer was deposited on top of BOX1 layer and in contact with the polysilicon layer. The polysilicon is undoped, while the silicon substrate is lightly p-doped with a resistivity of 10 kΩ·cm. Details related to the structure are given in Fig. 1(b).

C-V measurements were performed with Agilent B1500A analyzer at 1 kHz. The High and Low electrodes are connected to the front gate (metal on top of BOX1 layer) and the polysilicon layer, respectively. All C-V hysteresis responses were measured starting from negative voltage towards positive voltage, and then sweeping back. The hold time and delay time were set to 120 s and 0.1 s, respectively.

3. Experimental Results and Discussion

The C-V characteristics (Fig. 2) exhibit anomalies attributed to the substantial density of traps present in polysilicon. Without traps, the C-V curve has a "V" shape, with the gate voltage at the minimum capacitance (C_{min}) aligning with the flat band voltage (V_{FB}). However, in Fig. 2 a plateau emerges when electrons begin to accumulate at the interface. Since $C=\Delta Q/\Delta V$, the decreased value of capacitance reflects a reduction of free charge in the polysilicon. The charge balance equation of this structure is $\Delta Q_G=\Delta Q_{trap}+\Delta Q_{free}$, where ΔQ_G, ΔQ_{trap}, and ΔQ_{free} are the change of the gate charge, trapped charge, and free charge, respectively. This means that, with the application of a voltage, a portion of the charge carriers may become trapped and therefore cannot effectively contribute to the overall capacitance, resulting in a reduction of the total capacitance. Silvaco TCAD simulations are used to verify the origin of the C-V plateau.

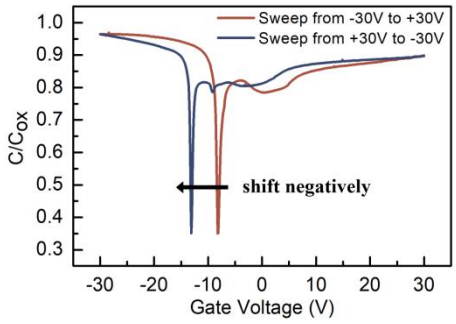

Fig. 2. Measured capacitance versus gate voltage of the polysilicon at 1 kHz.

Fig. 3 gives the device structure and physical parameters used in the simulation. The simulated C-V curves with different trap distributions are shown in Fig. 4. As illustrated in Fig. 4(a), the plateau emerges with a Gaussian distribution of acceptor traps located near the mid-gap. The corresponding capacitance value and the extension of the plateau increase for higher traps density. Conversely, with only tail distributions for donor and acceptor traps similar to [3], no plateau appears in Fig. 4(b). Thus,

it can be concluded that the plateau is a signature of the distribution of acceptor traps near the mid-gap.

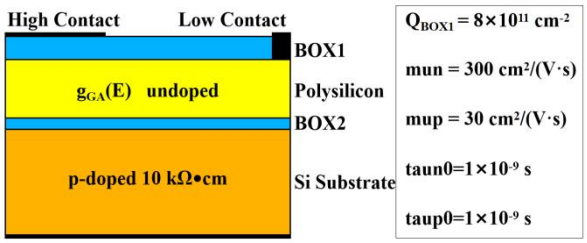

Fig. 3. Cross-section of the device structure and physical parameters used in TCAD simulation.

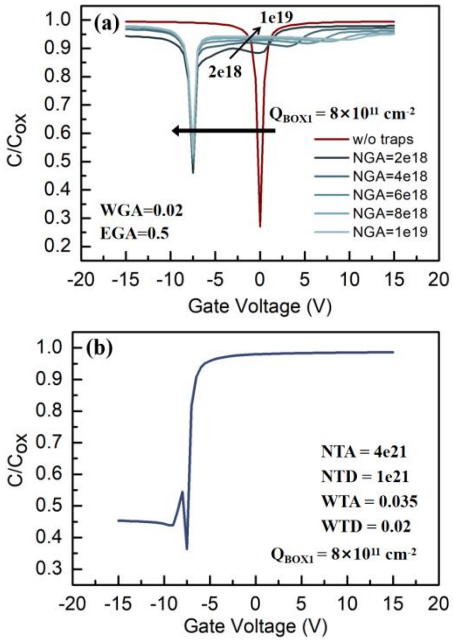

Fig. 4. Simulated C-V curves with different traps distributions: (a) only Gaussian distribution with different acceptor trap densities, (b) only tail distribution.

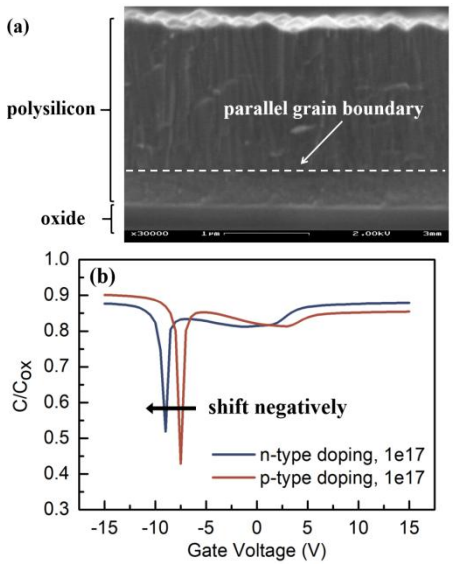

Fig. 5. (a) SEM diagram of polysilicon deposited at 625 ℃ (standard technology) without undergoing any annealing. (b) Simulation result of the hysteresis in polysilicon.

Hysteresis effect is also observed between forward and reverse gate voltage sweeps as shown in Fig. 2. The hysteresis effect is caused by the trapping and detrapping of carriers at the interface between the oxide and the semiconductor channel. A shift to positive gate voltage is observed in most studies due to oxide traps near the interface [5, 6]. However, in our experiment, a shift to the negative gate voltage is observed. It is probably due to the large density of traps in the polysilicon near the interface. In fact, the polysilicon is composed of a large number of grains. The traps density at the grain boundary is much higher than inside the grains, especially at the triple point. Fig. 5(a) gives the SEM picture of the polysilicon deposited on the oxide. A grain boundary parallel to the surface is clearly observed. The distance from the parallel grain boundary to the bottom polysilicon/oxide interface is around 500 nm, which equals to the thickness of polysilicon used in this paper. The trapping/detrapping of carriers at the parallel grain boundary changes the potential barrier at the front interface and leads to a negative shift of C-V curve. The trap density at the parallel grain boundary is larger than that in the oxide near the front interface. Thus, the traps in the parallel grain boundary dominate the shift direction.

Simulations are performed to verify the hypothesis mentioned above. Based on the TCAD model shown in Fig. 3, a 5 nm thickness polysilicon region with a high trap density is defined at the front interface. The Heiman's model in Silvaco is exclusively utilized for simulating the insulator trap-induced hysteresis. To mimic the change in the Fermi level caused by trapping and detrapping at the grain boundary, we employed p- and n-type doping in the parallel grain boundary. The p- and n-type doping correspond to the hole trapping and detrapping, respectively. The simulation result is shown in Fig. 5(b). It can be seen that, the C-V curve shifts to the negative gate voltage, which is in agreement with the experimental result. Therefore, the deep trap density at the grain boundary can be evaluated through the hysteresis effect. According to $\Delta N_{dt}=C_{ox}\times\Delta V_{hys}/q$, the amount of deep trap density in the grain boundary is 5.4×10^{11} cm^{-2}.

4. Conclusion

This work presents an analysis of the unusual C-V behavior in D-BOX structures. We show that deep traps in the polysilicon are responsible for both the plateau in the C-V curve and the negative shift in hysteresis. The structure used in this paper offers an effective and simple means to evaluate the trap density in the trap-rich layer.

References

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