Estimation analytique des taux de défaillance dans les SRAM sous seuil en régime de rétention de données

Analytical Prediction of Subthreshold SRAM Hold Failure Probability

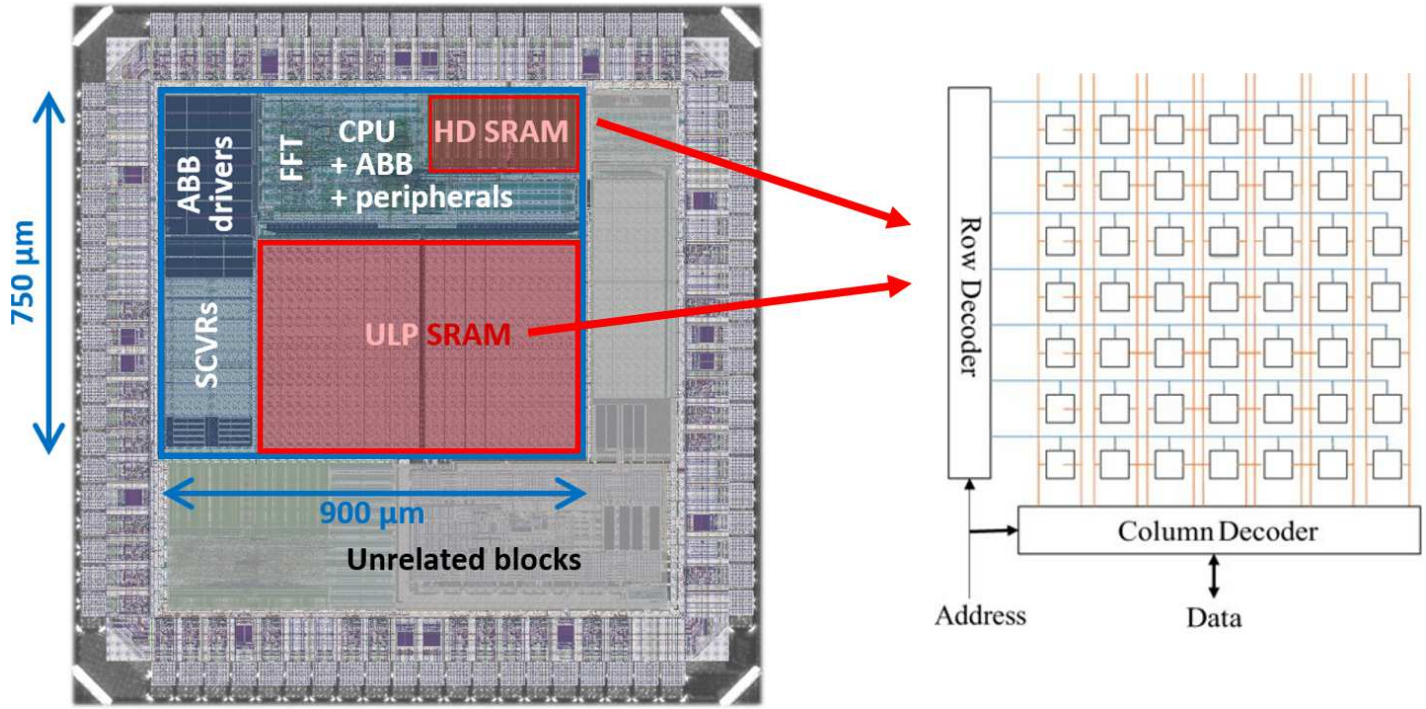
Léopold Van Brandt and Denis Flandre

Université catholique de Louvain

leopold.vanbrandt@uclouvain.be, denis.flandre@uclouvain.be

2nd of February

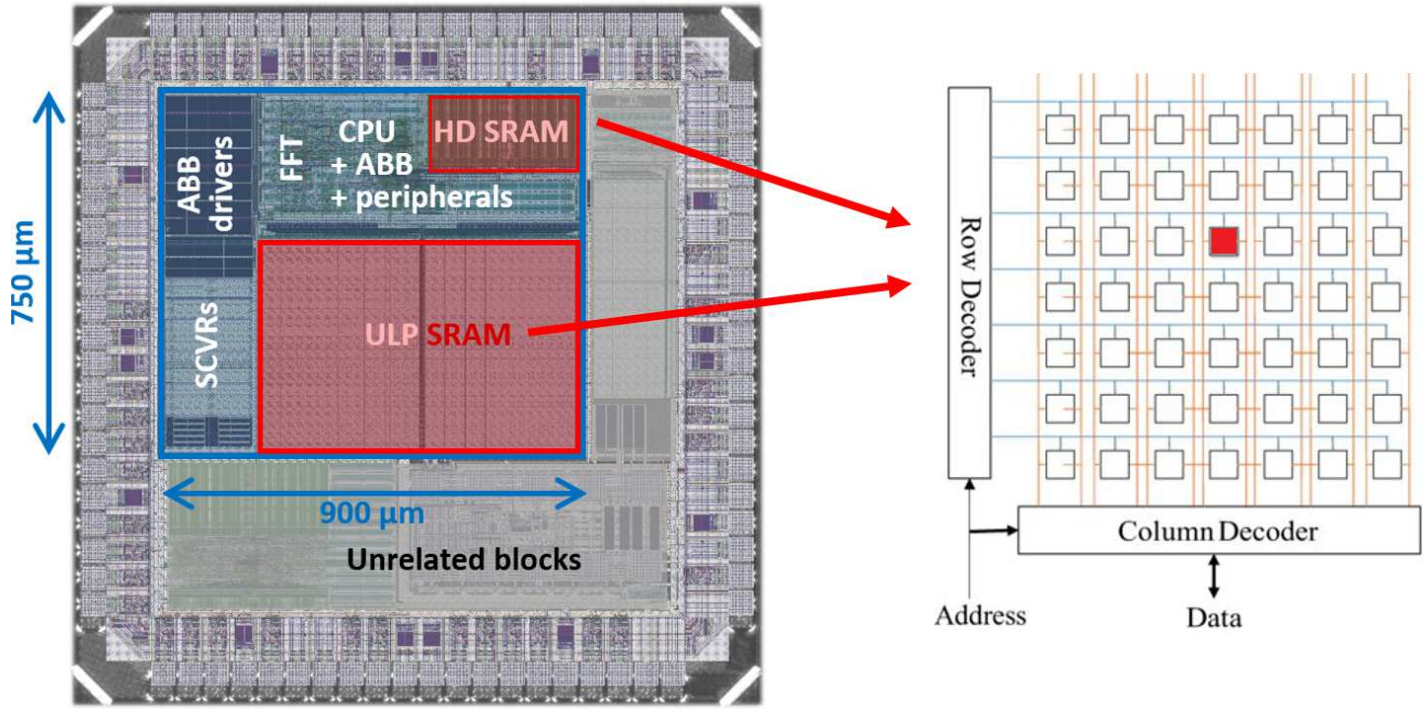
SRAM Arrays and Cell Failure Probability



SleepRunner ULP MCU [Bol et al., 2021]

$32\,\text{kB SRAM macro/array} = 32 \cdot 1024 \cdot 8 = 262\,144\ \textit{bitcells}$

SRAM Arrays and Cell Failure Probability



SleepRunner ULP MCU [Bol et al., 2021]

32 kB SRAM macro/array $= 32 \cdot 1024 \cdot 8 = 262\,144$ *bitcells*
Failure "risk" (*probability* P_{fail}) due to uncertainties (*process variability*)

System-level countermeasure: introduce redundancy
Design: need to guarantee $P_{\text{fail}} \lesssim 1 - 10\,\text{ppm}$ $\quad (1\,\text{ppm} = 10^{-6})$.

$\Longrightarrow$ Efficient and accurate prediction of P_{fail} at circuit level?

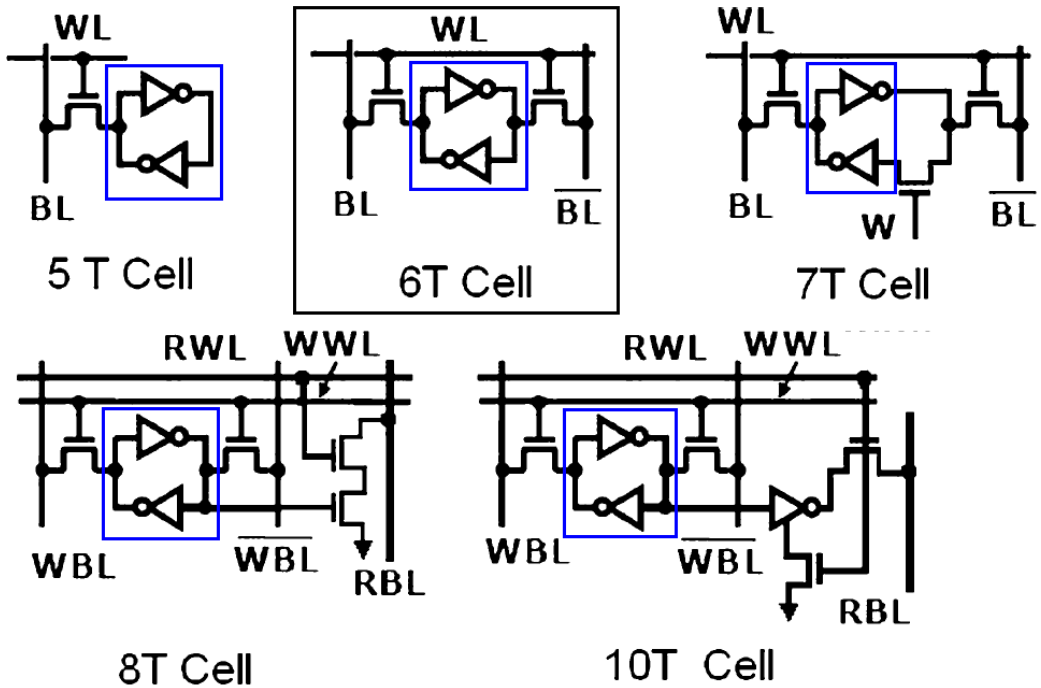
Subthreshold SRAM

Ultra-low power (ULP) SRAM design [Chandrakasan et al., 2010; Alioto, 2012]:

- smallest transistors ($W_{\min}$,$L_{\min}$) for high integration density
- *ultra-low voltage* (ULV) $V_{\mathrm{DD}} \searrow 400 - 500\,\mathrm{mV} \ldots \sim 150\,\mathrm{mV}$ (ultimate ?)

$\hookrightarrow$ Robustness against read/write/hold failures?

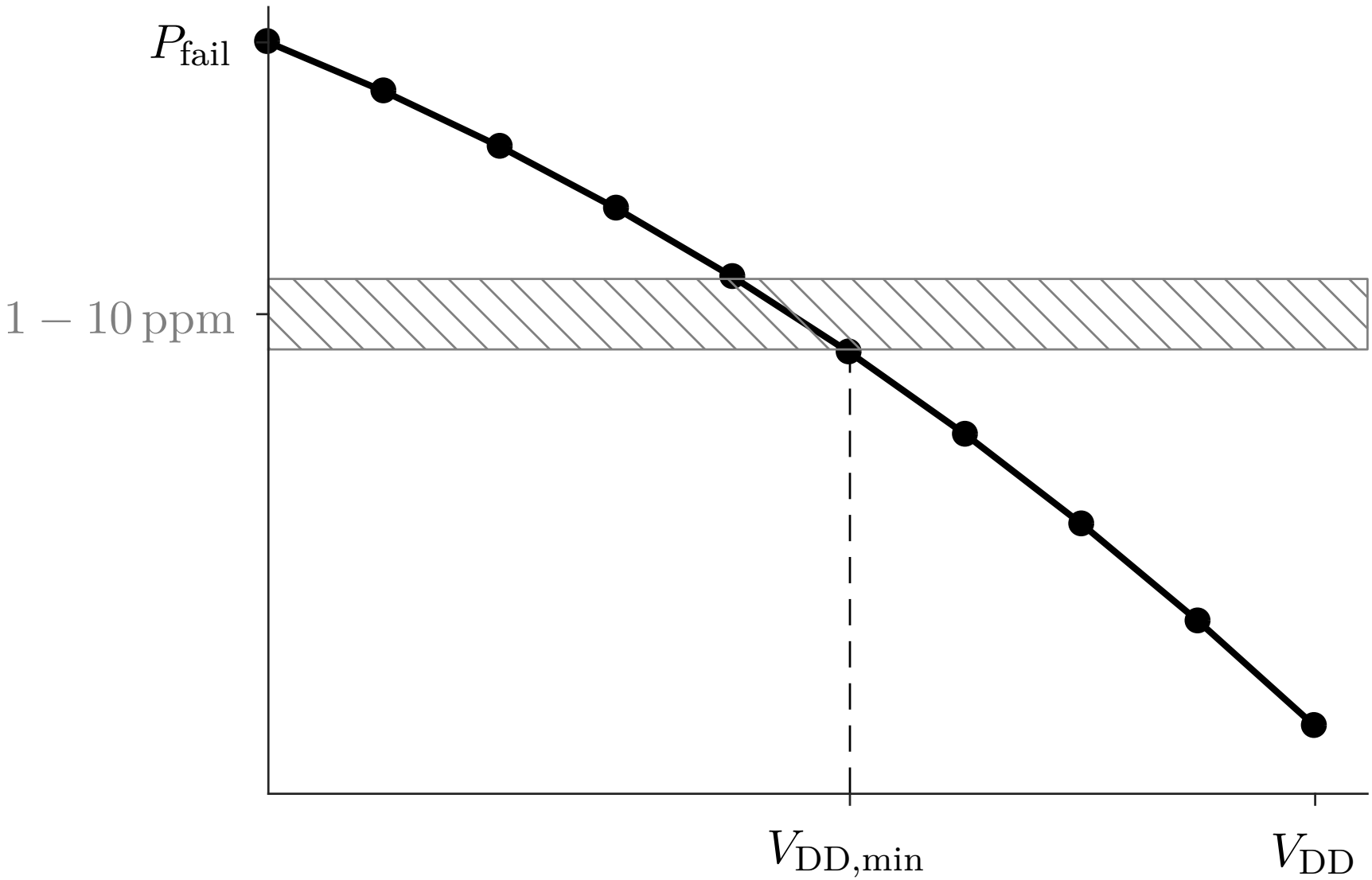
Subthreshold SRAM architectures [Kulkarni et al., 2007; Jaiswal et al., 2019]:



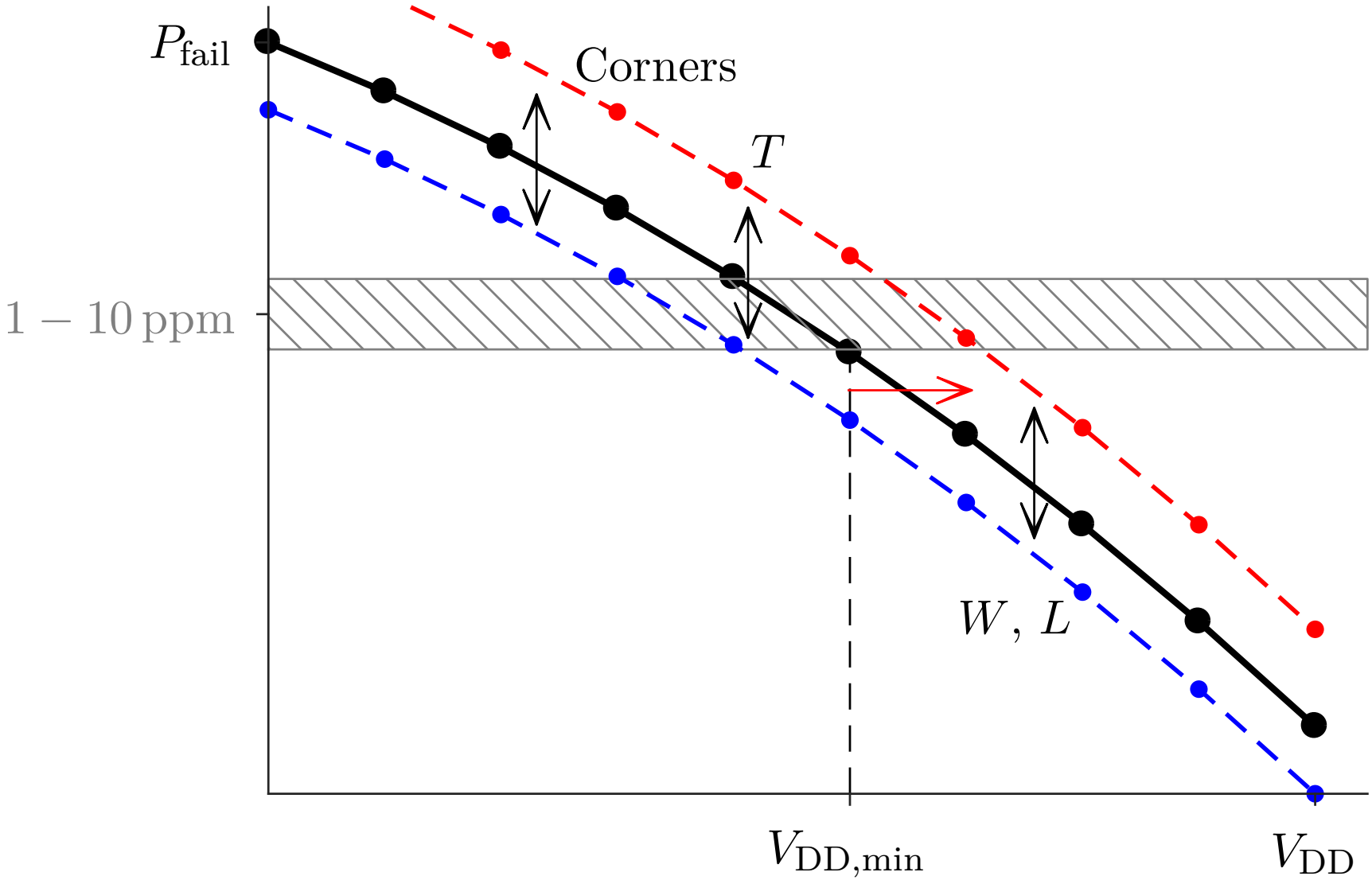
all use the same cross-coupled inverter pair (latch) for data *retention*.

The hold mode is the critical one when the read operation is buffered.

ULV SRAM Design: Failure Probability



ULV SRAM Design: Failure Probability

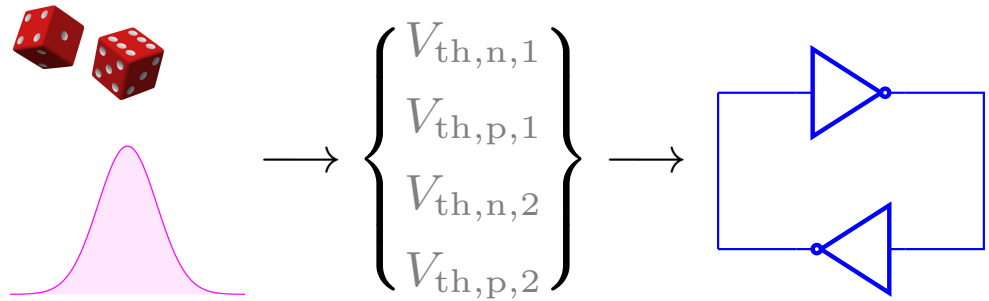


Estimation of Failure Probability

Monte-Carlo Simulation

Simulate N_s latches.
For each latch, "*throw dice*"

- for each transistor parameter (V_{th}), *sampling* from the *distribution*;



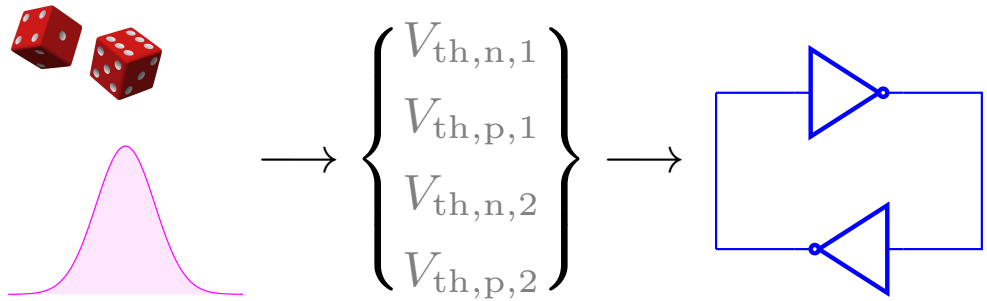
- classify as either functional or defective.
  ↪ iif the two stable logic states "0" and "1" exist

Estimation of Failure Probability

Monte-Carlo Simulation

Simulate N_s latches.
For each latch, "*throw dice*"

- for each transistor parameter (V_th), *sampling* from the *distribution*;



- classify as either functional or defective.
  $\hookrightarrow$ iif the two stable logic states "0" and "1" exist

How many samples (N_s) to estimate P_fail for some design (architecture, W, L), in a given corner, at *one* given T and *one* single V_DD?

$$\left.\begin{array}{l} \textit{accuracy of } (1-\varepsilon)\cdot 100\,\% \\ \textit{confidence level of } (1-\delta)\cdot 100\,\% \end{array}\right\} N_\mathrm{s} = \frac{2}{\varepsilon^2}\left(\mathrm{erf}^{-1}(1-\delta)\right)^2 \frac{1}{P_\mathrm{fail}}$$

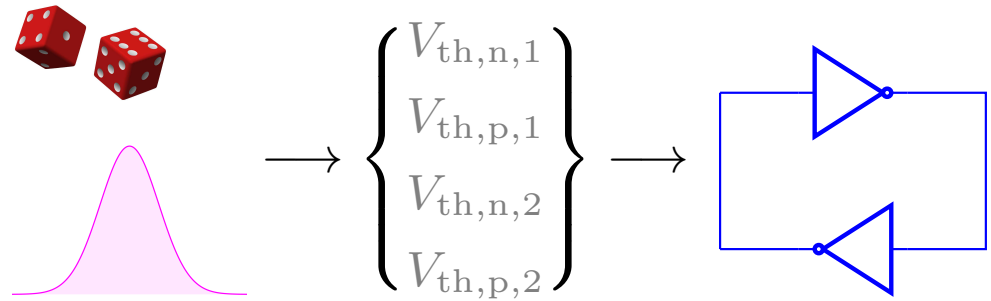
$(1-\varepsilon) = (1-\delta) = 90\,\%$, target $P_\mathrm{fail} = 10\,\mathrm{ppm} \implies N_\mathrm{s} = 27$ **million**!

Estimation of Failure Probability

Monte-Carlo Simulation

Simulate N_s latches.
For each latch, "*throw dice*"

- for each transistor parameter (V_th), *sampling* from the *distribution*;



- classify as either functional or defective.
  ↪ iif the two stable logic states "0" and "1" exist

How many samples (N_s) to estimate P_fail for some design (architecture, W, L), in a given corner, at *one* given T and *one* single V_DD?

$$\left.\begin{array}{l} \textit{accuracy of } (1-\varepsilon)\cdot 100\,\% \\ \textit{confidence level of } (1-\delta)\cdot 100\,\% \end{array}\right\} N_\mathrm{s} = \frac{2}{\varepsilon^2}\left(\mathrm{erf}^{-1}(1-\delta)\right)^2 \frac{1}{P_\mathrm{fail}}$$

$(1-\varepsilon) = (1-\delta) = 90\,\%$, target $P_\mathrm{fail} = 10\,\mathrm{ppm} \implies N_\mathrm{s} = 27$ **million**!

Cheaper but less accurate: accelerated Monte-Carlo (but still Monte-Carlo...);
SRAM analytical modelling (insightful!)

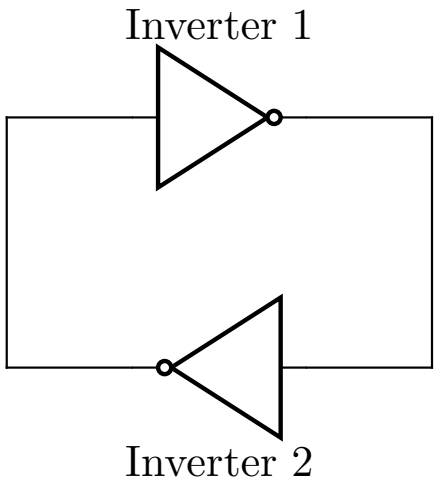
Our methodology "in between": *deterministic simulations + analytical statistics*

Outline

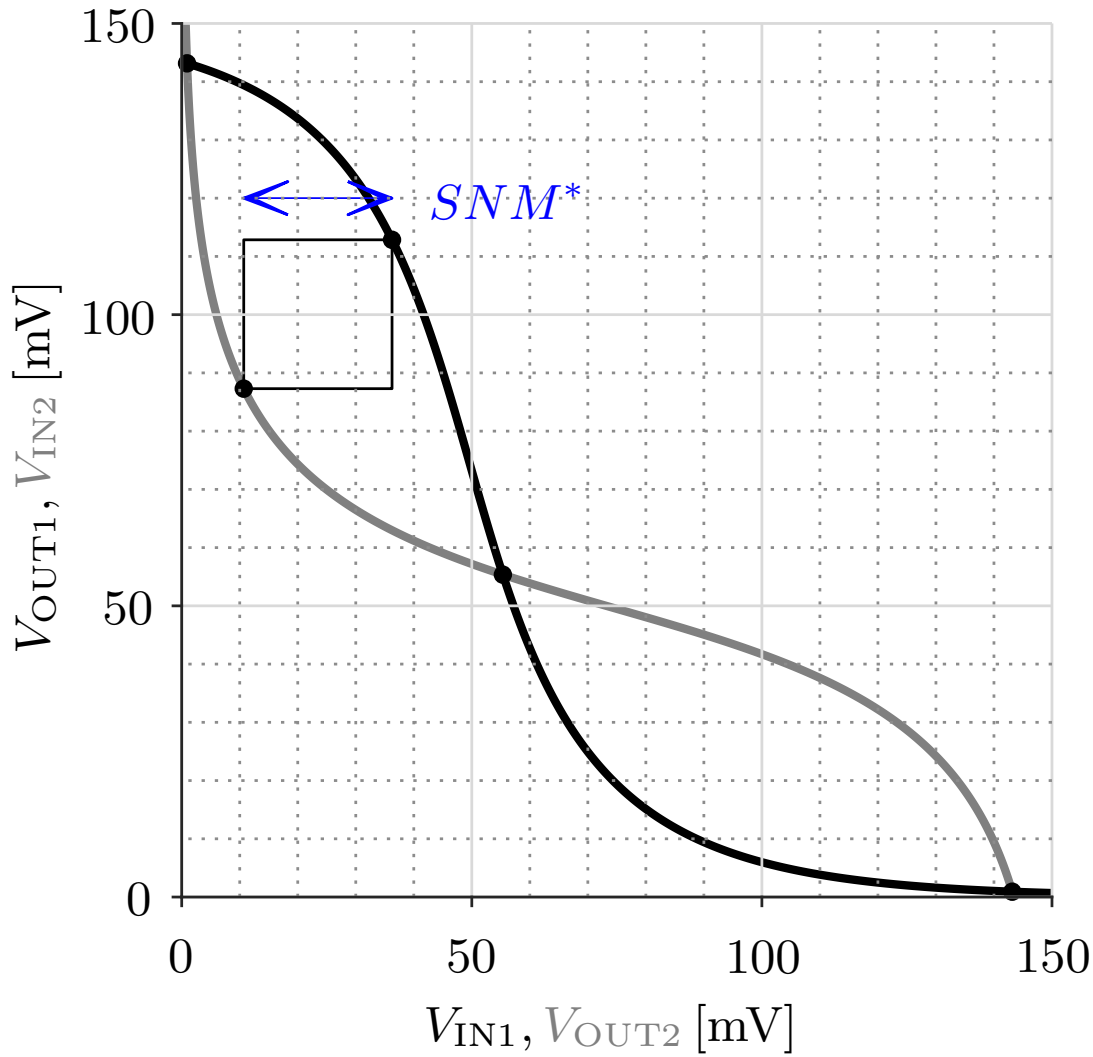
1. Context and Motivation
   - Subthreshold SRAM Bitcells
   - Estimation of Failure Probability
2. Methodology
   - Failure Detection
   - Threshold Voltage Imbalance Representation
   - Failure Probability Prediction
3. Discussion
   - Modelling Assumptions
   - Approximated Closed-Form Formula
   - Application: Effect of the Supply Voltage Variation
   - Accuracy: Benchmark with Former Works

Failure Detection

Static noise margin extraction:

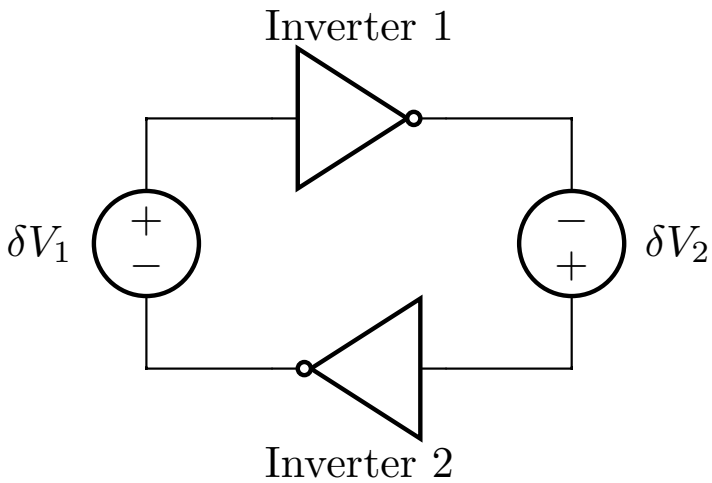


"Butterfly plot" [Seevinck et al., 1987]



Failure Detection

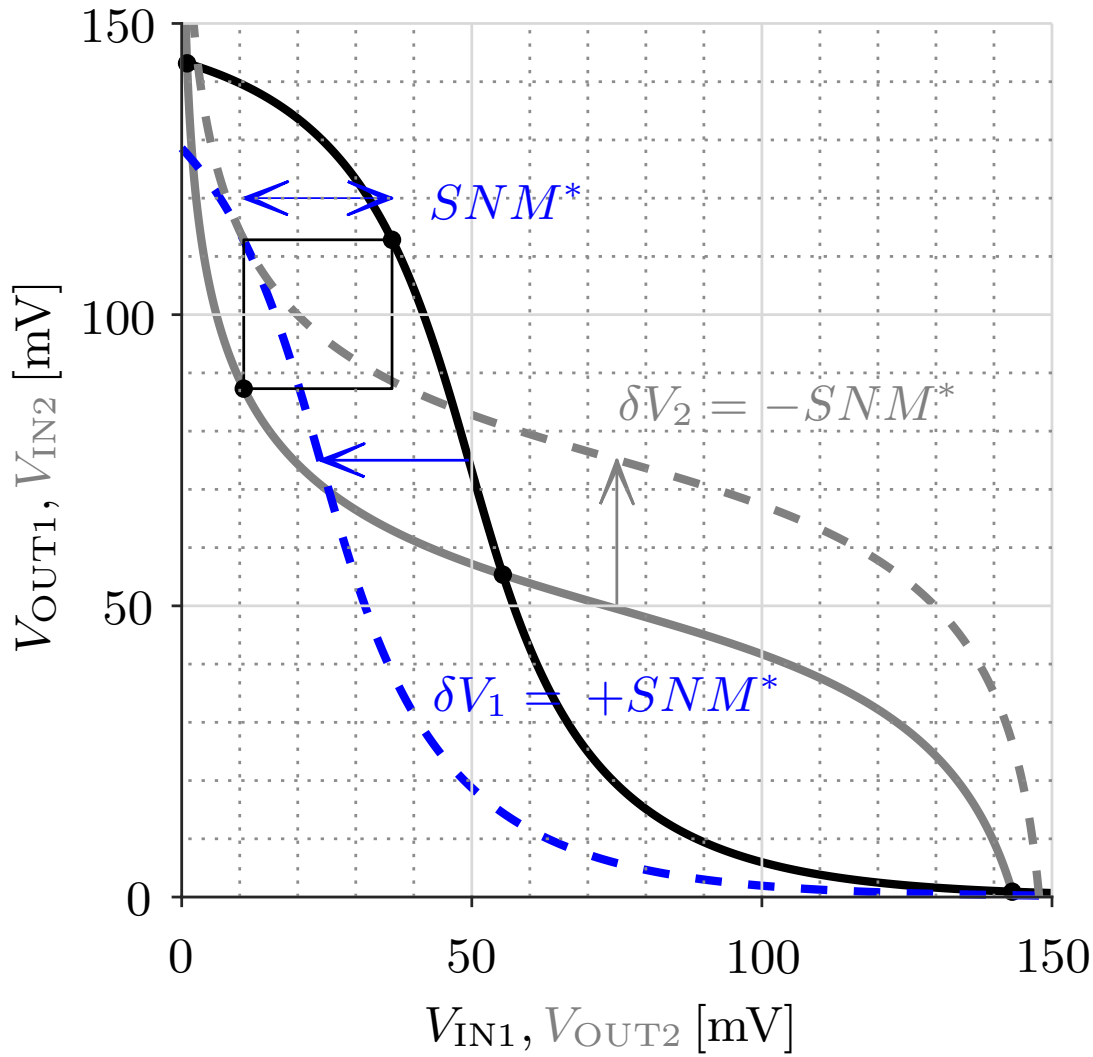
Static noise margin extraction:



$SNM(\delta V_1, \delta V_2) \gtrless 0$?

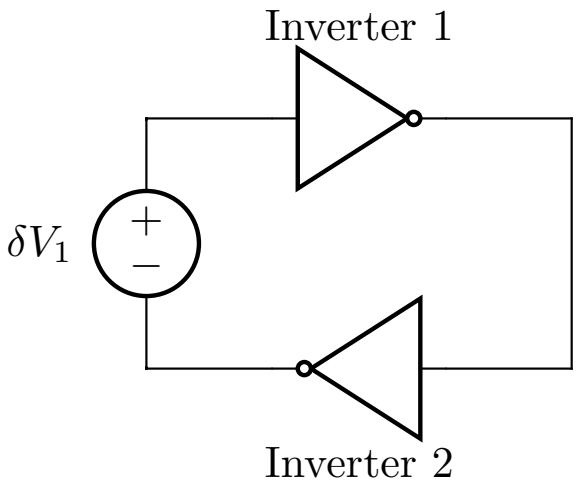
Cheap **deterministic** simulation
("`DC` sweep") at *circuit* level

"Butterfly plot" [Seevinck et al., 1987]



Failure Detection

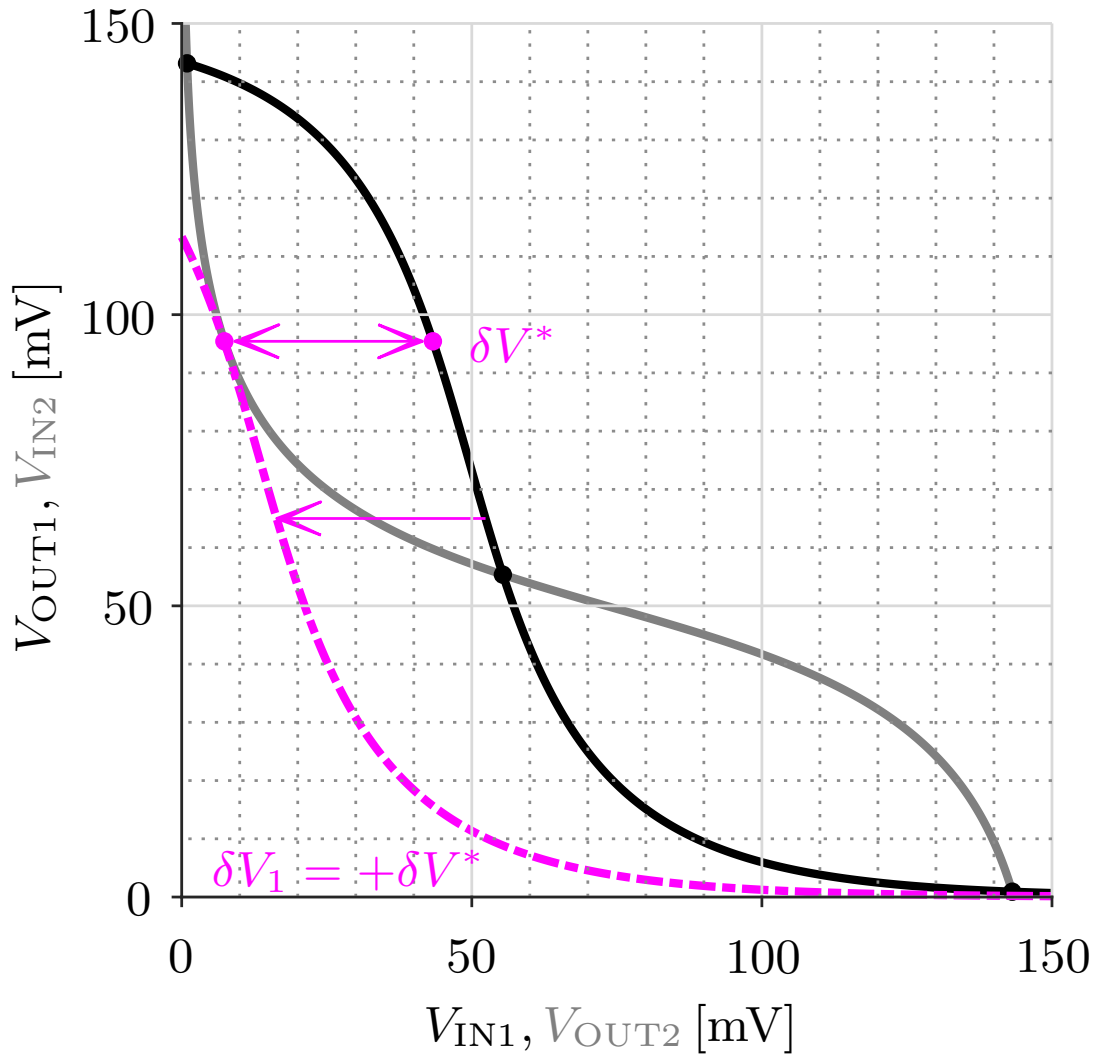
Static noise margin extraction:



$SNM(\delta V_1, \delta V_2) \gtrless 0?$

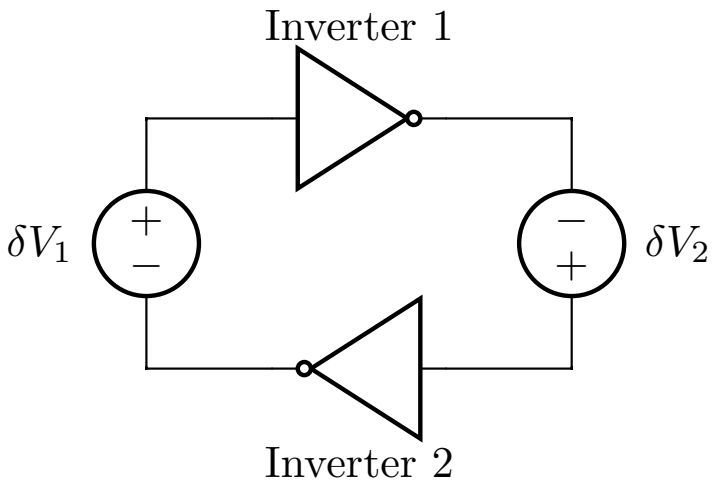
Cheap **deterministic** simulation
(“`DC` sweep”) at *circuit* level

“Butterfly plot” [Seevinck et al., 1987]



Failure Detection

Static noise margin extraction:

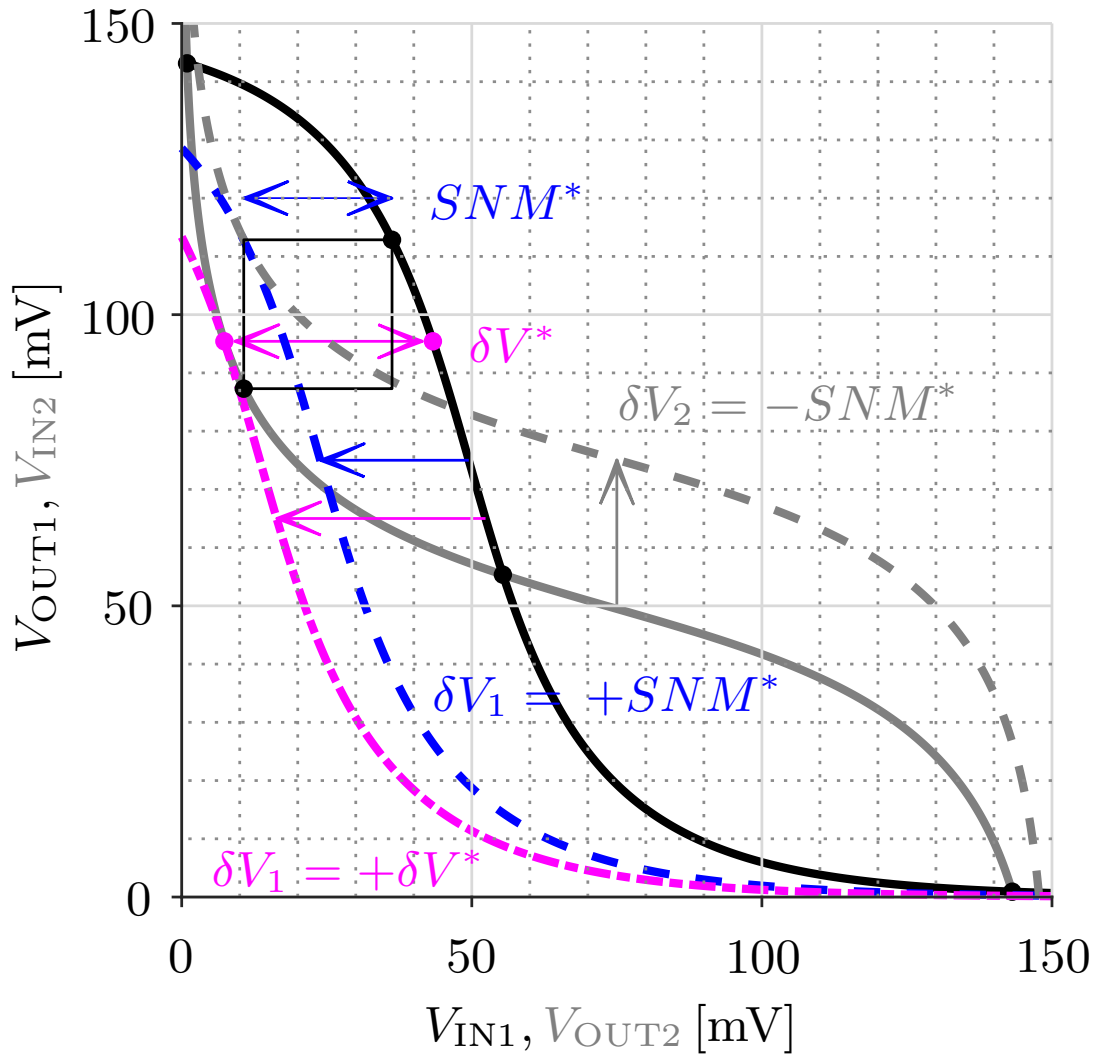


$SNM(\delta V_1, \delta V_2) \gtrless 0$?

Cheap **deterministic** simulation
("`DC` sweep") at *circuit* level

\+ knowledge of variability,
at the *transistor* level.

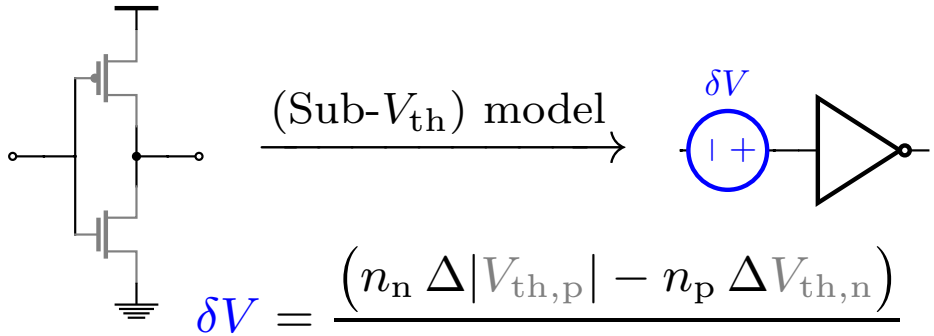
"Butterfly plot" [Seevinck et al., 1987]



"Propagate the *statistics*" $\longrightarrow$ efficient analytical calculation of P_{fail}!

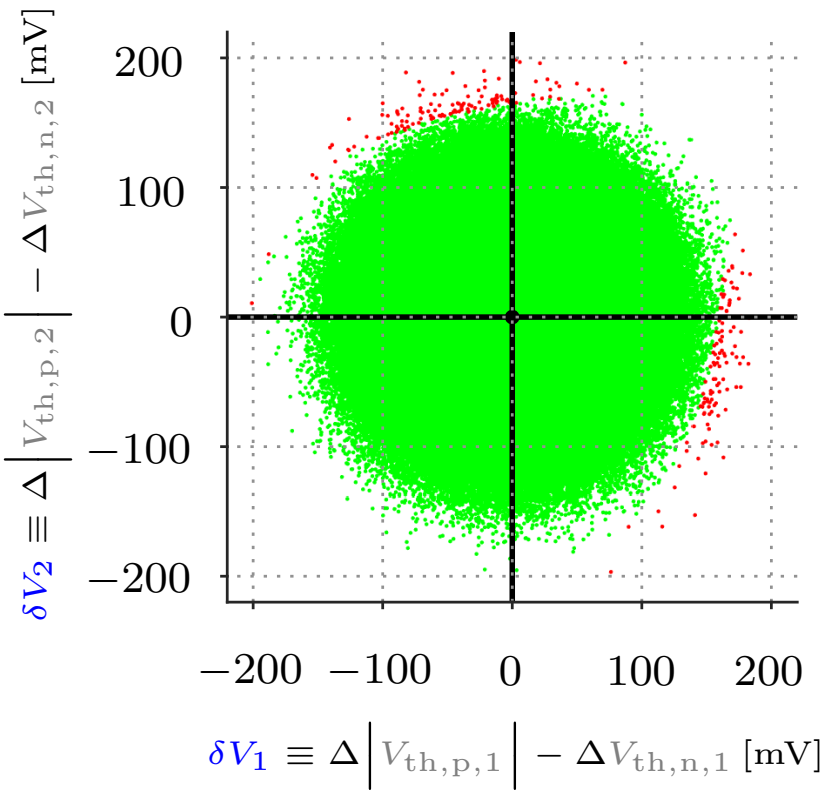
Threshold Voltage Imbalance Representation

"Transistor to circuit parameter"



$$\delta V = \frac{\left(n_{\mathrm{n}}\,\Delta|V_{\mathrm{th,p}}| - n_{\mathrm{p}}\,\Delta V_{\mathrm{th,n}}\right)}{n_{\mathrm{n}} + n_{\mathrm{p}}}$$

Illustration with Monte-Carlo simulation:



28 nm FD-SOI SPW latch

RVT nMOS and LVT pMOS transistors

Minimal dimensions ($L_{\mathrm{n}} = L_{\mathrm{p}} = 30\,\mathrm{nm}$ $W_{\mathrm{n}} = W_{\mathrm{p}} = 80\,\mathrm{nm}$);

$V_{\mathrm{DD}} = 200\,\mathrm{mV}$; $T = 300\,\mathrm{K}$; TT corner.

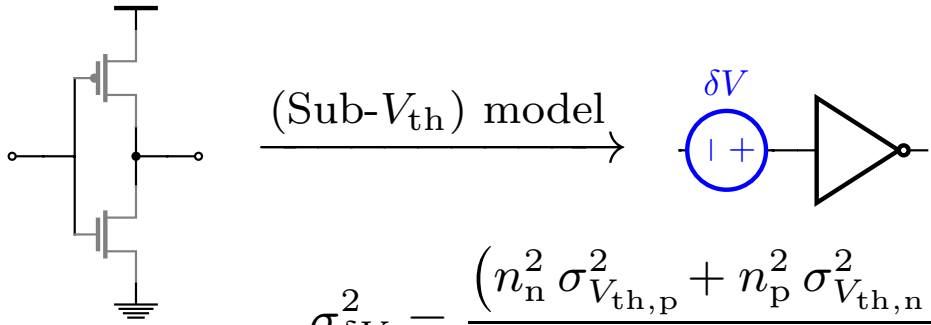
Two weeks of total simulation + analysis time!

5 M latches

$\hookrightarrow$ 235 defective ($P_{\mathrm{fail}} = 47\,\mathrm{ppm}$)

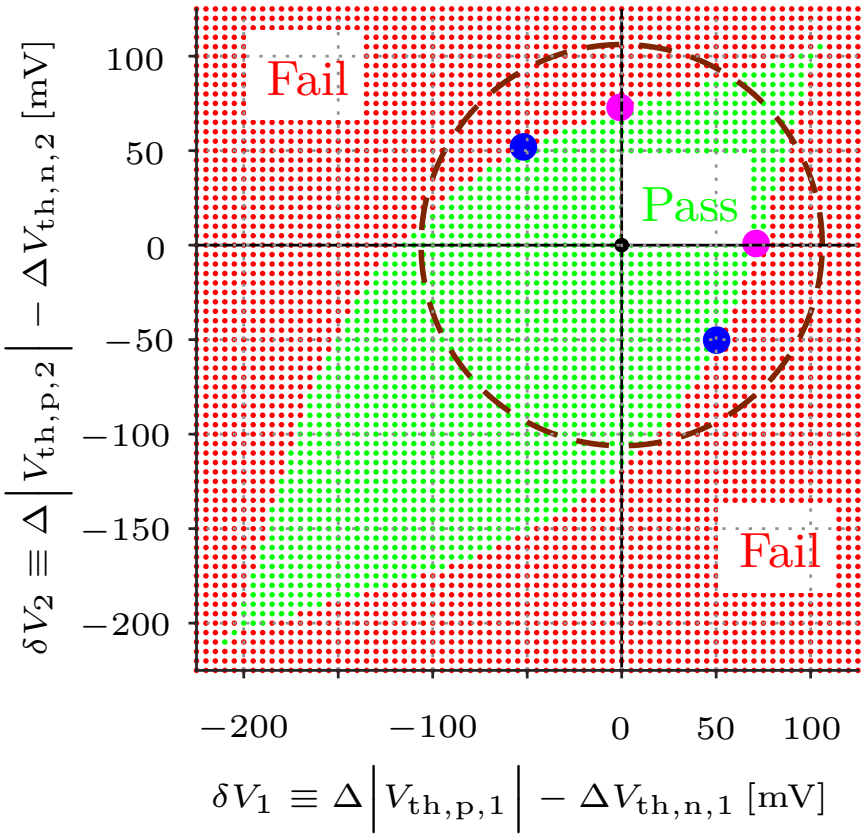
Failure Probability Prediction

"Propagate the randomness"



$$\sigma^2_{\delta V} = \frac{\left(n_{\mathrm{n}}^2\,\sigma^2_{V_{\mathrm{th,p}}} + n_{\mathrm{p}}^2\,\sigma^2_{V_{\mathrm{th,n}}}\right)}{(n_{\mathrm{n}} + n_{\mathrm{p}})^2}$$

Deterministic simulation ("DC sweep"):



Extraction of the failure *boundary* $g(\delta V_1)$.

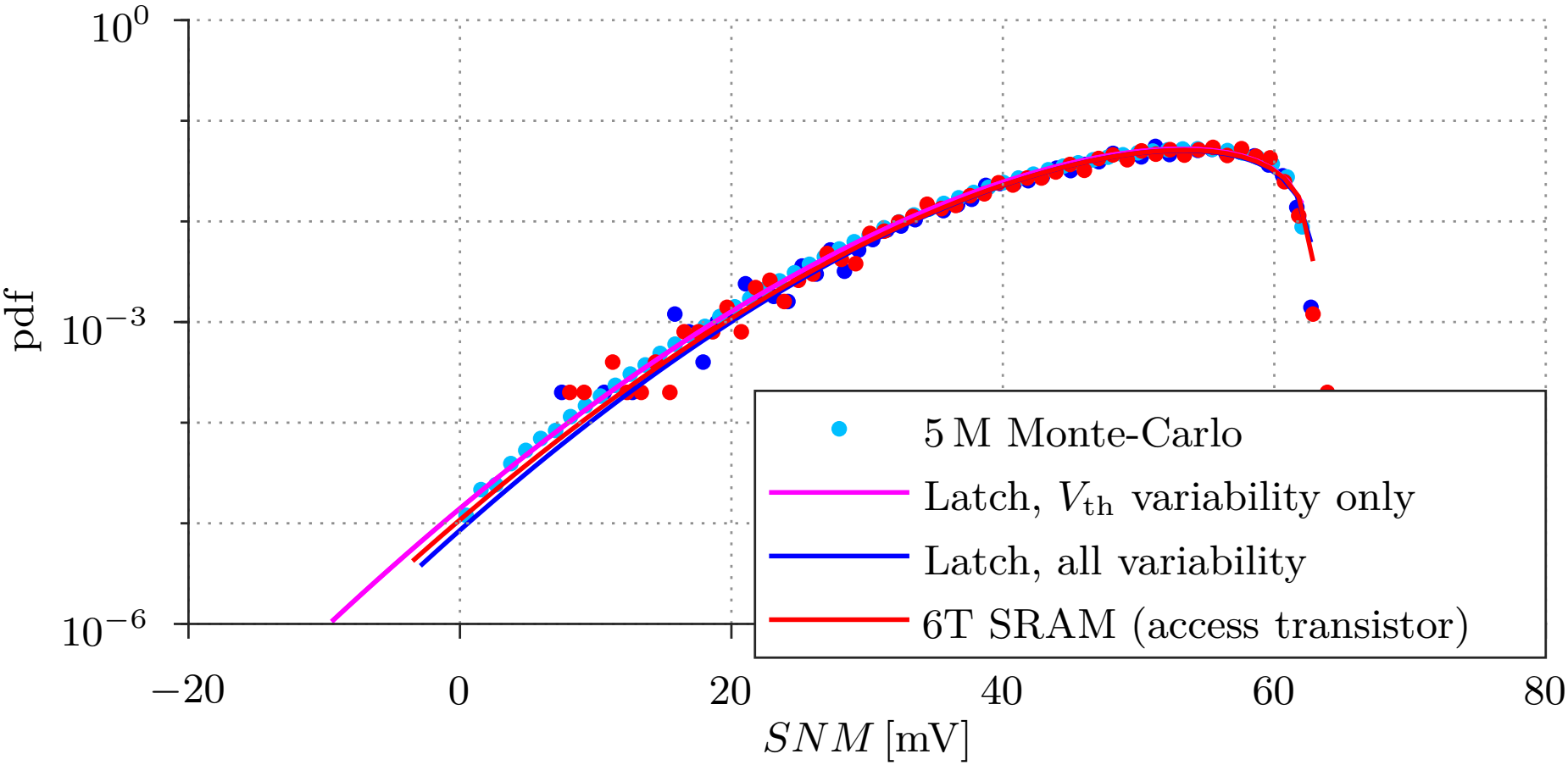
$\Longrightarrow$ (Almost) *exact* calculation of P_{fail}

$$= 2 \cdot \int_{-\infty}^{+\infty} \mathrm{d}\delta V_1\, f_{\delta V}(\delta V_1) \int_{-\infty}^{\boldsymbol{g(\delta V_1)}} \mathrm{d}\delta V_2\; f_{\delta V}(\delta V_2)$$

in **less than a minute**!

[Van Brandt et al., 2023, in preparation for TCASII]

Modelling Assumptions



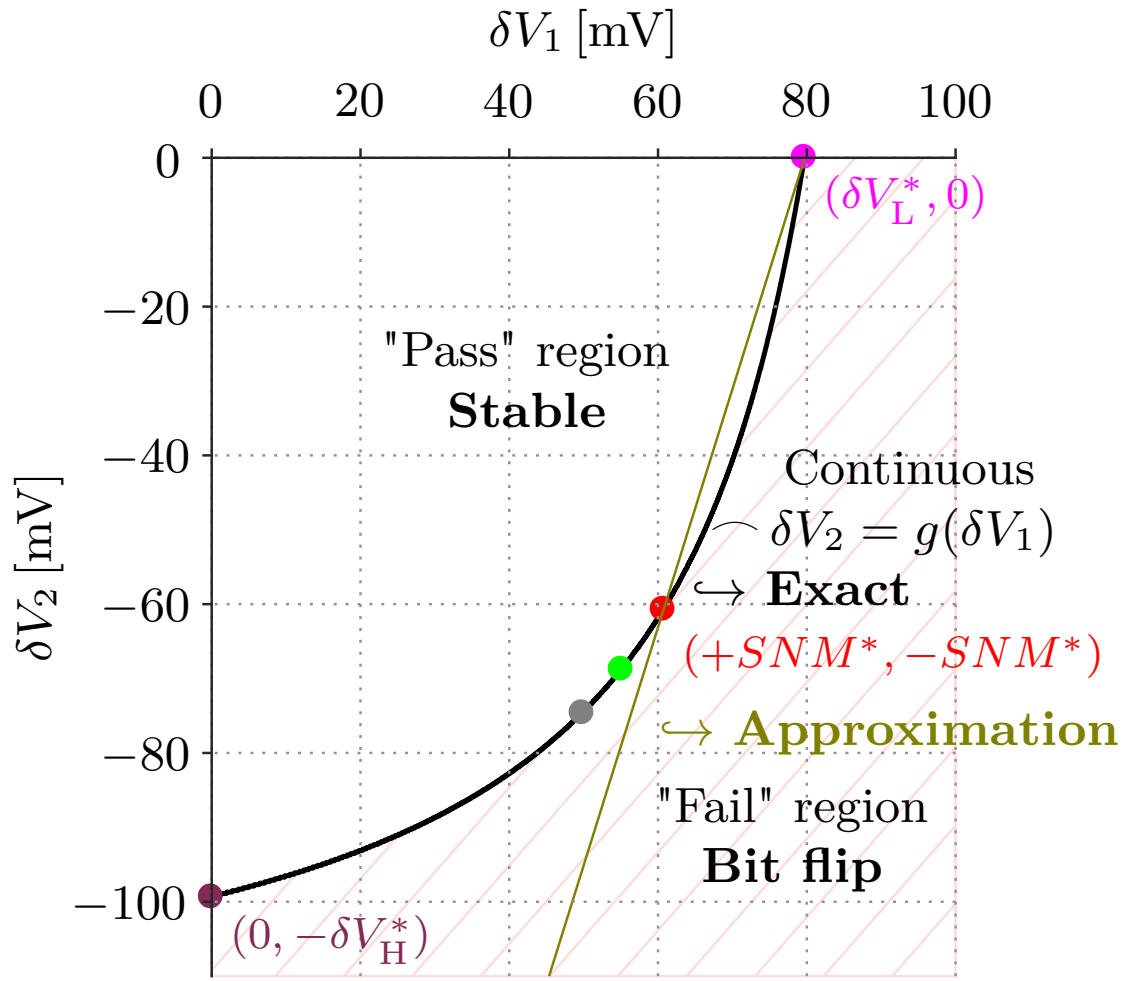
✓ The V_{th} variability strongly dominates the total variability.

✓ Modelling SRAM cell ≈ latch, in retention.

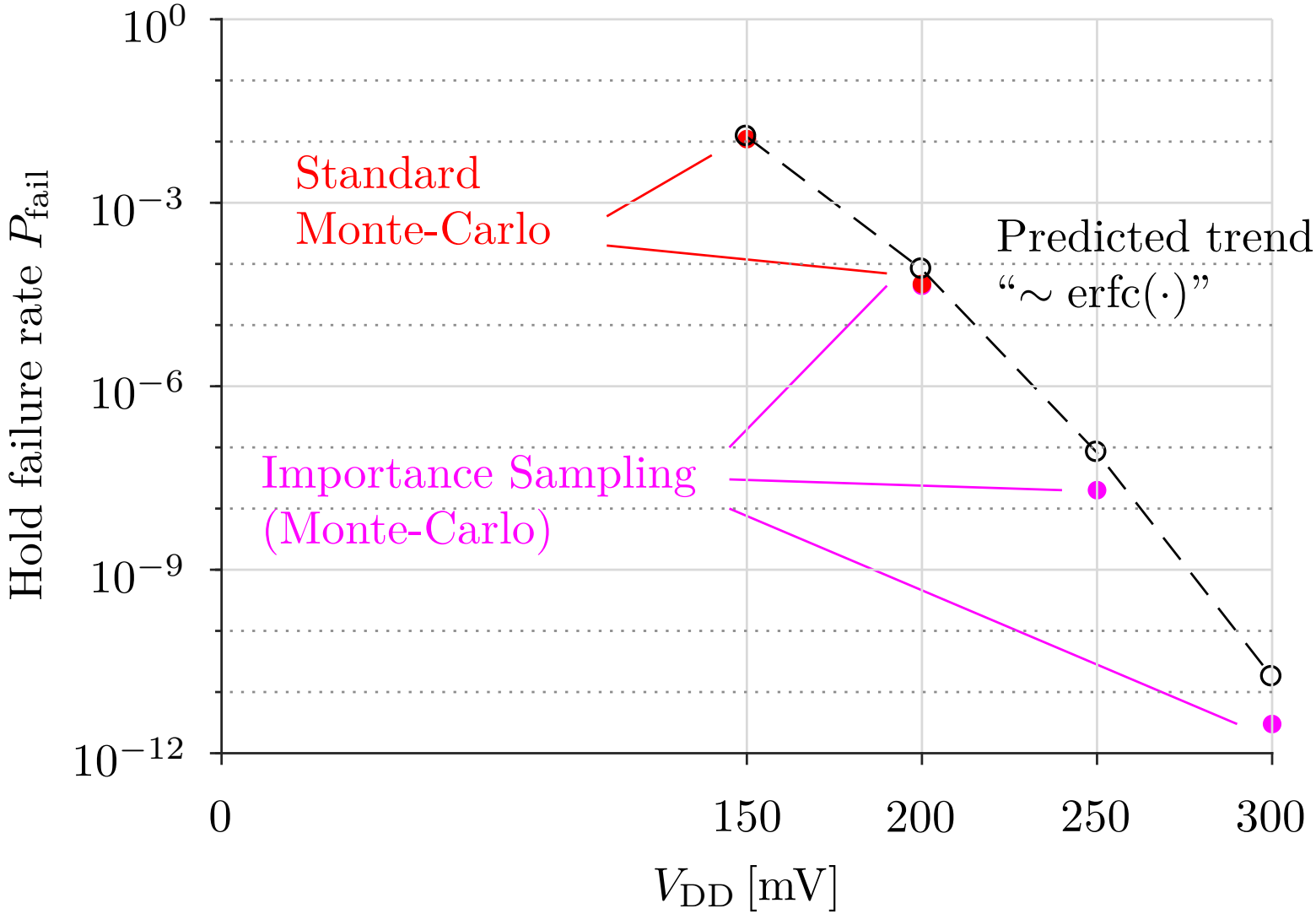
Approximated Closed-Form Formula

Using **only 2 DC simulations**! [Van Brandt et al., 2022, TCASI]

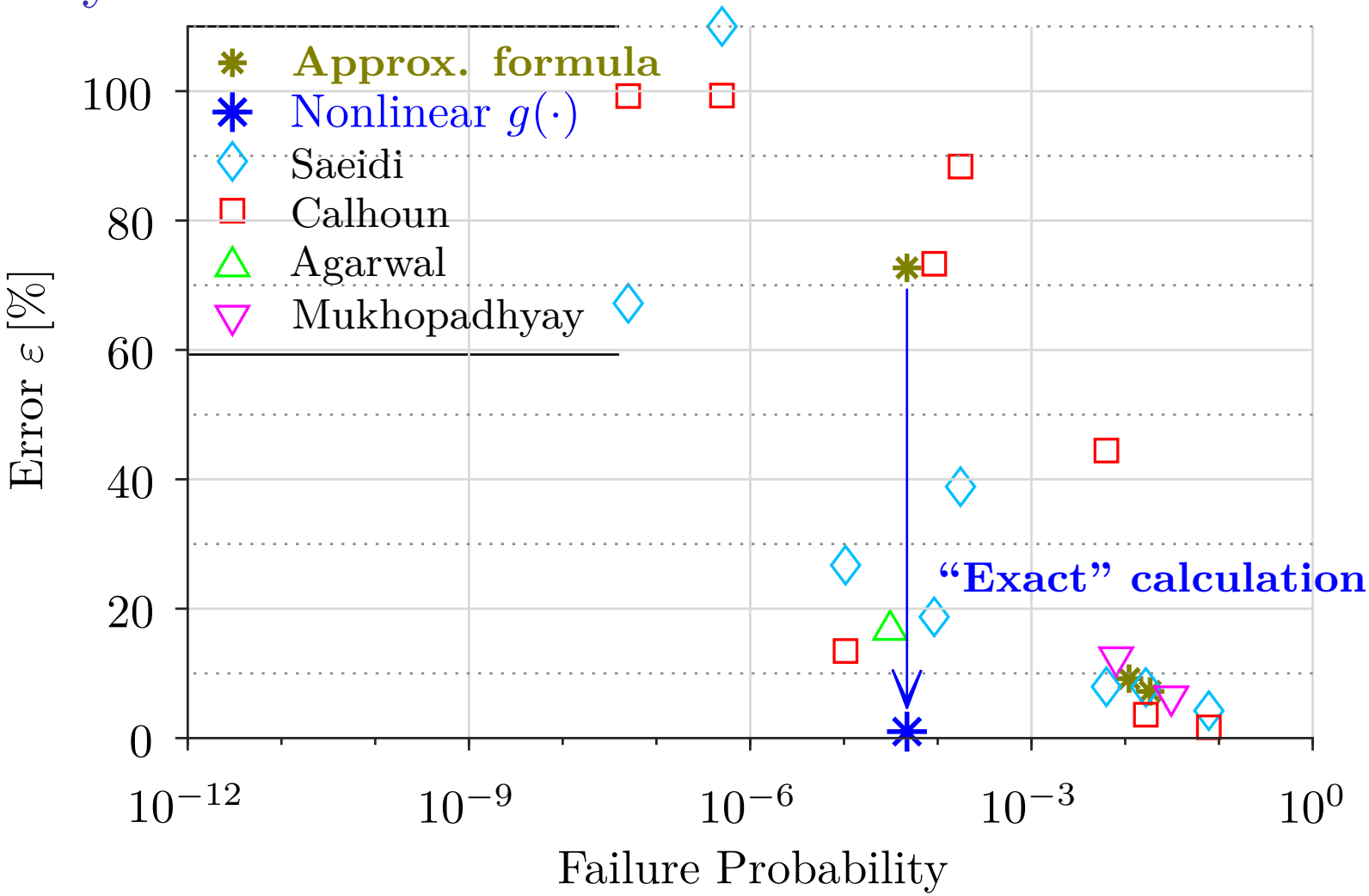
$$P^*_{\text{fail}} = \text{erfc}\left(\sqrt{\frac{2\,m^2}{1+m^2}}\,\frac{\delta V^*_{\text{L}}}{\sqrt{\sigma^2_{V_{\text{th,p}}} + \sigma^2_{V_{\text{th,n}}}}}\right) \quad \text{with } m = \frac{SNM^*}{\delta V^*_{\text{L}} - SNM^*}$$



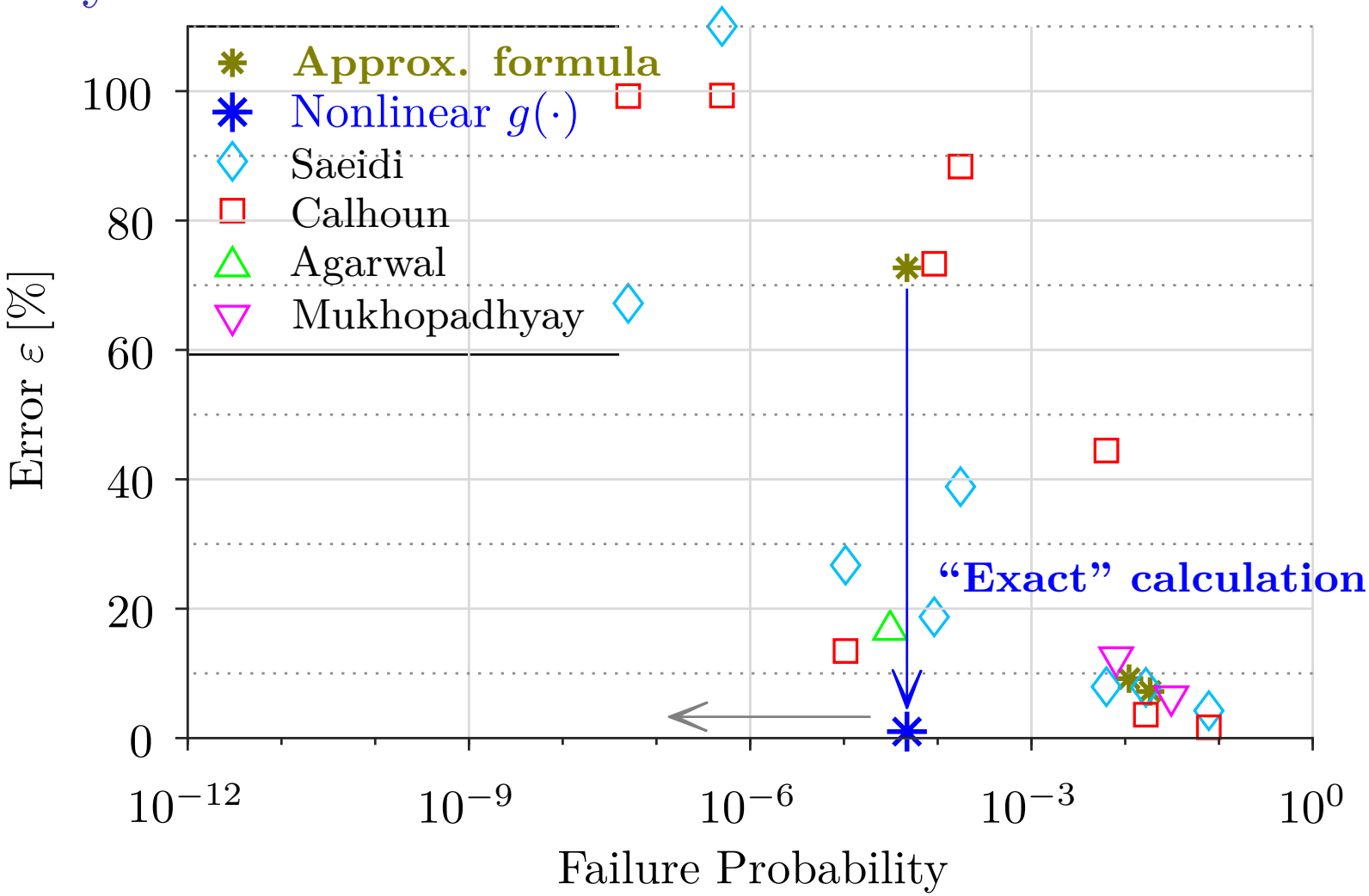
Application: Effect of the Supply Voltage Variation



Accuracy: Benchmark with Former Works



Accuracy: Benchmark with Former Works



Accuracy for P_{fail} down to the ppm still to be proven/confirmed

$\hookrightarrow$ further comparison with reliable importance sampling?

Conclusion and Perspectives

Summary:

- Latch retention robustness critical for subthreshold SRAM bitcells
- Monte-Carlo much too expensive for low failure probability (ppm)
- Novel non-Monte-Carlo methodology:
  deterministic circuit simulations + knowledge of V_{th} statistics

$\Longrightarrow$ P_{fail} calculated exactly in less than a minute!

Further work:

- Thorough comparison with enhanced Monte-Carlo methods (importance sampling), in terms of CPU time and accuracy.
- Generalisation to different and more complex architectures: access transistors, other ULV SRAM bitcells,...

Bibliography I

Agarwal, K. and Nassif, S. (2006). Statistical Analysis of SRAM Cell Stability. In *Proceedings of the 43rd annual Design Automation Conference*, pages 57–62.

Alioto, M. (2012). Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(1):3–29.

Bol, D., Schramme, M., Moreau, L., Xu, P., Dekimpe, R., Saeidi, R., Haine, T., Frenkel, C., and Flandre, D. (2021). SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6-3.6-μW/DMIPS 40-80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode. *IEEE Journal of Solid-State Circuits*.

Calhoun, B. H. and Chandrakasan, A. P. (2006). Static Noise Margin Variation for Sub-threshold SRAM in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, 41(7):1673–1679.

Chandrakasan, A. P., Daly, D. C., Finchelstein, D. F., Kwong, J., Ramadass, Y. K., Sinangil, M. E., Sze, V., and Verma, N. (2010). Technologies for Ultradynamic Voltage Scaling. *Proceedings of the IEEE*, 98(2):191–214.

Bibliography II

Jaiswal, A., Chakraborty, I., Agrawal, A., and Roy, K. (2019). 8T SRAM Cell as a Multibit Dot-Product Engine for Beyond Von Neumann Computing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 27(11):2556–2567.

Kulkarni, J. P., Kim, K., and Roy, K. (2007). A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM. *IEEE Journal of Solid-State Circuits*, 42(10):2303–2313.

Mukhopadhyay, S., Mahmoodi, H., and Roy, K. (2005). Modeling of Failure Probability and Statistical Design of SRAM Array for Yield Enhancement in Nanoscaled CMOS. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 24(12):1859–1880.

Saeidi, R., Sharifkhani, M., and Hajsadeghi, K. (2014). Statistical Analysis of Read Static Noise Margin for Near/Sub-Threshold SRAM Cell. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(12):3386–3393.

Seevinck, E., List, F. J., and Lohstroh, J. (1987). Static-Noise Margin Analysis of MOS SRAM Cells. *IEEE Journal of Solid-State Circuits*, 22(5):748–754.

Van Brandt, L., Bol, D., and Flandre, D. (2023). Exact Calculation of the Variability-Induced Failure Probability in Subthreshold CMOS Latches and SRAM. *IEEE Transactions on Circuits and Systems II: Express Briefs*. In preparation.

Bibliography III

Van Brandt, L., Saeidi, R., Bol, D., and Flandre, D. (2022). Accurate and Insightful Closed-Form Prediction of Subthreshold SRAM Hold Failure Rate. *IEEE Transactions on Circuits and Systems I: Regular Papers*, pages 1–14.