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A 2.24-pJ/bit 2.5-Gb/s UWB receiver in 28-nm FDSOI CMOS for low-energy chip-to-chip communications

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ABSTRACT

Chip-to-chip communications in high-performance applications such as server racks rely on wireline serial links. In this paper, we present a compact ultra-wideband receiver front-end in 28-nm FDSOI CMOS technology as a wireless interconnect alternative for low-energy and broadcast communications. It is based on binary pulse position modulation without guard interval using two periods of a 10-GHz carrier to reach 2.5-Gb/s datarate over distances >20 cm. The proposed receiver occupies 0.3 mm^2 (including decoupling capacitors) and consumes only 5.6 mW which results in an energy of 2.24 pJ/bit.

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1. Introduction

Nowadays wireline serial links are the most widely used technology for chip-to-chip high-performance communications thanks to their many advantages over parallel buses: routing simplicity, lower noise, power and pin count. They are widely used for the connection of the different components of a modern computer (CPU, GPU, storage devices, network interface card and other high-performance peripherals) [1], across server backplanes in datacenters, or to interconnect clustered processors. Peripheral Component Interconnect Express (PCIe) constitutes one of the major standards for high-speed wireline serial link communications.

Looking to the most aggressive designs [2], recent serial link transceivers can reach data rates above 28 Gb/s with energy consumption down to 6 pJ/bit. In such serial links, copper interconnects are used as transmission medium. Unfortunately, the channel RC characteristics limits is bandwidth (BW) and thus the system performance [2–3]. Therefore, communicating at a datarate above this BW requires more complexity and thus degrades the energy efficiency. Recently, wireless interconnects have thus been proposed as an alternative for this channel bottleneck, as they can provide higher energy efficiency for distances >1 cm, lower latency, better flexibility, lower system complexity, broadcasting capability and easier heat diffusion/cooling [3,4].

Because of previous advantages, we propose ultra-wideband (UWB) wireless communication as an alternative to high-performance wireline serial links, more specifically, to PCI-express for in-chassis server communications. UWB transmitters (TX) have shown record energy efficiency for short-distance [5–7]. However, the receiver (RX) for UWB is more complex than the TX and typically consumes much more power. Moreover, only a few previous works have used UWB for high-speed short-distance. [8] presents a 522-Mb/s UWB RX in 65 nm CMOS with 0.4nJ/bit within a few cm, [9] a 2-Gb/s UWB direct-conversion coherent TX in 90 nm CMOS with 75 pJ/bit at 3.4 cm and [10] an energy-efficient 25 pJ/bit UWB RX in 65 nm CMOS at 500 Mb/s at cm range.

In this paper, we also show that the energy efficiency of UWB can further be boosted for high-datarate short-distance communications with an energy below 3 pJ/bit at 2.5 Gb/s and 1-V voltage supply for the receiver when using an inductor-less non-coherent architecture in 28-nm FDSOI CMOS technology. FDSOI technology has been used as it allows efficient transistor control by biasing the substrate underneath the device. This is called back bias tuning. This tuning is used as a way to cancel system level PVT effects by continuously tuning the transistors threshold voltages [6]. The system architecture and communication protocol were analyzed in [11] and in this paper we discuss the circuit implementation, prototyping and measurement results. Section 2 presents the selected modulation. Section 3 unveils the design of the proposed low-energy UWB receiver. Section 4 outlines the experimental setup and Section 5 presents the main experimental results.

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2. Selected modulation scheme

The definition of a UWB signal does not specify a particular modulation scheme. Therefore, there is full freedom to choose the technique to generate the UWB signal. In [11], we analyzed various modulation schemes, which resulted in the following specifications:

- The transmitter (TX) output power is limited by the EMC regulations [12] so an extremely wide bandwidth (BW) without the restriction of a standard can be used.
- Non-coherent transmission/reception is chosen to target a higher RX energy efficiency because of its simplicity compared to its coherent counterpart.
- Binary pulse position modulation (PPM) without guard interval is selected over OOK (on-off keying) because of the better bit error rate (BER) at a given signal-noise ratio (SNR).
- A 10 GHz carrier frequency is used. Each PPM symbol consists of a pulse made of two carrier periods to enhance the pulse energy for SNR concern.
- Scrambling of the polarity of the TX pulses is used to cancel spectral lines, which allows to maximize the total TX output power without violating EMC regulations.

Fig. 1 shows the modulation signal. The limit on the maximum emitted power in Fig. 1(b) is given by EMC limitations considering a 0-dBi gain TX antenna. Fig. 1(b) also shows the FCC indoor mask. From this graph, we can see that the PPM waveform whose output power is set to meet the EMC regulations violates the −75.3dBm/MHz limit in the 0.96–1.61 GHz band but in practice the TX output will be filtered by the effect of the antenna and/or by using a pulse shaping PA at the TX side [6]. The slight violation of the −51.3dBm/MHz limit above 10.6 GHz can be fixed by fine adjustment of the TX output power. The TX output power, RX sensitivity and signal attenuation determine the maximum communication distance. Assuming an attenuation of 10 dB at 30 cm distance [13] and considering both matching losses and fine TX output power adjustment, we can expect an RX signal 15–20 dB below the PPM waveform. This gives an RX input PSD peak value between −62 and −67 dBm/MHz for a 30 cm transmission distance that corresponds to a required RX sensitivity between −28.0 and −32.5 dBm (integrated in the 5–15 GHz BW).

3. UWB receiver design

The architecture of the proposed RX is shown in Fig. 2. A non-coherent topology based on energy detection is used. First, the RF front-end amplifies the received signal through a low-noise amplifier (LNA) and down converts it to baseband with rectification performed by a self-mixing squarer. In the baseband part, a

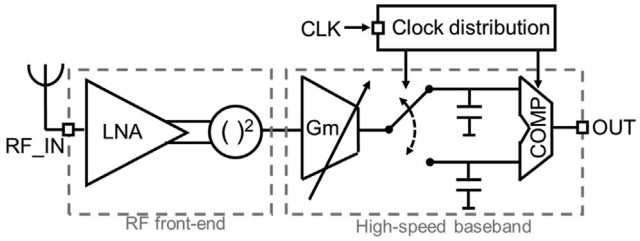


Fig. 2. UWB receiver block diagram.

Gm-C topology is chosen for energy detection because of its high frequency versus power performance. A variable-gain Gm block amplifies the signal, which is integrated on capacitors for each symbol PPM time slot. A relative comparison of integrated signal power in the two PPM time slots allows the demodulation of the transmitted symbol. A 2.5-GHz clock signal is necessary to generate the required control signals for the baseband part operation.

It is important to mention at this point that the possibility to apply external back bias control has been added in the design for mitigating the effect of PVT variations. In particular, a specific back-bias control node has been added for the LNA as this is the most critial block and a common back-bias control node has been added for the high-speed baseband and squarer. In consequence, in this section, simulation results are presented for the nominal process corner and back bias only, knowing that the back bias tuning scheme will take care to align the actual chip performance with the nominal ones such as explained in [6].

Let us now detail the main blocks that constitute the low-voltage low-power RX.

3.1. Low-noise amplifier (LNA)

An efficient UWB LNA is a key component of the receiver because of its highly-demanding performances: broadband input matching, low noise figure (NF) to improve the sensitivity of the receiver, high gain to reduce the noise requirements of the subsequent blocks and low-power consumption. To avoid the burden of RF inductor integration with respect to UWB operation and chip area density, we aim for an inductorless LNA topology. A balun LNA is designed to benefit from advantages of a differential topology such as robustness to power supply and substrate noise, while keeping the compatibility with low-cost single-ended antennas.

Fig. 3(a) shows the proposed LNA [14]. It is based on the common-gate common-source (CG-CS) noise cancelling LNA [15,16]. It minimizes the thermal noise I_{n1} of the M_1 transistor at the output because it appears in phase at the differential outputs while the input signal appears in phase opposition at the differential outputs. A cascode transistor is added to increase the voltage gain and reduce the Miller effect related to the gate-drain

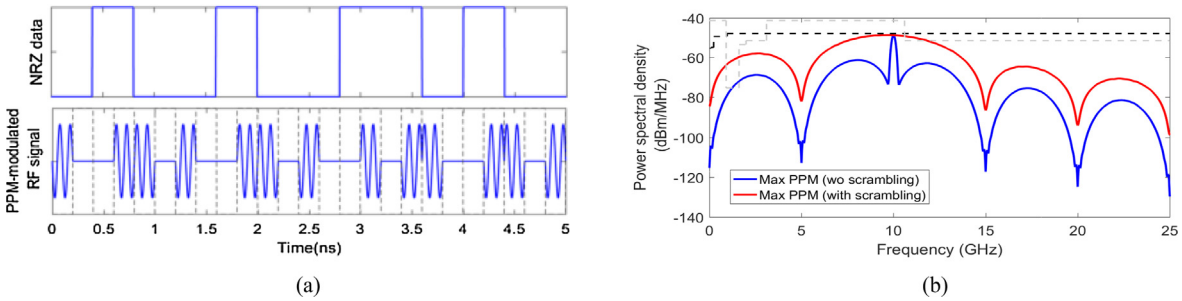


Fig. 1. Pulse position modulation signal with scrambling in the (a) time domain and (b) frequency domain. (NRZ-Non return to Zero data). Black dotted line shows the EMC limitation and grey dotted line the FCC standard.

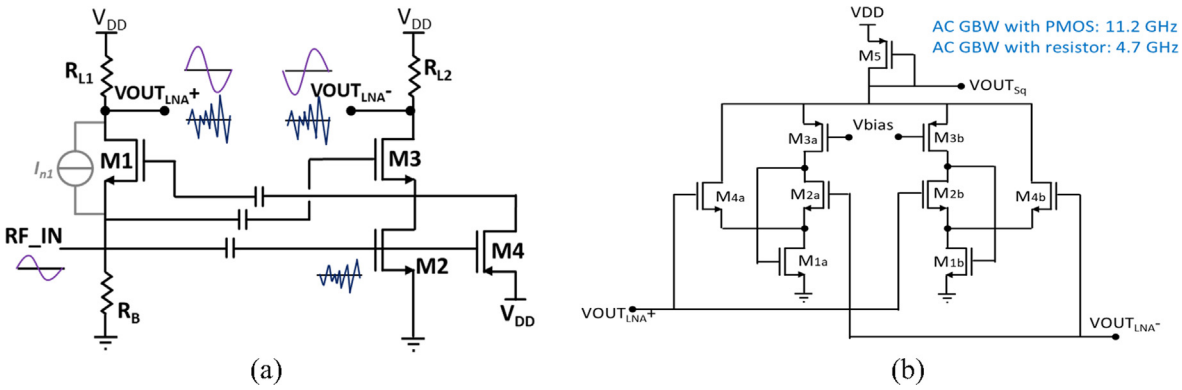


Fig. 3. (a) Proposed noise-cancelling LNA schematic; (b) Squaring circuit schematic.

capacitance of transistor M_2 [15]. A further optimization is achieved by cross-coupling the CG-CS LNA, which mitigates the tradeoffs between impedance matching, gain and noise [17]. Finally, a new version of the derivative superposition technique [18] has been used to reduce the linearity limitation, thus allowing to improve noise, BW and gain performance at the same time. This modification consists in the inclusion of an auxiliary PMOS transistor (M_4) in parallel with the CS transistor (M_2) but operating under different conditions. It improves the linearity-noise-BW tradeoff at the cost of a small increase of the power consumption. It also improves input impedance and gain [14]. The effect of the added PMOS transistor on the noise, linearity, input impedance and gain-BW product is shown in Fig. 4(a,b,c). To avoid the use of large, imprecise and narrow-band on-chip inductors, a resistor R_B is used to bias the CG stage at the expense of some voltage headroom.

With an S_{11} lower than −10 dB for the whole BW, the proposed LNA topology provides 16 dB of gain (Fig. 4(c)), 10.3 GHz of BW, 3.5 dB of noise figure and 2.1 mW of power consumption, under 1 V, and only using 900 μm^2 area, which makes it a better alternative than state-of-art LNAs.

3.2. Self-mixing squarer

Both rectifiers and squarers can be used to perform signal power detection. To avoid the use of Schottky diodes that are slow and not widely available in standard CMOS technologies, we selected a self-mixing approach, which exploits the quadratic-law behavior of MOS transistors in saturation. To achieve conversion gain in the squaring operation, we selected an active mixer [19].

The squarer circuit, similar to the one proposed in [20], is shown in Fig. 3(b). A flipped-voltage follower topology is used as a floating voltage follower for the squarer thanks to its ultra-low output resistance but also allows the squarer to operate at the low 1-V supply voltage used in the proposed receiver. The square current is transformed into voltage by means of a diode-connected transistor (M_5). The use of a diode-connected transistor instead of a resistor improves the transient gain of the topology. Transistors $M_{3a,b}$ operate as current mirrors. Even though not shown in the figure for simplicity, AC coupling capacitors are used to block the static DC offsets propagation.

Fig. 5 shows the operation of the squarer. A low power consumption of 200 μW (>3 times lower than [20]) is achieved with the used topology without limiting the BW of the full RX system and with a reduced area of 2000 μm^2.

3.3. Variable-gain Gm block

The signal generated by the squarer needs to be amplified and integrated independently over both PPM time slots to detect their energy. A tunable Gm block is used with integrating capacitors to provide variable gain control. The proposed Gm block, shown in Fig. 6, uses a two-stage cascode current mirror. In the first stage, the current is copied from the squarer by means of transistor M_1. Then a cascode current mirror further copies and amplifies the current flowing through M_1. The cascode topology increases the gain and BW at low power. The 3-bit ($B_{0\text{-}2}$) digital gain tuning (externally controlled) is implemented as follows: transistor M_4 is always on; by turning on or off transistors $M_{7a\text{-}c}$ acting as switches, we increase the current amplification. Fig. 6 right shows the voltage gain considering an output load of 35-fF integrating capacitance (shown in Fig. 2) as well as the power consumption as a function of the control bits $B_{0\text{-}2}$. It provides a maximum AC voltage gain of 17.5 dB with a minimum BW of 2.75 GHz and a maximum power consumption of 1.6 mW. This control can also be used as a way to mitigate gain variation due to PVT.

3.4. Mixed-signal baseband integrator and demodulation

Fig. 7 shows the designed mixed-signal baseband integrator and demodulation block. This block provides the demodulated signal by comparing the pulse energy in two adjacent PPM time slots.

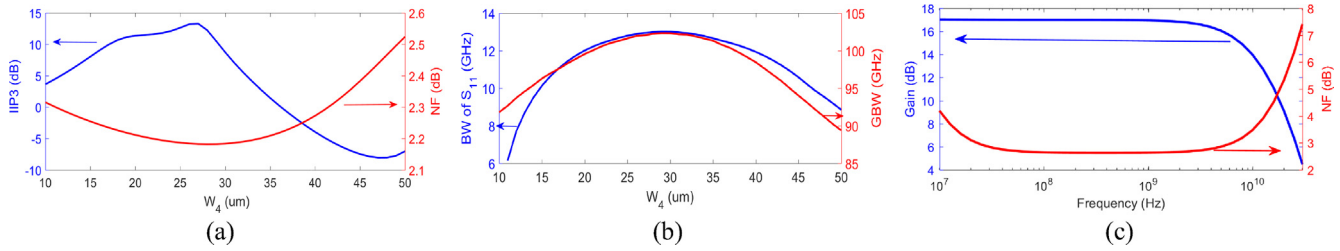
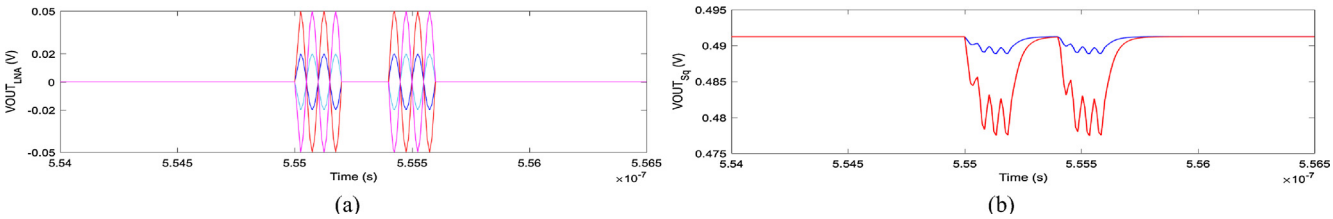


Fig. 4. (a) Impact of M4 PMOS transistor width on the LNA performances: IIP3 and NF (b) BW of S_{11} and Gain-BW product (GBW). (c) Gain, and NF versus frequency of the LNA.



(a) (b)

Fig. 5. Squarer circuit performance with 10 GHz sinusoidal carrier and 2.5 Gb/s transmission. Two different input amplitudes are shown: in blue color 20-mV amplitude signal and in red color 50-mV input amplitude signal.

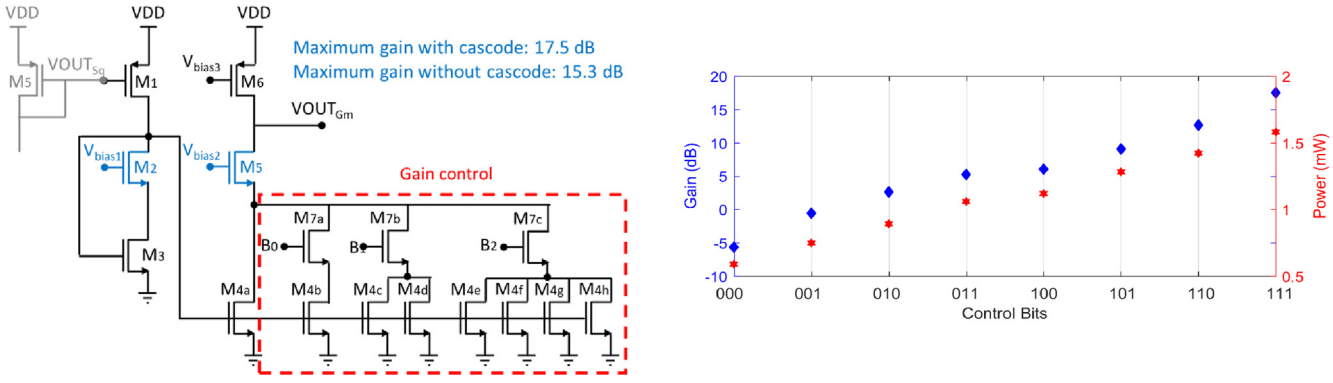
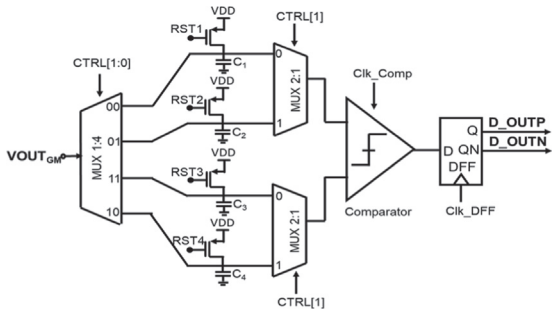


Fig. 6. Gm block schematic and Gm gain and power consumption as a function of control bits.



	CTRL[1:0]	C_1	C_2	C_3	C_4
T1 (0 ps)	00	Integrate	Reset	Hold	Hold
T2 (200 ps)	01	Hold	Integrate	Reset	Hold
T3 (400 ps)	11	Hold	Hold	Integrate	Reset
T4 (600 ps)	10	Reset	Hold	Hold	Integrate
T5 (800 ps)	00	Integrate	Reset	Hold	Hold
T6 (1.0 ns)	01	Hold	Integrate	Reset	Hold
T7 (1.2 ns)	11	Hold	Hold	Integrate	Reset

Fig. 7. Proposed mixed-signal baseband integrator and demodulation.

The proposed design is based on the one described in [11], but only two phases of an external 2.5-GHz clock are needed for the operation of the multiplexers 1:4 (MUX1:4).

To achieve rapid acquisition, uninterrupted time-adjacent integration windows are needed. Therefore, an interleaved architecture is proposed by using 4 integrating capacitors (instead of the 2 required) and an analog multiplexer 2:1 (MUX2:1) to divide by 2 the required operating speed. A MUX1:4, implemented by NAND gates and switches (using standard CMOS topologies), connect the input with each of the 4 integrating capacitors so that the integrated signal during the first and second time slots is accumulated onto separate capacitors C_1 and C_2 (or C_3 and C_4). As shown in the table in Fig. 7, the four capacitors rotate among three states: Reset (the capacitor is charged to V_{DD}), integrate (the Gm block delivers to the capacitor a current proportional to the signal power in that time slot), and hold (the output voltage is kept on the capacitor).

A simple standard high-speed dynamic comparator [21] driven by another control signal (Clk_comp) can detect which input is the largest and hence perform the pulse position demodulation. This comparator provides negligible static power consumption and less than 15 μW total power under dynamic operation. A true single-phase clocked (TSPC) D flip-flop (DFF) is added after the comparator to sample the data and generate its inverse. TSPC-DFF only uses one phase of the clock resulting in a simple structure allowing high-speed low-power operation [22].

A single input clock with a frequency of 2.5 GHz is required for the generation of the different control signals necessary for the correct operation of the whole receiver (Fig. 7). The other required control signals are generated on-chip from this one by means of DFFs, XOR gates and inverters. For test purposes in this prototype this clock will be externally applied, but a low power clock recovery is planned to be included in the future. Considering the state-of-art, a power consumption less than 2 mW is expected for a low-power PLL-based clock recovery system [23].

3.5. Output driver

An output driver is used for experimental purpose to achieve 50-Ω output impedance. Its schematic is shown in Fig. 8. A 1.8-V voltage supply is used for the I/Os to achieve higher gain and easier matching. The output driver is a simple topology consisting of two inverters to adapt the output signal to the higher voltage supply and a differential pair with 50-Ω on-chip polysilicon output resistances to easily achieve the required 50-Ω output impedance.

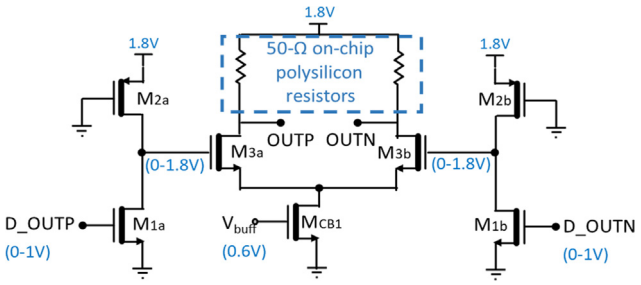


Fig. 8. Output driver schematic based on I/O transistors.

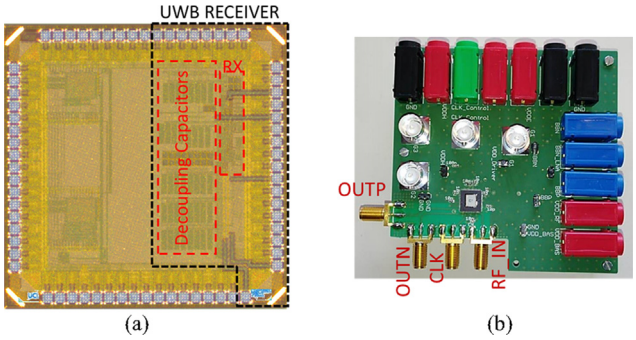


Fig. 9. (a) UWB receiver chip microphotograph with the layout superimposed and (b) PCB for measurements.

Low-V_t I/O transistors have been used to implement the output driver.

4. Testchip prototype and experimental setup

Fig. 9(a) shows the designed layout of the UWB RX. It was fabricated in a 28-nm FDSOI CMOS technology under 1-V voltage supply using exclusively low-V_t (LVT) transistors and occupies an active area of only 0.3 mm^2 (only 343 $\mu m \times 63\ \mu m$ if we exclude the decoupling capacitors). The die was packaged in QFN64 and mounted onto a PCB board (shown in Fig. 9(b)) specifically designed for high-frequency operation: Rogers 4000 series material, 50-Ω matched input and output paths, 4-layer PCB where the first one is saved for the RF signals, the second one is all grounded for isolation and layers 3 and 4 are used for DC signals distribution. Several tuning voltages such as Gm gain variation control bits or different back bias controls are used for test purposes and PVT effects mitigation as mentioned in Section 3. Two RF inputs (signal and clock) and two differential outputs use high-frequency SMA connectors.

As no commercial off-the shelf 10-GHz PPM UWB TX is available for the selected communication scheme, we aimed at generating the TX RF signal with the high-speed I/Os of modern FPGAs. Fig. 10 shows the experimental setup. A Xilinx Kintex UltraScale XCVU095 FPGA within a Xilinx VCU108 development board is used to generate the transmitted pulses. Fig. 11 describes the operation of the FPGA. In order to generate a 2.5-GHz clock channel with 200-ps pulse shaping in the data channel, transceivers operating at a 20-Gb/s data rate are required. The GTY transceivers [24] in the Kintex UltraScale XCVU095 FPGA meet this constraint and are

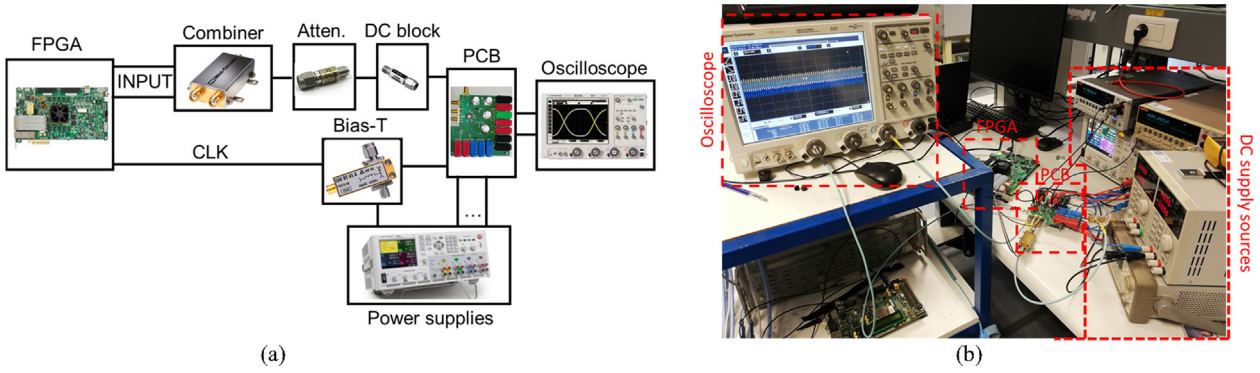


Fig. 10. (a) Block diagram of the experimental set-up and (b) photograph.

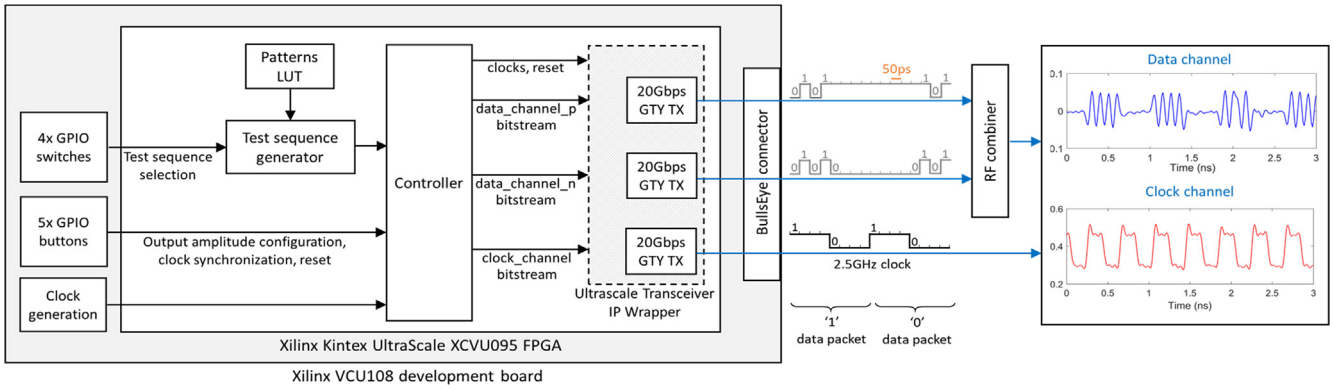


Fig. 11. Test setup for high-frequency data and clock signal generation for the proposed receiver.

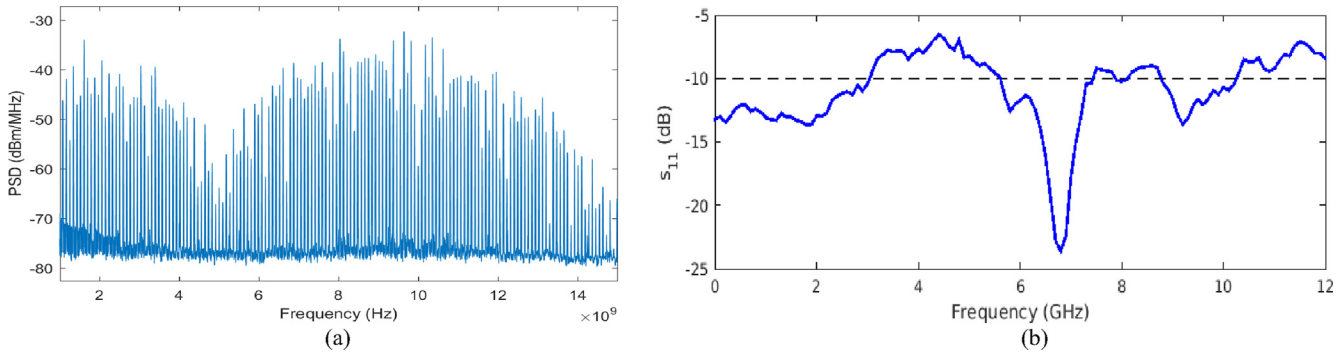


Fig. 12. (a) Spectrum of the signal generated by the FPGA for a pseudorandom bit sequence of 2^5-1. The spectrum is measured at the output of the combiner. (b) Measured input matching of chip with packaging and setup parasitics (no de-embedding is performed).

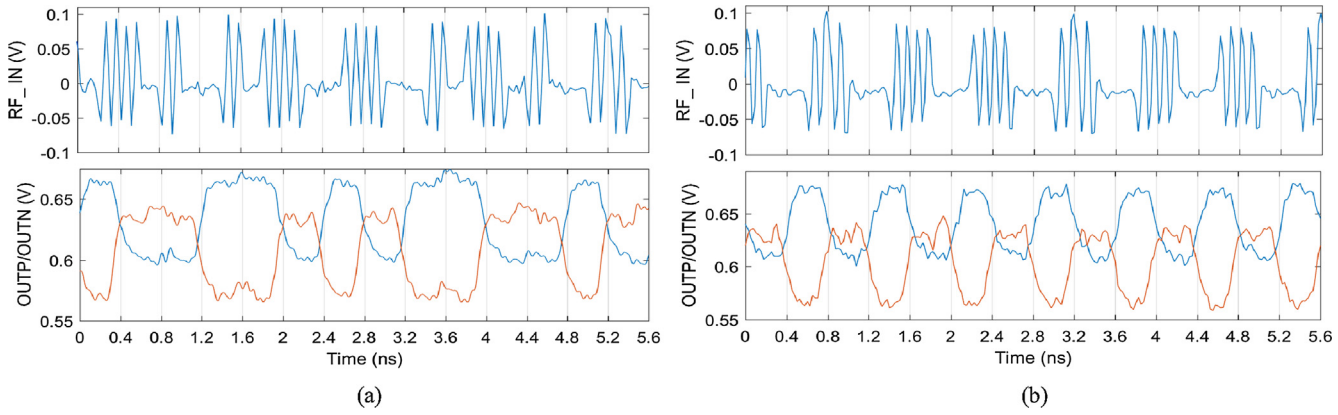


Fig. 13. Typical input and output signals for the UWB receiver. (a) A pseudorandom bit sequence is used and (b) a 1010 pattern is used for easier visualization and configuration.

configured using a Xilinx Ultrascale Transceiver IP [25]. Combining two binary sequences with an RF combiner allows for the generation of oscillating pulses.

Test sequences consisting of different combinations of data packets with PPM encoding (i.e. all zeros, all ones, random or alternating ones and zeros) and with random pulse scrambling can be selected. The output amplitude of the clock and data channels can be configured independently by changing the output power configuration of the GTY TXs, while the clock phase shift can be adjusted for compensation of the RF combiner delay. Example streams for the generation of a one-zero packet sequence are shown in Fig. 11; the associated measurements are provided on the right.

A special BullsEye adapter from SAMTEC (20 contacts, 20 GHz) is necessary to transmit the signals from the output BullsEye connector from the FPGA to SMA inputs with 20-GHz BW. The two differential signals are combined using a ZX10-2-183+UWB (1.5 to 18 GHz) RF splitter/combiner from Mini-Circuits. Fig. 11 shows an example of the combined signal for the case where 1010 data packets are transmitted. Fig. 12(a) shows the spectrum generated by the FPGA when a pseudorandom signal of order (2^5-1) is generated. As the output power generated by the FPGA is too high for the RX, a 20-dB Wiltron coaxial K connector 41KC-S attenuator (DC to 40 GHz) is used after the combiner. A DC blocking capacitor 11742A from Agilent is needed after the attenuator to block DC signals below 45 MHz letting signals up to 26.5 GHz pass.

The FPGA also provides the 2.5-GHz clock signal necessary for the receiver operation. Let us recall here that a synchronization mechanism would be required in a practical application. As stated in Section 3.4, a low-power PLL-based clock recovery system could be used to this end [23]. A Bias-T (SHF BT45-B) from 20 kHz to 40 GHz is used to shift the input clock DC level. The signal at the output of the Bias-T is directly taken to the PCB input clock. The DC supply voltages are generated with a DC Power Analyzer N6715B.

Finally, the two differential outputs from the PCB are acquired by a real-time 16-GHz oscilloscope DSOX91604A from Agilent. Although not shown in Fig. 10, for S_{11} measurements, we used a Vector Network Analyzer from Agilent (VNA PNA-X N5242A) that works up to 26.5 GHz with 130 dB dynamic range.

5. Experimental results

The prototyped low-energy UWB RX consumes 5.6 mW at 1 V: 2.1 mW for the RF front-end (dominated by the LNA) and 3.5 mW for the baseband (dominated by the Gm).

Operation at 2.5 Gb/s was verified by transmitting various RF signal patterns generated by the FPGA-based setup to the UWB RX. Fig. 13 shows two typical temporal measurement sequences of input signals and data demodulated by the RX: (a) pseudorandom pattern and (b) 1010 pattern. The results show how the receiver successfully recovers the transmitted data. Although not plot here, the spectrum of the output signal is that of a pseudorandom bit sequence, i.e. a *sinc* function.

Fig. 12(b) shows the measured input matching (S_{11} parameter) of the receiver. The measurement was done with the packaged die on the PCB, connected to SMA connectors through a transmission line designed for ideally 50-Ω match. Wirebond interconnection has been used in this design. The degraded performance of the

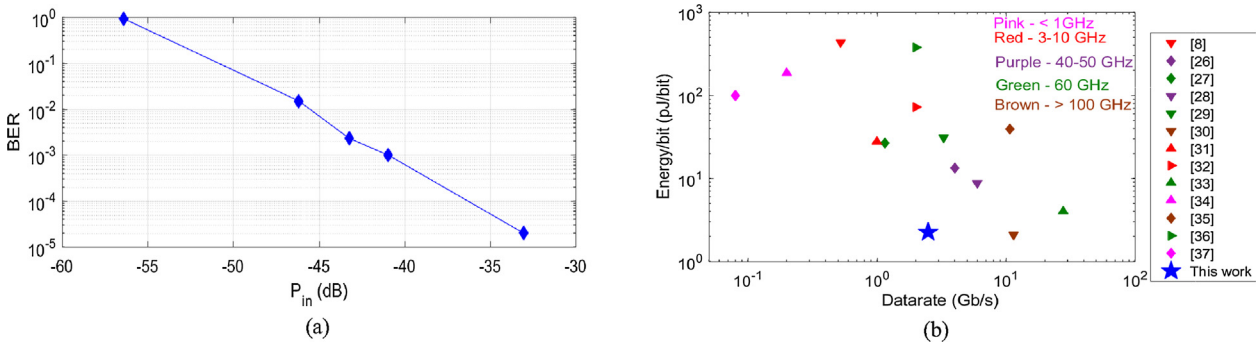


Fig. 14. (a) BER versus input power. (b) Energy/datarate tradeoff.

matching (S_{11} > −10 dB in part of the 5–15 GHz band of interest and shifted peak) is due to the RLC parasitics of the chip package, PCB and connections as no de-embedding was performed for this measurement. Another source of error might also be the die-package interconnection. In fact, simulation results show that a simple package model constituted by bondwire self-inductance (as well as mutual inductance), and RLC parasitics of the chip package can indeed lead to the measured degradation. This should be corrected in a future design.

Sensitivity analysis is performed by measuring bit error rate (BER) values as a function of the input signal level (Fig. 14(a)). BER measurement is done by using a known input pattern and comparing it with the output by using a Matlab code. For a BER of 10^{-3}, the measured sensitivity (considering the total integrated power in the BW) is −40.5 dBm. Taking into account the channel attenuation, antenna gain and matching losses (see Section 2), this would correspond to a transmission distance higher than 30 cm. It is important to mention that the sensitivity value extracted from SPICE simulations with ideal TX signal as in Fig. 1 with additive white Gaussian noise (AWGN corresponding to the thermal noise level on the 50-Ω antenna impedance over 10 GHz at 25 °C) is −47.3 dBm. The 6.8 dB difference is mostly due to the experimental TX signal and PCB channel imperfections resulting in the clear RX input signal distortion visible in Fig. 13, compared to the ideal signals from Fig. 1. In addition, the actual sensitivity of the RX is better than the measured one as the RX input power level was measured by connecting the TX output directly to the oscilloscope which features excellent 50-Ω matching whereas in our RX, losses occur due to the impedance matching imperfections due to the parasitics of chip package, PCB and connections, visible in the imperfect S11 parameter from Fig. 12(b).

Although this prototype is proposed as an alternative to PCI express standard, it is really competitive with state-of-art high-speed wireless RX chips. Table 1 shows a comparison with state-of-art. It achieves an excellent 2.24-pJ energy per bit, while preserving a relatively low carrier frequency with respect to the achieved datarate, which is an advantage with respect to SoC integration in processor, router or storage chips. Only the RX from [30] achieves a slightly lower (8%) energy per bit but requires BiCMOS technology, has 4 × active power and operates at 130 GHz, which are three hurdles for SoC integration.

Fig. 14(b) shows the energy vs. datarate tradeoff of state-of-art wireless receivers for short-distance communication (i.e. less than 1 m) [8, 26–37]. We can see the trend of better energy efficiency at higher datarates thanks to amortization of fixed power contributions over more bits. However, the proposed low-energy UWB receiver is competitive with receivers operating at 10 × the datarate, thanks to the simple non-coherent topology and the lower carrier frequency.

As the UWB RX was designed as a low-energy alternative to wireline serial links, let us compare it to state-of -art wirelines RXs. There are some research wireline RXs that have similar energy efficiencies [38–39]. However, the de facto standard is PCIe link and to the authors' knowledge, the best receivers for PCIe links require 25 pJ/bit for Generation 1/2 [40] and 27.9 pJ/bit for Generation 3 [41]. Therefore, the proposed wireless receiver achieves better energy efficiency as well as all the advantages of wireless systems as described in Section 1 (lower latency, broadcast capability, higher flexibility, etc.).

6. Conclusions

In this paper we proposed, described and validated an UWB RX for chip-to-chip communications, as a low-energy alternative to wireline serial links with the additional advantages of wireless communications, such as broadcast capability and easier connectivity.

Table 1
Comparison with high-speed receivers for chip-to-chip communications.

	This work	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]
Tech.	**28-nm FDSOI**	90-nm CMOS	90-nm CMOS	180-nm SiGe BiCMOS	90-nm CMOS	55-nm BiCMOS	65-nm GP CMOS	130-nm CMOS	28-nm CMOS
RX content	**RFFE +BB**	RFFE	RFFE +BB	RFFE +BB	RFFE + BB	RFFE + BB	RFFE +BB + CG	RFFE +CG	RFFE +BB + CG
Mod.	**PPM**	OOK	16 QAM	BASK	OOK	OOK	BPSK	BPSK	QPSK
Embedded synchro.	**No**	No	No	No	No	No	Yes	Yes	No
Carrier frequency	**10 GHz**	45 GHz	60 GHz	43 GHz	60 GHz	130 GHz	3.5 GHz, 4.5 GHz, 5.4 GHz	6–10 GHz	60 GHz
BW	**10 GHz**	10 GHz	640 MHz	6.3 GHz	8 GHz	15 GHz	7.5 GHz	4 GHz	>8 GHz
Datarate	**2.5 Gb/s**	4 Gb/s	1.152 Gb/s	6 Gb/s	3.3 Gb/s	11.5 Gb/s	1 Gb/s	2 Gb/s	27.8 Gb/s
Distance	**30 cm**	55 cm	25 cm	2 cm	60 cm	50 cm	1 cm	50 cm	13 cm
Active area	**0.02 mm²**	0.7 mm²	3 mm²	0.62 mm²	0.68 mm²	0.4 mm²	4.6 mm²	6.4 mm²	3.9 mm²
Power	**5.6 mW**	200 mW	31 mW	52.5 mW	103 mW	24 mW	27.8 mW	145.8 mW	110 mW
Energy/bit (pJ/bit)	**2.24**	50	26.9	8.75	31.2	2.1	27.8	72.9	6.8

BB = Baseband, CG = Clock generator, RFFE = RF front-end.

A non-coherent transmission/reception is used with PPM using a 10-GHz carrier and allowing a datarate of 2.5 Gb/s. The proposed low-energy UWB receiver, designed in a 28-nm FDSOI CMOS technology, consists of a UWB low-noise amplifier, a self-mixing squarer, a variable-gain G_m block and a mixed-signal baseband demodulator. This non-coherent topology allows us to achieve a low power consumption of 5.6 mW at low voltage operation (1 V power supply). This indicates the potential of UWB for low-power high-speed communications. The proposed receiver also achieves better energy efficiency than state-of-art PCIe receivers, which validates the wireless alternative to wireline serial links.

The prototype demonstrated an energy efficiency of 2.24 pJ/bit at 2.5 Gb/s. Therefore, it is, to the authors' knowledge, the most energy-efficient UWB RX working at 2.5 Gb/s and is competitive with the energy efficiency achieved by much higher datarate RXs in the literature, which amortize their significantly higher power consumption over more bits per second. The proposed low-voltage low-power receiver also provides lower area, mainly due to the inductorless topology which facilitate SoC integration in an advanced (but standard) CMOS technology.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] Saadé J, et.al. A system-level overview and comparison of three high-speed serial links: USB 3.0, PCI Express 2.0 and LLI 1.0. IEEE DDECS, 2013.
[2] Daly DC, Fujino LC, Smith KC. Through the looking glass-the 2018 edition. IEEE Solid-State Circ Mag 2018;2018:30–46.
[3] Laha S et al. A new frontier in ultralow power wireless links: network-on-chip and chip-to-chip interconnects. IEEE Trans Comp-Aid Des Integ Circ Syst 2015;34:2–186.
[4] Jung B, Yue CP. Trend and outlook of wireless I/Ós for short-range connectivity and beyond. In: IEEE RFIT. p. 33–6.
[5] Liu R et al. A 264-μW 802.15.4a-compliant UWB Transmitter in 22nm FinFET for wireless sensor network application. In: IEEE RFIC Symposium. p. 164–7.
[6] de Streel G. et.al. SleepTalker: A ULV 802.15.4a UWB transmitter SoC in 28-nm FDSOI achieving 14 pJ/b at 27 Mb/s with channel selection based on adaptive FBB and digitally programmable pulse shaping. IEEE J. Solid-State Circuits 2017; 53:4–1163.
[7] Qin B et al. 1.8 pJ/Pulse Programmable Gaussian Pulse Generator for Full-Band Noncarrier Impulse-UWB Transceivers in 90-nm CMOS. IEEE Trans Ind Electron 2010;57:5–1555.
[8] Miyashita D et al. A -70dBm-sensitivity 522Mbps 0.19 nJ/bit-TX 0.43nJ/bit-RX transceiver for TransferJetTM SoC in 65nm CMOS. In: Symposium on VLSI Circuits. p. 74–5.
[9] Abe T, Yuan Y, Ishikuro H, Kuroda T. A 2Gb/s 150mW UWB direct-conversion coherent transceiver with IQ-switching carrier recovery scheme. In: ISSCC. p. 442–3.
[10] Liu D, Geng S, Rhee W, Wang Z. A high efficiency robust UWB receiver design for high data rate CM-range communications. IEEE ISCAS, 2014.
[11] Gimeno C, Flandre D, Bol D. Analysis and specification of an UWB transceiver for high-speed chip-to-chip communication in a server chassis. IEEE Trans Circ Syst I Reg Pap 2018;65:6–2015.
[12] Wyatt K, Jost R. EMC Pocket Guide. Edison, NJ: Scitech Publishing; 2013.
[13] Redfield S et al. Understanding the ultrawideband channel characteristics within a computer chassis. IEEE IEEE Antennas Wireless Propag. Lett 2011:10–191.
[14] Gimeno C et al. Improving noise and linearity of CMOS wideband inductorless balun LNAs for 10-GHz software-defined radios in 28nm FDSOI. IEEE S3S Conference, 2017.
[15] Kim J, Silva-Martinez J. Wideband inductorless balun-LNA employing feedback for low-power low-voltage applications. IEEE Trans Microw Theory Techn 2012;60:9–2833.
[16] de Streel G, Flandre D, Dehollain C, Bol D. Towards ultra-low-voltage wideband noise-cancelling LNAs in 28nm FDSOI. In: IEEE S3S. p. 1–2.
[17] Chen T, Rodriguez S, Akerman J, Rusu A. An inductorless wideband balun-LNA for spin torque oscillator-based field sensing. In: IEEE ICECS. p. 36–9.
[18] Zang H, Sánchez-Sinencio E. Linearization techniques for CMOS low noise amplifiers: A tutorial. IEEE Trans Circ Syst-I: Reg Pap 2011;58:1–22.
[19] Daly D et al. A pulsed UWB receiver SoC for insect motion control. IEEE J Solid-State Circ 2010;45:1–153.
[20] Wu W, Fan X, Wei T, Charlesy CT. A low-voltage low-power self-mixer for 3.1-5GHz non-coherent UWB receiver. IEEE EDSSC, 2009.
[21] Goll B, Zimmermann H. Comparators in nanometer CMOS technology. Springer; 2015.
[22] Xu P, Gimeno C, Bol D. Optimizing TSPC frequency dividers for always-on low-frequency applications in 28nm FDSOI CMOS. IEEE S3S, 2017.
[23] Gimeno C, Flandre D, Bol D. Low-power half-rate dual-loop clock-recovery system in 28-nm FDSOI. IEEE 9th LASCAS, 2018.
[24] "UltraScale Architecture GTY Transceivers", Xilinx User Guide UG578 (v1.3), 2017.
[25] "UltraScale FPGAs Transceivers Wizard", Xilinx LogiCORE IP Product Guide (v1.7), 2018.
[26] Zhu F et al. A low-power low-cost 45-GHz OOK transceiver system in 90-nm CMOS for multi-Gb/s transmission. IEEE Trans Microw Theory Techn 2014;62:9.
[27] Kuo H-C et al. A 60-GHz CMOS sub-harmonic RF receiver with integrated on-chip artificial-magnetic-conductor Yagi antenna and balun bandpass filter for very-short-range gigabit communications. IEEE Trans Microw Theory Techn 2013;61:4.
[28] Chen W-H et al. A 6-Gb/s wireless inter-chip data link using 43-GHz transceivers and bond-wire antennas. IEEE J Solid-State Circ 2009;44:10.
[29] Lee J, Chen Y. A low-power low-cost fully-integrated 60-GHz transceiver system with OOK modulation and on-board antenna assembly. IEEE J Solid-State Circ 2010;45:2–264.
[30] Dolatsha N et al. A compact 130GHz fully packaged point-to-point wireless system with 3D-printed 26dBi lens antenna achieving 12.5Gb/sat 1.55pJ/b/m. In: ISSCC. p. 306–7.
[31] Kim N-S, Rabaey JM. A high data-rate energy-efficient triple-channel UWB-based cognitive radio. IEEE J Solid-State Circ 2016;51:4–809.
[32] Zhou L et al. A 2-Gb/s 130-nm CMOS RF-correlation-based UWB transceiver front-end. IEEE Trans Microw Theory Techn 2011;59:4–1117.
[33] Daneshgar S et al. A 27.8Gb/s 11.5pJ/b 60GHz transceiver in 28nm CMOS with polarization MIMO. In: ISSCC. p. 166–7.
[34] Li W, Duan Y. Rabaey JM, A 200Mb/s inductively coupled wireless transcranial transceiver achieving 5e–11 BER and 1.5pJ/b transmit energy efficiency. ISSCC 2018:290–1.
[35] Moghadami S, Hajilou F, Agrawal P, Ardalan S. A 210 GHz fully-integrated OOK transceiver for short-range wireless chip-to-chip communication in 40 nm CMOS technology. IEEE Trans THz Sci Technol 2015;5:5–737.
[36] Mitono T et al. A 2-Gb/s throughput CMOS transceiver chipset with in-package antenna for 60-GHz short-range wireless communication. IEEE J Solid-State Circ 2012;47:12–3160.
[37] Jang J et al. 4-camera VGA-resolution capsule endoscope with 80 Mb/s body-channel communication transceiver and sub-cm range capsule localization. In: ISSCC. p. 282–3.
[38] Analog Bits, "Case study of half power, multi protocol SERDES in 28 nm FDSOI", online: http://www.soiconsortium.org.
[39] Jaussi J et al. A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE bidirectional serial link in 22nm CMOS. In: ISSCC. p. 440–1.
[40] Lin M-S et al. A 5Gb/s low-power PCI express/USB3.0 ready PHY in 40nm CMOS technology with high-jitter immunity. In: IEEE ASSCC. p. 177–80.
[41] Chen W-C et al. A 2.5-8Gb/s transceiver with 5-Tap DFE and second order CDR against 28-inch channel and 5000 ppm SSC in 40nm CMOS technology. IEEE CICC, 2010.