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# Ultimate Limit in Optoelectronic Performances of Monolayer $WSe_2$ Sloping-Channel Transistors

Zhengdao Xie, Guoli Li, Shengxuan Xia, Chang Liu, Sen Zhang, Zhouxiaosong Zeng, Xingqiang Liu, Denis Flandre, Zhiyong Fan, Lei Liao,* and Xuming Zou*

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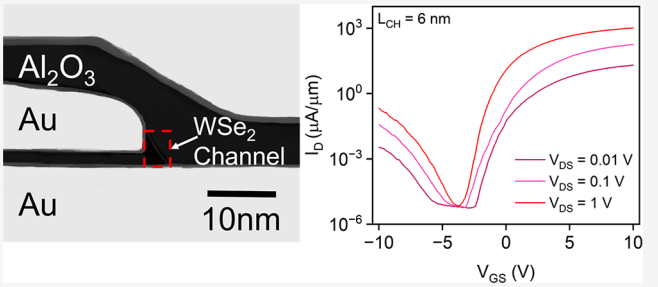
**ABSTRACT:** Atomically thin monolayer two-dimensional (2D) semiconductors with natural immunity to short channel effects are promising candidates for sub-10 nm very large-scale integration technologies. Herein, the ultimate limit in optoelectronic performances of monolayer $WSe_2$ field-effect transistors (FETs) is examined by constructing a sloping channel down to 6 nm. Using a simple scaling method compatible with current micro/nanofabrication technologies, we achieve a record high saturation current up to 1.3 mA/$\mu$m at room temperature, surpassing any reported monolayer 2D semiconductor transistors. Meanwhile, quasi-ballistic transport in $WSe_2$ FETs is first demonstrated; the extracted high saturation velocity of 4.2 × $10^6$ cm/s makes it suitable for extremely sensitive photodetectors. Furthermore, the photoresponse speed can be improved by reducing channel length due to an electric field-assisted detrapping process of photogenerated carriers in localized states. As a result, the sloping-channel device exhibits a faster response, higher detectivity, and additional polarization resolution ability compared to planar micrometer-scale devices.




**KEYWORDS:** *2D materials, sub-10 nm sloping-channel field-effect transistors, ballistic transport, photodetectors*



In the modern semiconductor industry, there has always been a strong demand to integrate more components on a chip, which has driven the critical size of optoelectronic devices down to a few nanometers.[1−4] In order to maintain effective electrostatic control at the nanoscale and thus avoid the influence of short channel effects, conventional Si field-effect transistor (FET) requires its channel thickness to be less than one-third of the channel length.[1,5,6] One issue is that even if the channel thickness is reduced to the nanometer range, the Si surface roughness would be too high to avoid the severe surface scattering that significantly reduces carrier mobility.[1,2,7] Consequently, an effective solution is to look for alternative materials, such as two-dimensional (2D) semiconductor with no dangling bonds on their surfaces.[8−10] In this arena, monolayer $WSe_2$ has been considered a promising candidate for deeply scaled optoelectronic devices in view of its ambipolar property, nonzero bandgap, and high-quality wafer-scale growth.[11−13] Till now, many studies have been performed on $WSe_2$ FETs regarding logic and optoelectronic applications.[14−16] However, the ultimate limit in device optoelectronic performances remains unexplored. The main constraint is the achievement of sub-10 nm channel length ($L_{CH}$) by conventional micro/nanofabrication technologies.[17,18] Recently, graphene or carbon nanotube was used as the gate electrode to reduce the gate length to less than 1 nm, but the drain-source distance is more than 500 nm.[19,20] In this device architecture, large series resistance causes a limited drive current less than 30 $\mu$A/$\mu$m, which conceals the intrinsic optoelectronic characteristics of the devices. Typically, ballistic transport is hardly realized despite its significance in fundamental optoelectronic applications.[21,22]

Herein, we present a simple scaling method to fabricate sub-10 nm sloping-channel $WSe_2$ FETs for very-large-scale device integration. In this method, $L_{CH}$ can be simply defined by the atomic layer deposition (ALD) process, achieving a maximum saturation current ($I_{SAT}$) of 1.0 mA/$\mu$m and an ultrahigh ON/OFF ratio ($I_{ON}/I_{OFF}$) of 1.4 × $10^8$ at $V_{GS}$ = 10 V and $V_{DS}$ = 1 V. The first quasi-ballistic transport analysis of monolayer $WSe_2$ FETs demonstrates a high ballistic efficiency up to 41%. Furthermore, the ultrashort sloping channel enables $WSe_2$ FETs for highly sensitive photodetection. As a result, the device exhibits a shorter response time of 0.4 ms and a higher specific detectivity ($D^*$) of 4.5 × $10^{14}$ Jones compared to planar devices. Interestingly, the sloping channel also enables polarization resolution ability due to optical anisotropy of

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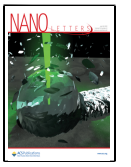





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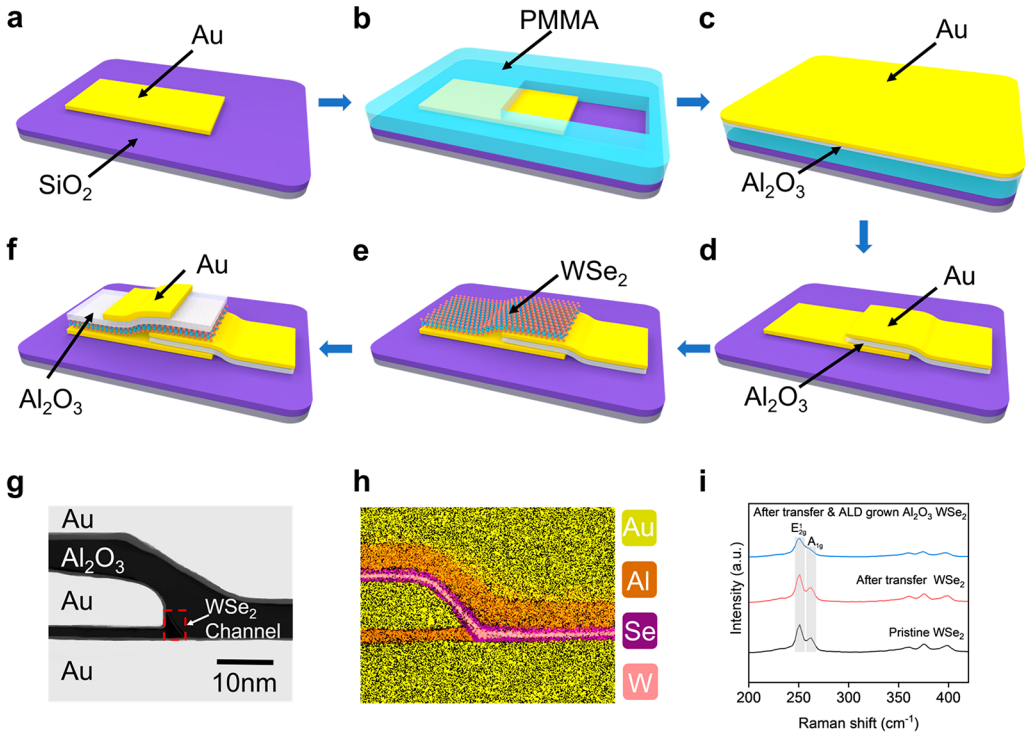


**Figure 1.** Fabrication process and characteristics of the sloping-channel $WSe_2$ FETs. (a–f) Fabrication process flow for sloping-channel $WSe_2$ FETs, with device channel defined by atomic layer deposition of $Al_2O_3$. (g) High-resolution transmission electron microscopy image of a typical $WSe_2$ FET, with the 6 nm channel length. (h) Energy dispersive X-ray spectroscopy element distribution mapping of the distribution of elements within g, which shows the elemental composition of tungsten (W), selenium (Se), aluminum (Al), and Aurum (Au). (i) Raman characterization of pristine monolayer $WSe_2$, after-transfer, and after-transfer and ALD-grown $Al_2O_3$, respectively.

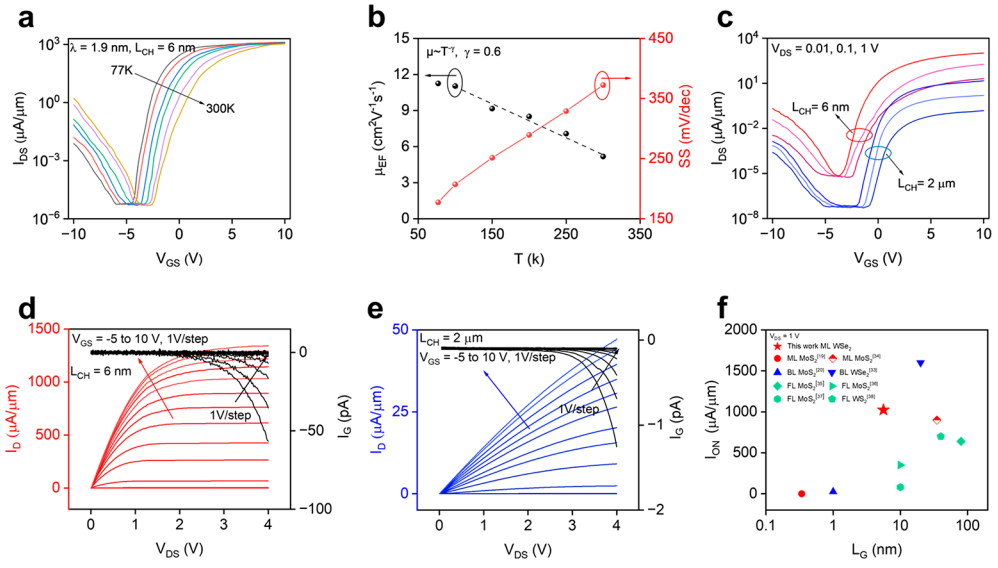


**Figure 2.** Electrical characterizations of the sloping-channel $WSe_2$ FETs. (a) Transfer curves for the $L_{CH}$ = 6 nm $WSe_2$ FETs measured at $V_{DS}$ = 1 V with varying temperature ($T$) down to 77 K. (b) $T$ dependence of the field effect mobility $\mu_{FE}$ and SS. (c) Transfer curves measured at $V_{DS}$ = 0.01, 0.1, and 1.0 V and $T$ = 300 K, for the $L_{CH}$ = 6 nm and $L_{CH}$ = 2 $\mu$m $WSe_2$ FETs, respectively. (d) Output and gate leakage curves measured at $T$ = 300 K and with $V_{GS}$ ranging from −5 to 10 V, for the sloping-channel ($L_{CH}$ = 6 nm) $WSe_2$ FETs. (e) Output and gate leakage curves measured at $T$ = 300 K and with $V_{GS}$ ranging from −5 to 10 V, for the planar ($L_{CH}$ = 2 $\mu$m) $WSe_2$ FETs. (f) The comparison of normalized ON-current ($I_{ON}$) for the varied 2D materials and gate length ($L_G$) at $V_{DS}$ = 1 V. The abbreviations "ML", "BL", and "FL" in the Figure stand for "monolayer", "bilayer", and "few layer", respectively.

$WSe_2$ between in-plane and out-of-plane directions, which is still a challenge for planar devices in view of the in-plane isotropy of $WSe_2$.

The fabrication process of the $WSe_2$ sloping-channel FETs is shown in Figure 1a–f. The preparation processes are described in detail in the Methods section. Briefly, an ∼50 nm-thick Au source electrode was first patterned on $SiO_2$ (300 nm)/$P^+$ Si



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substrate by electron beam lithography (EBL) and metal evaporation (Figure 1a). Second, self-aligned ∼4 nm-thick $Al_2O_3$ and ∼10 nm-thick Au drain electrodes were formed by EBL, ALD, metal evaporation, and subsequent lift-off processes (Figure 1b−d). It should be noted that the Au electrode deposited in this step is used as the support substrate for the monolayer $WSe_2$, and the thickness of the $Al_2O_3$ and Au films is related to the sloping-channel length of the device (Figure 1g). To evaluate the electrical reliability of ∼4 nm-thick $Al_2O_3$, measurement of the leakage current is performed as shown in Figure S1. Third, monolayer $WSe_2$ was transferred to the target substrate (Figure 1e). Low-energy van der Waals contact can introduce a high-quality metal/2D semiconductor interface.[23,24] These fabrication steps were followed by ALD of an ∼10 nm-thick $Al_2O_3$ dielectric and deposition of an ∼20 nm-thick top Au gate electrode (Figure 1f).

A cross-sectional high-resolution transmission electron microscopy image of typical monolayer $WSe_2$ sloping-channel FETs exhibits the self-aligned Au/$Al_2O_3$/Au vertical stack construction and the ultrashort monolayer $WSe_2$ channel of 6 nm (Figure 1g). The $WSe_2$ channel between the two Au source/drain electrodes has a sloping morphology. The energy dispersive X-ray spectroscopy (Figure 1h) confirms the spatial distribution of the corresponding elements in the device architecture. For the monolayer $WSe_2$ transferred to the substrate before and after, the Raman peaks are located at 249.5 and 260 $cm^{-1}$ (Figure 1i), corresponding to the in-plane vibration mode $E^1_{2g}$ and out-of-plane vibration mode $A_{1g}$, respectively.[25,26] However, the $A_{1g}$ of monolayer $WSe_2$ is slightly degraded after ALD-grown $Al_2O_3$, suggesting that this process may introduce little damage or bond disorder into monolayer $WSe_2$. The PL measurements are shown in Figure S2. Correspondingly, the fabrication process of the planar channel ($L_{CH}$ = 2 $\mu$m) $WSe_2$ FETs is shown in Figure S3.

Figure 2a exhibits the transfer characteristics ($I_D$−$V_{GS}$) of our sloping-channel ($L_{CH}$ = 6 nm) $WSe_2$ FETs by varying temperature ($T$) from 300 to 77 K. Here, the $WSe_2$ FET with $Al_2O_3$ capping layer showed n-type dominated ambipolar, which can be attributed to positively fixed charges inside the $Al_2O_3$ layer and the removal of atmospheric adsorbates on the $WSe_2$ surface during annealing.[27,28] Threshold voltage ($V_{TH}$) of the $WSe_2$ FETs increases from 2.2 to 3.0 V, as the transfer curves get positively shifted with the increasing $T$. In the highly ON state, the temperature-independent output current $I_D$ at the same of $|V_{GS} - V_{TH}|$ indicates tunneling dominance and ohmic-like contact at the metal/$WSe_2$ interface of the FETs (Figure 2a). In the OFF state, $I_D$ remains constant and low, which results in a high $I_{ON}/I_{OFF}$ ratio (∼1.4 × $10^8$). Here, $L_{CH}$ is about 3 times larger than characteristic length[18] ($\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}}$ = 1.9 nm, where $\varepsilon_{ox}$, $\varepsilon_s$, $t_{ox}$, and $t_s$ are $Al_2O_3$ dielectric constant, $WSe_2$ dielectric constant, $Al_2O_3$ thickness, and $WSe_2$ thickness, respectively), ensuring the effective electric gating. With the decreasing temperature, the subthreshold swing $\left(SS = \ln 10\left(\frac{dV_{GS}}{d(\ln I_{DS})}\right)\right)$ gets improved from 372 mV/dec to 177 mV/dec, following the Arrhenius relationship between $T$ and SS in Figure 2b. Moreover, in the range of 100−300 K, the intrinsic field-effect mobility ($\mu_{EF}$) can be calculated by the equation

$$\mu_{EF} = \frac{dI_{DS}}{dV_{GS}} \frac{L_{CH}}{W} \frac{1}{V_{DS}} \frac{R_{total}}{R_{total} - R_C} \frac{1}{C_g} \quad (1)$$

where the channel width ($W$) is normalized to be 1 $\mu$m, $C_g$ is the gate capacitance, $R_{total}$ is the total resistance, including channel resistance and contact resistance $R_C$. As illustrated in Figure S4, we have extracted the device contact resistance, based on the nonlinear characteristics of output conductance $G(dI_{DS}/dV_{GS})$ versus $V_{DS}$ at the low-biased condition.[29] The $\mu_{EF}$ has been extracted and fits well with the expression $\mu_{FE} \sim T^{-\gamma}$ in Figure 2b, indicating dominance of phonon scattering in our device.[30] Figure 2c shows the transfer characteristics of the sloping-channel ($L_{CH}$ = 6 nm) and planar ($L_{CH}$ = 2 $\mu$m) $WSe_2$ FETs. Transfer curves of the $L_{CH}$ = 17 and 40 nm $WSe_2$ FETs are plotted in Figure S5a, b, respectively. Here, the $I_{ON}/I_{OFF}$ extracted at $L_{CH}$ = 6 nm is similar to that of the 2 $\mu$m planar-channel FET, demonstrating the ability of the 6 nm sloping-channel FET to turn off the device. At $V_{DS}$ = 1 V, the OFF-current is lower than 5 pA/$\mu$m, which satisfies the low-operating-power 2024 requirement (100 pA/$\mu$m) of the International Technology Roadmap for Semiconductors (ITRS).[31]

Output characteristics ($I_D$−$V_{DS}$) and gate leakage current curves of the sloping-channel ($L_{CH}$ = 6 nm) and planar ($L_{CH}$ = 2 $\mu$m) $WSe_2$ FETs are illustrated in Figure 2d, e. For the $L_{CH}$ = 17 and 40 nm $WSe_2$ FETs, their output and gate leakage current curves are presented in Figure S5c, d. The maximum $I_{SAT}$ increases from 47 $\mu$A/$\mu$m at $L_{CH}$ = 2 $\mu$m to 1339 $\mu$A/$\mu$m at $L_{CH}$ = 6 nm. This result exceeds the critical current density target (1.0 mA/$\mu$m) proposed for 2D FETs in a recent perspective article.[32] We have summarized the normalized ON-current at $V_{DS}$ = 1 V for the varied 2D semiconductors and gate length, as depicted in Figure 2f.[19,20,33−38] It is worthy pointing out that the bilayer $WSe_2$ transistor can achieve a higher ON-current of 1.7 mA/$\mu$m,[33] but at the cost of reducing the $I_{ON}/I_{OFF}$ value to less than $10^3$. As the channel length increases from 20 to 230 nm, the $I_{ON}/I_{OFF}$ increases from 680 to $10^8$, but the $I_{ON}$ decreases from 1.7 mA/$\mu$m to 0.2 mA/$\mu$m.[39] The achievement of ultrahigh drive current and ultralow leakage current in our sloping-channel device demonstrates its potential to realize the trade-off between high-performance and low-power electronics.

While scaling the $WSe_2$ FETs from the planar, long channel ($L_{CH}$ = 2 $\mu$m) to the sloping channel ($L_{CH}$ = 6 nm), the diffusive transport model has failed to reproduce the device characteristics. We adopt the virtual source emission-diffusion (VSED) model, which was derived from Landauer scattering theory, to describe the drift-diffusive to ballistic transport regimes. The current $I_D$ is expressed as[40]

$$I_D = WQ_n(0)v_T F_{satVSED} \quad (2)$$

$$F_{sat,VSED} = \left(\frac{T_r}{2 - T_r}\right)\left(\frac{1 - \exp\left(-\frac{V_{DSI}}{\Phi_t}\right)}{1 + \frac{T_r}{2 - T_r}\exp\left(-\frac{V_{DSI}}{\Phi_t}\right)}\right) \quad (3)$$

where $v_T$ is the thermal/ballistic injection velocity, $Q_n(0)$ is charge at the virtual source point, and $\Phi_t$ is the thermal voltage. The function $F_{sat,VSED}$ can give transmission coefficient (Tr) while scaling $L_{CH}$ from carrier drift-diffusive to ballistic transport regimes:[41]


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$$\mathrm{Tr} = \frac{\lambda_{\mathrm{mfp}}}{\lambda_{\mathrm{mfp}} + l} \tag{4}$$

where $l$ is critical length for scattering at top of the barrier, $\lambda_{\mathrm{mfp}}$ $\left( = 2\frac{\Phi_t}{\upsilon_T}\mu_{\mathrm{FE}} \right)$ is carrier mean free path. Using the $\mu_{\mathrm{FE}}$ extracted in Figure 2b and $\upsilon_T$ $(=\sqrt{\frac{2k_BT}{\pi m^*}} \approx 8.4 \times 10^6$ cm/s, here $k_B$ is the Boltzmann constant, $m^* = 0.39m_0$ is the effective transport mass of carriers in monolayer $WSe_2$[42]), $\lambda_{\mathrm{mfp}}$ is calculated to be 1.9 nm for our monolayer $WSe_2$. For the long channel ($L_{CH} > \lambda_{\mathrm{mfp}}$), the drift-diffusion dominants in the carrier transport, whereas that are more ballistic for the short-channel devices in Figure 3a inset. Based on the eqs 2 and 3, we extract the Tr for

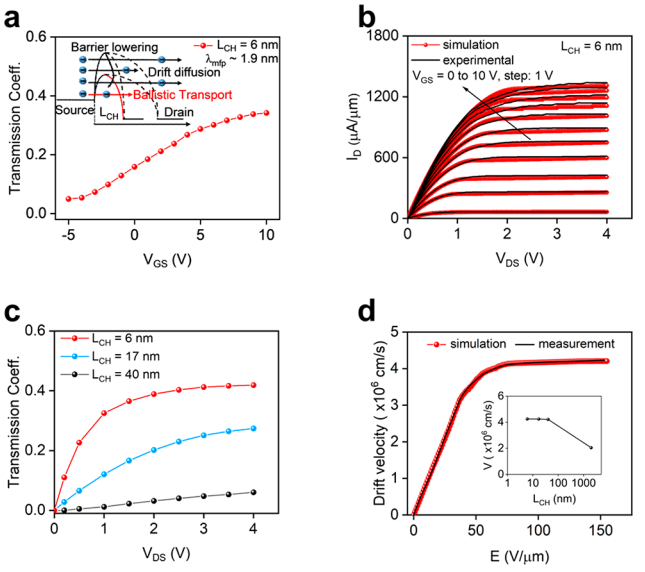


**Figure 3.** The simulation of the sloping-channel $WSe_2$ FETs. (a) Transmission coefficient Tr vs $V_{GS}$ for a $L_{CH}$ = 6 nm $WSe_2$ FET, while adopting the *VSED* model (extracted at $V_{DS}$ = 1 V). Inset: carrier drift-diffusive and ballistic transport regimes inside the short- and long-channel $WSe_2$ FETs, regarding carrier mean free path $\lambda_{mfp}$ (~1.9 nm) of the monolayer $WSe_2$. (b) The measured and simulated output curves for the $L_{CH}$ = 6 nm $WSe_2$ FETs. (c) Tr vs $V_{DS}$ (extracted from VSED model at $V_{GS}$ = 10 V), for the sloping-channel $WSe_2$ FETs with $L_{CH}$ = 6, 17, and 40 nm, respectively. The critical length $l$ decreases with the increasing $V_{DS}$, leading to Tr reaching up to 41% at $L_{CH}$ = 6 nm. (d) Drift velocity $\upsilon_d$ vs electric field $E$ for the $L_{CH}$ = 6 nm $WSe_2$ FETs, considering numerical extraction from the experimental data (black) and analytical simulation based on the Caughey-Thomas model (red). Inset: $\upsilon_{sat}$ of the devices with different channel lengths.

the $L_{CH}$ = 6, 17, and 40 nm FETs in Figure 3a, c. Output curves for the FETs are simulated in Figure 3b, Figure S6a, b, respectively. In Figure 3a, Tr ≈ 0.16 is obtained at $V_{GS}$ = 0 V, indicating the onset of the quasi-ballistic transport inside the 6 nm FET. In Figure 3c, it is seen that Tr increases with $V_{DS}$, due to the enhanced $V_{GSI}$ and $V_{DSI}$ and decreased $l$. This is mainly attributed to the fact that $R_C$ can reduce $V_{DSI}$ and $V_{GSI}$ voltages, thereafter leading to the increase of $l$ and decrease of $Q_n(0)$, Tr, and $I_D$ in the sloping-channel FETs. In Figure S4, $R_C$ decreases with applied voltages $V_{DS}$ and $V_{GS}$. Finally, at $V_{DS}$ = 4 V, Tr reaches up to 41% in the $L_{CH}$ = 6 nm $WSe_2$ FET, indicating quasiballistic transport behavior. Furthermore, the drift velocity $\upsilon_d$ (black line in Figure 3d) can be estimated by the equation[43,44]

$$\upsilon_d = \frac{I_D}{WC_g|V_{GSI} - V_{TH} - V_{DSI}/2|} \tag{5}$$

Here, the $\upsilon_d$ fits with the analytical calculation based on Caughey-Thomas model (the red line in Figure 3d), as below:

$$\upsilon_d = \frac{\mu_{EF}E}{\left[1 + \left(\frac{\mu_{EF}E}{\upsilon_{SAT}}\right)^{\gamma}\right]^{1/\gamma}} \tag{6}$$

where $E$ $(= (V_{DS} - 2I_{DS}R_C)/L_{CH})$ is the lateral electric field, $\upsilon_{SAT}$ is the saturation velocity, and $\gamma$ is the scattering factor in Figure 2b. At high electric field, $\upsilon_d = \upsilon_{SAT} = 4.2 \times 10^6$ cm/s, which is higher than previously reported.[42]

Besides FET applications, the ultrashort transit time of transporting carriers in the sloping channel enables a $WSe_2$ device for polarization-sensitive photodetector with improved sensitivity and response speed. Figure 4a gives transfer curves of the 6 nm device with and without illumination (incident light power intensity, $P_{light}$ = 2 W/cm$^2$). As exhibited in Figure S7, the transfer characteristic trace shifts to the positive direction after illumination and the off-state current increases, suggesting both photogating and photoconductive effect in the $WSe_2$ photodetector.[45] The device exhibits a large $I_{light}/I_{dark}$ ratio of $2.8 \times 10^4$ at $V_{GS}$ = −3 V and $V_{DS}$ = −1 V. Here, $I_{light}$ and $I_{dark}$ denote output current with and without illumination, respectively. Upon illumination, the hole current increases whereas the electron current decreases. It can be assumed that the photogenerated electrons are effectively trapped in localized states and act as a local gate, which increases the hole concentration in the $WSe_2$ channel. Figure 4b shows the dynamic response of the device. The $I_{light}$ increases with laser power, while $I_{dark}$ is always kept at a very low level. To quantitatively evaluate the photoresponse capability of the device, photoresponsivity ($R$) is calculated according to the equation:[46]

$$R = \frac{I_{light} - I_{dark}}{P_{light}S} = \frac{I_{ph}}{P_{light}S} \tag{7}$$

where $I_{ph}$ is the photocurrent and $S$ is the active area of $WSe_2$ photodetector. The spatial photocurrent mapping is used to characterize the effective area of the device, as shown in Figure S8. The maximum responsivity of the photodetector is then extracted to be 1027 A/W (Figure S9). The responsivity decreases as the $P_{light}$ value increases, probably caused by enhanced photogenerated carrier recombination upon an increase in light intensity. Next, in order to evaluate the identification ability of the device upon a weak signal, we further extract specific detectivity ($D^*$) according to the equation:[46]

$$D^* = \frac{(SB)^{1/2}}{\mathrm{NEP}} \tag{8}$$

$$\mathrm{NEP} = \frac{\overline{i}_n^{2^{1/2}}}{R} \tag{9}$$

where $B$, NEP, and $\overline{i_n^2}$ represent the bandwidth, noise equivalent power, and root-mean-square value of the noise current, respectively. In the Figure 4b inset, the noise level per unit bandwidth (1 Hz) is measured to be $2.9 \times 10^{-16}$ A$^2$ Hz$^{-1}$ at $V_{GS}$ = −3 V. Here, based on the maximum $R$ value of 1027 A/W, $D^*$ is calculated to be $4.5 \times 10^{14}$ Jones for the 6 nm


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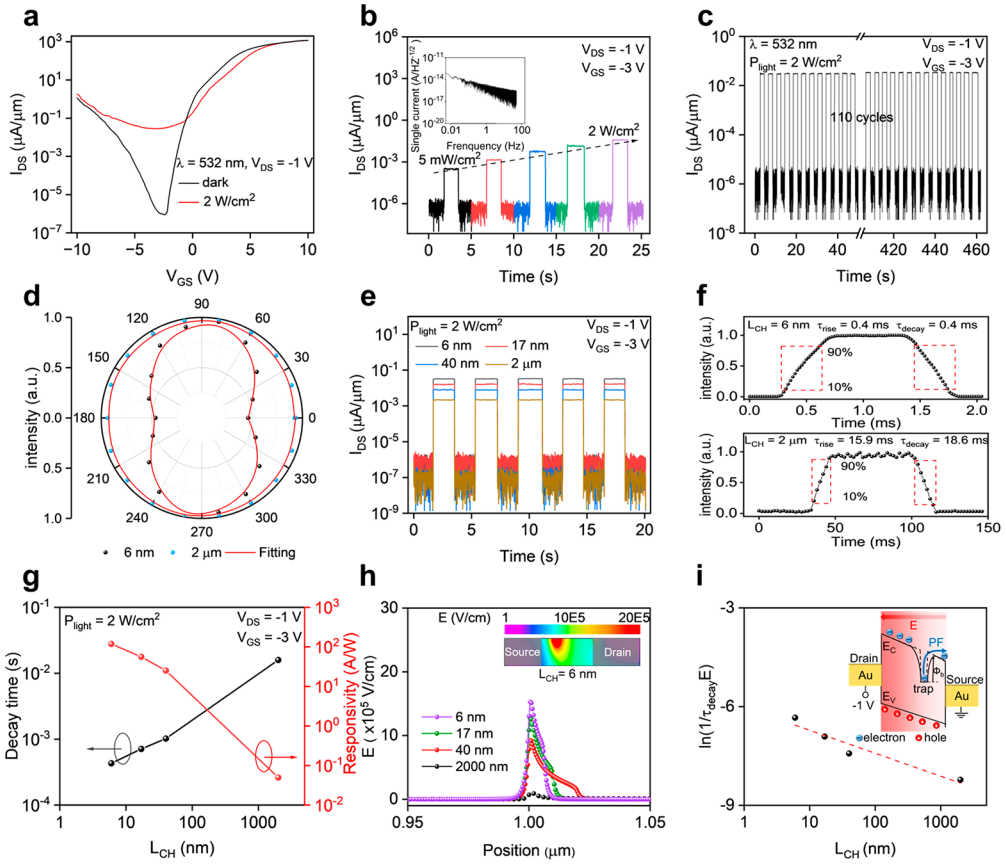


**Figure 4.** $WSe_2$ photodetector based on sloping channel. (a) Transfer curves at $V_{DS} = -1$ V for the $L_{CH} = 6$ nm $WSe_2$ photodetectors under dark (black) and illumination (red) conditions. (b) Dynamic response of the $L_{CH} = 6$ nm $WSe_2$ photodetector with increasing $P_{light}$ value. Inset: Noise analysis of the device. (c) Photoswitching response of the $L_{CH} = 6$ nm $WSe_2$ photodetectors under 532 nm laser illumination and $P_{light} = 2$ W/cm$^2$. (d) The extracted photocurrent as a function of polarization angle for the sloping $L_{CH} = 6$ nm (black dot) and planar $L_{CH} = 2$ $\mu$m (azure dot) $WSe_2$ photodetectors. (e) Photoswitching response of the $L_{CH} = 6$, 17, 40 nm and 2 $\mu$m $WSe_2$ photodetectors, under 532 nm laser illumination. (f) The $\tau_{rise}$ and $\tau_{decay}$ of the $L_{CH} = 6$ nm (above), 2 $\mu$m (below) $WSe_2$ photodetectors. (g) Photoresponsivity (red, right axis) and decay time (black, left axis) of the $WSe_2$ photodetectors, with $L_{CH}$ varying from 6 nm to 2 $\mu$m. (h) The extracted $E$ inside the $L_{CH} = 6$, 17, 40, and 2000 nm FETs, close to the source electrode (at $V_{DS} = 1$ V). Inset: Simulated electric field contour plot for of the 6 nm $WSe_2$ FETs. (i) The Frenkel-Poole (FP) plot of $\ln(1/\tau_{decay}E)$ vs $L_{CH}$. Inset: FP emission at a high electric field. $E_C$ is the minimum conduction band energy, $E_v$ is the maximum valence band energy, and $\Phi_b$ is the FP trap energy of the electron.

device (Figure S9). To the best of our knowledge, this is the highest value reported so far for $WSe_2$ photodetectors.[16,47−50] Figure 4c exhibits transient photoresponse of the device measured, in which 110 periodical on/off laser cycles are performed. Interestingly, utilizing optical anisotropy of $WSe_2$ between in-plane and out-of-plane directions, the ultrashort sloping-channel device is capable of sensing incident light polarization. The polarized photocurrent upon 532 nm laser illumination is presented in Figure S10b. The photocurrent as illuminated perpendicular to the $X$-axis (defined as 90° see Figure S10a) is much stronger than that along $X$-axis (defined as 0°). Thus, a linear dichroic ratio of 2.3 is achieved (Figure 4d), which is still a challenge for planar $WSe_2$ devices. This polarization dependent optical property mainly results from the anisotropy of $WSe_2$ between in-plane and out-of-plane directions instead of the plasmonic response of the Au structures (see Figure S11 for more details).

The influence of the channel length on the transient properties is investigated. Figure 4e shows the influence of $L_{CH}$ on the photocurrent of the devices with the same test conditions of $V_{DS} = -1$ V and $V_{GS} = V_{OFF}$ (at which the device is turned off completely). Here, the responsivity increases with the decrease of channel length and can be improved by 3 orders of magnitude in Figure 4g. In addition, the rise/decay time decreases from 15.9/18.6 ms for the 2 $\mu$m device to 0.4/0.4 ms for the 6 nm device (Figure 4f, Figure S12). Compared with other photodetectors, as shown in the Supporting Information (Table 1), our device demonstrates its potential to realize the trade-off between responsivity and response speed. The detailed decay processes of the devices with various channel lengths are shown in Figure 4g. By shortening the channel length, the responsivity and response speed can be improved simultaneously. In the traditional 2D phototransistor architecture, photogating effect is responsible for the channel current modulation upon light illumination.[43,51] As one type photogenerated carriers are trapped by surface and interface traps existing in nanomaterials, another type carriers would transport in the conducting channel, resulting in a photogain ($G$) given by[52]

$$G = \frac{\tau_{lifetime}}{\tau_t} \tag{10}$$

where $\tau_{lifetime}$ is the lifetime of the trapped photocarriers and is at the same order of the photoresponse time. Here, $\tau_t$ can be estimated by the equation:


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$$\tau_t = \frac{L_{CH}^2}{\mu_{FE} V_{DSI}} \tag{11}$$

For $L_{CH}$ = 6 nm, 17 nm, 40 nm and 2 $\mu$m, $\tau_t$ = 1.6, 6.2, and 19 ps and 260 ns, respectively. According to eq 10, the $G$ of $WSe_2$ devices is calculated to be $1.8 \times 10^8$, $1.1 \times 10^8$, $5.3 \times 10^7$, and $6.1 \times 10^4$ for $L_{CH}$ = 6, 17, 40, and 2 $\mu$m, respectively. Accordingly, it is reasonable to obtain a higher responsivity in devices with shorter channels in Figure 4g. Regarding the response speed, both $\tau_{rise}$ and $\tau_{decay}$ are limited by the lifetime of the captured electrons in the localized states. It is known that the current across Schottky barrier between metal electrode and semiconductor channel is determined by the barrier height ($\psi_B$) and expressed as[52]

$$I_D = A^* T^2 \exp(-q\psi_B/k_B T)(\exp(qV/k_B T) - 1) \tag{12}$$

where $A^*$ represents the effective Richardson constant, $q$ represents the electron charge, and $V$ represents the bias voltage applied on the junction. Under illumination, the carriers trapped in surface/interface traps act as a local gate, which would reduce the barrier height $\psi_B$ and increase the output current. These trapped carriers usually have relatively long lifetime. This is the reason that photodetectors based on 2D semiconductors, normally exhibit long response time.[50,53,54] For the shorter channel length $WSe_2$ device, the potential drop on the metal/semiconductor contact is higher due to the reduced channel resistance. Consequently, a higher electric field near the source electrode is introduced, which can reduce the lifetime of trapped carriers due to an electric field-assisted detrapping process, named Frenkel-Poole (FP) emission in the Figure 4i inset. To get a more intuitive understanding of the response mechanism, we perform 2D device simulation with SILVACO/Atlas in Figure 4h, where the local electric field near the source electrode for different $L_{CH}$ values is extracted. The Figure 4h inset shows the electric field distribution of $L_{CH}$ = 6 nm $WSe_2$ FETs. The numerical simulation is described in the Methods section. The relationship between FP current density ($J_{FP}$) and $E$ can be expressed as[52]

$$J_{FP} = AE\exp\left(-\frac{q(\Phi_b - \sqrt{qE/\pi\varepsilon_0\varepsilon_{ox}})}{k_B T}\right) \tag{13}$$

where $A$ represents the pre-exponential factor and $\Phi_b$ represents the FP trap energy (i.e., the energy level of the trap with respect to the conduction energy level of the $WSe_2$, as shown in Figure 4i inset). By assuming $J_{FP}$ is inversely proportional to $\tau_{decay}$, eq 13 can be converted to

$$\ln\left(\frac{1}{\tau_{decay}}\right) = N\sqrt{E} + O \tag{14}$$

where $N$ and $O$ are constants. Figure 4i shows $\ln(1/\tau_{decay}E)$ versus $L_{CH}$, and the linear relationship confirms the FP emission model in modeling the detrapping process.

In summary, we present a novel method to construct monolayer $WSe_2$ sloping-channel FETs with a record high $I_{SAT}$ of 1339 $\mu$A/$\mu$m and a large $I_{ON}/I_{OFF}$ of $1.4 \times 10^8$. The quasi-ballistic transport in $WSe_2$ FETs is first demonstrated, exhibiting a high ballistic efficiency of 41%. Furthermore, the sloping-channel device is suitable for building polarization-sensitive photodetector with improved response speed and detectivity. The method is applicable to other 2D semiconductors, thus broadening both experimental and theoretical research fields of 2D optoelectronic devices.

## METHODS

**Device Fabrication.** The Au electrodes were defined by standard electron beam lithography (JEOL 7610 with NPGS), metal evaporation, and lift-off process. Monolayer $WSe_2$ flake was obtained by mechanical exfoliation from a bulk crystal, and then transferred onto the source and drain electrodes by dry transfer.[55] Standard ALD (precursor: water as oxidant and trimethylaluminum as Al source; deposition temperature = 100 °C; the growth rate of 1 Å/cycle.) was used to deposit $Al_2O_3$ thin film.[56] The Au electrodes were deposited by metal evaporation process under vacuum conditions ($\approx 5 \times 10^{-4}$ Pa).

*Material and Device Characterizations.* Raman spectra were obtained by using a confocal Raman system (Horiba LabRAM HR). The high-angle annular dark-field STEM images and element mapping analyses were recorded with a Thermo Scientific Themis Z (3.2) microscope equipped with a probe-forming aberration corrector at an operating voltage of 300 kV (Analytical Instrumentation Center of Hunan University). Optoelectronic characterizations of the devices were carried out with the Lake Shore TTPX Probe Station under vacuum condition ($\approx 1.5 \times 10^{-4}$ Pa).

*Numerical Simulation.* The 2D device simulation in Figure 4h was performed in SILVACO/Atlas to check electrical field ($E$) distribution inside the varied channel lengths of 6, 17, 40, and 2000 nm, with a band gap of 1.43 eV, an affinity of 3.83 eV, and a metal work function of 5.1 eV (referred to Au). At $V_{DS}$ = 1.0 V, the local electric field near the source electrode for different $L_{CH}$ is extracted.

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.3c01866.

Characterization and leakage current of $Al_2O_3$ layer; PL characterization; fabrication process of the planar channel ($L_{CH}$ = 2 $\mu$m) $WSe_2$ FETs; contact resistance calculation by $G$-function method; electrical characterizations of the sloping-channel $WSe_2$ FETs; the simulation of the sloping-channel $WSe_2$ FETs; $WSe_2$ photodetector performance; spatial photocurrent image; optoelectronic characteristics of $L_{CH}$ = 6 nm monolayer $WSe_2$ photodetector; $WSe_2$ photodetector for optical polarization measurement; plasmon response with different polarization of the device; time-resolved photoresponse of $WSe_2$ photodetectors (PDF)

## AUTHOR INFORMATION

### Corresponding Authors

**Lei Liao** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics and State Key Laboratory for Chemo/Biosensing and Chemometrics, College of Semiconductors (Integrated Circuits), Hunan University, Changsha 410082, China; School of Physics and Electronic Engineering, Harbin Normal University, Harbin 150025,*



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*China*; orcid.org/0000-0003-1325-2410; Email: liaolei@whu.edn.cn

**Xuming Zou** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*; Email: zouxuming@hnu.edu.cn

### Authors

**Zhengdao Xie** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*

**Guoli Li** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*

**Shengxuan Xia** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*; orcid.org/0000-0002-3158-6257

**Chang Liu** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*

**Sen Zhang** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*

**Zhouxiaosong Zeng** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*

**Xingqiang Liu** − *Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, China*; orcid.org/0000-0002-3598-8755

**Denis Flandre** − *Institute of Information and Communication Technologies, Electronics and Applied Mathematics, UCLouvain, Louvain-la-Neuve B-1348, Belgium*

**Zhiyong Fan** − *Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong SAR 999077, China*; orcid.org/0000-0002-5397-0129

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.3c01866

### Author Contributions

X.Z. and L.L. conceived the concept and experiments. Z.X., G.L., and X.Z. prepared the manuscript. Z.X., C.L., and S.Z. fabricated and characterized the devices. Z.X., Z.Z., X.L., and Z.F. assisted experiments on device fabrication and measurements. Theoretical calculation was finished by G.L., S.X., and D.F. All authors examined and commented on the manuscript.

### Notes

The authors declare no competing financial interest.

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