Impact of High Temperature Up to 175 °C on the DC and RF Performances of 22-nm FD-SOI MOSFETs

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***Abstract*— In this work, the effect of rise in temperature from 25 °C to 175 °C on the performance of 22-nm fully depleted silicon-on-insulator (FD-SOI) MOSFETs is studied under different bias conditions. The devices are measured in dc and RF to observe the zero-temperature coefficient (ZTC) point and extract the prominent RF figures of merit (FoMs), i.e., current-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). The evolution of transconductance (g_m) with temperature appears to be one of the major causes of the 20% degradation in peak f_T and f_{max} at 175 °C. From a low-power application point of view, stepping down V_d from 0.8 to 0.6 V decreases the magnitude of peak f_T and f_{max} degradation to around 7%–10%, respectively, over the given temperature range while reducing static power consumption (P_{dc}) around 29%. Furthermore, the variation of f_T and f_{max} at and below the g_m-ZTC is investigated. Below the g_m-ZTC point, at a front-gate bias V_g of 0.3 V, an improvement in f_T of around 20% and an almost steady f_{max} are observed.**

***Index Terms*— Figures of merit (FoMs), f_{max}, f_T, fully depleted silicon-on-insulator (FD-SOI), high temperature, zero-temperature coefficient (ZTC) point.**

I. Introduction

THE exposure of electronic circuitry to high-temperature environment compels the need of investigating the impact elevated temperatures have on them. In the past, circuits were typically only subjected to high-temperature conditions in some niche applications, such as drilling and geothermal energy. Apart from these applications which have regained interest recently given the current energy crisis, certain currently used applications also encounter elevated temperatures. For example, automotive electronics, one of the most rapidly growing electronics sectors, faces increased temperatures, which could easily vary from 150 °C to 250 °C for on-wheel sensing, 150 °C–200 °C around on engine, 200 °C–300 °C for cylinder pressure, and can go up to as high as 850 °C for exhaust sensing, respectively [1]. This highlights the need to investigate the performance of devices at high temperature and predict the impact harsh environments could have on these advanced devices compared to room-temperature operation.

The 22-nm fully depleted silicon-on-insulator (FD-SOI) technology from GlobalFoundries is a prominent technology that is suited for a broad range of applications, such as the Internet-of-Things (IoT), wearables, automotive, millimeter-wave (mm-wave) radar, and 5G communications. The reported intrinsic values of two main RF figures of merit (FoMs), namely, the current gain cutoff frequency f_T and maximum oscillation frequency f_{max}, are as high as around 347 and 371 GHz [2], respectively. This showcases the capabilities of this technology with respect to RF and mm-wave design. Furthermore, this technology serves low-power applications, which is of growing importance owing to the widespread expansion of the IoT. Specific applications where low-power RF applications like ultralow-power (ULP) radios and RF front-ends are of interest are those of Bluetooth low-energy receiver front-ends [3], [4]. A proposed ultralow-voltage (ULV) RF front-end is shown in [3]. In [5], the use of forward body biasing on 22-nm FD-SOI MOSFETs has been introduced to design LNAs under low supply voltage and dc power. In particular, automotive IoT deploys low-power technology that requires operation under harsh environments [6]. These aforementioned works clearly underline the growing importance of low-power RF applications in the current electronics market. 22FDX[1] technology provides the perfect platform for this study as it targets applications like automotive electronics, which potentially face high temperatures along with in demand state-of-the-art low-power electronics applications.

There is a dearth of work on the performance of 22-nm FD-SOI MOSFETs at high temperature in literature. In [7], the RF performance of MOSFETs in older technology nodes (namely partially depleted SOI devices and bulk devices) was investigated with varying temperatures. To the best of our knowledge, just [8] studied the performance of FETs

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in 22FDX[1] technology, although the main goal of the work was the high-frequency performance of these devices rather than high temperature with limited discussion on data versus temperature. Our target is to add to the existing literature by investigating the high-temperature performance of 22-nm FD-SOI MOSFETs.

This article presents the effect of increased temperature on the RF and mm-wave performance metrics of 22-nm FD-SOI MOSFETs using on-wafer measurements under different drain (V_d) and gate (V_g) bias conditions. With an eye on low-power applications, studies are additionally made in this work at a lower drain voltage V_d of 0.6 V compared to the nominal value of 0.8 V. To go beyond our conclusions presented in [9], we study in detail the small-signal equivalent circuit (SSEC) parameters and compare f_T and $f_{\max}$ coming from the computation from SSEC parameters. New repeatable measurements over multiple dies are performed to confirm the results discussed here. The variation of the RF FoMs and SSEC parameters of MOSFETs on 22-nm FD-SOI technology going up to 175 °C is demonstrated for the first time to the best of our knowledge, while the process design kit (PDK) models are limited to a maximum temperature value of 125 °C. Apart from studying the impact of temperature on peak f_T and $f_{\max}$, the significance of the g_m zero temperature coefficient (ZTC) point is stressed on. RF FoMs are extracted at three different gate bias conditions (V_g) corresponding to the maximum g_m to the g_m-ZTC and below the g_m-ZTC.

II. Experimental Details

In this work, 22-nm FD-SOI n-MOSFETs (22FDX[1]) from GlobalFoundries are studied [2]. The device details are as follows: the gate length is 20 nm, and total width is 60 μm for each of these devices composed of 120 fingers (20 fingers with a multiplicity of 6) of 0.5-μm finger width.

For the RF characterization, S-parameters are measured in a frequency range from 200 MHz up to 40 GHz. The measurements are made on an MPI TS3000-SE probe station. This probe station offers a compact and more closed system to perform temperature measurement in a more accurate manner. A PNA-X vector network analyzer and two ground–signal–ground RF |Z| probes of 100-μm pitch are used for these measurements. The probes are compatible for high-temperature measurements up to the necessary temperature value of 175 °C. Load-reflect-reflect-match (LRRM) method is used for calibration at each temperature point separately. While the devices are placed on the primary chuck of the probe station that is heated up, the calibration kit is placed on an auxiliary chuck beside the primary chuck. It is important for the calibration procedure to take into account the variation of temperature on the standard values themselves. It is therefore verified that the resistance of the load standard is very steady with temperature and a variation of just 0.3% is seen, which is comparable with the variation of one load standard to another. For each device, dedicated open and short structures are measured and used for de-embedding. The measurements are carried out at four temperature points: 25 °C, 75 °C, 125 °C, and 175 °C. While the primary chuck on the MPI probe station can be heated up to 300 °C with accurate and stable temperature control, the limit of safe temperature range of operation was the reason of limiting the highest temperature value to 175 °C. In order to have a steady temperature value while measuring, the whole system was let to steady for at least half an hour at each set temperature. The back gate of FD-SOI was grounded for all the experiments ($V_{\text{bg}} = 0$ V).

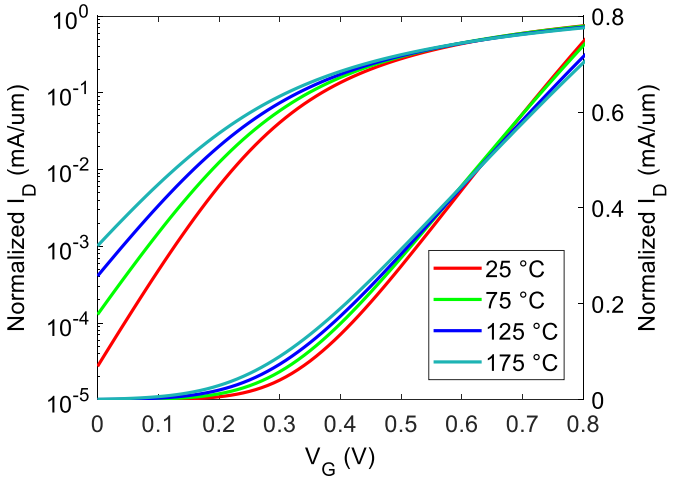

Fig. 1. Normalized drain current I_d in log and linear scale versus gate voltage V_g at $V_d = 0.8$ V at different temperatures.

III. Results and Discussion

The I_d–V_g characteristic of the device is shown in Fig. 1 in saturation at $V_d = 0.8$ V for temperatures varying from 25 °C to 175 °C. One of the primary observations is that of the ZTC point for drain current I_d-ZTC, this is the V_g bias corresponding to which I_d is constant with temperature, is observed at around 0.62 V (at $V_d = 0.8$ V). Due to threshold voltage reduction with temperature, I_d increases with temperature at V_g below I_d-ZTC, whereas I_d decreases with temperature at V_g above I_d-ZTC due to reduced carrier mobility. At the ZTC, these two mechanisms balance each other resulting in a temperature invariant I_d [10], [11].

In [9], a threshold voltage V_{Th} reduction with increasing temperature of 0.6 mV/°C has been demonstrated using the second-derivative method from [12] in the linear regime. The variation of threshold voltage with temperature has been widely reported in literature across different advanced technologies [13], [14], [15].

Fig. 2 represents the MOSFET SSEC used in this study. The circuit consists of both an intrinsic and an extrinsic part, where the extrinsic part includes the parasitic series resistances and parasitic shunt capacitances. In order to extract the various SSEC elements, the measured S-parameters are converted into Y- and Z-parameters. The conductances and capacitances are obtained from the real and imaginary part of Y-parameters, respectively, whereas the resistances from the real part of Z-parameters. The extraction procedure of SSEC elements is described in [16]. Extrinsic transconductance $g_{m,e}$ and extrinsic output conductance $g_{d,e}$ are obtained at low frequency from the real part of Y_{dg} and Y_{dd}, respectively, and include the contributions of the parasitic resistances. The other extrinsic parameters refer to the parasitic elements, while

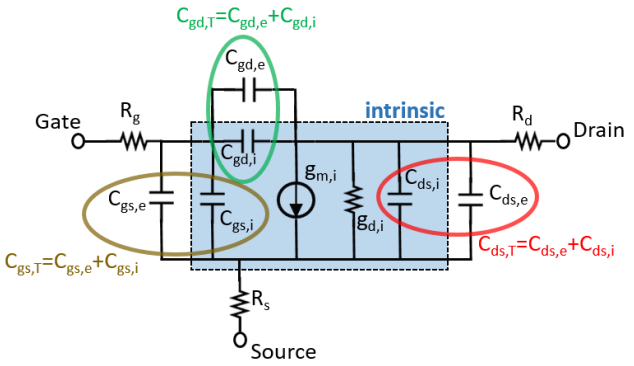

Fig. 2. SSEC for MOSFET [17].

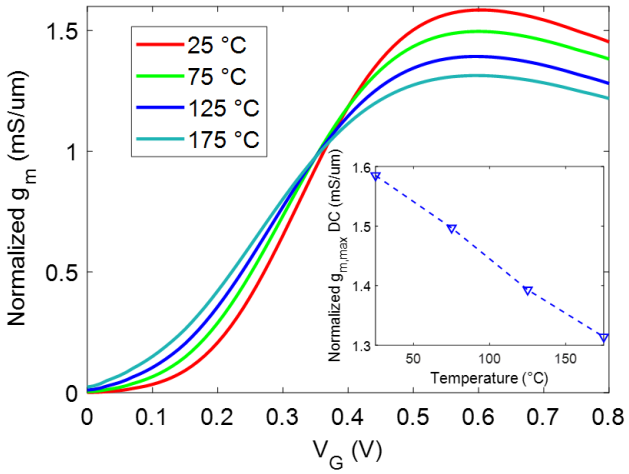

Fig. 3. Variation of g_m and maximum normalized transconductance $g_{m,\max}$ from dc measurements at $V_d = 0.8$ V with temperature.

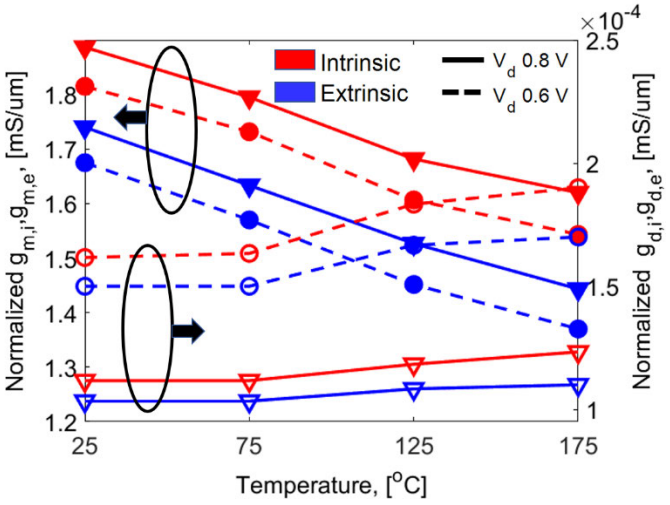

Fig. 4. Variation of maximum normalized intrinsic and extrinsic transconductance $g_{m,i}$ and $g_{m,e}$ and output intrinsic and extrinsic conductance $g_{d,i}$ and $g_{d,e}$ with temperature at $V_d = 0.8$ V (solid lines) and 0.6 V (dashed lines) and V_g corresponding to $g_{m,\max}$.

intrinsic parameters refer to the case where the parasitics are removed.

Thus, extrinsic parameters $C_{\mathrm{gd},e}$, $C_{\mathrm{gs},e}$, and $C_{\mathrm{ds},e}$ refer to the parasitic gate-to-drain capacitance, gate-to-source capacitance, and drain-to-source capacitance, respectively, while $g_{m,i}$, $C_{\mathrm{gd},i}$, $C_{\mathrm{gs},I}$, and $C_{\mathrm{ds},i}$ represent their intrinsic counterparts. The gate, drain, and source resistances are represented as R_g, R_d, and R_s, respectively. The total gate capacitance $C_{\mathrm{gg},T}$ is the sum of the total gate to drain capacitance $C_{\mathrm{gd},T}$, and total gate to source capacitance $C_{\mathrm{gs},T}$, while the source to drain resistance R_{sd} is defined as the sum of source resistance R_s and drain resistance R_d. In this article, these aforementioned SSEC parameters are demonstrated separately. Note that the parameter values are normalized with respect to the device total width.

Two salient RF FoMs are the current-gain cutoff frequency f_T and maximum oscillation frequency $f_{\max}$. Commonly used expressions for computing f_T and $f_{\max}$ are shown in (1) and (2), respectively

$$f_T \approx \frac{g_{m,e}}{2\pi\left(C_{\mathrm{gs},T}+C_{\mathrm{gd},T}\right)} \tag{1}$$

$$f_{\max} \approx \frac{f_T}{2\sqrt{2\pi f_t R_g C_{\mathrm{gd},T}+\left(R_s+R_g\right)g_{d,e}}} \tag{2}$$

$$f_T,\, f_{\max} \approx \frac{g_{m,e}}{2\pi\left(C_{\mathrm{gs},T}+C_{\mathrm{gd},T}\right)}. \tag{3}$$

In Fig. 3, the ZTC point for the transconductance g_m is found to be for V_g around 0.36 V, for which g_m is constant with temperature. The reduction in maximum transconductance $g_{m,\max}$ with temperature obtained from dc measurements is shown in the inset. Similar to the I_d behavior compared to the I_d-ZTC, g_m increases and decreases, respectively, below and above the g_m-ZTC point. The g_m-ZTC could be of great importance for applications that require temperature invariant g_m. As f_T is proportional to g_m, this relates to a ZTC in f_T (where f_T does not change with temperature) at that corresponding ZTC point for g_m, provided that the total gate capacitance $C_{\mathrm{gg},T}$ is relatively independent of temperature as shown later.

Both the maximum intrinsic and extrinsic transconductances $g_{m,i}$ and $g_{m,e}$ show a degradation of around 18% going from 25 °C to 175 °C, respectively, as demonstrated in Fig. 4. The trends are verified for two different V_d cases, 0.8 and 0.6 V with V_g corresponding to $g_{m,\max}$. A similar range of degradation in $g_{m,i}$ was observed in case of bulk and PD-SOI technologies studied in [7] was found to be 16.5% and 20.2%, respectively. An increase of around 10% is observed in intrinsic and extrinsic g_d. The absolute value of $g_{m,e}$ extracted from RF measurements is noted to be higher than that from dc measurements because of the removal of dynamic self-heating in the former case.

Fig. 5 demonstrates the variation of total intrinsic gate capacitance $C_{\mathrm{gg,Ti}}$ $(C_{\mathrm{gs},i}+C_{\mathrm{gd},i})$ versus temperature, extracted for $V_d = 0.8$ and 0.6 V each. $C_{\mathrm{gg,Ti}}$ extracted is mainly steady over the temperature range of 25 °C–175 °C, varying by only a few femtofarads, which is within the range of the extraction precision. Capacitances $C_{\mathrm{gs},i}$, $C_{\mathrm{gd},i}$, and $C_{\mathrm{ds},i}$ are also individually found to be steady with temperature as well.

The degradation of gain A_V, calculated as the ratio of $g_{m,i}/g_{d,i}$, with increasing temperature at the bias condition $V_d = 0.8$ V and $V_g = 0.6$ V, is shown in Fig. 6. A 23%

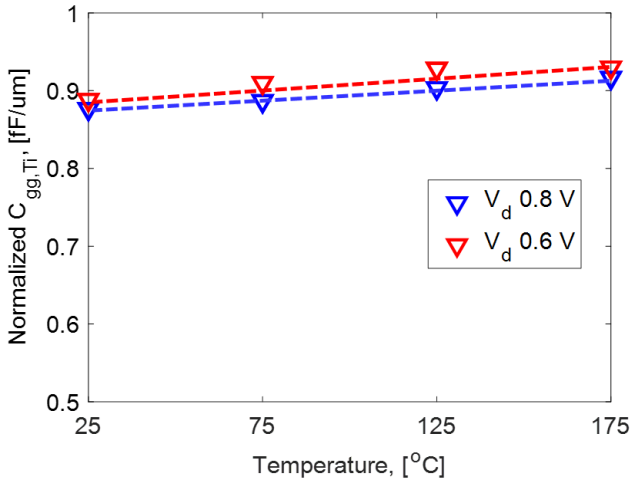

Fig. 5. Variation of normalized total intrinsic gate capacitance $C_{gg,Ti}$ ($C_{gs,i} + C_{gd,i}$) with temperature at $V_d = 0.8$ and 0.6 V with V_g corresponding to $g_{m,max}$.

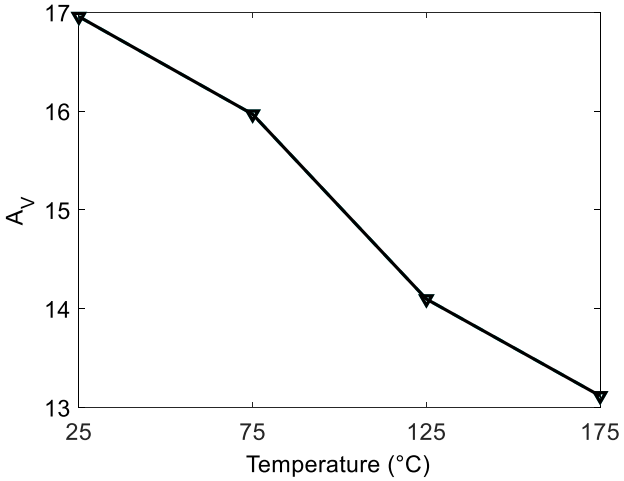

Fig. 6. Variation of intrinsic voltage gain A_V with temperature for $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$.

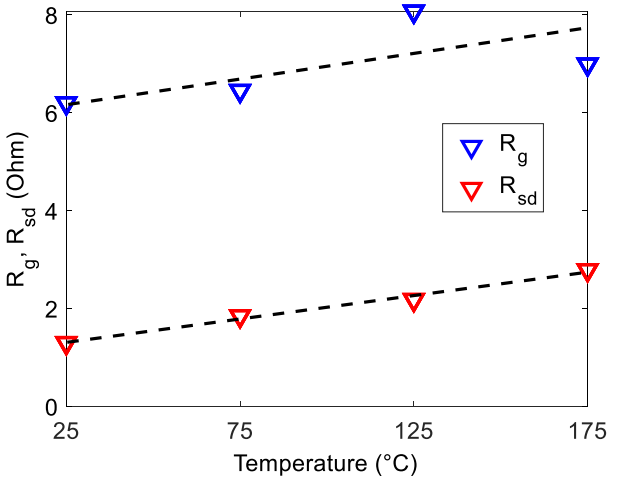

Fig. 7. Variation of gate resistance R_g and source–drain resistance R_{sd} ($R_s + R_d$) with temperature.

reduction in A_V is followed up from decreasing intrinsic g_m and slightly increasing g_d on increasing the temperature from 25 °C to 175 °C.

Fig. 7 shows the variation of resistances with temperature. It is observed that both the gate resistance R_g and the source to drain resistance R_{sd} ($R_s + R_d$) increase with temperature.

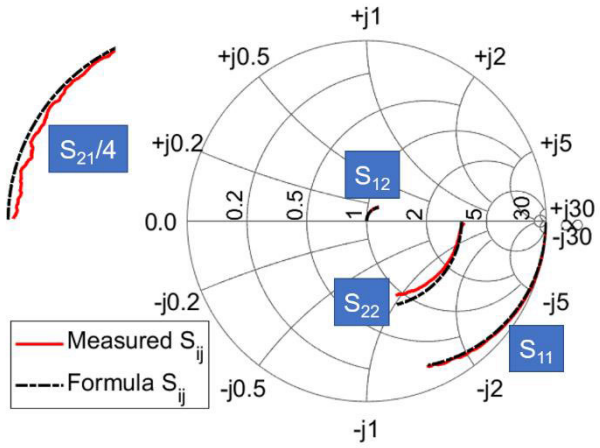

Fig. 8. Comparison of S-parameters measured and reconstructed from SSEC at room temperature for $V_d = 0.8$ V and $V_g = 0.6$ V.

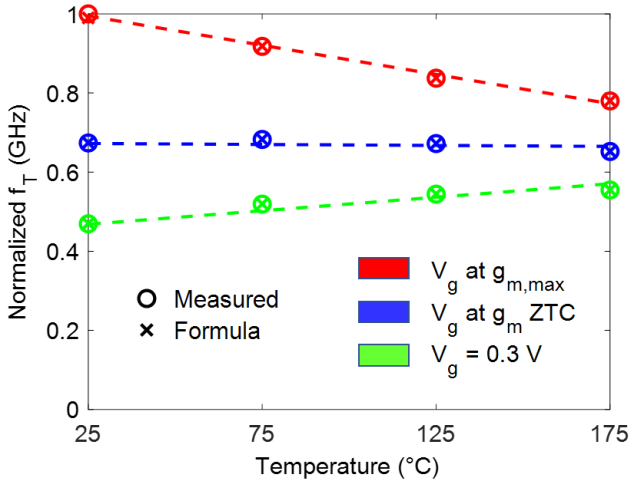

Fig. 9. Variation of normalized current-gain cutoff frequency f_T with temperature at $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$, g_m-ZTC, and 0.3 V (below g_m-ZTC). Normalization with respect to f_T from measurements at V_g corresponding to $g_{m,max}$ at 25 °C and $V_d = 0.8$ V.

In [8], R_g was observed to rise around 22% on increasing the temperature from 25 °C to 125 °C, in line with the 15% rise in R_g observed on the trends in this work.

Using the SSEC, the S-parameters are reconstructed; a comparison between the measured S-parameters and the ones reconstructed using the SSEC in Fig. 8 shows a good fit for the room temperature measurements. The fitting is verified at other temperature points too.

The effect of increase in temperature on the two main RF FoMs, the current-gain cutoff frequency f_T and maximum oscillation frequency f_{max}, is shown in Figs. 9 and 10, respectively. f_T and f_{max} are computed by two methods: first from the extrapolation of the current gain H_{21} and unilateral gain to 0 dB, respectively (which are in turn found from the S-parameter measurements). The values obtained from this method are referred to as those measured. Second, f_T and f_{max} are also computed from (1) and (2), respectively, involving the extracted SSEC parameters. The values obtained thus are referred to as the formula. An excellent correlation is obtained between the f_T and f_{max} values obtained from the measurements, and the formula using SSEC parameters is for each temperature and bias condition case investigated in this

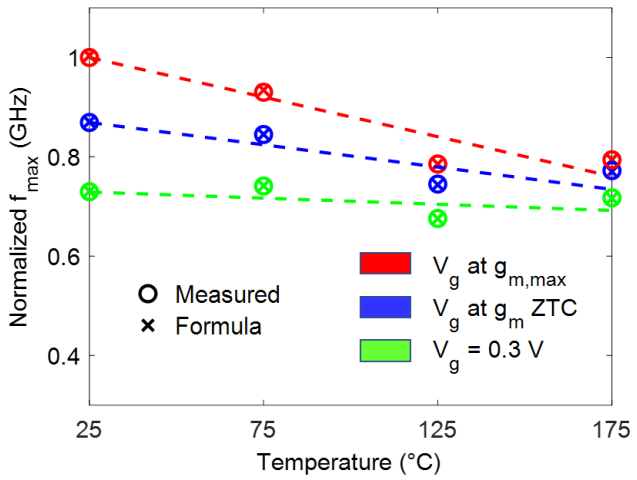

Fig. 10. Variation of normalized maximum oscillation frequency f_{max} with temperature at $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$, g_m-ZTC, and 0.3 V (below g_m-ZTC). Normalization with respect to f_{max} from measurements at V_g corresponding to $g_{m,max}$ at 25 °C and $V_d = 0.8$ V.

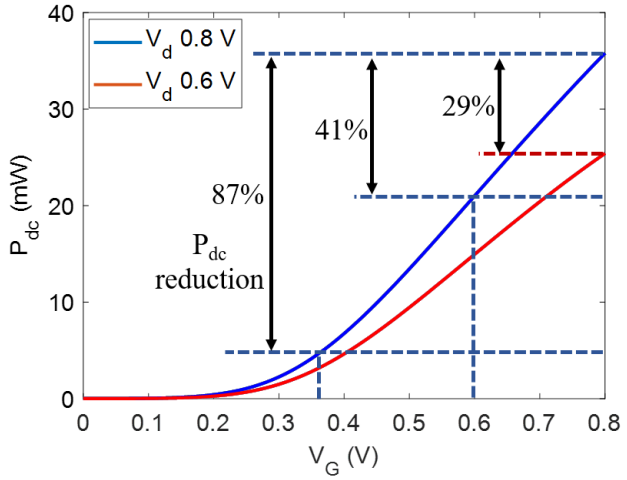

Fig. 11. P_{dc} variation with V_d showing percentage P_{dc} reduction at various biases.

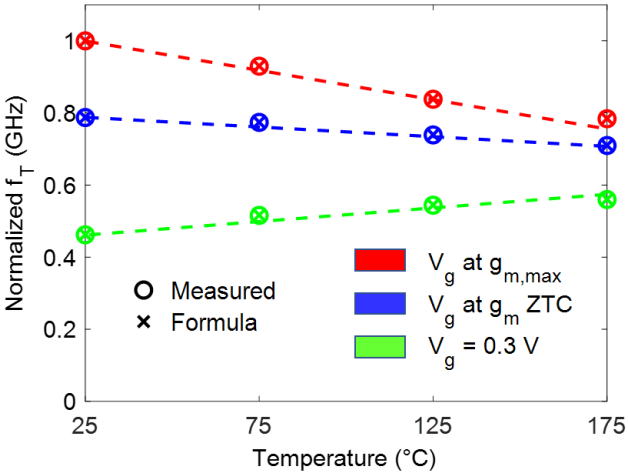

Fig. 12. Variation of normalized current-gain cutoff frequency f_T with temperature at $V_d = 0.6$ V and V_g corresponding to $g_{m,max}$, g_m-ZTC, and 0.3 V (below g_m ZTC). Normalization with respect to f_T from measurements at V_g corresponding to $g_{m,max}$ at 25 °C and $V_d = 0.6$ V.

study. All the f_T and f_{max} values have been normalized with respect to the peak f_T and f_{max} value (for V_g corresponding to maximum g_m) at room temperature of 25 °C. The computation of f_T and f_{max} has been carried out under three different bias conditions as well in order to better demonstrate the significance of the g_m-ZTC point. Each of these cases has V_d of 0.8 V or V_d of 0.6 V (for low-power applications), whereas V_g is varied: 1) corresponding to $g_{m,max}$ in which case the peaks f_T and f_{max} are observed; 2) corresponding to g_m-ZTC; and 3) below g_m-ZTC, at a value of V_g of 0.3 V.

A. Extraction at $V_d = 0.8$ V

First, considering V_g corresponding to $g_{m,max}$ bias condition and $V_d = 0.8$ V, it is observed from Fig. 9 that f_T degrades in a similar manner to g_m as expected. Qualitatively, referring back to (3), f_T is proportional to $g_{m,e}$ and this is the basis of this deduction. Following up from this, f_{max} is seen to be degrading with temperature as well. Going from room temperature of 25 °C–175 °C, a reduction of around 20% can be observed for both peak f_T and f_{max}, respectively, for V_g corresponding to $g_{m,max}$.

Second, the bias condition considered was V_g corresponding to g_m-ZTC (0.36 V in this case) and $V_d = 0.8$ V. At this g_m-ZTC bias point, g_m is independent of temperature, and therefore, we expect a much steadier f_T and f_{max} value with temperature since g_m is one of the main factors affecting both. This is verified from the following figures, where f_T is extremely stable with temperature (varying by 3% only over the temperature range) and f_{max} also shows a relatively reduced variation of 10%. The fact that the variation of the resistances also comes into play for the f_{max} reduction makes its behavior somewhat more variable than that of f_T. Given the fact that the absolute value of g_m at this bias point is lesser than that at the $g_{m,max}$ point, the absolute values of f_T and f_{max} are lower compared with the $g_{m,max}$ case that is evident from the magnitude of the normalized values at this bias condition.

Third, for a bias condition situation where V_g is 0.3 V and $V_d = 0.8$ V, that is V_g is below the g_m-ZTC of 0.36 V, an improvement in f_T of around 20% is observed with temperature in Fig. 9. This is due to an expected improvement in g_m with temperature under this bias condition. The f_{max} degradation at this bias is also much lesser than the two aforementioned cases as seen in Fig. 10. f_{max} is found to be relatively steady with temperature. This can be explained by the improvement of f_T with temperature that is directly proportional to f_{max} in (2). Note that the magnitudes of f_T and f_{max} are reduced further in this case because of further reduction in the magnitude of g_m itself at lower V_g bias. At V_d 0.8 V, the absolute values of peak f_T and f_{max} were 325 and 352 GHz, respectively.

B. Extraction at $V_d = 0.6$ V

From a dc power point of view, $P_{dc} = I_d$–V_d, lowering V_d results in lower I_d as well, thereby further lowering the I_d–V_d product P_{dc}. When V_g is kept constant at 0.8 V at 25 °C, P_{dc} is reduced around 29% from 35 to 25 mW by stepping down V_d from 0.8 to 0.6 V in line with low-power application trends. Alternatively, at $V_d = 0.8$ V, stepping down V_g to 0.6 and 0.36 V corresponding to $g_{m,max}$ and $g_{m,ZTC}$, respectively, reduces P_{dc} by 41% and 87%, seen in Fig. 11.

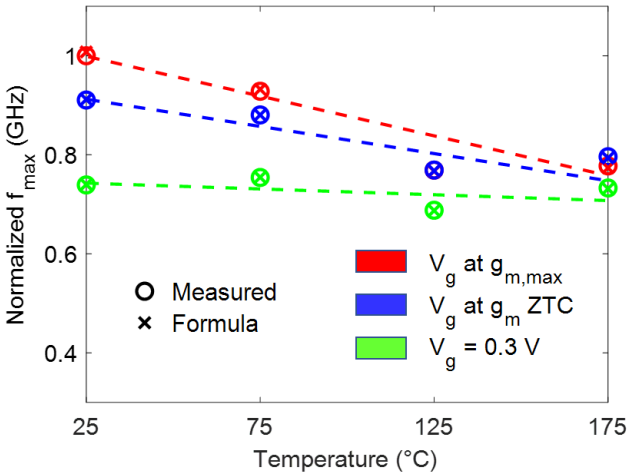

Fig. 13. Variation of normalized maximum oscillation frequency f_{max} with temperature at $V_d = 0.6$ V and V_g corresponding to $g_{m,max}$, g_m-ZTC, and 0.3 V (below g_m-ZTC). Normalization with respect to f_{max} from measurements at V_g corresponding to $g_{m,max}$ at 25 °C and $V_d = 0.6$ V.

The variation in f_T and f_{max} is studied next with V_d being stepped down to 0.6 V (from the earlier case of 0.8 V) for the three different V_g bias conditions again: V_g for $g_{m,max}$, V_g at $g_{m,ZTC}$, and $V_g = 0.3$ V (below $g_{m,ZTC}$). The trends observed in Figs. 12 and 13 are similar, and the f_T and f_{max} ZTC are observed around $g_{m,ZTC}$ and $V_g = 0.3$ V, respectively. At V_d 0.6 V, the absolute values of peak f_T and f_{max} were 302 and 322 GHz, respectively.

From a magnitude point of view, moving to $V_d = 0.6$ V reduces peak f_T and f_{max} by 7% and 10.8%, respectively. Due to the high f_T and f_{max} offered by this technology, moving from V_d 0.8 to 0.6 V provides around 29% reduction in P_{dc} while affecting f_T, f_{max} to a very limited extent. The resulting f_T and f_{max} values are high enough for standard RF applications.

IV. Conclusion

The impact of increased temperature on the performance of 22-nm FD-SOI MOSFETs is investigated. From the I_d–V_g characteristics, ZTC points for I_d and g_m were found to be at gate voltages V_g of 0.62 and 0.36 V, respectively. For the RF FoMs, around 20% reduction in both peak f_T and peak f_{max} was observed when temperature is increased from 25 °C to 175 °C. Due to the extraction of the SSEC, the degradation in g_m with temperature was found to be one of the major factors for the reduction in the aforementioned FoMs with the capacitances being mostly steady with temperature while the resistances increase. At the g_m-ZTC point, f_T and f_{max} are found to be more stable with temperature, with f_T varying within 3% and f_{max} varying around 11%. Below the g_m-ZTC point for V_g of 0.3 V, an improvement in f_T with temperature of around 20% is seen, whereas f_{max} is found to be rather steady with temperature. From a low-power application point of view, stepping down V_d from 0.8 to 0.6 V helps in reducing P_{dc} while affecting f_T and f_{max} limitedly, motivating the possibility to go to this bias condition when necessary. The utilization of the back gate to tune RF and noise performance over temperature is a prospect for future research.

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