A systemic analysis of silicon substrates toward improvements of integrated FD-SOI circuits performance at mm-wave frequencies

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Abstract

The emergence and deployment of new telecommunication standards (5G then 6G) requires low-cost, high RF performance and high integration density technologies. Fully-depleted-Silicon-on-Insulator (FD-SOI) technology is ideally placed in this context, thanks to best-in-class RF performance among CMOS, low-cost, high-volume manufacturability and intrinsic advantages enabling additional configurability. Furthermore, FD-SOI -in its current state- can be further engineered to meet current and future high-frequency challenges.

In particular, this thesis studies the performance improvements for millimeter-wave (mm-wave) applications that can be achieved in FD-SOI technology by replacing the current, moderately lossy substrate by a high-resistivity substrate of high RF quality. A systemic approach is adopted to analyze in depth the high-frequency performance at different levels of the integrated circuit, covering the substrate, transistor, passive elements and active circuits.

For the above analyses, accurate on-wafer characterization at mm-wave frequencies is needed. The origin of systematic errors in measurements generated at the 'probe-tip' calibration step is discussed in terms of user-related manipulation error and invalid assumptions made in the calibration process. We specifically show how (i) probe misplacement on standards measurements and (ii) radiation, dispersion and higher-order modes propagation on coplanar waveguide lines of commercial calibration substrates create systematic errors that are propagated and degrade the device under test characterization accuracy.

The challenging topic of characterizing low levels of substrate losses at high frequencies is also covered, enabling the monitoring of disruptive ideas development for new substrate solutions. Several extraction approaches are discussed to deal with the associated challenges and applied to a set of silicon substrates, covering a wide range of substrate resistivity values. Moreover, a careful sensitivity analysis demonstrates that an accurate extraction can still be achieved up to $\sim 50-60\,\text{GHz}$ for moderately low-loss substrates, despite the presence of residual systematic errors.

At transistor level, a detailed wideband MOSFET behavior analysis is carried out in two steps. With a careful 'in-situ' calibration procedure performed on custom-designed standards, we achieve a highly accurate MOSFET characterization up to 110 GHz and demonstrate high RF performance and the great fidelity of the process design kit's compact model.

In a distinct step, two concurrent effects: self-heating and substrate effects, are identified in the wideband, low frequency response (100 kHz to 10 GHz)

of a measured transistor. An original approach is introduced and successfully applied to unambiguously extract both effects in an ultra-thin body and buried oxide (UTBB) transistor.

Concerning high-level circuit aspects, this thesis presents the design of a 39 GHz low-noise amplifier (LNA) and two 24-43 GHz power amplifiers (PAs) in 22 nm FD-SOI technology. A special attention is dedicated to their behavior with back-gate bias modulation, enabling to trade-off key figures of merit in a simple way. Exhibiting great performance (noise figure as low as 2.5 dB, saturated power and efficiency as high as 20.1 dBm and 36.4 %), the presented circuits are in line with the state of the art in CMOS technology.

A recent innovative technique to passivate the silicon-oxide interface is applied to the industrial 22 nm FD-SOI technology fabricated on high-resistivity substrates. Experimental results demonstrate low substrate losses and substrate-induced harmonic distortion reduction with this new passivation solution. Furthermore, dielectric-like substrate coupling and quality factor enhancement of passive devices are also obtained in this technology with the passivation technique applied to high-resistivity wafers.

Circuit-level improvements are investigated via simulations thanks to the high measurement-simulation agreement obtained for the designed circuits. It is shown that, while little reduction in noise figure for the designed LNA with a low-loss Si substrate is expected, a substantial improvement can be achieved for the designed PAs. Thanks to substrate-induced insertion loss reduction in passives at the PAs' output, up to 0.8 dB in output power and 5 % in peak efficiency increases are expected with low-loss Si substrates.

Finally, perspectives of further developments enabled by all the work presented in this thesis are discussed. A wide range of topics are covered: (i) reduction of residual systematic errors in on-wafer mm-wave measurements, (ii) new interesting applications for the developed self-heating and substrate effects characterization technique, (iii) opportunities of adaptive body-biasing technique for circuit performance improvement, (iv) further assessment of substrate properties impact on circuit-level performance by the design of different circuits or with different topologies.

Overall, *this thesis demonstrates that enhancing the RF substrate quality in an FD-SOI technology can lead to substantial improvement of passives and circuits at mm-wave frequencies, and therefore paves the way for potential adoption of high-resistivity substrates in future industrial UTBB FD-SOI technology*.

Author's Publication List

Awards

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Acronyms

3G Third Generation of mobile telephony.
4G Fourth Generation of mobile telephony.
5G Fifth Generation of mobile telephony.
6G Sixth Generation of mobile telephony.

ABB Adaptive body-biasing.
ac Alternating current.
ACLR Adjacent channel leakage ratio.
AM-AM Output signal amplitude variation due to input signal amplitude variation.
AM-PM Output signal phase variation due to input signal amplitude variation.

BEOL Backend-of-line.
BER Bit error rate.
BiCMOS Bipolar CMOS.
BOX Buried oxide.

calkit Calibration kit.
CCDF Complementary cumulative distribution function.
CMOS Complementary metal-oxide-semiconductor.
CPP Contact-poly-pitch.
CPW Coplanar waveguide.

dc Direct current.
DIBL Drain-induced barrier lowering.
DPD Digital predistortion.
dut Device under test.

E-field Electric field.
EM Electromagnetic.
ESD Electrostatic discharge.
eSI enhanced signal integrity.
EVM Error vector magnitude.

FBB forward body-bias.
FD Fully-depleted.
FEM Front-end module.
FEOL Front-end-of-line.
FET Field effect transistor.
FoM Figure of Merit.
FR2 Frequency range 2.

G-CPW Grounded coplanar waveguide.
GaAs Gallium arsenide.
GSG Ground-Signal-Ground.

H1 Fundamental power.
H2 Second harmonic power.
H3 Third harmonic power.
HC Hybrid coupler.
HF High frequency.
HR High-resistivity.

IC Integrated circuit.
IF Intermediate frequency.
III-V Compound semiconductor containing elements from groups III and V in the periodic table.
IIP3 third-order input referred intercept point.
IL Insertion loss.
IMD3 Third-order intermodulation product.
IoT Internet-of-Things.
IP3 third-order intercept point.

LNA Low noise amplifier.
LRM Line-Reflect-Match calibration technique.
LRRM Line-Reflect-Reflect-Match calibration technique.
LTE Long-Term Evolution.
LVT Low-threshold voltage.

MIMO multiple input, multiple output.
mm-wave Millimeter-wave.
MOSFET Metal-oxide-semiconductor field effect transistor.
mTRL multiline Thru-Reflect-Line calibration technique.

NF Noise figure.
NIST National Institute of Standards and Technology.
NQS Non-quasi-static.

OFDM Orthogonal frequency division multiplexing.

P1dB 1 dB compression point.
PA Power Amplifier.
PA1 24-43 GHz wideband power amplifier designed in this thesis.
PA2 24-43 GHz configurable balanced power amplifier designed in this thesis.
PAE Power-added efficiency.
PAPR Peak-to-average power ratio.
PD Partially-depleted.
PDF Probability distribution function.
PDK Process design kit.
PEX Parasitic extraction.
POR Process of record.
PSC Parasitic surface conduction.

QAM Quadrature amplitude modulation.

RBB reverse body-bias.
RF Radio frequency.
RFIC Radio frequency integrated circuit.
RLGC Equivalent per-unit-length lumped model of a transmission line.
RVT Regular threshold voltage.
RX Receiver.

S-parameters Scattering parameters.

SA Spectrum Analyzer.
SC Single-carrier.
SCE Short channel effects.
SE Substrate effect.
SH Self-heating.
SHE Self-heating effect.
Si Silicon.
SLVT Super low-threshold voltage.
SNR Signal-to-noise ratio.
SOI Silicon-on-Insulator.
SOLT Short-Open-Load-Thru calibration technique.
std Standard-resistivity.
STI Shallow trench isolation.
STS Strain transfer structure.

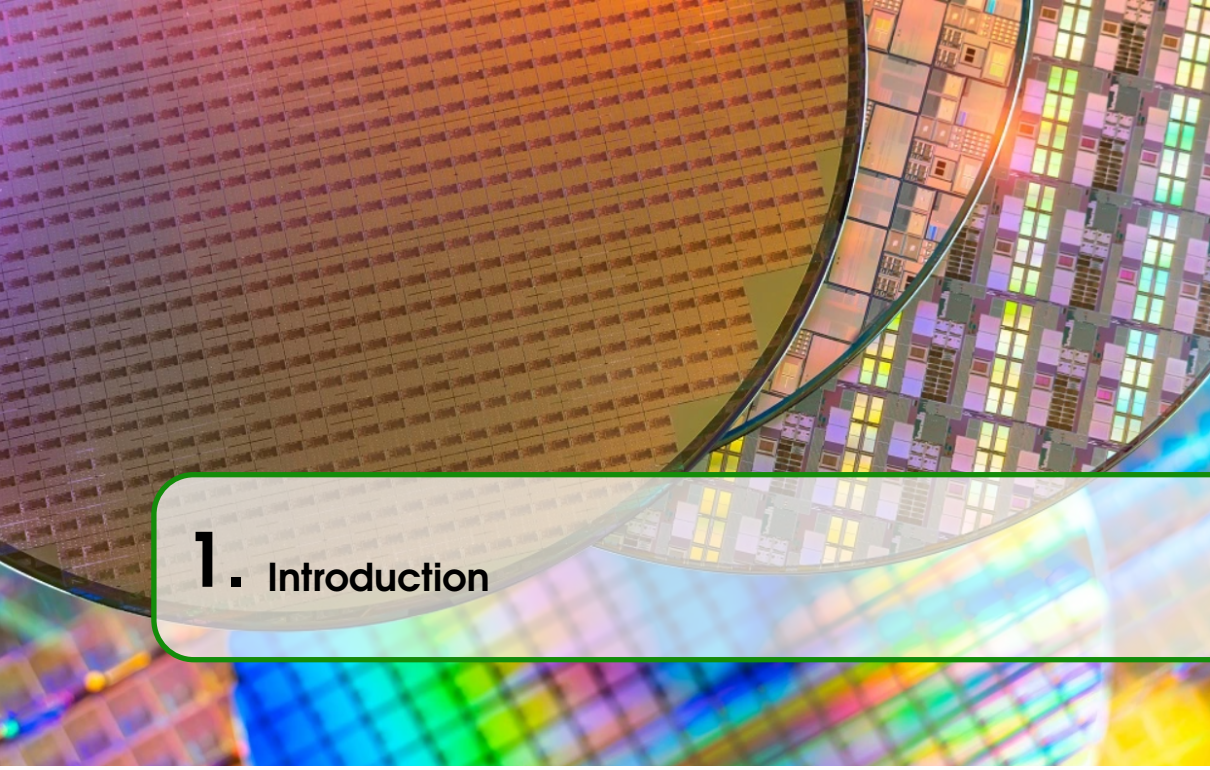
TEM Transverse electromagnetic.
TFMS Thin film microstrip line.
TL Transmission line.
TR Trap-rich.
TRL Thru-Reflection-Line calibration technique.
TX Transmitter.

UTBB Ultra-thin body with ultra-thin buried oxide.

VGA Variable gain amplifier.
VNA Vector network analyzer.
VSG Vector Signal Generator.
VSWR Voltage standing wave ratio.

Winfab Wallonia Infrastructure for Nano FABrication, cleanroom facilities at Université catholique de Louvain.

ZTC Zero-temperature coefficient.



1. Introduction

1.1 Context

Driven by the ever-increasing demand of more bandwidth for faster telecommunication with increased amount of data transfer, the RF electronic world has known a tremendous growth in the last two decades. The succession of various telecommunication standards (3G, 4G and now 4G LTE) has required mobile phones to be compatible with multiple frequency bands. To support a whole range of network configurations, the front-end module is becoming increasingly more complex [1, 2]. The emergence of 5G and Internet-of-Things (IoT) will lead to another strong growth in the RF industry that must be supported by a technology with low-cost and high-volume manufacturability. In addition, new transceiver architectures are investigated, in order to support new 5G functionalities (beamforming, multiple input multiple output, use of millimeter-wave spectrum), hence further increasing the front-end module complexity, which means a higher level of flexibility, configurability and at higher frequencies. The Silicon-on-Insulator (SOI) platform, fulfilling the demands of high-volume, low-cost manufacturability, and integrating high-performance RF functions along with digital, analog and mixed-signal circuitry, is an outstanding contender to meet the technological challenges presented by 5G.

RF-SOI technology (with partially-depleted Silicon-on-Insulator transistors, PD-SOI) offering high RF performance at low cost has become the mainstream

technology for RF switch banks in 4G LTE mobile applications [3] and is a serious candidate for 5G applications meeting the telecommunication standard's performance requirements [4]. Fully-depleted-SOI (FD-SOI), on the other hand, -also featuring outstanding RF performance, low power, with increased logic density and further room for device scaling and technology improvement- is of great interest for 5G applications and beyond, especially when configurability and flexibility come into play.

The SOI technology consists of a relatively thin layer of silicon -where the active devices are fabricated- on top of a dielectric (buried oxide, or BOX, in silicon dioxide) lying above a handle silicon substrate. This architecture provides numerous and well-known advantages of SOI technology with respect to bulk CMOS [5, 6], in terms of lower power consumption, reduced short-channel effects (SCEs), reduced and linear junction capacitances, fewer fabrication steps (thus lower production cost), robustness against radiation, etc.

The physical separation between active device and substrate has enabled to separately optimize each part. The developments of new device architectures (PD-SOI and FD-SOI) and low-loss, highly-linear substrates are at the origin of the commercial success of RF-SOI technology.

1.1.1 Introduction to FD-SOI

In FD-SOI device shown in **Figure 1.1**, which is discussed throughout this thesis, the silicon film on top of the BOX is made so thin that the depletion region below the inversion channel extends down to the buried oxide. The entire silicon (Si) film is depleted from free carriers, whence fully-depleted. In order to limit short channel effects (SCE), the channel thickness must be approximately $1/4$ of the channel length [7]. No channel doping is required since the Si film is entirely depleted thanks to its thin dimension. This architecture naturally enhances the electrical performances of the MOSFET with almost ideal subthreshold slope, reduced drain induced barrier lowering (DIBL) and lower output conductance. Not necessitating halo implant and channel doping induces a great improvement in variability compared with bulk CMOS [8]. Furthermore, in ultra-thin body and BOX (UTBB) FD-SOI, the front-side transistor's electrostatics can be controlled from the doped region underneath the thin BOX (called back-gate or body region). The front-gate threshold voltage (V_{th}) can be tuned by applying a voltage on the back-gate, which opens many perspectives in circuit. This device can be seen as an asymmetrical double gate transistor, with one gate at the front side (the regular one) and the other being the back-gate with the BOX as the

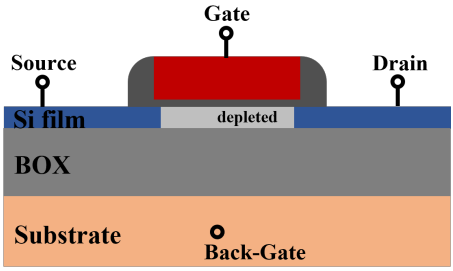


Figure 1.1: Sketch of FD-SOI MOSFET. The figures are not to scale. In case of ultra-thin BOX, the FD-SOI usually has an additional back-gate terminal.

back-side gate oxide.

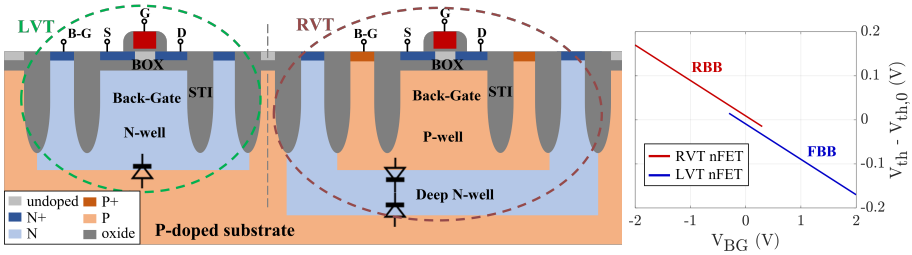
RF performance

Furthermore, beside the great dc figures of merit (FoMs), FD-SOI technology features excellent analog and RF properties. The two main RF FoMs are the cutoff frequency (f_t) and the maximum oscillation frequency (f_{max}). f_t and f_{max} are the frequencies at which the short circuited output current gain and maximum available gain, respectively, are unity. They are general indicators of how much gain a transistor can amplify at a given frequency, or until which frequency a transistor can be used to amplify a signal ($\sim 1/5$ to $1/3$ of f_t and f_{max} as a rule of a thumb). They are also found in other more specific FoMs, such as the noise figure (defined in **Chapter 5**). Benefiting from gate length reduction and controlled parasitics scaling, f_t and f_{max} well above 300 GHz have been demonstrated. FD-SOI technology currently exhibits the largest f_t and f_{max} pair[1] of 365 and 413 GHz for a single transistor among all CMOS technologies **[9]**, comparable with BiCMOS and some III-V technologies, to the best of our knowledge.

Back-gate as RF tuning knob

With the additional back-gate terminal, the UTBB FD-SOI technology offers a unique feature with several implications. As mentioned above, the front-gate electrostatics can be controlled by the back-gate voltage. This is not a new feature per se, as body biasing can also be used in planar bulk technology. The differentiator is the tuning range offered by UTBB: bulk CMOS has a lower

[1] The best pair in the sense that the lowest value between f_t and f_{max} for a single transistor is the highest.



(a) (b)

Figure 1.2: Left (a): cross-section view of LVT (left) and RVT (right) nMOSFETs with back-gate terminals (B-G) and wells, deep N-well, p-doped substrate, diodes and shallow trench isolations (STI). Right (b): illustration of V_{th} tuning with back-gate bias variation with reverse body-bias (RBB) in RVT nFETs or forward body-bias (FBB) in LVT nFETs.

body factor (25 mV/V) and the effective safe body-bias voltage range spans from ~ -0.3 to ~ 0.3 V, yielding a V_{th} modulation of approximately ± 75 mV [10]. **Figure 1.2a** shows a schematic of two flavors of UTBB nMOSFET: regular V_{th} (RVT) and low V_{th} (LVT). Thanks to the electrical isolation by the BOX of the source and drain regions from the back-gate, the only limiting parasitic diodes are those between the N-back-gate and P-substrate (for LVT, flipped well) and between the P-back-gate and deep N-well (for RVT, conventional well). These are Zener-type diodes, which, together with the breakdown voltage of the thin BOX, limits the maximum magnitude of the back-gate voltage to 2 V (for 22 nm FD-SOI). Overall, with a much larger body factor of ~ 80 mV/V, the V_{bg} tuning range spans from -0.3 V to 2 V for LVT nMOSFETs (forward body-bias, FBB) and from -2 V to 0.3 V for RVT nMOSFETs (reverse body-bias, RBB), yielding a total V_{th} variation range of ~ 200 mV as illustrated in **Figure 1.2b**.

This wide V_{th} tuning range does not come with performance degradation penalty, as the RF FoMs are essentially shifted due to different bias condition. So, in general, the back-gate terminal can be seen as a tuning knob, with a potentially great impact on circuit design thanks to the offered additional configurability.

1.1.2 Common SOI substrates

The active device does not define the technology performance by itself alone, the substrate also has a role. Indeed, the physical properties of the underlying substrate have a strong impact on device and circuit performance, particularly at RF and millimeter-wave (mm-wave) frequencies and can induce losses, non-linearity and increase the complexity of parasitic coupling modeling.

Standard (std) resistivity silicon substrates ($\sim 10\,\Omega\,$cm, cf. **Figure 1.3a**) have strong RF losses, non-linearity, inter-device coupling and degrade the quality factor of passives (inductors, coplanar waveguide lines, CPW) **[3]**. Overall, they are of mediocre performance for RF and mm-wave circuits. Moving to high-resistivity (HR) substrates ($> 3\,\text{k}\Omega\,$cm, cf. **Figure 1.3b**) is of little benefit, as the parasitic surface conduction (PSC) phenomenon counteracts the large substrate resistivity and still exhibits large (although lower than std Si substrate) losses and non-linearity. This PSC effect originates in the presence of fixed charges (generally positive) trapped in the BOX and generated during manufacturing that induces a thin sheet of highly conductive free carriers (generally electrons) at the silicon-BOX interface. Several solutions have been proposed to counter this PSC effect. The most famous and spread technique is the trap-rich (TR) substrate **[11]** illustrated in **Figure 1.3c**. In such substrates, a layer rich of traps is created with poly-silicon deposited on top of the high-resistivity Si substrate, at the interface with the BOX. The amount of traps is so high that the Fermi level is pinned in this layer close to the mid-gap, resulting in an extremely low amount of free carriers and therefore a high local resistivity. The TR substrate exhibits very low RF losses, enhanced quality factor of passives **[12, 13]**, high linearity **[14, 15]**, inter-device capacitive-like coupling at RF frequencies **[16]**.

A major advantage of the SOI architecture is the separation of the intrinsic device from the bulk substrate. This flexibility allows to engineer the intrinsic device and the substrate separately (to first order) and achieve a combination of the best of two worlds: benefiting from the advantages of SOI at the device level and from a high RF quality substrate with low losses and high linearity. TR is the benchmark Si substrate for SOI technologies with best high frequency performance and has been widely commercialized in RF-SOI technology. It is however not directly compatible with UTBB FD-SOI technology, as the defect-rich poly-silicon layer degrades the isolation of the back-gate contact of FD-SOI devices with the substrate's junctions, therefore increasing the reverse diode current. Nevertheless, other solutions compatible with the UTBB FD-SOI

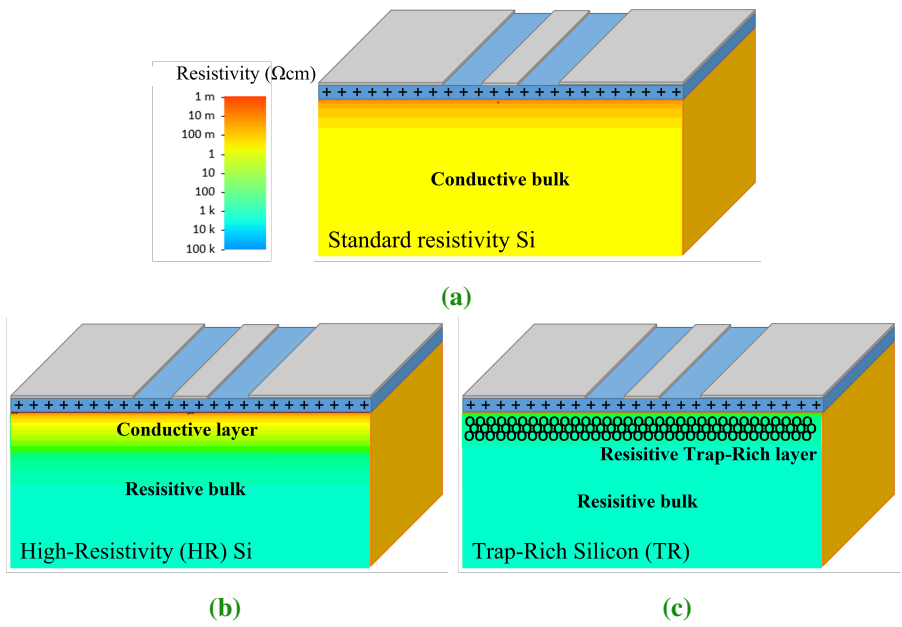


Figure 1.3: Schematic representation of a standard Si substrate (a), high-resistivity Si substrate (b), trap-rich Si substrate (c) with an arbitrary CPW line on top as device. A representative profile of the local resistivity is given inside the substrates with the scale present in (a). Fixed charges (in '+' symbols inside the BOX) attract free carriers at the Si-oxide interface inducing a thin conductive layer that mitigates the benefits of HR substrates. This conductive sheet is suppressed thanks to the introduction of a trap-rich layer in the TR Si substrate, yielding a high quality RF substrate.

process have been successfully demonstrated to counter the PSC effect [17, 18], in particular the *PN junctions interface passivation* introduced in [19] that will be further discussed in **Chapter 6**.

1.2 Substrate impact on integrated circuits

To illustrate how the substrate properties can affect overlying circuitry, an example of CMOS integrated circuit (IC) working at millimeter-wave frequencies is provided in **Figure 1.4**. It is made of several active and passive devices commonly separated in distinct regions as pinpointed in the figure.

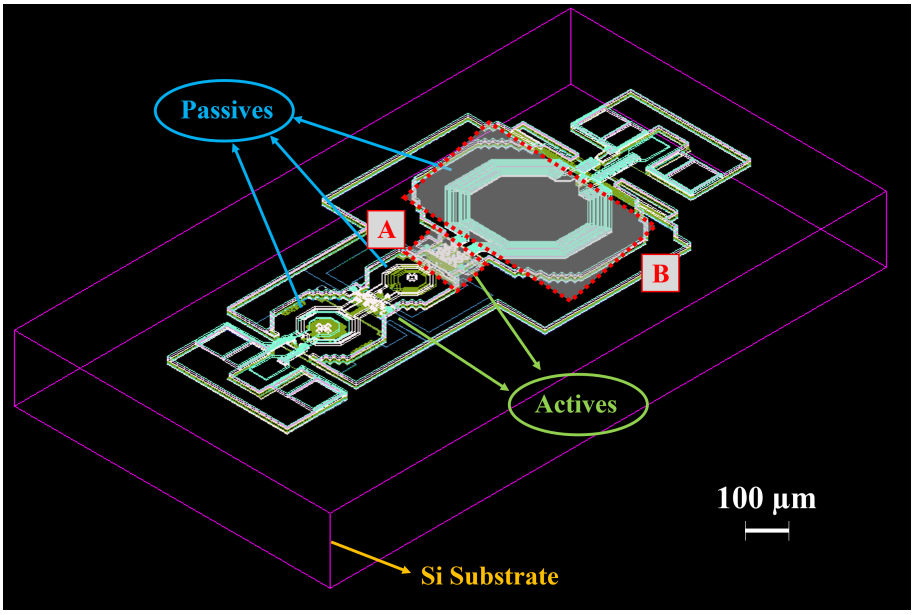
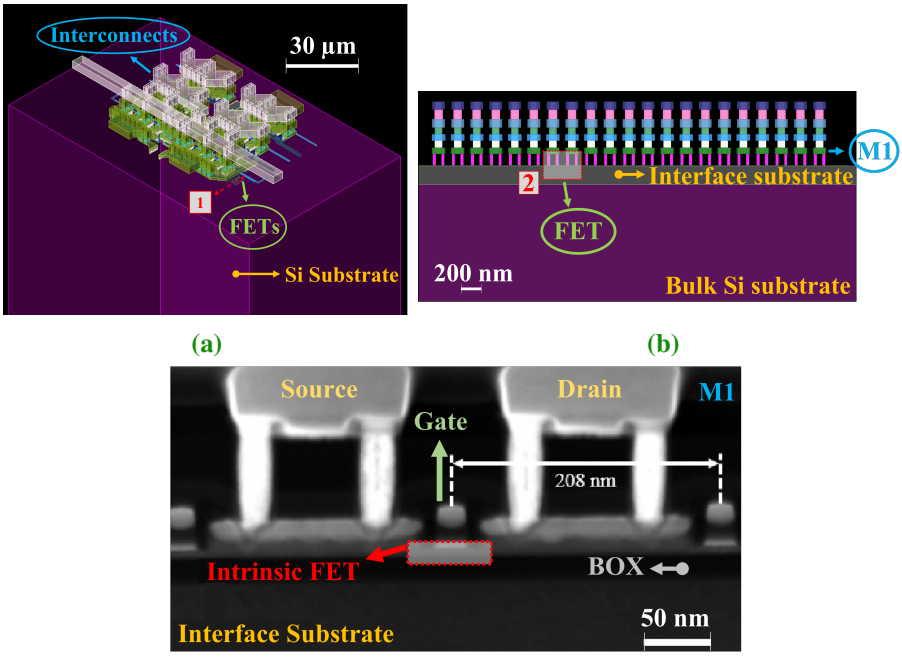


Figure 1.4: 3D view of a CMOS mm-wave integrated circuit and scale.

The IC lies on top of a substrate (silicon for CMOS technologies). Beyond offering a mechanical support, the substrate's physical properties can have a strong impact on the overlying circuitry behavior, particularly at RF and mm-wave frequencies. It does so by affecting the constituting elements of the IC: its active and passive devices.

At high frequencies, the thin dielectric layers isolating the metal interconnects and transistors from the substrate have a low impedance by their capacitive nature, resulting in a larger portion of the electric field propagating into the substrate. The relative strength of the substrate properties on the device depends on the device dimensions and how much the propagating signal senses the substrate, in other words to what extent the electromagnetic (-)EM) field propagates inside the substrate. Substrate effect can be detrimental to an IC as

it usually induces losses, non-linearity and increases the complexity of parasitic coupling modeling.



(c) From [20].

Figure 1.5: (a) Active region and high-level interconnects of the mm-wave IC from **Figure 1.4**. (b) Lower interconnects level of multi-finger FET. (c) Scanning Electron Microscope picture of intrinsic FD-SOI FET with immediate surrounding [20]. The 'interface substrate" (within a few µm from the Si-BOX interface) usually differs significantly from the bulk Si substrate, as it may contain STI, back-gate doping implants, etc.

Close-up views of the IC are shown in **Figure 1.5** to **Figure 1.6**, along with typical dimensions for selected passive and active devices. As clearly evidenced by the scale dimensions, *passive devices and interconnects dominate the overall IC area and are more sensitive to the substrate properties* due to the large dimensions being involved. Whereas, advanced active devices -in particular the intrinsic 22 nm FD-SOI MOSFET shown in **Figure 1.5c**- is tremendously smaller. So, *the substrate will only have second-order effects on*

the transistor's behavior (low-frequency drain-to-source coupling, self-heating, etc. see **Chapter 4**).

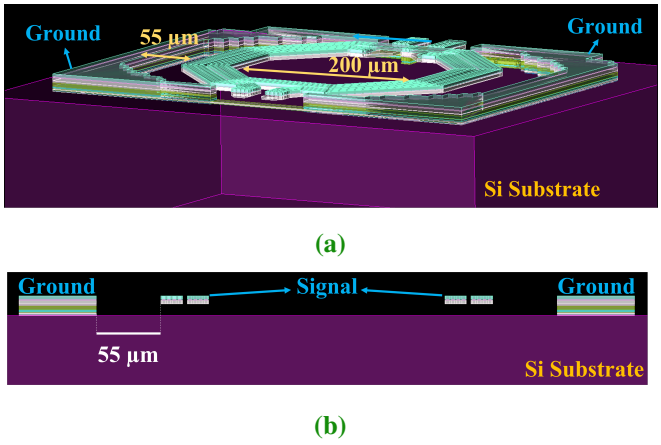


Figure 1.6: Close-up view of transformer passive device from the mm-wave IC shown in **Figure 1.4** (a) and its cross-section (b).

1.2.1 IC design with substrate

Having in mind what has just been mentioned, it is important to include the substrate considerations within the IC design flow, at least to some extent. In common design approaches, the substrate is either shielded (to prevent its influence on the designed circuit[2]), or its impact is included in the IC design via electromagnetic simulations of passives and interconnects using an EM stack provided in the technology's process design kit (PDK). This EM stack usually contains a substrate defined as a homogeneous layer with fixed permittivity and resistivity values.

However, as explained above, the substrate in an IC is not a homogeneous block, as it often contains regions of different resistivities (usually close to the silicon-oxide interface: see 'Interface substrate' label in **Figure 1.5b** to **Figure 1.5c**), e.g. PSC effect in HR substrate, a TR layer or p-doped and n-doped regions used to define the back-gate terminals, etc.

[2]This approach is usually limited above $\sim 10-20\,\text{GHz}$, as it consists of using a metal shield in the bottommost metal layers, which considerably increases capacitive parasitics that become too limiting for very high-frequency designs.

While the common design approach enables the design of ICs with a sufficient level of accuracy (in terms of substrate impact), it only provides a rough approximation of substrate effects[3] (such as inter-device coupling, substrate-induced non-linearity and losses) for two reasons.

First, the constant value of resistivity (of the single-layer-homogeneous substrate in the EM stack) is usually either extracted from dc four point probe measurements, or from sub-10 GHz effective resistivity measurements. Beside the obvious reason the dc four point probe measurements technique is not suited to evaluate the actual effective resistivity sensed by ICs[4], using a constant-valued effective resistivity at higher frequencies (extracted from low-frequency measurements) can be problematic too as explained in a subsequent sub-section.

Second, the substrate's vertical local resistivity profile is hardly constant. Indeed, representative vertical local resistivity profiles -that include interface effects- of three different substrates (std, HR and TR substrates) are shown in **Figure 1.7a**. Clearly, it is not realistic to model substrate coupling of any layout (that can take a wide range of dimensions) on a HR substrate by a simple homogeneous substrate layer with fixed resistivity value. Instead, a more accurate EM stack definition (valid for a wide variety of layouts) that could be used in EM simulators is illustrated in **Figure 1.7b** for a HR substrate including the PSC effect **[21]**.

In general, *usual methods do not achieve high substrate model accuracy*, such that we must go beyond conventional models as extensively investigated in **[21]**, which, in turn, *requires extensive substrate characterization*.

The common ground to all aforementioned substrate impact analyses is on-wafer measurement toward device and substrate characterization for accurate modeling and a better understanding of physical mechanisms behavior. As most effects to be studied here are of second order, they are usually complex to accurately evaluate, and some of them are very sensitive to the measurement procedure. It has set several characterization challenges that have been overcome in this thesis throughout its chapters. The encountered challenges and how they have been addressed are further detailed in the following.

[3] Since these substrate effects are not limiting the design of high-performance RF circuits (in most cases), they can be considered as second-order effects.

[4] dc four point probe measurements are performed on the Si substrate surface *after* removing all layers on top, including metal lines and dielectric layers (the BOX as well). While this method can determine the resistivity due to contamination or voluntary doping, it does not include field effects originating in materials on top of the Si, e.g. the PSC effect. This method is therefore not suited to evaluate the substrate impact on actual integrated devices.

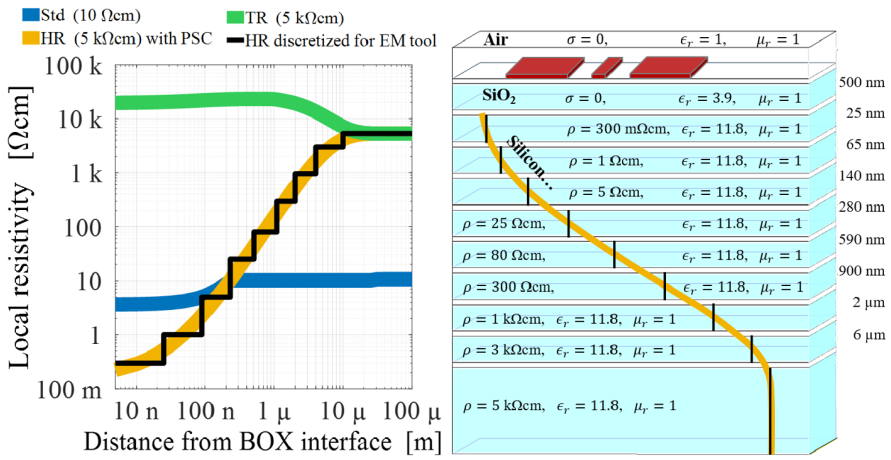


Figure 1.7: (a) Representative vertical resistivity profiles in the semiconductor volume beneath the BOX layer for the three SOI substrates. An example of profile discretization is shown for the case of the HR substrate. (b) Example of material stack definition for EM solver tools to capture the non-uniformity of an N-type HR substrate suffering from the PSC effect. From **[21]**.

1.2.2 Requirements on the effective resistivity evaluation

Substrate characterization usually involves evaluation of small-signal substrate losses (via on-wafer measurements of CPW lines) that are expressed with the effective resistivity figure of merit **[22]** (described in **Chapter 3**). This effective resistivity FoM is also often correlated to the substrate non-linear performance for most substrates. It is thus a common FoM used to evaluate the RF quality of substrates.

Existing commercial SOI substrates can feature very high resistivity values: up to a few tens of kΩcm. Currently, such high values of effective resistivity can be extracted, but their extraction is limited to a few GHz as the extracted values usually deviate from their expected trends at higher frequencies. So, the substrate effective resistivity behavior is generally extrapolated and assumed constant at higher frequencies as mentioned above.

In parallel, new substrate solutions are under development for improved performance or to anticipate the needs of future applications. For instance, existing commercialized solutions of high RF quality substrate (such as the

trap-rich) are not trivially applied to the industrial FD-SOI process. So, new approaches for increasing the substrate resistivity compatible with the FD-SOI process flow have to be considered. The monitoring of new low-loss substrate solutions development requires to extend the current extraction frequency range. Indeed, a wide variety of substrates must be characterized to that end, some of which with (intended or not) non-homogeneities giving rise to frequency-dependent effective resistivity.

To illustrate the related challenges of physical substrate loss mechanism characterization, let us consider a CPW line with a standard geometry regularly used for substrate effective resistivity extraction (see **Chapter 3**) that suffers from conductive and dielectric substrate losses. A sketch of the line is shown in **Figure 1.8a**. The contribution of metallic losses, conductive substrate losses (described by an equivalent resistivity) and dielectric substrate losses with frequency are shown in **Figure 1.8b** for different values of conductive and dielectric losses[5].

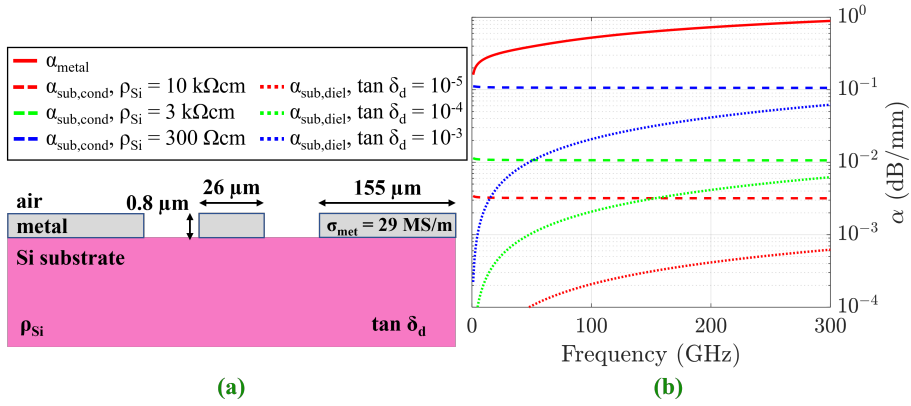


Figure 1.8: CPW line cross-section (a) and propagation line losses (α) contribution from metallic losses (solid line), conductive-only (dashed lines) and dielectric-only (dotted lines) substrate losses.

We first observe that, in all shown cases, substrate losses are (very) small compared to metallic losses, and they are therefore clearly second-order effects that we try to characterize (which is very sensitive as it will be shown

[5] Silicon dielectric loss tangent at RF, mm-wave and sub-THz frequencies is of 1.2×10^{-5} [23].

below). Second, for all shown values of dielectric loss, its effect becomes only significant at very high frequencies (and when a very low amount of conductive substrate losses is present), such that high-frequency measurement are required to reliably characterize this effect (or any frequency-dependent substrate loss mechanism with a similar intensity).

Therefore, the RF electrical performance via the effective resistivity FoM of such innovative substrates, as well as commercially available substrates, has to be assessed. *It is crucial to extend the effective resistivity extraction to very high frequencies* for both (i) understanding frequency-dependent substrate loss mechanisms of new substrate solutions under development and (ii) evaluating the performance of commercial SOI substrates at mm-wave frequencies, where an increasing number of applications are taking place nowadays (e.g. FR2 5G 24, 28 and 39 GHz mm-wave bands, 77 GHz radar applications, etc.).

However, the measurement accuracy degrades with higher frequencies. The substrate losses (and effective resistivity parameter) extraction is particularly sensitive to the correct evaluation of the transmission line characteristic impedance, which is directly related to the calibration reference impedance. As we shall see in the following chapters, many factors have a detrimental effect on the measurement accuracy and on the correct definition of the calibration reference impedance, including how the calibration procedure is performed, which is strongly user dependent. For illustration, **Figure 1.9** shows the effect of a common calibration errors in the evaluation of metallic and substrate losses of the CPW line shown in **Figure 1.8a**. The error induces meaningless extraction at higher frequencies, such as negative substrate losses (blue dahsed line) and decreasing metallic losses with frequency (green solid line).

To summarize, a strong need for very high-frequency (up to ~ 100 GHz and soon beyond) substrate loss characterization exists. However, the *current extraction procedure accuracy is limited and prevents a reliable characterization of low-loss substrates* (in the kΩcm range) *above 5 GHz*.

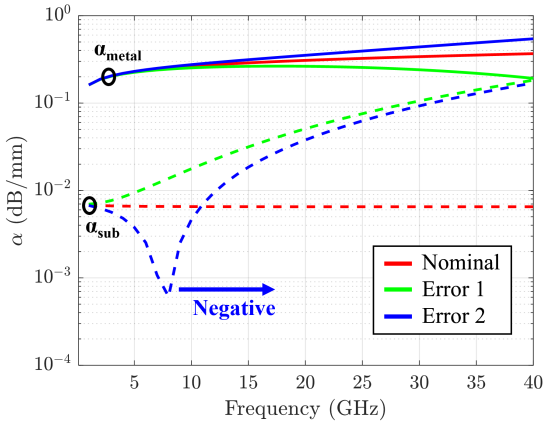


Figure 1.9: Propagation losses of the CPW line described in **Figure 1.8a** (with $\rho_{Si} = 5\,\mathrm{k\Omega\,cm}$ and $\tan\delta_d = 1 \times 10^{-5}$), contribution from metallic losses (solid line) and substrate losses (dashed lines). Nominal values (red), errors due to calibration (green and blue).

1.3 Objectives

In light with the present context of high-frequency applications, SOI technology is a prominent candidate answering the demands of massive deployment of RF electronic products. As we mentioned above, both PD-SOI and FD-SOI current technologies exhibit great performance in the mm-wave domain. Nevertheless, *FD-SOI, which has a good potential for further technology improvement via substrate enhancement (currently std resistivity), downscaling and channel strain engineering*, coupled with extra advantages of low power, back-gate contact and higher integration density (for more complex digital circuitry), is best positioned to meet the next challenges posed by current and future communication systems.

So, *this thesis studies FD-SOI performance for mm-wave applications, and, in particular, how it could benefit from a substrate of better RF quality.* This scientific question is the main driving theme of this thesis. Nevertheless, as discussed above, a thorough answer to this question requires studying the substrate impact at the different levels of the integrated circuit: substrate, front-end-of-line (FEOL, MOSFET), backend-of-line (BEOL) and circuit.

Therefore, a systemic approach is adopted in this thesis by working

(i) *on measurement aspects*: to improve on-wafer high-frequency measure-

ment accuracy;

(ii) *on substrate characterization*: to monitor new substrate solutions and model well second-order effects related to the substrate;

(iii) *on MOSFET characterization*: to characterize concurrent substrate and self-heating effects, as well as to verify current PDK model accuracy;

(iv) *on passives*: design (for circuits) and characterization (including the substrate impact);

(v) *on active circuits design*: to analyze the substrate impact on circuit-level and system-level figures of merit.

This thesis has been written with the purpose of studying each aspect described above in distinct chapters that can be read independently from each other. So, the interested reader can find all relevant information on a specific topic within the associated chapter. To ease the reader' search of the relevant chapter, an executive summary is provided in **Section 1.5**. It contains concise information on the covered topic, associated scientific questions and challenges, and it summarizes the novelties developed in this thesis and key results, for each chapter.

1.4 Thesis Structure

This thesis performs a detailed study about the substrate impact on FD-SOI technology as follows.

First, **Chapter 2** provides a brief overview of on-wafer S-parameter measurements and calibration techniques, with a special focus on transmission-line-based techniques. It further studies the main uncertainties and errors of common on-wafer calibration methods, and how they propagate to the characterization of the device under test (dut) through the reference impedance.

Then, **Chapter 3** focuses on the challenges associated to accurate low level of substrate loss characterization. Building on the theoretical background and uncertainty in calibration reference impedance covered in **Chapter 2**, the chapter proposes several solutions to extract meaningful substrate loss parameters based on CPW line measurements. Then, it evaluates residual errors in substrate loss extraction with the proposed approaches.

Next, **Chapter 4** provides an accurate ultra-wideband characterization of FD-SOI MOSFET from 100 kHz to 110 GHz and compares it to the process design kit compact model. The first part deals with challenges associated to MOSFET parameter extraction at mm-wave frequencies. The second part

proposes a method to separately characterize self-heating effect and substrate effect (source to drain coupling via the substrate) for FD-SOI MOSFETs in an unambiguous way.

Chapter 5 focuses on two key RF integrated circuits (RFICs) in a mm-wave front-end module: the low-noise and power amplifiers. Their design in the advanced 22 nm FD-SOI technology is first presented, then their performance are assessed and benchmarked to the state of the art.

Finally, **Chapter 6** analyzes via measurements and simulations the improvements an industrial FD-SOI technology can benefit from a better quality RF substrate. The first part demonstrates via experimental results how substrate losses in the 22 nm FD-SOI technology can be substantially reduced with a recently developed technique that is particularly suited to FD-SOI technology. Then, the second part studies the expected improvements in the designed circuits from **Chapter 5**. Since these circuits have not been fabricated on a high-resistivity substrate, simulations are used to quantify the substrate impact on the circuits, in particular via the quality factor improvement of key passive elements.

Ultimately, **Chapter 7** reviews the global conclusions of this thesis and proposes further research in line with the presented work.

1.5 Executive Summary

This thesis studies the *substrate impact on FD-SOI technology at mm-wave frequencies, and how it could benefit from low-loss substrates*. Since the substrate affects differently the constituting elements of integrated circuits, this thesis adopts a systemic approach by first studying each element separately, then using the accumulated knowledge to address the substrate impact question at the mm-wave IC level. As substrate effects are often of second-order, their characterization is quite sensitive, and they have generated most of the characterization challenges presented in this thesis.

Due to the wide variety of topics covered in this thesis, we have decided to write each chapter in such a way that the reader interested in a particular topic can find most of the information by reading the appropriate chapter. Thus, *this executive summary has the purposes* of (i) giving a clear summary of the *scientific subjects, motivation and challenges* tackled by each chapter and (ii) presenting the *key results* and *novelties*[6].

1.5.1 Chapter 2

1. Topic

Chapter 2 deals with general on-wafer S-parameters measurement aspects at mm-wave frequencies.

2. Motivation

The effective resistivity figure of merit used for substrate losses characterization is very sensitive to the reference impedance (Z_{ref}) of the calibration.

3. Challenges

The challenges consist of evaluating the reference impedance of on-wafer calibrations and of identifying a procedure or strategy to perform accurate calibration with well-defined reference impedance.

4. Novelties

We apply the existing calibration comparison technique in a new way: to evaluate the reference impedance of different on-wafer calibrations. The novelty mainly consist of the assessment of Z_{ref} of SOLT and LRRM calibrations, benchmarked to the mTRL calibration.

5. Key outcomes

We identify that SOLT and LRRM calibrations, when properly performed, feature a reference impedance very close to mTRL up to $\sim 40-50\,\text{GHz}$. However,

[6] To the best of our knowledge.

both LRRM and SOLT are very sensitive to probe misplacement on Load and Thru standards.

Although Z_{ref} from mTRL also suffers from systematic errors, mTRL calibration is more robust and is identified as the reference calibration method providing a reliable Z_{ref}. A custom-made calibration substrate is presented, for systematic error reduction in Z_{ref} mTRL up to 90 GHz at least.

1.5.2 Chapter 3

1. Topic

Chapter 3 tackles the small-signal substrate losses characterization via the effective resistivity (ρ_{eff}) figure of merit, at RF and mm-wave frequencies.

2. Motivation

Effective resistivity extraction at mm-wave frequencies is crucial (i) to monitor the development of new low-loss substrate solutions and (ii) for substrate loss characterization of new and existing commercial SOI substrates targeting accurate modeling of second-order substrate effects.

3. Challenges

Prior to this work, the extraction procedure accuracy was limited and prevented a reliable characterization of low-loss substrates (in the kΩcm) above 5 GHz.

4. Novelties

We show for the first time how an error during the calibration procedure leads to a wrong effective resistivity extraction above a few GHz. We introduce the *R-based* method to compensate for potential $\mathrm{Im}(Z_c)$ misestimation.

5. Key outcomes

The *R-based* method is demonstrated to be robust to significant calibration error and work well for moderately to strongly conductive substrate. However, it is not suited to low- or very low-loss substrates, as it introduces a systematic error.

The direct substrate loss extraction procedure applied to lower frequency measurements (up to $\sim 10-15$ GHz) has shown that conductive losses are still the dominant substrate loss mechanism in the frequency range of extraction, and the dielectric loss tangent is below 1×10^{-4} for the commercial eSI90$^{\text{TM}}$ substrate.

The identification of a reference calibration procedure in **Chapter 2** has improved the frequency range for reliable effective resistivity extraction up to $\sim 10-15$ GHz in case of very low-loss Si substrate (with $\rho_{eff} > 10$ kΩcm). Residual ripple error is now the main factor limiting the effective resistivity extraction at higher frequencies, and its impact is quantified in extracted ρ_{eff}

up to 110 GHz for substrates of different resistivities.

1.5.3 Chapter 4

1. Topic

Chapter 4 focuses on FD-SOI MOSFET small-signal characterization. The first part deals with high-frequency (up to 110 GHz) measurements and correction, while the second part is dedicated to the low-frequency (100 kHz – 10 GHz) substrate and self-heating effects.

2. Motivation

Transistors are at the basis of integrated active circuits. Their characterization is thus essential (i) for verification of existing models (available in the PDK) at the design frequencies (mm-wave) and (ii) to analyze the impact of substrate on the FET behavior.

3. Challenges

Due to several factors degrading the accuracy of common calibration and de-embedding approaches above a few tens of GHz, custom calibration kit designs integrated in the same chip as the transistors (i.e. 'in-situ') are essential. Even with such care, measurement accuracy is still degraded by residual probe-dependent errors in the mm-wave frequency range.

In UTBB FD-SOI MOSFETs, both the substrate effect (drain-to-source coupling via the back-gate and substrate networks) and dynamic self-heating effect induce a transition in the measured Y-parameters across similar frequency ranges, making it difficult to accurately characterize each effect.

4. Novelties

Concerning the high-frequency characterization, the existing Amakawa's method **[24]** for transmission line characteristic impedance (Z_c) characterization has been applied for the first time on in-situ Line standards toward MOSFET measurement correction.

Concerning the low-frequency characterization, we have suggested and shown for the first time that the zero-temperature coefficient (ZTC) bias can be used to characterize the substrate effect, then we have taken it into account for self-heating characterization at other biases.

We also show for the first time how the extracted complex thermal impedance might be used to characterize the rarely discussed heat capacity (at constant pressure) property of materials in the heat evacuation path from the transistor.

5. Key outcomes

A MOSFET is measured with different RF probes up to 110 GHz. The use of

Amakawa's method for in-situ Line standards Z_c characterization helps reducing probe-dependent residual errors. With the best calibration and de-embedding strategy, measured source-drain and gate resistances have frequency variations lower than 5 % and $\sim$ 20 %, respectively, up to 110 GHz for all tested probes. Measurements with different probes of extrinsic FET parameters at high RF performance bias feature almost overlapping curves up to 70 GHz, then little deviation ($\sim<$ 5 %) up to 110 GHz for capacitances, transconductance and cutoff frequency parameters.

The new self-heating characterization procedure (that includes the substrate effect) is demonstrated to (i) enable the thermal resistance (R_{th}) extraction at low power and (ii) significantly improve the accuracy of the extracted R_{th}. The new method yields an error below 20 % at low power and $<$ 10 % at moderate and high power, against up to $\sim$ 60 % error in R_{th} at low and moderate power levels when the substrate effect is neglected.

The PDK compact model of the tested MOSFET has a great agreement with measurements in the mm-wave frequency range. However it does not model well some second-order effects such as the low-frequency substrate and dynamic self-heating effects, which have a negligible impact on the MOSFET behavior at mm-wave frequencies.

1.5.4 Chapter 5

1. Topic

Chapter 5 focuses on the design of two integrated circuits at mm-wave frequencies in the 22 nm FD-SOI technology: the low-noise amplifier (LNA) and power amplifier (PA).

2. Motivation

The LNA and PA are two essential building blocks of practically any transceiver. For a pertinent analysis of the substrate impact at circuit level and subsequently on system-level figures of merit, it is important to perform this analysis on circuits at the state of the art.

3. Challenges

Integrated circuit design at mm-wave frequencies is not straightforward and requires accurate (active and passive) device models, as well as a sound design procedure to include all parasitics.

4. Novelties

The systematic analysis of back-gate bias static modulation on the designed circuits is the main originality of the chapter. For the LNA, we show that the

circuit can change its mode of operation and trade-off dissipated power for power linearity, noise and gain. For the PA, the back-gate bias can be used to trade-off AM-AM for AM-PM distortion. It is also shown for the first time via simulations and measurements of 5G modulated signals the impact of back-gate bias modulation on the error vector magnitude (EVM).

5. Key outcomes

The presented circuits performances are in line with the state of the art, confirming the pertinence of using them to evaluate the substrate impact on circuit-level performance. The 39 GHz LNA achieves 2.5 dB noise figure with 19.9 dB gain and -5.3 dBm IIP3 for a 20.8 mW power consumption. Two PAs covering the 24-43 GHz frequency bands are designed in 22 nm FD-SOI technology. They achieve a saturated output power and peak PAE up to 18.6 dBm and 36.4 % for the first PA (PA1), and 20.1 dBm and 28.3 % for the second PA (PA2), respectively. Furthermore, PA1 is shown to perform with up to 9.2 dBm and 13 % mean output power and PAE, respectively, for a target EVM of 5.5 % under 5G NR modulated signal measurements.

1.5.5 Chapter 6

1. Topic

Chapter 6 studies via experimental results and simulations the technological improvements an industrial FD-SOI technology can benefit from a high-resistivity substrate.

2. Motivation

Current FD-SOI process is fabricated on silicon wafers with standard resistivity (std, around 10 Ω cm), which are known to entail significant losses, non-linearity and complex substrate coupling modeling. Improving the substrate RF quality on which the FD-SOI technology is fabricated is thus an interesting short-term technological improvement perspective.

3. Challenges

To facilitate the technology transition, a high RF quality substrate compatible with the FD-SOI process flow is required. The high-resistivity substrate is a natural candidate as it necessitates very little modification from the current fabrication steps, but the PSC effect is known to hinder the substrate-related improvements. So, an interface passivation solution compatible with the FD-SOI process is needed for the FD-SOI technology to benefit from low substrate losses.

4. Novelties

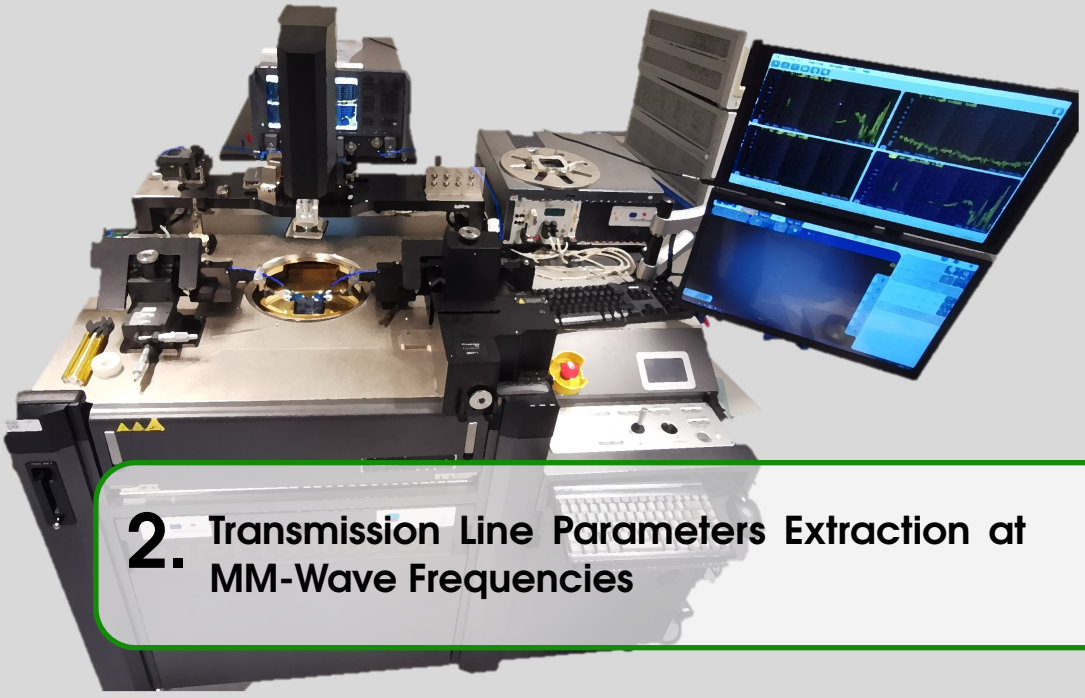
The *PN junctions interface passivation solution* recently developed by Rack et al. in **[19]** is applied for the first time to an industrial FD-SOI technology fabricated on high-resistivity substrates. The presented work from the PN junctions applied to the industrial FD-SOI technology results from a collaboration in which this thesis' author as well as some of his colleagues[7] have provided major contributions.

5. Key outcomes

In the best PN junctions deployment scenario, a substrate effective resistivity larger than 200 Ω cm up to 50 GHz is reported (at M1 level), which represents $>$ 30 times improvement with respect to the process of record (POR). CPW lines on thick metal layer demonstrate a 0.2 dB/mm reduction at 50 GHz in propagation losses compared to TFMS line design. Great reductions in substrate-induced non-linearity, substrate coupling and improvement of inductor quality factor (up to $\sim 60\,\%$) are also shown.

Negligible reduction in noise figure of the designed LNA is expected with a low-loss silicon substrate. Nevertheless, substantial performance improvements can be expected for the designed PAs: with saturated output power and peak efficiency increases of 0.5 dB and 4 % for PA1, and 0.8 dB and 5 % for PA2, respectively.

[7] An exhaustive list of contributors can be found in the list of authors from **[25–28]**.



2. Transmission Line Parameters Extraction at MM-Wave Frequencies

The tremendous growth in RF applications over the past two decades, enabled by technology downscaling and improvement of transistor RF performance, has required accurate on-wafer measurements as an essential tool for device characterization and process monitoring. With 5G and later 6G creating new applications at millimeter-wave (mm-wave) and sub-THz frequencies, accurate on-wafer characterization at such high frequencies become more challenging and require *'in-situ' calibration* **[29, 30]**, i.e. calibration within the same environment as the device, thus designing custom on-wafer calibration kits (calkits).

Indeed, in-situ calibration has the advantage of setting the measurement reference plane closer to the device under test (dut), in a wafer-probe environment similar to the situation when the dut is measured. More details concerning the advantages of in-situ calibration over the conventional 'probe-tip' calibration for accurate mm-wave frequency characterization are covered in **Chapter 4** and will not be discussed here.

It is however important to stress here that due to unknowns related to fabrication tolerances and user experience, the design of custom on-wafer calkits requires accurate characterization of its standards. Such standards are usually either (i) Short, Open, Load, Thru standards for lumped-standards-based calibration methods, or (ii) Short or Open, Thru, Line, potentially several ones of different lengths for (multiline) Thru-Reflect-Line (TRL) calibrations.

Beyond 110 GHz and, in general, above a few tens of GHz, TRL methods are either preferred and/or more accurate because they rely on distributed standards whose electrical properties need not to be known. On-wafer multiline TRL calibration has been successfully demonstrated for transistor characterization up to 750 GHz [31].

High-frequency device measurement is one crucial application that requires accurate transmission line characterization. Another type of application with similar requirements is the extraction of substrate electrical properties for SOI wafers [32, 33]. Indeed, as explained in Chapter 1, the parasitic surface conduction (PSC) is a surface effect affecting the Si substrate electronic properties up to a few µm in depth at most. This surface effect is sensed by ICs and its characterization is therefore crucial. Commonly used resonator-type methods to evaluate substrate permittivity and losses work on the whole substrate thickness, and they are thus not suited to capture surface effects. For instance, when applying this resonator technique to a high-resistivity (HR) wafer suffering from PSC, the surface conductive sheet would be averaged out by the thick, highly resistive bulk substrate and thereby appear to be negligible from the overall substrate loss measurement. Therefore, the most common method to characterize such SOI wafers is via on-wafer coplanar waveguide (CPW) line measurements [22, 34] that are designed such that they can sense the Si-oxide interface and any surface effect occurring there.

On-wafer, in-situ mTRL calibration and substrate electrical properties characterization are the main motivations for high accuracy transmission line parameters extraction at high frequency in this thesis. In this chapter, we review techniques for on-wafer transmission line characterization at mm-wave frequencies. First, transmission line parameters are briefly defined, and a glimpse of on-wafer S-parameter measurement procedure is provided. Then, the second part presents theoretical background for the extraction methods used to characterize on-wafer transmission lines: the multiline TRL and calibration comparison techniques. Finally, the last part discusses causes of systematic errors in transmission line parameter extraction and tries to remedy them.

2.1 Transmission Line Model

In general, a transmission line is represented as a two-wire line (signal and ground, cf. Figure 2.1a), described by two complex parameters, i.e. its char-

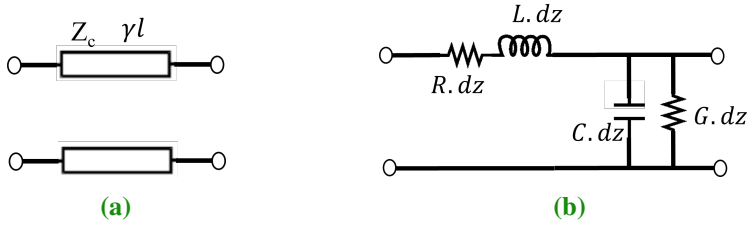


Figure 2.1: (a) Two-wire (signal and ground) transmission line model of length l. (b) Lumped-element equivalent circuit.

acteristic impedance (Z_c) and its propagation constant (γ)[1]. A piece of transmission line of infinitesimal length (dz) can be modeled as a lumped-element circuit, as shown in **Figure 2.1a**, described by R, L, G and C. They are defined as

1. R is the series resistance per unit length, for the signal and ground conductors, in Ω/m;
2. L is the series inductance per unit length, for the signal and ground conductors, in H/m;
3. G is the shunt conductance per unit length, in S/m;
4. C is the shunt capacitance per unit length, in F/m.

The well-known expressions to move from one representation (γ, Z_c) to the other ($RLGC$) are **[35, 36]**

$$Z_c = \sqrt{(j\omega L + R)/(j\omega C + G)}, \tag{2.1}$$

$$\gamma = \sqrt{(j\omega L + R)(j\omega C + G)}, \tag{2.2}$$

and

$$R = \mathrm{Re}\{\gamma Z_c\}, \tag{2.3}$$

$$L = \mathrm{Im}\{\gamma Z_c\}/\omega, \tag{2.4}$$

$$G = \mathrm{Re}\{\gamma/Z_c\}, \tag{2.5}$$

$$C = \mathrm{Im}\{\gamma/Z_c\}/\omega. \tag{2.6}$$

The propagation constant can also be written as

$$\gamma = \alpha + j\beta. \tag{2.7}$$

[1] Z_c and γ are well defined provided a single mode propagates through the transmission line.

where α and β are the transmission line losses per unit of length and electrical phase delay, respectively. β can be further defined either with the effective propagation velocity v_{eff} or the effective propagation wavelength λ_{eff}:

$$\beta = \frac{\omega}{v_{eff}} = \frac{2\pi}{\lambda_{eff}}. \tag{2.8}$$

Often an effective permittivity is also defined. For a wave propagating in a transverse electromagnetic (TEM) mode in a fictitious medium of permittivity $\varepsilon_{r,eff}\varepsilon_0$ and permeability μ_0, the effective permittivity is defined as

$$\varepsilon_{r,eff} = -\left(\frac{c_0\gamma}{\omega}\right)^2, \tag{2.9}$$

where c_0 is the speed of light in vacuum. $\varepsilon_{r,eff}$ is a useful quantity mostly used in the mTRL algorithm [37].

In practice, γ and Z_c are first extracted from measurements. The *RLGC* line elements are then extracted with **Equation 2.3-Equation 2.6** and are useful to assess the validity of the extraction, as they offer additional physical insight, complementary to γ and Z_c. Before explaining the extraction procedures for Z_c and γ, let us give an overview of on-wafer S-parameter measurements.

2.2 RF S-parameter Measurements and Calibration

2.2.1 S-parameter definition

The electrical behavior of linear n-port networks is usually described by its input and output impedance of admittance parameters (Z- and Y-parameters, respectively). These parameters are defined as ratios of input/output ports voltage and current, when one port is connected to a generator and the others are terminated by an open or short circuit. With increasing frequencies, the realization of ideal open and short terminations become more difficult. Furthermore, many types of devices (e.g. RF amplifiers) cannot be measured with a short-circuited output, as it may radically change the electrical behavior of the device (power amplifiers) and even break it.

Instead, another set of parameters are commonly used for high-frequency measurements: the *scattering* parameters, or *S*-parameters. They are defined as ratio of pseudo-waves, with one generator at one port and the others terminated by a specific load. S-parameters are significantly easier to measure at high frequencies. All these electrical descriptions (Z, Y, T, H, S, etc.) are equivalent and can be obtained from each other [35, 38].

For a general n-port, the a_i and b_i pseudo-waves are mathematical artifacts defined as [36]

$$a_i(Z_{ref,i}) = \left[\frac{|V_{0,i}|}{V_{0,i}} \frac{\sqrt{\mathrm{Re}(Z_{ref,i})}}{2|Z_{ref,i}|}\right](V_i + Z_{ref,i}I_i),$$
$$b_i(Z_{ref,i}) = \left[\frac{|V_{0,i}|}{V_{0,i}} \frac{\sqrt{\mathrm{Re}(Z_{ref,i})}}{2|Z_{ref,i}|}\right](V_i - Z_{ref,i}I_i),$$

where $Z_{ref,i}$, V_i, I_i are the port i reference impedance, voltage difference, flowing current, respectively. $V_{0,i}$ is a normalization constant [36]. The S-parameters are defined as ratios of pseudo-waves:

$$S_{ij} = \left.\frac{b_i}{a_j}\right|_{a_k=0, k\neq j}.$$

The above scattering parameter definition is actually called the *pseudo-scattering* parameters. We shall call them scattering parameters for brevity in this thesis. They are mathematical artifacts as defined in [36] that are actually measured using conventional calibration techniques implemented in most vector network analyzers. There are several definitions of these so-called 'waves' labeled 'a' and 'b' that are not or less convenient to on-wafer measurements[2].

[2]The pseudo-waves are in general linear combinations of the forward and backward waves also defined in [36]. These forward and backward waves are related to electromagnetic waves propagating in a transmission line with characteristic impedance Z_c. The pseudo-waves are proportional to the forward and backward waves only for the specific case in which $Z_{ref} = Z_c$. Since Z_c can greatly vary with frequency as we will see in the following of this thesis, the pseudo-waves are more convenient as it allows the use of a constant Z_{ref}, which simplifies the interpretation of measurements.

Another popular definition of waves is the power waves defined by Kurokawa [39], with its reference impedance $\widetilde{Z}$. When $\widetilde{Z}$ is real, the power waves reduce to pseudo-waves (except for a phase factor) with reference impedance $Z_{ref} = \widetilde{Z}$. However, this power waves definition is not practical for measurements interpretation or circuit design when the reference impedance $\widetilde{Z}$ is not purely real, as it is commonly the case in on-wafer calibrations (see Section 2.5). Indeed, for instance the Smith chart tool cannot be directly applied to this definition of power waves, as the reflection coefficient (in the power waves formalism) of an arbitrary load impedance Z_{load} depends on the normalized $Z_{load}/\widetilde{Z}$ *and* on the phase of $\widetilde{Z}$ [36], instead of solely on the normalized Z_{load}/Z_{ref} as it is the case for the pseudo-waves formalism.

2.2.2 S-parameter measurements - the vector network analyzer

Nowadays, practically all linear high-frequency measurements are carried out with a vector network analyzer (VNA). The basic measurement concept implemented in modern VNAs for a two-port network is shown in **Figure 2.2**.

An internal source is switched between port 1 and 2 to generate the incident wave, the other port being terminated by a load at a certain impedance (defining the system reference impedance, Z_{ref}, usually 50 Ω). Each power wave is measured via reflectometers (matched directional couplers). The source and load switching is operated with an internal switch, so, the device can be automatically measured in both forward (a_1) and reverse (a_2) directions without reconnecting.

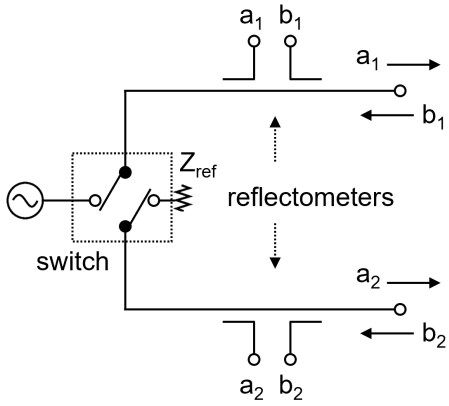


Figure 2.2: Basic high-frequency measurement concept with modern VNA.

2.2.3 On-wafer S-parameters measurements - need for calibration

A typical on-wafer S-parameters measurement setup is shown in **Figure 2.3a**. We see the VNA enabling S-parameter measurements, cables connecting the VNA to RF probes. RF probes (with examples shown in **Figure 2.3b**) enabling on-wafer measurements of structures whose dimensions are in the order of magnitude of 100 µm, on a probe station.

As observed from **Figure 2.3a**, calibrating RF measurements is crucial, already at a few hundreds of MHz, as the wavelength of the test signal is of several orders of magnitude smaller than the cables and probes length. The RF calibration objective is to remove systematic errors coming from any accessories

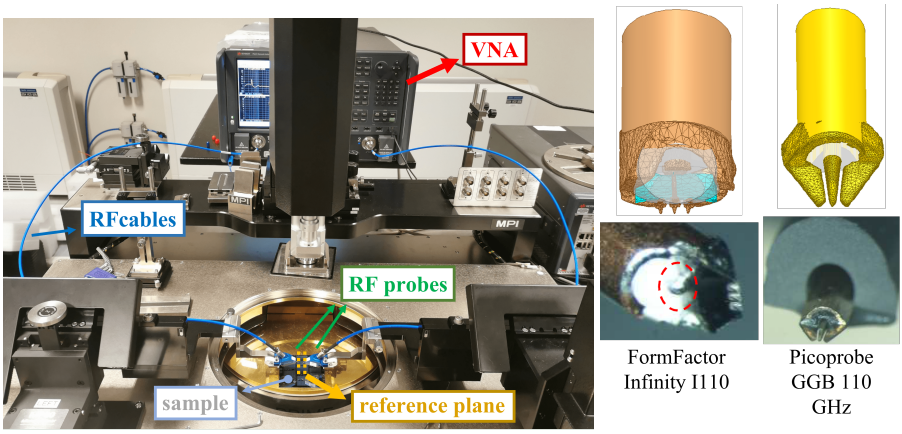


Figure 2.3: Left (a): example of on-wafer RF measurement setup. Measurement reference plane after calibration shown in orange, dashed lines. Right (b): Example of 100 µm-pitch RF probes: 3D model (top) **[40]** and picture (bottom) **[41]**.

(enabling the RF measurement) in the measurement signal path, to measure only the dut electrical behavior. In the setup shown in **Figure 2.3a**, the RF calibration corrects the impact of cables, RF probes and imperfections in the VNA, and it sets the measurement reference plane in the vicinity of the dut (see orange dotted lines in **Figure 2.3a** and in a magnified view in **Figure 2.4**).

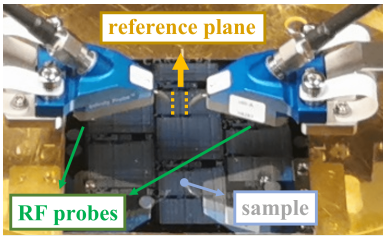


Figure 2.4: Magnified view of **Figure 2.3a**, with measurement reference plane after RF calibration.

2.2.4 On-wafer calibration

There exist many on-wafer calibration algorithms. For two-port measurements, the most common algorithms are Short-Open-Load-Thru (SOLT), Line-Reflect-Match (LRM), Thru-Reflect-Line (TRL) and their variations. There exist other calibration techniques for 2-port measurements, but they will not be mentioned here, as only SOLT, LRM-type and TRL calibrations will be used in this thesis. A detailed synthesis on VNA calibration methods and error box models can be found in [42–44].

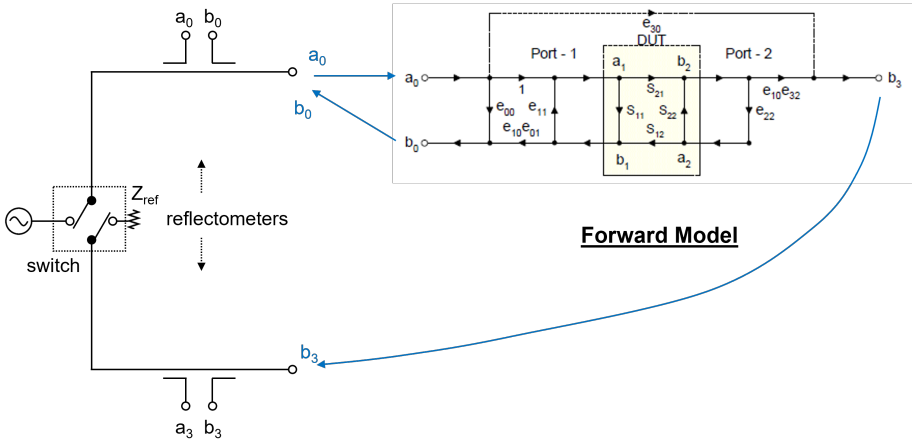
The SOLT calibration relies on a 12-term error box model shown in Figure 2.5, with 6 terms for forward measurement and 6 other terms for reverse measurement. It relies on the measurement of 4 perfectly known standards (Short, Open, Load and Thru standards, hence its name). It is the most commonly used method for RF calibration. However, its accuracy critically depends on fabrication and modeling tolerances of the standards, as they must be fully known. In on-wafer measurements, these standards electrical behavior usually deviates from their specified model at high frequencies[3], such that the accuracy of SOLT calibration degrades with increasing frequencies unless an accurate characterization is previously realized.

Other methods, called self-calibration methods, do not require all standards to be fully known. It is the case of LRM and TRL types of methods, firstly introduced in [48] and [49], respectively. They use redundancy of measurement results and an 8-term error box model to determine the missing standard information and calibrate the setup. The 8-term model is usually represented as two 2-port-network error boxes (thus, each with 4 error terms) and uses the transfer-matrix representation (defined in Section 2.3) instead of S-parameters, as shown in Figure 2.6. However, *only 7 error terms are needed to calibrate the measurement* [50].

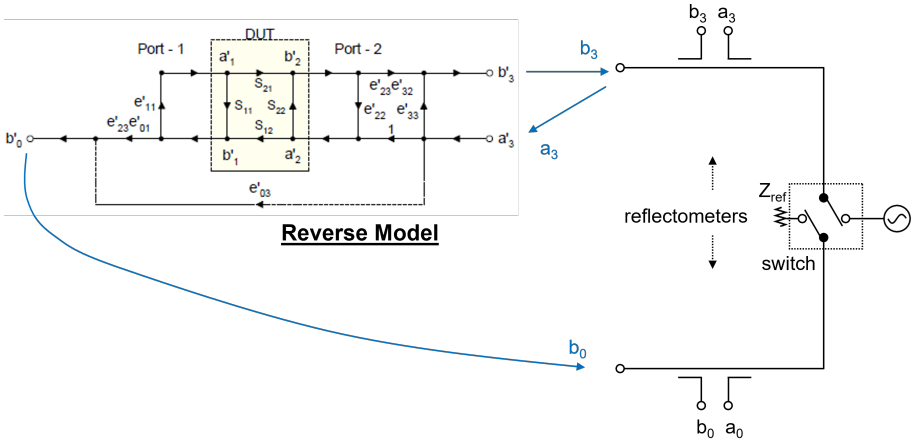
Despite using an error model with fewer terms, self-calibration methods are preferred for high-frequency on-wafer measurement calibration as they need fewer known parameters and provide more accurate measurements than the SOLT calibration in case some parameters are not well determined.

Before providing more details about the two main self-calibration methods: LRM and TRL, let us discuss more about the different error box representations.

[3] Indeed, varying the contact position on the standard already modifies the high-frequency electrical response of the measured standard, thus degrades the accuracy of SOLT if it is not accounted for. This has been demonstrated in [45–47], and it will be further shown for LRRM in Section 2.5.2.



(a) Forward model.



(b) Reverse model.

Figure 2.5: 12-terms error box model. Images from **[43, 44]**.

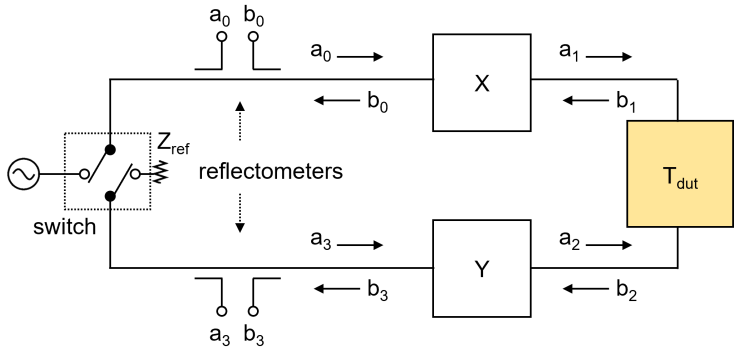


Figure 2.6: 8-term error box model.

12- and 8-term error box models

Several approaches have been published to move from one error box representation (12-term) to the other (8-term) [44, 51]. There are mainly two differences, (i) two terms accounting for non-ideal internal VNA switch and consequently a change in port match, (ii) two remaining terms that account for some leakage between ports, in the 12-term error box model.

The two terms accounting for non-ideal internal switch, the so-called *switch terms* or *switching terms*, can be added to the 8-term model with additional measurements [51]. In practice, it is usually applied to first-tier calibrations, even when using TRL and LRM-like methods.

The two remaining terms from the 12-term model are often called leakage terms, as they describe signal leakage from one port to another when they are perfectly matched, i.e. when the dut is perfectly matched to the system impedance. The 8-term model considers that these leakage terms are zero. Nevertheless, only two terms to describe leakage is not sufficient. Therefore, a 16-term error box has been introduced to account for all possible leakages in modern VNA [52].

The use of 16-term error box in on-wafer measurements remains scarce, because it needs a larger number of standards and, more importantly, because the probe-wafer environment changes (from one substrate to another, different probe to probe distance, probe coupling to neighbor devices that change from standard to standard, etc.), and so does the error terms, therefore reducing the accuracy of the 16-term model correction. Nevertheless, the 16-term model is still used in practice for on-wafer calibration by some commercial softwares

(WinCal XE), because of the simple correction algorithm that corrects measurements by solving a linear matrix equation [38, 53]. In this case, after solving the 8-term model from standards measurements, the model is simply augmented to the 16-term model by assuming all leakage terms are zero. Otherwise, in a 8-term error model, equations to correct measurements are developed in [50, 54].

LRM- and TRL-type calibrations

The TRL method uses the measurement of a Thru (or short Line), a Reflect and a Line (or long Line) standards. The transmission line propagation constant and the Reflect standard reflection coefficient are unknown parameters determined during calibration process. The TRL technique enables the use of well-defined transmission line standards that, in turn, enable calibration and measurement traceability.

A strong disadvantage of TRL is that it is frequency limited. This restriction is overcome with the measurement of additional Line standards of different lengths, with the so-called multiline (m)TRL method [55]. This mTRL method uses the redundant measurement information (from multiple Line standards) and applies a statistical analysis to improve the measurement accuracy and broaden the frequency range of validity. Finally, the traceability and very high measurement accuracy achieved without the need of prior standards characterization make mTRL the benchmark method for on-wafer measurements.

The LRM type of methods use two one-port Match (or Load) standards. Initially designed to overcome the frequency limitation of TRL method [48], it has significantly evolved with different variations: LRRM [56, 57], LRM+ [58], and TMRR [47]. The Reflect standard(s) reflection coefficient is unknown and is determined during the calibration process. The Thru and Load standards must be known. Although these methods are in general sensitive to probe misplacement on standards [45, 47] and/or asymmetry in port-1/port 2 Load standards [42], if well performed, it has been demonstrated to reach the same accuracy level as mTRL up to 110 GHz [58].

LRM-type methods have the strong advantage of measuring standards with the same probe-to-probe distance. It is thus much faster to perform and is regularly used for calibration on commercial calibration substrates. However, it is more complex to implement the LRM techniques on custom-made calkits because of the Load standard. Indeed, as its electrical behavior must be fully known over the whole measurement frequency range, it needs to be fully characterized (for instance with a benchmark mTRL calibration), which is time

consuming. Furthermore, to avoid repeating this characterization process each time, we need a highly repeatable process. Even though a highly repeated process might be accessible in industrial technologies[4], it cannot be achieved in our facilities.

Because of (i) the high accuracy level achieved with mTRL, which is also (ii) less sensitive to probe misplacement than LRM-type methods and (iii) does not require a hard-to-manufacture Load standard, the mTRL calibration procedure will be explained in the next section and will be widely used in this thesis.

Let us summarize this rather theoretical section by insisting in the main points that will be used or assumed to be known in the following.

- Calibration is absolutely necessary for on-wafer measurements. Calibration needs measurements of a set of standards.
- Self-calibration methods, in particular TRL-type, generally provide better accuracy at high frequencies, because they suffer less (or not) from inaccurate modeling of the standards.
- LRM and TRL types of calibration use an 8-term error model (of which *only 7 parameters are needed to correct the measurements*) that neglects leakage between ports and internal switch error. Equations to correct measurements based on the 8-term error model can be found in **[50]**.
- The switching terms accounting for non-idealities of internal VNA switch can be measured (usually during the Thru standard measurement) and corrected prior to the 8-term error box correction, with equations provided in **[51]**.

[4] Even Load standards dc resistance and Thru standard characteristic impedance from commercial calibration substrates can vary from 50 Ω. Indeed, not all Load standards are certified 50 Ω in FormFactor 101-190C and 104-783A substrates: their dc resistance is first measured and a map *specific for each product item* indicates 'precision' Loads for which an accuracy of ±0.3 % is guaranteed.

2.3 The Multiline TRL Calibration

The multiline TRL method has first been introduced in [55]. Even though different variations exist [59–61], which differ in the statistical technique used to deal with the redundant Line data, we will describe the original method [55], also explained in details in [37], that is widely used and yields excellent results, marginally improved by its variations.

As mentioned above, the mTRL calibration technique uses measurements of a Thru, a Reflect and Line standards of different lengths. It is based on an 8-term error box model, which is expressed as two 2-port networks that are more conveniently described with the transfer-matrix representation: T_A and T_B (defined in **Equation 2.10**).

In this section, we will briefly present the mTRL algorithm described in [55] that extracts the transmission line propagation constant and 4 out of the 7 required error terms. The goal in this section is not to fully describe the calibration method, but it is to provide a glimpse of the mTRL algorithm, necessary to understand its limitations and the sensitivity of extracted parameters. Readers interested in the full calibration procedure are invited to read [37] that has been published to that end. As this section is rather theoretical and contains several mathematical developments, a few green boxes are included at the end of some sub-sections to help the reader not lose track of important information.

2.3.1 Formalism of measurement conditions

The transfer matrix T of a two-port network is expressed in terms of the S-parameters as

$$T = \frac{1}{S_{21}} \begin{bmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{bmatrix}. \tag{2.10}$$

This definition of transfer matrix is such that the transfer matrix of a 2-port with transfer matrix A cascaded *to the left* of another 2-port with transfer matrix B is AB.

It is convenient to also introduce the reverse transfer matrix, denoted by an overbar:

$$\overline{T} = \widetilde{T^{-1}} \equiv \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} T^{-1} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} = \frac{1}{S_{12}} \begin{bmatrix} S_{21}S_{12} - S_{22}S_{11} & S_{22} \\ -S_{11} & 1 \end{bmatrix}, \tag{2.11}$$

which is equivalent to swapping indices 1 and 2 of **Equation 2.10**. A useful relationship to understand how some results are obtained from previous equations

is that

$$\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} = I.$$

The measured transfer matrix of standard i is M^i:

$$M^i = XT^i\overline{Y}, \tag{2.12}$$

where X and Y are the unknown transfer matrices of the left and right error boxes, respectively. T^i is the transfer matrix of the actual standard i. The overbar in $\overline{Y}$ simply reflects that Y is defined to cascade from *right to left*, as opposed to X. This choice in formulation takes advantage of the symmetry, such that equations leading to the determination of X are the same for Y with the simple exchange of port numbers 1 and 2.

In case of an ideal transmission line, perfectly matched (i.e. $Z_{ref,1} = Z_c = Z_{ref,2}$), T^i is equal to

$$L^i \equiv \begin{bmatrix} e^{-\gamma l_i} & 0 \\ 0 & e^{+\gamma l_i} \end{bmatrix} \equiv \begin{bmatrix} E_1^i & 0 \\ 0 & E_2^i \end{bmatrix}, \tag{2.13}$$

where γ is the propagation constant and l_i the length of Line standard i. In general, however, the standard is non-ideal, it is chosen to be represented by the following transfer matrix

$$T^i = (I + \delta^{1i})L^i\overline{(I + \delta^{2i})}, \tag{2.14}$$

where δ^{1i} and δ^{2i} are perturbation matrices representing imperfections, errors, associated to port 1 and 2, respectively. They are assumed to be small, such that any self- or cross-product will be neglected.

The important *take-away messages* in this sub-section are

- use of transfer and reverse transfer matrices to formulate the measurement conditions, with the unknown X and Y error boxes defined from left to right and right to left, respectively;
- the transfer matrix T^i of a non-ideal Line standard i is expressed (**Equation 2.14**) in terms of the ideal, matched Line transfer matrix L^i and two small perturbations δ^{1i} and δ^{2i}, representing errors associated to port 1 and 2, respectively.

2.3.2 Derivation of measurement equations for the propagation constant and error box terms

From the measurement **Equation 2.12**, any pair of Lines i and j measurements yield

$$M^{ij}X = XT^{ij}, \tag{2.15}$$

where

$$M^{ij} \equiv M^j(M^i)^{-1} \text{ and } T^{ij} \equiv T^j(T^i)^{-1}. \tag{2.16}$$

If the standard is ideal (i.e. $\delta^{1i} = \delta^{2i} = 0$), then **Equation 2.15** has the form of an eigenvalue problem, whose eigenvalues solution is expressed in terms of $e^{+-\gamma(l_i - l_j)}$, and the eigenvectors are error box terms of X.

In practice, however, the Line standards are not ideal and the small perturbation errors from **Equation 2.14** are still present in the eigenvalue and eigenvector expressions of T^{ij}. Therefore, each pair of Line measurements will provide a *measurement* of the propagation constant and error box terms. The mTRL algorithm provides a means to extract the *best estimate* for γ and error box terms out of the different *measurements*. A statistical analysis, based on a first-order perturbation error and some assumptions on the errors nature, computes weights to each *measurement*, to finally extract the *best estimate* for each parameter as a weighted average of its different *measurements*. This will be further detailed later on. Let us first show how the measurement equations for γ and error terms are derived.

The first observation is that M^{ij} and T^{ij} have the same eigenvalues. Furthermore, it is also shown that their eigenvectors are related by

$$U^{ij} = XV^{ij}, \tag{2.17}$$

where U^{ij} and V^{ij} are the eigenvectors of M^{ij} and T^{ij}, respectively.

Measurement of the propagation constant

Expanding **Equation 2.14** to a pair of standards, assuming the perturbations are small, give

$$T^{ij} \approx L^{ij} + \varepsilon^{ij}, \tag{2.18}$$

where ε^{ij} is a transfer matrix, whose full expression depends on $\delta^{1i,2i,1j,2j}$, $E^{i,j}_{1,2}$ and can be found in eq. (16) of **[55]**.

Let λ_1^{ij} and λ_2^{ij} be the eigenvalues of T^{ij}, associated to $e^{-\gamma(l_j-l_i)}$ and $e^{+\gamma(l_j-l_i)}$, respectively. To derive measurements of γ, we use the average of λ_1^{ij} and $1/\lambda_2^{ij}$, as they yield the same zero$^{\text{th}}$-order values ($= e^{-\gamma(l_j-l_i)}$ when $\delta^{1i} = \delta^{2i} = 0$). The first-order expansion of λ_p^{ij} ($p = 1,2$) in terms of the small perturbation $\delta^{1i,1j,2i,2j}$ gives

$$\lambda^{ij} \equiv \frac{1}{2}(\lambda_1^{ij} + 1/\lambda_2^{ij}) \approx e^{-\gamma(l_j-l_i)} \left[1 + \frac{1}{2}(\delta_{11}^{1j} - \delta_{11}^{1i} + \delta_{22}^{1i} - \delta_{22}^{1j} + \delta_{11}^{2j} - \delta_{11}^{2i} + \delta_{22}^{2i} - \delta_{22}^{2j})\right]. \quad \textbf{(2.19)}$$

From **Equation 2.19**, we find a *measurement equation of the propagation constant*:

$$\gamma^{ij} = \frac{\ln(\lambda^{ij})}{l_i - l_j} \approx \gamma + \Delta\gamma^{ij}, \quad \textbf{(2.20)}$$

where the explicit linear error term is

$$\Delta\gamma^{ij} = \frac{1}{2(l_i - l_j)} \left[\delta_{11}^{1j} - \delta_{11}^{1i} + \delta_{22}^{1i} - \delta_{22}^{1j} + \delta_{11}^{2j} - \delta_{11}^{2i} + \delta_{22}^{2i} - \delta_{22}^{2j}\right]. \quad \textbf{(2.21)}$$

An important observation to be made here is that *the error in measured γ is minimized by maximizing the difference in line lengths*.

Measurement equation the error box terms

Let us represent X in terms of its different matrix elements:

$$X \equiv r_X \begin{bmatrix} a_X & b_X \\ c_X & 1 \end{bmatrix}. \quad \textbf{(2.22)}$$

The mTRL algorithm provides estimates for b_X and c_X/a_X (as well as for the right error box Y: b_Y and c_Y/a_Y in a similar way, although it is not shown here). **Equation 2.17** gives the relationship between the *measured* quantities (U^{ij}), the *unknown parameters* (X) and the *perturbation error* (V^{ij}).

By renormalizing the M^{ij} eigenvectors, we can write U^{ij} as[5]

$$U^{ij} \equiv \begin{bmatrix} 1 & \eta^{ij} \\ \theta^{ij} & 1 \end{bmatrix}. \quad \textbf{(2.23)}$$

[5]Note the change in notation from **[55]** $\alpha^{ij} \to \eta^{ij}$ and $\beta^{ij} \to \theta^{ij}$, to avoid any confusion with transmission line loss and phase delay parameters α and β.

From the definition of η^{ij} and θ^{ij} in **Equation 2.23** and expanding the small perturbation error in **Equation 2.17**, we obtain the following *measurement equations for the b_X and c_X/a_X box error terms*:

$$\eta^{ij} \approx b_X + \Delta\eta^{ij}, \tag{2.24}$$

and

$$\theta^{ij} \approx c_X/a_X + \Delta\theta^{ij}. \tag{2.25}$$

The explicit error terms are

$$\Delta\eta^{ij} \equiv \varepsilon_{12}^{ij} \frac{a_X - b_X c_X}{e^{\gamma(l_j-l_i)} - e^{-\gamma(l_j-l_i)}}, \tag{2.26}$$

and

$$\Delta\theta^{ij} \equiv \varepsilon_{21}^{ij} \frac{a_X - b_X c_X}{a_X^2\left(e^{\gamma(l_j-l_i)} - e^{-\gamma(l_j-l_i)}\right)}. \tag{2.27}$$

Two important observations have to be emphasized here. First, only the off-diagonal terms in ε^{ij} contribute to first-order in η^{ij} and θ^{ij}. It is demonstrated in **[55]** that these linear errors are induced only by errors in the *reflection* coefficients S_{11} and S_{22} of the line measurements. This is an interesting observation, as it means that uncertainties in reflection coefficients only, which can be estimated with the ripple test **[62]**, could be used to first-order to propagate the uncertainty in the error box terms (and on the extracted line characteristic impedance, as seen in a subsequent section).

The second interesting observation is that both linear error terms $\Delta\eta^{ij}$ and $\Delta\theta^{ij}$ are inversely proportional to

$$e^{\gamma(l_j-l_i)} - e^{-\gamma(l_j-l_i)} = 2j\sin\left[(l_j-l_i)\beta - j(l_j-l_i)\alpha\right], \tag{2.28}$$

with $\gamma = \alpha + j\beta$.

For a lossless line ($\alpha = 0$),

$$|\Delta\eta^{ij}|, |\Delta\theta^{ij}| \propto \frac{1}{2|\sin[(l_j-l_i)\beta]|}. \tag{2.29}$$

This result show the frequency limitation of the TRL method. Indeed, the error made in the error terms measurement becomes infinite when the difference

in phase delays is equal to $n\pi, n \in \mathbb{Z}$. This is equivalent to $(l_j - l_i) = n\frac{\lambda_{eff}}{2}, n \in \mathbb{Z}$. So, *the calibration problem is ill-condition at each frequency for which the line length difference is a multiple of a half wavelength*. It also means that the error is minimized when the difference in phase delays is $90° + n180°, n \in \mathbb{Z}$, or $(l_j - l_i) = \frac{\lambda_{eff}}{4} + n\frac{\lambda_{eff}}{2}, n \in \mathbb{Z}$.

For a low-loss line, when $(l_j - l_i)\beta = n\pi, n \in \mathbb{Z}$,

$$|\Delta\eta^{ij}|, |\Delta\theta^{ij}| \propto \frac{1}{2|\sin[(l_j - l_i)\alpha]|} \approx \frac{1}{2|(l_j - l_i)\alpha|}. \tag{2.30}$$

This result show that, even though the calibration problem is still ill-conditioned when the phase difference is a multiple of 180°, the error is reduced for longer line length differences or lossier lines.

From those considerations, [55] defines a useful quantity that is linked to the error made in the error box terms measurement: the *effective phase difference*, ϕ_{eff}, such that

$$\begin{aligned}\phi_{eff} \equiv \arcsin\left|\frac{1}{2}\left(e^{\gamma(l_j - l_i)} - e^{-\gamma(l_j - l_i)}\right)\right| \\ = \arcsin\left|\sin\left[(l_j - l_i)\beta - j(l_j - l_i)\alpha\right]\right|.\end{aligned} \tag{2.31}$$

Since $\alpha \neq 0$ in general, it is $1/|\sin\phi_{eff}|$ and not $1/|\sin[(l_j - l_i)\beta]|$ that actually predicts the error magnitude. If the argument in the arcsin of **Equation 2.31** is larger than 1, ϕ_{eff} is set to 90°.

Several important observations are made in this sub-section:

- The mTRL algorithm formulates the calibration problem as a first-order perturbation problem.
- For each pair of line measurements, **Equation 2.20**, **Equation 2.24**, **Equation 2.25** give measurement equations of the propagation constant and b_X and c_X/a_X error box terms, respectively, and their associated linear error are expressed in **Equation 2.21**, **Equation 2.26**, **Equation 2.27**, respectively.
- The linear error in measured γ is *minimized* by maximizing the difference in line length.
- The linear error in measured b_X and c_X/a_X is *maximum* (infinite for a lossless line) when the difference in phase delays is an integer multiple of 180°, i.e. $(l_j - l_i)\beta = n\pi, n \in \mathbb{Z}$, or equivalently, when the length difference is a multiple of a half wavelength.
- The linear error in measured b_X and c_X/a_X is *minimum* when the difference in phase delays is $90° + n180°, n \in \mathbb{Z}$, or equivalently $(l_j - l_i) = \frac{\lambda_{eff}}{4} + n\frac{\lambda_{eff}}{2}, n \in \mathbb{Z}$.
- To generalize the error made on the error box terms to the case of lossy lines, a new variable ϕ_{eff} is defined in **Equation 2.31**. The error on the error box terms is maximized when $\phi_{eff} \to 0$ and minimized when $\phi_{eff} \to 90°$.

2.3.3 Best estimates from redundant measurements

From the measurement of several lines of different length, we accumulate redundant information on the propagation constant and some error box terms. **[55]** proposes a way to find the best estimates for these unknown parameters as a weighted average of their measurements from each pair of lines.

Let us refer to a general case, in which we have N independent measurements b_n of a quantity $a_n x$, along with some error e_n, x being the unknown parameter to be determined, such that

$$b_n = a_n x + e_n. \tag{2.32}$$

Assuming no systematic errors are present, the Gauss-Markov theorem states that the best unbiased linear estimate is obtained from a least squares regression:

$$\underline{x} = (\sigma_x)^2 \mathbf{a}^\dagger \mathbf{V}^{-1} \mathbf{b}, \tag{2.33}$$

where $\underline{x}$ is the best unbiased estimate, $\mathbf{a}$ and $\mathbf{b}$ are column vectors whose elements are a_n and b_n, † denotes the Hermitian adjoint, the covariance matrix $\mathbf{V}$ is defined by

$$V_{mn} \equiv \langle e_m^{\star} e_n \rangle, \tag{2.34}$$

and σ_x is defined by

$$\sigma_x \equiv \frac{1}{\sqrt{\mathbf{a}^{\dagger}\mathbf{V}^{-1}\mathbf{b}}}. \tag{2.35}$$

The estimate is 'best', because it minimizes the variance of $\underline{x}$. No assumption about the errors' statistical distribution is made.

Because the Gauss-Markov theorem cannot be applied to a set of linearly dependent measurements, for a set of $N+1$ measurements of different Lines (including the Thru), there are N linearly independent measurements of the unknown parameters. These N measurements are considered to come from the pairing of a particular Line i with each of the other Lines j. In general, the common Line i is not the same at all frequencies.

To evaluate the covariance matrix, a series of assumptions are made in [55] on the nature of the errors δ^{1i} and δ^{2i}.

- Errors in the measurements of two different Lines are uncorrelated.
- Each Line measurement is equally prone to error.
- Errors are caused by imperfect repeatability of the two contacts/connectors, instead of being caused by imperfect Lines.
- Ports 1 and 2 are equally noisy, and S_{11} and S_{22} of the contacts/connectors are also equally noisy.

Finally, the best estimates for the propagation constant and error box terms are obtained with the following substitutions:

$$x = \begin{Bmatrix} \gamma \\ b_X \\ c_X/a_X \end{Bmatrix}, \; b_n = \begin{Bmatrix} \ln\left(\lambda^{ij}\right) \\ \eta^{ij} \\ \theta^{ij} \end{Bmatrix}, \; a_n = \begin{Bmatrix} l_i - l_j \\ 1 \\ 1 \end{Bmatrix},$$
$$\text{and } e_n = \begin{Bmatrix} \Delta\gamma^{ij}(l_i - l_j) \\ \Delta\eta^{ij} \\ \Delta\theta^{ij} \end{Bmatrix}. \tag{2.36}$$

The covariance matrices are lengthy expressions found in eq. (66), (76) and (77) of [55]. They are all proportional to a standard deviation term related to

the errors (σ_κ for the covariance matrix of γ, σ_δ for the covariance matrices of the error terms). Exact evaluation of these standard deviations is not required as they simplify themselves in **Equation 2.33**, since $\mathbf{V}^{-1}$ appears both at the numerator and denominator.

Not knowing these standard deviations prevents the prediction of *absolute* standard deviations for the unknown parameters, however, we can still predict *relative* standard deviations for the unknown parameters and *compare various sets of calibration standards*. With that objective, two *normalized* standard deviations are defined as

$$\sigma_{\eta 0} \equiv \frac{\sigma_\eta}{|a_X - b_X c_X|\sigma_\delta}, \tag{2.37}$$

and

$$\sigma_{\theta 0} \equiv \frac{\sigma_\theta}{|a_X|^2|a_X - b_X c_X|\sigma_\delta}. \tag{2.38}$$

Their expressions only contain (i) on γ, which can be calculated from **Equation 2.33**, (ii) on measured λ^{ij} from **Equation 2.19** and (iii) on the Line standards length. Note that $\sigma_{\eta 0} = \sigma_{\theta 0}$ for any number of lossless lines, so, in practice, only one of the two is used. The normalization is such that $\sigma_{\eta 0} = \sigma_{\theta 0} = 1$ for a calibration using a single pair (TRL) of lossless transmission lines, evaluated at a frequency for which the effective phase difference (ϕ_{eff}) is 90°, i.e. when the error made on the error box terms measurement is minimum.

The important *take-away messages* in this sub-section are

- The mTRL algorithm uses a least squares regression to obtain weights and compute a weighted average of the unknown parameters measurements from different pairs of Lines. Assuming no systematic errors are present, the best unbiased estimate given by Gauss-Markov theorem is expressed in **Equation 2.32**. The link to the propagation constant and error box terms is given in **Equation 2.36**.
- Two normalized standard deviations are defined in **Equation 2.37** and **Equation 2.38**. They provide relative standard deviations for the error box terms and enable the comparison of extraction accuracy among different sets of calibration standards.

2.3.4 Performance of the multiline calibration method and design rules recommendations for an mTRL calkit

The mTRL algorithm enables the extraction of γ and 4 out of 7 of the needed error box terms, out of redundant information from the measurement of pairs of Line standards. The other terms are not specific to the mTRL algorithm and are discussed later. As mentioned above, the measurement error on γ and on the error box terms are different and are minimized with different criteria.

- We have seen that the error on γ is minimized by maximizing the difference in Lines length, irrespective to the frequency.
- Whereas the error on b_X and c_X/a_X are minimized when $\phi_{eff} = 90°$, which varies with frequency!

For a single pair of Lines (TRL), a common rule of thumbs relates the validity of the calibration to the frequency range in which $\phi_{eff} > 20°$. So, maximizing the difference in line lengths decreases the valid frequency range. Therefore, these two error minimization criteria are in conflict for a single pair of Lines, but they can be respected in case of multiple Lines of different lengths.

For the design of an mTRL calibration kit (calkit), the choice of the Lines length is crucial to minimize the calibration errors. Here is a procedure to determine the line length differences ($l_j - l_0$) of an mTRL calkit (l_0 being the Thru standard length, which is discussed shortly after).

1. For *Line1*, maximize the line length difference ($l_1 - l_0$) with the Thru standard to minimize the error made on the γ measurement. For low-loss transmission lines, a recommended value is 5-6 mm from experience. If the requirements in available area prevents using such a long line, it is recommended to use the longest possible line.
2. For *Line2* and *Line3*, to minimize the measurement error of the error box terms in a given frequency range of interest, the recommendations given in **[55]** apply here. *Line2* length should be set to have the first $\phi_{eff} = 90°$, or $(l_2 - l_0) = \lambda_{eff}/4$, at the center of the frequency range of interest. For *Line3*, setting $l_3 - l_0 = 3(l_2 - l_0)$ gives good results.
3. If additional Lines can be included in the calkit, we could recommend to add the minimum amount of Line standards such that $\phi_{eff} > 60°$ over the whole frequency range. This can be performed iteratively by computing ϕ_{eff} with **Equation 2.31**, based on an estimated frequency-independent $\varepsilon_{r,eff}$ of the transmission line.

Actually the first standard length to be determined is the Thru length (from which all other Line standards lengths are derived). However, the mTRL

algorithm does not provide any recommendations for the length of this standard (all calibration errors are a function of line length differences). Still, the Thru length determination is not a straightforward choice. There are several aspects to consider.

First, for the correct application of the (m)TRL method, a single mode must be propagating at the middle of the Thru standard. This sets a first condition on the minimum length of the Thru. As different modes can be excited by the probes or pad transition to the line section, the Thru standard must be long enough to ensure that they have vanished at the middle of the Thru.

Second, probe-to-probe coupling or crosstalk is another important issue at very high frequency. As a general rule of thumbs, a minimum of probe to probe separation of 150 µm is recommended (in all commercial calibration substrates)[6]. Experimental and simulation investigations **[63]** have failed to give a more precise general minimum distance recommendation.

Third, area is of uttermost importance in integrated circuits. Since the Thru length will affect the length of all other Line standards, using the minimum possible length is required to minimize area consumption of the overall calkit.

An illustrative example

To illustrate this procedure, let us take a simple example. A closed-form equations model **[64]** is used to build S-parameters from realistic low-loss CPW lines dimensions on silicon substrate ($\varepsilon_{r,eff} \approx 6.3$). Then, these S-parameters are used in the mTRL algorithm described above to compare the ϕ_{eff} and the normalized standard deviation $\sigma_{\eta 0}$ parameters of different TRL calibrations made with different sets of Lines.

Let [1 GHz, 110 GHz], be the frequency range of interest. Let us take a Thru length of 200 µm. According to 1, $l_1 = 6200\,\mu\text{m}$. At the center of the frequency range (55 GHz), a quarter wavelength is 540 µm, so $l_2 = 740\,\mu\text{m}$. According to 2, $l_3 = 3(l_2 - l_0) + l_0 = 1820\,\mu\text{m}$.

The extracted ϕ_{eff} and $\sigma_{\eta 0}$ are shown in **Figure 2.7**. As we can observe, the mTRL calibration is wideband, with $\phi_{eff} > 60^\circ$ almost over the whole frequency range (two minimum values at 10 and 100 GHz). Using two additional Lines of 500 µm (for 100 GHz) and 3200 µm (for 10 GHz) guarantees $\phi_{eff} > 60^\circ$ over the whole frequency range. Furthermore, the normalized

[6] This length is *after* probe overtravel, which depends on the probe technology, age, prober accuracy and user's will. The total Thru length of commercial calibration substrates is 200 µm so that a maximum of 25 µm of probe skating on metal should be used.

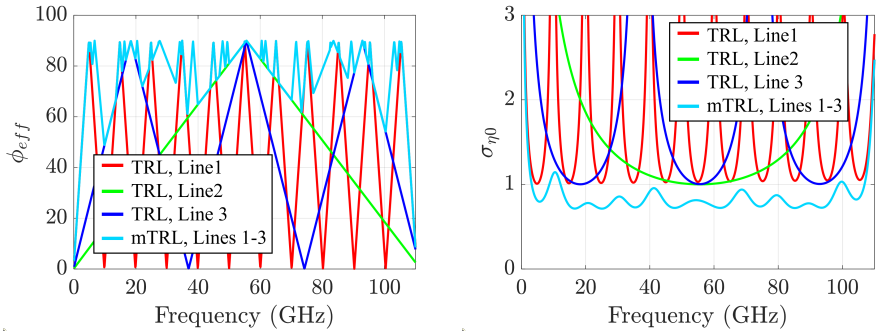


Figure 2.7: Illustrative example showing the performance of mTRL. (a) effective phase delay. (b) normalized standard deviation of error box terms.

standard deviation is almost always lower than 1, which means an improved accuracy level than any TRL can achieve over (almost) the whole frequency range.

2.3.5 Extraction of remaining parameters

The remaining calibration parameters to be extracted that has not yet been determined are: a_X, a_Y, r_X, r_Y, the Reflect reflection coefficient and the transmission line characteristic impedance. Actually, only the ratio r_X/r_Y is computed and is needed to perform the calibration. We provide references for the extraction of the first remaining parameters and we discuss in more details the determination of Z_c in the next sub-section.

The a_X and a_Y terms (as well as the Reflect reflection coefficient) are extracted from the Reflect standard measurement. The nature of the Reflect standard (Open or Short) is needed to solve an indetermination. Then, by assuming that the reflection coefficient is identical in both ports and there is no transmission from port 1 to port 2 (and vice versa), eq. (56)-(61) in **[37]** give a_X and a_Y.

The r_X, r_Y are also given in **[37]**, eq. (62)-(63), based on the Thru standard measurement and assuming it to be reciprocal. These expressions give a well-defined ratio r_X/r_Y, but the exact allocation of r_X and r_Y is tricky and has been investigated in different papers **[51, 65]**.

Finally, only the characteristic impedance is missing to transform the cali-

bration reference impedance from the so-far unknown Z_c in 50 Ω.

2.3.6 Characteristic impedance determination from the propagation constant

Several methods to extract the characteristic impedance of a transmission line exist and will be covered in the next section. In the present section, the benchmark method, commonly used in commercial and reference (NIST RM8130 GaAs substrate) calibration substrates [66, 67], is introduced.

The method from [66] starts from Equation 2.1 and Equation 2.2, their ratio gives:

$$\frac{\gamma}{Z_c} = j\omega C + G. \tag{2.39}$$

Assuming the substrate losses are low, i.e. $G \ll \omega C$, and C is known, then Z_c can be extracted from the measurement of γ, which is accurately determined by the mTRL algorithm.

[67] provides three methods to determine C, (i) from a load measurement, (ii) from the Lines dc resistance measurement, (iii) from the direct comparison of lines. In all of them, C is assumed to be frequency-independent.

Load measurement

For a small lumped resistor, its impedance at low frequency is approximated by

$$Z_{ref}\frac{1+\Gamma_{\text{load}}}{1-\Gamma_{\text{load}}} \equiv Z_{\text{load}} \approx R_{\text{load,dc}}, \tag{2.40}$$

where $R_{\text{load,dc}}$ is the dc resistance of the lumped Load and Γ_{load} is its reflection coefficient. During the (m)TRL calibration process, the measurement reference impedance is Z_c of the Line standard(s) (if Z_c is not yet known or Z_{ref} transformed to 50 Ω). Replacing Z_{ref} in Equation 2.40 by its expression from Equation 2.39 yields

$$C\,[1 - j(G/\omega C)] \approx \frac{\gamma}{j\omega R_{\text{load,dc}}}\frac{1+\Gamma_{\text{load}}}{1-\Gamma_{\text{load}}}. \tag{2.41}$$

Finally, C is extracted from a least-squares fit of a quadratic polynomial function to the measured low-frequency right-hand-side of Equation 2.41.

dc resistance Lines measurement

Another method proposed in [67] consists of re-writing Equation 2.2 in

$$RC + LG = \mathrm{Re}\left(\frac{\gamma^2}{j\omega}\right). \tag{2.42}$$

Assuming G is small, $LG \ll RC$, and approximating R to the dc resistance per unit length of the line, R_{dc}, at low frequency, then Equation 2.42 becomes

$$C \approx \frac{1}{R_{\mathrm{dc}}}\mathrm{Re}\left(\frac{\gamma^2}{j\omega}\right). \tag{2.43}$$

Here again, C is extracted from a least-squares fit of a quadratic polynomial function to the measured low-frequency right-hand-side of Equation 2.43.

Direct line comparison

The last method presented in [67] consists of comparing the measurement of an unknown Line based on a (m)TRL calibration made on a known Line. It is assumed that the measured reflection coefficient of this unknown Line solely describes the difference in characteristic impedance from the known Line (used for calibration) to the unknown Line.

The concept is actually very similar to the calibration comparison method (used a few years after for such application), which will be explained in the next section. The 'direct line comparison' is a less common method and, for that reason, it is not going to be further developed here.

2.3.7 Benchmark mTRL method

Those two papers [66, 67] are at the basis of the method for the Z_c extraction of CPW lines on low-loss substrates. Although this method is based on some approximations ($G = 0$ and C is frequency-independent, i.e. *negligible substrate losses* and *non-dispersive* lines), it is considered in the literature to be valid for CPW lines on very low-loss substrates [68–70] and, at times for other planar transmission lines [69] having higher losses [71]. A critical discussion on this approximation is provided in the last section of this chapter.

Finally, the mTRL algorithm described in this section, coupled to the Z_c extraction technique detailed in this sub-section, form the benchmark method for on-wafer calibration. Thanks to its high accuracy and use of well-defined standards that enable traceability, it is also used to evaluate system drift, evaluate other calibrations' accuracy, etc. In particular, this last aspect uses the

calibration comparison technique introduced in [72] that is the main method to extract Z_c of lines on an unknown (potentially lossy) substrate. It is the main topic of the next section.

2.4 Calibration Comparison Method for Characteristic Impedance Extraction

In the previous section, the benchmark method to extract the characteristic impedance of transmission lines on a low-loss substrate has been presented. However, it is not applicable to unknown or lossy substrates. Plenty of methods have been developed to that end [54, 73, 74]... Most of them rely on the so-called calibration comparison method.

In this section, the calibration comparison technique is first presented. Then, two state-of-the-art methods to extract the characteristic impedance of a transmission line are presented.

2.4.1 Calibration comparison technique

The calibration comparison technique has first been introduced in [72], initially to evaluate the accuracy of a given calibration, based on the benchmark mTRL calibration. It has later been used to extract the characteristic impedance of transmission lines on different types of substrates, either low-loss or lossy [70, 75–77].

In the calibration comparison technique two calibrations are performed. The first calibration, also called *first-tier* calibration, removes systematic errors from the VNA, cables, probes, etc. and places the reference plane position on-wafer (usually at the probe tips when performed with commercial calibration substrates), with a well-defined reference impedance. An example is given in **Figure 2.8**, where a 8-term error model is used, even though any error box model could be used. All subsequent measurements are first corrected with this first-tier calibration.

As a second step, a second calibration is performed, also called *second-tier* calibration, shown in **Figure 2.9**. It can be realized on the same standards (for system-drift or repeatability evaluation), on other standards of the same calibration substrate (compare different calibration methods) or on standards on a different substrate (to extract an unknown Z_c for instance). The newly calculated error terms (X' and Y') describe (i) the change in reference plane position, (ii) change in reference impedance, (iii) any other differences between

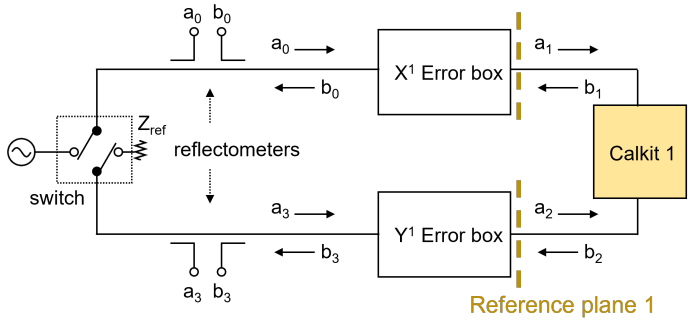


Figure 2.8: First-tier calibration.

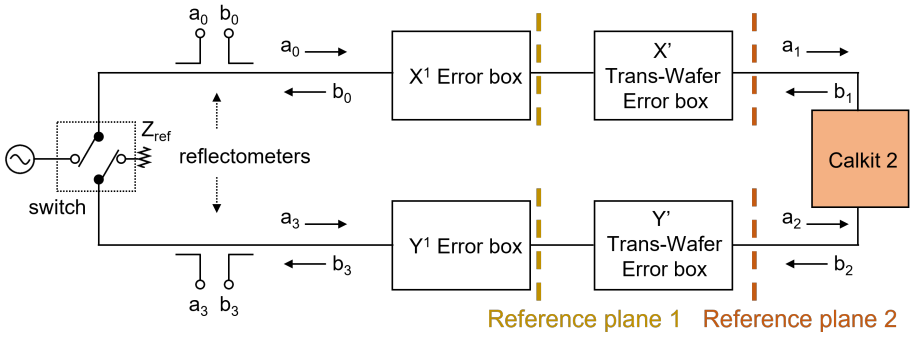


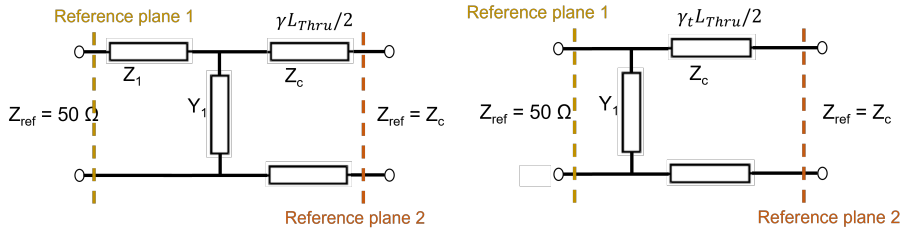
Figure 2.9: Second-tier calibration.

the two calibrations.

Typical additional differences between the first- and second-tier calibrations are (i) change in substrate permittivity (thus in shunt capacitance at each probe), (ii) pad-to-homogeneous-transmission-line transition that might be on the same metal layer (taper) or on a different metal layer (vias), (iii) probe coupling with neighbor devices.

Characteristic impedance extraction

This calibration comparison technique was first applied to extract the characteristic impedance of a transmission line in [75], for which only a change in reference plane position and reference impedance described the trans-wafer error boxes. Later, the formalism has been extended to take into account additional changes from the first-tier to second-tier calibrations. All these methods



(a) Trans-wafer error box from **[74]**. **(b)** Trans-wafer error box from **[73]**.

Figure 2.10: Equivalent circuits of trans-wafer error box.

vary in the equivalent circuit used to map the trans-wafer error box and, thus, on the equations to extract Z_c. Two more advanced equivalent circuits representing the trans-wafer error box are summarized in **Figure 2.10**.

In **[74]** (cf. **Figure 2.10a**), the trans-wafer error box has small shunt admittance and series impedance elements that can represent a potential change in substrate permittivity and losses and short pad transitions or vias. First, a shift in reference plane of the trans-wafer error boxes X' and Y' is performed from the middle of Thru to the probe pads (the Thru propagation constant is already extracted from the mTRL algorithm, and the Thru length is known). Then, the method extracts Z_c from

$$Z_c = \frac{A}{D} \cdot 50, \tag{2.44}$$

where A and D are elements of the $ABCD$-parameters representation of the trans-wafer error box, after reference plane correction. '50' accounts for the first-tier reference impedance that has been normalized to 50 Ω. Assuming the product of Z_1 and Y_1 elements is small, the extracted characteristic impedance does not depend on such elements. Since there are two (left and right) error boxes, Z_c is effectively obtained from an average of the right-hand-side of **Equation 2.44** for the left and right boxes.

This method works very well and yields excellent results in most cases. An example in which it might give inaccurate results is when a large series impedance is present. It might happen when long tapers are used to connect the probe pad to the to-be-characterized transmission line (dut). **Figure 2.11** illustrates such an example. In that case, approximating the taper to a piece of transmission line with the same propagation constant as the dut might be

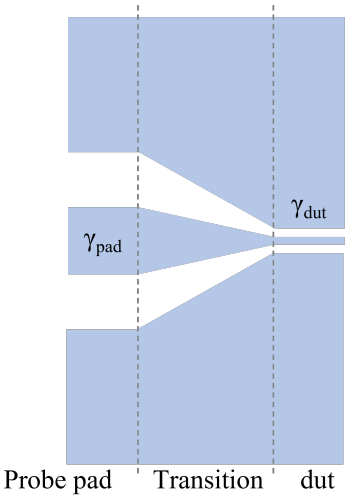


Figure 2.11: Illustrative example of long probe-pad-to-transmission line (dut) taper, with very different propagation constant.

incorrect. We developed a method in **[73]**, available in **Appendix A**, that might be more suited to this case.

This method relies on the equivalent model shown in **Figure 2.10b** for the trans-wafer error box. In this case, a shunt element is present to account for potentially different substrate permittivity and loss, as well as a piece of transmission line, of a half thru length, of a characteristic impedance equal to the dut but of unknown propagation constant (γ_T).

Actually, **Figure 2.10b** represents half of the Thru standard from probe tip to the middle of the Thru. So, the Thru standard, *measured from probe tip to probe tip*, is modeled with shunt elements at each end and a piece of transmission line with the same Z_c as the other lines, but with a different propagation constant accounting for a taper for instance. Another advantage of this method is that it does not require a Reflect standard measurement.

However, there are some indeterminations that require an estimation of Z_c. Such estimate can be provided either by the above method (Liu's) if a Reflect standard measurement is available or from **[54]** if not. The full expression yielding Z_c is lengthy and is not provided here, but it can be found in **Appendix A**.

The case of long taper connecting a probe pad to a transmission line dut

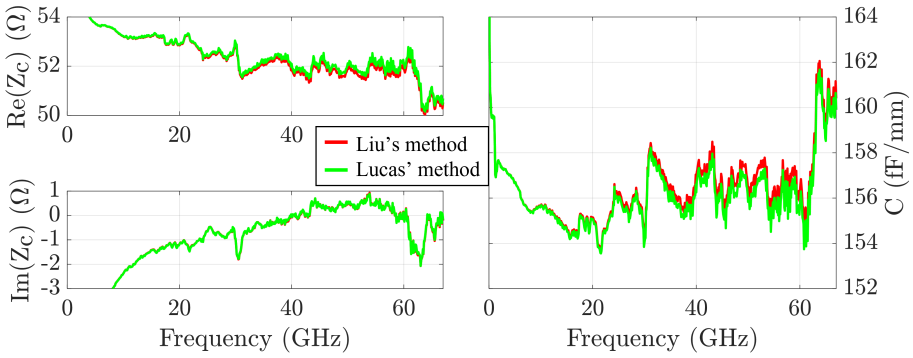


Figure 2.12: Extracted Z_c (left) and capacitance per unit length C of a CPW line on a low-loss (trap-rich) Si substrate. Comparison between two methods to extract Z_c: Liu's **[74]** in red and **[73]**'s in green.

of different propagation constant is used for comparison of the two aforementioned methods. The taper length is 93 µm and the pad length is 100 µm. The transmission lines are CPW lines on a low-loss (trap-rich) Si substrate. The line lengths are a Thru of 10 µm length and two Line standards of 2.1 mm and 8.1 mm lengths. The objective is to simply compare the performance of the two Z_c extraction methods, more details concerning the substrate and lines are available in **Chapter 3**. The Z_c extracted with both methods as well as the per-unit-length C of the transmission line are shown in **Figure 2.12**.

As shown above, as well as in general, both methods yield very similar results. So, in this thesis, Liu's **[74]** method is used if a Reflect standard is available, otherwise **[73]** is employed.

2.5 Reference Impedance of Calibration

To answer the needs of high measurement accuracy, accurate electrical behavior characterization of custom on-wafer standards is crucial. Whether it be for device characterization or substrate loss evaluation, transmission lines are widely used standards enabling benchmark mTRL calibration. The propagation constant of transmission lines can be accurately extracted with mTRL algorithm as seen above. The remaining unknown parameter, i.e. the characteristic impedance, is however more complex to determine and its extraction relies on more assumptions.

Marks' method [66] assuming $G = 0$ and C is frequency-independent is not applicable to any arbitrary transmission line. Although some interesting work indicates that accurate 3D electromagnetic (EM) simulations is a viable way to determine Z_c at sub-THz frequencies [78], the method of reference is the calibration comparison technique explained above.

However, this technique relies on several assumptions: (i) validity of the equivalent circuit representing the error boxes, (ii) the first-tier calibration is ideal with a *well-defined reference impedance* (Z_{ref}). A lot of work has been devoted to extend the equivalent circuit representation of the error boxes, but few papers have criticized the validity of the first-tier calibration [24, 79].

This section focuses on the latter assumption and investigates which calibration method provides the best-defined reference impedance for use in the calibration comparison method. This section is organized as follows. First, a method to extract the Z_{ref} of a calibration is described. Then, we evaluate the Z_{ref} of different commonly used calibration algorithms (SOLT, LRRM, mTRL) and analyze to which parameters it is sensitive. Finally, we discuss the validity of the assumptions to extract Z_c from γ in [66] of commercial calibration substrates.

2.5.1 Reference impedance extraction method

Little attention has been devoted to the assessment of a calibration reference impedance, with only three methods presented up to now, to the best of our knowledge. In [80], Z_{ref} is extracted from an Open standard measurement, providing a capacitance-based model for the Open, as in an SOLT calibration. This model is too simple and does not account for radiation loss in Open standard, thereby not representing well an Open standard behavior at high frequencies. The accuracy of the extracted Z_{ref} with this method becomes thus questionable at high frequencies.

In [81], the Z_{ref} of an mTRL calibration is assessed with a second mTRL calibration performed on step impedance lines that create an impedance transition. Although an interesting method to evaluate the quality of the Z_{ref} of an mTRL calibration, it requires special structures, not available on commercial calibration substrates and does not propose a way to evaluate the Z_{ref} of other types of calibration.

[72], where the calibration comparison method is firstly introduced, also describes the extraction of a calibration Z_{ref}, based on a known, reference calibration, assuming they only differ from a different reference plane position and Z_{ref} change.

Here, we augment the method from [72] to extract the reference impedance of a calibration, based on a more recent formulation of the calibration comparison technique [74] (Liu's method, explained in the previous section). The procedure is the following. A first-tier calibration is realized, the *test* calibration for which the Z_{ref} is to be determined. Then, a (m)TRL calibration is performed as the second-tier calibration. The trans-wafer error boxes obtained describe (i) the shift of reference plane, (ii) change in calibration reference impedance and (iii) other parasitics, for instance different substrate permittivity and losses, pad transition (taper and/or vias) to transmission line.

With the formulation used in the Appendix of [74], the extracted Z_{ref} becomes independent from such other parasitics, as opposed to [72]. The trans-wafer error box equivalent circuit used for this method is shown in **Figure 2.10a**. As a reminder from **Equation 2.44**, the transmission line Z_c from the second-tier calibration can be computed by

$$Z_c = \frac{A}{D} \cdot Z_{ref}, \tag{2.45}$$

where A and D are the elements of the $ABCD$-matrix representation of the trans-wafer error boxes and Z_{ref} is the reference impedance of the first-tier calibration. Note that the reference plane of the second-tier calibration has already been shifted from the middle of the Thru to the probe tips in the trans-wafer error box parameters, although not explicitly mentioned in [74].

The proposed method to extract the reference impedance is to simply reverse **Equation 2.45**, assuming Z_c is known. Since there are two error boxes extracted, one for each port, and Z_c of the line is unique and does not depend on the measurement direction, we can therefore extract the reference impedance for

each port (subscript 1 and 2 below), i.e.

$$Z_{ref1} = Z_c \cdot \left(\frac{D}{A}\right)_1, \text{ and } Z_{ref2} = Z_c \cdot \left(\frac{D}{A}\right)_2. \tag{2.46}$$

Note that the first-tier reference plane position does not necessarily need to be at the probe tips, although it will be the case in the rest of this section. What is important is to minimize the parasitic Z_1 and Y_1 terms (defined in **Figure 2.10a**) such that **Equation 2.45** remains independent of such terms. So, this Z_{ref} extraction method can also be applied at a different reference plane than the probe tips, as long as the transitions between the first-tier and second-tier calibrations are small.

Concerning the second-tier Z_c determination, we use the method from **[66]** in the following, in which Z_c is extracted from the measured propagation constant and known per-unit-length transmission line C element **[67]**.

By using the same Z_c extraction method for the mTRL calibration and Z_{ref} extraction, we artificially assume that the mTRL calibration yields a perfect $Z_{ref} = 50\,\Omega$ (after reference impedance transformation from Z_c to $50\,\Omega$). It therefore enables a relative comparison between Z_{ref} of different calibrations algorithms and mTRL, taken as reference.

2.5.2 Reference impedance of SOLT and LRRM calibrations

SOLT calibration is the most used calibration, even though its accuracy critically depends on fabrication and modeling tolerances of the standards and usually degrades with increasing frequencies. LRM-type calibrations are also limited by the Load and Thru standards that must be known. Despite both being sensitive to probe misplacement on standards **[45, 47]**, LRM-type calibrations, as self-calibration methods, are less sensitive than SOLT. The Load standard is used in LRM-type calibrations to set the reference impedance **[36]**.

Description of measurement setup and procedure

Open, Short, Load, Thru and Lines (0.45, 0.9, 1.8, 3.5, 2.25 mm) standards of the commercial AC-2 calibration substrate are measured with Ground-Signal-Ground (GSG), 110 GHz, 100 µm-pitch, MPI TITAN^{TM} probes and a Keysight N5291A VNA from 200 MHz to 110 GHz[7], with 100 Hz IF bandwidth and

[7] All '110' GHz measurements in this thesis are performed up to 130 GHz. The VNA is specified up to 125 GHz, but allows measurements up to 130 GHz. However, the connectors and probes are specified up to 110 GHz. A narrowband resonance can appear in measurements

−5 dBm power at the VNA, on a semi-automatic MPI probe station, with East motorized positioner PMP80. The AC-2 substrate is placed on a ceramic chuck.

For the standards definition needed in the LRRM and SOLT calibration algorithms, each standard is preliminary characterized based on an mTRL calibration to compensate for manufacturing inaccuracies and variations in probe placement with respect to AC-2 substrate specifications. The extracted standard parameters are summarized in **Table 2.1**. Automatic Load inductance search (in LRRM **[56, 57]**), which consists of an optimization algorithm and complicates the Z_{ref} dependence on measured standards, is disabled for this experiment to ease results interpretation. Similar and further investigations on LRRM with the automatic load inductance search enabled is presented in **Appendix B**.

Table 2.1: Standards model used in SOLT and LRRM calibrations, with TITAN probes on AC-2 calibration substrate.

Load		**Open**	**Short**
R-term	*L-term*	*C-term*	*L-term*
49.95 Ω	−4.5 pH	6.3 fF	5 pH

For all experiments in this section, raw measurements are saved for post-processing. The first-tier calibrations are performed with WinCal XE software. The second-tier calibration and subsequent post-processing is realized with in-house Matlab scripts implementing the mTRL algorithm described in **[37, 55]**. When available, the per-unit-length C term of transmission lines is determined with the load method explained in **Section 2.3.6** (**[67]**) and confirmed with the calibration comparison method. Otherwise, the C term is directly obtained from the calibration comparison technique.

Comparison among SOLT, LRRM and mTRL

Figure 2.13 shows the extracted Z_{ref} from the three most common calibration algorithms: SOLT, LRRM and mTRL. As anticipated above, the extracted Z_{ref} with mTRL features an ideal 50 Ω across the whole frequency range.

The Z_{ref} extraction procedure presented in this paper might be sensitive to system drift, as it takes some time to accurately perform the experiments.

around 120 GHz because of those connectors. When measurements are performed shortly after calibration this resonance can be corrected. So, sometimes some graphs are shown up to 130 GHz and others up to 110 GHz, but they have all been acquired with the same measurement setup.

To quantify the impact, the transmission line standards have been re-measured after 3 days and used to extract the mTRL Z_{ref}, after a 3-days system drift. As shown by the cyan lines, negligible deviation from 50 Ω is observed, thus demonstrating the negligible impact of system drift in these experiments.

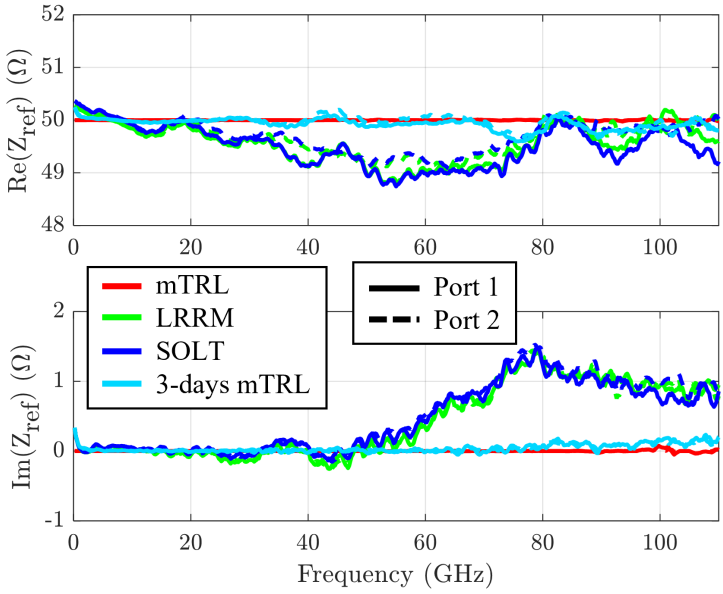


Figure 2.13: Extracted $Z_{ref1,2}$ from different calibrations on AC-2 calibration substrate.

For both LRRM and SOLT calibrations, we see that $\mathrm{Re}(Z_{ref})$ stays close to 50 Ω within 2 %, whereas $\mathrm{Im}(Z_{ref})$ features three different behaviors across frequency. From low frequencies up to ∼ 50 GHz, $\mathrm{Im}(Z_{ref})$ stays close to 0 Ω and is mainly described by a series inductance term in the Load model as we shall see in the following. The higher frequency behaviors in Z_{ref} (from 50 GHz to ∼ 80 GHz and above 80 GHz) include other effects, which require further investigations (it shall not be further discussed in this thesis). The extracted Z_{ref} depends on the Load model used by the calibration algorithm. The systematic deviation in Z_{ref} could be avoided with a more complex model than the series R-L used by WinCal, but it is out of scope of this thesis. Since the SOLT and LRRM calibrations mainly deviate in the Open and Short models, extracting approximately identical Z_{ref} for SOLT and LRRM suggests that errors in Open and Short models have less influence on the calibration Z_{ref}.

Reference impedance sensitivity to probe misplacement

Previous work has already investigated calibration uncertainty on probe contact position for SOLT [45, 46] and LRM-type calibrations [45, 47]. They have shown that LRRM is less sensitive to probe position misplacement and have proposed another version of LRM-type algorithm to reduce the inaccuracies coming from probe misplacement on Reflect standards [47]. Here, we focus on the reference impedance of LRRM calibration, because it is less sensitive to probe misplacement than SOLT[8], and we analyze how it is affected by variation in probe contact position on each standard.

Each standard is re-measured by varying the left probe (port 1) contact position by $\sim$10 µm to the right (toward the right probe). **Figure 2.14** shows the extracted Z_{ref} for an LRRM calibration performed with (i) measurements with no variation in contact position ('Nominal' in legend, red lines), (ii) measurements where contact position varies from the nominal contact for a single standard only (alternately the 'Load', 'Short' and 'Thru', in legend), (iii) measurements with varied contact position on all standards ('All standards' in legend, pink lines). **Figure 2.15** shows a picture of the different contacts traces on the Load standard.

On the Load standard, a change in probe contact position changes both real and imaginary parts of the Load impedance (Z_{Load}). The change in its imaginary part is caused by a different series inductance term and explains the strong systematic deviation in $\mathrm{Im}(Z_{ref})$ observed from low frequency. The observed change in $\mathrm{Re}(Z_{Load})$ and subsequently in $\mathrm{Re}(Z_{ref})$ is more pronounced at higher frequencies, however determination of its origin would require more experiments.

Three clear trends in $\mathrm{Im}(Z_{ref})$ are observed, from low frequency to $\sim$ 45 GHz, (ii) from $\sim$45 to 80 GHz and (iii) beyond 80 GHz. While the low frequency-45 GHz trend is mostly influenced by a probe misplacement on the Load standard, due to its series inductance, the upper frequency trends cannot be entirely explained in the same way, and further investigation is needed to address these observations.

Changing the contact position on the Thru also has a significant impact on Z_{ref}, because the Thru standard is used to shift the reference plane from probe tips (where the Load model is defined) to the middle of the Thru (where the calibration equations are solved). Although the exact impact of the Thru

[8] The interested reader can find the same sensitivity analysis applied to SOLT calibration in **Appendix B**.

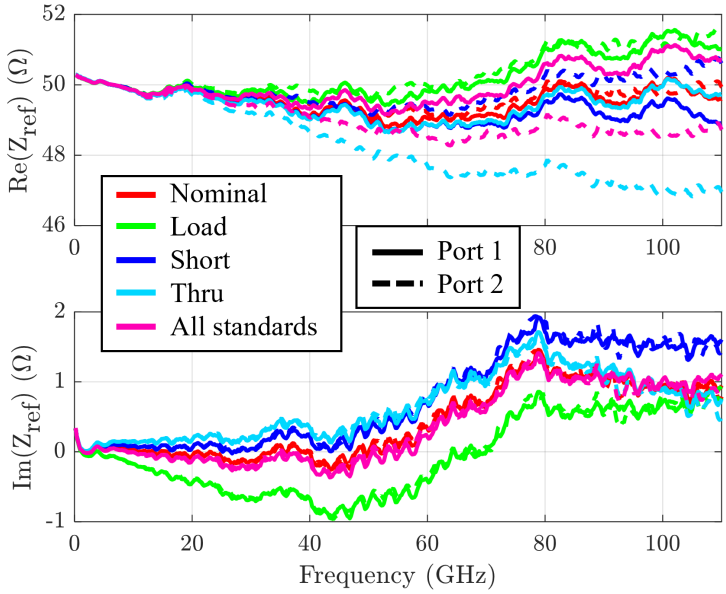


Figure 2.14: $Z_{ref1,2}$ of LRRM calibration with different left probe placement on pad. Nominal position on all standards measurements in red lines. Variation of probe position from nominal in only one standard measurement: green, blue, cyan lines. Variation of probe position in all standards measurements in pink lines.

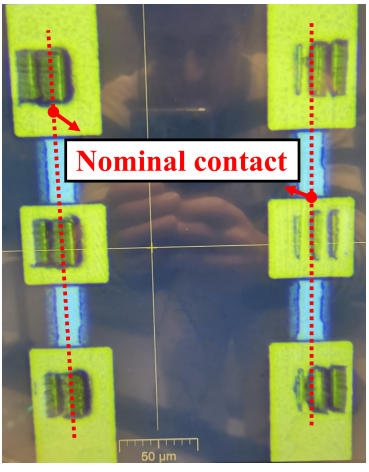


Figure 2.15: Picture of probed Load standard with different contact positions.

standard measurement on Z_{ref} is not straightforward and might vary from one LRM-type calibration method to another, additional measurements demonstrate that the absolute probe-to-probe distance on the Thru standard is not the only parameter affecting the extracted Z_{ref} for LRRM. Indeed, as evidenced in **Figure 2.16**, an asymmetry of the probe placement on the Thru induces a difference in extracted $Z_{ref,1}$ and $Z_{ref,2}$.

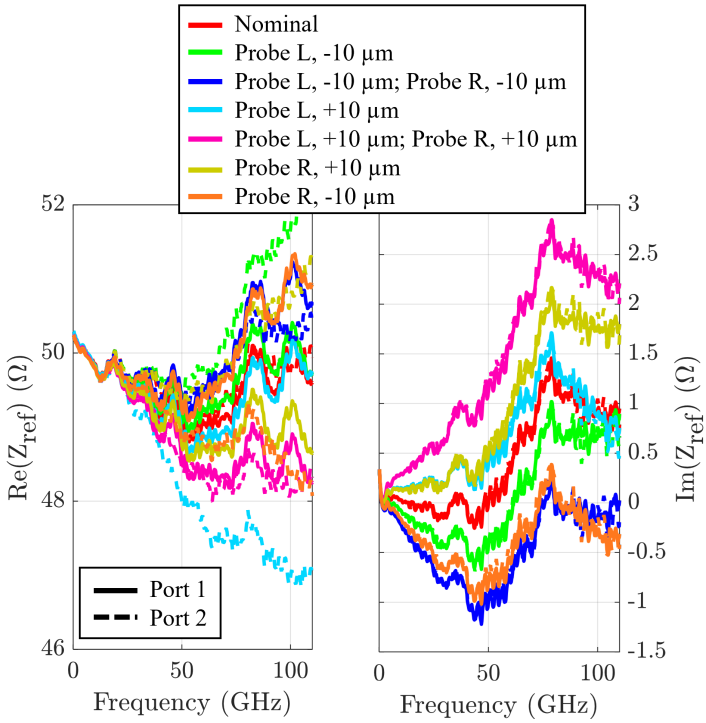


Figure 2.16: $Z_{ref1,2}$ of LRRM calibration with different probe placements on Thru standard measurements. Nominal position in red lines. A variation in left (L) or right probe (P) contact position is defined positive toward the center of the Thru.

Figure 2.16 shows extracted Z_{ref} with additional probe contact variations on the Thru standard. A variation in left (L) or right probe (P) contact position is defined positive toward the center the Thru. We clearly observe that for symmetric contacts (red, dark blue, pink), $Z_{ref,1} \approx Z_{ref,2}$, while for asymmetric contact $\mathrm{Re}(Z_{ref,1}) \neq \mathrm{Re}(Z_{ref,2})$. This result can interestingly be used to verify

symmetry in probe contact position on the Thru standard, which is not as easy to verify as opposed to the Open, Short and Load standards for which symmetric reflection coefficients obtained from a (m)TRL calibration guarantees a symmetric probe contact.

Previous work on the sensitivity of probe misplacement on calibration accuracy reported global calibration comparison errors of two data sets. Here we analyze probe misplacement impact on a specific parameter of the calibration, i.e. its reference impedance. We demonstrate for LRRM calibration that, while $\mathrm{Re}(Z_{ref})$ is mostly affected by probe misplacement on Thru standard, probe misplacement on all standards have an impact on $\mathrm{Im}(Z_{ref})$ of comparable order of magnitude.

A probe misplacement on the Thru standard for the mTRL calibration has very small impact on the extracted Z_{ref}, with variations up to $\pm(0.6 + j0.15)$ Ω (not shown). This could be expected as mTRL is sensitive to the difference in line lengths and not the absolute placement error on the Thru. With Line standard lengths longer 1 mm, an error of $\sim$10 µm in length difference is very small.

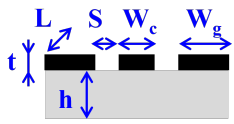
This sub-section has identified systematic deviations in Z_{ref} either due to the Load model or to probe misplacement for SOLT and LRRM calibrations taking mTRL as a reference. In the next part, we discuss the validity of the mTRL, with Z_c computed from [66, 67], to serve as a benchmark Z_{ref}.

2.5.3 Reference impedance of mTRL calibration

The mTRL method [55, 66], relying on fewer assumptions and on distributed standards is usually taken as reference calibration for high-frequency measurements. This calibration's reference impedance is defined by the Z_c of the Line standards. The Z_c is extracted from the measured γ and a constant C term [66] as $Z_c = \gamma/(j\omega C)$, assuming $G = 0$ and C is frequency-independent [67]. G and C are the per-unit-length shunt conductance and capacitance elements from the *RLGC* elements of a transmission line.

Description of measurement setup and calkits

In this second set of experiments, CPW lines (as well as a Short) are measured on commercial calibration substrates (AC-2 and 104-783A) and a custom-made calkit. Two types of 110 GHz, 100 µm pitch RF probes are used: MPI TITAN and FormFactor Infinity probes. The AC-2 and 104-783A substrates are placed on a ceramic chuck, whereas the custom calkit is placed on a metallic chuck.



	t	W_c	S	W_g	h
(µm)	2.24	42.7	25.6	210	700
L (mm)	0.1, 0.93, 1.43, 5.4				

Figure 2.17: Sketch and geometry of CPW lines on custom-made calkit. **Measured metal conductivity** $\sigma = 2.91 \times 10^7\,\mathrm{S/m}$.

The VNA, VNA settings and prober are the same as in the previous **Section 2.5.2**.

The custom-made calkit is fabricated in our cleanrooms and consists of 2.2 µm-thick CPW lines of a single aluminum metal layer patterned on top of an RFeSI 90^{TM} substrate **[82]**. The CPW lines cross-section is measured with a scanning electron microscope (SEM) and are summarized in **Figure 2.17**. Each structure is spaced by at least 1.5 mm in both x and y directions to reduce probe coupling with neighboring devices. The RFeSI 90 substrate consists of a 700 µm-thick very-low-loss silicon substrate (with $\rho_{\mathrm{Si}} > 1 - 10\,\mathrm{k\Omega\,cm}$) beneath a 200-400 nm-thick SiO_2 oxide. It is a commercial SOI wafer, from which the top Si film is removed.

Comparison of mTRL among different commercial calkits

To analyze the mTRL Z_{ref}, we start by comparing two mTRL calibrations made on different calibration substrates with the same probes. **Figure 2.18a** and **b** show the Z_{ref} of a first-tier mTRL calibration performed on the AC-2 substrate extracted from a second-tier mTRL calibration realized on the 104-783A substrate, all with TITAN probes. Equivalently, **Figure 2.18c** and **d** show the C and G terms extracted for the 104-783A CPW lines with the calibration comparison technique **[74]**, based on the first-tier mTRL calibration realized on the AC-2 substrate.

We observe a systematic deviation in both $C(f)$ and $G(f)$ (directly correlated to the extracted $\mathrm{Re}(Z_{ref})$ and $\mathrm{Im}(Z_{ref})$, respectively) of the 104-783A's lines that are in contradiction to the assumptions made to compute Z_c in the benchmark mTRL calibration procedure. Despite similar lines geometry in the two commercial calkits, some parasitic effect is present and violates the assumptions made to evaluate Z_c in at least one of the calkits, leading to a systematic error in Z_{ref} as shown in **Figure 2.18a** and (b) and consequently in the mTRL calibration.

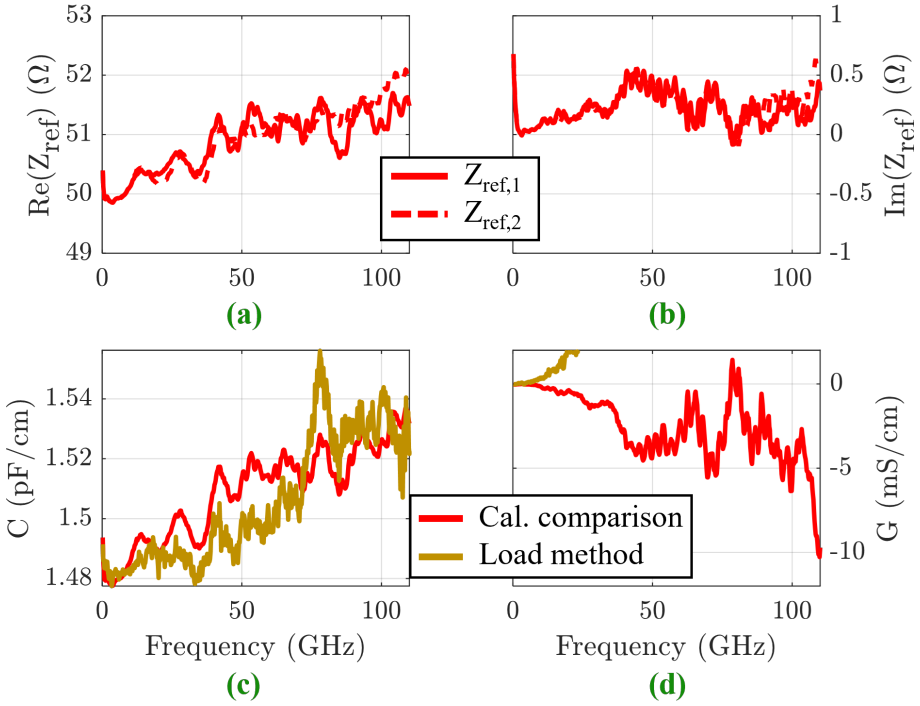


Figure 2.18: (a) and (b): Z_{ref} of mTRL on AC-2, evaluated on 104-783A substrate. (c) and (d): C and G of 104-783A's Lines evaluated from mTRL performed on AC-2 substrate and from the load method [67].

For further analysis, the C_{Load} and G_{Load} extracted from the load method [67] (i.e. assuming the Load is solely described by its dc resistance), measured on the 104-783A substrate, are shown in yellow lines. A frequency-dependent C_{Load} (extracted from the load method) can have two possible (non-exclusive) origins: either the real part of Z_{Load} is not entirely described by a resistance, or the 104-783A's CPW lines are dispersive and the C term of the lines is frequency-dependent.

The G term agrees well for both methods at low frequency, and its deviation is expected due to omission of a reactance part in Z_{Load} for the load method.

Having C_{Load} roughly constant up to ~ 40 GHz therefore suggests that the C term of the 104-783A lines is constant in that frequency range. So, the dc-40 GHz frequency-dependent C observed in Figure 2.18c from 104-783A's

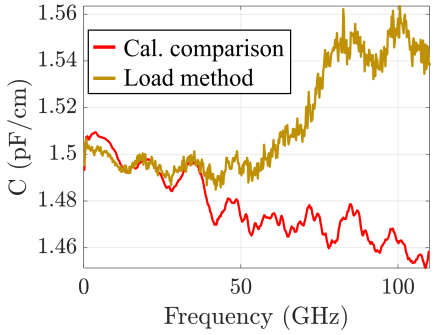


Figure 2.19: *C* of AC-2's Lines evaluated from mTRL performed on 104-783A substrate and from the load method **[67]**.

line measurements likely comes from a systematic error in $\mathrm{Re}(Z_{ref})$ of the first-tier mTRL AC-2 calibration that is related to *frequency-dependent C* of the AC-2 lines in that frequency range. For verification, let us show the opposite in **Figure 2.19**: the *C* term of the AC-2 lines extracted from a first-tier mTRL 104-783A calibration, along with the C_{Load} obtained from the load method applied to a Load standard measured on the AC-2 substrate.

Figure 2.19 shows also a roughly constant C_{Load} up to $\sim 40\,\mathrm{GHz}$. Actually both C_{Load} have a $\sim 1\,\mathrm{pF/cm}$ variation up to 40 GHz (from **Figure 2.18c** and **Figure 2.19**), which makes it difficult to identify the Lines from which (if there is one) substrate exhibit a slight frequency dependence on the *C* term.

Figure 2.18 shows that even the mTRL calibration can be affected by noticeable systematic errors in $\mathrm{Re}(Z_{ref})$ and $\mathrm{Im}(Z_{ref})$ due to the assumptions $G = 0$ and constant C. However, identification of the errors' origin requires measurements of a third substrate: the custom-made calkit that are presented in the following.

Comparison of mTRL reference impedance from different commercial calibration substrates with different probes on a custom-made calkit

Finally, let us compare the Z_{ref} extraction of three different first-tier mTRL calibrations made on commercial alumina substrates, based on a second-tier mTRL calibration performed on the custom calkit, see **Figure 2.20**. The first two calibrations are made with TITAN probes (i) on the AC-2 substrate (red lines) and (ii) on the 104-783A substrate (green lines). The third calibration is made with Infinity probes on the 104-783A substrate (blue lines). The CPW

line model from [64], based on the CPW geometry, is shown in dotted lines in Figure 2.20c and d. The substrate losses (described by G) are modeled by a single term representing conductive losses in the Si substrate extracted below 10 GHz where all measurements agree (more information is found in Chapter 3).

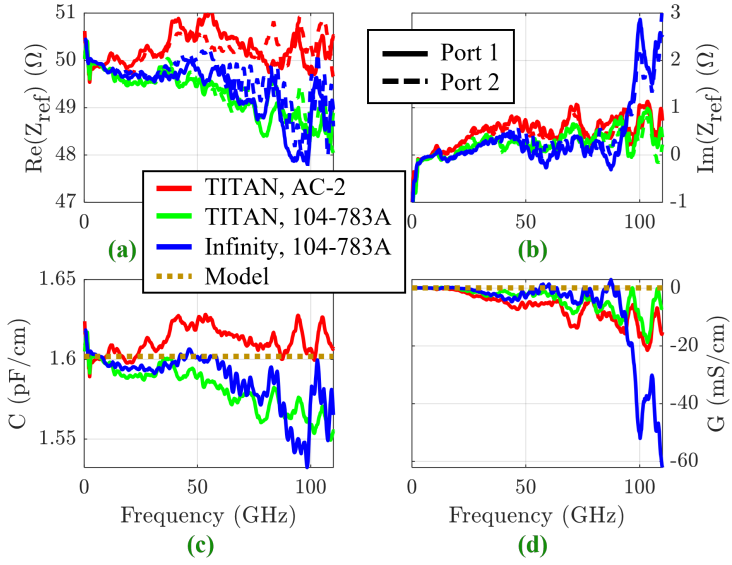


Figure 2.20: (a) and (b): Z_{ref} of first-tier mTRL on AC-2, 104-783A sustrates, with TITAN and Infinity probes, evaluated with a custom calkit. (c) and (d): per-unit-length C and G of the custom calkit lines evaluated from different first-tier mTRL. CPW line [64] model from measured dimensions in dotted lines.

From Figure 2.20, we can make several observations:

- there are noticeable differences according to the alumina substrate used for calibration;
- there are some residual calibration errors that are probe-dependent;
- these probe-dependent residual errors are present in both alumina substrates and the custom calkit.

In particular, the steady decrease in the C term (and $\mathrm{Re}(Z_{ref})$, mostly visible above 50 GHz) and a G term that is more consistent to the substrate loss model of [64] (almost lossless, so G and $\mathrm{Im}(Z_{ref})$ closer to 0) are specific to the 104-

783A calibration. Except for some bumps that are probe-dependent residual calibration errors.

Whereas for the calibration made on the AC-2 substrate, the C term is overall more constant, and the G shows a steadily decreasing negative value with frequency. The latter correlates well with a more positive value of $\mathrm{Im}(Z_{ref})$.

Finally, there is a sudden drop in G (increase in $\mathrm{Im}(Z_{ref})$) at 90 GHz observed for Infinity probes that is consistent with measurements of other lines on the same wafer and with other types of calibration. So, it is attributed to the probe coupling to the wafer of the custom-made calkit (thus again residual probe-dependent error).

Discussion

In **Figure 2.18**, we have seen systematic deviations in Z_{ref} and C and G terms that are in contradiction to the assumptions used to compute Z_c in mTRL calibration. In **Figure 2.20**, based on a separate calkit, we have seen two clear trends in Z_{ref} (or in $C(f)$ and $G(f)$) that depend on the calibration substrate, hence physical lines, used for calibration. The 104-783A trend is similar for measurements with both types of probes, which indicates that the systematic deviations are larger than probe-related residual error.

The slight increase and decrease in extracted $C_{Load}(f)$ up to 40 GHz (**Figure 2.20c** and **Figure 2.19**, respectively) on 104-783A and AC-2 substrates, respectively, are likely probe-dependent residual errors. Additional measurements with a different probe technology are needed for confirmation.

To help interpret these results, **Figure 2.21** shows the measured γ of CPW lines on different calkits, with different probes.

On the one hand, we observe more dispersion in the 104-783A lines than in the AC-2 lines (increase in normalized β(f) at high frequency). It implies an increasing $C(f)$ with frequency above $\sim$ 50 GHz for the 104-783A lines. That explains the steadily increasing $C(f)$ in **Figure 2.18c** and decreasing $C(f)$ trends (more pronounced above 50 GHz) in **Figure 2.20c** for calibrations on the 104-783A substrate. It also implies the frequency-independent C assumption in the benchmark mTRL calibration is less valid for the 104-783A calkit lines than the AC-2 lines, thus clearly introducing a systematic error in $\mathrm{Re}(Z_{ref})$ of 104-783A mTRL calibration.

On the other hand, we observe evident additional losses above $\sim$ 70 GHz in the AC-2 lines (stronger than for the 104-783A calkit), probably due to excessive radiation caused by the presence of a resistive layer under the CPW ground conductors and extending beyond them **[83]** (bump in α and $\varepsilon_{r,eff}$:

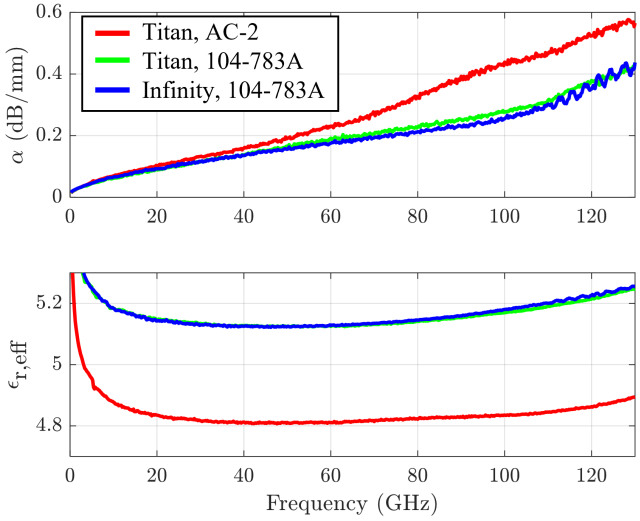


Figure 2.21: Measured propagation constant of the lines on different alumina substrates (AC-2 and 104-783A), with different probes. Top: propagation losses α, **Equation 2.7**. Bottom: effective permittivity sensed by the line, **Equation 2.9**.

(i) thicker 635 µm AC-2 substrate instead of 254 µm for 104-783A, (ii) wider resistive sheet for AC-2 than 104-783A substrate). These additional losses might wrongly be associated to series-branch losses (R term) when we assume $G = 0$ and thus cause a systematic error in $\mathrm{Im}(Z_{ref})$ of AC-2 mTRL calibration.

Finally, another aspect that has not been given any attention here is the fact that these alumina substrates feature non-zero dielectric losses. Indeed, typical values of dielectric losses are in the order of 1×10^{-4} at microwave frequencies **[84–86]**, and they contribute to non-zero G term.

Perspectives for systematic error reduction in mTRL calibration made on commercial calkit

For new calkit designs, accurate characterization of its standards is crucial and is usually realized with the calibration comparison technique. The accuracy of this technique (and subsequent results) relies on well-defined Z_{ref}. It is thus essential to identify a reference calibration with well-defined Z_{ref}.

We observed that SOLT, LRRM and mTRL calibrations have comparable

Z_{ref} up to $\sim 40-50$ GHz. We also showed that lumped-standard calibrations are very sensitive to probe misplacement, thus requiring accurate lumped standards characterization. Since mTRL is more robust to probe misplacement and does not require known electrical model for its standards, mTRL provides the most accurate Z_{ref} with least characterization effort, confirming its pertinence as reference calibration even in term of Z_{ref}.

However, measurements of two commercial calibration substrates have shown that mTRL Z_{ref} also suffers from systematic errors linked to violation of the assumptions $G = 0$ and frequency-independent C line terms either due to radiation or dispersion. Here, we will discuss about potential methods to reduce the systematic errors made in mTRL calibration on commercial calibration substrates.

It should be noted as well that the commercial substrate results presented here come from measurements for which the commercial substrates lay on top of a thick ceramic chuck. Such boundary condition has proven to yield the best CPW line measurement results and reduced high-order mode impact, compared to the substrate (i) on top of an absorber, (ii) on top of a metallic chuck, (iii) suspended in the air **[87]**.

So, another way to evaluate the characteristic impedance of commercial substrate transmission lines is primordial to enhance the mTRL calibration. That could be achieved either numerically or experimentally.

There have been several numerical methods to properly evaluate Z_c when radiation is present:

- Equation-based modeling, such as the one presented in **[88]** for a conductor backed CPW line with finite ground planes.
- Quasi-analytical tool, a software tool developed in **[89]** that enables fast characterization of dynamic phenomena of a wide variety of transmission lines[9].
- 3D EM simulations, with the procedure described in **[78]** for instance.

Alternatively (or complementary), if lack in knowledge of exact materials or dimensions used in commercial calibration substrate lines prevents the accurate determination of Z_c based on the above numerical methods, the calibration comparison technique can still be used. In that case, a custom calkit can be specifically designed to reduce radiation effects and be used as reference. **[90]**

[9] The tool is available for free download at `http://terahertz.tudelft.nl/Research/project.php?id=74&ti=27`

provides general guidelines for calkit design with reduced parasitic modes up to 325 GHz. A summary of the guidelines are

- Use a chuck dielectric material with permittivity close to or larger than the calibration substrate. Such an interface condition theoretically does not support surface wave modes[10], and, in practice, an actual mTRL accuracy improvement has been observed.
- If not available, surface waves will be excited along the substrate, which will induce radiation loss and dispersion. According to the chuck material (metallic or dielectric), the first substrate mode to be excited[11] is either TM_0 (metallic chuck) or TE_0 (dielectric chuck). The critical frequency (when energy from the nominal CPW mode starts leaking in the un-wanted modes) is a function of substrate permittivity (ε_r), thickness (h) and total CPW width ($W_{\text{tot}} \equiv W_g + S + W_c + S + W_g$). These parameters should be selected such that the critical frequency of the first un-wanted mode is beyond the calkit frequency range.
  - For a metallic chuck, first higher-order mode critical frequency:

$$f_{\text{Metal}} = \frac{\arctan(\varepsilon_r)}{\pi h \sqrt{2\mu_0\varepsilon_0(\varepsilon_r - 1)}} \tag{2.47}$$

  - For a dielectric chuck, first higher-order mode critical frequency:

$$f_{\text{Dielectric}} = \frac{2}{W_{\text{tot}} \sqrt{2\mu_0\varepsilon_0(\varepsilon_r - 1)}} \tag{2.48}$$

- Even with these precautions, radiation and dispersion still occurs in CPW lines on top of semi-infinite substrates [92]. Dispersion and radiation loss are minimized for narrower CPW line inner cross-section ($S + W_c + S$), in a similar way as a slot mode (from ground to ground conductor) in an antenna aperture [91].

Although reducing the CPW cross-section reduces radiation and multimode propagation in general, it is limited to the physical dimensions of the probes,

[10] Parasitic substrate modes TE_n and TM_m are also called surface waves, because the field strength of these modes propagating inside the substrate falls off exponentially outside the dielectric [91].

[11] TE_0 and TM_0 modes have no cutoff frequencies, they can occur at any frequency. However, there is a critical frequency at which the CPW mode will leak energy in these modes, i.e. when these un-wanted modes' propagation constant is larger than the CPW mode propagation constant [91].

which do not reduce with higher operating frequencies. The probe pitch limits the ground width and the probe tips trace width limits the central conductor width and spacing to ground [12] . The use of larger pads with a transition to narrower line cross-section could be used only if the dut lies within the same substrate, with the same access. Performing a probe-tip calibration that can serve as a reference to characterize other calkits standards cannot be accurately performed on standards having a pad transition, as this transition adds uncertainty when moving the reference plane calibration to the probe tips.

The custom-made calkit presented in **Section 2.5.3** meets the criteria specified above. When measured on the metallic chuck, $f_{\text{Metal}} = 43\,\text{GHz}$, but if it is measured on the ceramic chuck, $f_{\text{Dielectric}} = 252\,\text{GHz}$. Furthermore, two other sets of lines with narrower cross-section exist on the same substrate. The set described in **Section 2.5.3** is called 'set Dh' . The lines with narrowest cross-section could not be measured with TITAN probes, because of the large tips trace width, but they have been measured with Infinity probes. The cross-section dimension of this set of lines (called 'set Ch') are $t = 2.22\,\mu\text{m}$, $W_c = 23.5\,\mu\text{m}$, $S = 13.7\,\mu\text{m}$, $W_g = 108\,\mu\text{m}$. For this 'set Ch', $f_{\text{Dielectric}} = 483\,\text{GHz}$.

Furthermore, TE_0 and TM_0 are not the only parasitic modes generating radiation loss and dispersion (there is also the 'slot mode' described above that depends on the inner CPW cross-section dimensions). Indeed, for the same measurement conditions, on a metallic chuck, where the critical frequency (**Equation 2.47**) does not depend on the total CPW cross-section, we observe more dispersion in $\varepsilon_{r,eff}$ for the 'set Dh' lines (with wider inner CPW cross-section) than the 'set Ch', cf. **Figure 2.22**.

This custom-made calkit seems promising to be used as a reference calibration to accurately evaluate the Z_c of commercial substrate transmission lines. Some un-wanted effects are still present: strong $\text{Im}(Z_{ref})$ deviation above 90 GHz in **Figure 2.20**), ripple (that could probably be reduced if measured on top of a ceramic chuck, it is discussed later in **Section 3.5.2**), and further characterization or simulation-based work is needed to understand their origin. Nevertheless, present measurements seem to be behaving rather well up to 90 GHz, indicating its potential validity up to 90 GHz at least.

[12] Example of prove tips traces are shown in **Figure 2.15** for the TITAN 100 µm-pitch probes.

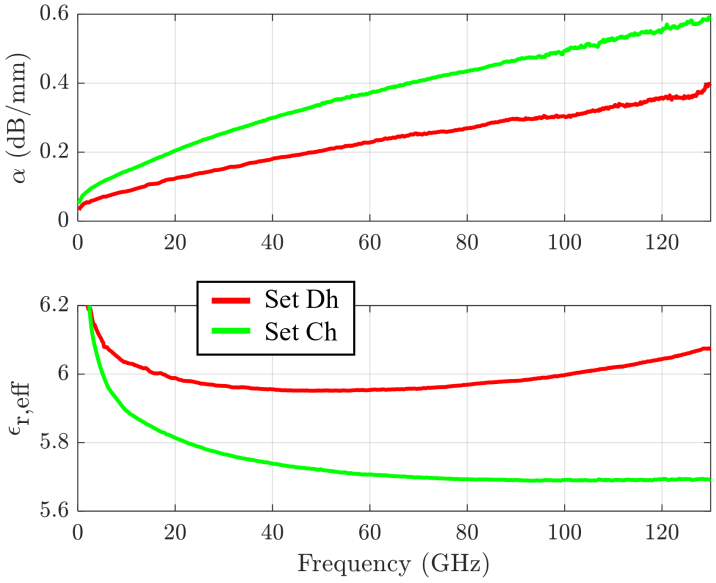


Figure 2.22: Measured propagation constant of the CPW lines from 'set Ch' (green, $W_c + 2S = 50.9\,\mu m$) and 'set Dh' (red, $W_c + 2S = 93.9\,\mu m$) from the custom-made calkit. Top: propagation losses α, **Equation 2.7**. Bottom: effective permittivity sensed by the line, **Equation 2.9**.

2.6 Conclusion

First, a brief summary of on-wafer measurements is presented. Covering wide aspects, from S-parameters definition to VNA introduction and reminder of common measurement calibrations and their associated error box model, this first chapter aims at setting the ground for the remaining of this thesis, in which a lot of characterization work has been performed. In particular, a special focus is given to transmission lines, as they are extensively characterized in the following chapters.

A distinct section is therefore devoted to the multiline TRL method, being the reference calibration and extracting transmission line parameters with high accuracy. The theoretical framework of mTRL is described and is used to explain the accuracy limitations of the method. A series of recommendations are provided to determine the length of the Lines standards in the design of a new calibration kit.

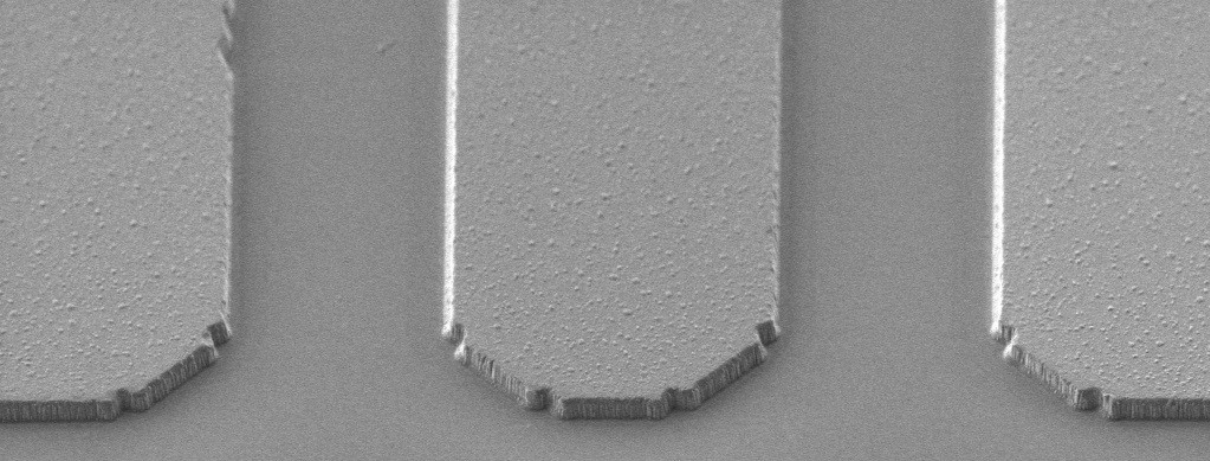
Then, several methods to extract the characteristic impedance of transmis-

sion lines are presented: (i) extraction from the measured propagation constant and (ii) calibration comparison technique. Both methods rely on some assumptions, i.e. for (i): $G = 0$ and frequency-independent C (from per-unit-length *RLGC* line parameters), for (ii): well-defined reference impedance of first-tier calibration.

The verification and identification of a well-defined calibration reference impedance is performed in the last part of this chapter. A method to extract Z_{ref} is described. Its application to SOLT and LRRM calibrations have shown that Z_{ref} is very sensitive to probe misplacement on Load and Thru standards. Thanks to the better robustness of mTRL in terms of probe misplacement and not requiring known (or previously characterized) electrical model for its standards, the mTRL calibration is identified as the reference calibration method providing a reliable Z_{ref}.

However, the application of mTRL calibrations on different substrates have shown that even its reference impedance suffers systematic errors. Indeed, the assumptions *per-unit-length* $G = 0$ *and frequency-independent* C used to evaluate the Z_c are not correct on the two tested commercial substrates (AC-2 and 104-783A), because of non-negligible dispersion and radiation. As a consequence, systematic errors are still present in mTRL calibration performed on such commercial substrates and are thus propagated when measuring the dut.

Several perspectives to improve the Z_c evaluation of commercial substrate transmission lines are discussed. Complementary to advanced numerical evaluation of Z_c that includes surface wave radiation and higher-order mode excitation, a custom-made calkit to define a proper reference calibration becomes essential for high-accuracy, high-frequency measurement. Preliminary measurements of a custom calkit fabricated in 2 µm-thick aluminum layer on top of a very low-loss Si substrate yield promising results for a reference calibration up to, at least, 90 GHz.



3. Small-Signal Extraction of Low-Level Substrates Losses

As explained in **Chapter 1**, in SOI-based ICs, the active and passive devices are fabricated on top of a dielectric (buried oxide, or BOX, in silicon dioxide), laying above a handle silicon substrate. This physical separation has enabled co-engineering the active and back-end of line (BEOL) regions, in parallel to the substrate. Today's commercial success of PD-SOI technology is due to significant technological improvement made at both the transistor level and at the level of the substrate **[3]**.

Indeed, the electrical properties of the substrate have a strong impact on device and circuit performance. Especially at RF and mm-wave frequencies, where capacitive coupling through the thin BOX becomes negligible compared to the substrate impedance sensed by the electric fields from overlaying devices. According to the substrate nature, it can induce significant losses and strongly impact the values of parasitic coupling elements.

A thick back-end of line can partly make up for the substrate's influence by using the lower metal layers to shield the interconnects and passive devices from the substrate parasitic effects. This gives rise to lines and passives of acceptable quality (though usually high capacitance), but some designs remain a challenge under these constraints, notably spiral inductors, transformers and transmission-lines at mm-wave frequencies **[26–28, 93]**.

Without careful substrate considerations, losses, coupling and linearity issues of key RF blocks can easily be dominated by the substrate's properties

[3, 94].

The first substrate alternative to standard resistivity (std) Si substrate that has been introduced is the high-resistivity (HR) Si substrate. The resistivity of semiconductors is by nature dependent on the local electric field (and we call this the field-effect). Low-doped, high-resistivity substrates are particularly field-sensitive, and it is typical for the semiconductor volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer. The most common parasitic fields originate from fixed charges (usually positive in Si/SiO_2 heterostructures) that are present at the insulator/semiconductor interface (PSC effect). Other parasitic fields come from non-zero biased signal lines in the back-end of line. Altogether, these parasitic fields induce a (potentially) highly conductive channel-like layer beneath the insulator, as depicted in **Figure 3.1**, for the case of a low-doped HR substrate.

These fixed oxide charges (represented '+' symbols in **Figure 3.1**), are inevitable in the IC fabrication process, and induce free electrons at the interface in very high concentrations, locally lowering the resistivity beneath the circuits by a factor of 10^3 to 10^6. This, in turn, lowers the sensed resistivity by a factor of 10 to 10^4, to values as low as $1\,\Omega$cm. This is referred to as the parasitic surface conduction (PSC) effect that strongly mitigates the performance expected from a HR substrate as compared to standard-doped silicon ($\rho_{nom} \approx 10\,\Omega$cm) [95]. A way to yield the substrate field-effect-independent at the Si-BOX interface has thus become crucial for SOI wafers, in order to effectively meet the IC-level needs of low substrate losses and low substrate-induced harmonic generation.

Several techniques have been developed, in particular the trap-rich substrate solution [11] that has been widely commercialized in PD-SOI technology [1]. Other innovative solutions have been created that either outperform trap-rich Si substrates [17] or target other technologies not fabricated with trap-rich substrates, e.g. FD-SOI technology [18, 19].

All these developments have needed some characterization work to assess the small- and large-signal performance of such SOI substrates, under various conditions: bias application, temperature sensitivity, electrical field depth penetration [21, 32, 33, 96].

The surface nature of the field-related loss in SOI wafers prevents the use of dielectric-based methods [23, 97, 98], being the reference method for low-loss dielectric electrical properties characterization. This has led to the introduction of the *effective resistivity* (ρ_{eff}) to evaluate small-signal substrate performance

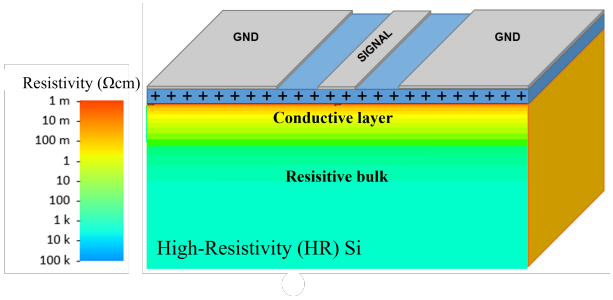


Figure 3.1: Schematic representation of a high-resistivity Si substrate with a CPW line on top. A representative profile of the local resistivity is given inside the substrates with the scale present on the left. Fixed charges (in '+' symbols inside the BOX) attract free carriers at the Si-oxide interface inducing a thin conductive layer that mitigates the benefits of HR substrates.

[22]. It has served as a metric that can be related to interconnects losses, passive quality factors and substrate noise coupling [16, 28, 74]. Throughout the rest this thesis, the effective resistivity will be considered as a figure of merit (FoM) describing substrate-related conductor loss of RF substrates. This chapter, in particular, focuses on this FoM.

The first part of this chapter introduces the definition of the effective resistivity and analyzes its sensitivity to systematic errors. It is shown that even small systematic errors can lead to strong evaluation error or misinterpretation of substrate losses in the case of a low-loss substrate. The rest of this chapter proposes different methods and procedures to better characterize substrate losses of substrates exhibiting a large variety of loss levels. The second part presents a method to correct systematic errors in the extraction of substrate losses from CPW line RF, dc and geometry measurements. Then, another procedure is provided to more accurately characterize very low-loss substrates. These two methods are applied to CPW line measurements on a wide variety of silicon substrates to demonstrate their limitations and successful applications. Finally, prospects to further enhance the measurement accuracy of low-loss substrates at mm-wave frequencies and beyond are discussed.

3.1 Extraction Procedure of Effective Resistivity

The per-unit-length *RLGC* representation of a transmission line described in **Chapter 2** is the starting point in the effective resistivity extraction procedure. Indeed, the *G* and *C* terms describe the admittance of the transmission line cross-section, which is of particular interest for substrate characterization.

3.1.1 Effective resistivity definition

In general, the semiconductor region of a typical metal-oxide-semiconductor stack is characterized by a space-dependent resistivity (ρ(x,y)). A typical example of non-homogeneous structure with space dependent resistivity is shown in **Figure 3.1**, with a HR substrate. To characterize the overall performance of this material stack with regard to the performance of overlying RF and mm-wave passives, it is convenient to equate this material stack to an equivalent effective substrate (**Figure 3.2**) of uniform effective relative permittivity ($\varepsilon_{r,sub,eff}$[1]) and uniform effective resistivity (ρ_{eff}).

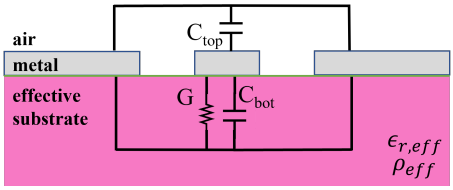


Figure 3.2: Cross-section of a CPW line on top of an effective uniform substrate.

In this equivalent effective structure, the per-unit-length shunt capacitance *C* is the sum of a top contribution (C_{top}), including the metallization thickness, and a bottom contribution (C_{bot}) from the effective substrate. They are expressed as the product of the medium permittivity and a geometry factor (F_{top}, F_{bot}) that depends on the CPW cross-section dimensions, such that

$$C_{top} = \varepsilon_0 \varepsilon_{r,top} F_{top}, \tag{3.1}$$

$$C_{bot} = \mathrm{Im}(Y_{bot})/\omega = \varepsilon_0 \varepsilon_{r,sub,eff} F_{bot}, \tag{3.2}$$

[1] Be careful to not confuse with the effective permittivity $\varepsilon_{r,eff}$ defined in **Equation 2.9** from **Chapter 2**. The latter ($\varepsilon_{r,eff}$) is defined as the relative permittivity of a fictitious medium *entirely surrounding the transmission line*, so applicable to any type of (TEM-mode-propagating) transmission line. The former ($\varepsilon_{r,sub,eff}$) is defined as the relative permittivity of a fictitious substrate *under a CPW line*.

where $\varepsilon_{r,top}$ is the relative permittivity of the top medium and Y_{bot} is the equivalent admittance of the bottom structure. The geometry factors (F_{top} and F_{bot}) account for the field distribution among the top and bottom parts and are computed by accurate closed-forms analytical expressions formulated in **[64]**. Assuming no losses in the top medium (air in this case), the shunt conductance is given by

$$G = \mathrm{Re}(Y_{bot}) = \frac{F_{bot}}{\rho_{eff}}, \tag{3.3}$$

$$\rho_{eff} \equiv \frac{F_{bot}}{G}. \tag{3.4}$$

This expression for ρ_{eff} is equivalent to the original definition of the effective resistivity given in **[22]**, which is

$$\rho_{eff} \equiv \frac{qC_0}{\varepsilon_0 G}, \tag{3.5}$$

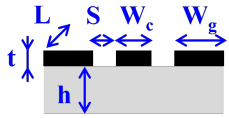
and can be derived from **Equation 3.4** by defining q and C_0, as the filling factor and the air-filled capacitance, respectively. They are related to the top and bottom geometry factors by

$$C_0 \equiv C|_{\varepsilon_{r,top}=\varepsilon_{r,sub,eff}=1} = \varepsilon_0(F_{top} + F_{bot}), \tag{3.6}$$

$$q \equiv \frac{F_{bot}}{F_{bot} + F_{top}}. \tag{3.7}$$

The *effective resistivity* computed from **Equation 3.4** *accounts for all shunt RF losses* (not series metallic losses) *present in the non-uniform structure*, originating from some real component of the shunt admittance $\mathrm{Re}(Y_{bot})$. The term resistivity is used, because these RF losses are *interpreted as conductive losses* in the substrate. Keeping in mind that interpretation, the effective uniform resistivity and permittivity strongly decay with increasing frequency in the low frequency range, because the slow-wave mode is still dominant[2]. Then, they are expected to reach a plateau and remain constant at higher frequencies.

[2]Frequencies at which the resistive nature of the substrate dominates its capacitive nature. Such slow-wave mode, when referring to the structure from **Figure 3.2**, occurs for frequencies below the majority carriers relaxation frequency, which depends on the substrate permittivity and resistivity: $f_{c,sub} = 1/(2\pi\rho_{sub}\varepsilon_{sub})$. For standard resistivity ($\rho_{Si} = 10\,\Omega\mathrm{cm}$) Si substrate, $f_{c,sub} = 15\,\mathrm{GHz}$. For a $10\,\mathrm{k}\Omega\mathrm{cm}$ HR resistivity Si substrate, $f_{c,sub} = 15\,\mathrm{MHz}$.



	t	W_c	S	W_g	h
(µm)	2.22	23.5	13.7	108	700
L (mm)	0.68, 0.93, 1.23, 1.53, 1.83, 2.43, 3.4, 8.35, 15.05				

Figure 3.3: Sketch and geometry of CPW lines measured in **Section 3.1.2**. No transition from pad to line. **Measured metal conductivity** $\sigma = 3.3 \times 10^7\,\mathrm{S/m}$.

However, this is not necessarily observed in practice, mainly for substrates having a high effective resistivity. As it will be explained in the following, two potential reasons for this unexpected decay of effective resistivity are identified: (i) a misestimation of the transmission lines characteristic impedance (Z_c) and (ii) the presence of additional non-conductive losses in our samples.

3.1.2 Sensitivity of effective resistivity to calibration

As we have seen in **Chapter 2**, the characteristic impedance extracted with the calibration comparison method is strongly correlated to the reference impedance of the first-tier calibration (often made on a commercial calibration substrate). However, the calibration reference impedance is prone to systematic errors either due to user manipulation, e.g. wrong probe placement on standards strongly affects Z_{ref} in SOLT and LRM-type calibrations, or due to invalid assumptions made in the calibration algorithm, e.g. invalid electrical models of lumped standards in SOLT and LRM-type calibrations or non-dispersive and non-radiative lines in mTRL calibration. Such systematic errors have a strong impact on effective resistivity extraction for low-loss substrates.

To illustrate this, we show the ρ_{eff} extraction using **Equation 3.4**, from CPW line measurements on the RFeSI90$^{\mathrm{TM}}$ wafer described in **Section 2.5.3**. The CPW geometry dimensions are given in **Figure 3.3**. The CPW lines are measured from 0.2 to 130 GHz, with 100 µm-pitch Infinity I110 probes on a metallic chuck.

Several first-tier LRRM calibrations are compared. The mTRL calibration is used as a benchmark (with Z_c extracted from the load method **[66, 67]**). The Load standard is modeled by a series $R_{Load} = 50.13\,\Omega$ and a series $L_{Load} = -3.3\,\mathrm{pH}$, characterized from dc measurements and mTRL calibration, respectively. To illustrate the systematic error made due to probe misplacement during calibration, we propagate the error from several first-tier LRRM

calibrations for which the L_{Load} is varied from -0.3 to -6.3 pH, based on the same raw measurements of the Load standard. Such variations correspond to probe misplacement on the Load standard by $\sim\pm 10\,\mu$m. As we have seen in the previous chapter that $\mathrm{Im}(Z_{ref})$ (thus $\mathrm{Im}(Z_c)$) is most sensitive to an error in Load misplacement due to different series inductance values below 40 GHz, such variation should be representative of a common manipulation error.

The extracted characteristic impedance and ρ_{eff} are shown in **Figure 3.4**. We observe a strong deviation in Z_c from one first-tier calibration to another, starting from frequencies as low as ~ 6 GHz (especially for $\mathrm{Im}(Z_c)$). We also observe a steep change in frequency behavior for Z_c above 90 GHz. This was already observed in **Section 2.5.3** with Infinity probes. It might be related to probe-dependent residual error, but it will not be investigated here. So, we will only focus on the lower frequency behavior.

The extracted effective resistivity is not behaving as expected for conductive-only shunt substrate losses (ρ_{eff} should be constant with frequency above a few tens of MHz). The graph of $\rho_{eff}(f)$ is in log scale, so negative values are not displayed. It is more convenient to analyze the substrate loss in terms of G in such a case.

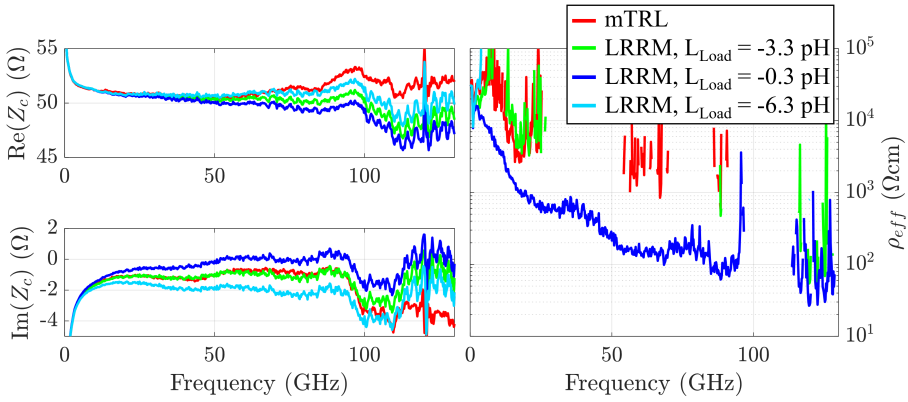


Figure 3.4: Extracted characteristic impedance (a) and effective resistivity (b) of measured CPW lines, for different first-tier calibrations.

The extracted *RLGC* line parameters are shown in **Figure 3.5**, along with the *RLGC* parameters calculated with Heinrich model from measured CPW

geometry (and metal conductivity). There several interesting observations to note[3].

- There is a *strong deviation* in R and G among the different LRRM methods above ~ 6 GHz due to a misestimation of the L_{Load} term, or equivalently, to a *probe misplacement in the standards during first-tier calibration*.
- There is some low-periodicity (bumps at ~ 40 GHz and 80 GHz) ripple in measurements that induce a systematic $G < 0$ in the reference mTRL and nominal LRRM calibrations. Because of it, evaluating very low level of substrate loss becomes inaccurate above ~ 20 GHz. Its origin is likely probe-dependent (probe-calkit-dependent as it varies from one test substrate to another) residual error and will not be discussed here, but a broader discussion over the accuracy limits of the overall extraction method is provided at the end of this chapter, in **Section 3.5**.
- The *RLGC* terms evaluated with Heinrich model based on scanning electron microscope (SEM), profiler and dc measurements show a very close fitting to the ones extracted from reference measurements, in particular R below 20 GHz.

As demonstrated above, extracting very low level of substrate losses is really challenging because of systematic errors present in high-frequency measurements, either due to user manipulation error (during calibration) or due to residual errors. Even though user-related systematic errors could be reduced to a minimum with a sound measurement procedure[4], even a small amount of uncertainty on the first-tier calibration, for instance on the assumption that $G = 0$ as discussed in **Section 2.5.3**, still leads to significant error in the G evaluation of low-loss substrates. A way to deal with such systematic errors is crucial for high-frequency extraction of low levels of substrate losses. The next section presents a method to correct for potential systematic errors in measurements.

[3] Although not relevant to the discussion here. We can also note that the C term is not constant from the mTRL extraction. We observe a deviation above ~ 60 GHz, whereas the nominal ($L_{Load} = -3.3$ pH) LRRM yields a frequency-independent C up to 90 GHz. This is in agreement with the observations made in **Section 2.5.3** that dispersion is observed in the 104-783A calibration substrate lines.

[4] mTRL calibration was demonstrated in the previous chapter to yield the most reliable Z_{ref}, even in case of probe misplacement. However, LRM-type method could also be used provided the Load and Thru standards are characterized. A procedure for their characterization and to achieve an accurate LRRM calibration is described in **Appendix B**.

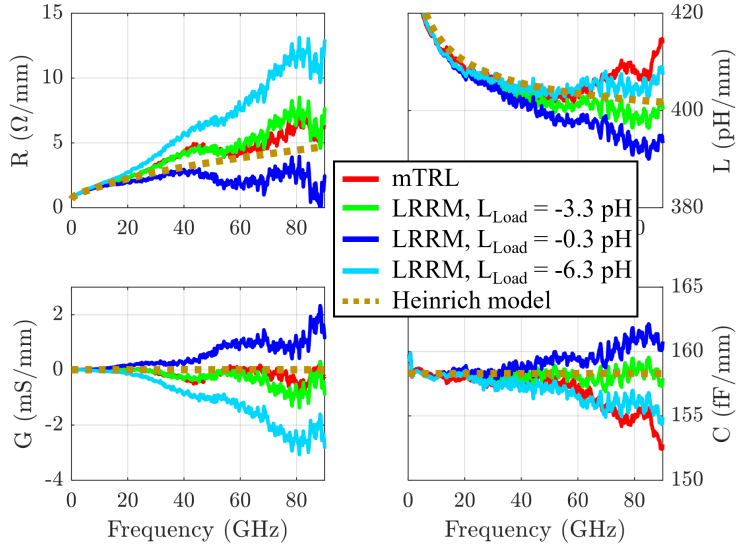


Figure 3.5: Extracted *RLGC* parameters of the measured CPW lines, for different first-tier calibrations. Heinrich model based on geometry and dc measurements (dotted yellow lines).

3.2 The R-based Correction Method

Let us first analyze the sensitivity of the G term to the transmission line Z_c, in particularly to its imaginary part. Based on this observation, we propose a correction method to compensate for its misestimation. This work was first presented in [99], then extended in [34].

3.2.1 Sensitivity analysis of the extracted characteristic impedance

A transmission line is fully described by two complex parameters, i.e. its characteristic impedance and its propagation constant. While the multiline TRL algorithm [55] gives the value of γ in an accurate manner, as we have just seen, the estimation of Z_c is more prone to errors. Targeting the extraction of substrate properties, it is necessary to express γ and Z_c in terms of the *RLGC* line elements. For low-loss transmission lines ($R \ll j\omega L$ and $G \ll j\omega C$), Equation 2.1 and Equation 2.2 become

$$Z_c \approx \frac{L}{C} + j\frac{1}{\omega C}\left(\sqrt{\frac{L}{C}}\cdot\frac{G}{2} - \sqrt{\frac{C}{L}}\cdot\frac{R}{2}\right), \tag{3.8}$$

and ($\gamma = \alpha + j\beta$)

$$\alpha \approx \frac{\mathrm{Re}(Z_c)G}{2} + \frac{R}{2\mathrm{Re}(Z_c)}, \tag{3.9}$$

$$\beta \approx \omega\sqrt{LC}. \tag{3.10}$$

These equations can be reversed in order to evaluate G and R:

$$G \approx \frac{1}{\mathrm{Re}(Z_c)} \cdot (\alpha + \omega C \cdot \mathrm{Im}(Z_c)), \tag{3.11}$$

$$R \approx \mathrm{Re}(Z_c) \cdot (\alpha - \omega C \cdot \mathrm{Im}(Z_c)). \tag{3.12}$$

Here, the second term of the products plainly shows that an (under-) over-estimation of $\mathrm{Im}(Z_c)$ has the effect of (over-) under-estimating R and (under-) over-estimating G. Indeed, as stated above, the *total loss* α *is accurately evaluated* by the mTRL approach. So, *an error in the extracted* $\mathrm{Im}(Z_c)$ *induces an error in the allocation of this total loss to the series metallic R term and to the shunt substrate G term.*

This is in complete agreement with the observations made from **Figure 3.4** and **Figure 3.5**. We see, for instance, that an overestimation in $\mathrm{Im}(Z_c)$ (toward positive value, dark blue line), under-estimates R and over-estimates G. Furthermore, a sensitivity analysis carried out in **[34]** shows that a relative uncertainty in $\mathrm{Im}(Z_c)$ is the main contributing factor to relative variations in R and G. Since $\mathrm{Im}(Z_c) \approx 0$, a small absolute error in $\mathrm{Im}(Z_c)$ leads to strong evaluation error of G, thus in substrate loss. Therefore, *an accurate evaluation of* $\mathrm{Im}(Z_c)$ *is crucial to a meaningful extraction of the substrate losses.*

3.2.2 Description of the correction method

A new procedure to *correct* the imaginary part of Z_c is proposed here. First, an existing Z_c extraction method is used to compute the terms L and C (from **Equation 2.4** and **Equation 2.6**), which only depend on β and the real part of Z_c in the low-loss transmission line approximation. From this first extraction, that we shall label as '1', reliable values for C_1 and L_1 are obtained. Ultimately, we are interested in extracting a reliable value of G toward substrate electrical characterization. But, as we have seen, it is difficult to evaluate $\mathrm{Im}(Z_c)$ with sufficient precision for series losses R_1 and shunt losses G_1 to be well discriminated, and this is especially true for high-quality substrates (low G), and at high frequencies. We therefore propose the *R-based method*, by which we assume

that R is perfectly known over the entire frequency range. In practice, R_{forced} is set by the closed-form analytical expressions from Heinrich model [64], and G_{corr} is computed using

$$G_{\text{corr}} = -\omega C_1 + \frac{\gamma^2}{R_{\text{forced}} + j\omega L_1}. \tag{3.13}$$

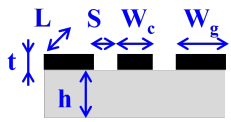
It is important to note that this method is no longer a pure measurement extraction technique, as R_{forced} is now an input to the extraction, and must be accurately known for meaningful results. In general, we found that knowing the metal dimensions along with its conductivity permits a fairly accurate estimation of R_{forced}. Nevertheless, the value of R_1 from the initial extraction is trusted up to at least $\sim 6\,\text{GHz}$, even in the presence of significant user-related systematic error, as it was observed above in Figure 3.5. Therefore, if an uncertainty in the metal dimensions or conductivity still persists, a fine tuning of one of these parameters can be performed to ensure a good agreement of R_{forced} with R_1 at low frequency.

In practice, only the real part of Equation 3.13 is taken just to ensure that we have a real value for G, the imaginary part of the right-hand side of Equation 3.13 is negligible (at least 2 orders of magnitude lower than the real part). As it was stated in Section 2.4.1, both Liu's [74] or Lucas' [73] methods provide meaningful extractions and can be used to evaluate L_1 and C_1.

Let us see its application to CPW line measurements of a different wafer. CPW lines are fabricated on top of a trap-rich (TR) SOI wafer (fabricated in our cleanrooms) are measured from 10 MHz to 67 GHz using a pair of 100 µm-pitch GSG Infinity probes (I67) from FormFactor. An mTRL calibration is performed on a 101-190C calkit as first-tier calibration. In a second setup, the lines are measured from 140 to 220 GHz with a pair of 100 µm-pitch Infinity probes, with a first-tier LRRM calibration. The CPW lines are fabricated with a 910 nm-thick aluminum layer, and their dimensions, that were measured using a precision profiler, are described in Figure 3.6. An Open structure, a Thru and two Lines of different lengths are measured.

Figure 3.7 shows the characteristic impedance as well as the series metallic loss (R) and shunt substrate loss (G), using the calibration comparison technique and the correction with the R-based method.

As we can see from the upper frequency range measurement (140-220 GHz), $\text{Im}(Z_c)$ strongly oscillates. It is hard to extract meaningful substrate losses (even large substrate losses) from such large variations in uncorrected $\text{Im}(Z_c)$. That



	t	W_c	S	W_g	h
(µm)	0.91	22.5	12.1	155	500
L (mm)	0.1, 2.1, 8.1				

Figure 3.6: Sketch and geometry of CPW lines measured in **Section 3.2**. Pad to line transition of 93 µm, not included in the line lengths in the table. *Measured metal conductivity,* $\sigma = 3.16 \times 10^7\,\mathrm{S/m}$.

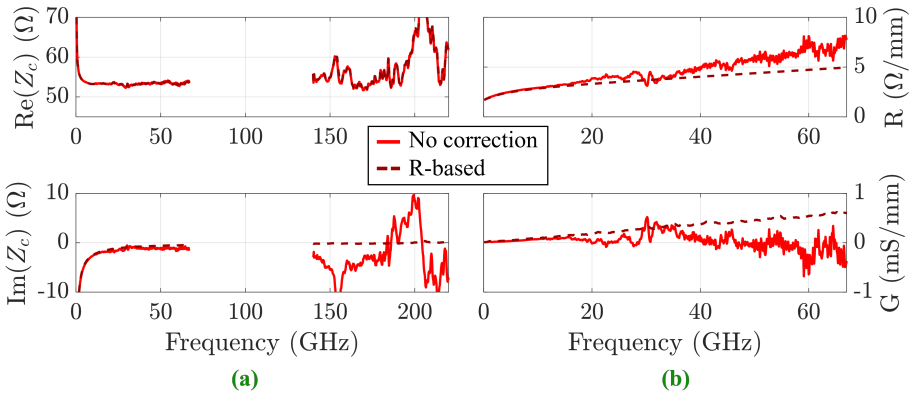


Figure 3.7: Extracted characteristic impedance (a) and *R* and *G* terms of CPW lines: using calibration comparison method (solid, light red lines), by applying the R-based method (dashed, dark red lines).

is why *R* and *G* are not shown in **Figure 3.7b** at those frequencies. This high-frequency data set further shows that it is crucial to find a different way to extract substrate losses than from direct measurement of Z_c.

The correction applied to $\mathrm{Im}(Z_c)$ with the R-based method is significant. A rather good fitting of $R(f)$ and $G(f)$ is obtained at low frequencies. The extracted $\rho_{eff}(f)$ is shown in **Figure 3.8**. Despite a small shift between the direct extraction and the corrected one, the overall trends in $\rho_{eff}(f)$ are similar, and the corrected curve is less noisy and does not suffer from repeated bumps.

However, $\rho_{eff}(f)$ is still not constant with frequency, as it should be from conductive-only substrate losses, which likely means that another loss mechanism is not accounted for in the *G* formulation from **Equation 3.3**. The linear frequency dependence of this unaccounted for substrate loss indicates poten-

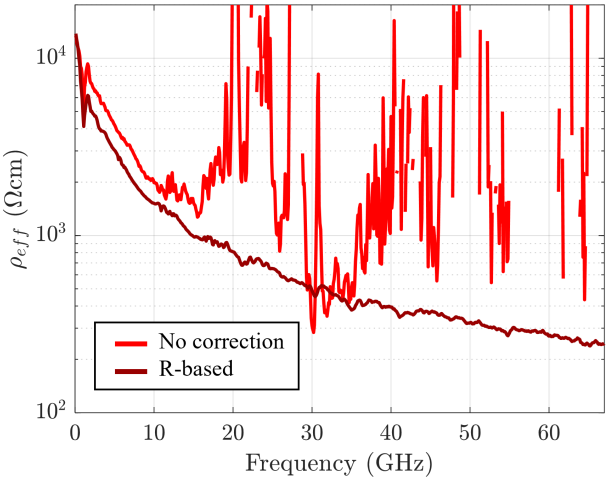


Figure 3.8: Effective resistivity extracted either by using calibration comparison method (light red), or by applying the R-based method (dark red).

tially significant dielectric losses. So, the next section extends the substrate loss model from **Section 3.1.1** to include dielectric-based losses.

3.3 Accurate and Meaningful Substrate Loss Parameters Extraction for Low-Loss Substrates

3.3.1 Addition of dielectric losses to the substrate loss model

If the model presented in **Figure 3.2** is extended to include dielectric losses, then the shunt admittance of the transmission line can be written as follows:

$$G + j\omega C = \frac{F_{bot}}{\rho_{eff}} + \omega\varepsilon_0 \left[F_{bot}\varepsilon_{r,sub,eff} + F_{top}\varepsilon_{r,top}\right], \tag{3.14}$$

and G and C become

$$G = \frac{F_{bot}}{\rho_{eff}} + + \omega\varepsilon_0 \left[F_{bot}\varepsilon''_{r,sub,eff} + F_{top}\varepsilon''_{r,top}\right], \tag{3.15}$$

$$C = \underbrace{\varepsilon_0\varepsilon'_{r,sub,eff}F_{bot}}_{=C_{bot}} + \underbrace{\varepsilon_0\varepsilon'_{r,top}F_{top}}_{=C_{top}}, \tag{3.16}$$

where complex effective relative permittivities are defined for the top and bottom materials: $\varepsilon_{r,sub,eff} \equiv \varepsilon'_{r,sub,eff} - j\varepsilon''_{r,sub,eff}$ and $\varepsilon_{r,top} \equiv \varepsilon'_{r,top} - j\varepsilon''_{r,top}$.

Due to the linear frequency term of **Equation 3.15**, if dielectric loss is non-negligible and **Equation 3.4** is used to evaluate the effective resistivity, then it would yield a ρ_{eff} that is decreasing with frequency. In the present study, the material on top of the CPW metal lines is assumed to be air, corresponding to $\varepsilon''_{r,top} = 0$. The discussion could easily be extended to a general material for which $\varepsilon''_{r,top} \neq 0$. To include conductive and dielectric loss mechanisms, the effective loss tangent is defined as

$$\tan\delta_{eff}(f) \equiv \frac{G(f)}{\omega\varepsilon_0\varepsilon'_{r,sub,eff}F_{bot}} = \frac{1}{\rho_{eff}\omega\varepsilon_0\varepsilon'_{r,sub,eff}} + \tan\delta_{d_{eff}}, \qquad \textbf{(3.17)}$$

with

$$\tan\delta_{d_{eff}} \equiv \frac{\varepsilon''_{r,sub,eff}}{\varepsilon_{r,sub,eff}}, \qquad \textbf{(3.18)}$$

where **Equation 3.18** is the *definition* of the effective dielectric loss tangent.

So, the new substrate loss model is described by two distinct loss mechanisms: conductive and dielectric. We propose to extract two *constant-valued* parameters $\tilde{\rho}_{eff}$ and $\tan\tilde{\delta}_{eff}$ (representing the two loss mechanisms, thus the new model) by a least squares fitting of **Equation 3.17** over an intermediate frequency range. Once those two parameters are extracted, one can assess the consistency of the extracted model by computing two *equivalent* frequency-dependent material parameter FoMs, i.e.

$$\rho^{\star}_{eff}(f) \equiv \left[\left(\tan\delta_{eff}(f) - \tan\tilde{\delta}_{d_{eff}}\right)\omega\varepsilon_0\varepsilon'_{r,sub,eff}(f)\right]^{-1}, \qquad \textbf{(3.19)}$$

$$\tan\delta^{\star}_{d_{eff}}(f) \equiv \tan\delta_{eff}(f) - \frac{1}{\tilde{\rho}\,\omega\varepsilon'_{r,sub,eff}(f)}. \qquad \textbf{(3.20)}$$

Several parameters have been defined several times above. So, let us recap to avoid any confusion. Assuming G is perfectly extracted.

- In case substrate losses are entirely described by a *conductive* loss mechanism, G and ρ_{eff} computed from **Equation 3.4** are constant with frequency[a], and further definitions (**Equation 3.17**-**Equation 3.20**) are irrelevant.
- In case *dielectric* losses are non-negligible and conductive losses are not sufficient to entirely describe the substrate loss mechanisms, it is better to refer to **Equation 3.17** for a complete and meaningful description of substrate loss mechanisms.
  A low-frequency tail in **Equation 3.17** is characteristic of *conductive* losses, and a non-zero, constant, high-frequency value in **Equation 3.17** is representative of *dielectric* losses. To extract a complete loss model taking into account both contributions, **Equation 3.17** is fitted with *constant-valued* parameters: $\tilde{\rho}_{eff}$ and $\tan\tilde{\delta}_{eff}$.
  Once this complete substrate loss model is extracted, the *residual (frequency-dependent)* error can be either visualized
  - from a point of view of conductive losses, $\rho^{\star}_{eff}(f)$ (*total* losses from which we *subtract modeled dielectric* losses) with **Equation 3.19**,

  or, in a completely equivalent way,
  - from a point of view of dielectric losses, $\tan\delta^{\star}_{d_{eff}}(f)$ (*total* losses from which we *subtract modeled conductive* losses) with **Equation 3.20**.

[a] This is valid in a CPW line as long as the field distribution does not change with frequency. There are a several cases in which the field distributions can change with frequency: for instance in presence of surface waves or high-order mode excitation. It can also occur in a non-homogeneous substrate material with regions of different majority carriers relaxation frequencies, and at frequencies for which some of these regions are still in the 'slow-wave' mode (when frequency is below these majority carriers relaxation frequencies).

To better visualize this new substrate loss model, let us apply it to the previous measurement set for which a frequency-dependent $G(f)$ was extracted (cf. **Figure 3.9**).

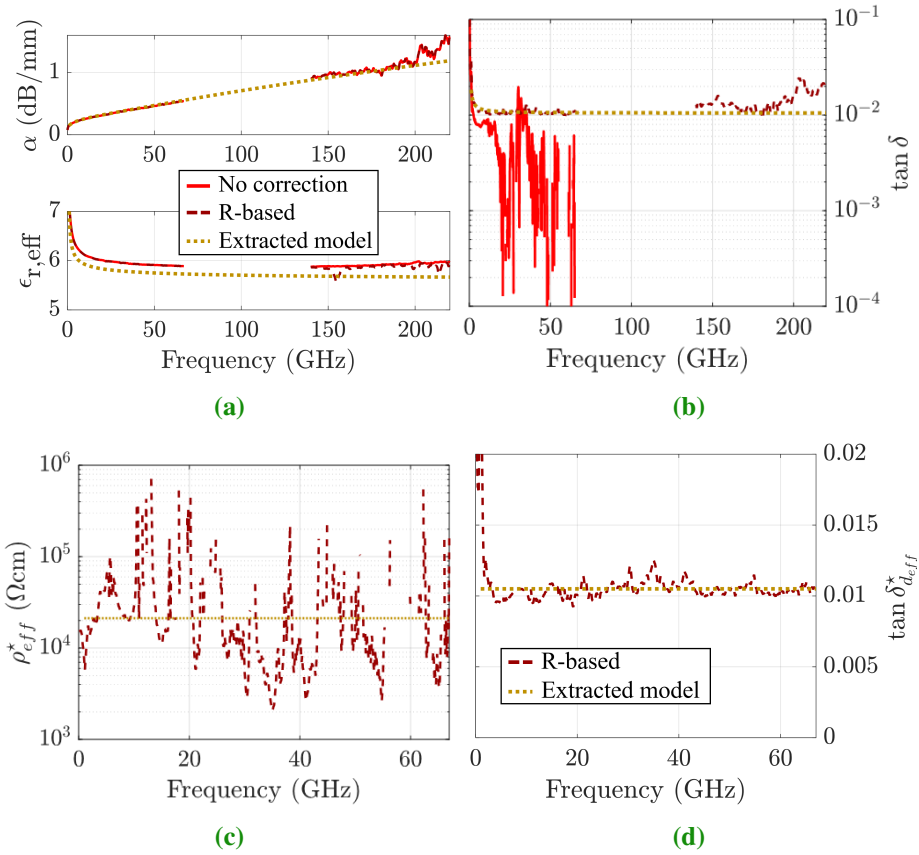


Figure 3.9: Total (a) and substrate loss extraction (b) from measured CPW lines on a 'home-made' TR Si substrate. Residual *conductive* (c) and *dielectric* (d) losses, $\rho^{\star}_{eff}$ and $\tan^{\star}_{d_{eff}}$, respectively. Solid, light red lines: direct extraction from calibration comparison. Dashed, dark red lines: corrected extraction with R-based method. Dotted yellow lines: complete CPW line models, i.e. Heinrich model with extracted substrate loss model ($\tilde{\rho}_{eff} = 21.2\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 1.05 \times 10^{-2}$).

Fitting the loss tangent curve from the R-based corrected measurement (see **Figure 3.9a**), we extract a substrate loss model with $\tilde{\rho}_{eff} = 21.2\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 1.05 \times 10^{-2}$. By using it to compute G -and the remaining *RLC* parameters being obtained from Heinrich model (with the CPW geometry presented in **Figure 3.6**)- we obtain the dotted yellow curves. We observe a good agreement between this reconstructed CPW model and the 140-220 GHz measurements in propagation losses (cf. **Figure 3.9a**), which validates the overall extracted model.

In **Figure 3.9c** and **Figure 3.9d**, we observe the residual substrate losses either interpreted as *conductive* or as *dielectric*, respectively. We observe that $\rho^{\star}_{eff}$ remains at very high values, which confirms the extraction consistency.

Care should be taken with the extracted values of conductive and dielectric losses using this R-based method. As we can clearly see in **Figure 3.9b** below 15 GHz, by forcing a R_{forced} that is only slightly smaller than the extracted $R(f)$, we get an (roughly 30 %) over-estimated $G(f)$ and loss tangent, already above a few GHz.

Another disadvantage of this technique is its range of applications. Due to the strong assumption that R can be accurately described by Heinrich's model, it cannot be applied in several cases, e.g. CPW geometry that varies from the one used in **[64]**: CPW metal lines on several metal layers, meshed metal lines, or in industrial BEOL due to the presence of dummy fills, etc. Nevertheless, this method has its advantages that are illustrated in the following.

3.3.2 Application of R-based method in presence of systematic error

The R-based method was initially developed as we faced the problem of misbehaving $\mathrm{Im}(Z_c)$, even at low frequencies (thus propagated to $R(f)$ and $G(f)$), before identifying this issue to not-well defined calibration Z_{ref}. By forcing a known $R(f)$, the R-based method becomes almost insensitive to misevaluation of $\mathrm{Im}(Z_c)$.

To illustrate this, let us apply the R-based method correction to the example from **Section 3.1.2**, in which data is spoiled by the effect of a wrong probe placement on the calibration standards[5].

Figure 3.10 shows the R and G terms and loss tangent (**Equation 3.17**) directly computed from the calibration comparison technique (light lines), and to which we applied the R-based technique (dark lines). It is preferable to

[5] Data above 90 GHz are not shown because of a strong systematic deviation in measurements that is likely related to probe-dependent residual error. It was already identified above.

visualize substrate losses with the loss tangent definition than the previous ρ_{eff} from **Equation 3.4**, because of the very high resistivity (and low loss) of this wafer (RFeSI 90 substrate, cf. **Figure 3.4**).

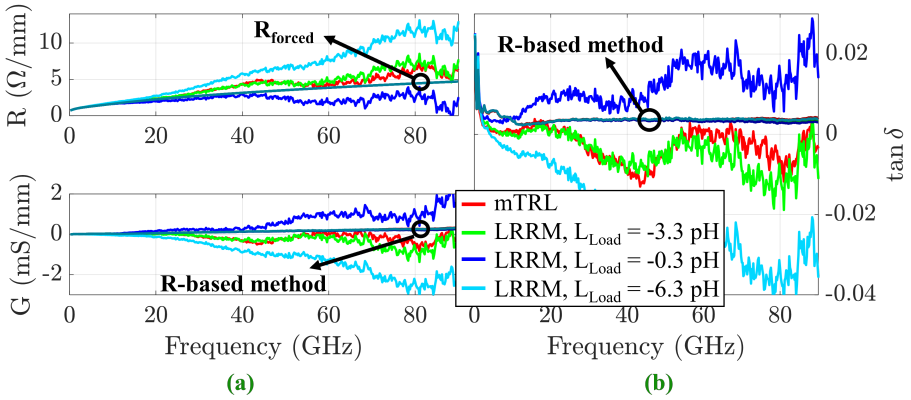


Figure 3.10: *R* and *G* terms (a), loss tangent from **Equation 3.17** (b), from CPW line measurements with different first-tier calibrations representing user-related systematic error, cf. **Section 3.1.2**. Direct extraction (light lines) and application of R-based method (dark lines, shown in legend).

We again observe a significant discrepancy at low frequency between the loss tangent from direct extraction, with a 'good' first-tier calibration (mTRL and LRRM with $L_{Load} = -3.3\,\text{pH}$), and the data to which the R-based method is applied. However, after applying the R-based method, the extracted substrate losses are insensitive to the systematic errors introduced, as expected. The extracted substrate parameters from R-based corrected data are $\tilde{\rho}_{eff} = 18.8 - 42.3\,\text{k}\Omega\text{cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 2.87\times10^{-3} - 3.76\times10^{-3}$, with very little variation. The residual substrate losses both in terms of conductive and dielectric losses are shown in **Figure 3.11**. The residual substrate losses in $\rho^{\star}_{eff}(f)$ are very large across the whole dc-90 GHz.

As we have seen here, the correction method is rather robust in case of user-related systematic errors and provides an overall propagation loss model that fits well direct measurements. For an accurate material properties extraction, however, we propose the procedure described in the next sub-section.

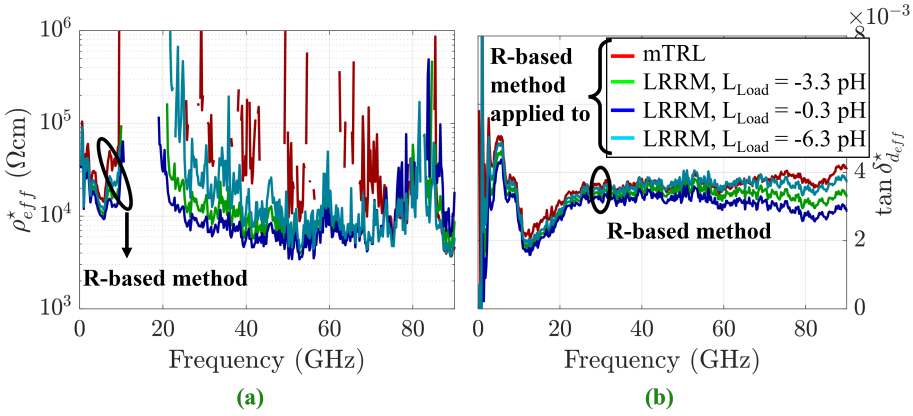


Figure 3.11: Residual substrate losses: $\rho^\star_{eff}(f)$ (a) and $\tan\delta^\star_{d_{eff}}$, from R-based-corrected measurements, with substrate model parameters $\tilde{\rho}_{eff} = 18.8 - 42.3\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 2.87\times10^{-3} - 3.76\times10^{-3}$.

3.3.3 Accurate material parameter extraction at low frequency

As we have seen with the two last examples, there is significant disagreement in substrate losses (for instance visible in **Figure 3.9b** and **Figure 3.10b** below 15 GHz) between direct extraction and corrected data with the R-based method. Therefore, this method is hardly accurately applied to very low-loss substrate electrical properties extraction, because a small misestimation in R introduces a large relative error in corrected G. Instead, with an accurate first-tier calibration (mTRL for instance), we have seen that the extracted $RLGC$ parameters are highly accurate below 20 GHz in general. So, we propose to extract the material parameters from the low-frequency data (where the curves are behaving smoothly), without any correction.

In the case shown above in **Figure 3.10**, extracting a substrate model from frequencies below 11 GHz (cf. **Figure 3.12**) yields $\tan\tilde{\delta}_{d_{eff}} = 2.5\times10^{-4}$ and $\tilde{\rho}_{eff} = 30\,\mathrm{k\Omega cm}$, the resulting $\rho^\star_{eff}(f)$ is shown in **Figure 3.12b** and agrees well with an average value of $30\,\mathrm{k\Omega cm}$ within the extracted frequency range (below 11 GHz).

Since the dielectric losses are very small in that case: $\tan\tilde{\delta}_{d_{eff}}$ is lower than $\tan\delta$ over the whole extraction range ($\tan\delta > 4\times10^{-4}$ for $f < 11\,\mathrm{GHz}$), it means that conductive losses, although very small too, dominate the overall substrate losses in that frequency range. So, let us look at the total substrate

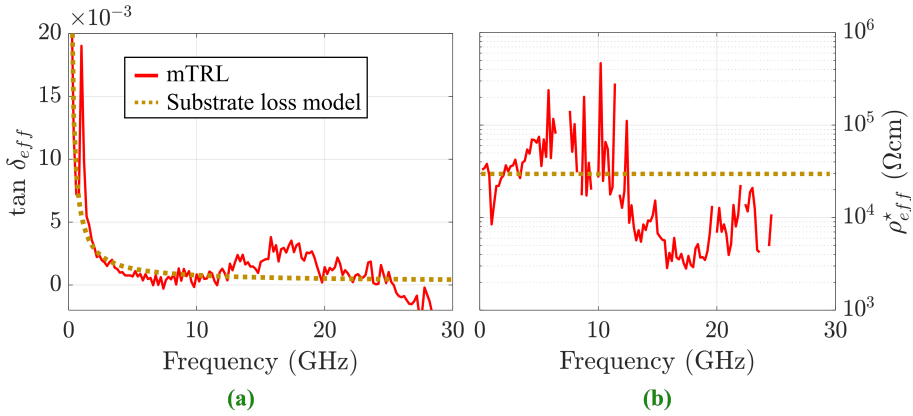


Figure 3.12: Substrate loss tangent (a) and residual conductive losses $\rho^{\star}_{eff}(f)$ (b). Direct measurements in red solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 30\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 2.5\times10^{-4}$.

losses in case they are entirely conductive: ρ_{eff} from **Equation 3.4**, see **Figure 3.13**.

We observe that, even at such low frequencies and with such low level of dielectric losses, the substrate loss model features a small noticeable decrease in $\rho_{eff}(f)$: it *reaches 50% of its nominal value at* 21 GHz *already*. So, let us define the frequency at which dielectric losses and conductive losses have an equal contribution to total substrate losses ($f_{c,loss}$):

$$f_{c,loss} \equiv \frac{1}{2\pi\varepsilon_0\tilde{\rho}_{eff}\varepsilon'_{r,sub,eff}\tan\tilde{\delta}_{d_{eff}}}. \tag{3.21}$$

It also corresponds to the frequency at which $\rho_{eff}(f)$ from **Equation 3.4** is reduced by half from its nominal (low frequency) value, so $f_{c,loss} = 21\,\mathrm{GHz}$ in the example shown above.

For more conductive substrates, this cutoff frequency is pushed to higher frequencies. It means that conductive losses are dominating, thus the validity of the extracted dielectric loss contribution becomes questionable. In lack of an accurate uncertainty analysis from measured data, let us define an arbitrary criterion to decide to either validate or invalidate the extracted value of dielectric losses ($\tan\tilde{\delta}_{d_{eff}}$).

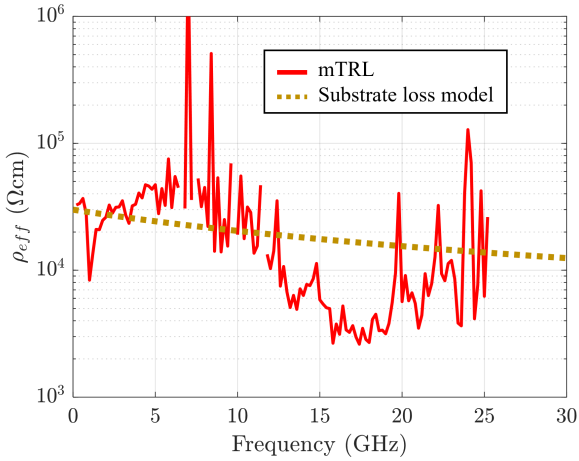


Figure 3.13: Substrate effective resistivity (**Equation 3.4**). Direct measurements in red solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 30\,\mathrm{k\Omega\,cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 2.5 \times 10^{-4}$.

Even if it is completely arbitrary, let us assume that dielectric loss cannot be accurately extracted if, at the highest frequency at which we 'trust' our directly extracted measurements (until occurrence of first bump in measurements, for instance 12 GHz in the example from above, cf. **Figure 3.12a**), the value of reconstructed $\tan\delta_{eff}$ (from substrate loss model) is, say, ten times larger than the nominal value of dielectric losses extracted ($\tan\tilde{\delta}_{d_{eff}}$). Equivalently, it means that if the highest 'trustable' frequency is larger than $f_{c,loss}/9$, then the extracted value of $\tan\tilde{\delta}_{d_{eff}}$ is valid.

So, applied to the above example, the highest frequency at which the measured $\tan\delta_{eff}(f)$ is not affected by any bump (except for a very localized deviation at 1 GHz) is 12 GHz. Since $f_{c,loss} = 21\,\mathrm{GHz} < 9 \cdot 12\,\mathrm{GHz}$, then the extracted $\tan\tilde{\delta}_{d_{eff}} = 2.5 \times 10^{-4}$ is validated.

The previous observations have led to propose the following procedure for a pertinent substrate loss model extraction and choice of visualization. We consider the two possible substrate models: (i) conductive losses only (**Equation 3.4**) and (ii) conductive+dielectric losses (**Equation 3.17**). Concerning visualization, the most pertinent graph is either $\rho_{eff}(f)$ or $\tan\delta_{eff}(f)$.

The procedure is the following.

1. Start by extracting a substrate loss model including both conductive and dielectric losses from curve fitting of **Equation 3.17** in a 'trustable' frequency range (free from bumps *and* above some potential slow-wave mode), with boundaries defined $[f_{LF,trust}, f_{HF,trust}]$.
2. Check for validity of nominal dielectric loss value extracted. The value is valid if $f_{HF,trust} > f_{c,loss}/9$,
   - if it is not valid, we consider dielectric losses are negligible. Use the *conductive-only substrate loss model* from **Equation 3.4**, i.e. $\rho_{eff}(f)$ with a single $\tilde{\rho}_{eff}$ substrate loss parameter;
   - if it is valid, then dielectric losses are non-negligible, so use the *conductive and dielectric substrate loss model* from **Equation 3.17**, i.e. $\tan\delta_{eff}(f)$ with the two $\tilde{\rho}_{eff}$ and $\tan\tilde{\delta}_{d_{eff}}$ substrate loss parameters.
3. According to the highest frequency at which data is extracted ($f_{sub,max}$ which might be lower than the highest measured frequency, for instance in case of strong systematic error that can be easily identified in $\mathrm{Im}(Z_c)$),
   - if $f_{c,loss} > f_{sub,max}$, then conductive losses dominate over the whole frequency range, so it is more pertinent to plot $\rho_{eff}(f)$ from **Equation 3.4**;
   - if $f_{c,loss} < f_{sub,max}$, then dielectric losses are non-negligible, so it is more pertinent to plot $\tan\delta_{eff}(f)$ from **Equation 3.17**.

To illustrate the pertinence of defining such criteria and procedures, let us show some practical substrate loss characterization of silicon substrates of various resistivities.

3.4 Selected Set of Examples for Substrate Loss Characterization

In this section, we present different substrates processed with different methods. Furthermore, the set of measured data has been acquired from the measurement of CPW lines of different designs and with different first-tier calibrations. To ease comparison, **Table 3.1** summarizes (i) substrate name, (ii) process fabrication, (iii) measurement procedure, (iv) CPW line geometry, (v) extracted

substrate loss information.

We have the habit to measure the lines by varying several parameters: chuck temperature, top signal line or chuck bias, etc. Note here that all measurements presented are at ambient temperature (23 °C) and with 0 V bias on the chuck and signal lines. Sound explanations on how ρ_{eff} of a large variety of substrates varies with these parameters can be found in **[21]**. Since we are interested here in extending the extraction procedure to very low-loss substrates to higher frequencies and with potential dielectric losses, we work under nominal conditions of ambient temperature and zero bias. If desired, this procedure could be applied to these different cases, but it is out of scope in the present work.

There are many observations that can be made on the presented graphs and extracted substrate models. To stay within the scope of this chapter and avoid lengthy discussions, we will only analyze data with respect to the R-based correction method and the substrate loss extraction procedure explained above. Additional parameters are reported in **Table 3.1** for completeness and traceability, but discussing all of them would drive the discussion out of topic.

3.4.1 Presentation of wafer samples

First, let us briefly describe the wafer samples.

- A first series of wafers: the 'Soitec' series ('Soitec-eSI90', 'Soitec-eSI80', 'Soitec-iFEM', 'Soitec-HR'), complemented with the 'FD-SOI-std' (typical FD-SOI wafer with standard resistivity bulk Si from Soitec) represents typical commercial SOI wafers covering a wide range of decreasing order resistivities: from $> 10\,\mathrm{k\Omega cm}$ to $\sim 10\,\Omega\mathrm{cm}$, respectively. They have all been manufactured by Soitec (except for a second oxide growth of the 'FD-SOI-std' wafer made in our facilities, Winfab) and the metal deposition and etching was realized in our cleanrooms (wet etching). The 'Soitec-eSI90', 'Soitec-eSI80', 'Soitec-iFEM' include some trap-rich technology, while the others do not, thus suffer from PSC effect (although losses are dominated by the conductive bulk substrate for the 'FD-SOI-std').
- The 'TRUCL' wafer sample was entirely manufactured in our cleanrooms (full process description is available in **[21]**). It consists of a purchased $> 5\,\mathrm{k\Omega cm}$ bulk Si wafer, with a 'home-made' trap-rich process and SiO_2 thermal growth. The metal deposition and etching processes are the same as for the other wafers (though not made at the same time, or by the same people).

- The 'Hudson' wafer sample consists of a set of CPW lines fabricated in the *industrial* GF 45RFSOI process that uses a high-resistivity trap-rich Si wafer.
- Finally, the 'Calkit-eSI90' sample is the same physical wafer as the 'Soitec-eSI90' sample but with a lift-off metallization process attempting to fabricate in our facilities thick ($> 2\,\mu m$) metal lines with a high uniformity across the wafer that cannot be achieved with the default wet etching process. This sample is the one already presented in the previous chapter as a potential candidate for a custom reference calibration substrate. This sample's results have just been presented in **Figure 3.12a** and **Figure 3.13**, and they will not be repeated here.

3.4.2 Results

There are a series of observations that can be made from **Figure 3.14** to **Figure 3.20**. We group them in 4 different categories that are discussed sequentially. The most important ones are highlighted in *italic*.

1. Relative to the R-based correction method.
   - As it was noticed before, for all low-loss Si wafers with a single metal process, ('Calkit-eIS90', 'Soitec-eSI90', 'Soitec-eSI80', 'Soitec-iFEM', 'TRUCL') a significant error in substrate losses is introduced by the R-based correction due to a non-perfect fit of $R(f)$ from R_{forced}. So, this correction technique prevents an accurate extraction of substrate loss parameters for very low-loss wafers.
   - **Figure 3.20** confirms that the *R-based method cannot be applied to CPW line geometries that vary from the single-metal-layer CPW line* described in Heinrich's model. Indeed, *the 'Hudson' sample manufactured in an industrial technology includes dummy fills* (that are known to increase and reduce per-unit-length R and L, respectively, of transmission lines **[100]**) *and CPW grounds made of stacked metal layers* that significantly deviate from Heinrich's model of CPW line used in the R-based technique. As observed in the inset of **Figure 3.20a**, R strongly deviates from the Heinrich-model R_{forced}, which introduces a large error in the substrate losses.
   - For moderately to 'strongly' lossy wafers ('Soitec-HR' and 'FD-SOI-std', even for the 'Soitec-iFEM' to a lesser extent), the R-based correction works rather well as the introduced error is relatively small compared to the intrinsic amount of substrate losses.

2. Relative to the extracted substrate loss parameters.

   - *For almost all very low-loss substrates* ('Calkit-eSI90', 'Soitec-eSI90', 'Soitec-eSI80'), *very large effective resistivity and very low dielectric loss parameters are extracted* from the low-frequency data. As observed in the frequency-decreasing $\rho_{eff}(f)$ graphs, *even such low values of dielectric loss have a larger impact on total substrate losses than conductive losses above* 15-20 GHz. *Dielectric loss mechanism is dominant and* must *be included in the substrate loss model.* For such substrates, it is therefore more meaningful to evaluate the substrate losses in terms of $\tan\delta_{eff}(f)$ graphs.
   - *For more conductive substrates, zero-valued dielectric loss parameters have been extracted. It does not mean that such losses are not present or negligible across the whole measured frequency range.* In particular, the $f_{c,loss}$ of the 'Soitec-iFEM' would have been ~ 55 GHz for the same dielectric loss parameter as the 'Soitec-eSI80' wafer. However, *it means that conductive losses dominate over dielectric ones in the 'trustable' low-frequency range* used for extraction.
   - The low-loss 'Hudson' sample exhibiting very large $\tilde{\rho}_{eff}$ seems to not show any dielectric loss, even below 10 GHz. It might actually be hidden by some small residual systematic error from the calibration process. Indeed, an LRRM calibration has been used for these measurements, which is very sensitive to probe misplacement as it was demonstrated in the previous chapter.
   - Whereas the *large ($\sim$10 times larger) dielectric loss observed from the 'TRUCL' sample* is hardly caused by systematic errors in the calibration as an mTRL has been used, which should not propagate such large systematic errors. This large value of dielectric loss (as well as other values of dielectric losses) extracted for a Si substrate is *further discussed* in **Section 3.4.3**.
   - The rather *large deviation in extracted* $\tan\tilde{\delta}_{d_{eff}}$ *between the two samples ('Calkit-eSI90' and 'Soitec-eSI90')* is curious, because both samples have been fabricated based on the same physical wafer. There might be two systematic error contributions to explain this. First, *mTRL assumes the calibration substrate features zero substrate losses*, which is not strictly speaking correct as *alumina dielectrics have loss tangent in the order of* 1×10^{-4} at microwave

frequencies [84–86]. *This assumption might lead to considerable systematic errors since we are extracting substrate loss tangent in the same order of magnitude.* Second, LRRM is still sensitive to probe misplacement, as mentioned above, which might not be well accounted for in the calibration, thus propagates as a systematic error.

- Another deviation in substrate loss parameters among the two ('Calkit-eSI90' and 'Soitec-eSI90') samples is observed in the $\tilde{\rho}_{eff}$ term (30 and 16.7 kΩcm). This difference is not critical as it represents extremely low amount of substrate losses in both cases. Nevertheless, it might be physically explained by the narrower gap between the central and ground conductors of the 'Calkit-eSI90' sample. Indeed, the substrate losses are 'sensed' by the electric field of the EM wave propagating on the CPW line up to a given depth inside the substrate. This depth is related to the cross-section spacing (S) between metal lines. For a trap-rich wafer, a layer rich in traps is formed at the silicon-dioxide interface that is much more resistive than the rest of the substrate. Thus the narrower CPW line 'senses' a more resistive layer on average than the wider CPW line.

3. Relative to the application of the extraction procedure to substrates of a wide range of loss level.

   - The highest 'trustable' frequency ($f_{HF,trust}$) is somehow subjective and impacts the value of extracted substrate loss parameters. It has been selected on a case-to-case basis that is subject to criticism. It might be more rigorously selected from an uncertainty analysis, but, in lack of such analysis, care should be taken to the absolute extracted values, especially for low-loss substrates. Nevertheless, the validity of the extracted values of dielectric losses is further discussed shortly in **Section 3.4.3** .
   - The substrate loss parameters are less sensitive to the choice of $f_{HF,trust}$ in case of lossier substrates. However, the low-frequency $f_{LF,trust}$ should be selected with care due to the slow-wave mode that can affect measurements up to ~ 30 GHz for standard resistivity substrates. For such substrates, fitting $\rho_{eff}(f)$ with a constant $\tilde{\rho}_{eff}$ parameter is more accurate than least-squares-curve-fitting $\tan\delta_{eff}(f)$, thereby justifying the more pertinent visualization of substrate losses with $\rho_{eff}(f)$ graph for moderately-to-strongly con-

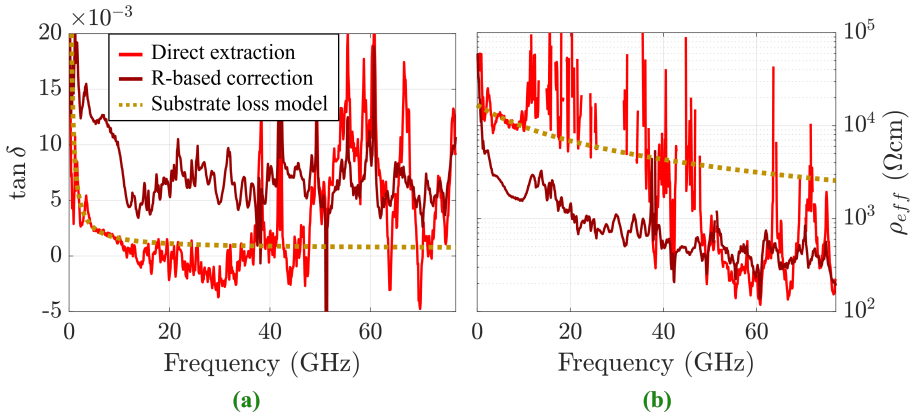


Figure 3.14: Substrate loss extraction of wafer 'Soitec-eSI90'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 16.7\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 6.6 \times 10^{-4}$.

ductive substrates.

4. A last interesting point that will be further developed later is that *all measurements contain some remaining systematic errors*, whether it be from calibration algorithm, or probe-dependent residual error. We clearly see here that *low- and very low-loss substrates have very sensitive substrate loss curves* and that the upper 'trustable' frequency is between 10 to 20 GHz. Whereas for *lossier substrates, the* $\rho_{eff}(f)$ *curves are less sensitive* and $f_{HF,trust}$ is larger (30-70 GHz).

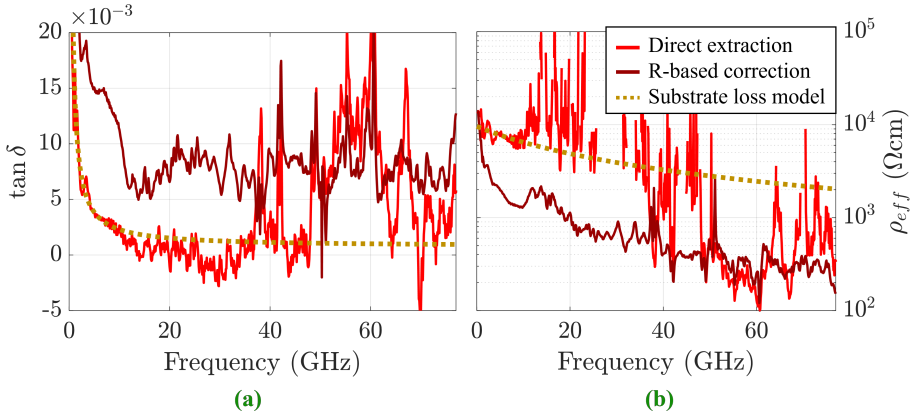


Figure 3.15: Substrate loss extraction of wafer 'Soitec-eSI80'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 9.6\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 7.5 \times 10^{-4}$.

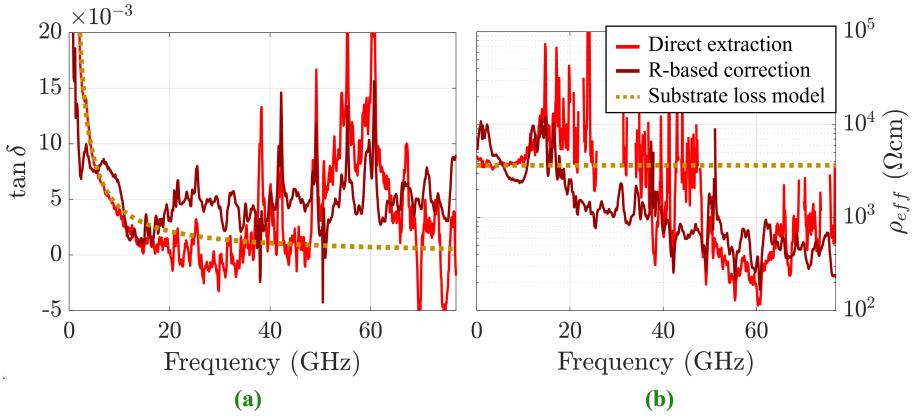


Figure 3.16: Substrate loss extraction of wafer 'Soitec-iFEM'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 3.65\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 0$.

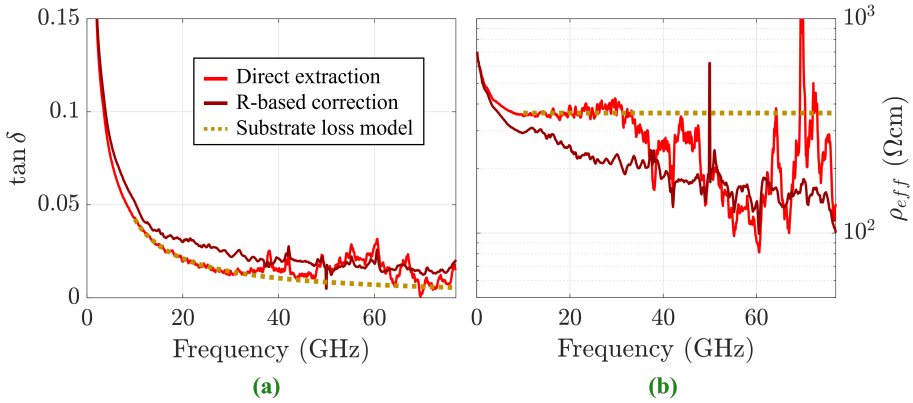


Figure 3.17: Substrate loss extraction of wafer 'Soitec-HR'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 363\,\Omega\,\text{cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 0$.

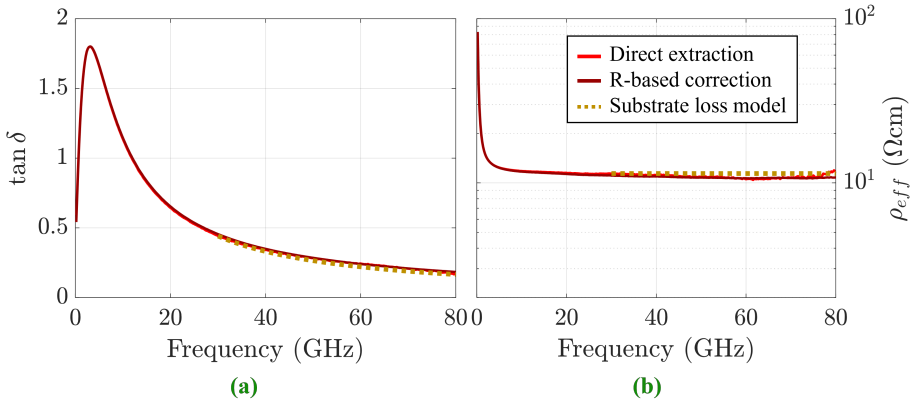


Figure 3.18: Substrate loss extraction of wafer 'FD-SOI-std'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 11.4\,\Omega\,\text{cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 0$.

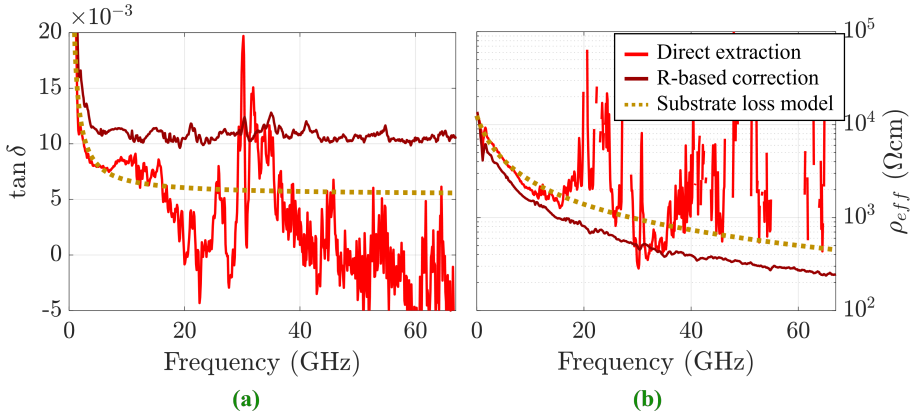


Figure 3.19: Substrate loss extraction of wafer 'TRUCL'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 12.5\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 5.38 \times 10^{-3}$.

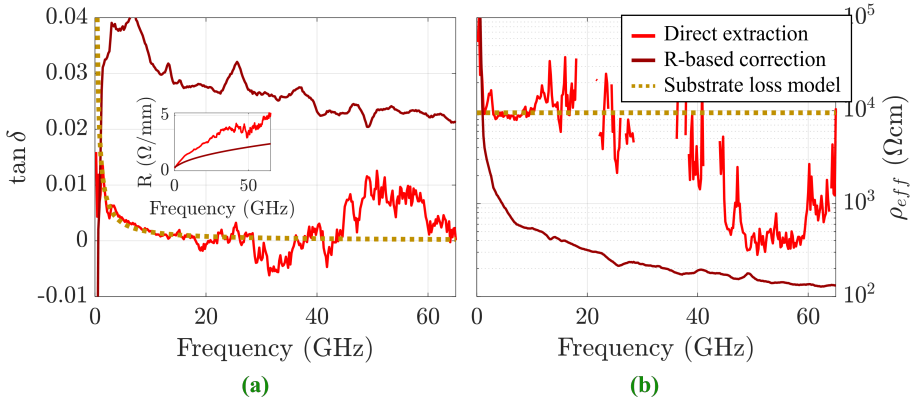


Figure 3.20: Substrate loss extraction of wafer 'Hudson'. Substrate loss tangent (a, **Equation 3.17**), substrate effective resistivity (b, **Equation 3.4**). Direct measurements in light red solid lines, R-based correction in dark solid lines, substrate loss model in dotted yellow lines, with substrate model parameters $\tilde{\rho}_{eff} = 12.5\,\mathrm{k\Omega cm}$ and $\tan\tilde{\delta}_{d_{eff}} = 0$.

Table 3.1: Summary of wafer samples presented in this chapter.

Substrate name	Name in thesis	'Calkit-eSI90'	'Soitec-eSI90'	'Soitec-eSI80'	'Soitec-iFEM'	'Soitec-HR'	'FD-SOI-std'	'TRUCL'	'Hudson'
Process fabrication	Handle wafer origin	Soitec	Soitec	Soitec	Soitec	Soitec	Soitec	Winfab	GF 45RFSOI
	Oxide process	Soitec process	Soitec process	Soitec process	Soitec process	Soitec process	20 nm Soitec +180 nm Winfab thermal growth	200 nm Winfab thermal growth	45RFSOI process
	TR process	Soitec process	Soitec process	Soitec process	Soitec process	N/A	N/A	rapid thermal annealing	Manufacturer process
	Metallization process	e-beam evapor. Winfab	e-beam evapor. Winfab	e-beam evapor. Winfab	e-beam evapor. Winfab	e-beam evapor. Winfab	e-beam evapor. Winfab	e-beam evapor. Winfab	45RFSOI process
	Etching process	Lift-off Winfab	Wet etching Winfab	Wet etching Winfab	Wet etching Winfab	Wet etching Winfab	Wet etching Winfab	Wet etching Winfab	45RFSOI process
Measurement procedure	Freq. range (GHz)	0.2-130	0.2-130	0.2-130	0.2-130	0.2-130	0.2-130 growth	0.1-67	0.2-130
	Probes	I110	I110	I110	I110	I110	I110	I67	I110
	Calibration substrate	104-783A	104-783A	104-783A	104-783A	104-783A	104-783A	101-190C	104-783A
	First-tier calibration	mTRL	LRRM	LRRM	LRRM	LRRM	LRRM	mTRL	LRRM
CPW line geometry	Measurement type	SEM + profiler	Profiler	Profiler	Profiler	Profiler	Profiler	Profiler	GDS layout
	W_c (µm)	23.5	31	32	33	32	23	22.5	35
	S (µm)	13.7	20	21	18	19.2	13.5	12.1	25
	t (µm)	2.22	0.83	0.73	0.8	0.76	0.8	0.91	4
	W_g (µm)	107.5	162	162	162	162	155	155	132.5
	h (µm)	700	700	700	700	700	700	500	700
	σ_{met} (S/µm)	33	28.6	27	28.1	26.81	29	31.6	35
	L (µm)	**Figure 3.6**	426, 906, 1326, 1626, 2106, 2526, 2826				100, 2100, 8100		160, 500 900, 1800 3600
Extracted substrate model	$\varepsilon_{r,sub,eff}$	11.25	11.65	12.08	11.46	11.73	11.9	10.65	10.3
	$\tilde{\rho}_{eff}$ (Ωcm)	30 k	16.7 k	9.6 k	3.65 k	363	11.4	12.5 k	9.5 k
	$\tan\delta_{d,eff}$	2.5×10^{-4}	6.6×10^{-4}	7.5×10^{-4}	0	0	0	5.38×10^{-3}	0
	$f_{c,loss}$ (GHz)	21	14	20.7	N/A	N/A	N/A	2.5	N/A
	$f_{LF,trust}$ (GHz)	0.1	4.2	4.2	4.2	10	20	0.2	3
	$f_{HF,trust}$ (GHz)	11	10	10.7	10.7	26.3	75	6.6	17.8
	Valid $\tan\tilde{\delta}_{d,eff}$?	Y	Y	Y	N	N	N	Y	N
	Recommended plot	$\tan\delta_{eff}(f)$	$\tan\delta_{eff}(f)$	$\tan\delta_{eff}(f)$	$\rho_{eff}(f)$	$\rho_{eff}(f)$	$\rho_{eff}(f)$	$\tan\delta_{eff}(f)$	$\rho_{eff}(f)$

3.4.3 Discussion of extracted values of dielectric losses

Different values of dielectric loss have been extracted for several Si substrate samples. Whereas this extraction procedure still suffers from some (even small in mTRL) remaining systematic error, let us discuss briefly about the extracted values and how it compares to reported loss tangent values of Si.

A short introduction to different dielectric loss mechanisms and polarization effects can be found in [101].

To keep it brief in the text, we will only mention the relevant loss mechanism in silicon [102]. Silicon dielectric losses are described by electronic polarization in neutral atoms when an electric field displaces the nucleus with respect to the electrons that surround it. This phenomenon can be described by the interaction of a phonon system with the electric field. Gurevich and Tagantsev developed a complete theory of this dielectric loss mechanism [103].

Losses in silicon substrates (even high-resistivity substrates with several kΩcm) are usually dominated by conductive losses at RF and mm-wave frequencies [97, 98]. Indeed, dielectric loss measurements at RF, mm-wave and sub-THz frequencies (up to 320 GHz in [98]), with either split post dielectric resonators [23] or Fabry-Perot resonator technique [98], of HR substrates from 1 kΩcm to > 230 kΩcm (a sample with a resistivity larger than the theoretical intrinsic Si resistivity have been obtained in [23] by irradiating a HR Si wafer with high-energy particles), have shown that Si has $\tan\delta_d \approx 1.2\times10^{-5}$. Such a low value of dielectric loss makes non-conducting Si the material with lowest dielectric losses up to about 2 THz [23].

We obtain a much larger value of dielectric losses than these reported above, thus questioning the validity of extracted dielectric loss tangent value. Perhaps a better visualization to determine whether dielectric losses are present or not can be achieved with a 'log-log' plot of $\tan\delta_{eff}(f)$. Indeed, from **Equation 3.17**,

$$\log(\tan\delta_{eff}) = \log\left(\tan\delta_{d_{eff}}\right) \text{ when } f\to\infty, \tag{3.22}$$

$$= -\log\left(\rho_{eff}\varepsilon_0\varepsilon'_{r,sub,eff}\right) - \log(\omega) \text{ when } f\to 0, \tag{3.23}$$

such that $\tan\delta_{eff}(f)$ in a log-log plot should be a pure straight line with a $-1\,\mathrm{dec}/1\,\mathrm{dec}$ slope irrespective to the amount of substrate losses, as long as dielectric losses are negligible.

Figure 3.21 shows such a log-log plot for the very low-loss substrates for which a non-zero value of $\tan\tilde{\delta}_{d_{eff}}$ is extracted. A kind of plateau (indicative

of dielectric losses) really seems to emerge around 5-10 GHz for the 'Soitec-eSI90', 'Soitec-eSI80' and 'TRUCL' curves. Whereas the linear function provided by the *conductive-only* substrate loss model seems to agree better with measurements of 'Calkit-eSI90' sample, which invalidates the extracted value of $\tan\tilde{\delta}_{d_{eff}} = 2.5 \times 10^{-4}$.

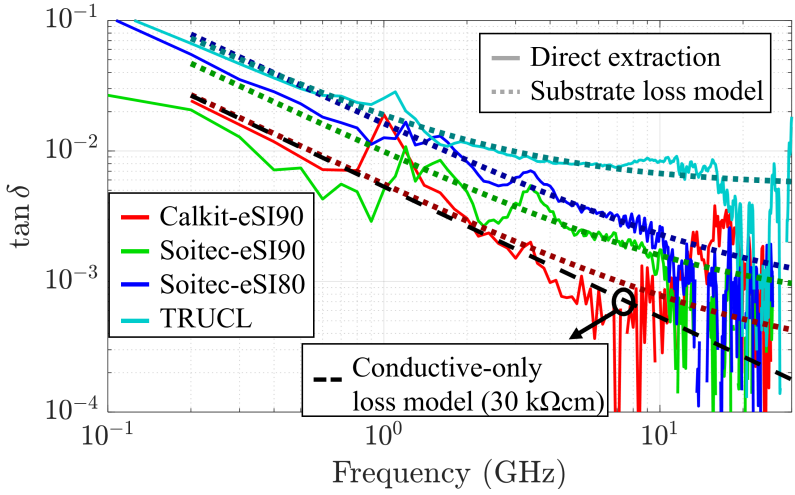


Figure 3.21: Log-log plot of $\tan\delta_{eff}(f)$ for low loss substrates. Direct (uncorrected) extraction from measurement in solid lines. Extracted substrate model (with non-zero $\tan\tilde{\delta}_{d_{eff}}$ value) in dotted lines. Equivalent *conductive-only* substrate model of 'Calkit-eSI90' sample in black, dashed line.

On the one hand, the non-negligible dielectric loss parameter value of the 'Soitec-eSI90' and 'Soitec-eSI80' can be related to potential systematic error in the LRRM calibration (as mentioned above). On the other hand, the even larger dielectric loss term extracted for 'TRUCL' sample can hardly be explained by large systematic errors since an mTRL calibration was used to get these data.

While it is possible that other types of errors not considered here might explain these large dielectric losses extracted, measurements of different wafers manufactured in similar conditions as 'TRUCL' seem to also feature much larger dielectric losses than expected from Si wafers[6].

[6]Measurements of the other wafers are not shown here, because they have been performed with either LRRM or SOLT calibrations, so the extracted substrate loss model is prone to potentially strong systematic errors.

It is also likely that these 'dielectric' losses are wrongly attributed to dielectric loss mechanism[7]. Radiation or higher-order mode propagation are unlikely, as 'Calkit-eSI90' sample has a similar CPW geometry and did not feature the same level of substrate losses. Perhaps some 'pockets' of trapped conductive charges still exist in the Si close to the oxide interface that have not been captured by the trap-rich regions. Highly conductive 'pockets' could act as an equivalent substrate admittance made of a resistance in series with a capacitance. It would therefore induce a frequency-increasing G with frequency, in a similar way as the 'PN-junctions' substrate (see **Chapter 6**).

Anyway, additional characterization and experiments (test different probe technologies and calibration substrates, other measurements: e.g. large-signal, C-V, etc.) of these wafers would first be needed to confirm the presence of such large dielectric losses. Then, fabrication of more samples by isolating each fabrication process step could lead to the identification of the origin of these losses.

[7] Surface roughness could also be responsible for such losses as they also feature a linear frequency dependence. However, it is unlikely since it would be present in the R term that mTRL-based first-tier calibration should be able to accurately extract at least up to 10 GHz.

3.5 Prospects for Accurate Substrate Loss Extraction of Low-Loss Substrates at MM-Wave and sub-THz Frequencies

Two main observations have been made in the previous section. First, we have seen that measurements above 10-20 GHz suffer from systematic deviations that prevent a reliable extraction of *low* level of substrate losses. So, we developed an extraction procedure based on a 'trustable' low frequency range. It turned out that we are able to discriminate from the noise floor dielectric loss values in the order of 8×10^{-4} (for $\tilde{\rho}_{eff} \approx 10\,\mathrm{k\Omega\,cm}$).

It is nevertheless too high for dielectric loss extraction of pure silicon crystal ($\tan\delta_d = 1.2 \times 10^{-5}$), and it does not make use of higher frequency data. Even though homogeneous substrates should be entirely characterized by conductive and dielectric losses, which can be already extracted at low frequency as seen above, some heterogeneous structures might have a more complex substrate loss frequency behavior. In that case, it is important to determine the accuracy limits of our extraction method to (i) evaluate the uncertainty on the extracted substrate losses and to (ii) determine its origin and potentially correct it.

3.5.1 Evaluation of effective resistivity uncertainty

As it was demonstrated above, the uncertainty in G mostly comes from an uncertainty in $\mathrm{Im}(Z_c)$, which directly depends on the uncertainty in $\mathrm{Im}(Z_{ref})$. The most accurate results are obtained with an mTRL first-tier calibration, which is also prone to systematic errors. Systematic errors in $\mathrm{Im}(Z_{ref})$ from mTRL calibration for two different calibration substrates and probe technologies have been quantified in **Figure 2.20b**. This figure is repeated in **Figure 3.22a**.

There seem to be 2 different behaviors in the $\mathrm{Im}(Z_{ref})$ systematic error: (i) steady increase in $\mathrm{Im}(Z_{ref})$ away from $0\,\Omega$ (especially in the red lines), (ii) ripple with frequency-increasing amplitude. The former has already been discussed in the previous chapter and might be partly related to the calibration substrate itself and neglected radiation losses in its CPW lines. The latter however has an increasingly large impact with frequency and is strongly related to the probes used. Its origin is discussed shortly after.

Figure 3.22b shows the measured systematic error and a modeled error with the two components: (i) linear increase and (ii) ripple. Assuming we can correct the first systematic error: steady deviation of $\mathrm{Im}(Z_{ref})$ away from $0\,\Omega$[8],

[8] For instance using TITAN probes with a pre-characterized Z_c of calibration substrate lines using the custom-made calkit, as discussed in **Section 2.5.3**.

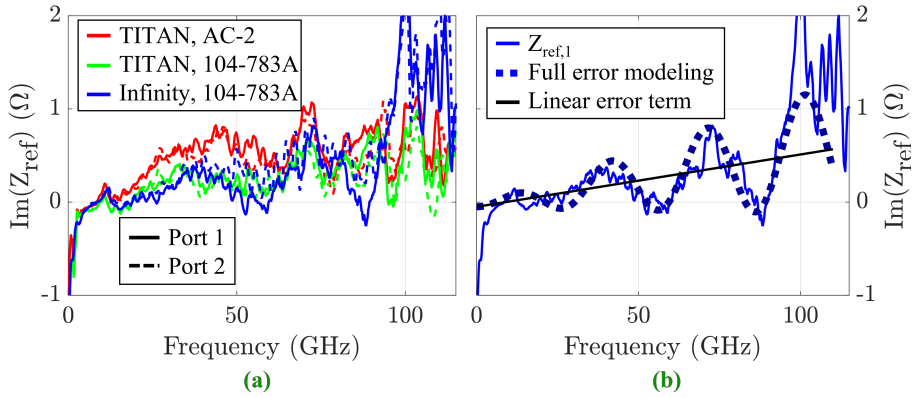


Figure 3.22: (a) Systematic error in $\mathrm{Im}(Z_{ref})$ extracted in **Section 2.5.3** from first-tier mTRL calibration of TITAN and Infinity probes on AC-2 and 104-783A calibration substrates. (b) Same $\mathrm{Im}(Z_{ref})$ error from Infinity probes measurements and the modeled error (dotted thick line) with a linear error term (black line) and ripple.

we still have the remaining ripple error. Let us evaluate the uncertainty caused by the remaining ripple in effective resistivity (as it should be the dominant substrate loss mechanism in Si wafers at mm-wave frequencies) for substrates of different effective resistivity values, see **Figure 3.23**.

As expected, lossier substrates are less impacted by this systematic-ripple error. Assuming only ripple-related systematic errors are present, **Figure 3.23** should provide good estimates of ρ_{eff} uncertainty with frequency for different values of substrate losses.

3.5.2 Possible origins of remaining systematic errors

As identified above, $\mathrm{Im}(Z_{ref})$ has a systematic error described by two components. The first one has already been discussed at length in **Chapter 2** and the second is the remaining ripple.

This ripple likely comes from the interaction of the probes with the substrate environment. Indeed, in **[104]**, Phung et al. demonstrated that a residual 'wave-like' behavior in corrected $|S_{21}|$ of transmission lines comes from various parasitic substrate modes excited by the probe, i.e. coupling from probe to substrate modes, radiation, and fringing fields between the probe and other

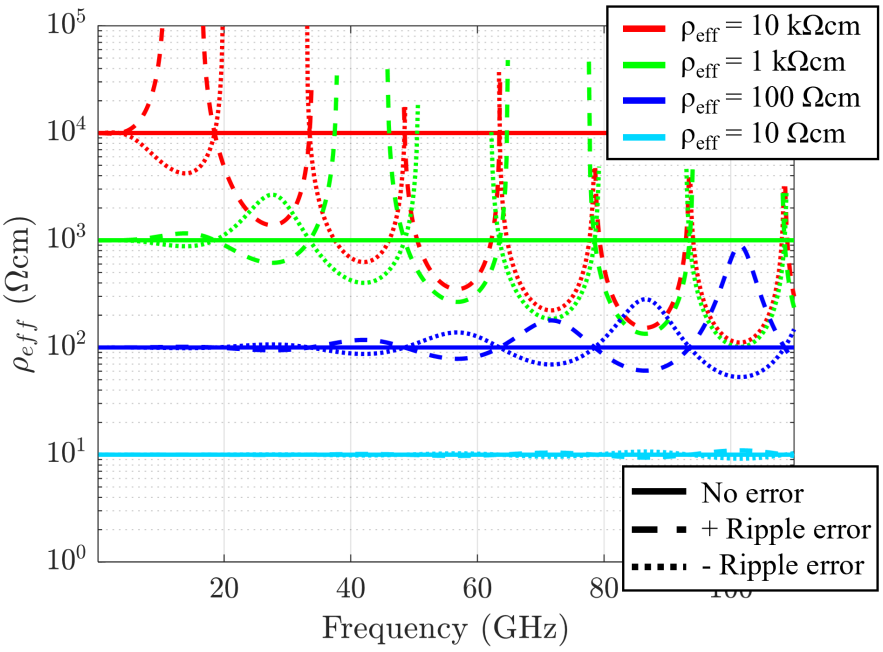


Figure 3.23: Estimated uncertainty on $\rho_{eff}(f)$ extraction due to quantified ripple error in measurements with I110 Infinity probes up to 110 GHz. Estimated error bounds in dashed and dotted lines for material effective permittivity from 10 kΩcm (red) to 10 Ωcm (cyan).

structures. Furthermore, they have also shown that the propagation of these parasitic substrate modes excited by the probes can be significantly reduced by the use of a chuck dielectric material of the same or larger permittivity as the substrate **[90, 105, 106]**[9].

Even in the advent of a complete suppression of these modes, there are still some other sources of errors in measurements. The VNA noise floor for instance, which can be reduced with (i) higher power levels, (ii) lower IF bandwidth and (iii) by averaging repeated measurements. We do not believe the VNA noise floor to be limiting the measurement accuracy in this case, as it would rather result in a noisy data dispersion varying from one measurement to

[9] Already measuring samples on a ceramic chuck instead of a metal chuck shoud help reducing ripples measured in α and transmission coefficients **[87]**.

another instead of the observed systematic ripples.

Another cause of error that deserves further investigation is ripples coming from non-perfectly matched VNA signal generator. Indeed, mismatches at both the signal source and the dut generates repeated reflected waves that affect measurements with ripple [107]. This type of hardware-related error can be evaluated for on-wafer measurement with the modified ripple-test [62]. This test estimates the source match that is the reflection coefficient of the VNA signal source (with some assumptions [62]), and whose value determines the uncertainty in measured reflection coefficient. This modified ripple-test has been applied to the 0.2-130 GHz measurement setup with TITAN probes and found the source match shown in Figure 3.24. Based on it and the measured dut, uncertainty in S_{11} and S_{22} can be estimated with the method explained in [108].

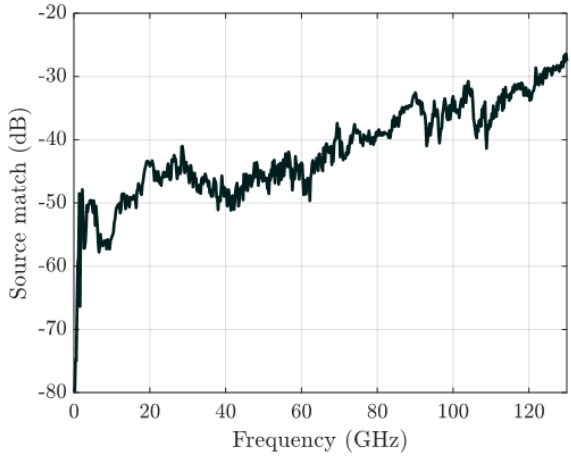


Figure 3.24: Source match evaluation based on CPW line measurements of the custom calkit standards (on 'Calkit-eSI90' wafer), with TITAN probes using the modified ripple-test [62].

3.5.3 Other methods to extract low-loss substrate parameters at mm-wave frequencies

Although the method described above works well up to 10-20 GHz for very low loss substrates and to higher frequencies for lossier substrates, we would like to extend its high frequency accuracy. However, we have seen that, except for some

few additional characterization and experiments that are worth investigating (pre-characterization of commercial calibration substrate Z_c based on a custom calkit, change of chuck material with permittivity equal or larger than the test substrate), we are reaching the limits of this direct characterization approach.

Therefore, it might be worth considering other methods that have recently been developed in the literature for low-loss substrate characterization at mm-wave frequencies. In particular, two methods seem promising and have demonstrated accuracy levels of $\sim 2-5\times10^{-4}$ in $\tan\delta$ extraction above 60 GHz **[109, 110]**. Since the accurate determination of Z_c is the main limitation to our present method, these two above methods circumvent direct extraction of Z_c, by using full-wave EM simulations for **[109]** or optimization with numerical model for **[110]**.

In **[109]**, direct measurements of different line lengths extracts γ with the mTRL algorithm. Then, full-wave simulations of a microstrip line are performed to determine the ratio $R/(\omega L)$, which is insensitive to the substrate permittivity (that is to be evaluated). Surface roughness is included in the simulations and its value is fitted to low-frequency measurement extraction, where it is assumed that substrate losses are negligible. Finally, the subsequent $G/(\omega C)$, then dielectric complex permittivity are extracted.

The method in **[85, 110]** is similar to the R-based method in the fact that it uses a CPW line model (it uses the extended model from **[88]** that includes radiation, dispersion and higher-order mode propagation) coupled with propagation constant extraction from measurements of different line lengths. However, instead of using a constant metal conductivity (σ_{met}) value, it uses an effective frequency-dependent conductivity that better describes the relationship between transverse and longitudinal losses in CPW line. The extraction of such frequency-dependent σ_{met} is explained in **[85]** and requires an accurate estimate of loss tangent at low frequencies[10].

[10]The extraction procedure is the following. First, the given low-frequency value of loss tangent is valid at all frequencies. Then, an effective $\sigma_{met}(f)$ is calculated for each frequency by fitting the loss tangent equation from Heinrich's CPW line model **[64]** feeded by (i) CPW line geometry, (ii) (constant) loss tangent value, (iii) measured propagation constant.
Then, the real part of the substrate permittivity ($\varepsilon_{r,sub}(f)$) is extracted from **[111]**. Finally, both $\sigma_{met}(f)$ and $\varepsilon_{r,sub}(f)$ are used again in the G term fitting (using Heinrich's CPW model) to find a final estimation of $\tan\delta(f)$. Although applied to different low-loss substrates (GaAs, alumina, SiO_2), its double fitting of loss mechanisms (first time with $\sigma_{met}(f)$, second time with $\tan\delta(f)$) makes the final extracted loss tangent curve questionable as $\sigma_{met}(f)$ already used a certain $\tan\delta(f)$ estimate.

3.6 Conclusion

This chapter has been dedicated to accurate substrate loss extraction from CPW line measurements to capture potential surface effects in silicon-based substrates. First, a review of the effective resistivity definition as main figure of merit describing substrate losses in Si-based substrates has been introduced. Then, we have shown that this effective resistivity parameter is very sensitive to potential systematic erroneous evaluations of the imaginary part of the transmission lines characteristic impedance. We have linked it to systematic errors on the calibration reference impedance evidenced in **Chapter 2**.

Therefore, we have introduced the *R-based* method to compensate for potential $\mathrm{Im}(Z_c)$ misestimation. This method has been demonstrated to be robust to significant user-related error (systematic probe misplacement during calibration), but it introduces a significant systematic error in the substrate loss evaluation for low-loss substrates. While it works rather well for moderately to strongly conductive substrate, it is *not* suited to low- or very low-loss substrates.

Furthermore, we have also shown that some samples exhibit excessive substrate losses with a frequency response that is not predicted by homogeneously *conductive-only* substrates. We have accordingly extended the initial substrate loss model to include dielectric loss mechanism.

Then, we have presented an extraction procedure for very low-loss to lossy substrates by including the new substrate loss model. This extraction procedure uses low-frequency data in a frequency range (typically up to 10-20 GHz) where measurements are free from parasitic oscillations.

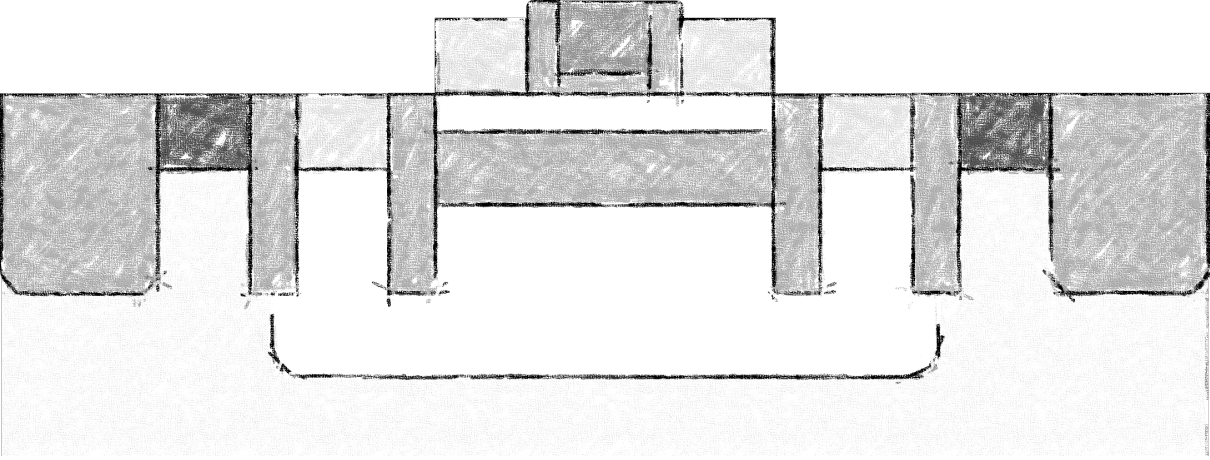
It has been applied to several Si-based substrates covering a wide range of resistivity and loss levels. Except for one particular sample, conductive losses dominate inside the reliable[11] frequency range used for extraction (where residual systematic errors are not too strong).

For this particular sample ('TRUCL'), a dielectric loss parameter of $\tan\tilde{\delta}_{d_{eff}} = 5.38\times10^{-3}$, which is 2 orders of magnitude larger than reported values of high-resistivity Si. Although we are confident that such a large value of loss does not come from systematic errors related to the measurement procedure, additional experiments should be performed to confirm the presence and identify the origin of such large dielectric-like loss.

[11] It therefore rules out the $\sim 8\times10^{-4}$ value of $\tan\tilde{\delta}_{d_{eff}}$ from 'Soitec-eSI90' and Soitec-eSI80' samples, as their measurements have been acquired based on a LRRM first-tier calibration that could suffer from significant systematic error.

Perspectives to enable the high-frequency accurate characterization of substrate losses have been presented. Even though additional experiments should be performed to try to improve the measurement accuracy, we are reaching the limits of the presented approach. So, a change of paradigm might be necessary, to eliminate the need of the Z_c extraction from direct measurements, which is the parameter most sensitive to errors. Two ways already used in the literature could be envisaged: relying either on 3D EM simulations **[109]** or on optimization via numerical models **[110]**.

Finally, we have discussed about remaining errors in measurements that can hardly be corrected with further standard characterization work: ripple with frequency-increasing amplitude. This ripple is partly responsible for unsuccessful substrate loss characterization of low-loss substrate above 10-20 GHz. In case an ideal calibration is performed (for which $\mathrm{Im}(Z_{ref})$ does not steadily deviate from 0 Ω), ripple would still be present and degrade the extracted measurements. Its effect on the effective resistivity extraction has been quantified in **Figure 3.23** for the 110 GHz measurement setup with I110 Infinity probes. It is shown that very low-loss substrates are strongly impacted by this remaining ripple. However, moderately low-loss substrate (with ρ_{eff} in the hundreds of Ω cm range) characterization still features accurate results up to several tens of GHz, which is sufficient for the $\rho_{eff}(f)$ substrates characterization of **Chapter 6**.



4. Ultra-Wideband Characterization of UTBB FD-SOI nMOSFETs

The advances in semiconductor technology have opened the path to applications operating at millimeter-wave and sub-THz frequencies. CMOS technology with its low-cost integration of digital and analog circuitry coupled with its high RF performance has become a serious contender of III-V technologies in the RF and mm-wave domain. As mentioned in **Chapter 1**, FD-SOI technology notably exhibits best-in-class RF performance among CMOS, with cutoff and maximum oscillation frequencies (f_t and f_{max}, respectively) that are as high as $\sim 400\,\text{GHz}$ **[9]**.

In parallel to RF performance improvements, the aggressive downscaling in CMOS technology has resulted in higher current and power densities, thereby increasing the self-heating (SH) effect and device temperature. Accurate characterization of SH effect is primordial as it affects critical FET parameters such carrier mobility, threshold voltage (V_{th}) and reliability **[7, 112]**. In case of FD-SOI technology, the presence of the buried oxide (BOX, with lower thermal conductivity than Si) makes FD-SOI devices more prone to self-heating issues than their bulk counterparts **[113]**. While there are several methods to extract self-heating effect (pulsed-IV, gate resistance **[114, 115]**), the method most suited to this advanced 20 nm FD-SOI device is the RF method **[114]**, which uses low-frequency measurements from 100 kHz to a few GHz.

Therefore, to enable circuit design at mm-wave and sub-THz frequencies, compact models of high accuracy are essential, including low-frequency effects

such as self-heating, as well as very high-frequency effects: non-quasi-static (NQS) effects. These models have thus to be fed with accurate transistor characterization over a very wide frequency range: from 100 kHz up to high in the mm-wave spectrum and above.

While on-wafer measurement is not problematic up to a few GHz, it becomes a complex task above a few tens of GHz. Special care to the de-embedding strategy **[29]**, structures design and floorplan **[116]** is needed for high-frequency measurements and modeling. Indeed, it is now commonly accepted that the best high-frequency measurements are obtained when the calibration reference plane is placed as close as possible to the device, via 'in-situ' calibration, i.e. with a similar on-wafer environment when performing the calibration *and* when measuring the device under test (dut). Even with these considerations, probe-dependent residual errors are still present, which complicates result interpretation **[40, 117]** in the upper mm-wave frequency range.

In this chapter, 20 nm gate length UTBB FD-SOI MOSFETs of GF 22FDX® technology are studied. This chapter is organized as follow.

The first part tackles challenges for accurate high-frequency measurements towards device characterization in CMOS-based technologies. Building on **Chapter 2**, de-embedding strategies and residual errors due to probe coupling are discussed and their effect analyzed on the extrinsic series resistances and other extrinsic parameters of a MOSFET up to 110 GHz.

Then, in the second part, 100 kHz to 10 GHz MOSFET characterization is discussed. It shows that drain-to-source coupling via the back-gate terminal and self-heating effect have concurrent impacts on the same measured parameters and in similar frequency ranges, thus complicating their separate characterization. An original method is presented that enables to accurately discriminate each effect. It is applied to a UTBB MOSFET measurement up to 10 GHz and each effect is accurately extracted for different biases.

4.1 Accurate MOSFET Measurements at MM-Wave Frequencies

To move the calibration reference plane as close as possible to the dut (MOSFET) and perform in-situ calibration, i.e. with an on-wafer environment similar as the situation when the dut is measured, a dedicated calkit is designed in the same chip. This section first introduces and presents the characterization results of the designed calkit and de-embedding structures. Then, the performance

of different de-embedding and calibration strategies applied to the extrinsic series resistances of the dut are analyzed and one strategy is selected for further extraction. Finally, extraction of the dut's extrinsic elements are compared for different probes and the impact of probe technology is discussed on a few critical parameters. Results presented here have been partially published in **[117, 118]**.

4.1.1 Calkit design

The designed calkit consists of a multiline TRL calkit, along with additional standards (such as a Load) and de-embedding structures (Probe-Short, Short-M1, Open-M1). A super-low-threshold voltage (SLVT) nMOSFET of 20 nm gate length and total width of 64 µm (0.5 µm finger width, 2 rows of 16 fingers, relaxed poly-pitch 2xCPP, device multiplicity of 4) is used as dut in this section. The FET is measured in common-source configuration with port 1 and 2 connected to the gate and drain, respectively. A back-gate bias of 0 V is used for the whole section.

Calkit standards and dut layout

The 22FDX stack option used in this work has a backend-of-line (BEOL) with 10 metal layers (labeled from M1 to M7, then JA, QA, QB from bottom to top) and an additional AluCap layer (LB).

Figure 4.1 shows a sketch of the transmission line cross-section. The transmission line signal is designed in a 3 µm-thick (QB) and 9 µm wide, lying at a distance of $\sim 6.6\,\mu m$ above the ground plane. The ground plane is made of several thin metal layers and one thick ($\gtrsim 1\,\mu m$) metal layer for a combined thickness of $\sim 1.7\,\mu m$ (M1-JA). Ground sidewalls are also present at a distance of 12.7 µm from the signal line in order to comply to the minimum density design rules without needing to add any dummy fills. Due to the relatively short distance to the signal line, the transmission line is effectively a grounded coplanar waveguide (G-CPW) line. The dimensions are selected to achieve a $\sim 50\,\Omega$ characteristic impedance (Z_c). Lines of multiple lengths (67 µm, 207 µm, 625 µm, 1648 µm) are fabricated, along with dedicated Open and Short to enable wideband mTRL calibration. The Open (Short) shares the same footprint and probe to probe distance (of $\sim 188\,\mu m$) as the Thru to ease the measurements, thus with an 18 µm long opening (shorted section).

The RF signal pad in AluCap is 60 µm long, 40 µm wide and 15 µm away from the ground pads. A ground shield beneath the signal pad is designed

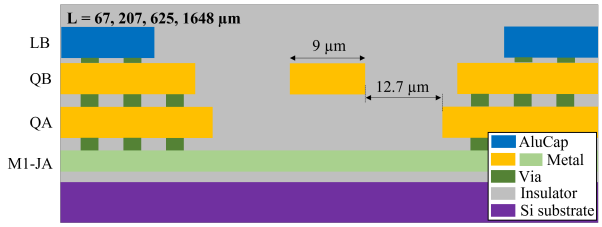
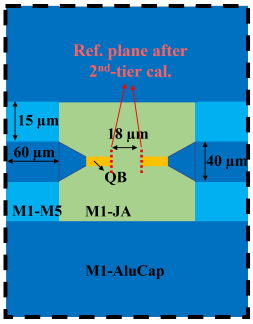
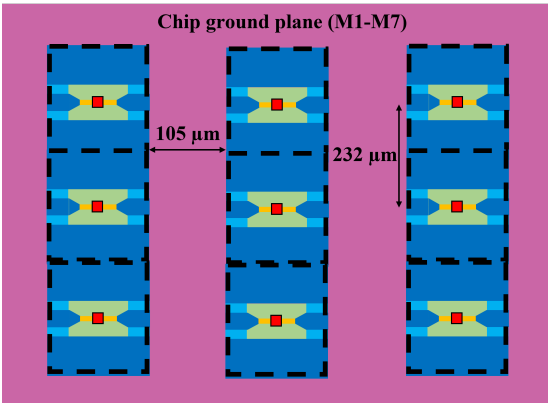


Figure 4.1: Sketch of in-situ calkit transmission line, with dimensions.

to prevent the electric field to enter in the lossy Si substrate by stacking only the 5 thin bottommost metal layers (M1-M5) for a reduced pad capacitance. The Open structure measurement yields a 15 fF shunt capacitance for the Open structure. A sketch of the Open is given in **Figure 4.2a**.



(a) Open standard.



(b) Floorplan.

Figure 4.2: Sketch of Open calkit standard and floorplan.

The nMOSFET (dut) is designed in a separate structure with the same pads and accesses as the in-situ calkit, with the same footprint (and probe to probe distance) as the Thru, Open and Short structures. It lies inside an opening in the TL's ground plane. In addition, Short and Open structures with all the FET access parasitics down to M1 are included (called Short-M1 and Open-M1) for a complete extraction down to M1.

The chip floor management is designed to present similar first neighboring structures on the left and right side of each measured structure: in-situ calkit

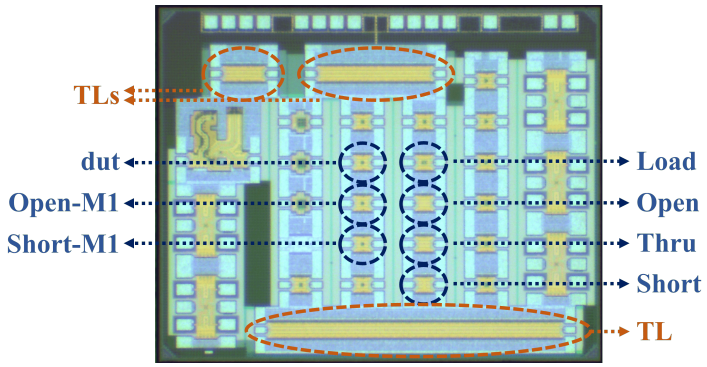


Figure 4.3: Picture of the 2x2.5 mm^2 chip.

standards, FET and its Open-M1 and Short-M1 de-embeddings. The top and bottom structures share the same ground plane, which saves some area with a limited impact on probe coupling, since their coupling is stronger in the horizontal (x) direction **[119]**. The structures are separated by 105 µm in the x-direction and their ground planes are tied together by a uniform ground plane using the 7 thin bottommost metal layers (M1-M7), as proposed in **[31, 116]** in order to present a neighbor environment that is as close as possible for all structures (cf. **Figure 4.2b**) and to eliminate the possibility of slot modes between grounds of adjacent structures. A picture of the whole chip is also provided in **Figure 4.3** for better visualization.

Standards characterization

Measurements of the calkit standards, dut and de-embedding structures have been performed with (i) FormFactor Infinity I67 probes ('I67') from 0.1 to 67 GHz and (ii) with Picoprobe GGB 110 GHz ('GGB'), (iii) MPI TITAN 110 GHz ('TITAN') and (iv) FormFactor Infinity I110 ('I110') probes from 0.2 to 110 GHz[1]. All probes have a 100 µm pitch. The 0.1-67 GHz measurements are performed on a manual probe station. The 0.2-110 GHz are realized on a semi-automatic MPI probe station, along with East motorized positioner. First-tier calibrations are performed on the commercial calibration substrate specific to each probe technology (LRRM on 101-190C for I67; LRRM on CS15 for

[1]As explained in **Chapter 2**, all '110' GHz measurements have been performed up to 130 GHz. However, the connectors are specified up to 110 GHz. Resonances appear at 120 GHz that can be temporarily corrected after calibration. So, sometimes measurements up to 130 GHz are shown, which come from the same data set as the 110 GHz data.

GGB; mTRL on AC-2 for TITAN; LRRM on 104-783A for I110)[2], with these substrates lying on a ceramic chuck for the 0.2-110 GHz measurements and a metallic chuck for the 0.1-67 GHz measurement. The test chips are measured on top of a metallic chuck[3] [4]. The first-tier calibrations are realized with WinCal XE software and subsequent processing (including second-tier calibrations) are performed with in-house Matlab scripts.

The first step is to characterize the transmission line standards. As seen in **Chapter 2**, they are fully described by the propagation constant (γ) and characteristic impedance (Z_c). γ is accurately extracted with the mTRL algorithm while Z_c is obtained with the calibration comparison technique **[74]** (**Section 2.4.1**). The extracted Z_c and γ are shown in **Figure 4.4**, along with full-wave (3D electromagnetic) simulations of the Lines standards[5].

We observe some strong bumps in measurements of the propagation constant (around 40 GHz for I67, 60-90 GHz for GGB, 40-70 GHz for I110, 50-90 GHz for TITAN) that are not expected from the intrinsic transmission lines (smooth behavior of full-wave simulations). As seen in **Chapter 2**, the mTRL algorithm extracts γ as part of the self-calibration process. Thus, the extracted γ *does not depend on the first-tier calibration*, contrarily to Z_c. As these bumps vary according to the probes, they are attributed to probe coupling with the nearby on-wafer environment. We will further discuss about the probe-dependent bumps later in the text.

There is an overall satisfying agreement between the simulations and the

[2] Ideally the mTRL method should have been used as first-tier calibration for all probe measurements, as it provides the most reliable and robust calibration in case of probe misplacement (cf. **Chapter 2**). However, measurements with this calibration are only available for the TITAN probes.

[3] Measurements of other, similar structures, have been performed on a ceramic chuck and on an absorber with no visible impact on measurements. This could be expected as the whole chip is covered by a ground plane in the BEOL metal layers.

[4] These 22FDX chips have a really small area (2x2.5 mm^2) and are immobile if placed directly on the chuck (their area is too small to cover multiple aspiring holes that normally hold the wafers still). So, they are preliminary 'stuck' to a dummy (standard resistivity Si) wafer with a special resin. In that way, the 22FDX chips do not move when probes land on the structures and the chips are approximately planar (one does not need to planarize the probes above each chip, which is rather time consuming and requires untouched probe pads). The native oxidation of Si does not guarantee that the metallic chuck fixes the chips' backside bias. However, an ohmic contact designed under each ground pad ensures that the chips' substrate is at 0 V. The chip thickness is 254 µm and the supporting Si wafer is 500-700 µm.

[5] 3D EM simulations performed with HFSS using a wave ports excitation of intrinsic transmission line.

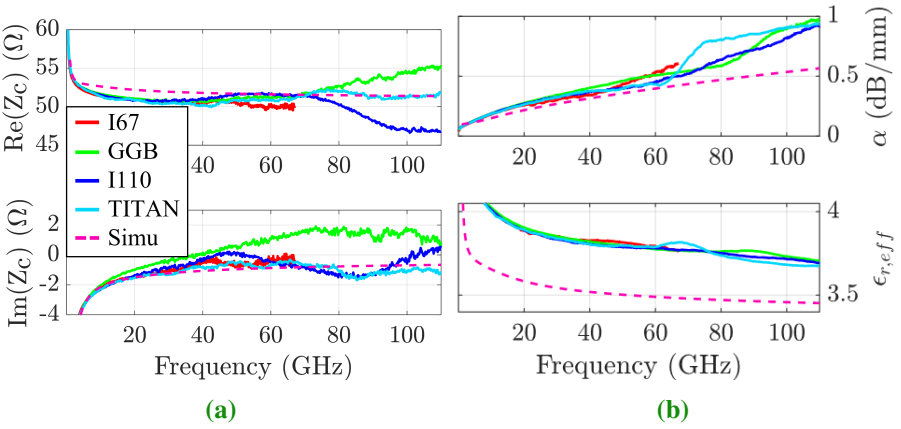


Figure 4.4: Extracted characteristic impedance (a) and propagation constant (b) extractions from transmission line standards measurements.

measured γ and Z_c. A small $\sim 7\,\%$ discrepancy in $\varepsilon_{r,eff}$ remains, which might be explained by fabricated structures with material parameters that slightly deviate from their typical values that are used in the simulation (different metal conductivity or dielectric permittivity values). Better agreement could be achieved by accounting for potential fabrication corners variation, fewer layout simplification, etc., but an exact agreement is out of scope of this thesis.

The extracted characteristic impedance also varies significantly from probe to probe. Contrarily to γ, Z_c does depend on the first-tier calibration. So, the probe-to-probe variations can be partially explained by significant systematic deviations coming from the first-tier calibration performed on different calibration substrates and with different calibration methods (LRRM, mTRL), as seen in **Chapter 2**. Then, there are still some bumps that seem correlated (similar frequency range) to the observed bumps in γ.

We could also have used the load method **[66, 67]** to compute Z_c from propagation constant measurement, assuming the per-unit-length C is constant and $G = 0$. Let us apply it here to the I110 probes measurement as it features the smoother γ. **Figure 4.5** shows the extracted Z_c, per-unit-length C and G terms from the transmission line using different methods. As we clearly see in **Figure 4.5c-d**, *C is not constant with frequency* and *G is clearly positive*, thus invalidating the two assumptions used in the benchmark method to evaluate Z_c. So, using this method should induce a significant error in extraction.

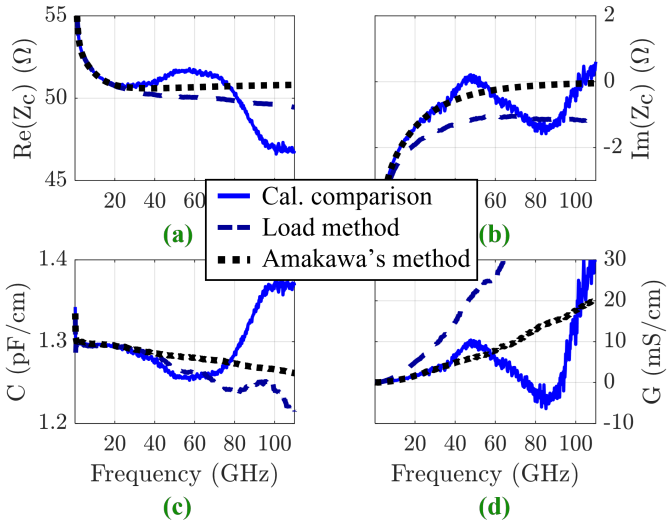


Figure 4.5: Extracted characteristic impedance (a, b), per-unit-length C (c) and G (d) terms, with the calibration comparison (solid lines), load method (dashed lines) [66, 67], Amakawa's method [24] (black dotted lines), from I110 measurements.

Another way to evaluate Z_c could have been from accurate EM simulations [78]. However, more effort should have been devoted to get a better agreement with EM simulation.

Instead, let us investigate an interesting method that has recently been proposed by Amakawa [24]. This method makes the assumption that the first-tier calibration and the calibration comparison technique yield meaningful Z_c at 'low frequencies' (up to 67 GHz in their work). This 'low-frequency' data is used to fit a shunt admittance network that is extrapolated to obtain $G(f)$ and $C(f)$ curves over the whole frequency range (up to 220 GHz in [24]). Finally, Z_c is extracted as

$$Z_c = \frac{\gamma}{G(f) + j\omega C(f)}. \tag{4.1}$$

By synthesizing a meaningful shunt admittance network (shown in Figure 4.6), this method yields a *causal*[6] characteristic impedance. The third order

[6]Every physical system is causal and therefore responds to an excitation starting at time $t = 0$

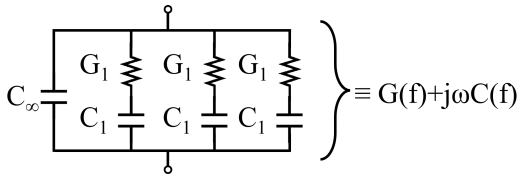


Figure 4.6: Shunt admittance network used to fit 'low-frequency' (< 35 GHz) measurements and extrapolated to higher frequencies (up to 110 GHz) in Amakawa's Z_c extraction method [24].

network shown in **Figure 4.6** has been used to fit measurement data up to 35 GHz, where no bump in γ or Z_c is observed for any probes. This method is applied to the I110 probe data shown above in **Figure 4.5** (black dotted lines), and we observe a much smoother behavior in Z_c that is behaving above 40 GHz in a much better way than the Z_c uniquely extracted from the calibration comparison technique (especially in its real part above 80 GHz).

Amakawa's technique can be seen as a 'correction' method in which we use the 'reliable' low-frequency data to fit a meaningful electrical model and extrapolate it to 'correct' the higher frequency data. This technique is also applied to the other probe data and its 'corrective' effect will be evaluated on the extrinsic parameters extraction of a MOSFET. **Figure 4.7** shows the Z_c from (i) direct calibration comparison and (ii) Amakawa's method for the other probes data. As we can see, the amount of 'correction' provided by Amakawa's method varies from negligible (I67) to very important (I110 and GGB) and so will be affected the corrected results in the following.

As we have seen from the measured γ, there are some significant probe-dependent effects in the measurements of calibration standards that will be propagated in corrected measurements of other structures. To help identifying the origin of these effects, let us analyze the Open-M1 measurements with different probes.

Probe-dependent measurement errors

To clearly evidence probe-dependent effects, let us first work with measured data that have only been corrected by the first-tier -'probe-tip'- calibration made on a commercial calibration substrate. Reflection coefficient measurements with reference plane at the probe tips of the 'Open-M1' de-embedding structure

only at $t \geq 0$. If a system responds to the excitation at $t < 0$, it is said to be non-causal [24].

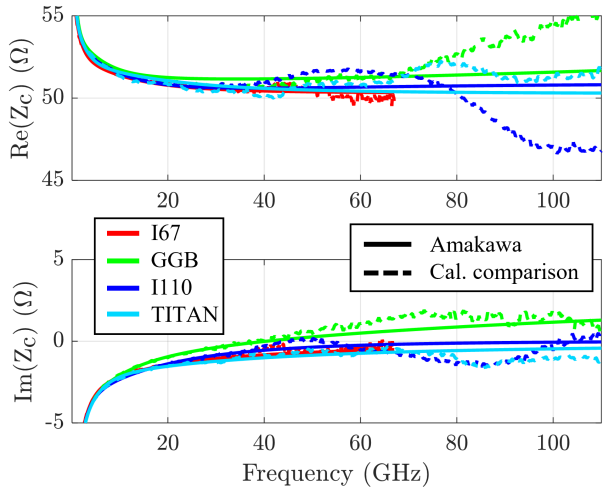


Figure 4.7: Extracted characteristic impedance calibration comparison (dashed lines) and Amakawa's method **[24]** (solid lines) for different probes.

are shown in **Figure 4.8a**.

A strong bump is systematically observed in the magnitude of the reflection coefficients. Furthermore, the bump is different for the left and right probes. *The frequency at which these bumps occur and their magnitude vary according to the probe technology, and absolute position of the structure on the chip*. Indeed, this is clearly observed by comparing the $|S_{22}|$ at **Figure 4.8b** of two Open de-embedding structures at different locations on the chip. One of them is toward the center of the chip, while the second one is closer to the right edge. A sketch representing the two measurement situations is shown in **Figure 4.9**. Although the two Open de-embedding structures are not exactly the same structures, their intrinsic electrical behavior should not feature such bumps. So, the strong bumps are evidently due to probe coupling to the on-wafer environment, which varies between these two Open de-embedding structures.

Furthermore, we observe that the $|S_{22}|$ of the *I110 measurement is even more sensitive to the on-wafer environment*, as the variation is stronger than for the other I67 and GGB probes (such measurement is not available for the TITAN probe). The GGB probe measurements also exhibit a strong bump, but (i) at higher frequency, and (ii) the two curves are in good agreement up to $\sim 50-60\,\text{GHz}$ (whereas deviation in the two $|S_{22}|$ is already observed around

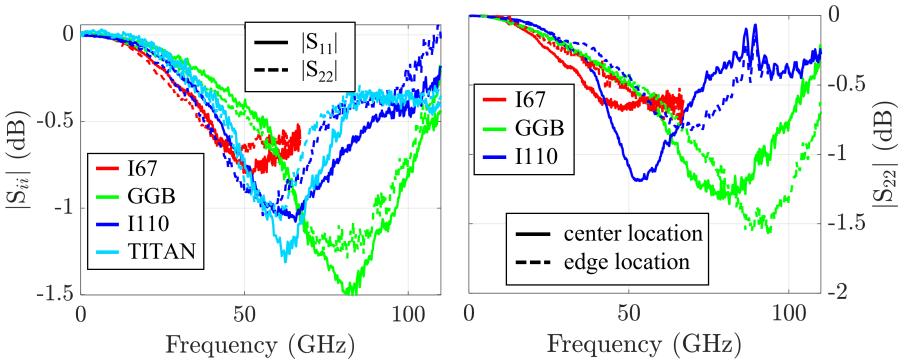


Figure 4.8: Reflection coefficient magnitude of Open-type de-embedding structures. Measurements with different probes corrected after first-tier calibration only (reference plane at probe tips). (a) Open-M1 de-embedding structure, $|S_{11}|$ (solid lines) and $|S_{22}|$ (dashed lines). (b) $|S_{22}|$ of two similar Open-type de-embedding structures, one at the center of the chip (solid lines), the other close to the right edge (dashed lines): see measurement situation in **Figure 4.9**.

20-30 GHz for the two pairs of Infinity probes).

These trends with GGB and I110 probes[7] have recently been observed and explained in **[40]** in terms of the nature of probe coupling. Fregonese *et al.* show via 3D EM simulations reproducing the measurement conditions (including a probe model and neighbor calkit structures) that the trends in I110 measurement is mainly explained by a strong and localized coupling between the I110 probe and the on-wafer test structures due to the presence of a solder joint in the probe that is $\sim 500\,\mu$m away from the probe tips and $\sim 176\,\mu$m above the substrate (its picture is shown in **Figure 2.3b**). The probe to on-wafer environment is more distributed for the GGB probe. Indeed, it is less sensitive to the test structure environment (as seen in **Figure 4.8b**), as there is not such strong and localized coupling happening that far away from the probe tips. However, it still suffers from larger probe to probe crosstalk than I110 probes, which degrades measurement accuracy at higher frequencies.

Such a detailed EM analysis of 110 GHz TITAN probes coupling with

[7] Another 'signature' of I110 probes present in measured data that has not been shown so far is a 'wavy'-like frequency behavior. It will be evidenced later on in the text.

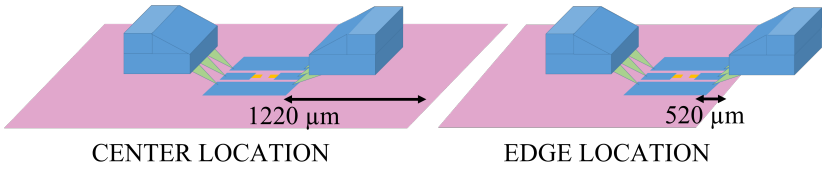


Figure 4.9: Sketch of the two Open-type de-embedding structures measurements: chip center location (left) and chip edge location (right).

on-wafer test structures on Si-based technology has not yet been reported to the best of our knowledge[8]. However, we will see in the following that TITAN probe measurements exhibit a 'wavy'-like behavior with frequency, similar to I110 probes, but with some differences in behavior, mainly in the upper frequency range.

Anyway, with the effort of reproducing a similar environment for each measured structure, one could hope that some of these undesired effects are corrected (or at least attenuated) with a second-tier in-situ calibration. The 'Open-M1' de-embedding measurements corrected with the mTRL second-tier calibration (with Z_c determined using Amakawa's method [24]) are shown in **Figure 4.10**, together with PDK parasitic extraction (PEX, up to QB) simulations. The reference plane after the second-tier in-situ mTRL calibration is in QB, as illustrated in **Figure 4.2a**. The measured capacitances C_{ij} from the π-equivalent model are also shown. They are computed from the Y-parameter measurements as

$$C_{12} \equiv -\mathrm{Im}(Y_{12})/\omega,\ C_{11} \equiv \mathrm{Im}(Y_{11}+Y_{12})/\omega, \\ \text{and } C_{22} \equiv \mathrm{Im}(Y_{22}+Y_{12})/\omega. \quad (4.2)$$

The PDK parasitic extractions agree well, mostly in terms of capacitance, with roughly frequency-independent C_{11} and C_{22}. C_{12} deviates at similar frequencies as the bump in reflection coefficients, which is explained by probe coupling too [40]. The reflection coefficients are partially corrected (compared to **Figure 4.8**), but a bump is still present in measurements.

This non-ideal correction could have been expected as mTRL is based on an 8-term error box and does not account for crosstalk terms. So, it is unlikely to accurately correct probe-to-probe crosstalk. In addition, mTRL

[8] Neither with Allistron probes, previous model on which TITAN probes are based.

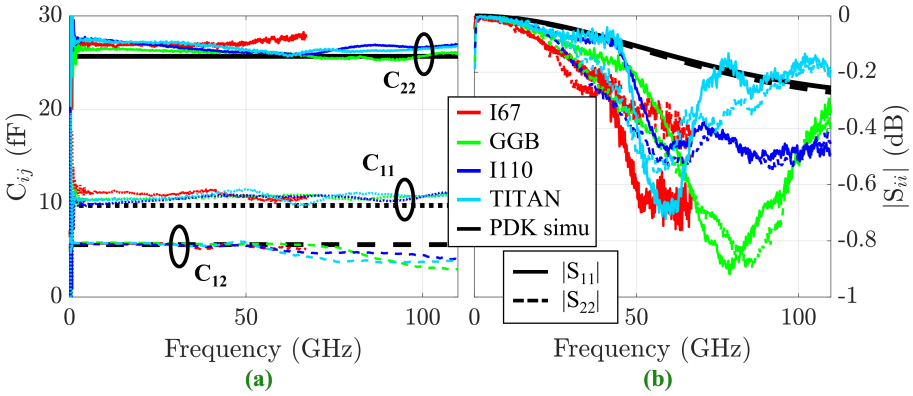


Figure 4.10: 'Open-M1' measurements with different probes, corrected by in-situ second-tier calibration. Reference plane in QB. Capacitance measurements (a) and reflection coefficient magnitude (b).

assumes there is only one mode propagating inside the transmission line, while the bumps in measured γ (**Figure 4.4**) suggest the existence of several modes propagating on-wafer, thus degrading the accuracy of mTRL calibration. Finally, due to the distributed nature of the crosstalk (mainly for GGB probe), even SOLT algorithm (with two crosstalk terms) fails to correct well these parasitic behaviors **[40]**. The final de-embedding step will provide a further correction to the transistor measurements, which should (hopefully) reduce the parasitic effects including the bumps. This is evaluated next.

4.1.2 Analysis of different de-embedding strategies

By correcting measurements with the second-tier mTRL calibration using Amakawa's method to determine the Line standards characteristic impedance, we have anticipated the results from this part. Indeed, we will demonstrate here that this specific measurement correction strategy yields the best and most meaningful results for all tested RF probes.

To evaluate the accuracy of a calibration/de-embedding strategy we will compare them via the extraction of the extrinsic series resistances of a MOSFET, based on *corrected measurements with reference plane in M1*. They are critical parameters to model the FET behavior, and its gate resistance (R_g) in particular is very sensitive and tricky to extract. Bracale's method **[120]** has been proved

to be a robust method to extract the series extrinsic resistances in case of measurement noise [121]. It is based on the measurement of the FET in cold and strong inversion regimes ($V_{ds} = 0\,\mathrm{V}, V_{gs} \gg V_{th}$). The measurements under such conditions (port 1 connected to the gate, port 2 to the drain) yield the following expressions:

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g - \frac{1}{4g_d} \tag{4.3}$$

$$\mathrm{Re}(Z_{22}) = R_{sd} + \frac{1}{2g_d} \tag{4.4}$$

where R_g is the extrinsic gate resistance, R_{sd} is the sum of the series source and drain resistances, g_d is the output conductance. g_d is proportional to the overdrive voltage ($V_{gs} - V_{th}$), such that its contribution to the above expressions becomes smaller with larger gate voltage.

In Bracale's method, Equation 4.3 and Equation 4.4 are evaluated for several V_{gs} biases and a linear regression from their values is used to get rid of the $1/g_d$ term. The goal being to compare measurement and extraction accuracy, we only present Equation 4.3 and Equation 4.4 versus frequency at the highest recommended V_{gs} bias of the technology (0.9 V), instead of extracting the actual series resistances values (R_g and R_{sd}). Nevertheless, Equation 4.3 and Equation 4.4 are expected to be constant with frequency (above a few GHz for Equation 4.3). Indeed complete expressions for Equation 4.3 and Equation 4.4 in terms of the FET small-signal equivalent circuit parameters can be found in [121]. Any frequency-dependent deviation is attributed to inaccuracy in measurement extraction.

In the following we test two types of calibration/de-embedding strategies. First, we compare two entirely de-embedding-based procedures to the in-situ second-tier calibration. Then, we study the effect of different methods to evaluate Z_c of transmission line standards on MOSFET extrinsic resistances extraction. All subsequent MOSFET measurements shown have a reference plane in M1.

Different de-embedding strategies

The Open-Short de-embedding is the classical de-embedding used in most cases. However, its accuracy is limited in frequency due to the distributed nature of the accesses. For high-end mm-wave measurements, the best calibration-de-embedding strategy consists of performing an in-situ calibration with a custom calkit to move the reference plane as close as possible to the device, followed

by a classic Open-Short de-embedding [29, 30]. To keep it concise, we study the effect of three different strategies: (i) 2-tier calibration with Open-Short de-embedding that serves as reference, (ii) 'off-wafer'[9] (or 'probe-tip') calibration followed by an Open-Short de-embedding, (iii) 'off-wafer' calibration followed by a more complex 5-step de-embedding, similar to the one proposed in [119].

(i) The 2-tier calibration consists of performing a first-tier calibration on a commercial calibration substrate (either LRRM or mTRL according to availability, see Section 4.1.1) to move the reference plane to the probe tips, followed by a second-tier calibration performed with the calkit embedded on the same wafer as the dut(s). The in-situ calibration structures have to present a neighboring environment as close as possible as dut's close environment to include probe coupling to neighboring structures [116]. The second-tier calibration moves the reference plane at the dut's vicinity, effectively removing the pads and some access parasitics. Then, an Open-M1-Short-M1 de-embedding is applied to remove additional parasitics down to the extrinsic accesses at M1.

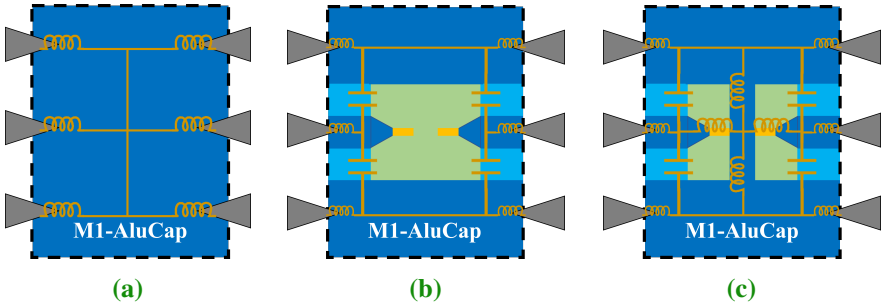


Figure 4.11: Sketch three de-embedding structures: 'Probe-SHORT', 'OPEN-Top', 'SHORT-Top' and equivalent access network used in steps (a) to (c) from the 5-step de-embedding approach. Steps (d) and (e) accounts for parasitics from QB to M1 close to the dut (red square) and are not shown here.

The latter correction procedure is compared to an 'off-wafer' first-tier calibration performed on the commercial calibration substrate followed by two different de-embedding procedures.

(ii) In the first one, a classic Open-M1-Short-M1 de-embedding is applied, which is the usual method applied in industries.

[9] First-tier calibration on a commercial calibration substrate.

(iii) In the last case, the first-tier calibration is followed by a 5-step de-embedding. The complete 6-step de-embedding technique described in [29, 119] could not be applied here due to missing de-embedding structures. Instead, the 5-step de-embedding used here consists of the following sequence (Figure 4.11 illustrates steps (a) to (c), more information can be found in [29, 119]):
   (a) Probe-SHORT: short at probe tips (it reduces calibration residuals);
   (b) OPEN-Top: same structure used for in-situ (m)TRL calibration, sketch given in Figure 4.2a (it corrects the shunt impedance of pad and part of the access);
   (c) SHORT-Top: same structure used for in-situ (m)TRL calibration (it correct the series impedance of pad and part of the access);
   (d) OPEN-M1 (it corrects the shunt impedance of the metal/via access above the transistor);
   (e) SHORT-M1 (it corrects the series impedance of the metal/via access above the transistor);

Note that the OPEN-M1 and SHORT-M1 structures contain all metal lines from M1 to LB identical to the studied MOSFET, without the active part. So, all MOSFET measurements corrected with these OPEN-M1 and SHORT-M1 structures have the reference plane in M1 (which will be the case for all MOSFET measurements shown in this section).

The three different calibration/de-embedding approaches are used in the extraction of extrinsic series resistances from Equation 4.3 and Equation 4.4. Results for GGB probe measurements are shown in Figure 4.12.

The classic Open-M1-Short-M1 strategy (ii) is limited above 20 GHz, frequency at which the distributive elements of the accesses become significant and induce a decreasing $\mathrm{Re}(Z_{22})$ trend with frequency. Although the extraction is improved with the more complex 5-step de-embedding (iii), it is still diverging above ~ 40 GHz, whereas the 2-tier calibration followed by Open-Short de-embedding (i) displays a consistent behavior for $\mathrm{Re}(Z_{22})$ up to 70 GHz, then a slight increase. For the $\mathrm{Re}(Z_{11}-Z_{12})$ curves, all measurements agree well up to 60 GHz, then they all feature a bump in the 60-90 GHz range followed by a decreasing trend with frequency. The bump has been identified above as coming from probe coupling to the on-wafer environment that is not well corrected.

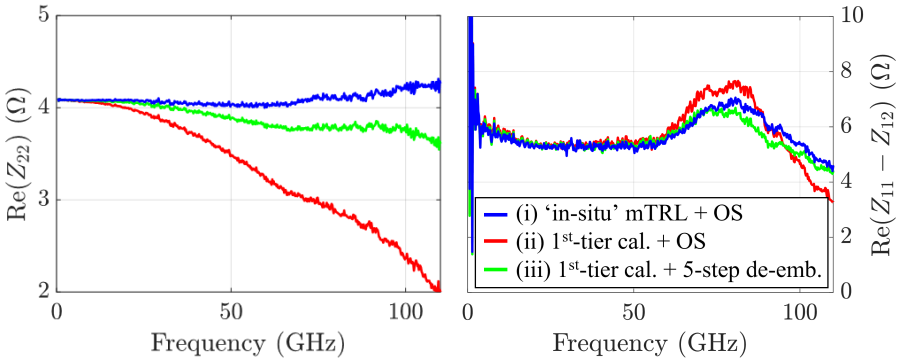


Figure 4.12: Re(Z_{22}) (a) and Re($Z_{11} - Z12$) (b) from cold FET measurement biased in strong inversion. Comparison between different calibration/de-embedding strategies for GGB probe measurements. Reference plane in M1.

Effect of Amakawa's correction to Zc

As anticipated and in agreement with [29, 30], the in-situ calibration provides the best measurement accuracy. Nevertheless, the calibration comparison technique was used to obtain Z_c of the Lines standards in the above results and the load method in [29, 30, 40]. Yet, as we have seen above, both methods are prone to error. For the load method, it highly depends on the calkit design and on the validity of the assumptions of constant C and $G = 0$. Even without such assumptions, the calibration comparison method yields Z_c with unexpected deviations at higher frequencies. The interesting correction method proposed in [24] provides a better-behaved Z_c at higher frequencies as shown above. So, we will assess the validity of these different Z_c extraction methods via the same extrinsic FET series resistances measurements used above.

Figure 4.13 shows Re(Z_{22}) and Re($Z11 - Z_{12}$) for different probes measurements corrected by the second-tier mTRL calibration using different Z_c evaluation techniques: calibration comparison, Amakawa's correction method and the load method (only shown for I110 to avoid overloading the graphs), followed by Open-M1-Short-M1 de-embedding.

As expected, the data corrected using the load method shows strong deviations, mostly in Re($Z_{11} - Z_{12}$), and it shall no longer be discussed in the following. Apart from that, there are two types of observations that can be made from **Figure 4.13**, i.e. probe-related and Z_c-extraction-related. Let us first start

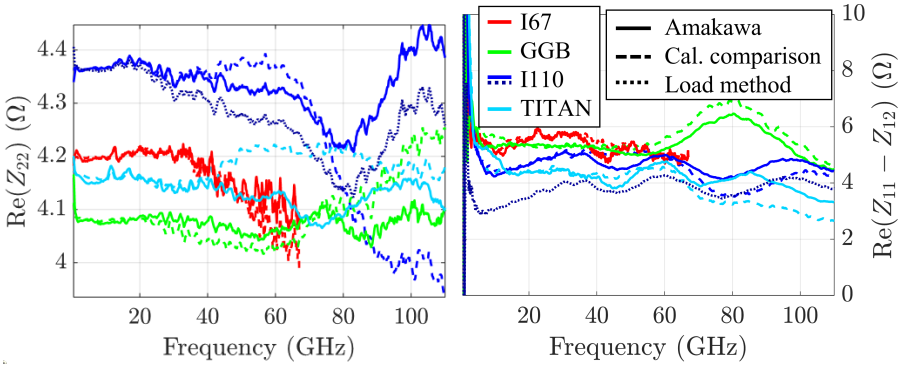


Figure 4.13: $\mathrm{Re}(Z_{22})$ (a) and $\mathrm{Re}(Z_{11} - Z_{12})$ (b) from cold FET measurement biased in strong inversion. Data corrected by 2-tier calibration with Open-M1-Short-M1 de-embedding. Reference plane in M1. Comparison between different Z_c extraction (for second-tier calibration) methods **[74]** (dashed lines) and **[24]** (solid lines), for different probe measurements.

with the latter.

In $\mathrm{Re}(Z_{22})$, we observe that Amakawa's method enables the correction of residual non-ideal behaviors (mostly for the I110 probe measurements) and an excellent consistency up to 110 GHz is achieved, *with frequency-dependent variations up to 5 % in all curves*. As for $\mathrm{Re}(Z_{11} - Z_{12})$, the bumps still present are dampened and the high-frequency roll-offs (in TITAN and I110) are decreased. With the exception of the I67 probes (for which little difference is observed already in Z_c, cf. **Figure 4.7**), Amakawa's method does a good job at correcting unexpected measured behaviors thanks to a more meaningful high-frequency Z_c extraction.

Concerning the probe to probe variations, there is little deviation ($\Delta\mathrm{Re}(Z_{22}) < 8\,\%$ and $\Delta\mathrm{Re}(Z_{11} - Z_{12}) < 24\,\%$ at 20 GHz) among the measurements with different probes. It means that all elements (FET, de-embedding and calibration structures) have been measured with high quality and repeatable contact and

that there is little die-to-die process variation[10][11]. Furthermore, **Figure 4.13b** shows the same typical probe trends made above: (i) steady behavior up to $\sim 50-60$ GHz then strong deviation for GGB probe, (ii) 'wavy' curves for I110 (and TITAN) already around 20-40 GHz but with smaller bump amplitude than GGB.

R_g (expressed as $\mathrm{Re}(Z_{11}-Z_{12})$ in cold FET, high inversion regime) is not commonly used to evaluate the extraction accuracy. Instead, the following two curves are rather used: $f_t(f) \equiv f|H_{21}|$ and/or $f_{max}(f) \equiv f\sqrt{|U|}$, H_{21} being the short-circuited-output current gain and U (Mason) unilateral power gain. However, $f_t(f)$ is not so sensitive to measurement errors, and the extrinsic FET behavior only features a frequency-independent $f_{max}(f)$ above ~ 20 GHz (it can be observed from measurements in the following sub-section). On the other side, R_g (as $\mathrm{Re}(Z_{11}-Z_{12})$) *is just as sensitive to measurement errors as* $f_{max}(f)$ *and should feature a frequency-independent behavior* (already above 5-10 GHz), which makes it a pertinent figure of merit (FoM) to evaluate the extracted results accuracy.

As a last step, let us analyze the effect probes and their related residual errors have on the measurements of extrinsic FET parameters.

4.1.3 Extrinsic MOSFET characterization up to 110 GHz

The measurements in the rest of this section are corrected with the mTRL two-tier calibration using Amakawa's method to determine Z_c, then de-embedded with the classic Open-M1-Short-M1. The reference plane is thus in M1. nMOSFET measurements (and simulations) biased in saturation (nominal $V_{ds} = 0.8$ V) and at peak f_t (corresponding to $V_{gs} = 0.6$ V, for $V_{bg} = 0$ V) are shown in the following. The measured extrinsic parameters displayed in **Figure 4.14** are

[10] Guaranteeing a high-quality contact during measurements is critical for correct dut characterization, whether it be transmission lines, FETs, inductors, etc. In Si-based technologies, the top metal layer is usually aluminum, which oxidizes in presence of air forming a thin dielectric sheet that needs to be crossed by the probes for each contact. Even though some RF probes have been especially designed for Alu pad contact **[122]**, high-quality contact is still tricky to achieve while measuring Si-based devices. A practical procedure provided in **Appendix C** helps identifying a contact issue for many types of duts during measurements. It is critical to detect contact issues at the early phase of characterization, i.e. during measurements instead of data processing, thus saving a lot of overall characterization time.

[11] Accurate measurements with GGB probes especially are difficult to accomplish on Alu probe pads **[71]**. The little offset in $\mathrm{Re}(Z_{11}-Z_{12})$ curves could be explained by (i) a contact of slightly lower quality with GGB (and I67) probes and (ii) error during first-tier calibration. The latter is further explored in **Appendix B**.

defined as

$$f_t \equiv f|H_{21}|, \tag{4.5}$$
$$f_{max} \equiv f\sqrt{|U|}, \tag{4.6}$$
$$g_m \equiv \mathrm{Re}(Y_{21}), \tag{4.7}$$
$$g_d \equiv \mathrm{Re}(Y_{22}), \tag{4.8}$$
$$C_{gg} \equiv C_{gs} + C_{gd} \equiv \mathrm{Im}(Y_{11} + Y_{12})/\omega - \mathrm{Im}(Y_{12})/\omega, \tag{4.9}$$
$$C_{ds} \equiv \mathrm{Im}(Y_{22} + Y_{12})/\omega. \tag{4.10}$$

Note that the parameters defined above include the effect of intrinsic and extrinsic MOSFET elements. These parameters depend only weakly on frequency, and they are often used as metrics to evaluate the ability of a calibration to measure MOSFET parameters **[9, 29, 30, 77]**.

Except for a larger spread in $f_{max}(f)$, all probe measurements agree very well with each other up to ~ 70 GHz. Beyond 70 GHz, each probe data show distinct deviations. These almost overlapping curves give great confidence in measurement accuracy up to ~ 70 GHz and their deviations beyond 70 GHz seem to provide an interval within which should lie the actual FET electrical behavior.

The $f_{max}(f)$ curves exhibit larger variations from probe to probe *and* across frequency. It is, as mentioned earlier, a very sensitive parameter that is difficult to accurately extract **[40, 123, 124]**, in particular for technologies featuring high f_{max} values (such as this one). Even though it features impressively large bumps (up to ~ 100 GHz deviation), it is in the same order of relative variations (up to $\sim 25\,\%$) as R_g observed above. However, its measured behavior is not so constant with frequency as observed from the steady decreasing trend in measurements above 10 GHz (as opposed to R_g), which makes R_g an interesting sensitive alternative to evaluate residual measurement error.

Finally, the very good agreement obtained in general with the PDK's compact model simulations further confirms that despite the residual probe-dependent errors, a high measurement accuracy up to 110 GHz is achieved with the selected extraction procedure. It also demonstrates the very high accuracy provided in general by these 22FDX technology's models, which leads to the excellent measurement-simulation agreement in the designed circuits from the next chapter. However, there are some systematic discrepancies between our measurements and the simulations that are worth pinpointing.

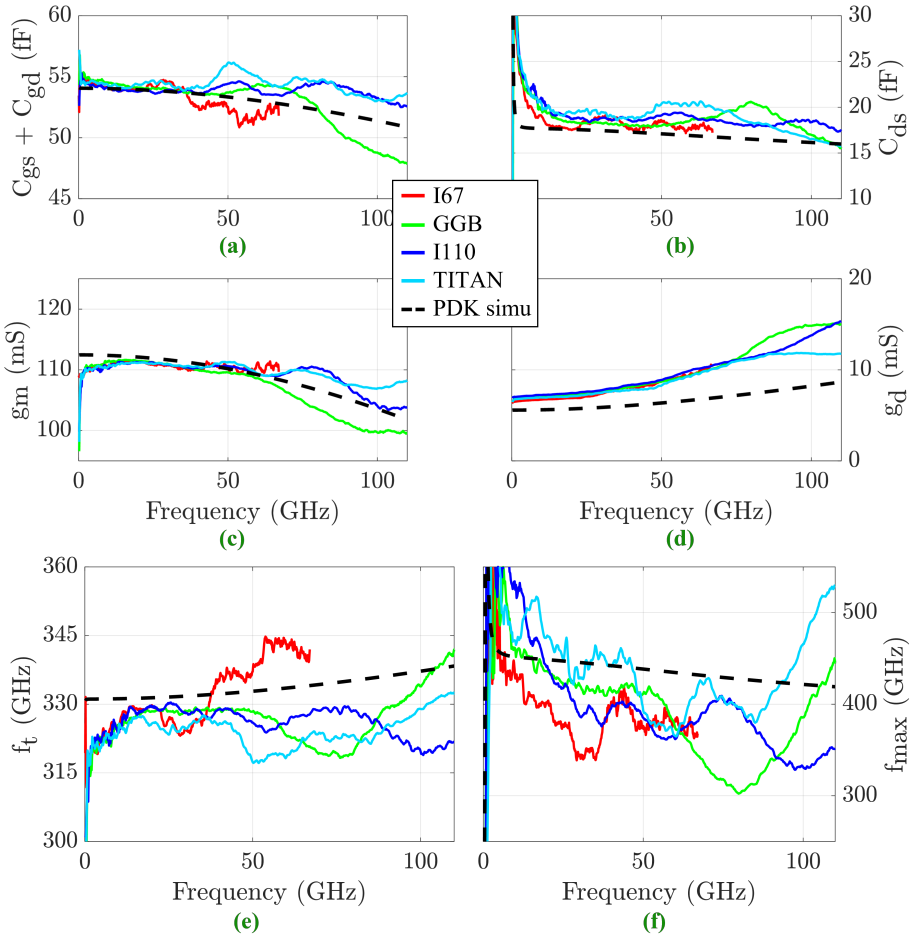


Figure 4.14: Extrinsic FET parameters C_{gg} (a), C_{ds} (b), g_m (c), g_d (d), f_t (e) and f_{max} (f), measurements (solid lines) for different probe technologies and compact model (from PDK) simulations (black dashed lines). FET biased in saturation and peak f_t regime: $V_{ds} = 0.8\,\mathrm{V}$, $V_{gs} = 0.6\,\mathrm{V}$ and $V_{bg} = 0\,\mathrm{V}$. Reference plane in M1.

- First, although not so obvious because of the graphs scale, there is a stronger discrepancy ($\sim 20\,\%$) in the 'low-frequency' (below 20 GHz) value of g_d compared to all other parameters (except perhaps for f_{max} that features a larger variation among different probe data). It is better observed in **Figure 4.15** that shows a zoomed-in view of **Figure 4.14d**.
- Next, we observe a faster frequency increase (up to at least 70 GHz) in g_d in measurements than in simulations.
- Two other systematic discrepancies concern the low-frequency (below 10-20 GHz) trends. One of them is clearly observed in g_m and f_t (propagated from g_m, as $f_t \approx g_m/(\omega C_{gg})$). Indeed, both measured g_m and f_t decrease below 10 GHz, while simulations stay constant.
- Finally, another (less notable) divergence is visible in C_{ds} below 20 GHz. Measurements as well as simulations exhibit an 'elbow' but at different frequencies: around 2 GHz for simulations and 12 GHz for measurements.

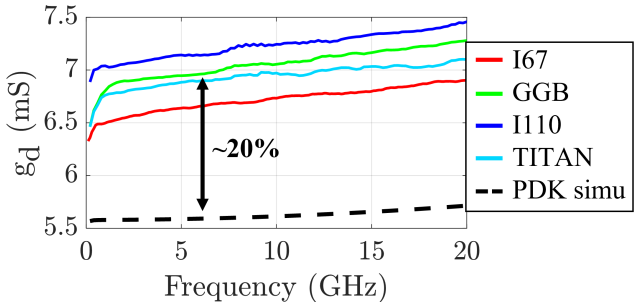


Figure 4.15: Zoomed-in extrinsic g_d measurements (solid lines) for different probe technologies and compact model (from PDK) simulations (black dashed lines). FET biased in saturation and peak f_t regime: $V_{ds} = 0.8\,\text{V}$, $V_{gs} = 0.6\,\text{V}$ and $V_{bg} = 0\,\text{V}$. Reference plane in M1.

Even though the reported divergences are small and do not prevent an overall excellent measurement-simulation agreement. They warrant some physical phenomena that are either not considered or not well modeled by the current PDK's compact model, which invites us to further investigations.

The discrepancies being mainly related to 'low-frequency' Y_{22} (g_d and C_{ds}) and Y_{21} (g_m), it suggests the consideration of two important phenomena known to directly impact at least one of these two electrical parameters: *dynamic self-heating effect* **[113, 125–128]** and *substrate effect* (or substrate-related

coupling) **[129, 130]**. Characterization and modeling of these two phenomena are studied in details in the next section via the measurements of 20 nm UTBB FD-SOI MOSFETs.

4.2 On the Separate Extraction of Self-Heating and Substrate Effects in FD-SOI MOSFET

The aggressive downscaling in CMOS technology results in higher current and power densities, thereby increasing the self-heating (SH) effect and the lattice temperature (T_c, also called channel temperature, i.e. temperature of intrinsic device). Increase of lattice temperature induces undesirable effects like mobility reduction, threshold voltage (V_{th}) shift, lower output current and reduced reliability [7, 112] and is therefore important to appropriately characterize.

While there are several methods to extract self-heating effect (pulsed-IV, gate resistance [114, 115]), the method most suited to these advanced 20 nm FD-SOI devices is the RF method [114]. This method [113, 125–127, 129, 131–134] relies on the fact that dynamic self-heating induces a transition in the Y-parameters over frequency, in particular in the Y_{22} parameter. So, self-heating is usually characterized from the measured step in output conductance over frequency. An example of such a curve is provided in Figure 4.16. The extraction procedure will be further detailed later on.

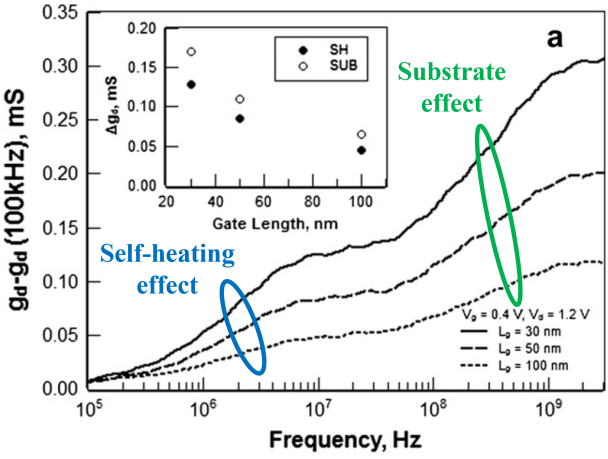


Figure 4.16: Experimental data showing distinct self-heating and substrate effects in $g_d(f)$ of an old FD-SOI technology [135].

However, the drain to source coupling through the back-gate (B-G) node (or Si substrate under the BOX, also called body) is also known to induce a transition in the Y-parameters in a similar frequency range [130, 135] (called

substrate effect, SE). An example of such a transition in an old FD-SOI technology is shown in **Figure 4.16**. In this case, the self-heating- and substrate-related transitions in $g_d(f)$ are distinct, which enables their separate characterization without ambiguity.

Although this substrate-related transition was originally very pronounced in FD-SOI devices with thin BOX **[135]** (cf. **Figure 4.16**), the introduction of a highly-doped region below the BOX demonstrated a strong reduction in this SE transition **[113]**. The transition associated to the coupling via substrate is thus usually neglected or ignored in these devices, which may lead to misinterpretation and erroneous modeling of SH **[113, 133]** and substrate effects.

To the best of our knowledge, no prior work to **[128]** has proposed to separately characterize each contribution, i.e. SH and substrate effect, from Y-parameters frequency response. In this section, as a first step, we will (i) demonstrate that the SE partially overlaps SH effect (SHE) in the studied device forming a common, indistinguishable distributed transition from 100 kHz to 10 GHz, (ii) show that the dynamic SH effect vanishes at the zero-temperature coefficient (ZTC) bias point, (iii) use this bias point to extract the SH-free transistor electrical model including the B-G and substrate nodes, (iv) extract the frequency-dependent thermal impedance ($Z_{th}(f)$) for different biases, and (v) compare it to the conventional extraction procedure that neglects the transitions associated to the B-G node. The results presented in this part have already been published in **[128]**.

Then, as a second step, we will address some points raised in the first step, namely (i) assess the accuracy of the PDK compact model, (ii) give a physical interpretation of the extracted thermal-related parameters, and, (iii) finally, discuss the validity of extracted substrate and back-gate networks and propose different means that lead to more accurate results.

4.2.1 Dut and measurement setup

This section presents measurements of an FD-SOI super-low threshold voltage (SLVT) nMOSFET from 22FDX® **[136]** featuring a gate length of 20 nm, finger width of 0.5 µm, 20 fingers and a multiplicity of 6 for a total width of 60 µm. Its S-parameters are measured on-wafer from 100 kHz to 10 GHz using a wideband N5291A VNA from Keysight, coupled with a probe station hosting a thermal chuck for additional dc I-V measurements at 300, 320, 335, 350, 370 and 390 K. The back-gate voltage (V_{bg}) is set to 0 V. The RF MOSFET is

probed using 100 µm-pitch Ground-Signal-Ground (GSG) RF probes[12]. The port 1 is connected to the FET gate terminal and port 2 to the drain, while the FET is in common-source configuration (so $V_s = 0\,\mathrm{V}$ implicitly). So, indices g and d refer to port 1 and 2, respectively. The back-gate terminal is connected to a dc pad, with a large ($\sim 10\,\mathrm{pF}$) on-chip shunt capacitor to the ground. This shunt capacitor presents a low impedance at RF frequencies to the back-gate terminal.

A Short-Open-Load-Thru (SOLT) calibration[13] is performed and dedicated Open-M1 and Short-M1 structures are measured to de-embed the transistor measurements down to the first metal layer. We have seen that this de-embedding approach accuracy is degraded above 20 GHz. However, the effects to be analyzed in this section are limited to a few GHz. So, this de-embedding procedure should yield accurate results in the studied frequency range.

4.2.2 Dynamic self-heating effect

The conventional RF method that extracts SH parameters from S-parameter measurements **[126, 131, 132]** relies on the fact that the lattice temperature is able to follow a "slowly" (with respect to its thermal time constant) varying ac signal, but ceases to follow the ac signal if it is too 'fast'. In other words, a time-varying $I_d(t)$ induces a time-varying $T_c(t)$ (due to varying power consumption) for low-frequency ac signals. Whereas $T_c(t)$ remains constant (cannot follow) time-varying $I_d(t)$ of high-frequency ac signals (above the *dynamic-self-heating-free* frequency). This difference in behavior leads to a step between the low- and high-frequency values of Y_{dd} (Y_{22}) and Y_{dg} (Y_{21}). This so-called dynamic SH effect has been rigorously put into equations for a general two-port device

[12] FormFactor Infinity I110 for RF measurements and FormFactor |Z| probes for dc I-V measurements.

[13] Although the mTRL calibration was identified to give the best results at mm-wave frequencies in **Chapter 2**, it is not the case at very low frequencies. Indeed, the (m)TRL low-frequency validity depends on the longest line difference as explained in **Section 2.3**, which is limited by the available Lines in the commercial calibration substrate. In practice we have found that the mTRL calibration significantly deviates from LRRM and SOLT below $\sim 1\,\mathrm{GHz}$, such that lumped-based calibration methods should instead be used for the considered frequency range ($100\,\mathrm{kHz} - 10\,\mathrm{GHz}$). SOLT's accuracy compared to LRRM's is mainly degraded due to wrong reactive element modeling of the measured Reflect standards. Since the contribution of reactive elements are small at low frequencies, SOLT calibration yields good results below $\sim 20\,\mathrm{GHz}$ in general **[29, 30]**.

in [125]:

$$Y_{ij} = Y_{ijT} + Z_{th}\frac{\partial I_i}{\partial T_A}\left(V_g Y_{gjT} + V_d Y_{djT} + I_j\right),\ i,j = g,d. \tag{4.11}$$

with Y_{ijT} being the *isothermal* Y-parameters, i.e. when the lattice temperature does not vary with the ac signal. The Y_{ijT} parameters are by definition not affected by dynamic self-heating. T_A is the ambient temperature (or chuck temperature). In our case (MOSFET device), $\frac{\partial I_g}{\partial T_A} \approx 0$ so that $Y_{gg} = Y_{ggT}$ and $Y_{gd} = Y_{gdT}$ (if any frequency variation in $Y_{gg}(f)$ due to dynamic self-heating is present, it is too low to be detected as it was not observed in measurements). With other simplifications applicable to our case, the equations simplify in:

$$Y_{dd} = Y_{ddT} + Z_{th}\frac{\partial I_d}{\partial T_A}\left(V_g Y_{gdT} + V_d Y_{ddT} + I_d\right), \tag{4.12}$$

and

$$Y_{dg} = Y_{dgT} + Z_{th}\frac{\partial I_d}{\partial T_A} V_d Y_{dgT}. \tag{4.13}$$

Once the Z_{th} is extracted (its extraction procedure is detailed in the following), the thermal resistance ($R_{th} \equiv \mathrm{Re}(Z_{th}(f \to 0))$) and lattice temperature rise (ΔT) are linked by

$$\Delta T \equiv T_c - T_A = R_{th} P, \tag{4.14}$$

where P is the dissipated power.

The zero-temperature coefficient bias

As detected in the above equations, self-heating characterization from this method needs RF measurements at ambient temperature (Y_{ij}) and dc I-V measurements at different temperatures to derive $\frac{\partial I_d}{\partial T_A}$[14]. Let us have a closer look at the $I_d(V_g, T_A)$ curve given in Figure 4.17.

[14] We would like to bring the attention to the reader that *in this formalism* [125], the derivative of the current with temperature is evaluated at *ambient temperature*. The actual temperature (ambient or lattice) at which the derivative should be evaluated could be subject to confusion, as it depends on the formalism, or equation used. Rinaldi [125] explicitly makes a change in variables to find Equation 4.11 that depends on the derivative of the ambient temperature that is directly measurable instead of the derivative with respect to the channel temperature (that is to be characterized).

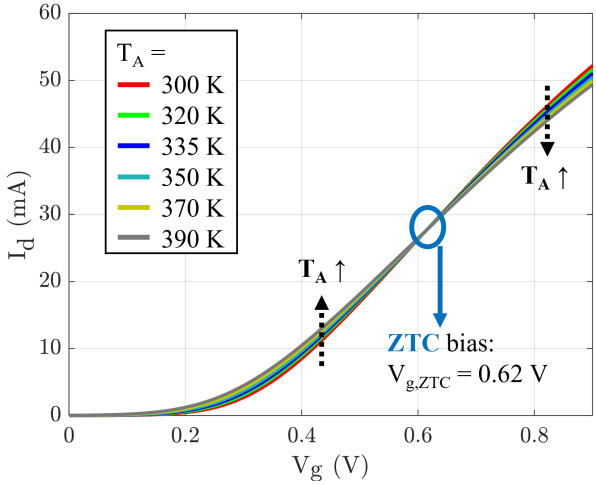


Figure 4.17: Measured I_d-V_g of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8\,\mathrm{V}$ at different ambient temperatures. The ZTC bias point is identified at $V_g = V_{g,ZTC} = 0.62\,\mathrm{V}$.

An earlier description of this RF technique [126] (also called 'ac conductance technique'), which was later used in other papers [114], uses another formulation that requires to evaluate the derivative of the current with respect to the *channel* temperature. Although omitting this detail leads to small errors in the 300-400 K range, it is fundamental when dealing with cryogenic temperatures as $I_d(T_A)$ becomes non-linear [137].
To finalize this long footnote, let us compare the equations using the two formalisms and highlight their differences. In [125], using the *ambient temperature*, the high-frequency (HF, isothermal frequency) to low-frequency (LF) transition in g_d gives:

$$g_{d,HF} - g_{d,LF} \approx R^{\star}_{th} \frac{\partial I_d}{\partial T_A}(g_{d,HF} V_d + I_d),$$

$$\text{where } R^{\star}_{th} \equiv \mathrm{Re}(Z^{\star}_{th,LF}) \text{ and } Z^{\star}_{th} \equiv \frac{1 + \frac{P}{Z_{th}} \left.\frac{\partial Z_{th}}{\partial P}\right|_{T_A}}{1 + P \left.\frac{\partial Z_{th}}{\partial T_A}\right|_{P}} \cdot Z_{th}, \quad (4.15)$$

and the same transition with the other formulation [126] (w.r.t. *channel temperature*):

$$g_{d,HF} - g_{d,LF} \approx R_{th} \frac{\partial I_d}{\partial T_c}(g_{d,LF} V_d + I_d). \quad (4.16)$$

Note how the g_d is either evaluated at high frequency, or at low frequency according to the formalism used, and the correction term introduced in **Equation 4.15** to account for non-constant

Due to the threshold voltage reduction with increasing temperatures, I_d increases with T_A at low V_g. Whereas I_d decreases with T_A for large V_g biases, because of stronger phonon scattering decreasing carrier mobility. These two mechanisms compensate each other at the ZTC bias point [138], such that the I_d associated to this bias does not change with temperature. For the studied device, the ZTC bias is $V_{g,ZTC} = 0.62\,\mathrm{V}$ for $V_d = 0.8\,\mathrm{V}$ and $V_{bg} = 0\,\mathrm{V}$.

Figure 4.18a shows the variation of $g_d(f)$ (computed as $\mathrm{Re}(Y_{dd})$). The curve for $V_g = 0.54\,\mathrm{V}$ shows a monotonic decrease in $g_d(f)$ starting from $\sim 1\,\mathrm{MHz}$ related to SH, followed by an increase for frequencies above 100 MHz that cannot be described by dynamic self-heating effect (**Equation 4.12**) and which is attributed to the SE. The SE is also present at the other biases. For $V_g > V_{g,ZTC}$, both substrate and self-heating effects contribute to a step increase in $g_d(f)$, such that the thermal resistance R_{th} (and thus lattice temperature) would be overestimated if the SE were to be ignored.

At the ZTC bias, the dynamic SH does not affect the ac curves and the observed transition (**Figure 4.18**, green data) is solely due to the SE. Similar trends are observed in the output capacitance $C_{dd}(f)$ (computed as $\mathrm{Im}(Y_{dd})/\omega$) in **Figure 4.18b**. The ZTC bias point therefore enables the extraction of the small-signal parameters associated to the B-G and substrate nodes without any dependency on the SH effects. This observation is at the basis of the extraction procedure proposed hereunder.

By taking the real and imaginary parts of **Equation 4.12**, we can derive the equations describing the dynamic SH effect on $g_d(f)$ and $C_{dd}(f)$:

$$g_d \approx g_{dT} + \mathrm{Re}(Z_{th}) \frac{\partial I_d}{\partial T_A} (g_{dT} V_d + I_d)\,, \tag{4.17}$$

$$C_{dd} \approx C_{ddT} + \frac{\mathrm{Im}(Z_{th})}{\omega} \frac{\partial I_d}{\partial T_A} (g_{dT} V_d + I_d)\,. \tag{4.18}$$

From **Equation 4.17** and **Equation 4.18**, it is plain to see that the low frequency values of g_d and C_{dd} (and the transition sign) depend on the sign of $\partial I_d/\partial T_A$, and is thereby governed by the two opposing mechanisms of mobility and threshold voltage reduction with increasing temperature [126, 131,

thermal resistance with power and ambient temperature. Even though we assume Z_{th} to be independent of power and ambient temperature, so that the two equations give roughly the same results at room temperature, extracting R_{th} from the g_d step is not recommended because of the substrate effect and poor estimation of isothermal frequency. Instead, we invite the reader to use the method described in the following.

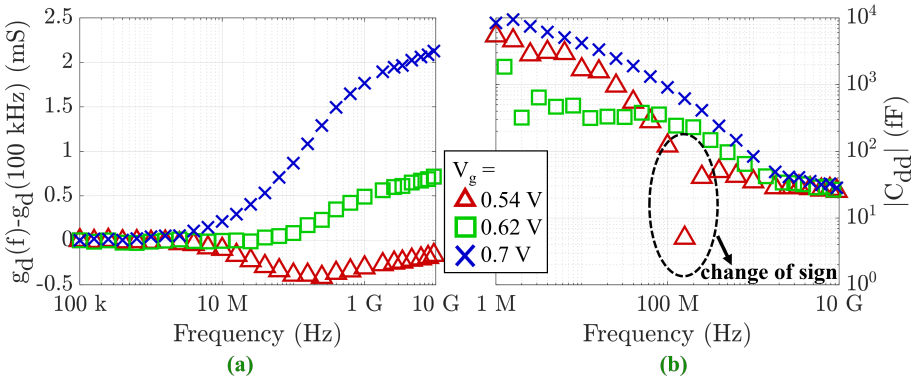


Figure 4.18: Variation of the output conductance $g_d(f)$ ($\mathrm{Re}(Y_{dd})$) with respect to its value at 100 kHz (a), and $C_{dd}(f)$ ($\mathrm{Im}(Y_{dd}/\omega)$, b) of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8$ V and $V_g = 0.54$, 0.62 and 0.7 V (symbols).

139]. The frequency transition in itself is due to a delay in the heat transport mechanism from device to heat sink, yielding a lattice temperature that is not able to follow instantaneous variations of an ac power at frequencies above the isothermal frequency (as explained above).

Extraction procedure for separate self-heating and substrate network characterization

Thanks to the previous observations made in **Figure 4.18** and in **Equation 4.11**, the proposed extraction procedure consists of using the ZTC bias point to first extract a model of the isothermal electrical behavior (Y_{ijT}, which is equal to the measured Y_{ij} at $V_{g,ZTC}$). Due to the importance of the substrate effect, an electrical network including the back-gate and substrate nodes is used to capture frequency-dependent $Y_{ddT}(f)$ and $Y_{dgT}(f)$ parameters.

After, the extracted electrical model is used to compute the Y_{ijT} parameters at other V_g biases (by updating some elements of the equivalent network, such as the gate capacitances, transconductance, etc.), and an n^{th}-order thermal network representing Z_{th} is used to fit the $Y_{dd}(f)$ data from **Equation 4.12**.

Note that the ZTC bias point is not specific to this technology **[140–144]** and has been experimentally verified down to cryogenic temperatures **[137, 145]**. So, the proposed methodology can be applied to a wide range of cases.

The steps involving electrical model fitting and thermal impedance extraction are explained in details in the following.

4.2.3 Extraction of substrate and back-gate nodes model at ZTC

The equivalent circuit including back-gate and substrate nodes used to model the measured FET electrical behavior is shown in **Figure 4.19a**. To better visualize the substrate and back-gate related parameters, **Figure 4.19b** shows a typical cross-section schematic of a UTBB FD-SOI nMOSFET (LVT back-gate type[15]), along with the main elements contributing to the $Y_{dd}(f)$ frequency response.

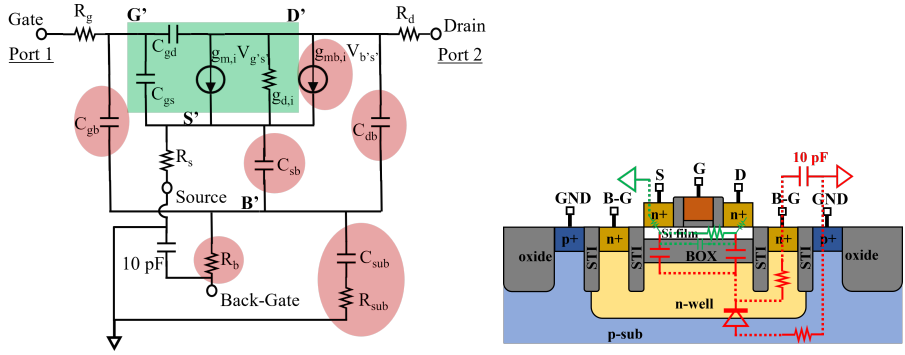


Figure 4.19: (a) FET small-signal equivalent circuit with substrate and back-gate networks. (b) schematic cross-section of FD-SOI UTBB nMOSFET.

Analytical equations for the circuit in **Figure 4.19a** (without R_g and R_d) have been derived and are presented in **Appendix D**. We can observe from **Figure 4.18** that the substrate effect induces a transition from $\sim 10\,\text{MHz}$ to $\sim 5-10\,\text{GHz}$[16]. This sets the frequency range used for parameter fitting of Y_{dd}, because the other Y_{ij} parameters are very noisy below a certain frequency: (i) Y_{dg} that is very noisy below $100\,\text{MHz}$[17], (ii) $\text{Im}(Y_{gg})$ and $\text{Im}(Y_{gd})$ are both very noisy below $\sim 1\,\text{GHz}$ (probably because these parameters are dominate by

[15] As mentioned in **Chapter 1**, there are mainly two varieties of UTBB devices according to the back-gate implant type: i.e. either low V_{th} (LVT) same as the channel, or regular V_{th} (RVT) opposite to the channel doping type.

[16] The curves seem to reach a plateau around 5-10 GHz then increase again. The high frequency increase is likely due to the gate resistance.

[17] This frequency limitation in Y_{dg} is related to the used measurement hardware, as measurements with another VNA and external bias tees from 10 kHz to 3 GHz exhibit much better-behaved measured Y_{dg}. Nevertheless, this VNA can hardly been used in this case, because of its high frequency limitation (3 GHz).

capacitances, which become very large impedances at low frequencies). The extraction procedure is the following.

1. Start by evaluating the extrinsic series resistances R_g, R_s and R_d with Bracales' method **[120]** (so, in cold FET $V_d = 0\,\mathrm{V}$ and in inversion).
2. At ZTC bias, find a first guess for the g_d, g_m, g_{mb}, C_{gd} and C_{gs} parameters:
   (a) Remove the contributions of all extrinsic series resistances (R_g, R_d and R_s) from the measured Y_{ij} to obtain Y^0_{ij} [18].
   (b) From the obtained Y^0_{ij}, extract a *first guess* of
      - g_d, g_m, g_{mb} from $\mathrm{Re}(Y^0_{dd})$, $\mathrm{Re}(Y^0_{dg})$, $\mathrm{Re}(Y^0_{dg})/10$[19], respectively, evaluated at low frequency (10 MHz),
      - C_{gd}, C_{gs} from $-\mathrm{Im}(Y^0_{gd})/\omega$ and $\mathrm{Im}(Y^0_{gg}+Y_{gd})/\omega$, respectively, evaluated at 1 GHz.
3. Still at ZTC bias, find a first guess for the C_{db}, C_{sb}, C_{gb}, R_b, C_{sub} and R_{sub} parameters:
   (a) Remove the contributions of the gate and drain extrinsic series resistances (R_g and R_d) from the measured Y_{ij} to obtain $Y^{0\prime}_{ij}$.
   (b) From the obtained $Y^{0\prime}_{ij}$, perform a fitting of $Y^{0\prime}_{dd}$ (from 10 MHz to 1 GHz) and $Y^{0\prime}_{dg}$ (from 100 MHz to 1 GHz) based on **Equation 4.4** and **Equation 4.2** of both real and imaginary parts, with C_{ds}, C_{db}, C_{sb}, C_{gb}, R_b, C_{sub} and R_{sub} as fitting parameters.
4. Again at ZTC, evaluate the final values of the 'intrinsic'[20] (g_d, g_m, g_{mb}, C_{gd}, C_{gs}, and C_{db}, C_{sb}, C_{gb}, R_b, C_{sub}, R_{sub}):
   (a) Remove the contributions of the gate and drain extrinsic series resistances (R_g and R_d) from the measured Y_{ij} to obtain Y'_{ij}.
   (b) From Y'_{ij}, perform a fitting of
      - $\mathrm{Im}(Y'_{gg})/\omega$, $\mathrm{Im}(Y'_{gd})/\omega$ from 1 GHz to 1 GHz,
      - Y'_{dd} from 10 MHz to 1 GHz,
      - Y'_{dg} from 100 MHz to 1 GHz.

This upper frequency limit of 1 GHz can be extended to higher frequencies if the isothermal g_d and C_{dd} curves have not reached a plateau at 1 GHz *and* as long as the de-embedding procedure guarantees reliable data.

To enable such straightforward and direct fitting strategy, some assumptions have been made. They are summarized hereunder.

- The extrinsic resistances are bias-independent.

[18] This can be easily performed using the Z-parameter representation.

[19] The choice $g_m/10$ as first guess of g_{mb} is justified in **Section 4.2.7**.

[20] In the sense that the extrinsic series resistances R_g and R_d are not present.

- The substrate and back-gate nodes are neglected to compute the series extrinsic resistances.
- C_{ds} is forced to 0 F.
- Although it will only be made later in the procedure, another important assumption is that *the back-gate- and substrate-related parameters* (in red in **Figure 4.19a**) *are gate bias-independent*.

The above assumptions are subject to critics[21], in particular the last one. The overall substrate and back-gate nodes extraction procedure could certainly be improved to yield more accurate and representative values, and some perspectives to that end will be given in **Section 4.2.7**. However, an *exact* substrate and back-gate modeling is out of the scope in this work. Indeed, what *matters* here is to *extract a circuit model that correctly fits the frequency-dependent Y-parameters*, such that *meaningful values of self-heating effect* can be extracted *at different biases*. It just so happens that the equivalent circuit from **Figure 4.19a** and the extraction procedure being described here enable an accurate and consistent characterization of self-heating effect, as it will demonstrated in the following.

Application to dut

The procedure described above is applied to the studied dut. **Figure 4.20** shows the extracted parameters, from which the contributions of the series R_g and R_d have been removed.

The first guess already gives fairly good trends, but with the second global optimization step, an excellent fitting is obtained for all parameters (except for a small offset in g_m that will be removed in the next step).

4.2.4 Extraction of electrical model at other biases

In order to extract thermal effects at other biases than ZTC, one still needs to update the electrical model to other biases. As dynamic self-heating effect induces a transition at similar frequencies than the back-gate and substrate nodes, we cannot update the parameters associated to those nodes and therefore *assume them to be constant with V_g bias*.

So, only the value of the g_m, C_{gs}, C_{gd} and g_d parameters are updated at a different V_g bias (the parameters in red in **Figure 4.19a** are assumed constant and the parameters in green are updated). In practice, we perform a fitting of the

[21] A sensitivity study of the extracted back-gate and substrate parameters to a incorrect evaluation in R_g is provided in **Appendix D**.

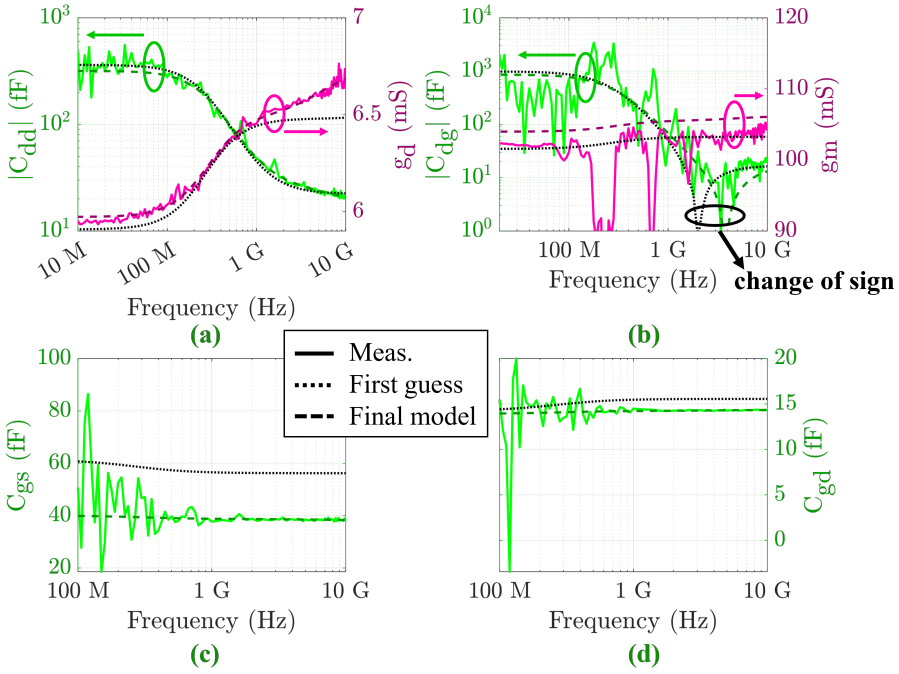


Figure 4.20: $|C_{dd}|$ and g_d (a), $|C_{dg}|$ and g_m (b), C_{gs} (c), C_{gd} (d). Measurements (light solid lines), first guess (black dotted lines), final model (dark dahsed lines) of the Y'_{ij} parameters (measured Y_{ij} from which R_g and R_d contributions have been subtracted), at ZTC bias.

above Y'_{ij} parameters evaluated at a different V_g, (i.e. measured Y_{ij} from which R_g and R_d have been subtracted) at high frequency, i.e. above the isothermal frequency. In this case, we use 1 GHz.

Figure 4.21 shows the measured extrinsic Y_{ij} parameters (which includes contributions from all extrinsic series resistances) and the fitted model at $V_g = V_{g,ZTC}$, after the last optimization step. **Table 4.1** summarizes the values of the electrical parameters obtained for this fitting. A good fitting is obtained for almost all parameters: indeed, C_{dg} is rather noisy below ~ 300 MHz and it is hard to validate its low-frequency behavior.

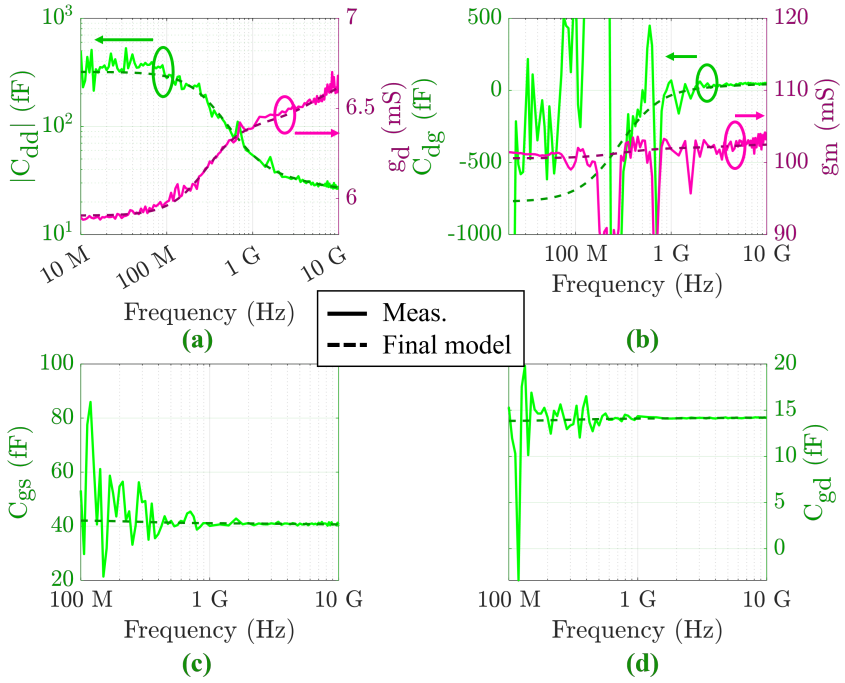


Figure 4.21: $|C_{dd}|$ and g_d (a), C_{dg} and g_m (b), C_{gs} (c), C_{gd} (d). Measurements (light solid lines), final electrical model (dark dahsed lines) of the extrinsic Y_{ij} parameters, at ZTC bias.

Table 4.1: Extracted values of electrical parameters of the equivalent circuit shown in **Figure 4.19a**, at ZTC bias, used in **Figure 4.21**.

	R_s	R_d	R_g	R_b	R_{sub}		
Ω	0.83	1.54	4.58	2700	830		
	C_{sub}	C_{gb}	C_{sb}	C_{db}	C_{gs}	C_{gd}	C_{ds}
fF	50.5	9.2	136	6.4	33.8	13.8	0
	g_{mb}	g_m	g_d				
mS	18	113.1	6.63				

4.2.5 Thermal impedance extraction

Once the *isothermal* electrical behavior has been characterized, the complex thermal impedance can then be extracted at different biases. Based on **Equation 4.12** and the known $Y_{ddT}(f)$ from the previous steps, measured $Y_{dd}(f)$ data is fitted using an n$^{\text{th}}$-order thermal network (as fitting parameters) to represent Z_{th}.

Both the imaginary and real parts of Y_{dd} are used for fitting, although only fitting $\mathrm{Im}(Y_{dd})$ gives very close results. In our case, selecting $n = 4$ (cf. **Figure 4.22**) appeared to be sufficient to correctly model the distributed transition. The resulting *thermal and electrical model* of $Y_{dd}(f)$ is shown for different bias points and compared to the measured Y-parameter in **Figure 4.23**.

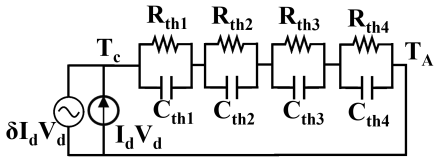


Figure 4.22: 4$^{\text{th}}$-order thermal network used to model the complex thermal impedance $Z_{th}(f)$.

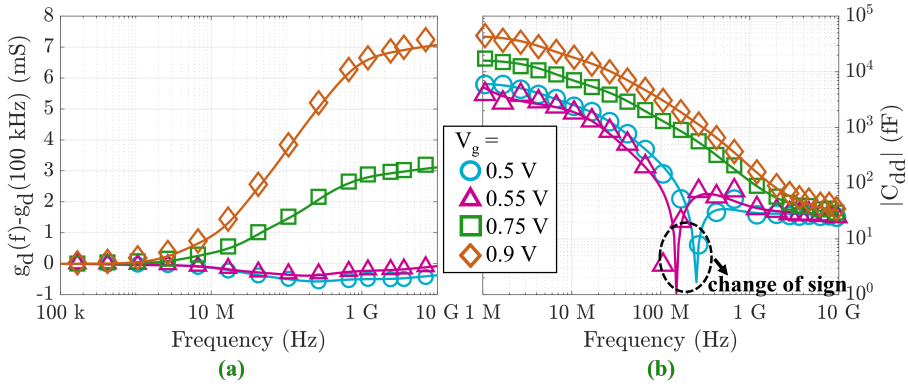


Figure 4.23: g_d (a) and $|C_{dd}|$ (b), measurements (symbols) and complete thermal and electrical model (lines), at different V_g biases, $V_d = 0.8\,\mathrm{V}$ and $V_{bg} = 0\,\mathrm{V}$.

We observe that a very good fitting is obtained across a very wide frequency

range from 100 kHz up to approximately 10 GHz for the different bias points. The sign of the step (either positive or negative) is correctly reproduced in agreement with **Equation 4.17** and **Equation 4.18**. To the best of our knowledge, the first time that $g_d(f)$ and $C_{dd}(f)$ curves for $V_g < V_{g,ZTC}$ with a negative step have been presented and the total R_{th} extracted from them was in **[128]**. Although the physical origin of this negative step is known and explained in **Section 4.2.2**, such curves had not been presented prior to **[128]**, since high biases -where SH has higher impact, and thus a positive step in $g_d(f)$- are commonly used in self-heating characterization. With technology scaling down and power reduction, the voltage range below ZTC becomes of interest. Even if SH is lower in that range, it nevertheless has to be taken into account (in particular its frequency response).

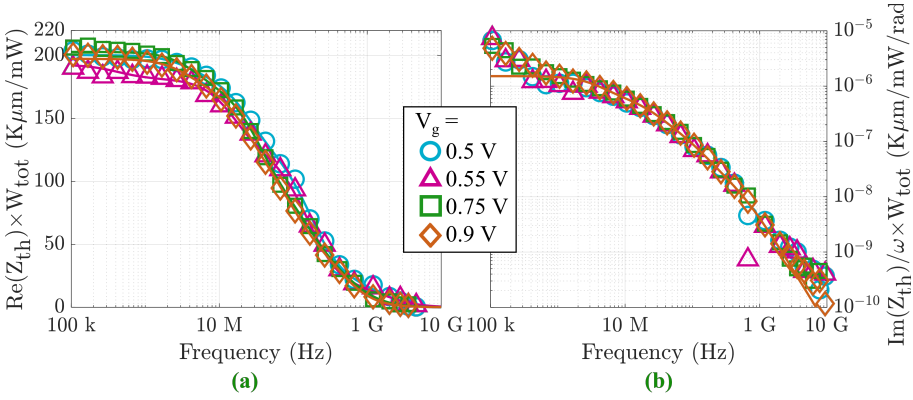


Figure 4.24: $\mathrm{Re}(Z_{th})$ (a) $\mathrm{Im}(Z_{th})$ (b) normalized to the total device width of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8\,\mathrm{V}, V_{bg} = 0\,\mathrm{V}$ and different V_g. Measurements in symbols and fitted model in solid lines.

Figure 4.24 shows the real and imaginary parts of the extracted Z_{th} for different biases. All curves overlap suggesting that the frequency-dependent $Z_{th}(f)$ is power-independent (or almost), as expected at room temperature, thus confirming the consistency of the method. Though a roughly constant R_{th} ($R_{th} = \mathrm{Re}(Z_{th}(f \to 0))$) with power is extracted in this work, it is not necessarily the case for other devices or in different conditions, such as at cryogenic temperatures **[115]**. We also observe that $\mathrm{Re}(Z_{th})$ becomes negligible only above 2.4 GHz ($< 1\,\%$ its maximum value), therefore yielding an isothermal frequency above 2.4 GHz. This confirms our previous statement that SH and

the SE cannot be easily distinguished in such devices as they appear in the same frequency range.

Indeed, extracting Z_{th} directly, without taking into account the back-gate and substrate nodes, i.e. by using constant g_{dT} and C_{ddT} versus frequency (as in [127, 134]) can lead to a strong misestimation of Z_{th}. Figure 4.25a shows the variation in $g_d(f)$ captured by the electrical and thermal model by either including the back-gate and substrate networks (solid lines) or neglecting them and fitting $\mathrm{Im}(Y_{dd})$ as in [127] (dashed lines).

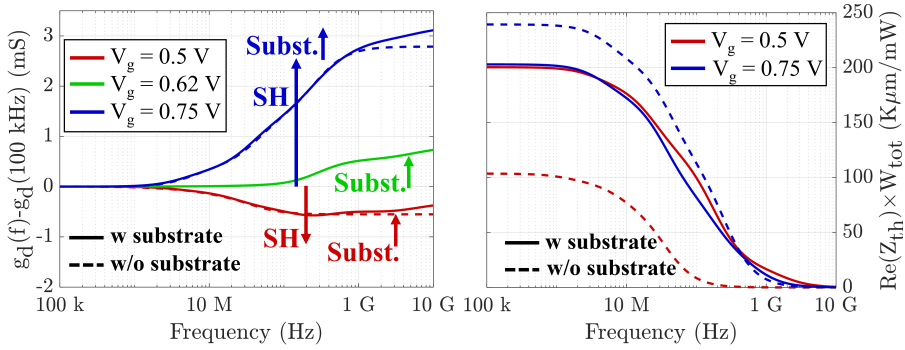


Figure 4.25: Left (a): Variation of $g_d(f)$ of a 20 nm FD SOI MOSFET biased at $V_d = 0.8\,\mathrm{V}, V_{bg} = 0\,\mathrm{V}$ and different V_g. Fitted model including back-gate and substrate nodes in solid lines. Fitted self-heating model including back-gate and substrate nodes (solid lines) and ignoring their modeling (dashed lines). Right (b): extracted self-heating model of $\mathrm{Re}(Z_{th})$ including back-gate and substrate nodes (solid lines) and ignoring their modeling (dashed lines).

The associated $Z_{th}(f)$ for each case is presented in Figure 4.25b. Ignoring the B-G associated transition leads to an overestimation (underestimation) of the total R_{th} ($R_{th} \equiv \sum_i R_{th,i}$, with $R_{th,i}$ defined in Figure 4.22) when $V_g > V_{g,ZTC}$ ($V_g < V_{g,ZTC}$), because its effect adds up with (cancels) the self-heating effect, respectively, as shown in Figure 4.26a, which plots the extracted total R_{th} for different V_g, with (blue data) and without (pink data) accounting for SE. The R_{th} is not extracted close to the ZTC bias point, because of the singularity (divide by zero) provided by the $\partial I_d/\partial T_A$ term tending to 0 as V_g tends to $V_{g,ZTC}$, thus introducing a larger error.

While for large $I_d(V_g)$ bias conditions (as in [113, 133]), the SH effect

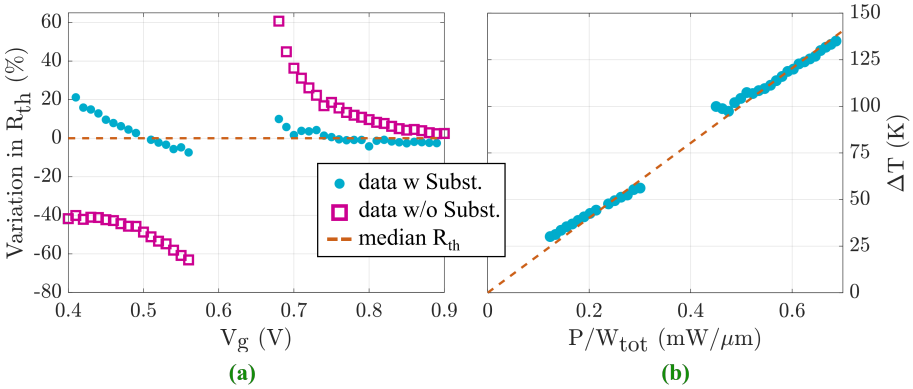


Figure 4.26: Left (a): variation of total $R_{th} = \sum_i R_{th,i}$ of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8\,\mathrm{V}, V_{bg} = 0\,\mathrm{V}$ and different V_g, in dots. Median value of normalized $R_{th,n} \equiv W_{tot} R_{th} = 202\,\mathrm{K\,\mu m/mW}$ in dashed lines. Variation of R_{th} extracted neglecting the back-gate and substrate nodes, in squares. Right (b): extracted temperature rise versus dissipated power normalized by the total transistor width (60 µm).

dominates the transition and neglecting the B-G/substrate nodes leads to a minor (5 %) error in the R_{th} evaluation, accounting for SE (and its independent modeling) is crucial for low-power applications (with potential error as large as 60 % in R_{th}).

In contrast, the novel method achieves an excellent accuracy at intermediate power and still performs well at low power, with resulting errors below 5 % and 20 %, respectively. The small remaining error at low V_g can be explained by a slightly bias-dependent Y_{ddT} not accounted for. The corresponding temperature rise ($\Delta T = R_{th} P$) versus power (P) is displayed at **Figure 4.26b**. The extracted R_{th} is roughly constant across the whole V_g range and gives a median value of $R_{th,n} = 202\,\mathrm{K\,\mu m/mW}$.

Since the divide by $\partial I_d / \partial T_A$ introduces a larger error around the ZTC bias point, we can apply the same procedure at a different V_{bg} and/or V_d (that yields a different $V_{g,ZTC}$) to fill the missing data points around $V_g = 0.62\,\mathrm{V}$. The self-heating effect (and equivalent back-gate and substrate network) has been extracted at a different $V_{bg} = 1\,\mathrm{V}$ using the same procedure. The resulting normalized thermal resistance $R_{th,n}$ and temperature rise (ΔT) are shown in **Figure 4.27**. An excellent agreement is obtained for both V_{bg} biases. The

better accuracy that seems to be obtained in R_{th} with the larger $V_{gb} = 1\,\mathrm{V}$ bias is actually related to power consumption, as similar accuracy is achieved with $V_{gb} = 0\,\mathrm{V}$ for the same power (cf. **Figure 4.27b**).

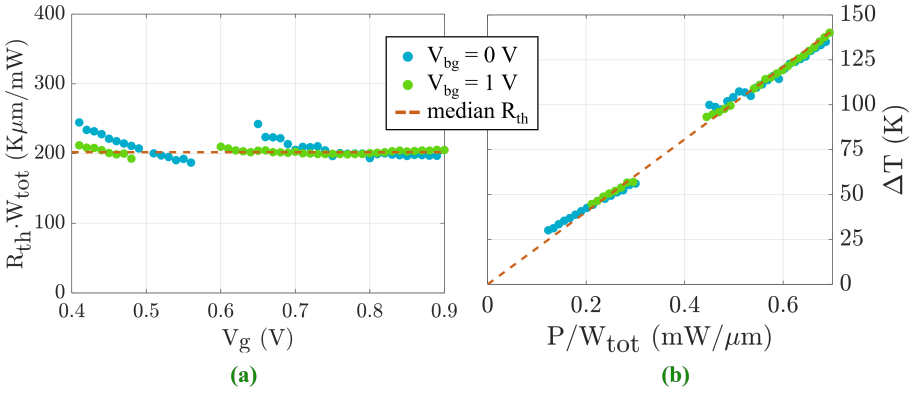


Figure 4.27: Total $R_{th,n} = W_{tot} \sum_i R_{th,i}$ (a) and temperature rise (ΔT, b) extraction for $V_{bg} = 0\,\mathrm{V}$ (performed above, blue dots) and $V_{bg} = 1\,\mathrm{V}$ (green dots), for different V_g, at $V_d = 0.8\,\mathrm{V}$.

The presentation of this original extraction procedure and its application to an actual UTBB nMOSFET demonstrates its great accuracy, but it also entails further questions concerning (i) the validity of the assumptions made, (ii) MOSFET modeling consequences of the strong correction with respect to the 'usual' RF extraction method, (iii) physical phenomena that are being modeled. These points are discussed in the following.

4.2.6 Impact on model accuracy

As we have seen above, the usual self-heating effect extraction procedure (neglecting substrate effect) can lead to potentially strong misestimations, *according to power level*, in R_{th}, thus in temperature rise and actual lattice (or channel) temperature of UTBB devices. Since many important parameters such as V_{th} and carrier mobility depend on the lattice temperature, its incorrect evaluation could affect the accuracy of the extracted MOSFET (compact) model. So, this new extraction method could enhance the MOSFET compact model accuracy.

However, from a practical point of view, i.e. assessing the accuracy improvement of a (compact) model using a thermal resistance extracted with the

new method, it really depends on the strategy adopted for the (compact) model.

Using a temperature-independent (and therefore power- or bias-independent) value of R_{th} in the model is the strategy used (to our knowledge) in compact models [146]. It is a correct approximation as long as the working temperature is around 300-400 K as shown in [115].

In this case, it is important to know at which bias the thermal resistance is extracted, because the method accuracy greatly depends on the power level. In most of self-heating-related papers, a condition of high power (large I_d and V_d) is usually taken. In this section, it is clearly stated that the usual method (ignoring the back-gate/substrate network) and the presently introduced method yield close results (less than 5 % variation) for a large I_d. Therefore, if such a condition is used to extract R_{th}, and R_{th} is assumed constant with bias, the electrical behavior of the device should be similar with and without taking into account the corrected value of R_{th}.

Nevertheless, we will still briefly verify the (PDK) MOSFET compact model available to us.

Comparison to PDK's compact model

Note that most of the observations made here were already made in [147].

In this comparison, pre-layout (without parasitic extraction) of a single FET instance (with the same dimensions as the dut) is simulated at different RF and dc bias conditions.

A first, significant discrepancy is already observed at ZTC bias in simulations. Although ZTC bias ($V_{g,ZTC,simu} = 0.59\,\mathrm{V}$ for $V_d = 0.8\,\mathrm{V}, V_{bg} = 0\,\mathrm{V}$) is very close to measurements (0.62 V), the large transition in $Y_{dd}(f)$ due to substrate effect is not present in simulations. Actually, the simulated frequency response of $Y_{dd}(f)$ strongly depends on the elements introduced at the back-gate terminal, cf. **Figure 4.28a**. Indeed, to fit the measurements shown in **Figure 4.28b**, it is necessary to add a series resistor of $\sim 10\,\mathrm{k\Omega}$ between the FET schematic instance's back-terminal and the external lumped capacitor of $\sim 10\,\mathrm{pF}$ (see inset of **Figure 4.28b**).

With this more accurate simulation condition (addition of external components to the back-gate terminal), the same full extraction procedure as explained above is used to characterize the self-heating effect. The extracted $\mathrm{Re}(Z_{th})$ and the same $g_d(f)$ trends are shown in **Figure 4.29**. The curves in $\mathrm{Re}(Z_{th})$ diverges for low biases ($V_g < V_{g,ZTC}$) probably because the assumption of bias-independent substrate-related parameters is not so valid as V_g approaches V_{th}.

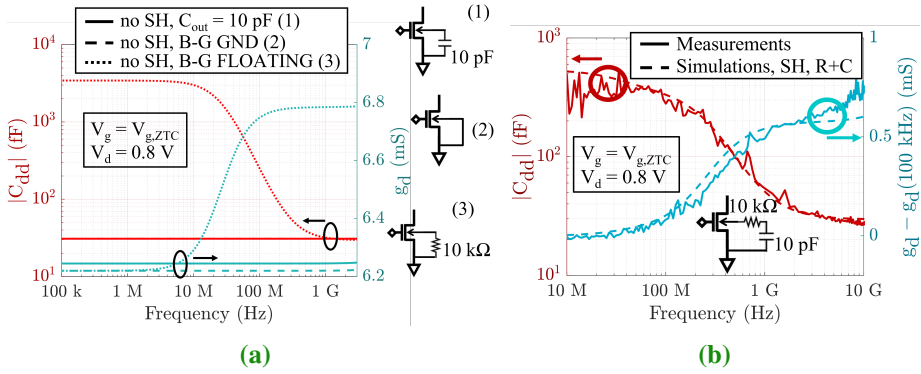


Figure 4.28: C_{dd} and g_d, PDK simulations and measurements, at ZTC bias. (a) simulations with various terminations at the back-gate terminal. (b) Simulations and measurements in agreement for a 10 kΩ resistor in series with a 10 pF capacitor connected at the back-gate terminal in simulations (inset).

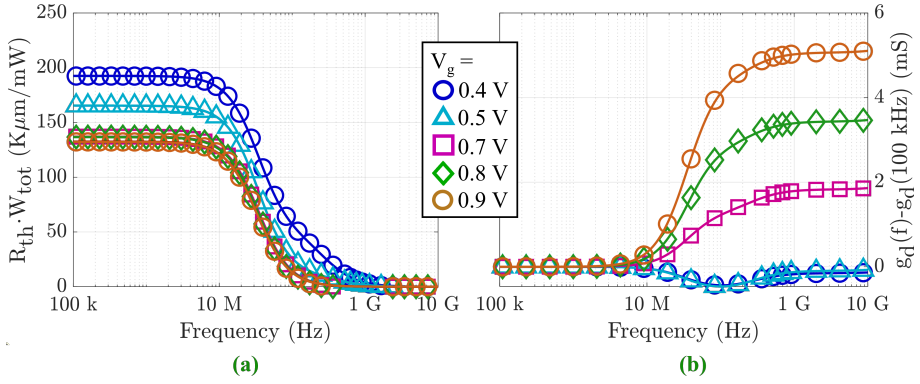


Figure 4.29: Variation of $g_d(f)$ (a) and $\mathrm{Re}(Z_{th})$ normalized to the total device width (b): compact model simulations (symbols) and complete thermal and electrical model (lines), at different V_g biases.

For larger gate biases ($V_g > V_{g,ZTC}$), we observe smaller steps ($g_{d,HF} - g_{d,LF}$) in simulated $\Delta g_d(f)$ (**Figure 4.29b**) than in measurements (**Figure 4.23**), which agrees with the lower extracted value of $R_{th,n}$ of 136 K µm/mW (instead of 202 K µm/mW from measurements). It means that even if there is an uncertainty on the term $\frac{\partial I_d}{\partial T_A}$ [22], the extracted $R_{th,n}$ is still lower in simulations than in measurements. So, it indicates that the PDK compact model underestimates the dut self-heating effect by $\sim 30\,\%$.

Another observation that can be made from **Figure 4.29** is that the self-heating-related transition takes place in a narrower frequency band: from ~ 10 MHz to ~ 1 GHz, instead of ~ 100 kHz to ~ 1 GHz in measurements. This is actually related to the order of the thermal network used in the model. The PDK compact model uses a first-order thermal network (as in **[146]**), which does not fit well measurements, as shown in **Figure 4.30**. This figure shows measured $\mathrm{Re}(Z_{th})(f)$, the thermal network fittings of different orders and the errors made in Z_{th} with each thermal network models of different orders. The residual fitting error (computed as the cumulative absolute difference in Z_{th} between measurements and fitted model from 100 kHz to 10 GHz) strongly decreases when using a higher-order thermal network (≥ 3) and tends to a constant value ($\sim 0.18\,\Omega$) that can be a residual error from the substrate effect, or another electrical phenomenon that is not well taken into account.

It is clear that a first-order thermal network fails to represent well the distributive nature of the heat dissipation process[23]. Indeed, the error made with a first-order thermal network is 7 times larger than with a 4$^{\text{th}}$-order network. As we will show in the next sub-section, each pair of ($R_{th,i}$,$C_{th,i}$) elements represent a distinct material or region in the heat dissipation path. So, the need of a higher-order thermal network for modeling the self-heating effect indicates that the heat generated in the device and evacuated to the outer world passes through several materials or regions of different properties or dimensions. This will be further discussed below.

[22] It is indeed a parameter that is sensitive to repeatable contact quality, as it is extracted from different contacts on the same pads at different temperatures.

[23] The description of the thermal impedance frequency behavior with a higher order (than one) thermal impedance has already been applied in several cases **[125, 148, 149]**.

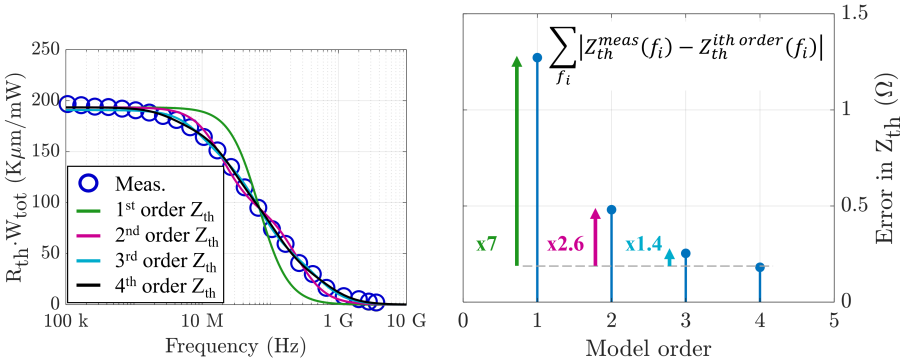


Figure 4.30: (a) Measured Re(Z_{th}) normalized to the total device width and several thermal network fittings of different order. (b) Error in Z_{th} (computed as shown in the inset) between measurements and fitted model from 100 kHz to 10 GHz.

We have identified three main discrepancies between the PDK compact model and measured FET behavior.

- Substrate effect below 1 GHz is not well modeled with the FET instance itself.
- Thermal resistance, temperature rise and self-heating effects are underestimated by $\sim 30\,\%$.
- Thermal network of first-order in the compact model is not enough to accurately model the distributive nature of the self-heating effect and associated heat dissipation. The error made is 7 times larger than with a fourth-order model.

Although the first and third points show that simulations might fail to accurately predict the electrical response of a MOSFET in the $\sim$ 100 kHz to 1 GHz frequency range, the second point has an impact much more important. Indeed, a wrong estimation of R_{th} directly affects the extracted lattice temperature on which depend some important temperature-dependent parameters such as the channel mobility and V_{th}. Therefore, this point is the one that might have the most important impact on the circuit designs that will be developed in **Chapter 5**.

4.2.7 Further considerations

Thermal evacuation path

The last figure (**Figure 4.30**) brings some interesting observation about the distributed nature of the heat dissipation network that we are going to discuss next. First, let us give a reminder of the analogy between a generic thermal problem and the derived thermal network[24].

The local heat transfer mathematical expression is

$$c_p \rho_{den} \frac{\partial T}{\partial t} = q_{vol} + \kappa_{th} \nabla^2 T, \tag{4.19}$$

where T is the temperature, κ_{th} the thermal conductivity, c_p the heat capacity at constant pressure, ρ_{den} the density, q_{vol} the volumetric heat source. In our case, the only heat source is the self-heating of the device. So, any position outside the device channel, the volumetric heat source is zero, and the above equation reduces to

$$\frac{\partial T}{\partial t} = \alpha_{th} \nabla^2 T, \tag{4.20}$$

where $\alpha_{th} = \frac{\kappa_{th}}{c_p \rho_{den}}$ is the thermal diffusivity.

The analogy between thermal problems and electrical networks comes from the resemblance of the above equation with the differential equation describing a transmission line. For a transmission line with non-zero per-unit-length C and R elements (G and L are zero), the differential equation reads

$$\frac{\partial^2 u}{\partial x^2} = RC \frac{\partial u}{\partial t}, \tag{4.21}$$

where u is the voltage along the line. The analogy between **Equation 4.21** and **Equation 4.20** becomes obvious, and the link between thermal problem-related quantities and equivalent circuit-based quantities are given in **Table 4.2**.

Finally, given this analogy, we can summarize that any piece of material can be thermally described by its equivalent *per-unit-length* $R_{th,dz}$ and $C_{th,dz}$ elements.

So, coming back to our practical case, the way we have used a thermal network of cascaded elements suggests the description of the heat evacuation path via several cascaded materials. However, some work indicated that a

[24] The derivation is kept short to accommodate to the topic, a nice explanation with more details can be found in **[150]**.

Table 4.2: Corresponding parameters in the analogy of heat transfer and circuit network.

Temperature	Voltage
Heat flux	Current density
Power transmitted	Current transmitted
Thermal resistance	Resistance
Thermal capacitance	Capacitance

significant portion of the generated heat is evacuated at the top of the wafer through the BEOL [112, 151, 152], either via the Source and Drain terminals or via the Gate. Such findings suggest another representation of the thermal network with some cells in parallel.

Anyway, the faithfulness of a given equivalent thermal network would often be questionable. So, a more complete approach would be to perform 3D transient simulations of the heat transfer problem including the FET, its surroundings (BEOL layers) and the Si substrate. Such an approach was studied in [150] but limited to static condition. Extending this technique to transient simulations could (i) more accurately describe the complete heat evacuation path, (ii) pinpoint the main bottlenecks preventing heat flow, thus increasing the channel temperature, and (iii) help in the identification of a physically-aware thermal network used for self-heating effect modeling.

At last, to finalize the analogy between our case and the general thermal problem described above, it is important to realize that the above thermal problem is formulated at any given point in space (and time), while our case study deals with an overall heat transfer problem with well-set boundary conditions at the macroscopic level. So, for a direct comparison to our case study, it is necessary to integrate the heat transfer equation across the area within which circulates the heat flux. For the following, let us assume all the heat evacuates through the substrate, taking the total intrinsic MOSFET area as an equivalent cross-section A_{eq} ($A_{eq} = 20\,\text{nm} \times 60\,\mu\text{m}$).

From the fitting of measured $Z_{th}(f)$ with different orders of thermal network in **Figure 4.30a**, we identify different cells ($R_{th,i}, C_{th,i}$) contributions with associated cutoff frequencies ($f_{th,i} \equiv 1/(2\pi C_{th,i} R_{th,i})$) ranging from a few MHz to $\sim 1\,\text{GHz}$, and the main contribution is centered at 67 MHz. This is better illustrated in **Figure 4.31**.

In case of a single order thermal network, the analogy made above between

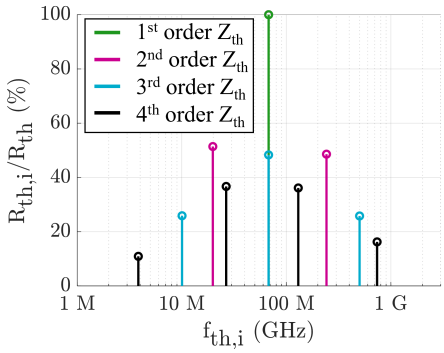


Figure 4.31: Extracted contribution of each thermal network cell $R_{th,i}$ to the total R_{th} for different orders of thermal network fitting used in **Figure 4.30**.

Equation 4.20 and **Equation 4.21** links the *material thermal parameters* to f_{th} as

$$f_{th} = \frac{\kappa_{th}}{2\pi A_{eq} \rho_{den} c_p}. \tag{4.22}$$

Computing this equivalent f_{th} for silicon thermal parameters ($\rho_{den} = 2.33\,\mathrm{g/m^3}$, $\kappa_{th} = 1.3\,\mathrm{W/cmK}, c_p = 0.7\,\mathrm{J/gK}$ **[153]**) gives $f_{th} = 10\,\mathrm{MHz}$, which lies inside the frequency range shown in **Figure 4.31**.

A more detailed analysis is out of scope of this work. However, this simple connection between the extracted Z_{th} network and the material thermal parameters of silicon suggests that this approach (extract Z_{th} from FET measurements and fit to an equivalent model) might be used to extract material thermal parameters, if not precisely (because of a number of simplifications made), it could at least give an order of magnitude. Using a more faithful 3D model, as suggested above, might increase the method accuracy. Characterization of material thermal properties is of particular importance in advanced nodes, because thermal properties of these materials change significantly with (i) fabrication process, (ii) temperature, (iii) doping and (iv) thickness **[154–160]**. While some work have reported values of thermal conductivity in some extreme cases as encountered in UTBB devices (ultra-thin Si and silicon dioxide layers) **[154, 156, 159]**, no work, to our knowledge, reported values of material heat capacity at constant pressure (c_p) in these cases.

Validity of extracted back-gate and substrate parameters value

Finally, let us discuss about the pertinence of the extracted back-gate and substrate parameters value from **Table 4.1**.

The procedure described in this section enables an accurate extraction of self-heating effect, but it relies on some assumptions, especially on the assumption that the substrate- and back-gate-related parameters are gate bias-independent. While it might be accurate in strong inversion, as the conductive channel screens the back-gate terminal and substrate from the front-gate, it is likely less valid for V_g approaching V_{th}. Violation of this assumption likely explains the extracted R_{th} value that deviates at low-power from the median value (cf. **Figure 4.26**, **Figure 4.27** and **Figure 4.29**).

In order to assess this statement, tcad simulations of a UTBB FD-SOI MOSFET [25] have been performed. The results will not be shown in details, because the stack definition is not entirely appropriate to the studied device. Nevertheless, the simulations have identified some general trends in the values of extracted substrate and back-gate parameters that have also been confirmed with preliminary 4-port measurements of FETs in the same technology [26]. These trends are listed in the following.

- Strong variations in C_{gb} and g_{mb} with V_g at low biases (close to V_{th}) are observed in simulations. C_{gb} becomes practically bias-independent above some V_g value, while g_{mb} keeps changing a little. It validates the assumption of gate bias-independence of back-gate and substrate parameters for large V_g values, but it invalidates it at low V_g.
- A ratio of ~ 10 is obtained between g_m and g_{mb} via simulations, which is not too far from the extracted one (~ 6). This ratio is linked to the body factor, more information can be found in **[5]**. This observed ratio of ~ 10

[25] The FET stack definition comes from **[161]** that was used as preliminary work to extract back-gate- and substrate-related parameters. Although the stack definition comes from a 28 nm FD-SOI technology **[162]**, uses a gate length of 25 nm and, therefore, does not correspond exactly to the studied device, the geometry and architecture are similar enough to extract some trends.

[26] Otherwise, we could also have assessed the validity of V_g independence via 2-port measurements. Since SHE is also present at low $V_g < V_{g,ZTC}$ biases, one would first need to remove the contribution of self-heating from the measured Y-parameters. If $Z_{th}(f)$ is known, it could be easily achieved by reversing **Equation 4.11**. It has been applied to the measurements of the same dut in **[163]**, by assuming the extracted $Z_{th}(f)$ (at a given bias) is gate bias-independent. Although we were able to extract some interesting trends in the back-gate and substrate parameters, the accuracy of the extracted parameters suffers from the same discrepancies identified in this section.

actually justifies the first guess estimation of g_{mb} from g_m described in **Section 4.2.3**.

- Simulations show a ratio of roughly 1 between C_{db} and C_{sb}, with values in the range of 5-20 fF. Measurements extraction exhibit a ratio larger than 20, with $C_{sb} > 100$ fF.

These inconsistencies (mostly observed for C_{sb}) questions the pertinence of the choice made to model the substrate and back-gate nodes. Indeed, a more accurate model could have been used, such as the one in **[164]**, where distributed elements are used to represent the back-gate and substrate accesses. However, extracting substrate and back-gate parameters from 2-port measurements has limited accuracy and is sensitive to the first guess used in the optimization, due to the limited amount of fitting curves (Y_{dd} and Y_{dg}) and large amount of fitting parameters. A certainly more pertinent way to accurately characterize substrate and back-gate parameters is via FET measurements in a 4-port configuration. In that case, much more data affected by back-gate and substrate parameters are available, and a more physically-aware characterization could be achieved.

4.3 Conclusion

Proper wideband modeling of transistor is crucial for millimeter-wave IC design. On the one hand, dynamic self-heating effect (and substrate effect in FD-SOI technology) appears over a wide, low frequency range, and affects crucial intrinsic parameters such as carrier mobility, threshold voltage, reliability, etc. On the other hand, accurate FET electrical behavior is also needed at high frequencies, i.e. at the circuits' operating frequencies. To address these challenges, this chapter was separated in two main parts, the first dealing with very high-frequency aspects, the other with lower frequency ones.

High frequency characterization

Several procedures have been studied in the first part to correct measurements from on-wafer parasitics and successfully achieve meaningful corrected measurements of the tested MOSFET up to 110 GHz.

First, we have characterized a specially designed in-situ calibration kit with different RF probes. The extracted transmission line parameters (γ and Z_c) feature some undesired probe-dependent bumps (that are identified as coming from strong probe coupling to adjacent environment), which deteriorate the FET measurement accuracy even after in-situ calibration correction.

By using the series extrinsic resistances of a MOSFET as measurement

accuracy test, we have confirmed for our test structures that in-situ calibration (followed by classic Open-Short de-embedding) yields the most accurate results, in agreement with previous work [29, 30]. Furthermore, we have also tested Amakawa's method [24], which extracts a causal Z_c for the Lines standards. *For the first time*, to the best of our knowledge, it is shown that *Amakawa's method applied to in-situ calibration provides an interesting correction reducing probe-dependent errors* (of various probe technologies) *in MOSFET measurements*. Indeed, measured source and drain resistances varying by less than 5 % up to 110 GHz is obtained for all tested probes. Moreover, the bumps in R_g are dampened with this method, and its roll-off at higher frequencies is reduced, achieving variations up to $\sim 20\,\%$ in the worst case.

This 2-tier calibration (with Open-Short de-embedding) using Amakawa's Z_c extraction has been applied to correct the measurements of extrinsic FET parameters from different probes data, which are compared to the PDK's compact model. Even though each probe data still suffer from probe-dependent residual errors that are more visible beyond 70 GHz, we have achieved high-accuracy measurements of the tested transistor geometry up to 110 GHz, which is demonstrated by: (i) almost overlapping curves below 70 GHz for each parameter (with a wider spread in f_{max} though) that (ii) consistently follow the PDK's compact model up to 110 GHz with marginal deviation. The proposed methodology yields promising results for high-frequency transistor characterization, even though more work is needed to verify the achieved accuracy for FETs of different geometries and dimensions.

Despite this excellent overall agreement obtained between measurements and simulations, a few small discrepancies were observed, mainly in the low-frequency Y_{22} and Y_{21} behaviors, which entailed further investigation in self-heating and substrate effects.

Low frequency effects

In such advanced CMOS technology, the RF method is usually more suited for self-heating effect characterization. In this method, the dynamic SHE-induced transition in measured $Y_{dd}(f)$ is used to extract self-heating parameters. However, this transition also includes non-thermal effects, such as drain-to-source coupling through the back-gate (substrate effect) in FD-SOI devices, which might lead to strong extraction error in self-heating effects if not taken into account.

Therefore, we presented for the first time to the best of our knowledge a way to properly characterize both effects separately using the so-called zero-

temperature-coefficient bias. At this bias, dynamic self-heating effect disappears, and an equivalent circuit with substrate and back-gate nodes is used to fit measurements (yielding *isothermal* parameters). The isothermal parameters are then estimated at other biases (based on some assumptions) and used to accurately extract self-heating parameters.

This procedure was applied to measurements of a UTBB FD-SOI MOSFET from the 22FDX® technology, and a very consistent thermal resistance was extracted at various power levels. We also demonstrated that the conventional RF method (that neglects the back-gate and substrate effects) can lead to a potentially strong misestimation of R_{th} according to the power level used.

Furthermore, we have shown that a first-order thermal network model yields an error in fitted Z_{th} 7 times larger than when a fourth-order network is used. By analyzing the extracted thermal network in terms of the heat transfer problem, we have linked each pair of $(R_{th,i}, C_{th,i})$ elements to a distinct material or region in the heat dissipation path, and we have further shown the relative impact of each material on the overall thermal resistance. Then, we have linked some fitted thermal parameters to the material thermal properties of silicon. Although further developments are still needed, extracting a complex $Z_{th}(f)$ model from FET measurements might open the way to the characterization of the heat capacity (at constant pressure) property from different materials in the heat evacuation path.

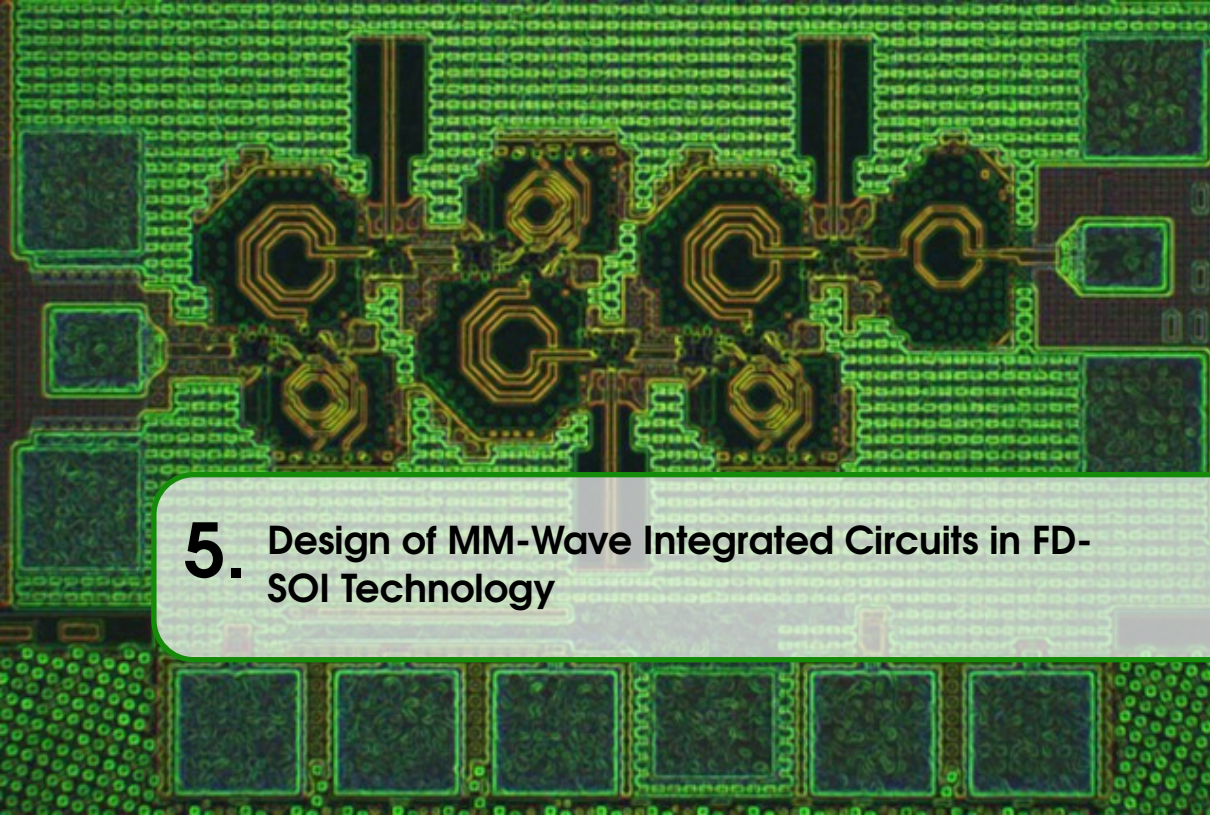
Subsequently, we have criticized the extracted values of substrate and back-gate parameters with the help of some tcad simulations and additional 4-port FET measurements. Some parameters exhibit values or trends that are indeed not meaningful. For a better modeling of back-gate and substrate accesses, FET measurements with additional ports is a must to provide sufficient information for curve fitting.

Finally, the MOSFET's PDK compact model has been verified by applying the same extraction procedure, and some discrepancies have been identified. First, it is found that the FET low-frequency behavior due to substrate effect is not well modeled in the PDK FET instance. A better agreement can be obtained with the addition of a 10 kΩ series resistor at the back-gate terminal. Although it is not shown here, the impact of a good substrate effect modeling (as the one presented in this part) at higher frequencies (up to 110 GHz) has been analyzed and found to be small. A more detailed analysis is provided in **Appendix E**, in which the MOSFET measurements from **Section 4.1** are used to extract the small-signal equivalent circuit of **Figure 4.19a**, including back-gate and

substrate nodes, and they are compared to the PDK simulations corrected with a 10 kΩ series resistor.

So, the substrate does have a small but non-negligible impact on the MOSFET behavior. For circuit design, its effect can be included in simulations to first-order with a 10 kΩ series resistor at the back-gate terminal for a better agreement with the measured FET behavior at mm-wave frequencies.

Instead, the main discrepancy identified between measurements and the PDK model simulations concerns the $\sim 30\,\%$ lower value of R_{th}, which *might lead to self-heating effect underestimation in circuit design*. Since the thermal resistance is roughly inversely proportional to the FET width, for a constant dissipated power, a larger FET (as is the case for power amplifiers) will suffer from a lower increase in lattice temperature. So, the actual impact at circuit-level might be less important than one could think. Nevertheless, a circuit-level quantitative analysis of such a misestimation on R_{th} will still be covered in **Chapter 5**.



5. Design of MM-Wave Integrated Circuits in FD-SOI Technology

Cellular communication has tremendously progressed in the last decades having a deep impact on today's connected society. Each successive cellular generation has brought dramatic increase in data rates. The deployment of 5G, supporting the Internet-of-Things (IoT) is further expected to bring a new transformation toward a society of connected people and connected objects. 5G's promises of very high data rates (> 1 Gbps), low latency, increased spatial coverage, massive machine-type communications will be met through several techniques, including multi-user multiple input, multiple output (MIMO) antennas with beamforming, use of millimeter-wave (mm-wave) spectrum, small cells, low Earth orbit satellites, etc.

For instance, the use of FR2 bands in the mm-wave spectrum enables high data rate capability for short range 5G communications. Indeed, with extra available bandwidth at these high operating frequencies and with complex modulation schemes such as 64- to 256-QAM orthogonal frequency division multiplexing (OFDM) signals, 5G targets of data rate communications in the Gbps range can be achieved. However, such targets require high linearity in front-end module elements (especially at the power amplifier side) and low noise receivers at mm-wave frequencies.

SOI technology offering high performance at low cost is a serious contender for these high frequency mass market applications. The suitability of RF-SOI (with partially-depleted Silicon-on-Insulator transistors) for RF applications

does not need to be demonstrated anymore. Its strong commercial success speaks for itself, mainly in RF switch banks equipping virtually a 100 % of modern-day smartphones [3]. Furthermore, many outstanding circuit demonstrators at mm-wave frequencies exhibiting best-in-class performance among CMOS technologies have recently been developed in RF-SOI technology and will be used as benchmark in this thesis.

On the other hand, fully-depleted SOI (FD-SOI) technology offers comparable device RF performance, with higher integration density for increased digital functionalities, at lower power. Furthermore, the presence of the back-gate terminal adds a tuning knob to the circuit for increased configurability. Therefore, FD-SOI is seen as a driving technology for low power RF applications or smart mm-wave front-end modules (FoMs) using advanced signal-processing [165].

This chapter presents the design of two mm-wave integrated circuits in 22 nm FD-SOI technology: a low-noise amplifier (LNA) and two power amplifiers (PAs), i.e. two critical elements in front-end modules, thus essential for telecommunications in the mm-wave spectrum. First, a brief introduction of a typical front-end module architecture is presented, and key LNA and PA figures of merit are described[1]. Then, the designed circuits are presented, characterized and their performance benchmarked with the state of the art.

5.1 MM-Wave Front-End Module

Beamforming is a key technique to enable 5G application in the mm-wave FR2 bands by increasing the radiated power. It consists of multiple front-end module (FEM) cells assembled together to create an antenna array. A typical design strategy foreseen for mm-wave FEM cells is shown in **Figure 5.1**. Each antenna is connected to an LNA and a PA via a switch. Then, comes a phase shifter and variable variable gain amplifier (VGA) to enable beamforming [4].

In this integration scheme, the switch enables the receiver (RX) and transmitter (TX) to share a common antenna. In the RX chain, the first element is the LNA, which amplifies the signal, without degrading too much the signal-to-noise ratio (SNR). In the TX chain, the last element is the PA, which amplifies the signal and delivers sufficient power to be radiated by the antenna. These three aforementioned elements (switch, LNA, PA) are the most important and critical ones in a front-end module, though only the LNA and PA will be

[1] Complementary design information for LNA and PA circuits can be found in **Appendix F**. It provides a general design overview linking circuit key figures of merit to device-level metrics.

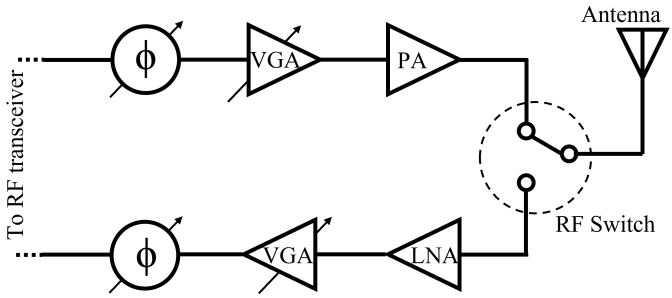


Figure 5.1: Unit cell of RF front-end module for 5G mm-wave frequency bands.

discussed in the following.

5.1.1 LNA figures of merit

The two main figures of merit in an LNA are its noise figure and gain. As the first (amplifying) element after the switch in a front-end module, its noise figure (*NF*) being the ratio of output and input SNR, directly contributes to the total receiver *NF*, which has to be minimized. In addition, the signal received at the input must be sufficiently amplified in order to avoid that subsequent circuitry (mixers) adds significant noise to the signal and further degrades the receiver SNR. This is a direct outcome from Frii's formula of cascaded devices total noise [35].

It should be noted that design targets of $\sim 3\,\text{dB}$ in *NF* and $> 20\,\text{dB}$ in gain are common values for 5G 28 and 39 GHz user equipment applications [166–168]. An exact value would require a full link budget analysis of the exactly targeted application, which is out of scope of this thesis, but the above values are representative of targeted mm-wave on-wafer designs.

5.1.2 PA figures of merit and challenges

The last element in the transmission (TX) chain (before the switch) is the PA. This circuit block faces tremendous design challenges due to the stringent requirement of being able to deliver large amount of power at a high efficiency and with high linearity. Indeed, the transceiver's overall power consumption is usually dominated by the PA, which therefore has a major impact on battery-life in portable applications (such as mobile handsets).

The high-order digital modulations envisaged for 5G have a large peak-to-average power ratio (PAPR), of the order of 8-9 dB. This can be visually understood as a wide probability distribution function (PDF) such as illustrated in **Figure 5.2c**, therefore requiring a high degree of linearity for a low bit error rate (BER) and error vector magnitude (EVM) **[169, 170]**. Due to the large signal bandwidth, digital predistortion (DPD) is power hungry and is not a solution of immediate interest, i.e. the requirements for 5G systems should be met without the use of digital predistortion **[4]**. With more investigation in this topic, DPD could be envisaged in the future to improve 5G systems.

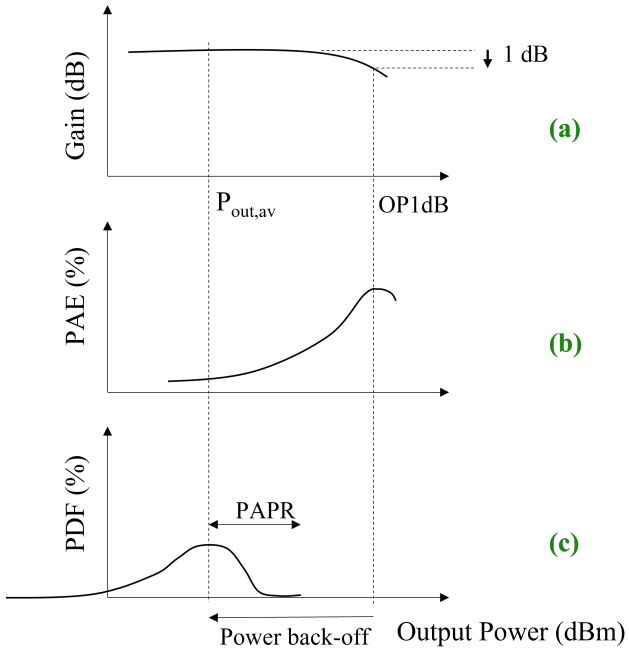


Figure 5.2: Sketch of typical gain vs P_{out} (a), PAE vs P_{out} (b) curves and probability distribution function of high-order modulation (c).

To achieve such high linearity, the average signal power is therefore backed-off (from the 1 dB compression point), since the PA is always more linear the further away its regime is from compression: the average power of the PDF in **Figure 5.2c** is shifted to lower values such that the PDF lies across a linear region in the gain vs P_{out} curve (shown in **Figure 5.2a**). The main

drawback of working in power back-off is the loss in average efficiency of the PA, which is maximum at compression and decreases at lower power as shown in **Figure 5.2b**. For the complex modulations with 64-QAM OFDM[2] considered for uplink 5G handset applications **[4, 171, 172]**. The targets in rms EVM and adjacent channel leakage ratio (ACLR) to guarantee low bit error rate and manageable channel leakage are -25.2 dB and -30 to -25 dB, respectively. Moreover, according to the number of antennas used for beamforming (as well as interconnects loss, antenna gain, etc.), the average power to be delivered by each PA is expected to be around 11 to 15 dBm **[4]**. Whereas the target PA efficiency for 5G applications is around 20 %, which is critical for mobile applications as the PA is typically responsible for most of the power consumption of wireless transceivers.

Despite the obvious advantages of Si-based technologies for high integration and the high performance demonstrated below in LNA, the PA still remains the bottleneck for these technologies due to their intrinsic device limitations to being able to deliver large amount of power at high efficiency. Detailed explanations are given in **Appendix F**, revealing why GaN technologies are more suited to these circuits.

[2] Using OFDM instead of single carrier also intensifies the need for high linearity, which is translated in an additional 1.5 to 2 dB of power back-off.

5.2 A 39 GHz LNA in 22 nm FD-SOI technology with 2.5 dB NF

This section presents a 39 GHz LNA designed in GlobalFoundries 22FDX® technology, alredy pbulished in [173]. After describing its design, its performance is analyzed with a particular focus on the circuit behavior with back-gate bias tuning. Finally, its performance is compared to the state of the art in CMOS technology.

5.2.1 Design

A low-noise amplifier is designed in the 22 nm FD-SOI technology at 39 GHz, covering the N259 and N260 5G bands. A cascode common-source with inductance degeneration topology is chosen. A simplified schematic is shown in **Figure 5.3** and a picture of the fabricated prototype in **Figure 5.4a**.

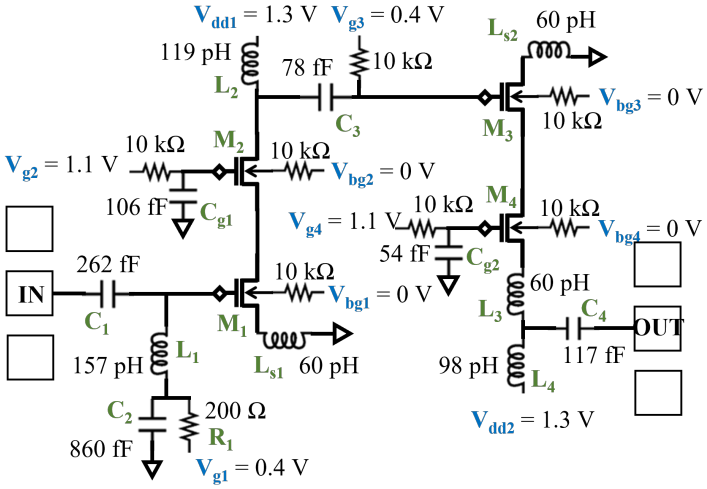


Figure 5.3: LNA schematic, with nominal bias and components values.

The LNA is designed in GlobalFoundries' 22FDX® technology, with a mm-wave back-end of line (BEOL). This BEOL (**Figure 5.4b**) includes 4 layers with thicknesses larger than 1 µm (JA to LB). This technology provides several types of transistors, including the super-low threshold voltage (SLVT) nMOSFET with high f_t, high f_{max} and low NF_{min} performances, and is chosen in this design using the nominal gate length of 20 nm. A relaxed contact-poly-pitch (CPP) of 208 nm (2xCPP) enables to boost the f_t and f_{max} performance

[174] at the cost of a slightly larger active layout area, which remains negligible at circuit-level, whose total area is dominated by that of the passives. The gate bias of M1 and M3 ($V_{g1,3}$) of 0.4 V yields lowest NF_{min} with sufficiently large f_t and f_{max} (see later in **Figure 5.9a**). The voltage bias M2 and M4 ($V_{g2,4}$) is determined to have equal voltage drop on each device. The FET's total width is selected based on trade-offs among input matching, noise matching and power dissipation. All FETs have the same dimensions. Linearity performances including third-order input referred intercept point (IIP3) and 1 dB compression point are g_d limited. Therefore, the V_{dd} bias of 1.3 V ($V_{ds} = 0.65$ V) is selected as a reasonable trade-off between linearity and dissipated power [175].

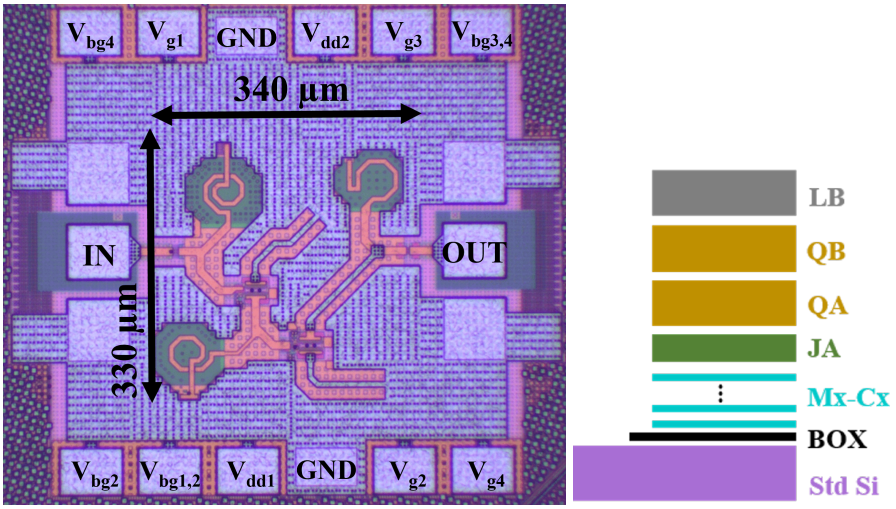


Figure 5.4: (a) Picture of the 39 GHz LNA prototype. Core size of $0.34 \times 0.33\,\text{mm}^2$ and $0.6 \times 0.62\,\text{mm}^2$ including all pads. (b) Millimeter-wave BEOL in 22FDX®.

In LNA design, the gate resistance (R_g) of the common-source FET is one of the major contributions of noise. It can be reduced with special layout techniques. Finger widths spanning from 300 to 500 nm feature the lowest NF_{min} in this technology. In most advanced processes, the lowest metal layer (M1) is used to connect in parallel the poly-Si gates of multiple fingers. Due to the small width and thickness of the M1 interconnect, it adds a significant contribution to the total R_g when a large number of fingers is used. For this reason, a multi-

number of vertical fingers (or rows) is available in this technology, it reduces R_g by decreasing the length of the narrow M1 gate wire that connects fewer fingers horizontally as shown in **Figure 5.5**. The final FET is laid out as a combination of 6 cells of 2 vertical rows 10 horizontal gate fingers of 500 nm width (for a total width of 60 µm). The gates of each instance are connected together via the thick JA metal layer for negligible additional gate resistance. The overall FET footprint size is 30 µm, which is $< \lambda/50$ at 40 GHz. The NF_{min}, f_t and f_{max} at 39 GHz for different back-gate voltages (V_{bg}) of M1 including parasitics up to the JA level are shown in **Figure 5.9a**. For the nominal bias point given above (corresponding to the current density normalization $J_d = 1$, in **Figure 5.9a**), $NF_{min} = 0.86$ dB, $f_t = 141$ GHz, $f_{max} = 299$ GHz. The dc back-gate contact is connected through a large bias resistor (10 kΩ) to decouple RF and dc signals in a compact way.

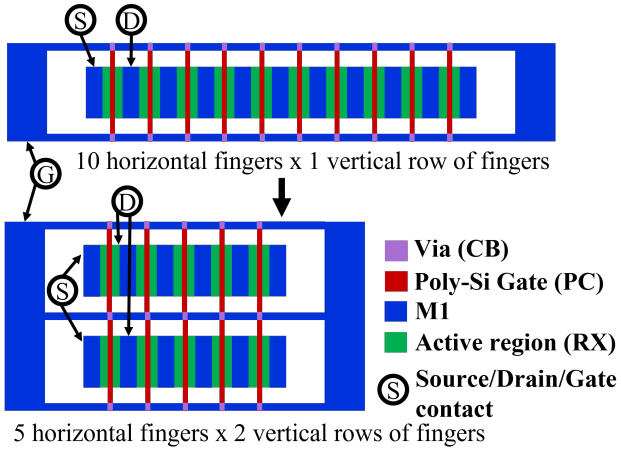


Figure 5.5: Sketch of horizontal and vertical gate fingers concept.

The degeneration-inductor (L_{s1}) is used to increase the real part of the input impedance as well as to provide in-band stabilization, at the cost of a small gain reduction. The input matching is realized with a shunt inductor (L_1) and input series capacitor (C_1) that also decouples the RF and dc paths. Such a configuration enables the implementation of electrostatic discharge (ESD) protections at the input with large diodes acting as large decoupling capacitors (though these were not implemented in this design). A second stage is added to provide further gain. The interstage matching is designed with a

shunt inductance (L_2) and series capacitance (C_3). The output matching consists of a series inductance (L_3), a shunt inductance (L_4) and series capacitance (C_4) for a broader bandwidth. L_1, L_2 and L_4 are designed as spiral inductors in QB. The others are realized with short pieces of inductive thin-film microstrip lines with the ground plane in JA and signal in LB. All series capacitors are designed as metal-on-metal lumped capacitors with high density ($3.3\,\mathrm{fF}/\mu\mathrm{m}^2$) using the top 3 thin metal layers (C3-C5) to reduce parasitic shunt capacitance. An RC network is present at the input matching to provide low frequency stabilization, despite its detrimental effect on total NF (around 0.24 dB, see **Section 5.2.5**).

$V_{g1,3}$ and $V_{dd1,2}$ biasings are fed from dc pads to the circuit using $10 \times 10\,\mu\mathrm{m}^2$ cells with 360 fF decoupling capacitors to ensure a low in-band impedance signal feed up to the circuit. Low-frequency grounds are enforced at the dc pads off-chip using 120 pF and 0.1 µF decoupling capacitors on the dc probes themselves. JA ground is used beneath all high-level interconnects and under L_{s1}, L_{s2} and L_3, in order to minimize the ground inductance throughout the whole circuit, thereby avoiding related stability issues that can be critical in single-ended circuits. The parasitics of the FET interconnects and close routing are extracted as a whole block via a combination of local parasitic extraction (PEX) cells (using Calibre xACT) and EM simulations (Keysight Momentum). A full EM simulation is performed including inductors, large-scale interconnects, pads and ground planes. The full EM simulation and other blocks are connected together in order to account for ground impedance, coupling between inductors, pads parasitics, etc. and to ensure a sound simulation concerning circuit stability.

5.2.2 Measurements at nominal bias

The LNA is measured on-wafer with GSG probes. S-parameters and linearity measurements are performed with a Keysight VNA (PNA-X). Noise measurements are performed from 25 to 50 GHz. Nominal bias conditions are shown in **Figure 5.3**, consuming a current of 8 mA, thus a 10.4 mW power consumption (P_{dc}), for each stage. The measured and simulated S-parameters at nominal bias, shown in **Figure 5.6a**, agree well. The LNA exhibits a peak gain of 19.9 dB at 38 GHz with a 3 dB bandwidth from 34.9 GHz to 43.3 GHz. The input and output return losses are below -10 dB across the 36.7-49.5 GHz frequency range. **Figure 5.6b** shows the measured and simulated noise figure. NF measurements agree well with simulations across the whole bandwidth. The LNA achieves a minimum in NF of 2.5 dB at 39 GHz and remains below 3 dB from 34.5 GHz

to 48 GHz.

Two input tones with a 100 MHz spacing (39 and 39.1 GHz) and equal power (swept from −30 dBm to −15 dBm) are applied at the LNA input to determine the third-order intercept point (IP3). The measured output power at the IP3 is shown in **Figure 5.6c**. Extrapolation from the lowest power level is used to extract the input referred IP3, which is of IIP3 = −5.4 dBm.

Table 5.1 compares the performances of the presented LNA with best-in-class CMOS LNAs operating in the 39 GHz band. The proposed LNA has great noise performance, $NF < 3$ dB in the 37-50 GHz band, and low power consumption, featuring comparable performances with state-of-the-art LNAs in (SOI) CMOS technologies. Although it has similar noise perfomance and total power consumption to the LNA in **[176]**, the latter probably features lower IIP3 for several reasons, (i) lower P_{dc} per stage and (ii) increased complexity at output: presence of tunable loads, attenuators and by-pass switch. A second column is added in *this work*'s results for the low-power mode described in more details in the following.

Table 5.1: Comparison to best-in-class 39 GHz CMOS LNA designs.

	This work		[177]		[178]	[179]	[176]
Techno.	22FDX		22FDX		22FDX	45RFSOI	45RFSOI
Freq. (GHz)	36.7 43.3	36.7 42.5	23-43		27.1-29.4 & 37.7-43.9	27-46	37-40
Peak Gain (dB)	19.9	14.8	23	18.2	24.8 & 22.4	21.2	25
NF (db)	2.5- 2.6	3.2- 3.4	3.1- 3.7	3.4- 4.3	3.6-4.9**	2.4- 4.2***	2.3- 2.85*
P_{dc} (mW)	20.8	7.4	20.5	12.1	13.6	25.5	18.6
IIP3 (dBm)	-5.4	-7.3	-19*	N/A	N/A	-11	-12.9

*: graphically estimated. **: dual-band design. 4 dB at 39 GHz.
***: $NF > 3$ dB above 30 GHz, ~ 3.8 dB at 39 GHz.

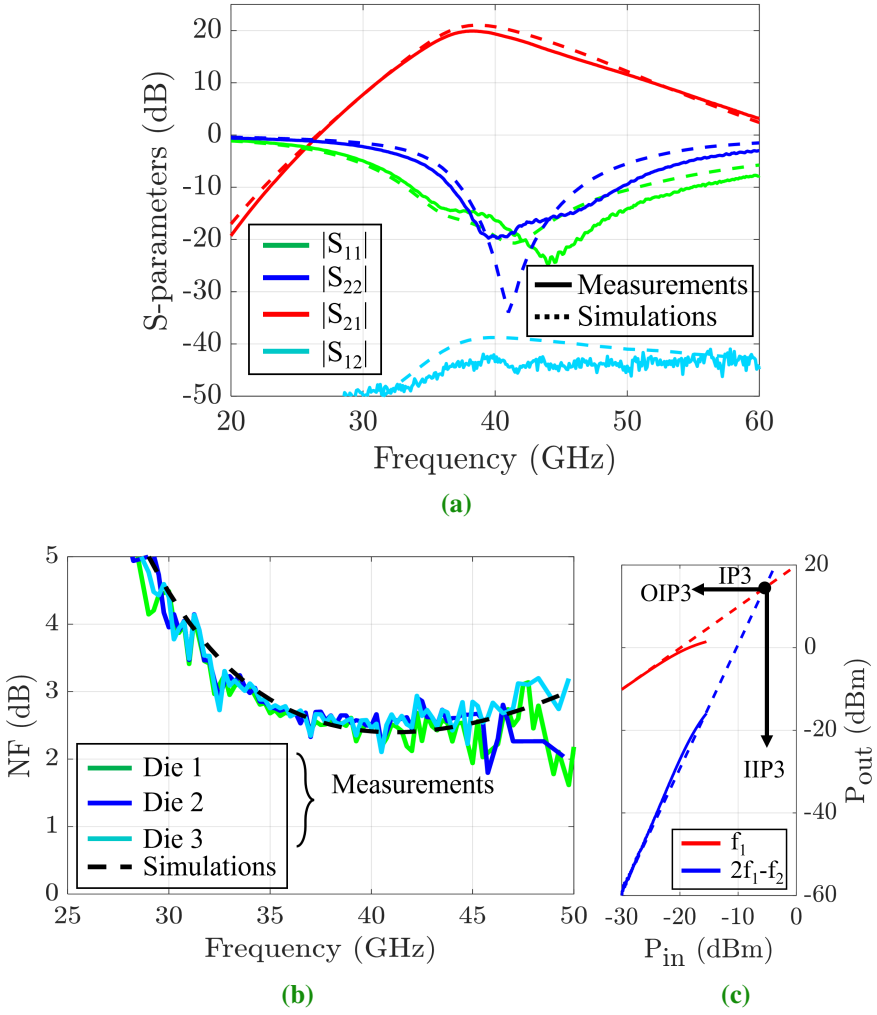


Figure 5.6: (a) S-parameters. (b) *NF* measurements (solid lines) of several dies and simulations (dashed lines). (b) IIP3 measurements. LNA biased in nominal conditions ($V_{g1,3} = 0.4\,\mathrm{V}, V_{g2,4} = 1.1\,\mathrm{V}, V_{dd1,2} = 1.3\,\mathrm{V}, V_{bgi} = 0\,\mathrm{V}$).

5.2.3 Circuit behavior with back-gate bias tuning

The back-gate bias modulates the transistor threshold voltage (V_{th}). So, it affects the FET's operating bias point, as well as the overall LNA's. We limit the back-gate bias range in this work[3] from $-0.2\,\mathrm{V}$ to $2\,\mathrm{V}$, to avoid forward biasing the n-well/p-substrate diode and to prevent reverse breakdown of the diode. To benefit a larger V_{bg} sweep, we change the gate biases from nominal values such that an overall bias of $V_{g1,3} = 0.3\,\mathrm{V}, V_{g2,4} = 1\,\mathrm{V}, V_{dd1,2} = 1.3\,\mathrm{V}, V_{bgi} = 1.25\,\mathrm{V}$ yields equivalent results (P_{dc}, NF, S-parameters, IIP3) to the nominal bias. By modulating the back-gate biases of each stage, we can change each stage working mode, with drain current (I_d) and power consumption variations of 2.2 to 14 mA and 2.85 to 18.1 mW, corresponding to a sweep in V_{bgi} from -0.2 to $2\,\mathrm{V}$, respectively.

Figure 5.7 shows the measured NF and gain versus dissipated power when the back-gate biases of both stages are varied together. We see a drastic change in NF and gain as the transistors are biased closer to the threshold voltage. As both stages do not affect NF or the non-linearity performance in the same way, we can also vary them separately.

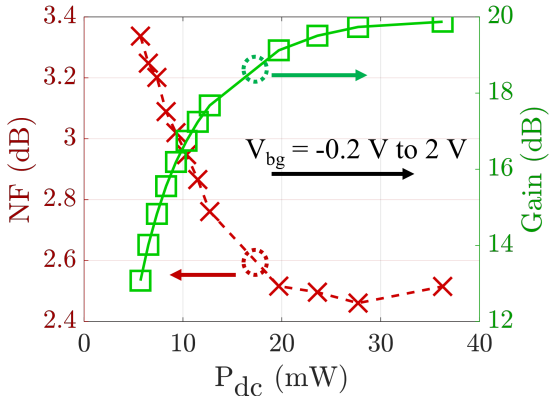


Figure 5.7: Summary of LNA measurements at $V_{g1,3} = 0.3\,\mathrm{V}, V_{g2,4} = 1\,\mathrm{V}, V_{dd1,2} = 1.3\,\mathrm{V}$ and $V_{bg1,2}$ and $V_{bg3,4}$ varying from 0 to 1.25 V. A bias of $V_{bgi} = 1.25\,\mathrm{V}$ yields very close results to the nominal bias detailed above.

Indeed, by varying the back-gate biases of stage 1 and 2, one can trade P_{dc} for NF and gain (affected by stage 1 bias) or P_{dc} for IIP3 and gain (affected

[3] Although not recommended by the technology design rules, we could have extended the bias range. However, this range is wide enough to observe significant variations.

by stage 2 bias mainly). **Figure 5.8** summarizes these trade-offs with data obtained from measurements. Indeed, noise and gain are traded-off for power by biasing the transistors closer to its threshold voltage, thereby lowering f_t and f_{max}, along with larger NF_{min}, but reducing I_d. **Figure 5.9a** shows simulations of f_t, f_{max} and NF_{min} of M1 with interconnects up to JA. The optimal noise impedance is also modified, which further increases the NF for a constant input matching, mainly when biased close to threshold voltage where the FET characteristics have a sharp transition.

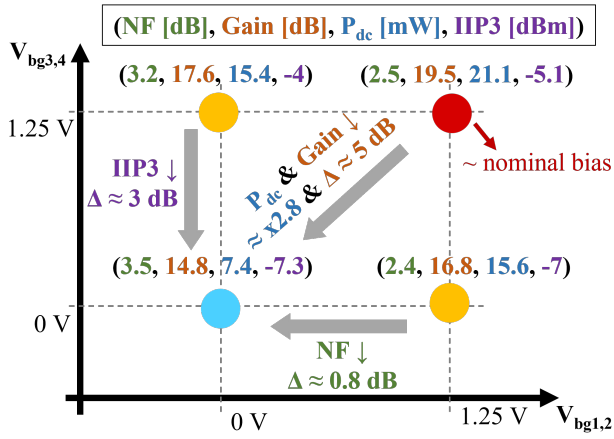


Figure 5.8: Summary of LNA measurements at $V_{g1,3} = 0.3\,\text{V}, V_{g2,4} = 1\,\text{V}, V_{dd1,2} = 1.3\,\text{V}$ and $V_{bg1,2}$ and $V_{bg3,4}$ varying from 0 to 1.25 V. A bias of $V_{bgi} = 1.25\,\text{V}$ yields very close results to the nominal bias detailed above.

IIP3 also deteriorates with lower P_{dc}. Indeed, as displayed in **Figure 5.9b**, the output power of the 3rd intermodulation product remains roughly constant, while the power of the fundamental decreases due to lower gain at lower I_d.

Overall, back-gate biasing offers a high flexibility in circuit design enabling compensation and correction for process, voltage or temperature variation, besides tunability for different operation modes: low-power, low-noise, high-linearity.

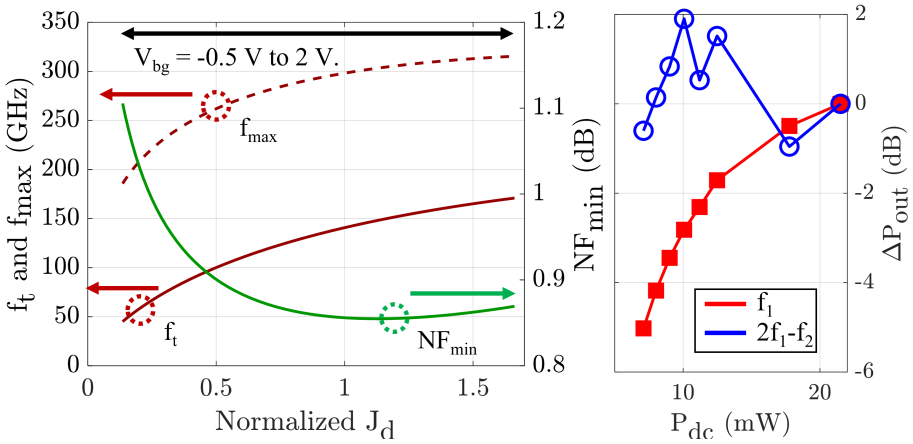


Figure 5.9: (a) Simulated f_t, f_{max} and NF_{min} at 39 GHz of the common-source FET with parasitics up to JA, $V_{gs} = 0.3\,\text{V}, V_{ds} = 0.65\,\text{V}$ and V_{bg} varying from -0.5 to 2 V. (b) 2-tone measurements. Variation of output power at 39 GHz (f_1, red) and 38.9 GHz ($2f_1 - f_2$ blue) for V_{bgi} swept from 0 to 1.25 V and input power (P_{in}) of $-30\,\text{dBm}$.

5.2.4 Impact of underestimated self-heating effect

As we have seen in the previous **Chapter 4**, self-heating effect might be underestimated in the simulated behavior of the LNA [4]. To quantify its potential misestimation, we first need to evaluate the FETs' channel temperature. Due to the similar dimensions of the FETs (all identical) used in the LNA and studied in the previous chapter, let us assume the actual FET thermal resistance is $R_{th,meas} = 202\,\text{K}\,\mu\text{m/mW}/60\,\mu\text{m} = 3.37\,\text{K/mW}$, i.e. the one measured in **Chapter 4**, while the one from the PDK compact model is $R_{th,simu} = 2.27\,\text{K/mW}$.

For a measured dissipated power of 20.8 mW, the worst case estimations[5] of channel temperature increase are 17.5 K and 11.8 K, based on the measured $R_{th,meas}$ and the PDK model $R_{th,simu}$, respectively. However, it should be noted

[4] We had also seen that adding a 10 kΩ series resistor helped improving the measurement-simulation agreement. This element would not have an impact here since the designed LNA already uses 10 kΩ resistors at the back-gate terminals to decouple the RF and dc signals.

[5] Some power is dissipated in the dc probe needles, cables from the dc instruments and on-chip metallic losses, so that it does not participate to an increase in FET channel temperature.

that the measurements are realized in a controlled room temperature of 21 °C, whereas the simulations are ran with a default ambient temperature of 27 °C. So, the actual difference in channel temperature between the estimated 'measurement condition' ($R_{th,meas} = 3.37\,\mathrm{K/mW}$, $T_A = 23\,^\circ\mathrm{C}$) and 'simulation condition' ($R_{th,simu} = 2.27\,\mathrm{K/mW}$, $T_A = 27\,^\circ\mathrm{C}$) is $-0.3\,\mathrm{K}$, which is too small to have a significant impact on the LNA performance.

5.2.5 Contribution to the total noise figure analysis

To identify the main bottleneck in our design with respect to the LNA key-metric noise figure, we will proceed to a quantitative analysis via simulations to evaluate the contribution of each element in the input matching to the NF_{min} of the circuit. The excellent agreement we obtained between simulations and measurements above gives us confidence as to the quantitative accuracy of the following analysis. Note that we carry on this analysis only for the input matching network, as the contribution of successive elements are reduced thanks to the first amplifying stage, according to the well-known Frii's formula **[35]**.

All subsequent figures are given for a simulated frequency of 40 GHz, but the relative numbers are valid for frequencies inside the LNA bandwidth. With separate EM simulations of each element (despite being less accurate than a full EM simulation as described in **Section 5.2.1**), we could identify their noise contribution by changing the location of the input port from the FETs gate input toward the pads and checking the increase in NF_{min} each time an element is added [6].

The results are summarized in **Figure 5.10**, which also shows the position of each element contribution in the LNA's layout and schematic. The circuit without input matching (green), i.e. the contribution of the cascoded FETs and remaining of the circuitry (interstage matching and second stage) yields a total of 1.52 dB of NF_{min}. The major part is due to the intrinsic NF_{min} of the FETs, though the subsequent matching elements and second stage have a contribution of a few hundreds of mdB due to the limited gain of the first stage. The L_1 spiral inductor (red) adds 0.58 dB, and the R_1-C_2 stabilization network (grey) adds 0.24 dB. Finally, the pad and input series capacitor (C_1, yellow) add another 0.12 dB to the NF_{min}, yielding a total simulated NF_{min} of 2.46 dB for the overall

[6] These figures and procedure have been confirmed by replacing each of the analyzed elements by a lumped-based equivalent circuit. The same variations in NF and NF_{min} are observed when the resistive elements of each equivalent circuit are set to zero, therefore confirming the consistency of these numbers.

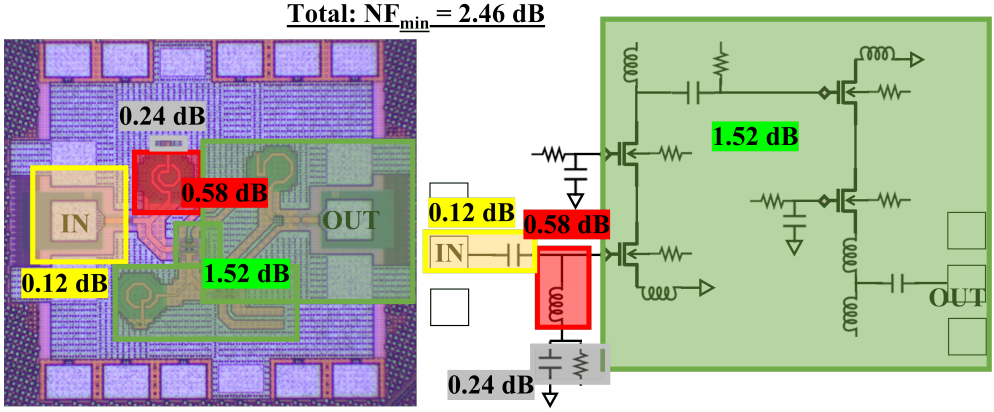


Figure 5.10: Summary of noise contribution analysis.

circuit.

The main noise contribution in the input network is clearly from the spiral inductor L_1. Losses in a spiral inductor can either come from the metal (signal path) or from the substrate (conductive losses). To reduce losses from the metal, we can increase the conductor width or stack several layers. Both have an impact on the inductive value, thus needing a re-design of the inductor. As for the substrate, since this technology is fabricated on a standard resistivity substrate, conductive losses can be reduced by using a more resistive substrate, such as a high-resistivity substrate.

In this section, we have presented a 39 GHz LNA designed in a cutting-edge mm-wave technology. *The prototype*, which was *optimized on a technology supporting a standard resistivity Si substrate*, achieves *noise performance at the state of the art* in (SOI) CMOS technology. After a detailed *NF* contribution analysis, we have identified that the *input spiral inductor* (L_1), the only element *not shielded from the substrate*, is the *main contributor by* 0.58 dB *in the input matching network to the overall LNA noise*. These observations suggest a *potential significant improvement could be achieved in the designed LNA with the use of a higher resistivity substrate*. Impact of the substrate resistivity on the inductor quality factor and loss will be tackled in the next chapter, in which the potential improvement in L_1 quality factor and subsequent LNA *NF* will also be studied.

5.3 24-43 GHz Power Amplifiers in 22 nm FD-SOI

Building on the basics of CMOS-based PAs available in **Appendix F**, two wideband 24-43 GHz PA designed in GlobalFoundries 22FDX® technology are presented in this section. The first PA (PA1) relies on a 3-stacked FET output stage and a distributed balun, covering the 24-43 GHz bands. The second one (PA2) uses PA1 in a balanced topology with configurable 90° hybrid couplers, enabling a multiband operation. After a design overview, their small-signal, large-signal continuous-wave (CW) and modulated signal performance are assessed and their behavior with back-gate bias modulation analyzed. Finally, the overall performance is benchmarked with the state of the art in CMOS technology.

5.3.1 Instantaneously wideband PA (PA1): design

PA1 is based on a pseudo-differential two-stage configuration, with the schematic shown in **Figure 5.11a**. The power (second) stage uses a 3-stacked FET differential architecture **[180]**, while the driver (first) stage features no FET stacking. Their circuit schematics are shown in **Figure 5.11b** and **Figure 5.11c**. Both stages use cross-coupled neutralization capacitors to stabilize the amplifier in differential operation **[181]**. The single-ended to differential (and inversely) transformation is operated by the input and output baluns that also perform the required impedance matchings. An inter-stage transformer converts the input impedance of the power stage into the required impedance of the driver stage for optimum large-signal performance. The gate and drain biases are fed to the transistors through the ac-common ground of the transformers' center-taps as shown in **Figure 5.11a**. Large bias resistors are added in the gate bias lines to stabilize common-mode operation **[181]**. The back-gate terminals of all FETs are connected to dc pads via large bias resistors, to decouple RF and dc operation (not shown in **Figure 5.11**).

The PA design is done in several steps. First, the output stage is designed, thereby fixing the main large-signal, non-linear performances, such as saturated output power (P_{sat}), power added efficiency, compression, etc. Then, an output matching network is carefully designed. Since losses in this matching network reduces the output power, this matching network's performance has a direct impact on the overall performance of the PA. The driver stage and inter-stage matching network are subsequently designed to provide enough linear input power to the power stage for normal operation. Finally, the input matching is designed to match the input impedance to 50 Ω.

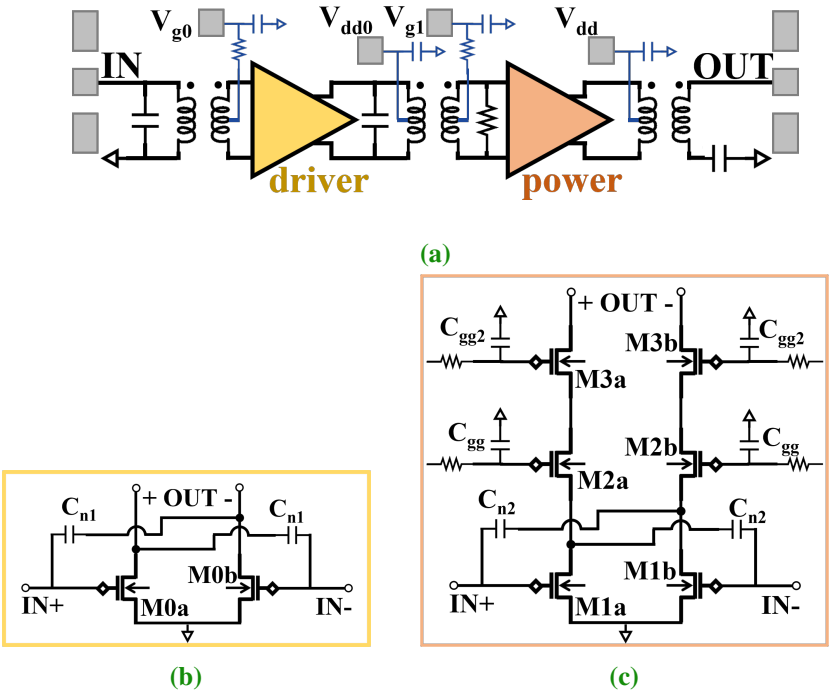


Figure 5.11: Schematic of PA1 (a), the driver stage (b) and power stage (c).

As the output matching network is the most important passive element in the PA design, it is also designed as a standalone structure for characterization. The measurements of this structure are used to adjust EM simulations (by changing the EM stack to a non-typical corner for instance) and obtain *adjusted post-layout simulations* of all matching networks.

Giving a detailed design description would be too long in this section. So, only a few selected key design points will be presented here. The interested reader can find a more complete design description in **Appendix G**.

We first start detailing the design of the power stage. Then, the design of the output matching is described, and, finally, we briefly mention the designs of the driver stage and input and inter-stage matching networks.

Power stage design

A detailed schematic of this stage is given in **Figure 5.11c**. The output stage uses nMOSFETs super-low threshold voltage with a gate length of 20 nm and

a total FET width of 160 µm for all FETs. The 20 nm gate length is a good trade-off between high RF performance (f_t and f_{max}) and reliability, for which the breakdown voltage is not significantly lower than other sub-30-nm gate lengths **[182]**. The total FET width results in a trade-off between high P_{out} and input impedance transformation over a large bandwidth. A relaxed poly-pitch is used (2xCPP), which increases f_t and f_{max}, reduces the source and drain extrinsic resistances, and relaxes the electromigration constraints. The source and drain terminals are contacted via an M1-C2 staggered metal stacking, thus significantly lowering the drain-source capacitance, for a negligible increase in drain-source resistance: reduce reactive elements for phase mismatch, and ease of output impedance matching. This optimum design choice yields peak f_t and f_{max} of 320 and 280 GHz, respectively, while meeting electromigration rules for a 5 years lifetime mission profile[7] operation at 125 °C.

Overall, the interconnects parasitics are extracted via a smart partitioning between Spice-netlist-based parasitic extraction (PEX) tool and 2.5D EM based simulations. The parasitics at the vicinity of each unit transistor cell and the shunt gate capacitors (C_{gg} and C_{gg2}) are extracted with Quantus RC, including the bottom metal layers (M1 to C5 or JA, according to the FET terminal). The remaining parasitics (interconnects between FETs and input/output) are extracted with a 2.5D EM solver on all metal layers for a more accurate description of distributed effects.

1. Biasing

The V_{dd} bias voltage is set to 2.4 V, to present a dc V_{ds} of 0.8 V to each FET, the nominal voltage in this technology. Small variations of V_{ds} around 0.8 V has little influence on the FET parameters, such that we can safely design with this V_{dd} bias and afterwards analyze the effect of V_{dd} variation at the PA level, while it is still operating in close to optimal designed conditions (with appropriate load impedance, same input impedance).

As both V_{gs} and V_{bg} modulates the drain current and class of operation, in the following paragraphs, the back-gate voltage is set to 0 V, to discuss the design choice of the V_{gs}. We will come back to the choice of V_{bg} later.

By modulating the drain current, the gate bias determines the operating class of the PA. At low and medium power ranges, class A linearity is better than class B. However, as power increases close to saturation, due to internal

[7] Based on an LTE product, a 5 years lifetime use-case scenario gives a mission profile of 2027 hours = 0.23 years, at a junction temperature of 125 °C (which corresponds to the ambient temperature for on-wafer measurements).

harmonic cancellations, class B features a sweet-spot in 3rd order harmonic (when linearity is higher) at a high input power, resulting in a better linearity at high power region than class A [183] (it is illustrated below for our case). In addition, class A works inherently with lower efficiency (maximum 50 % in the ideal class A, instead of up to 78.5 % in the ideal class B, as explained in Section F.2.3 of Appendix F). Therefore, by carefully choosing the gate bias that controls the PA operating class, we can simultaneously achieve high efficiency and linearity.

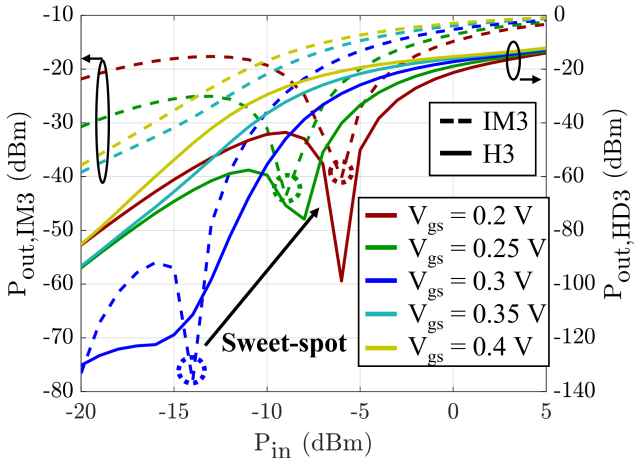


Figure 5.12: Output third-order intermodulation product (IMD3) power (dashed lines, left axis) from simulations and output third harmonic power (solid lines, right axis) from single-tone analytical model of [184] versus input power at different gate biases.

An analytical analysis of the large-signal behavior (neglecting memory effects) of a common-source CMOS FET as a power amplifier is explained in [184] and also applied in [183]. A full description of the large-signal model is beyond the scope of this chapter. The take-away messages are that some sweet-spots in linearity (minimum in the generated 3rd harmonic, thus in the third-order intermodulation product, IMD3) exist (which can be traced back to the memoryless non-linear transfer function of a CMOS PA) and can be pushed to lower or higher input powers by varying the gate bias. Similar results can be found for this 22 nm FD-SOI technology. Simulations of the unit transistor cell designed above are reported in Figure 5.12. It shows the third-

order intermodulation power of the unit transistor cell in a common-source topology, with 2 input tones spaced by 1 kHz at 1 MHz (to avoid memory effects) and loaded by a 50 Ω port. In addition, the analytical model from [184] is constructed from the simulated dc trans- and output characteristics of the FET. The third harmonic power (H3) computed from the model is plotted in Figure 5.12 in solid lines. The excellent agreement in model and simulation confirms here again the validity of the large-signal model. From Figure 5.12, we observe that $V_{gs} = 0.3\,\mathrm{V}$ yields good linearity at medium power levels up to relatively large input power. Furthermore, $V_{gs} = 0.3\,\mathrm{V}$ is also a good compromise between high linearity and sufficient gain that is fundamental at mm-wave frequencies. Indeed, as shown in Figure 5.13, the f_t and f_{max} (thus gain) quickly drops as the gate bias approaches the threshold voltage. A V_{gs} of 0.3 V still yields $f_t = 141\,\mathrm{GHz}$ and $f_{max} = 202\,\mathrm{GHz}$ which is large enough for 28-39 GHz operation.

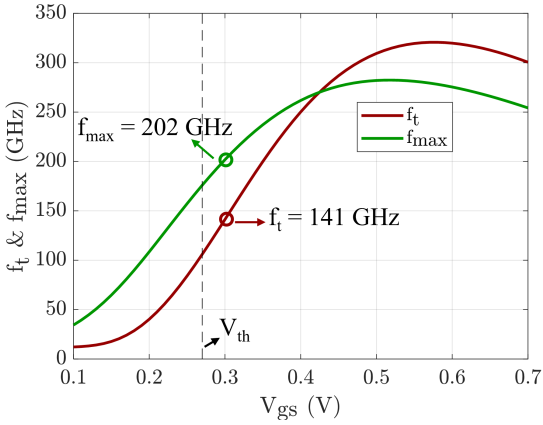


Figure 5.13: f_t and f_{max} versus gate bias for the designed unit FET cell. The threshold voltage is 0.27 V for $V_{bg} = 0\,\mathrm{V}$. $V_{gs} = 0.3\,\mathrm{V}$ and $V_{ds} = 0.8\,\mathrm{V}$ yields $f_t = 141\,\mathrm{GHz}$ and $f_{max} = 202\,\mathrm{GHz}$.

As for the back-gate voltage (V_{bg}), it is important to keep in mind its effect on the FET characteristics. V_{bg} changes the threshold voltage, thus the drain current (for a fixed V_{gs}) and thereby the class of operation. Thus, I_d is modified by both V_{gs} and V_{bg} variations, yet I_d is much more sensitive to V_{gs} than to V_{bg} variation. Indeed, in the 22 nm FD-SOI technology, the V_{th} has an approximately linear relationship with V_{bg} characterized by a slope of $\sim -80\,\mathrm{mV/V}$ [161]

for the SLVT FETs. So, for $+1\,\mathrm{V}$ increase in V_{bg}, V_{th} decreases by $80\,\mathrm{mV/V}$ and the overdrive voltage ($V_{ov} = V_{gs} - V_{th}$) increases by $80\,\mathrm{mV/V}$. The dc trans-characteristics of the unit transistor cell used in the PA design is shown in **Figure 5.14**. Due to the n-type back-gate of SLVT transistor, only positive (from ~ -0.3 to $+2\,\mathrm{V}$) V_{bg} values are allowed to prevent forward biasing the P-N diode between the back-gate and substrate node (as for the LNA). Note that the V_{bg} values recommended by the PDK are 0 to 2 V.

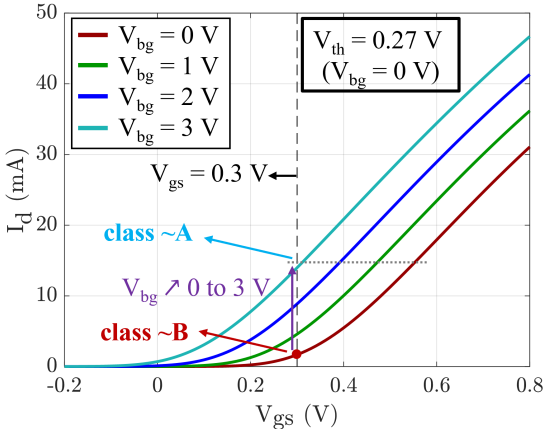


Figure 5.14: Trans-characteristics of the designed unit cell FET for different back-gate voltages ($V_{ds} = 0.8\,\mathrm{V}$).

We fix $V_{bg} = 0\,\mathrm{V}$ in nominal operation. Such a value of V_{bg}, combined with the previously determined $V_{gs} = 0.3\,\mathrm{V}$ results in deep class AB operation with good trade-off between linearity and efficiency. Moreover, this $V_{bg} = 0\,\mathrm{V}$ value can be adjusted after fabrication to compensate for process variation inducing small V_{th} variation. With V_{bg} varying from -0.5 to $+3\,\mathrm{V}$, it can compensate for -240 to $+40\,\mathrm{mV}$ of V_{th} variation. Finally, and more importantly, we can easily change the PA class of operation from deep class AB to class A, by simply increasing the V_{bg} bias, as shown in **Figure 5.14**. So, $V_{bg} = 0\,\mathrm{V}$ is selected for this design but can be varied during characterization to (i) compensate for V_{th}-process variation and (ii) change the PA class of operation, at a small penalty of non-optimal load impedance. Indeed, load-pull simulations (**Figure 5.15**) show that the optimal impedance remains roughly constant and close to the selected load impedance $Z_{opt,L}$ (black dot) with increasing V_{bg}.

Even though the differential topology can remove even harmonics from the

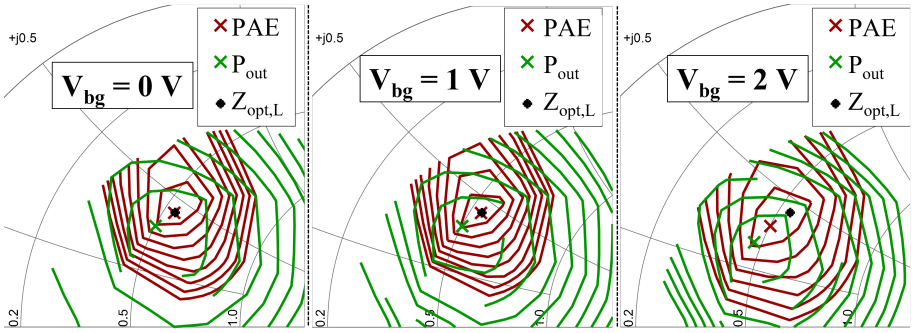


Figure 5.15: Load-pull simulations at 39 GHz of the power stage for different V_{bg} biases, moving from a deep-class AB operation to class A. The selected load impedance for the output stage is $Z_{opt,L}$ (black dot). The Smith charts are normalized to a 100 Ω reference impedance.

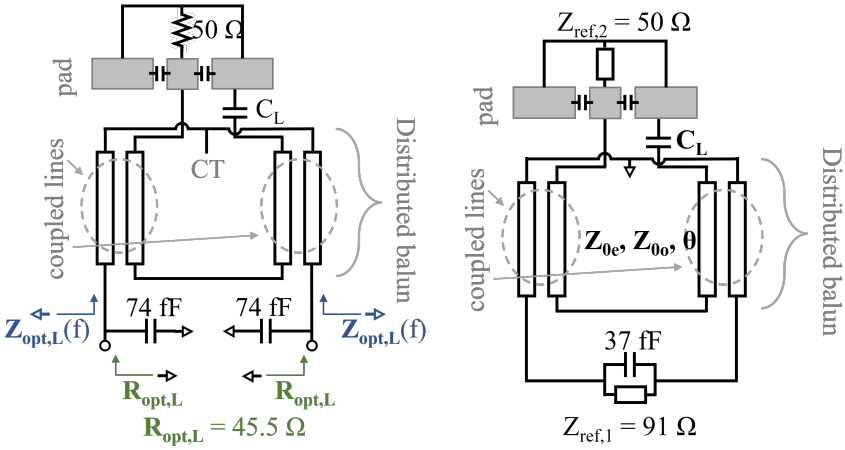
output, even harmonics are still present in internal nodes of each branch and generate side-band asymmetries and other effects reducing the PA efficiency **[183, 185, 186]**. Furthermore, parasitic capacitances in intermediate nodes contribute to phase misalignment, which degrades the output power and efficiency **[180]**. Some methods exist to compensate for these effects, but they are narrowband, hence not suited to a wideband PA design.

Distributed output balun

Once the output stage is designed, load-pull simulations are performed at several frequencies to evaluate the optimal impedance to present at the output. Optimal large-signal power matching is achieved when reactive elements are compensated and the intrinsic loadline is purely resistive. Due to the nature of the output stage design, an equivalent impedance ($Z_{opt,L}$), made of a resistance and capacitance of 45.5 Ω ($R_{opt,L}$) and 74 fF in parallel (for each branch), maximizes the output stage large-signal performance over a large bandwidth, see **Figure 5.16a**. The capacitance accounts for the overall capacitive couplings in the output stage that dominate the inductive ones and the resistance is related to the optimal loadline achieved for each stacked FET.

1. Design

The output matching circuit is shown in **Figure 5.16a**. The design of the output balun is based on the slightly modified equivalent circuit shown in **Figure 5.16b**, which converts a 50 Ω load in the required differential optimal load



(a) Sketch of output matching design with optimal load impedance. **(b)** Sketch of distributed balun design, along with design parameters.

Figure 5.16

impedance (represented by the parallel 37 fF capacitance and 91 Ω reference impedance port 1). The impedance transformation criterion corresponds to minimizing $|S_{11}|$ in the configuration shown in **Figure 5.16b**, which is easier to define in an optimizer tool. The pair of coupled transmission lines (TLs) forms a transformer. Using a distributed element (coupled TLs) to model a transformer, as in **[187]**, has the advantage of being more accurate over a large bandwidth than a lumped element-based model.

Thanks to the rich BEOL available in this technology, several options to design the coupled TLs are possible. Lines made in 18.2 µm-wide stacked QB-LB with a gap of 4 µm and a distance of 54.8 µm to the stacked M1-LB ground resulted in the lowest insertion loss (IL). A top view of the output matching network is shown in **Figure 5.17**, with the distributed balun, output pad, series capacitor, bias feed and decoupling capacitors.

It is also interesting to note from **Figure 5.17** that the probe pad ground and the local coupled line ground (that is also connected to the differential ground) are not connected on-chip. This voluntary disconnection is made in order to reduce the asymmetry at the balanced ports **[188]**. It is further explained in **Appendix G**.

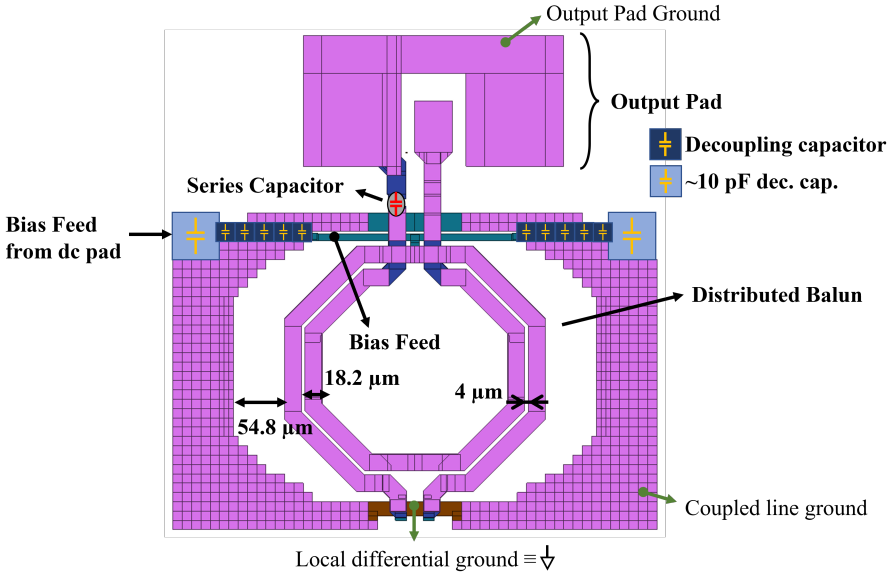


Figure 5.17: Top view of designed output matching with cross-section dimensions.

2. Simulation results

The simulated 2-port S-parameters, corresponding to the equivalent circuit of **Figure 5.16b**, including the bias feed line and decoupling capacitors up to the dc pad, are shown in **Figure 5.18**.

The resulting output matching features a return loss larger than 10 dB from 24 to 51 GHz and above 20 dB from 28 to 44 GHz, therefore accurately achieving the desired impedance transformation. The insertion loss is non-negligible, but remains controlled over the entire designed frequency range: $\sim 1-1.5$ dB from 24 to 45 GHz. Furthermore, it should be reminded that these simulations include all losses from the output of the FETs up to the probe tips. Initial design simulations are shown in dashed lines. The distributed balun (along with the output probe pad) is also designed as a standalone structure for characterization. The measurements of this structure and adjusted simulations to better agree with measurements are described in **Appendix G**, **Section G.1.2**. Adjusted simulations underestimate the measured transmission losses by 0.1 dB and the measured matching is shifted by ~ 1.8 GHz toward higher frequencies as shown in **Figure G.14**. These new simulations are in solid lines in **Figure**

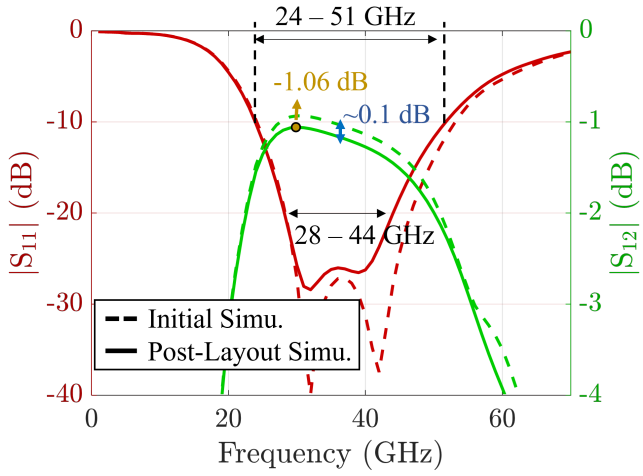


Figure 5.18: $|S_{11}|$ (left axis) and $|S_{12}|$ (right axis) of the designed output matching network in the configuration shown in **Figure 5.16b**. Initial design simulations in dashed lines. Adjusted post-layout simulations based on hardware in solid lines.

5.18.

3-port simulation is carried out in **Appendix G** and demonstrate that the impedances seen by each branch are well balanced, with a small residual imbalance remaining ($|2\Delta Z_L/(Z_{L,1}+Z_{L,2})| < 10\,\%$ from 24 to 43 GHz).

Driver stage and input/inter-stage matching design

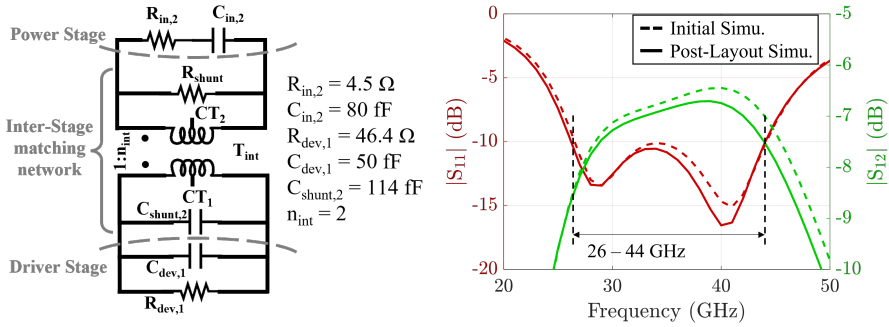
1. Driver stage

A schematic of the driver stage was shown above in **Figure 5.11b**. The driver stage is designed with a differential pair of common-source FETs and neutralization capacitors. The same unit FET cell from the output stage is used, but only repeated twice (total FET width of 80 µm). The overall interconnects and layout are similar to the output stage.

2. Inter-stage matching network

Load-pull simulations are performed to determine the appropriate wideband impedance to present at the output of the driver stage, in a similar fashion as the output load impedance of the power stage. It is found that the inter-stage matching network has to transform a 4.5 Ω resistance in series with a 80 fF capacitance (input of power stage as mentioned above) into the complex

conjugate[8] of a 46.4 Ω resistance in parallel to a 50 fF capacitance over the whole design bandwidth. As mentioned above, the inter-stage matching network is realized with a transformer, a lumped-based schematic can be found in **Figure 5.19a**. Due to the large resistance transformation ratio, to achieve such a wideband impedance transformation, a 365 Ω shunt resistor is added in parallel to the input of the driver stage. The design of the unit resistor cell must take into account the large-signal power injected to the power stage, more details can be found in **Appendix G**.



(a) **(b)**

Figure 5.19: Inter-stage matching network, schematic (a), S-parameter simulations (b). Initial design simulations in dashed lines. Adjusted post-layout simulations in solid lines.

Figure 5.19b shows the simulated frequency response of the designed inter-stage matching network. A decent matching, implying a correct impedance transformation, is achieved from 26 to 44 GHz. This wideband impedance matching comes at the cost of low insertion loss caused by the presence of the shunt resistor.

3. Input matching network

The input matching network is designed in a similar way to the inter-stage matching (see **Figure 5.20a**). In this case, we aim at matching a 10 Ω resistance in series with a 41 fF capacitance (impedance seen at the input of the driver stage) to the 50 Ω input port.

The simulated S-parameters of the input matching is shown in **Figure 5.20b**. The 10 dB input return loss is not met across the whole bandwidth, but

[8] Power matching condition.

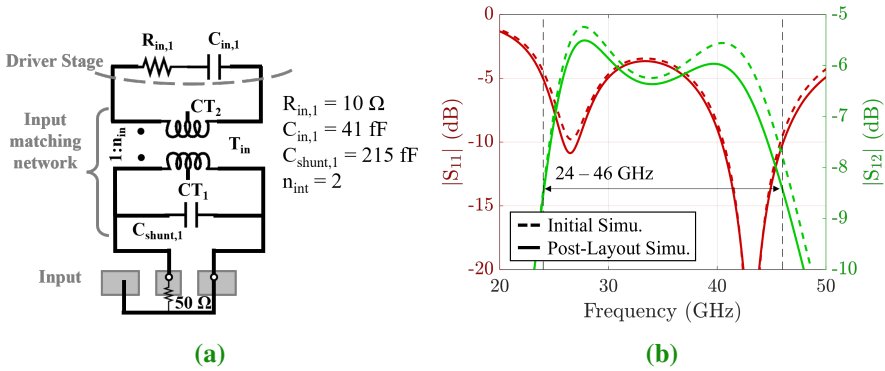


Figure 5.20: Input stage matching network, schematic (a), S-parameter simulations (b). Initial design simulations in dashed lines. Adjusted post-layout simulations in solid lines.

the matching is designed to maintain a non-too steep amplifier gain drop at the 24 and 43 GHz bandwidth edges.

5.3.2 Instantaneously wideband PA (PA1): results

The fabricated PA1 is shown in **Figure 5.21**. It is measured with a Keysight PNA-X VNA from 100 MHz to 67 GHz under small-signal conditions and from 24 to 47 GHz in continuous-wave large-signal sweeps. Two RF Ground-Signal-Ground (GSG) I67 probes from FormFactor are used for the RF paths and two Multi-Contact Wedge dc probes from GGB Picoprobe bring the dc biases. The small-signal measurements are calibrated with a Line-Reflect-Reflect-Match (LRRM) calibration performed on the 101-190C calibration substrate. The large-signal measurements are also de-embedded to place the reference plane of the small- and large-signal measurements at the probe tips.

First, measurements at the nominal gate or overdrive bias condition are shown, including additional measurements at a higher supply bias (V_{dd}). Then, we analyze measurements made at different back-gate biases. Measurements and simulations for modulated signals are covered later in **Section 5.4**.

Nominal gate bias

The nominal bias condition explained in the previous sections is $V_{g0} = V_{g,1} = 0.3\,\text{V}, V_{g2} = 1.165\,\text{V}, V_{g3} = 2.03\,\text{V}, V_{dd} = 2.4\,\text{V}$ and the back-gate biases are varied to reach the target drain current I_{d0} and I_{d1} of 6.8 mA and 13.5 mA for

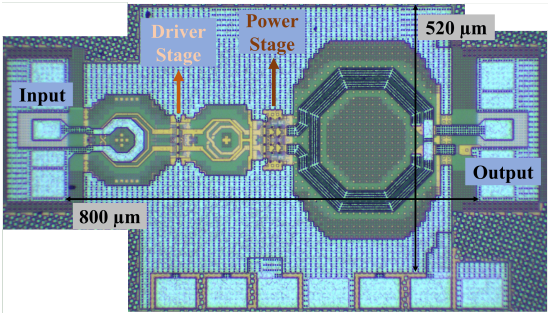


Figure 5.21: Fabricated wideband power amplifier (PA1).

the driver and power stages, respectively.

1. Small-signal measurements

The (adjusted post-layout) simulated and measured S-parameters are shown in **Figure 5.22**. The PA features a peak gain of 27.7 dB at 28 GHz and a smaller local peak of 18.8 dB at 44 GHz. The 3 dB-bandwidth associated to the low-and high-frequency peaks span from 24.7 to 30.5 GHz and from 32.8 to 47.3 GHz, respectively. The post-layout simulations agree well with measurements. A small mismatch in peak gain (0.8 dB) is observed and can be partially explained by a better input matching. The measurements also show an overall shift to higher frequencies (shift of 2.4 GHz around 43 GHz, less than 5 %) in the simulated frequency response, similarly to the output distributed balun measurement-simulation correlation presented in **Section 5.3.1**.

2. CW large-signal measurements

Large-signal measurements are also performed, by varying the RF power of a single tone at the input. **Figure 5.23** shows the output power and PAE at 1 dB compression level (P1dB) and at peak PAE. The measured peak PAE goes as high as 36.4 % at 30 GHz, for a corresponding P_{sat} of 18.3 dBm, the P_{sat} is maximum (18.6 dBm) at 31 GHz with an associated peak PAE of 35.7 %. Because of the deep-class AB operation, the 1 dB compression point is close to the peak PAE, such that the output-referred 1 dB compression power (OP1dB) varies from 16.2 to 18.1 dBm across the 24 to 43 GHz bandwidth. The corresponding PAE at P1dB varies from 26.8 % (at 43 GHz) to 36.1 % (at 30 GHz).

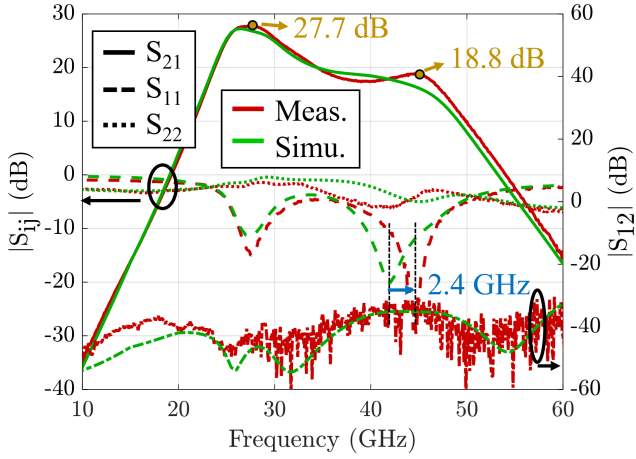


Figure 5.22: Measured and simulated S-parameters of PA1, at nominal bias condition.

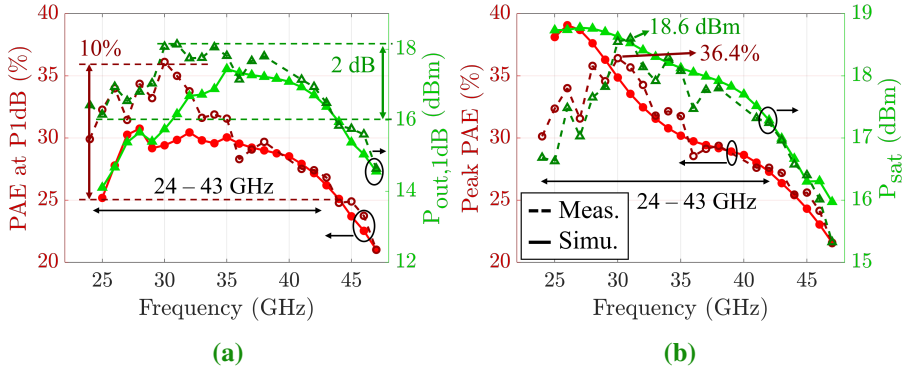


Figure 5.23: PAE (left axis) and P_{out} (right axis) of the PA1, at 1 dB compression point (a) and at peak PAE (b). Measurements in dark, dashed lines and simulations in light, solid lines. Nominal bias.

Figure 5.24 shows the gain, PAE and AM-PM[9] as a function of output power for several fundamental frequencies. As we can observe from **Figure 5.23** and **Figure 5.24**, an excellent agreement is obtained between simulations and measurements above ~ 32 GHz. Below 30 GHz, the peak PAE is lower than expected and at a much lower output power level (see **Figure 5.24b**). Indeed, the PA enters in saturation earlier than anticipated from simulations (visible at 26 GHz in red at **Figure 5.24a**).

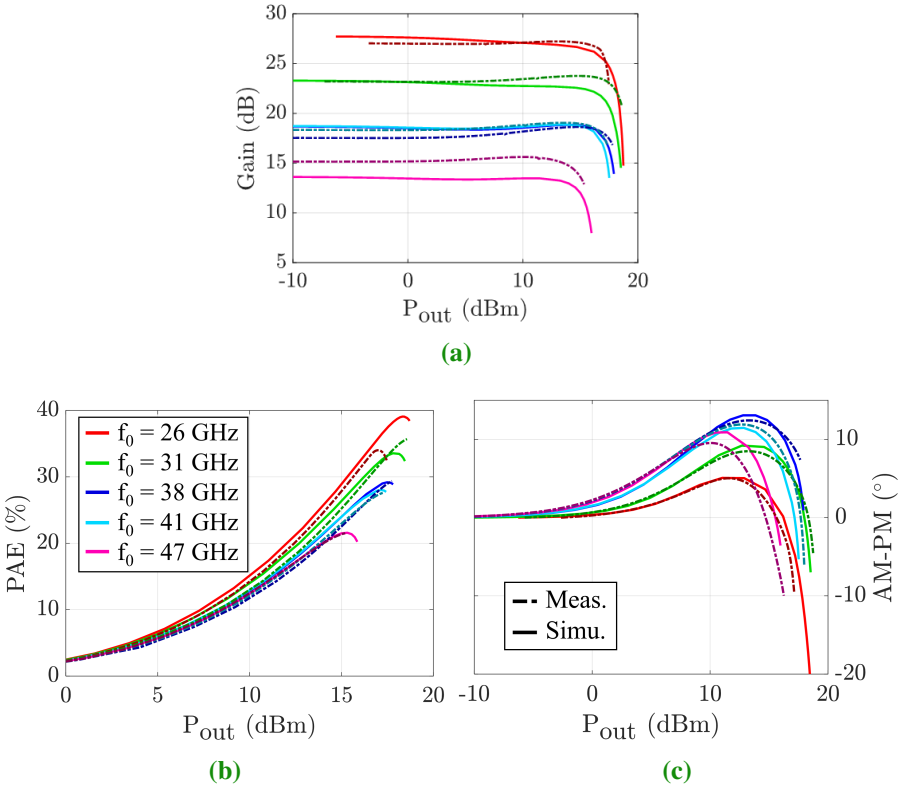


Figure 5.24: Gain (a), PAE (b) and AM-PM (c) versus output power of PA1. Measurements in dark, dashed-dot lines and simulations in light, solid lines. Nominal bias.

[9]Output signal phase variation due to input signal amplitude variation.

Additional measurements performed at higher V_{dd} for the power stage (shown in **Figure 5.25**) seem to indicate that the driver is compressing earlier than expected below 30 GHz. The reason is likely due to a frequency shift in the inter-stage matching (indeed a ~ 1.8 GHz shift still exists between post-layout simulations and measurements of the output balun, cf. **Figure G.14**) that exhibits a sharp transition below 30 GHz, such that a non-optimal impedance is presented at the driver stage output below 30 GHz, thereby making the driver stage compress earlier.

Measurements conducted at $V_{dd} = 2.7$ V[10] are shown in **Figure 5.25** and compared to the previous measurements at nominal bias conditions ($V_{dd} = 2.4$ V). By increasing the bias supply, one can trade-off performance for reliability. Indeed, by increasing the V_{dd} bias, the V_{ds} maximum voltage swing at transistor-level increases, which thus increases the maximum output power. The peak PAE increases as well, because the knee voltage is unchanged (cf. **Section F.2.2**).

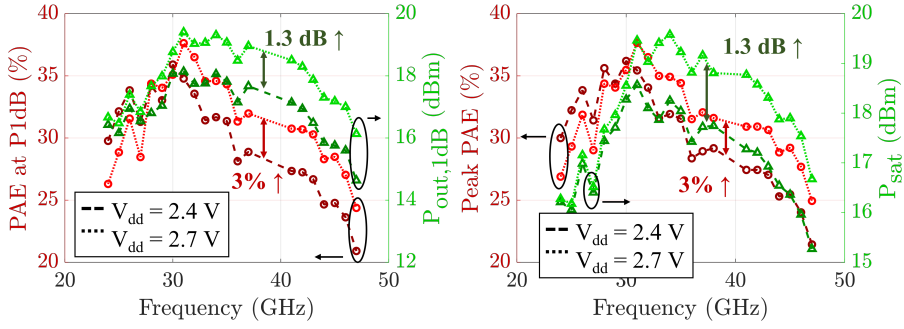


Figure 5.25: PAE (left axis) and P_{out} (right axis) of the PA1, at 1 dB compression point (a) and at peak PAE (b). Measurements at nominal $V_{dd} = 2.4$ V bias in dark, dashed lines and at increased $V_{dd} = 2.7$ V bias in light, dotted lines.

Only the power stage bias is modified, as the driver stage is fed by a distinct supply: V_{dd0}. Overall, a 1.3 dB and 3 % increase in output power and PAE, respectively is achieved at frequencies above 30 GHz, while no significant

[10] Additional dc biases are also modified to ensure the same overdrive voltage on each stacked FET (including the common-source FET). Since the V_s of the stacked FETs increase by 0.1 V and the $V_{g,i}$ are already fixed, we vary the back-gate voltages (increase by 1.25 V) of the stacked FETs to shift the V_{th} and keep a constant overdrive voltage for all FETs.

variation is observed below 30 GHz. The strong improvement only observed above 30 GHz is in agreement with the statement made above that the driver stage non-linear response dominates the PA large-signal performance below 30 GHz,

Back-gate bias variation

As shown in the above figures, the deep class AB operation features large P_{out} and PAE at 1 dB compression point, close to the peak PAE, however, it comes with significant AM-PM distortion at medium power levels (see **Figure 5.24c**), which degrades EVM **[189]**. As mentioned above, by increasing V_{bg}, the PA operation class shifts to class A, with improved AM-PM distortion. However, AM-AM[11] distortion deteriorates, and the $P_{out,1dB}$ and associated PAE decrease significantly too. This trade-off is shown in **Figure 5.26** at a measured frequency of 35 GHz.

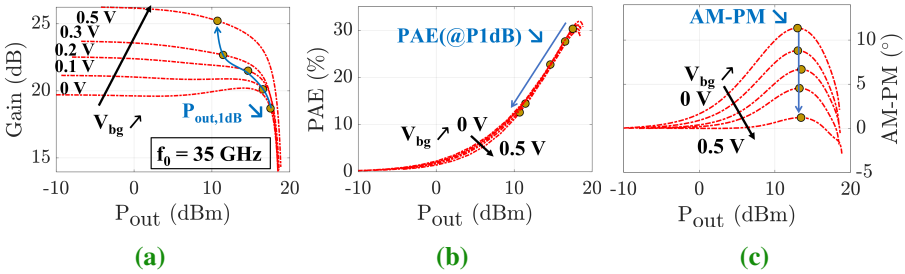


Figure 5.26: Gain (a), PAE (b) and AM-PM (c) versus output power of PA1 for different $V_{bg,i}$ biases from 0 V to 0.5 V. Large-signal CW measurements at 35 GHz. 1 dB compression point in P_{out} and PAE (a, b) and peak AM-PM distortion (c) are shown in yellow dots.

This interesting trade-off is further explored in **Section 5.4** for modulated signals in which the PA is working in high linearity regime at back-off power.

Stability

Stability is always important to be achieved in an amplifier. In this thesis, we only analyze small-signal stability. A circuit is unconditionally stable if the Rollett factor K is larger than 1 and $|\Delta| \equiv |S_{11}S_{22} - S_{12}S_{21}| < 1$[12]. If these

[11] Output signal amplitude variation due to input signal amplitude variation.

[12] Assuming the circuit is also stable for open and short circuit at input and output **[190]**.

conditions are fulfilled, the circuit is stable in small-signal conditions for any load and source impedances. Even though this condition is not sufficient for power amplifiers that often work in non-linear regime, stability analysis is a rather complex topic and will not be thoroughly explored here. An interesting non-linear stability analysis approach that could be envisaged is the one described in [181].

The Rollett factor and $|\Delta|$ are shown in Figure 5.27 for PA1 at nominal bias condition. We observe that the criterion $K > 1$ is not met around 23.2 and 29 GHz. The post-layout simulations reproduce well the measured trend. This was not expected at design time as shown in the 'initial simulations', for which a margin is even present. This discrepancy probably comes from some non-negligible coupling between the transformers of different matching networks that were unaccounted for in the initial simulations and have been included in the post-layout ones.

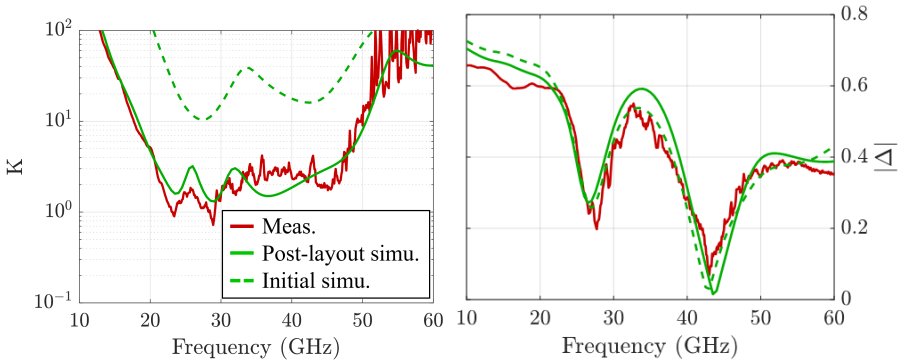


Figure 5.27: Measured (red) and simulated (green) Rollett factor (a) and $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$ (b). Initial simulations (dashed lines) and adjusted post-layout simulations (solid green lines).

Even if not desirable, not guaranteeing unconditional stability does not necessarily means potential instability, as it depends on the source and load impedances. However, stability usually gets worse as gain increases, which can be achieved with larger back-gate bias. Indeed, Figure 5.28 shows measurements at different V_{bg} swept from 0 V to 1 V. For $V_{bg} > 0.5$ V, $K < 0$ and $|S_{22}| > 0$ dB, which means that PA1 presents a negative resistance at the output

port. For an oscillation to take place and amplify, additional conditions need to be satisfied, which depends on the output load value. All measurements (at different biases) have been performed under 50 Ω source and load impedances, and no oscillation or instability has been observed, which indicates that the PA is stable. Although not satisfying for real life application, it is enough for our further studies.

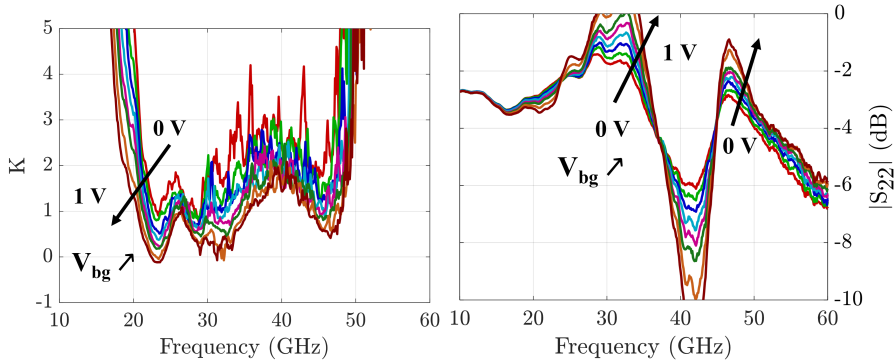


Figure 5.28: Measured Rollett factor (a) and $|S_{22}|$ (b) for different back-gate biases: from 0 V to 1 V.

Impact of underestimated self-heating effect

As we have previously seen in **Chapter 4**, self-heating effect might be underestimated in the simulated circuit behavior[13]. To quantify its potential misestimation, we perform a similar analysis as what we have done for the LNA, i.e. evalute the FETs channel temperature. The normalized thermal resistance extracted from simulations of the FET used is 80 K µm/mW (instead of the ∼ 130 K µm/mW from previous chapter). Since the FETs dimensions significantly vary from previous chapter, we will assume that there is still a 30 % underestimation by the PDK, although it should be confirmed via measurements of the same FET.

[13]The resistor in series with the back-gate terminal, which helps improving the low-frequency measurement-simulation agreement of the MOSFET (cf. **Chapter 4**) has no impact on the PA behavior for the same reason as the LNA, because it is already used to decouple RF and dc signals.

The highest measured peak in power consumption yields a 180 mW for the power stage, which should be equally dissipated by all stacked FETs if well designed. So, each individual FET of 160 µm total width should dissipate up to 60 mW. Therefore, the increase in channel temperature is of 30 K, estimated from the PDK's R_{th}. Here again, we could argue that the simulator ambient temperature is larger than the ambient temperature in measurement conditions. Nevertheless, in the worst case (assuming the ambient temperature is the same in both cases), the channel temperature would only be underestimated by ~ 9 K, which is not a large discrepancy. Still, simulations at an ambient temperature of 36 °C (+9 °C) are performed and a negligible variation in peak power values ($<$ 0.05 dB in P_{sat} and < 0.2 % in peak PAE) is observed. Therefore, it demonstrates once again that a 30 % misestimation in self-heating effect has a negligible impact on the designed circuit. The same conclusion can also be drawn for the balanced PA, as it uses two cells of this wideband PA.

5.3.3 Configurable balanced PA (PA2): design

In the context of mm-wave 5G deployment, the use of beamforming is crucial as it alleviates the power requirements on each front-end module cell by combining together the power radiated by several antennas in a chosen direction. However, in beamforming phased array, the environment difference seen by each antenna can lead to antenna mismatch (described by voltage standing wave ratio, VSWR) and to harmful voltage overshoot at the output of individual power amplifiers.

Balanced amplifier topology provides several advantages, including robustness to input and output impedance mismatch, which is ideal for beamforming phased array implementation. Moreovers, power combining with the use of quadrature hybrid couplers at the output improves the maximum achievable output power and 1 dB compression point by 3 dB (in case of ideal hybrid coupler).

A schematic of the balanced topology is shown in **Figure 5.29**. Two power amplifier unit cells are combined via quadrature hybrid couplers at the input and output. The hybrid coupler design is explained below. Furthermore, 50 Ω resistors are added at the 4$^{\text{th}}$ port of each hybrid coupler to dissipate the reflected power. In case of output (antenna) mismatch, the reflected power recombines at the output 50 Ω resistor, which has to be able to withstand and dissipate significant power. Classic integrated resistors in polysilicon or in the substrate cannot withstand such large power levels, such that a special 50 Ω resistor design is realized. To avoid distracting the reader with in-detail design

considerations, a broader design overview is provided here, while thorough explanations are found in **Appendix G**. Then, the balanced PA results are detailed in **Section 5.3.4**.

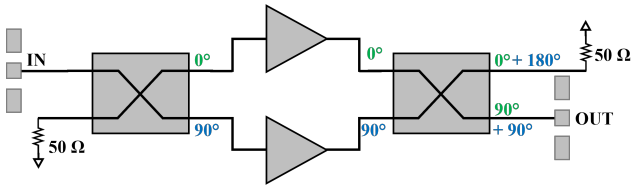


Figure 5.29: Schematic of a generic balanced power amplifier.

High power resistor

In case of load mismatch, a significant portion of the high power reflected at the load ends up dissipating in the 50 Ω resistor present in the output hybrid coupler. Thus, special care has to be taken when designing this resistor.

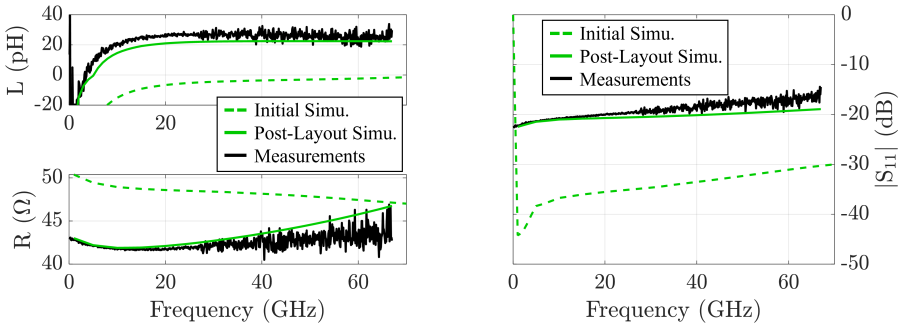
Assuming an ideal 90° hybrid coupler, the power dissipated in the 50 Ω resistor is

$$P_{50\,\Omega} = \frac{1}{2}|\Gamma_{\text{load}}|^2|\Gamma_{\text{amp}}|^2 P_{\text{amp}}, \tag{5.1}$$

where Γ_{load} is the reflection coefficient at the load, Γ_{amp} is the output reflection coefficient of the PA unit cell (assumed identical in both branches), and P_{amp} is the available power delivered by the PA unit cells. Considering the worst-case situation for a VSWR of 5 : 1 (Γ_{load} of -3.5 dB), a $\Gamma_{\text{amp}} = -1$ dB return loss at the PA unit (it corresponds to the worst $|S_{22}|$ measured value, which is very conservative, as the output should be matched in high power condition) and saturated power of 19 dBm, the maximum power dissipated in the resistor is 11.5 dBm. It corresponds to an rms current of 16.8 mA flowing through the 50 Ω resistor.

Due to the high current potentially flowing through the load, it has to be designed with metal lines that can better withstand electromigration. Thin and resistive metal layers in Cx with the widest allowable signal trace are used. They can support an rms current up to 10.5 mA. So, two parallel 100 Ω resistors are designed in Cx metal layers, such that the current flowing through each resistor is only half, reducing the electromigration stress on the metal lines. An adjusted post-layout simulation model is extracted thanks to separate characterization of a standalone structure. Results are shown in **Figure 5.30**. The achieved

reflection coefficient (cf. **Figure 5.30b**) remains around −20 dB from 20 to 50 GHz, well covering the PA operating bands.



(a) **(b)**

Figure 5.30: High power 50 Ω resistor measurements (black) and simulations (green). Equivalent R-L series circuit (a) and reflection coefficient (b). Initial design simulations in dashed lines. Adjusted post-layout simulations in solid lines.

Quadrature hybrid coupler

The configurable hybrid coupler design is based on a topology made of coupled transmission lines and described in **[191]**. This topology has proven to (i) be compact, (ii) have low insertion loss and good robustness to at least 3 : 1 VSWR conditions, (iii) have appropriate ports position for integration in a balanced amplifier topology, and (iv) tunable capacitors can easily be integrated **[191, 192]**.

1. Design

The hybrid coupler is represented by the simple lumped element schematic of **Figure 5.31**. In practice, however, the hybrid coupler is made of two pieces of coupled transmission lines connected together with an odd number of twisted elements, in order to have the ports in a convenient position to connect two PA cells in a balanced topology, see **Figure 5.32a**.

To cover all bands from 24 to 43 GHz, the hybrid coupler is made tunable with the addition of lumped switchable capacitors at each end (see **Figure 5.32a**). The switchable capacitor is designed by the series combination of lumped mom capacitors and two FETs in a switch configuration (as shown in **Figure 5.32b**), such that it switches between three states, each with distinct

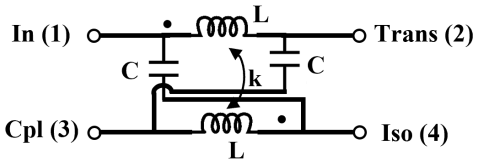


Figure 5.31: Equivalent lumped element schematic of the hybrid coupler.

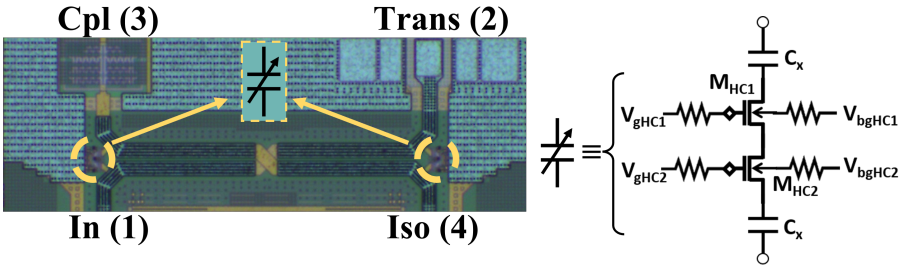


Figure 5.32: Configurable quadrature hybrid coupler description (a), schematic of tunable capacitor (b).

values of capacitors designed to work in one of the 24-29 GHz (FR2 n257 and n258), 30-33 GHz and 37-43 GHz (FR2 n259 and n260) bands.

The lowest capacitance value corresponds to the highest frequency of operation (39 GHz) and is achieved by turning both FETs off (State 1). Its value is therefore dominated by the C_{off} capacitance of the smallest FET (MHC2). For the other states, MHC2 is turned on and its on-resistance (R_{on}) induces losses in the overall hybrid coupler. For a given technology, the product $R_{on}C_{off}$, a switch FoM, is fixed. In 22FDX®, its value is around 98 fs **[193]**, but can be further reduced with specific interconnect design as it is shown in **Appendix G**. Therefore, to reduce losses caused by the smallest FET (with largest R_{on} and lowest C_{off}), the lowest capacitance value of the switchable capacitor is limited by the corresponding R_{on} from the smallest FET.

Furthermore, it has been previously shown that a simple series R_{on} or C_{off} model of SLVT FETs is not accurate at mm-wave frequencies **[194]**. Indeed, due to the thin buried oxide and the moderately conductive standard silicon substrate ($\sim 10\,\Omega$cm), shunt elements must be added to accurately predict

the behavior of a FET connected in switch configuration above a few tens of GHz. In [195], the authors propose to add a BFMOAT region around the FET to increase the shunt impedance and therefore reduce its impact at high frequency, while keeping the advantages of a back-gate bias access. In this work, a BFMOAT ring is similarly designed around each element of the switchable capacitor and, more importantly, between these elements and the nearby hybrid coupler ground. The substrate impedance connecting a common ground node of the switchable capacitor and a pin from the nearby hybrid coupler ground (it can visualized on the right side of Figure 5.33) is represented by a parallel R_{sub} and C_{sub}, which values are discussed in the following.

Design equations and an iterative procedure to design the hybrid coupler layout, the switchable capacitor and achieve optimized performance are provided in Appendix G. In this section, let us directly discuss the simulation results and measurements of a specially designed standalone structure.

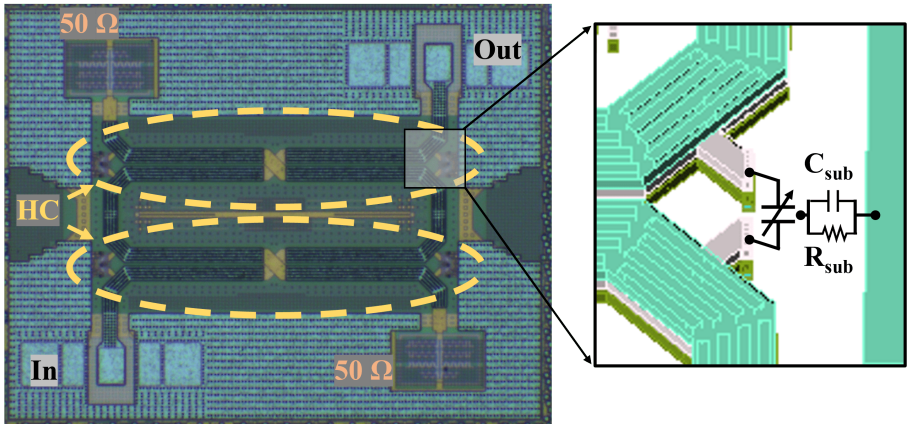


Figure 5.33: Fabricated structure for standalone hybrid coupler (HC) characterization, with representation of equivalent substrate impedance ($R_{sub} \parallel C_{sub}$) between a common ground node of the switchable capacitor and a pin from the nearby hybrid coupler ground. The standalone structure consists of two cascaded hybrid couplers, dc pads are not shown.

2. Results

The hybrid coupler is also designed as a standalone structure for proper characterization. To that end, two identical hybrid couplers are cascaded to end up with a 2-port structure (the two other ports are connected to two specially

designed 50 Ω high-power resistors described above) to replicate the hybrid coupler interconnects when integrated in the balanced PA structure. A picture of the structure is given in **Figure 5.33**.

The measurement reference plane is at the probe tips, so only an LRRM calibration is performed (with Infinity I67 probes) on the 101-190C calibration substrate without additional de-embedding. Measurements and simulations of the cascaded hybrid couplers are shown in **Figure 5.34**. Initial simulation of the hybrid coupler is shown in dashed lines, in which the substrate impedance is modeled by a large resistance ($R_{sub} = 10\,\text{k}\Omega$), thus with negligible shunt loss contributions. Adjusted EM simulations[14] are shown in dotted lines. Even with this adjustment in EM simulation setup (or with other EM stack corners), simulations do not closely fit measurements in all states.

Another parameter that was neglected (modeled by very large 10 kΩ cm resistance) at design time is the coupling between the switchable capacitor and the nearby ground from the hybrid coupler through the substrate. Here, we introduce an equivalent substrate impedance with parallel resistor and capacitor elements (R_{sub} and C_{sub}). By varying R_{sub} and C_{sub} values, we get a best agreement for $R_{sub} = 800\,\Omega$ and $C_{sub} = 6.6\,\text{fF}$, whose product is associated to an equivalent resistivity of the Si substrate of 5 Ω cm. These values yield what we shall use as *adjusted post-layout simulations* in the following.

Note that the initial to adjuted EM simulations have a $\sim 0.3\,\text{dB}$ of difference, and the addition of this non-negligible substrate impedance degrades the results by another $\sim 0.2\,\text{dB}$. Indeed, as soon as this substrate impedance is below a few kΩ, it has a strong impact on insertion loss: as seen by the dotted lines, mostly at the higher frequency bands when one or more FETs are in off-state. Although these degradations could partially be corrected by a re-design of the hybrid coupler, the substrate equivalent network impact could probably be neglected using a higher resistivity substrate.

The good agreement of post-layout simulations with measurements enables a confident extraction of the hybrid coupler characteristics via simulations as integrated in the balanced PA (the measured structure consists of two cascaded hybrid couplers). **Figure 5.35** shows the post-layout simulated $|S_{13}|$ and $|S_{23}|$ as well as the phase difference for the different states. A good phase quadrature is achieved in post-layout simulations as well as insertion loss (1.2, 1.2 and 1.3 dB at 27, 32 and 39 GHz, respectively) in all states.

[14] With the addition of an edge mesh at 200 nm in 2.5D Momentum simulations.

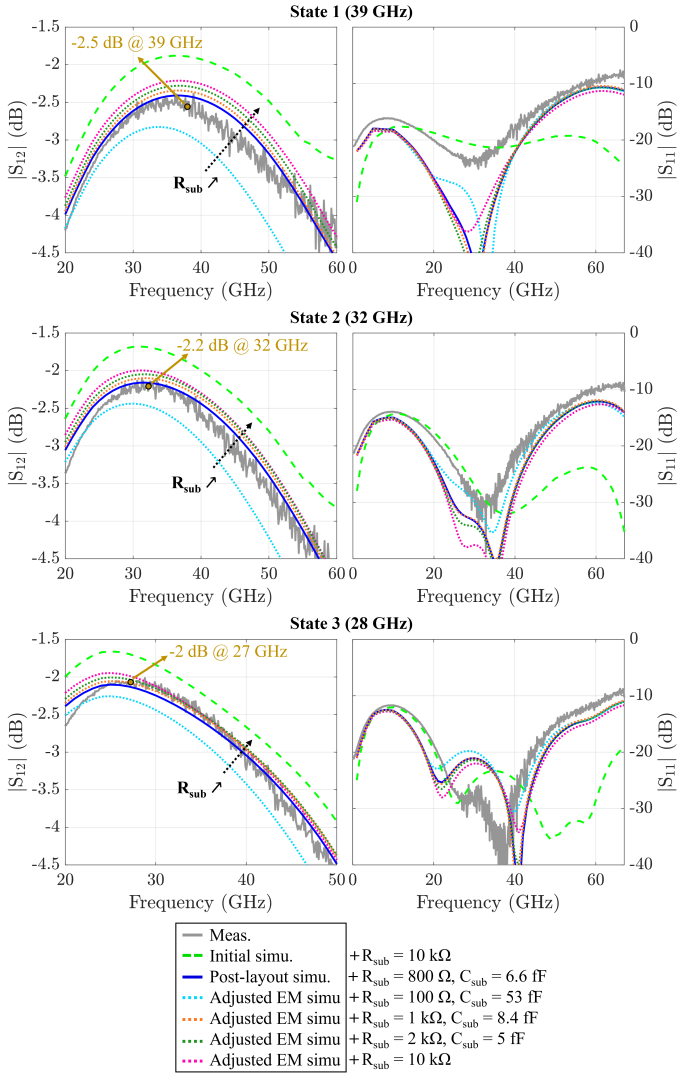


Figure 5.34: Measurements (grey) and simulations of the cascaded hybrid couplers in three different states, state 1 (a), state 2 (b), state 3 (c) and legend.

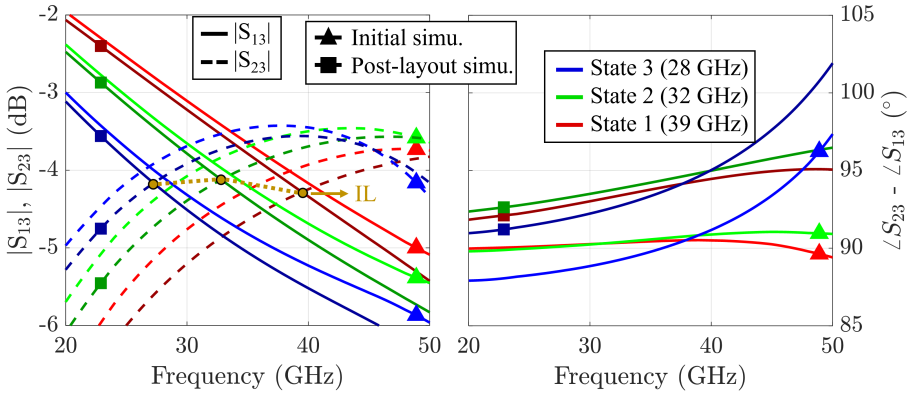


Figure 5.35: Simulations of the resulting hybrid coupler performance: S_{13} and S_{12} magnitude (left) and phase difference (right).

5.3.4 Configurable balanced PA (PA2): results

The fabricated PA2 is shown in **Figure 5.36**. The S-parameters are shown in **Figure 5.37**. Again, a good agreement between measurements and simulations is achieved (**Figure 5.37a**). From **Figure 5.37b**, we see the matching improving in each band when the appropriate state is used.

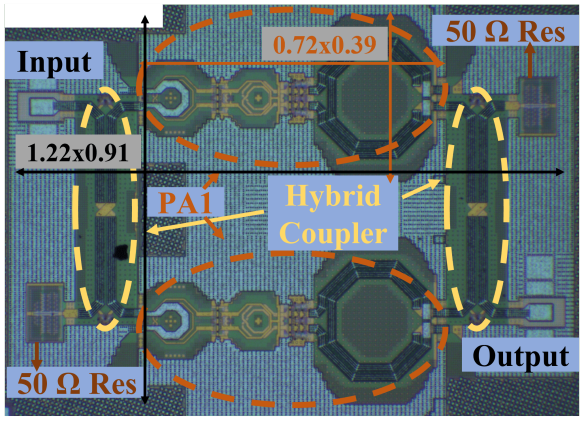


Figure 5.36: Fabricated configurable balanced power amplifier (PA2).

CW large-signal measurements are also conducted and shown in **Figure 5.38**, with P_{out} and PAE at P1dB and in peak conditions. P_{sat} goes as high as

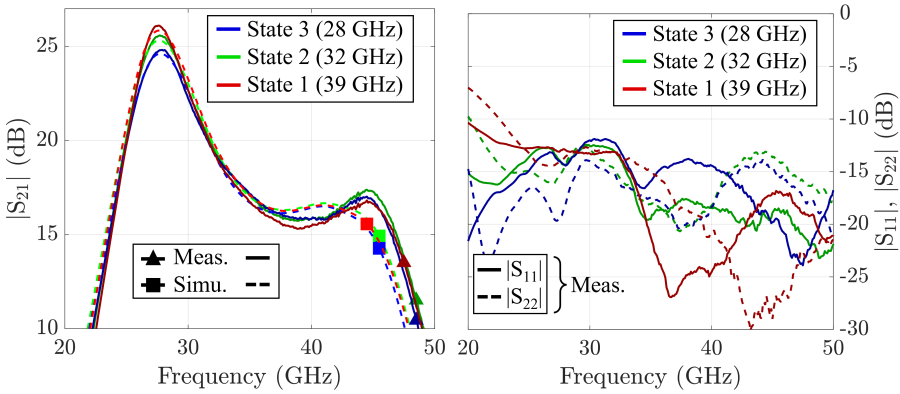


Figure 5.37: Measured and simulated S-parameters of PA2 in different states. (a) $|S_{21}|$, (b) $|S_{ii}|$.

20.1 dBm at 34 GHz, and the peak PAE reaches 28.3 % at 31 GHz. PA2 features up to 1.8 dB increased P_{out} than PA1, both in saturation and P1dB ($P_{out,1dB}$ = 16.5-19.6 dBm, associated PAE = 17.5 – 28.3 %), whereas the PAE is reduced by $\sim$ 9 %. The P_{out} improvement is limited below 30 GHz for the same reason as PA1 simulations are not fitting measurements below this frequency, because the driver stage saturates earlier than expected and dominates the PA's overall non-linear behavior. The low-frequency state is not shown in **Figure 5.38** for the same reason. In each band, the configurability (switching from state 1 to state 2 according to the frequency range) of the hybrid couplers gains up to 0.5 dB and 2 % in P_{out} and PAE, respectively, compared to the case where only a single state is available.

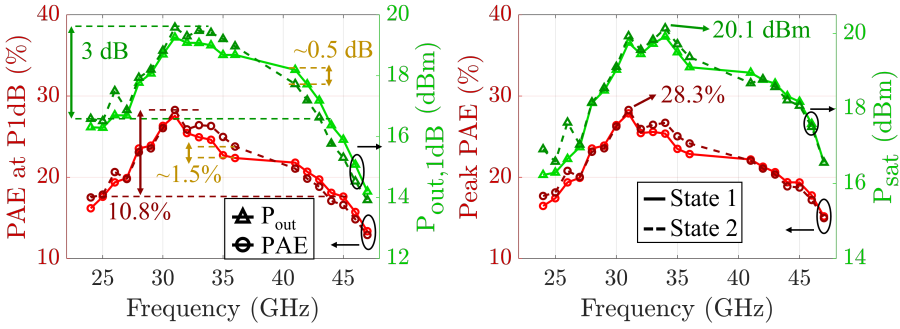


Figure 5.38: Measured PAE (left axis) and P_{out} (right axis) of PA2, at 1 dB compression point (a) and at peak PAE (b). Measurements of State 1 in light, solid lines, and State 2 in dark, dashed lines. Nominal bias.

5.4 Designed PAs with 5G Modulated Signals

This part will be covered via simulations and partially with measurements, as some modulated signal measurements are still missing at the time of writing this thesis (for PA2). Nevertheless, a high level of confidence in simulation results can be expected thanks to the excellent measurement-simulation agreement observed above and here again.

In this section, we first describe the measurement and simulation setups. Then, the 5G NR waveforms are briefly introduced. Finally, we show results for both designed PAs.

Setup

1. Simulations

Simulations are performed with the Vision software developed by AMCAD Engineering. It is a comprehensive modeling platform that enables system-level simulations. In practice, a behavioral model of the circuit is built in Vision using PDK simulation data obtained from the post-layout netlist (with simulation results shown above) in Cadence Virtuoso. In parallel, Matlab with its 5G toolbox is used to generate baseband signals and post-process the signal distorted from the PA. A schematic of the simulation flow is shown in **Figure 5.39**.

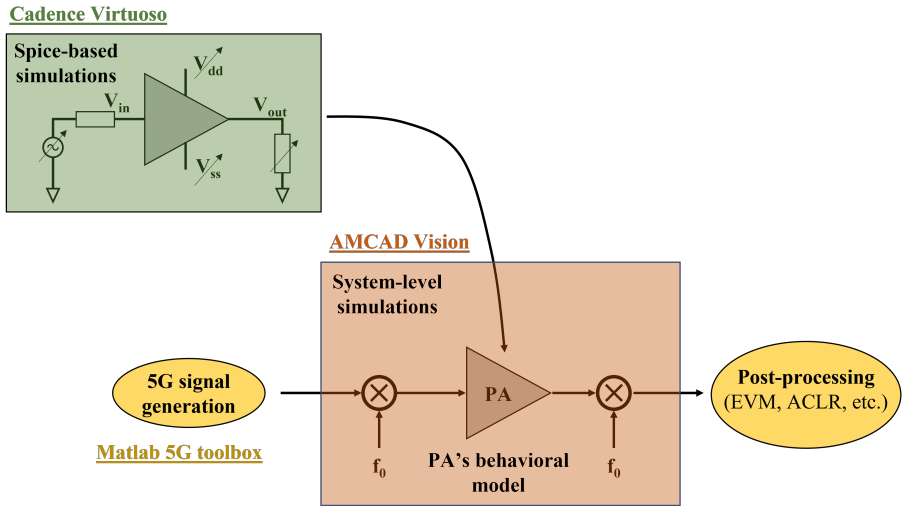


Figure 5.39: Flow for modulated signals simulation using different tools.

2. Measurements

A vector signal generator (VSG, SMW200A from Rohde & Schwarz) generates the modulated signal and is connected to the input of the tested PA via a cable and an RF probe. After the dut (PA), the distorted signal is read by a spectrum analyzer (SA, FSW 50 GHz from Rohde & Schwarz) that also demodulates the signal and computes the EVM[15]. The cables and RF probes at the input and output are calibrated based on their S-parameters with built-in tools both in the VSG and the SA.

5G modulated signal

1. Simulations

The choice of modulated signal has a strong impact on final performance, in particular its PAPR, in terms of output power and PAE. A realistic waveform for 5G applications in FR2 bands consists of 64-QAM OFDM with a 50 MHz bandwidth. The test model NR-FR2-TM3.1 waveform[16] with such specifications is available in the Matlab 5G toolbox and used in following modulated signal simulations. The PAPR of this waveform is of 12.9 dB. The complementary

[15] Information about the EVM definition, calculation, measurements and the required signal processing steps for its evaluation (via simulations or measurements) can be found in [196, 197].

[16] Fully specified in [198].

cumulative distribution function (CCDF) of the baseband signal, as well as the voltage magnitude of the time signal are shown in **Figure 5.40**.

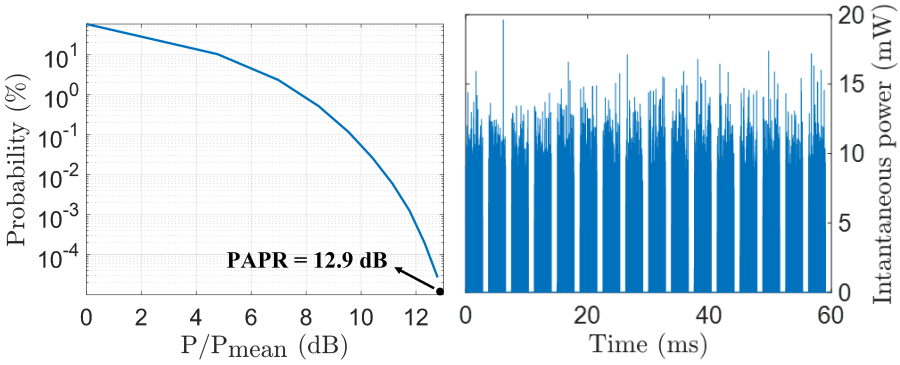


Figure 5.40: CCDF (a) and instantaneous power (b) of baseband NR-FR2-TM3.1 waveform used in the EVM simulations.

The pertinence of this particular waveform for benchmarking is disputable, in particular with respect to the bandwidth and PAPR. Indeed, bandwidths as large as 400-800 MHz are used and typical PAPR values encountered are 9-10 dB for 64-QAM 5G (OFDM) signals. The reason for such larger PAPR in our test signal probably comes from zero-valued transmitted symbols (observed in **Figure 5.40b**) used for synchronization in real applications that are likely not present in modulated signal measurements performed in the literature.

2. Measurements

5G NR default signals available in the SMW200A VSG from Rohde & Schwarz are used. They consist of TDD FR2 uplink signals with 64-QAM digital modulation and bandwidths ranging from 100 to 800 MHz (with a subcarrier spacing from 120 kHz to 240 kHz for the largest bandwidth). The CCDF of the test signals is shown in **Figure 5.41**. The differences between the test signals used for measurements and simulations are the larger bandwidths in measurements and a $\sim$ 1 dB difference in the CCDF. Nevertheless these two effects affect the PA performance in opposite trends, such that the simulations of the tested PA agree well with measurements for the 100 MHz bandwidth signal as we will see in the following.

Here again, the input signal used for measurements features a large PAPR

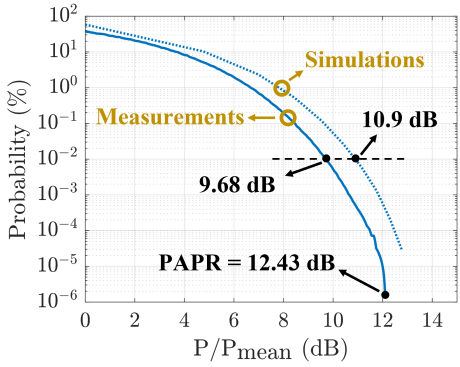


Figure 5.41: CCDF of baseband 5G NR test signals used for measurements (solid line) and simulations (dotted line).

(of 12.4 dB), which is still several dB above the signals reported in the literature. Operating with a larger PAPR implies that the PA needs to work even more in backoff power (with $2-3$ dB more) to achieve the same EVM. In other terms, for the same EVM target, this waveform (instead of the ones with lower PAPR used in the literature) will result in lower PA efficiency and output power, thus underestimating its performance when compared to other publications. Using a user-defined signal with closer specifications to what is used in the literature is out of the scope of this thesis. Furthermore, our test signals are representative enough to study how the back-gate bias affects the PA under modulated signal conditions.

Wideband PA1 performance - simulations

In the following, we analyze the PAs performance excited with a 5G modulated signal for a carrier frequency of 32 GHz, as it featured close to largest peak PAE and P_{sat} measurements in CW, together with an excellent measurement-simulation agreement.

Simulated rms EVM, average PAE and P_{out} are shown for PA1 at different power levels and V_{bg} biases[17] in **Figure 5.42**. By increasing V_{bg}, the gain increases and the curves are shifted to higher power values (identical input power points for both V_{bg} biases are shown in **Figure 5.42a**). The mean PAE

[17]The back-gate biases of all PA's transistors are changed together in this section. Separate back-gate biasing of individual transistors has been tested via simulations and experimentally, but it has not resulted in improved performance. So, it will not be shown in the following.

increases slightly faster for $V_{bg} = 0\,\text{V}$ as the PAE is known to be larger in backoff power in class B than class A operation. The increase in EVM with larger power is due to both AM-AM and AM-PM distortions [189]. As we have seen in **Section 5.3.2**, by varying V_{bg}, one can trade-off one type of distortion for the other.

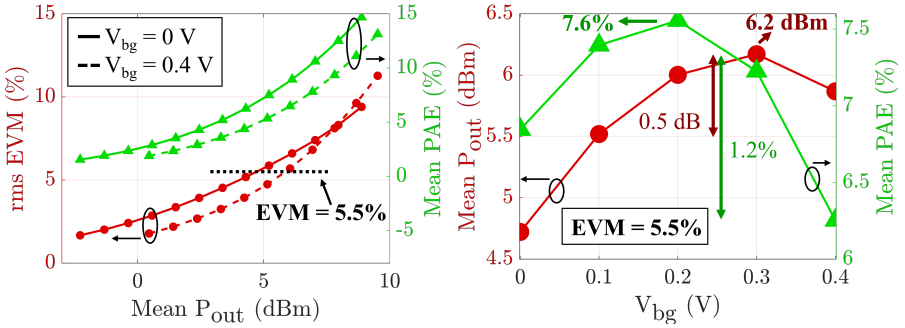


Figure 5.42: 5G NR-FR2-TM3.1 test model signal *simulations*, with a 50 MHz bandwidth baseband signal and a carrier of 32 GHz. Left (a): PA1 simulated rms EVM, average PAE and P_{out} for $V_{bg} = 0\,\text{V}$ (solid lines) $V_{bg} = 0.4\,\text{V}$, for different input power levels. Right (b): PA1 simulated average PAE and P_{out} versus V_{bg} for a target $\text{EVM}_{\text{rms}} = 5.5\,\%$.

For a fixed target of 5.5 % rms EVM[18], which is the EVM requirement for low bit error rate in 5G signals [4], the corresponding mean output power and PAE for different back-gate biases are shown in **Figure 5.42b**. For this target rms EVM, the ACLR remains below $-31.4\,\text{dB}$ for all simulated V_{bg} biases, which also fulfills the ACLR requirements of $-30\,\text{dB}$ to $-25\,\text{dB}$ [4].

A peak in overall PA performance -with mean P_{out} and PAE as high as $\sim 6.2\,\text{dBm}$ and 7.6 % for a target EVM of 5.5 %- can be achieved by fine tuning the back-gate bias (optimal for $V_{bg} \approx 0.25\,\text{V}$). Furthermore, the PA performance is rather sensitive around this bias: a $\pm 0.15\,\text{V}$ variation in V_{bg} (corresponding to an overdrive voltage variation of $\pm 12\,\text{mV}$) induces a reduction of 0.5 dB and 1.2 % in mean P_{out} and PAE performance.

[18] An EVM of 5.5 % is equal to $-25.2\,\text{dB}$, which is the unit used in **Table 5.2**.

Wideband PA1 performance - measurements

The EVM behavior with back-gate bias is also analyzed experimentally with *measurements*. The results are shown in **Figure 5.43**. The nominal V_{bg} bias $V_{bg,0}$ is the back-gate bias necessary to yield the same designed bias current values of 6.8 mA and 13.5 mA for the driver and output stages, respectively, which corresponds to $V_{bg} = 0$ V in simulations.

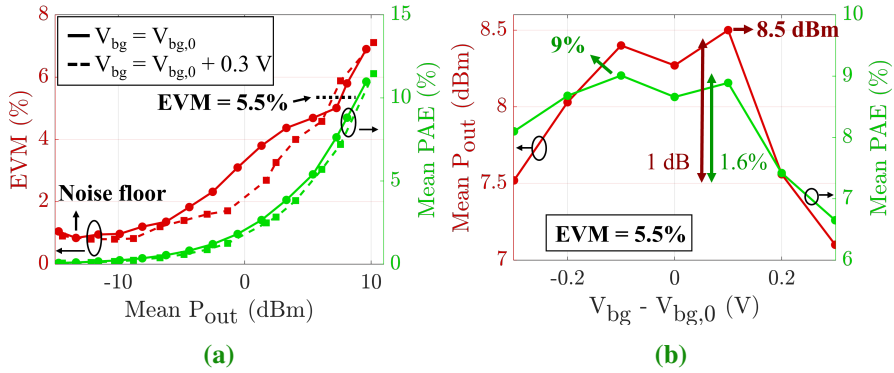


Figure 5.43: 5G NR modulated signal *measurements*, with a 100 MHz bandwidth baseband signal and a carrier of 40 GHz. Left (a): PA1 measured rms EVM, average PAE and P_{out} for $V_{bg} = V_{bg,0}$ (solid lines) $V_{bg} = V_{bg,0} + 0.3$ V (dashed lines), for different input power levels. Right (b): PA1 measured average PAE and P_{out} versus V_{bg} for a target $\text{EVM}_{\text{rms}} = 5.5\,\%$.

In **Figure 5.43a**, at low EVM values, the measurements are dominated by the noise floor of the whole measurement setup ($\sim 1\,\%$). Furthermore, the two EVM-P_{out} curves meet each other at a lower EVM value than what is predicted in simulations. Despite these small differences, approximately the same trends as in simulations (cf. **Figure 5.42a**) are observed.

Similarly for **Figure 5.43b**, measurements and simulations feature comparable behaviors, which was already explained above in terms of the circuit operation. An optimum is found around $V_{bg} = V_{bg,0}$, which is different from what is expected from simulations ($V_{bg} \approx V_{bg,0} + 0.25$ V) This represents a significant shift that can likely be explained by the different modulated signal used in simulations. Indeed, as we will see below, the optimal bias for a target EVM value depends on the modulated signal bandwidth and carrier frequency.

The ACLR is also measured in peak conditions (for $V_{bg} = V_{bg,0}$ and an EVM of 5.5 %) and is shown in **Figure 5.44**. A worst-case value of -24.9 dBc

is measured, which fulfills the 5G requirements.

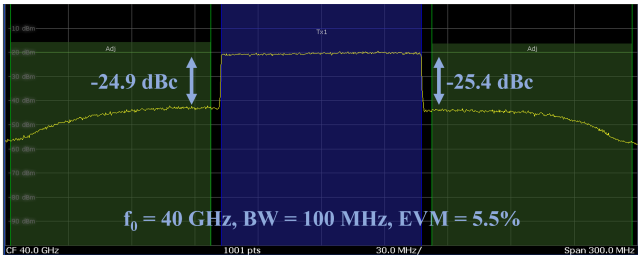


Figure 5.44: Output spectrum and ACLR measurements from PA1 with a 100 MHz bandwidth baseband signal, a carrier of 40 GHz, at the nominal bias of $V_{bg} = V_{bg,0}$ and for an EVM of 5.5 %. The corresponding mean output power and PAE are 8.3 dBm and 8.7 %, respectively.

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The optimal bias condition ($V_{bg} = V_{bg,0}$) is used for measurements at other carrier frequencies and with different signal bandwidths. Measured mean P_{out} and PAE are reported in **Figure 5.45** for a target EVM of 5.5 %. In **Figure 5.45a**, we observe that PA1 has peak performance around 27 and 41 GHz, with average P_{out} and PAE of 9.2 dBm, 13 %, and 8.3 dBm, 9.2 %, respectively. PA1's performance is degraded with larger signal bandwidths as shown in **Figure 5.45b** mostly between 100 and 200 MHz, as the PA needs to work in higher backoff power due to additional linearity constraints. The PA still features mean P_{out} and PAE of 6.8 dBm, 8.3 % at 28 GHz, and 4.8 dBm, 5.2 % at 43 GHz, respectively, for a signal bandwidth of 800 MHz.

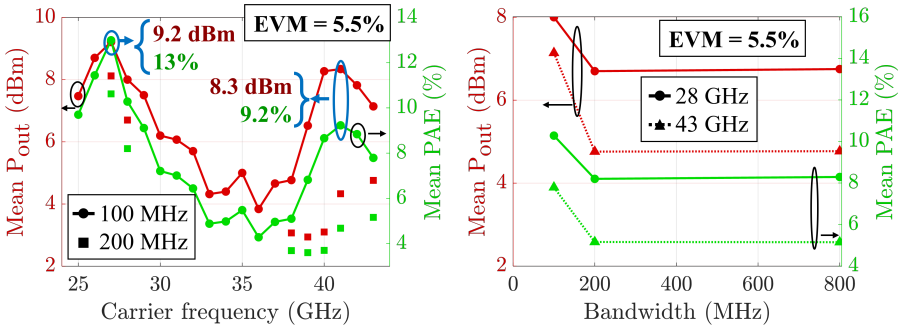


Figure 5.45: 5G NR modulated signal *measurements*, with various bandwidths and different carrier frequencies. PA1 measurements at $V_{bg} = V_{bg,0}$ at the EVM target of 5.5 %. Left (a): PA1 measured average PAE and P_{out} versus carrier frequency and signal bandwidth of 100 MHz (circles) and 200 MHz (squares). Right (b): PA1 measured average PAE and P_{out} versus bandwidth for different carrier frequencies: 28 GHz (circles) and 43 GHz (triangles).

Note that the optimal bias condition of $V_{bg} = V_{bg,0}$ is found above (**Figure 5.43b**) by optimizing the PA's performance for a given signal bandwidth (100 MHz) and at a given carrier frequency (40 GHz). However, it might not be the optimal bias for a different modulated signal. To test it, the optimal bias is searched by varying the back-gate biases for two different modulated signals, in which we change either the signal bandwidth (800 MHz at 40 GHz) or the carrier frequency (100 MHz at 32 GHz). **Figure 5.46** shows the mean P_{out} and PAE for different back-gate biases for these two new cases.

As shown in **Figure 5.46a**, the optimum bias for a signal of 100 MHz

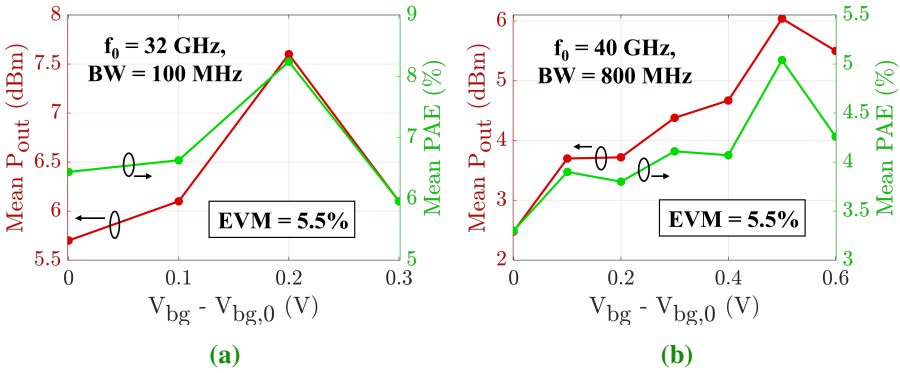


Figure 5.46: 5G NR modulated signal *measurements* of PA1, average PAE and P_{out} at a target $\text{EVM}_{\text{rms}} = 5.5\,\%$, for different V_{bg}. Left (a): 5G NR modulated signal with a 100 MHz bandwidth at a carrier of 32 GHz. Right (b): 5G NR modulated signal with a 800 MHz bandwidth at a carrier of 40 GHz.

bandwidth at 32 GHz is closer to the optimum found in simulations (with a 50 MHz of bandwidth at 32 GHz). Moreover, the measured peak performance of 7.6 dBm and 8.3 % are comparable to the optimum in simulations of 6.2 dBm and 7.2 % for mean ouput power and PAE, respectively (the differences can be explained by the $\sim$ 1 dB-lower PAPR in the measured test signal). Overall, these results further demonstrate the excellent agreement between measurements and simulations, which indicates that the simulated model can be used to predict quantitative results.

Furthermore, the optimal back-gate bias from **Figure 5.46b** ($V_{bg} = V_{bg,0} + 0.5\,\text{V}$) is far from the optimum found for a signal bandwidth of 100 MHz at the same carrier frequency. It therefore shows that the signal bandwidth can greatly influence the PA biasing point that exhibits the best performance. The PA's performance (mean P_{out} and PAE) for a target EVM of 5.5 % at different carrier frequencies is shown in **Figure 5.47** for two biases: $V_{bg} = V_{bg,0}$ and $V_{bg} = V_{bg,0} + 0.5\,\text{V}$. Around $39 - 40\,\text{GHz}$, the improvement with the new bias is great in both output power and efficiency. At the other carrier frequencies, the output power is significantly increased but at the cost of a reduced efficiency.

So, the optimal bias yielding largest output power and efficiency (for a target EVM) depends on both the signal bandwidth and carrier frequency. The back-gate terminal -a unique feature for UTBB FD-SOI devices- is a great tuning knob enabling to fine tune the bias in a straightforward way. It could

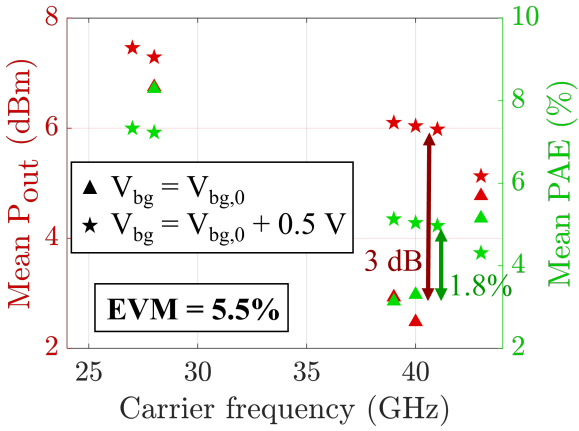


Figure 5.47: 5G NR 800 MHz-bandwidth modulated signal *measurements* of PA1 for two biases: $V_{bg} = V_{bg,0}$ (triangles) and $V_{bg} = V_{bg,0} + 0.5\,\text{V}$ (stars), at the EVM target of 5.5 %. Average PAE and P_{out} versus carrier frequency. PA1 measured average PAE and P_{out} versus carrier frequency and signal bandwidth of 100 MHz (circles) and 200 MHz (squares).

therefore easily be implemented in a front-end module to achieve optimal PA performance either by pre-characterizing the PA with the test signal, or in an adaptive way with an additional feedback loop to form a closed-loop controlled system.

Configurable balanced PA2 performance

The same simulations are run for the configurable balanced PA, PA2, in state 2, optimized for 32 GHz operation. Similarly, the back-gate bias can be tuned to find the best compromise between AM-AM and AM-PM distortion and maximize the mean output power and PAE for a target EVM of 5.5 % **[189]**. The results are shown in **Figure 5.48a**.

We observe that the mean output power is increased with this configuration (up to 9.8 dBm, instead of 6.2 dBm for PA1), as it could be expected, and that a similar mean PAE is achieved (up to 6.9 %, instead of 7.6 % for PA1). This can be understood by looking at the PAE $-$ P_{out} CW measurements in **Figure 5.48b**. We observe that for a similar amount of backoff power from the 1 dB compression point (yellow dots), similar PAE is achieved for both PAs, while PA2 exhibits larger output power.

5G modulated signal measurements of PA2 are unfortunately not available

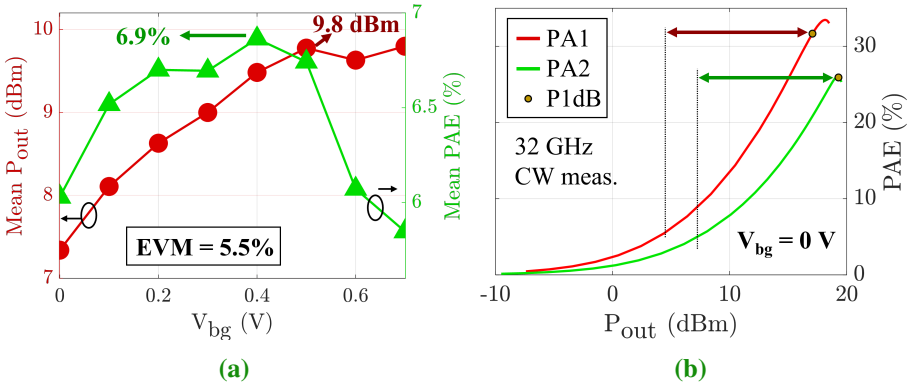


Figure 5.48: Left (a): PA2 simulated average PAE and P_{out} versus V_{bg} for a target $\mathrm{EVM_{rms}} = 5.5\,\%$. Right (b): 32 GHz CW measurements of PAE versus P_{out} of PA1 (red) and PA2 (green). 1 dB compression point indicated in yellow dot.

at the time of writing this thesis.

5.5 Benchmarking to State of the Art

Table 5.2 presents state-of-the-art PAs in CMOS technologies in 24 to 43 GHz bands. The presented PAs feature P1dB P_{out} and PAE in line with the state of the art of narrowband PAs over a broad frequency range. It even outperforms other wideband PAs in FD-SOI technology. Although measurements with modulated signals are still missing for PA2, measurements of PA1 and simulations of PA2 indicate that they are well suited to 5G modulations and perform well compared to the state of the art, taking into account that the test signal features a larger PAPR of $2-3\,$dB. Although not as efficient as 45 nm PD-SOI PAs, the proposed FD-SOI-based PAs can benefit from (i) tuning provided by the back-gate access as demonstrated with AM-AM and AM-PM distortions, and (ii) high logic density from advanced CMOS nodes to integrate more functions in a single low-cost chip.

Having been able to design two PAs at the state of the art, the discussion on the impact of substrate resistivity increase at circuit level covered in the next chapter becomes of particular interest.

Table 5.2: Summary of state-of-the-art CMOS-SOI-based PA performance in continuous-wave (CW) mode and with 64-QAM on a single-carrier (SC) or on OFDM (5G NR).

	This work		ISCAS'22	ISSCC'20	JSSC'19	CICC'20	TMTT'21	EuMC'22	ICECS'22	LCCS'21
	PA1	PA2	[199]	[200]	[187]	[201]	[202]	[203]	[204]	[205]
Technology	22 nm FD-SOI			45 nm PD-SOI		22 nm FD-SOI			28 nm FD-SOI	
Architecture	Distributed balun	Configurable balanced	RC feedback 1-stage diff.	Distributed balun	Mixed-signal Doherty	Current combining	Doherty	2-stacked diff.	2-stacked diff.	Adaptive bias control
Supply (V)	2.4		1.8	2	2	2.4	2.4	1.6	2	2
Frequency (GHz)	24-43		19.1-46.5	24-42	27	28	28	28	26	28
Gain (dB)	17.4-27.7	15.3-26.1	13.4-16.4	17.5-20*	19.1	27	26.1	23.5	24	13.8
P_{sat} (dBm)	16.6-18.6	16.6-20.1	12.9-14.6	17.9-20.4	23.3	21.7	22.5	21	19	17.8
PAE_{max} (%)	27.2-36.4	17.7-28.3	15.2-26.1	35-45	40.1	27.1	28.5	31.5	43	37.8
$P_{out,1dB}$ (dBm)	16.2-18.1	16.5-19.6	9.2-11.5	15.7-19.6	22.4	19.1	21.1	19.2*	N/A	17.4
Modulation	64-QAM 5G NR 100 MHz	64-QAM 5G NR 50 MHz	256-QAM 5G NR 400 MHz	64-QAM 5G NR 400 MHz	64-QAM SC N/A	64-QAM SC N/A	64-QAM SC N/A	64-QAM OFDM 100 MHz	64-QAM 5G NR N/A	64-QAM SC 600 MHz
PAPR (dB)	12.43		8	9.64	6.5	6.4	N/A	N/A	9.9	8.65
Data rate (Gb/s)	N/A		N/A	N/A	6	3	2.4	N/A	3	3.6
EVM_{rms} (dB)	-25.2		N/A	-25.4	-25.3	-25	-25.1	-28	-21.4	-25.1
P_{mean} (dBm)	3.8-9.2	9.8**	6.2-7.1	13.8	15.9	12.9	10.9	12.5	8.9	9.4
PAE_{mean} (%)	4.3-13	6.9**	5.3-7.7	23.3	29.1	9	9.2	6.7	15	12.8

*: Estimated from graph. **: Simulated values.

5.6 Conclusion

In this chapter, the design of two fundamental circuits in an RF front-end module are discussed: the low-noise amplifier and power amplifier.

A first brief introduction to mm-wave front-end module architecture is provided, and the LNA and PA key figures of merit are introduced, including typical target values for mm-wave circuit design. Then, the designed circuits are presented.

The designed 39 GHz LNA achieves 2.5 dB NF with 19.9 dB gain and -5.3 dBm IIP3 for a 20.8 mW power consumption in the 22 nm FD-SOI technology. We observe that the back-gate bias can be used to tune the operation point and trade-off power for noise and gain, achieving a 2.8 times reduction in P_{dc} for $+1$ dB and -5 dB variations in NF and gain, respectively.

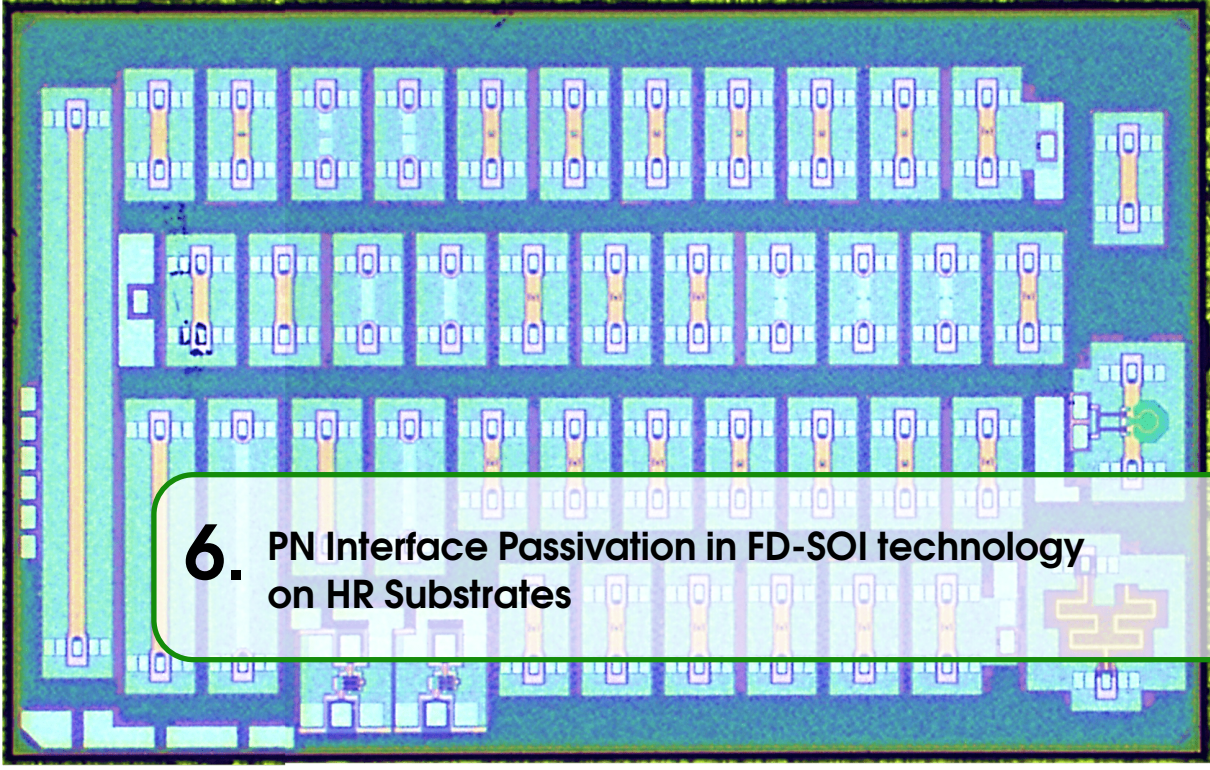
Then, two PAs covering the 24-43 GHz frequency bands in 22 nm FD-SOI technology are presented in detail, the first one (PA1) implements a distributed balun at the output, the second one (PA2) consists of a balanced topology using two PA1 cells connected with configurable hybrid couplers. They achieve a saturated output power and peak PAE up to 18.6 dBm and 36.4 % for PA1, and 20.1 dBm and 28.3 % for PA2, respectively. Simulations and measurements of 5G NR modulated signals (with PAPR $>$ 12 dB) applied to both PAs are realized. Back-gate bias modulation enables to trade-off AM-AM for AM-PM distortion by a fine control of the operating class, and it is used to optimize the average output power and PAE (up to 9.2 dBm and 13 % for PA1 at 27 GHz; and 9.8 dBm and 6.9 % for PA2 at 32 GHz[19]) for an rms EVM target of -25.2 dB ($=$ 5.5 %). To the best of our knowledge, the impact of back-gate bias modulation on the EVM figure of merit was shown for the first time here.

The designed circuits achieve state-of-the-art performance among (SOI) CMOS technology. The designed LNA is in line with the LNA performance requirements for 5G handset applications ($\sim$ 3 dB NF and $>$ 20 dB gain). From the PA benchmarking at **Table 5.2**, one can see that PD-SOI technology demonstrated sufficient average power ($\sim 11-15$ dBm) and efficiency ($\sim$ 20 %) for a successful integration in front-end modules for 5G applications. PAs in FD-SOI technologies are currently still lacking a bit of power and have lower efficiency, but a strong effort is currently in progress in this research area to fill this gap, which might yet be overcome.

One way to potentially improve FD-SOI-based circuits is to replace the

[19] Only 5G modulated signal simulations are available for PA2 at the time of writing this thesis.

standard resistivity substrate by another substrate of higher resistivity. Indeed, we have seen in this chapter that crucial passive elements in these circuits (input spiral inductor for LNA, output balun and hybrid coupler for PAs) are not shielded from the substrate, thus potentially sensitive to substrate losses that can be significant with standard resistivity substrate. Thanks to the excellent agreement between measurements and simulations achieved for all circuits, we investigate in the next chapter via simulations the quantitative performance improvements that might be achieved with the use of a low-loss high-resistivity silicon substrate for each designed circuit.



6. PN Interface Passivation in FD-SOI technology on HR Substrates

The substrate in integrated circuits is more than just a mechanical support. Indeed, as already stressed in **Chapter 1**, at high frequencies, the thin dielectric layers isolating the metal interconnects and transistors from the substrate have a low impedance by their capacitive nature, resulting in a significant portion of the electric field propagating into the substrate, inducing losses, non-linearity and increasing the complexity of parasitic coupling modeling.

Standard resistivity ($\sim 10\,\Omega\,\mathrm{cm}$) substrate entails significant RF losses, non-linearity, inter-device coupling and limited quality factor of passives (spiral inductors, CPW lines, etc.) **[3]**. Moving to high-resistivity substrates ($> 3\,\mathrm{k}\Omega\,\mathrm{cm}$) already reduces such detrimental effects, but the enhancement is hindered by the parasitic surface conduction (PSC) effect. The trap-rich solution, which consists of a layer rich of traps close to the Si-SiO_2 interface, successfully counters the PSC effect and features excellent RF quality, i.e. highly linear and very low-loss substrate. Its application to PD-SOI technology is well known and has contributed to the commercial success of this technology. However, its integration in an FD-SOI technology process is not straightforward, as the defect-rich poly-silicon layer degrades the isolation of the back-gate contact of UTBB devices in the substrate's PN junctions, therefore increasing the reverse diode current.

Other more recent techniques **[17–19]** dealing with the PSC effect have been proposed, which seem to be more easily compatible with the FD-SOI

process. The *PN junctions interface passivation solution* [19] in particular has the highest maturity level [19, 25, 26, 28, 206–208] among the above solutions. Indeed, thanks to the simple fabrication steps required by the technique that are already present in a UTBB FD-SOI process, this PN junction solution has already been successfully applied in the 22 nm FD-SOI technology [25, 26, 28].

This chapter presents the results of the PN junction technique applied in GlobalFoundries' 22FDX® technology to passive devices. We first briefly describe the PN junctions technique. Then, we show that a strong reduction in substrate loss, coupling and harmonic distortion is achieved with high-resistivity substrates and the smart PN pattern solution, leading to passives of high quality factor, such as transmission lines (TLs) and spiral inductors. Finally, after demonstrating that high quality resistive substrates can be obtained in industrial FD-SOI technology, we analyze the potential improvements of the designed circuits from Chapter 5 with a low-loss substrate.

6.1 Introduction to the Smart PN Pattern Technique

The concept of PN junctions solution starts from the problematic parasitic surface conduction effect, which consists of a thin conductive sheet formed close to the Si-BOX interface (cf. Figure 3.1). The proposed technique consists of patterning a series of alternating N+ and P+ regions under the BOX, i.e. at the interface where the PSC effect takes place, see Figure 6.1a. By doing so, the conductive layer is interrupted by highly resistive regions corresponding to the depleted region of each PN junction, as illustrated by the horizontal resistivity profile below the BOX shown in Figure 6.1b.

With this technique, the overall impedance sensed by the electric fields of an overlying structure is greatly increased, thus reducing substrate losses and coupling. To describe the overall small-signal performance of the substrate, we use the figure of merit of effective resistivity described in Chapter 3, with its definition from Equation 3.4 that does not include dielectric loss mechanism in the total substrate losses[1]. There are a few important characteristics of the PN junctions solution to highlight.

- This solution increases the substrate impedance close to the interface, not in the substrate depth. So, to achieve a high quality RF substrate, it is important to apply this technique to a high-resistivity substrate (that can

[1] Indeed, we demonstrated in Chapter 3 that conductive losses are the dominant loss mechanism in Si substrates in the frequency range of interest.

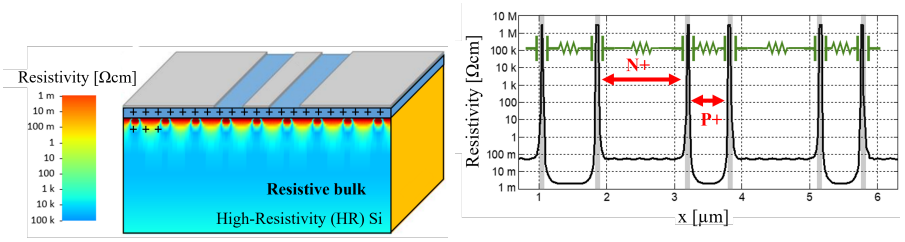


Figure 6.1: Left (a): representation of the 2D resistivity profile in a HR substrate enhanced with buried PN depletion junctions. Right (b): local resistivity in the HR substrate with the PN junctions solution directly beneath the BOX. From **[19]**.

suffer from PSC effect).

- The increase in substrate impedance (and effective resistivity) is directional (in the cross-section direction shown in **Figure 6.1a**. So, a co-design between the pattern of PN implants and the RF device should be performed simultaneously during layout.
- This technique uses P+ and N+ doping implants close to the interface that are already part of the fabrication process in a variety of CMOS technologies (SOI and bulk).
- By construction, the surface substrate impedance (and overall substrate impedance sensed by the overlying circuitry) decreases with frequency. Indeed, the series of highly conductive regions (P+ and N+) separated by highly resistive (depletion) regions can be seen as a series combination of resistance and capacitance elements (illustrated in **Figure 6.1b**). This capacitive coupling through the depletion regions induces an impedance value that is decreasing with frequency. Therefore, frequency-decreasing effective resistivity is expected for these substrates using the PN junctions solution.
- The effectiveness of the PN junctions technique is enhanced with a larger density of depleted junctions. This can be accomplished with (i) a high resolution lithography to increase the density of PN junctions, (ii) intrinsic region between the P- and N-doped regions, (iii) reverse biasing the PN diodes. These enhancements are further discussed in the following.

6.2 High Quality RF Substrate in an Industrial FD-SOI Technology

The above *PN interface passivation* solution is applied within the industrial GlobalFoundries' 22FDX® line run on standard and HR SOI wafers provided by Soitec. In this section, we analyze in detail the effect of different PN passivation patterns, designed and fabricated in the same run, on several passive structures. After describing the fabricated passives and PN patterns, we evaluate the substrate RF performance and the PN interface passivation solution on the electrical behavior of several passives: (i) coplanar waveguide (CPW) lines, in terms of substrate losses and non-linearity, (ii) quality factor of spiral inductors, (iii) crosstalk through the substrate between adjacent pads. The results presented here have already been partially published in **[25–27]** and mainly in **[28]**.

6.2.1 Fabricated structures

Several passives and PN passivation patterns are designed. Each passive is replicated several times to include different PN passivation patterns, and are fabricated in the industrial GlobalFoundries' 22FDX® line run on 4 wafers of different resistivities: two wafers around 10 Ω cm (std1 and std2) -the process of record (POR) corresponding to std1- 620 Ω cm (HR1) and 985 Ω cm (HR2). All the wafers include a BOX and are thus subject to PSC, even though it is only a strong problem for high-resistivity substrates for which the improvements brought by a highly-resistive bulk are hindered.

Passive structures

The first set of CPW lines is designed in the last copper layer 'QB' (3 µm thick and approximately 10 µm away from the Si substrate) and has a signal line width w of 35 µm, and a signal to ground spacing s of 25 µm (**Figure 6.2a**). The second set of CPW lines is formed in stacked M1 and M2 (combined thickness of ~ 0.17 µm, and approximately 130 nm from the Si substrate) using $w = 20$ µm and $s = 20$ µm (**Figure 6.2b**). Additionally, a set of thin film microstrip lines (TFMS) is designed with the signal line width of 10 µm implemented in QB, ground plane in the 5 thin bottommost metal layers stacked for a combined thickness of ~ 400 nm at a distance of approximately 9 µm below the signal line (**Figure 6.2c**). The CPW and TFMS lines dimensions are selected to have a 50 Ω characteristic impedance (Z_c) for a meaningful performance comparison. Lines of multiple lengths (760 µm and 2000 µm) are fabricated, along with dedicated Open and Thru structures, to enable a wideband multiline Thru-Reflect-Line (mTRL) calibration and extraction of the line's equivalent *RLGC* parameters,

as explained in **Chapter 3**.

Two inductors are also designed, targeting different operating frequencies : $5-20\,\text{GHz}$ (called 'RF inductor') and $30-60\,\text{GHz}$ (called 'MMW inductor'). These inductors are designed on the QB layer. A sketch of the inductors and their geometrical dimensions are presented in **Figure 6.2d** and **Figure 6.2e**. The dummy fills are minimized to avoid degrading the inductors quality factor.

A crosstalk structure is designed as two pads, stacking the bottommost 8 metal layers (M1 to JA), facing each other with a width of $20\,\mu\text{m}$, length of $100\,\mu\text{m}$ and spacing of $30\,\mu\text{m}$ as reported in **Figure 6.2f**.

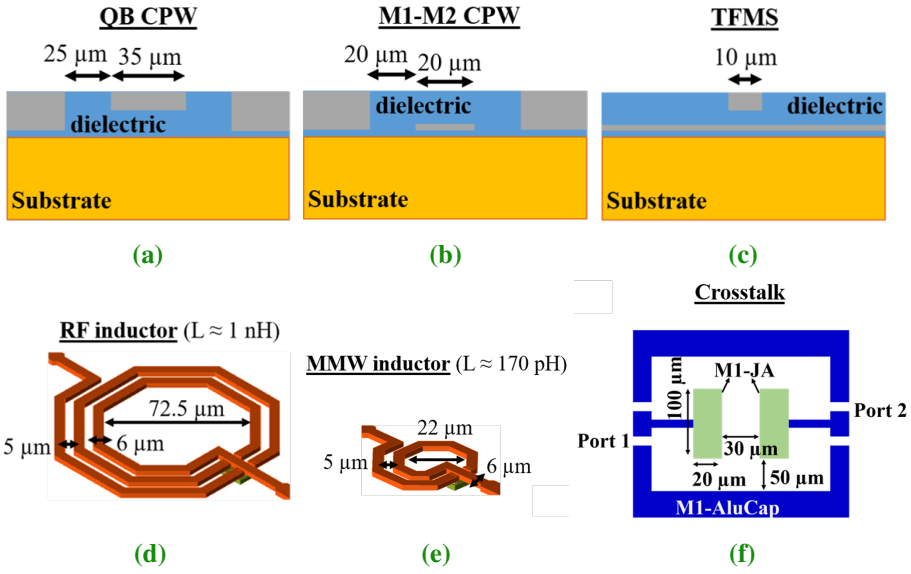
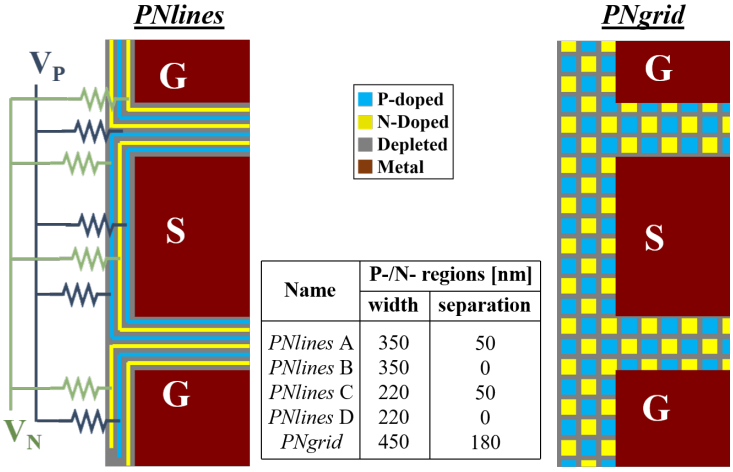


Figure 6.2: Sketches along with main dimensions of all passive structures fabricated and characterized in this section: (a), QB CPW, (b) M1-M2 CPW, (c) TFMS, (d) RF inductor, (e) MMW inductor, (f) Crosstalk structure.

PN interface passivation patterns

Two types of PN passivation patterns are designed and presented here: (i) *PNlines* and (ii) *PNgrid*. They are both represented in **Figure 6.3**, and serve to increase the impedance between two terminals through the substrate (for instance the 'S' and 'G' lines of the CPW illustrated in **Figure 6.3**). The *PNlines* pattern includes a dc biasing option through on-chip high-valued resistor elements. This allows for the reverse dc biasing of the PN junctions, to widen



Name	P-/N- regions [nm]	
	width	separation
PNlines A	350	50
PNlines B	350	0
PNlines C	220	50
PNlines D	220	0
PNgrid	450	180

Figure 6.3: Sketch and dimensions of designed PN passivation patterns: *PNlines* (left) and *PNgrid* (right).

the depletion regions and further increase the substrate impedance. Out of the *PNlines* type solution, four different patterns are obtained: (i) different P-/N-doped region widths, (ii) presence of an intrinsic region between the P-/N-doped regions or not. Small dimensions are used to define the patterns in compliance with the process design rules (**Figure 6.3**).

6.2.2 RF performance results - transmission lines

The transmission line measurements have been performed from 0.1 GHz to 67 GHz with FormFactor I67 probes on a metallic chuck. The measurements are first corrected with a probe-tip Line-Reflect-Reflect-Match (LRRM) calibration performed on the 101-190C calibration substrate. Then, the mTRL method is applied to the measurement of transmission lines of different lengths and an Open reflect structure. As explained in **Chapter 2**, the TL propagation constant (γ) is extracted from the mTRL algorithm, and the characteristic impedance is extracted from the calibration comparison technique using either **[74]** when the Reflect is available or **[73]** otherwise.

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CPW in M1-M2

Figure 6.4 shows the total transmission losses (α), the substrate effective resistivity (ρ_{eff}) and the substrate effective permittivity ($\varepsilon_{sub,eff}$) extracted from the M1-M2 CPW lines on different substrates. As expected, the effective resistivity and permittivity of the standard resistivity substrates reach $\rho_{eff} = 7$ and $10\,\Omega$cm, for std1 and std2, respectively, and $\varepsilon_{sub,eff} \approx 11.7$ (the underneath stack includes a thin layer of oxide and a 152 µm-thick substrate), beyond the slow-wave mode cut off frequency f_{sw} (> 40 and 30 GHz for std1 and std2, respectively).

The $985\,\Omega$cm (HR2) and $620\,\Omega$cm (HR1) high-resistivity substrates without any interface passivation suffer from PSC effects, featuring an effective resistivity of 36 and $42\,\Omega$cm (at 50 GHz), representing an improvement of 1.5 and 1.7 dB/mm in α, respectively, with respect to the standard resistivity substrate (std2).

It is interesting to note how a small absolute variation in ρ_{eff} (from 7 to $10\,\Omega$cm) among the std1 and std2 substrates leads to strong additional losses in the M1-M2 CPW lines: $+1.5$ dB/mm in α at all frequencies above f_{sw} (> 40 GHz) from std2 to std1; whereas the difference of ρ_{eff} (from 36 to $42\,\Omega$cm) in HR1 and HR2 leads only to ~ 0.2 dB/mm of difference in transmission losses. The reason is that the rather large relative variation of ρ_{eff} among the std1 and std2 substrates significantly reduces the substrate losses that are much larger for a $\rho_{eff} \approx 10\,\Omega$cm effective substrate than a $\approx 40\,\Omega$cm effective substrate.

Figure 6.4 also shows that the *PNline* pattern (A) effectively solves the PSC issue and retrieves high values of effective resistivity ($\sim 300 - 1000\,\Omega$cm at 10 GHz). The series combination of highly doped and depleted regions at the silicon-oxide interface slightly changes the electric field configuration inside the substrate by increasing by a small extent its concentration at the interface. Therefore, the effective permittivity sensed by the CPW lines increases a little (13.1). Furthermore, the effectiveness of the PN patterns decreases with frequency due to the frequency-decreasing capacitive impedance in the depletion regions as explained above, which is translated into a decreasing effective resistivity with frequency. Nevertheless, applying a reverse-bias to the P-doped and N-doped regions enlarges the depletion regions, which (i) overall improves the effective resistivity (to 100 and $200\,\Omega$cm at 50 GHz for HR2 and HR1, respectively) and propagation losses (0.7 and 0.6 dB/mm losses improvement compared to HR2 and HR1, respectively, without interface passivation), (ii) as

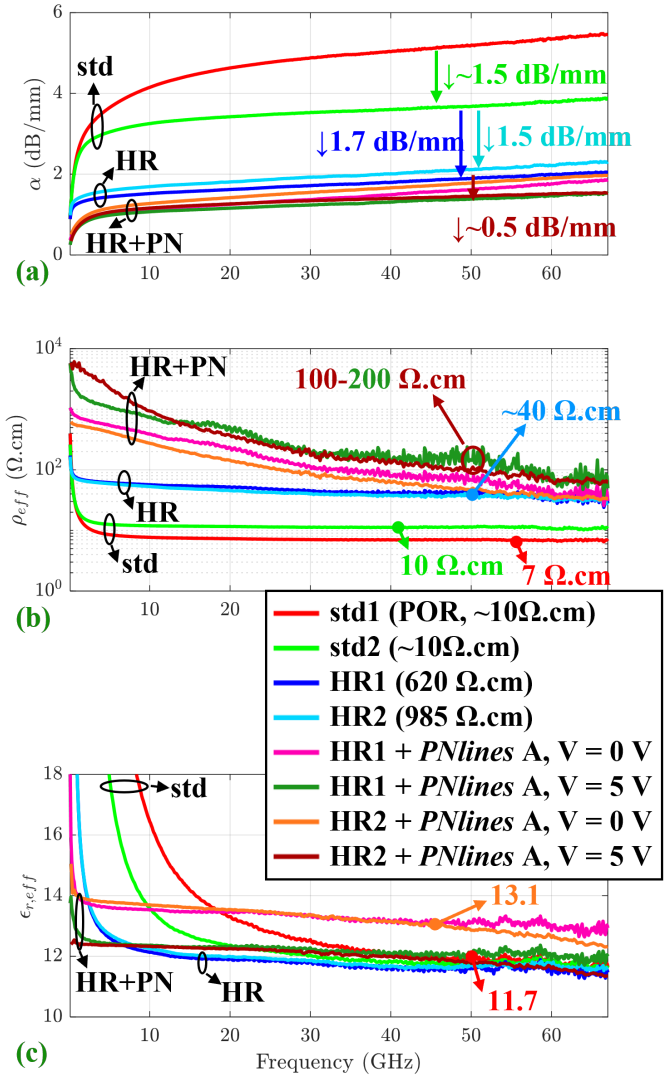


Figure 6.4: Propagation losses (a), and substrate parameters: effective resistivity (b) and permittivity (c), from M1-M2 CPW line measurements.

well as its roll-off with frequency and (iii) reduces the effective permittivity to ~ 12.

Large-signal measurements of the 2 mm-long M1-M2 CPW lines are also performed. The power of a 900 MHz single-tone input signal is swept and the spectral content of the output is measured. The substrate non-linearity, distorting the signal propagating along the CPW line, is benchmarked in **Figure 6.5**, where the output harmonic components H2 (1.8 GHz) and H3 (2.7 GHz) are plotted relative to the H1 fundamental (f_0) power.

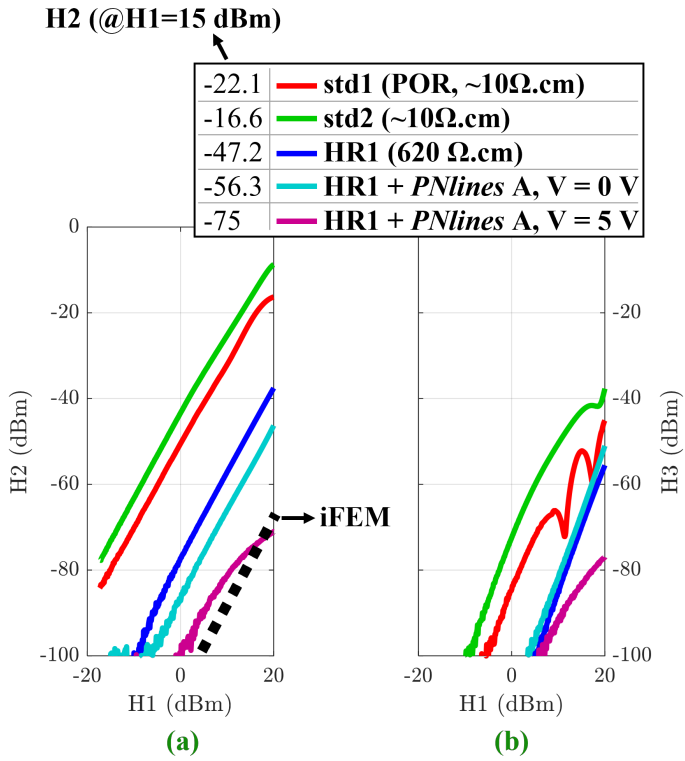


Figure 6.5: Substrate non-linearity benchmark. Measured second (a) and third harmonic (b) levels versus power at fundamental frequency of the output signal propagating in a 2 mm-long M1-M2 CPW line on different substrates. The H2 levels at H1 = 15 dBm are reported in the legend. Estimated harmonic distortion for the same CPW lines on a iFEM^{TM} substrate, in thick, black, dashed lines.

The HR substrate achieves a $25-30\,\text{dB}$ reduction in substrate-induced second harmonic level compared with the std substrates. H2 is further reduced by 9 and 28 dB when the interface is passivated with the *PNlines* A pattern, with 0 V and 5 V reverse-bias, respectively. The same CPWs on a commercial trap-rich substrate (iFEM$^{\text{TM}}$) are expected to have a H2 of $-77\,\text{dBm}$ (at H1 $=$ $15\,\text{dBm}$) for an f_0 of 900 MHz, according to the large-signal substrate model developed and described in **[209]**. So, at f_0 of 900 MHz, the linearity results (H2 $=-75\,\text{dBm}$ at H1 $=15\,\text{dBm}$ for the reverse-biased *PNlines* A on HR1) are competitive to those estimated for the same CPW line on trap-rich iFEM substrates.

Several PN patterns with different dimensions (cf. **Figure 6.3**) are designed and fabricated. **Figure 6.6** shows the impact of those dimensions on the effective resistivity and relative permittivity for M1-M2 CPW lines from the $985\,\Omega\text{cm}$ HR substrate. For both pattern widths, the presence of an intrinsic region between the P-/N-doping regions improves the effectiveness of the PN passivation solution by widening the depletion regions. In this run (with fixed implant energy and dose parameters), a width of 350 nm yields the best results. It is also worth noting that applying a reverse bias to the PN junctions improves the substrate losses resulting in almost the same ρ_{eff} for all *PNlines* patterns.

More interestingly is the fact that the *PNgrid* passivation method features the highest effective resistivity among zero-biased or unbiased PN patterns. Indeed at high frequencies (above 10 GHz), the *PNgrid* pattern features an effective resistivity ($\sim 440\,\Omega\text{cm}$ at 15 GHz) really close to the reverse-biased PNline patterns ($\sim 440-570\,\Omega\text{cm}$ at 15 GHz). Although the reverse-biased *PNlines* patterns perform better (mainly visible below 10 GHz), the *PNgrid* pattern offers the great advantage of not requiring a co-design between the PN interface passivation solution and the overlying layout, therefore significantly saving design time. In terms of area consumption, both patterns are designed below the passives, such that they do not increase the overall footprint. It should be noted that the curves are somehow noisier in **Figure 6.6**, compared to **Figure 6.4**, because only 760 µm-long lines (as well as thru lines) are available on the mask to study the impact of PN patterning (as opposed to 2 mm-long lines for the lines with *PNlines* A pattern and the ones without PN junctions).

The substrate non-linearity performance of the different PN patterns is benchmarked in **Figure 6.7**. The measurements of the 760 µm-long M1-M2 CPW lines are used (instead of the 2 mm-long lines), because not all PN patterns are available for the longest line. The length difference is the reason for the

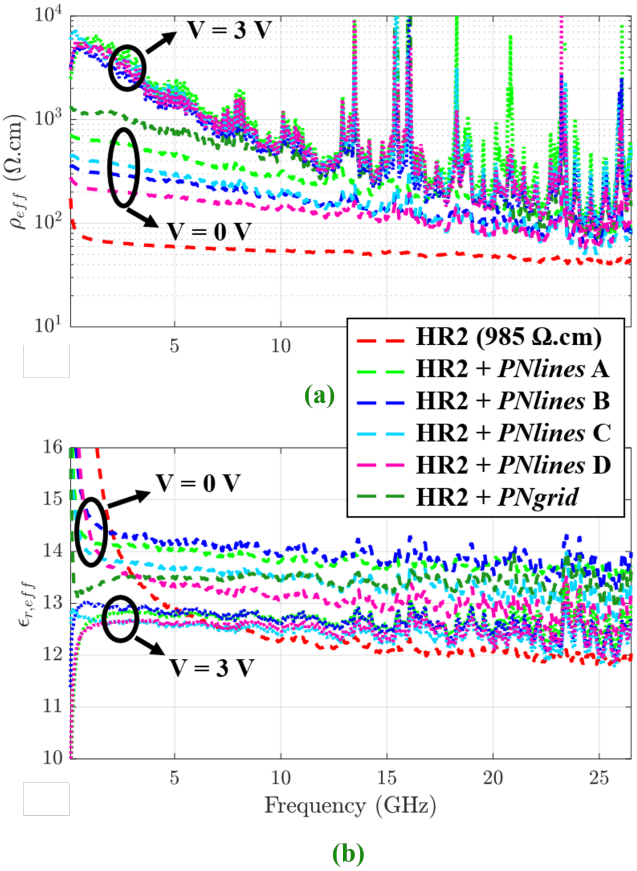


Figure 6.6: Substrate parameters: effective resistivity (a) and permittivity (b), from M1-M2 CPW line measurements on 985 Ω cm high-resistivity substrate with different PN pattern designs. The measurements in this figure are noisier than in **Figure 6.4**, because only 760 µm-long CPW lines and thru lines are available for the different PN patterns to save test chip area.

differences in absolute levels of H2 and H3 powers reported in **Figure 6.5** and **Figure 6.7** for identical substrates.

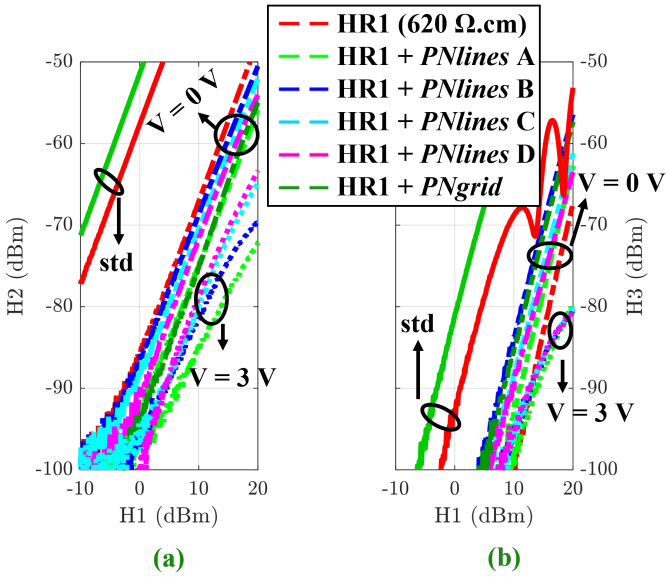


Figure 6.7: Substrate non-linearity benchmark. Measured second (a) and third harmonic (b) levels versus power at fundamental frequency of the output signal propagating in a 760 µm-long M1-M2 CPW line on different substrates. std1 and std2 measurements are added in solid lines for reference.

Similar observations made for the substrate losses (ρ_{eff}) above hold in terms of non-linear performance. (i) All PN patterns improve the harmonic levels compared to the case where the interface is not passivated. (ii) Increasing the depletion region (mostly by reverse biasing) greatly enhances the effectiveness of the PN passivation solution (and reduces the harmonic levels). (iii) The *PNgrid* pattern offers great performance (7 dB reduction compared to the HR case without passivation), nevertheless, (iv) the best performance is achieved with the reverse-biased *PNlines* A pattern (14 dB of further improvement). A summary of the different PN patterns large-signal performances is reported in **Table 6.1** showing the H2 level at H1 = 15 dBm.

Table 6.1: Substrate non-linearity becnhmark of the different PN patterns. Reported H2 values at H1 = 15 dBm.

Substrate options	**H2 at H1** = 15 dBm **(dBm)**	
	Reverse bias = 0 V	***Reverse bias*** = 3 V
HR1 (620 Ω cm)	−57.1	N/A
HR1 + *PNlines* A	−65.4	−78.2
HR1 + *PNlines* B	−59.3	−74.3
HR1 + *PNlines* C	−61.1	−71.7
HR1 + *PNlines* D	−62.4	−70.4
HR1 + *PNgrid*	−64.5	N/A

CPW and TFMS in QB

The total propagation losses and effective substrate parameters extracted from the CPW lines in QB are shown in **Figure 6.8**. Due to the ∼ 10 µm-thick dielectric stack between the CPW line and substrate, the effective permittivity and resistivity are averaged out and yield a lower $\varepsilon_{r,sub,eff}$ and larger ρ_{eff} compared to the values extracted from the M1-M2 CPW lines [2] . The same trends are observed with respect to the effective resistivity among the various substrates. From a ρ_{eff} value of 30 and 42 Ω cm at 50 GHz for the std1 and std2 substrates, respectively, the ρ_{eff} is increased to ∼ 200 Ω cm with HR substrates. The *PNlines* A pattern enhances the performance with a ρ_{eff} increase from ∼ 350 Ω cm (0 V bias) up to ∼ 1 kΩ cm (5 V reverse biasing).

The bump in $\rho_{eff}(f)$ around 25-40 GHz (mostly visible for the low-loss substrates) is non physical and is caused by an incorrect distribution of total losses α among metallic resistive (R) and substrate-related losses (G) as explained in **Chapter 3**. Indeed at those frequencies, the $R(f)$ term has a non physical bump as can be seen in the inset of **Figure 6.8b**. This bump in measurements is attributed to some probe coupling to the chip environment in a similar way as the couplings discussed in **Section 4.1** and is only partially corrected by the mTRL de-embedding. Such bump and probe coupling is also present in the

[2] Large-signal measurements of the same type as the one shown in **Figure 6.5** and **Figure 6.7** have also been performed for the CPW and TFMS lines in QB. However, their large-signal response is dominated by a parasitic antenna diode that is mandatory to pass the DRC rules. The non-linearity in those lines coming from the substrate is expected to be reduced compared to the M1-M2 CPW lines due to the substrate being farther away from the metal lines. No variation due to different substrates is observed, so these measurements are not reported here.

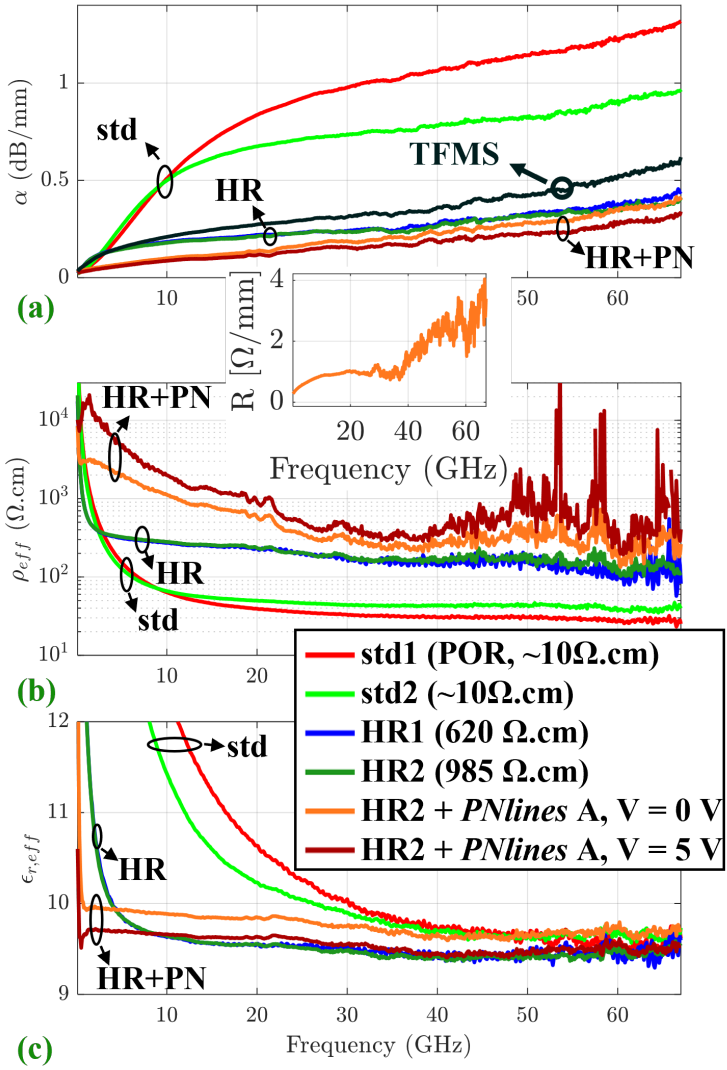


Figure 6.8: Propagation losses (a), and substrate parameters: effective resistivity (b) and permittivity (c), from QB CPW and TFMS lines measurements. Inset: extracted per-unit-length series losses $R(f)$ (from the per-unit-length *RLGC* transmission line elements) from CPW lines measurements.

measurements of the MMW inductor as explained in a subsequent section.

The propagation losses of a TFMS line designed for 50 Ω characteristic impedance is also shown in **Figure 6.8a**. TFMS lines are usually preferred in CMOS technology using standard resistivity substrate thanks to the shielding ground plane that prevents any substrate losses. Neglecting losses in the BEOL dielectric layer, it is assumed here that the only losses present in TFMS lines are thus metallic losses. Nevertheless, when a quasi-lossless substrate is available, a CPW topology seems more interesting as it offers the possibility of synthesizing a given characteristic impedance with wider metal lines, and hence reduced metallic losses. The resulting 50 Ω Z_c TFMS line in this work has a signal width of $\sim 10\,\mu m$, yielding $\alpha = 0.42\,dB/mm$ at 50 GHz. As expected, the designed 50 Ω CPW line fabricated on a standard resistivity substrate suffers from significant substrate losses: $\alpha = 1.14$ and $0.83\,dB/mm$ at 50 GHz for std1 and std2, respectively, which is much larger than the TFMS line losses. However, when a low-loss substrate is available (i.e. high-resistivity substrate with or even without PN junctions), the designed CPW line becomes a better choice of transmission line featuring $\alpha = 0.22\,dB/mm$ at 50 GHz in the best case, thanks to reduced metallic losses and small or negligible substrate losses.

The above results demonstrate the effectiveness of the PN interface passivation solution to counter the PSC effect, featuring low substrate losses and harmonic distortion through the measurement of CPW lines designed with different metal layers. These encouraging results are confirmed in the following with other types of passive devices.

6.2.3 RF performance results - inductors

The inductors are measured from 100 MHz to 67 GHz. A 2-step calibration is performed (LRRM calibration on a calibration substrate, followed by an on-wafer mTRL calibration using the TFMS set of lines) to move the reference plane to the device under test (dut) vicinity with high accuracy at mm-wave frequencies, as seen in **Chapter 4**. Then, the S-parameters are transformed in Y-parameters and the inductance (L) and quality factor (Q) of the inductors are computed as

$$L = \mathrm{Im}\left(\frac{1}{Y_{11}}\right)\cdot\frac{1}{\omega},\ \text{and}\ Q = \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})}. \tag{6.1}$$

RF inductor

Figure 6.9 shows the 1 nH inductance and quality factor of the RF inductor on several substrates. There is a small difference in the RF inductor quality factor between the std substrates: the std1 features a peak Q of 15.6 while the peak Q of std2 is 16, in agreement with the larger substrate losses for std1 already observed above in **Section 6.2.2**. A great improvement in the RF inductor quality factor is achieved with a HR substrate thanks to a much greater bulk resistivity. Indeed, the peak Q value is around 1.4 times higher (from 16 to 23) and shifted to higher frequencies. Further improvement (from 23 to 25) is achieved thanks to the 5 V reverse-biased PN junctions, which significantly increase the substrate resistivity at the interface (and overall the substrate losses at high frequencies as seen above).

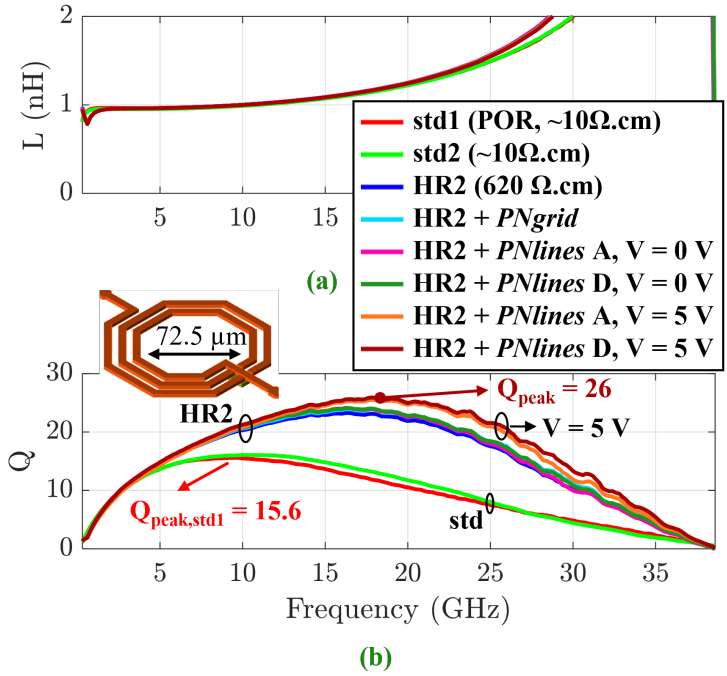


Figure 6.9: Inductance (L) and (b) quality factor (Q) of 5-20 GHz inductors on different substrates, with or without interface passivation.

The impact of substrate losses to the peak Q between std1 and std2 (15.6 to 16) or between the HR substrate with and without PN passivation (23 to 25) is

much lower than the observed substantial increase in effective resistivity and reduction in CPW losses (α) from the **Section 6.2.2** (in particular for the M1-M2 CPW lines). For instance, the effective resistivity of CPW lines in QB on HR substrate gets an up to $\times 4$ increase with PN junctions (see **Figure 6.8**). The corresponding gain in propagation losses is also considerable ($-0.1\,\mathrm{dB/mm}$ at 20 GHz), but is not as large as the one achieved for the CPW lines in M1-M2 ($-0.5\,\mathrm{dB/mm}$ at 20 GHz). As explained above and similarly to the CPW lines in QB, the signal line in QB is separated from the substrate by a $\sim 10\,\mu$m-thick dielectric stack. As a consequence, the inductor's overall shunt losses through the substrate (related to the effective resistivity) are already rather low, because there is a lower concentration of electric field inside the substrate (compared to the CPW lines in M1-M2).

MMW inductor

Figure 6.10 reports the measurement of the 170 pH inductance and its quality factor on different substrates. In **Figure 6.10b**, the measured inductor quality factor shows little variation among different substrates. The inductors on both standard resistivity substrates feature a similar quality factor with a peak value around 21.1. The inductor on HR2 without interface passivation exhibits a quality factor very close to std1 and std2 ones, with a potential improvement that is clouded by the measurement noise at such high frequencies. The inductors with PN patterns feature a small, but noticeable, improvement in quality factor and, more importantly, applying a reverse-bias to the PN junctions results in a small, but consistent and distinct, improvement in quality factor. Overall, the improvement is small, estimated to be no more than 15 % (the main curves from **Figure 6.10b** are reported again in **Figure 6.10c** to ease the reading).

In **Figure 6.10b** the curves from the inductor measurement on HR2 with *PNlines* D pattern are affected by a bump in measurements from 45 to 63 GHz. The data points have then been removed from the figure to avoid any misinterpretation. The origin in the bump is the same as the one in the 25-40 GHz measurements of the QB CPW lines from **Section 6.2.2**, i.e. an uncorrected probe coupling to the nearby chip environment. The environment (and thereby the coupling) varies between duts and the on-wafer calibration structures, therefore a residual error is sometimes present in the corrected measurements, in a similar way as the discussed probe-dependent residual error in **Section 4.1**.

The above measured trends are confirmed by EM simulations performed with Keysight Momentum as shown by the circle data points in **Figure 6.10c**. Detailed explanations on how EM simulations are performed, de-embedded

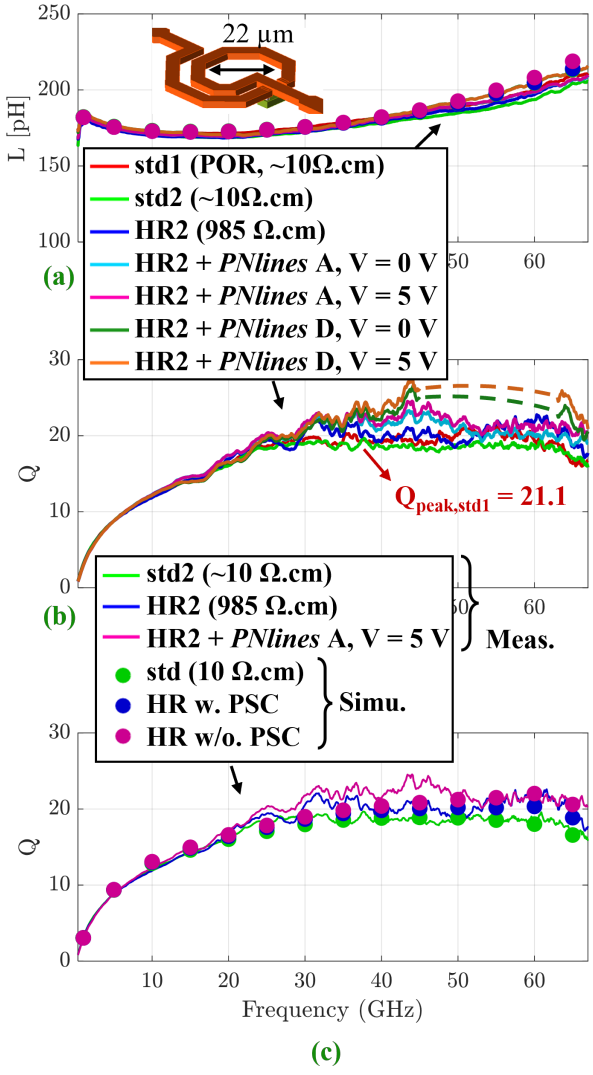


Figure 6.10: (a) Inductance (L) and (b and c) quality factor (Q) of MMW inductors on different substrates, with or without interface passivation. Measurements in solid lines, EM simulations in circles.

and how the EM stack of the HR substrate with PSC is calibrated to this study can be found in [27] [3]. The improvement reported here for this MMW inductor is smaller than the RF inductor or previously reported studies [210, 211] mainly because of the smaller geometry of the MMW inductor, scaling down with higher operating frequency. Indeed, the smaller geometry of the MMW inductor, which is also far from the substrate ($\sim 10\,\mu m$), leads to a reduced concentration of electric field (E-field) and eddy currents inside the substrate, thus attenuating the impact of substrate resistivity on the inductor quality factor. A second effect of higher operating frequency is an increase in metallic losses due to skin and proximity effects, which further reduce the relative impact of substrate losses on the overall inductor losses.

In the case of the MMW inductor, full-wave 3D EM simulations[4] show that 24 % of the E-field is concentrated inside the substrate[5], as shown in Figure 6.11, [27]. A different layout design of this MMW inductor (targeting mm-wave frequencies, such as 28 or 39 GHz) could have been proposed by stacking several metal layers to reduce metallic losses. By stacking the metal layers, the distance between the coil and substrate is reduced, making the inductor more sensitive to the substrate resistivity (due to an increased E-field concentration inside the substrate). Such inductor design (shown in Figure 6.11) is investigated via simulations in [27] for which a $\sim 35\,\%$ improvement in quality factor is expected moving from a std to a HR substrate with interface passivation.

The reduction in substrate losses achieved with a surface-passivated high resistivity substrate is again demonstrated in this sub-section through the quality factor improvement of two inductors designed at RF (5-20 GHz) and mm-wave

[3] In short, EM simulations using Keysight Momentum are performed on each in-situ mTRL calibration structure, i.e. TFMS Lines of different lengths and a Reflect, as well as on the inductor including the probe pads. Then, calibrated EM simulations are extracted in the same way as the measurements with the mTRL method. The EM stack for the HR substrate with PSC consists of a two-layer substrate stack of a bulk HR (1 kΩ cm) Si layer below a 1 µm-thick 3 Ω cm Si layer, whose resistivity value was adjusted to fit $\rho_{eff}(f)$ measurements of the above M1-M2 CPW lines, with additional EM simulations.

[4] Performed at 30 GHz with Ansys HFSS, driven modal solution type, with bridge-type lumped ports (access not simulated, only intrinsic inductor), up to 46000 tetrahedra.

[5] The E-field concentration is computed on a vertical plane cutting the inductor in its middle (in an approximately symmetric way). The E-field concentration ratio in the substrate is computed by integrating the magnitude of the E-field vector ($|\vec{E}| = \sqrt{|E_x|^2 + |E_y|^2 + |E_z|^2}$) on the vertical plane inside the substrate only, divided by the E-field vector magnitude integrated across the whole vertical plane.

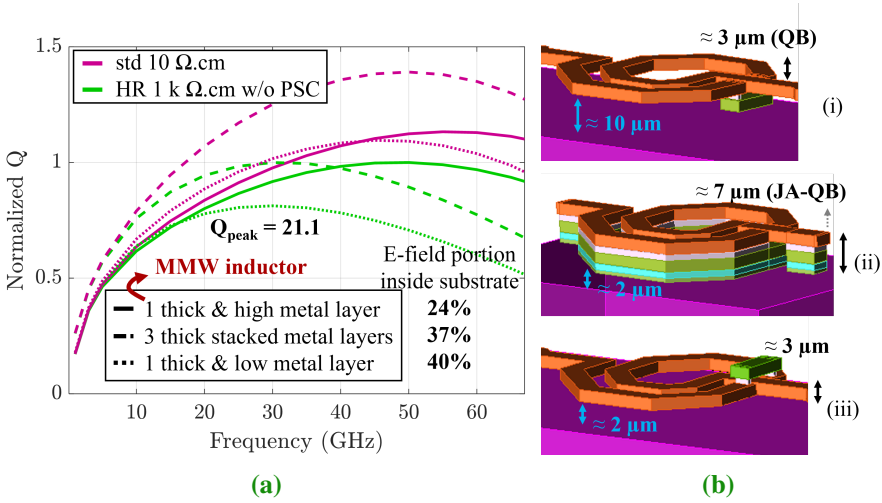


Figure 6.11: Left (a): EM simulations of inductors' Q normalized to the peak Q of the MMW inductor on std substrate ($Q_{peak} = 21.1$). 3 inductors are simulated: (i) MMW inductor (solid lines, $\sim 10\,\mu$m away from the substrate, $\sim 3\,\mu$m-thick metal), (ii) inductor on 3 thick Cu layers (dashed lines, $\sim 2\,\mu$m away from substrate, $\sim 7\,\mu$m-thick metal), (iii) inductor on 1 metal layer closer to the substrate (dotted lines, $\sim 2\,\mu$m away from substrate, $\sim 3\,\mu$m µm-thick metal), on top of two substrates: std (green), HR without PSC (purple). Right (b): Sketch of the simulated inductors.

(30-60 GHz) frequencies. Although the improvement is rather small for the MMW inductor, a re-design of the inductor, taking benefit of the full back-end of line available in the technology, should again strongly benefit from a low-loss substrate such as proposed by the PN interface passivation solution.

6.2.4 RF performance results - crosstalk structure

A crosstalk structure (sketch in **Figure 6.2f**) is also designed and fabricated on several substrates. It consists of 2 metal pads in bottom metal layers facing each other. It is used to evaluate the amount of crosstalk through the substrate between two adjacent structures (transistors, circuits or systems **[212]**). The crosstalk structures are measured from 10 kHz to 100 GHz. The measurements are de-embedded with an open-pad measurement. The magnitude of S_{21} is plotted in **Figure 6.12** for different substrates.

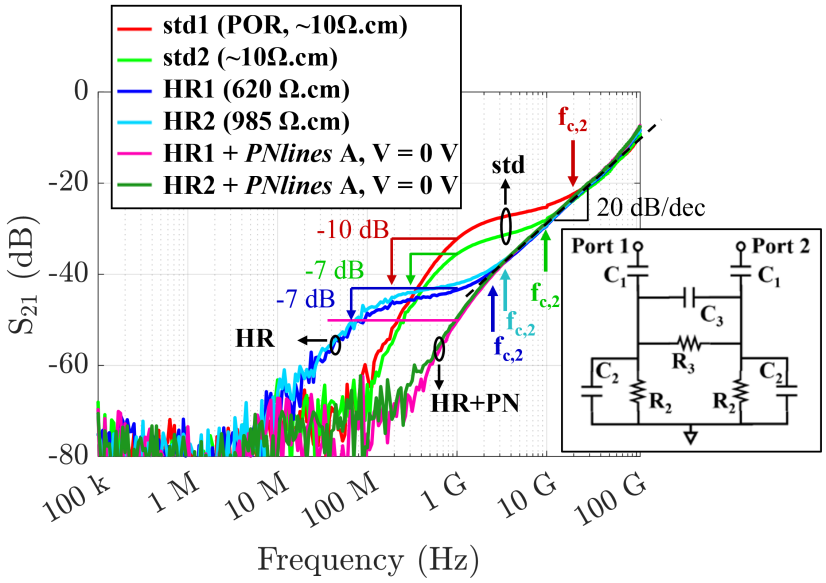


Figure 6.12: Crosstalk measurements on different substrates. Higher cutoff frequency ($f_{c,2}$) are shown with arrows for each substrate. Crosstalk reduction with different substrates at 1 GHz are also indicated. Inset: small-signal equivalent circuit of the crosstalk structure.

The crosstalk structures can be modeled by the equivalent circuit shown in the inset of **Figure 6.12 [212]**. For all substrates, the high frequency behavior of $|S_{21}|$ is dominated by the capacitive coupling between the two pads (through C_3). Since all substrates have the same permittivity, all $|S_{21}|$ curves converge at high frequencies. Then, as frequency decreases, the $|S_{21}|$ slope starts flattening, $|S_{21}|$ tending to a plateau. This upper cutoff frequency ($f_{c,2}$), connecting the plateau to the high frequency 20 dB/dec slope in $|S_{21}|$ (indicated with arrows in **Figure 6.12**) is related to the substrate resistivity profile. It depends on the C_3 and R_3 terms from the small-signal equivalent circuit:

$$f_{c,2} = \frac{1}{2\pi R_3 C_3}. \tag{6.2}$$

For a non-uniform substrate resistivity profile, such as is the case in HR substrates suffering from PSC, the R_3 term averages out the resistive behavior of the coupling between the two pads, in a similar way as the effective resistivity

for substrate losses in CPW lines[6]. In other terms, since C_3 is constant for all substrates (of same permittivity), $f_{c,2}$ (through R_3) is directly correlated to the substrate RF losses: the higher $f_{c,2}$, the lower R_3 (the lower the effective resistivity), the larger the RF losses. Indeed, the values of ρ_{eff} extracted from CPW lines measurements in **Section 6.2.2** correlate well with the cutoff frequencies in the crosstalk measurements.

The highest cutoff frequencies around 10-20 GHz for the std resistivity substrates (std2 and std1) is mainly caused by the low bulk substrate resistivity. The HR substrates without PN implants feature lower cutoff frequencies ($\sim$ 3 GHz), but in these cases, R_3 is dominated by the thin conductive sheet at the interface due to the PSC effect. The higher cutoff frequency of the HR2 than the HR1 (without interface passivation) correlate well with the lower extracted ρ_{eff} from M1-M2 CPW lines, i.e. 50 and 68 Ω cm at 50 GHz for HR2 and HR1, respectively. These observations show that the HR2 substrate feature a slightly higher level of PSC than HR1. Whereas the measured crosstalk structures on HR substrates with the designed PN pattern do not exhibit a plateau (above the measurement noise floor), demonstrating that the PSC effect has been effectively countered.

The $|S_{21}|$ behavior below the plateau strongly depends on the overall geometry of the crosstalk structure, mainly on the crosstalk pads distance to ground. The low frequency deviation from a 20 dB/dec slope (for the interface-passivated HR substrates) or plateau (for all other substrates) in the $|S_{21}|$ curve does not only depend on the substrate resistivity profile, but mainly on how the pads couple to the ground (hence on the structure layout). For that reason, the low frequency behaviors of the curves are considered out of scope of this analysis and are not discussed. At 1 GHz (a frequency arbitrarily chosen to be high enough for the crosstalk to solely depend on the substrate resistivity profile), moving from a std resistivity (std2) to a HR substrate (with PSC) brings a 7 dB improvement in crosstalk, while a further 7 dB can be achieved when PN implants are used to negate the PSC effect. With a larger crosstalk pad spacing to ground (distance of 50 µm in **Figure 6.2f**), the $|S_{21}|$ plateau would extend over a larger frequency range below $f_{c,2}$ and the crosstalk reductions from one substrate to another would be much larger at lower frequencies.

[6] This simulation is similar to the substrate coupling of the switchable capacitor in **Section 5.3.3**. The R_3 and C_3 are equivalent to the substrate impedance between the transistor and nearby ground, represented by R_{sub} and C_{sub}.

6.2.5 Summary of passives results on 22 nm FD-SOI on HR substrates

In this section, we have demonstrated that a high quality RF substrate can be obtained in an advanced industrial FD-SOI technology using the *PN interface passivation* solution applied to high-resistivity substrates.

Indeed, the substrate features an improved effective resistivity above $\sim 200\,\Omega$cm up to 50 GHz in the best PN junctions scenario, which represents a > 30 times improvement with respect to the POR, at M1 level. Even for lines in QB, a reduction of $0.2\,\mathrm{dB/mm}$ in α is shown for CPW lines on the best substrate case compared with TFMS line design at 50 GHz. Great substrate isolation is also demonstrated with the PN junctions technique via measurements of crosstalk structures. Finally, we show that strong quality factor improvement with higher quality RF substrates can observed for inductors with a large portion of electric field inside the substrate (i.e. globally with large dimensions) even at mm-wave frequencies, although it might require a re-design of the passive.

These results are of particular interest for the designed circuits presented in **Chapter 5**, as it indicates that quality factor of the passives from the designed circuits can be greatly increased, and therefore a significant improvement in the circuits' FoMs could potentially be achieved. In the next part, we perform simulation analyses to, first study how the substrate loss impacts critical passives for each circuit, then how the circuit can be optimized with a low-loss substrate and quantify the expected improvement.

6.3 Improvement of 39 GHz LNA

As identified in the previous chapter, the main contributor to NF in the input matching network of the designed 39 GHz LNA is the shunt spiral inductor, with a contribution of 0.58 dB. Let us thus focus on this passive.

The input spiral inductor is designed on the QB layer, which is optimized for integration on a standard resistivity (std) substrate (called 'Ind-S'). Its dimensions are given in the inset of **Figure 6.13**. The simulated quality factor is 17.6 at 39 GHz. EM simulations of the same inductor geometry on a quasi-lossless high-resistivity (HR) Si substrate yields a similar quality factor (green line in **Figure 6.13**). Therefore, no improvement in gain or noise figure (small-signal performance) is expected with a more resistive Si substrate.

Nevertheless, stacking all thick metal layers available[7] results in an inductor (called Ind-H) with lower metallic losses and, if coupled with a HR substrate, in

[7] And re-designing its dimensions to reach the same inductance value at 39 GHz.

a 30 % improved quality factor ($Q = 22.9$) as shown in blue lines in **Figure 6.13**. Inserting this inductor in the overall LNA simulation yields a minimum noise figure of 2.38 dB, which represents an improvement of 0.06 dB with respect to the implemented LNA. The much larger improvement in Q for Ind-H when moving from a std to a HR substrate compared to Ind-S is explained by a larger concentration of electric field in the substrate due to the inductor being closer to it, as explained in **Section 6.2.3**.

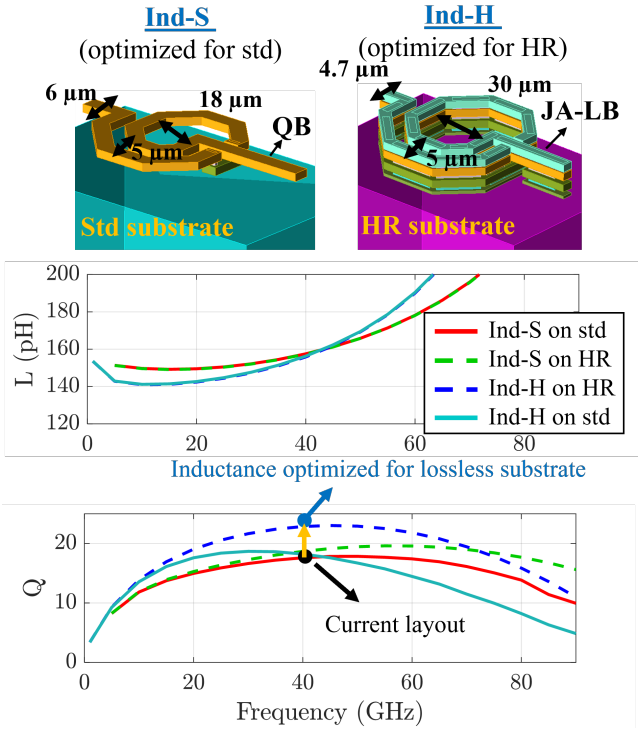


Figure 6.13: Simulated L and Q of the shunt input inductance (L_1) on std (solid lines) and HR (dashed lines) substrates. Ind-S is optimized for std substrate and is used in the LNA prototype. Ind-H is optimized for HR substrate by stacking JA to LB metal layers.

A second attempt at further increasing the shunt inductor quality factor with a particular focus on metallic loss reduction is made. It results in two new inductors (each optimized for a given substrate, not shown) with a peak quality factor at 40 GHz of 24.4 and 37.3 on a std and a HR (without PSC effect)

substrate, respectively. These values are to be compared with the previously designed inductors with $Q = 17.6$ and 22.9 at 40 GHz on std and HR substates, respectively. However, it comes at the cost of a much larger footprint ($\times 3.6$). These two new inductors are placed in the LNA for overall simulations and they result in an improvement of 0.15 dB and 0.21 dB in NF, with respect to the nominal design (on standard resistivity substrate).

Even with re-optimized inductors, we still only observe a 0.06 dB improvement in NF, when a low-loss Si substrate is available for this LNA design. It suggests that, given the chosen strategy of input matching, substrate-related losses have a small impact on this LNA[8]. Other matching strategies could be studied that might result in more impactful substrate losses, such as with series inductor, transformer, transmission-line-based, etc. Furthermore, other elements such as the input pad and interconnects between the pad, inductor and FETs could be optimized for a low-loss substrate by removing the shielding and increase the signal width (while achieving 50 Ω characteristic impedance) for reduced losses, in a similar way as QB CPW lines feature lower losses on HR substrate than TFMS lines in **Section 6.2.2**.

[8]Despite the improvements in inductor quality factor, we still observe only a small 0.06 dB reduction in overall LNA's noise figure. Such a small improvement can seem surprising, however, understanding in details why it is the case for this circuit is not a straightforward task. Indeed, the relationship between losses in a matching network and the overall LNA's noise figure is not obvious. Frii's formula provides a simple expression of NF for cascading elements, but it assumes that there is no reflection. In our case, we do not have simultaneous noise and gain matching, meaning that there is some reflection occurring at the input, such that Frii's formula does not directly apply to the input-matching network and the remaining of the LNA.

In this case, exactly determining why the shunt inductor quality factor improvement has a small overall impact, would require to consider all matching elements (input pad, series capacitor, R-C stabilization network, etc.) and perform a detailed noise analysis. This becomes rather cumbersome and out of scope of this thesis.

6.4 Power Amplifier Improvement: Passives

As we have seen, the designed LNA is not so sensitive to substrate losses. However, the designed power amplifiers are likely more responsive to the substrate electrical properties as they feature un-shielded passives of a much larger footprint, thus with a larger portion of electric field sensing the substrate.

Let us first analyze the behavior of the output passives: output distributed balun and configurable hybrid coupler. Then, we study how the overall PAs performances are affected by a potential change of substrate.

The preliminary work performed in the previous chapter led to accurate *adjusted post-layout* simulations that agreed very well to measurements of the standalone output balun and hybrid couplers. In order to study the impact of a higher substrate resistivity, the simulations are repeated in the same conditions, except for an increase in substrate resistivity from the pre-defined value in the PDK (around 10 Ω cm for standard resistivity) up to 3 kΩ cm. The substrate resistivity of 3 kΩ cm can be considered as a 'lossless' substrate[9] (negligible substrate loss contribution), while the 200 Ω cm is representative of what could be accomplished with the best design of the PN junctions solution in **Section 6.2.2**.

Output balun

Simulation results for the output distributed balun are shown in **Figure 6.14**. Contrarily to the LNA's inductor, the substrate resistivity increase has a strong impact on the output matching insertion loss (IL). We observe that a 200 Ω cm resistivity substrate features a sufficiently low level of substrate loss, such that the IL is not further improved with the 3 kΩ cm HR substrate. A ~ 0.5 dB increase in IL can be achieved solely by increasing the substrate resistivity above ~ 200 Ω cm, without a re-design of the passive structure. Indeed, the distributed balun was optimized for a standard resistivity substrate, where a trade-off between substrate loss and metallic loss must be found. Given a low-loss substrate, we could have further optimized the balun by reducing metallic losses for instance.

[9] The associated loss tangent from a 3 kΩ cm resistivity Si substrate is lower than 2×10^{-3} above 20 GHz, see **Section 3.4**.

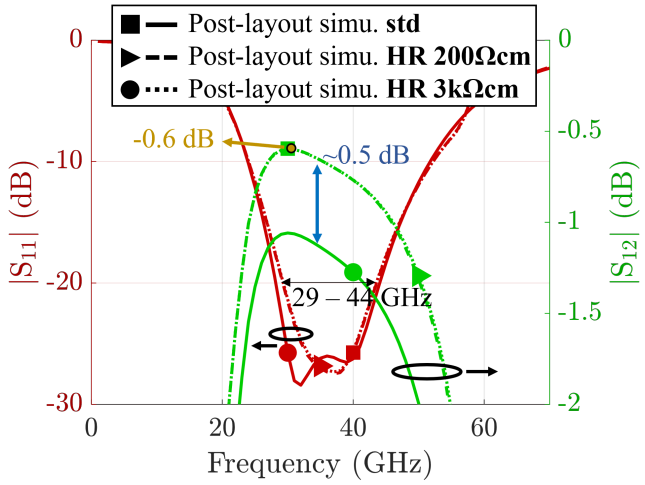


Figure 6.14: Adjusted post-layout simulation $|S_{11}|$ (left axis) and $|S_{12}|$ (right axis) of the designed output matching network. Simulations with different substrate resistivities from std to HR 3 kΩcm (without PSC effect).

Hybrid coupler

Simulations with larger substrate resistivities are also perform for the hybrid coupler. In addition to increase the EM stack substrate resistivity, the resistor R_{sub} from the equivalent substrate impedance between the switchable capacitor and local coupler ground (cf. **Figure 5.33**) is increased. C_{sub} is kept constant such that the R-C product ($R_{sub}C_{sub}$) is related to an effective resistivity equal to the EM stack substrate resistivity[10].

Simulation results for different states are shown in **Figure 6.15**. Here again, a strong improvement in insertion loss (0.6 to 0.8 dB) is achieved, with an optimum of 0.36 dB at 32.4 GHz. The phase differences do not vary much, and they could benefit from a re-design to achieve values closer to 90°. Although not shown in **Figure 6.15**, simulations with a 200 Ωcm resistivity are also conducted and yield the same performance as the 3 kΩcm HR substrate, similarly as the output balun.

[10] So, for the HR 3 kΩcm simulation, $R_{sub} = 800\,\Omega \times 6.6\,\text{fF}/(\varepsilon_0 \varepsilon_{r,Si}) = 480\,\text{k}\Omega$.

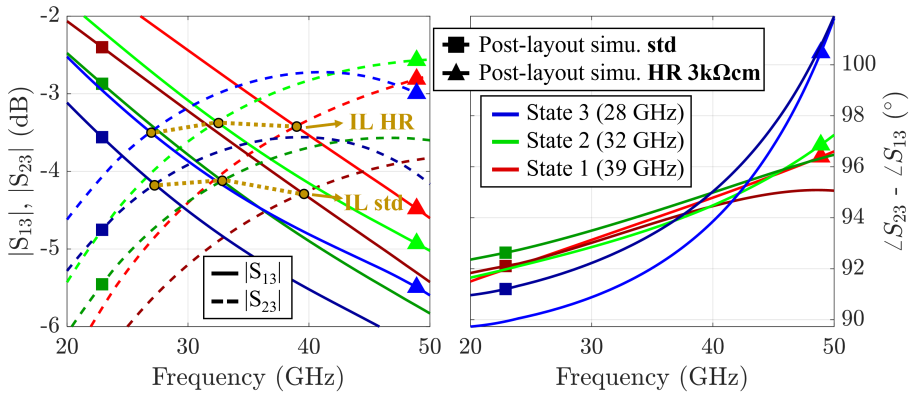


Figure 6.15: Adjusted post-layout simulations of the designed hybrid coupler performance: S_{13} and S_{12} magnitude (left) and phase difference (right). Simulations with different substrate resistivities from std to HR 3 kΩcm (without PSC effect).

6.5 Power Amplifier Improvement: Circuits

The strong improvements observed in passive circuit insertion loss suggest that the PAs can also benefit from enhanced figures of merit. So, we replace the simulated passives with larger substrate resistivities in the overall PAs simulations and analyze the results.

6.6 Improvement of Wideband 24-43 GHz PA1

The PA1 post-layout simulations with std and HR substrates are shown in **Figure 6.16** in the nominal bias condition ($V_{bg} = 0$ V). We observe a small-signal gain increase from 0.2 dB to 0.7 dB across the whole bandwidth thanks to the substrate loss improvement. Once again, negligible improvement is achieved for substrate resistivity above 200 Ωcm, so that only simulations of the std resistivity and 3 kΩcm HR will be shown in the following. A great increase in overall output power (~ 0.5 dB in P_{sat}) and peak PAE ($\sim 4\,\%$) is observed over the whole PA bandwidth. This is a direct consequence of the ~ 0.5 dB reduction in output balun insertion loss observed above.

Furthermore, we observe in **Figure 6.16c** that the load presented to the FETs does not seem to be altered by the change of substrate, because the CW large-signal gain and P_{out} are simply shifted to higher values, without a

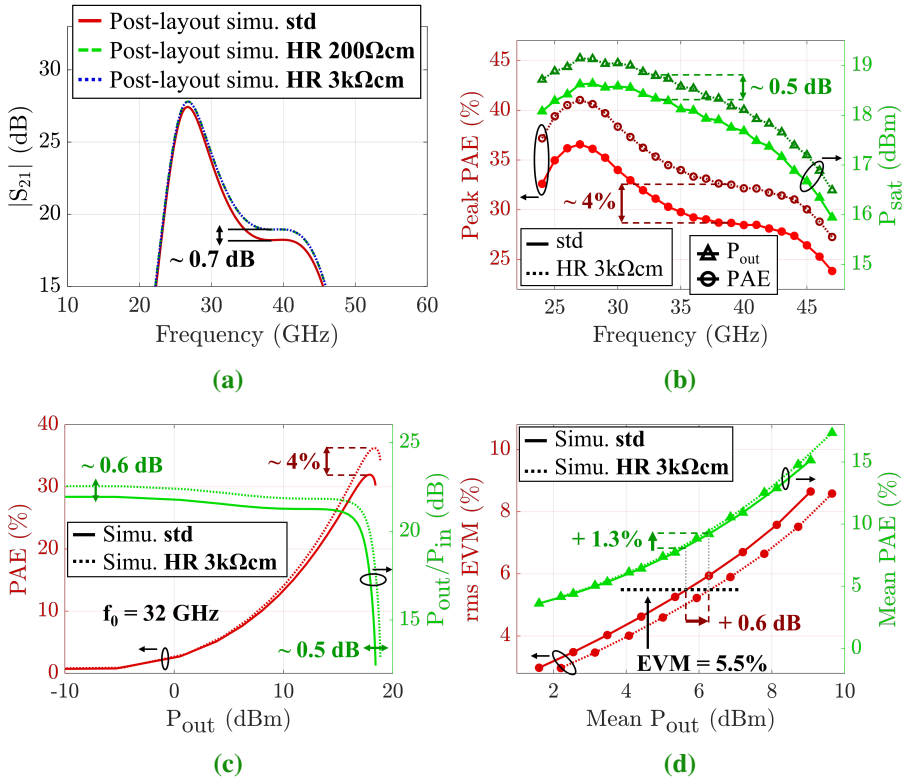


Figure 6.16: *Simulations* of PA1 with different substrate resistivities: std and HR (without PSC). (a) Small-signal gain. (b) CW large-signal peak PAE and P_{sat} versus frequency. (c) CW large-signal PAE and gain versus output power at 32 GHz. (d) 5G modulation signal at 32 GHz carrier frequency, rms EVM and mean PAE versus mean P_{out}.

modification in AM-AM distortion behavior.

In more representative application conditions, i.e. with 5G modulation signal *simulations* (**Figure 6.16d**), the improvement is also mainly described as an increase of output power for a given EVM. *Thanks to the reduced substrate loss, a* 0.6 dB *larger average* P_{out} *is achieved for the same EVM target (*5.5 *%), which directly increases the average PAE too by* 1.3 *%*. Since we are working with a large amount of backoff power, the larger peak PAE in compression with the HR substrate does not improve much the operation with 5G modulated signal.

6.7 Improvement of Configurable Balanced 24-43 GHz PA2

Simulations with a 3 kΩ cm HR substrate have been performed in a similar fashion for the configurable balanced PA2. Small-signal gain and CW large-signal gain and PAE at 32 GHz are shown in **Figure 6.17**. The HR simulations show a second unexpected peak in gain around 40 GHz. This second peak in gain is not present in the PA1 behavior, so its appearance in the balanced configuration is suspect and suggests the current PA2 design on HR substrate is not stable. Even though the small-signal Rollett stability analysis indicates that the PA is unconditionally stable ($K > 1$ and $|S_{12}S_{21} - S_{11}S_{22}| < 1$, not shown here), its application to a balanced topology (or to any topology with several internal amplifying stages) is not sufficient to guarantee a stable behavior. Additional simulations indicate that the presence of the hybrid couplers simulation on HR substrate is at the origin of these second peaks in gain. So, a re-design of these elements might be needed for a future stable design of PA2 on HR substrate.

Nevertheless, let us analyze the potential improvements PA2 could benefit from a HR substrate by looking at the CW large-signal simulations at 32 GHz, far from the likely unstable region. For PA2, increases of 0.8 dB and 5 % in P_{sat} and peak PAE are obtained with a low-loss Si substrate. The enhancement is even larger than PA1, because of insertion loss reduction in both the balun and the hybrid coupler at the output. These simulations demonstrate a great performance improvement could be achieved for PA2. However, for an experimental assessment, a re-design on low-loss substrate is necessary to ensure stability.

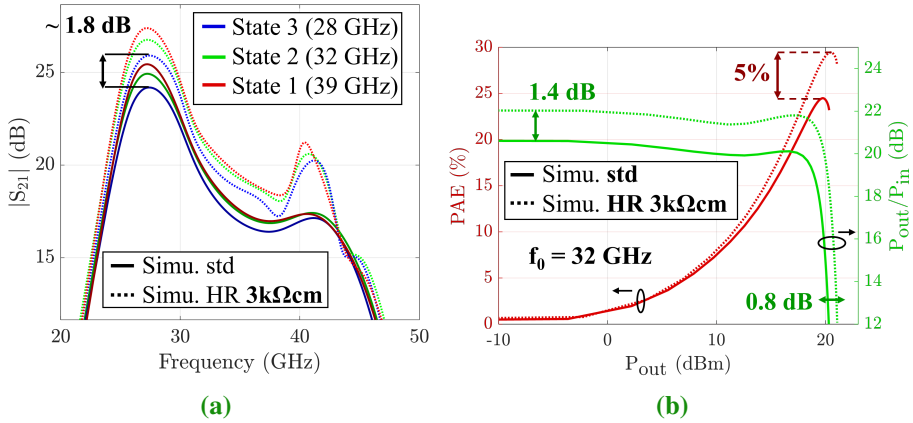


Figure 6.17: Simulations of PA2 with different substrate resistivities: std and HR (without PSC). (a) Small-signal gain. (b) CW large-signal PAE and gain versus output power at 32 GHz.

6.8 Conclusion

Current UTBB FD-SOI technology is fabricated on top of standard resistivity ($\sim 10\,\Omega$cm) substrate, which is known to entail significant substrate losses and coupling. Contrarily to PD-SOI technology, the well-known trap-rich HR substrate is not directly compatible with the FD-SOI process, so other substrate enhancement techniques have to be investigated.

In this chapter, we analyzed the *PN junctions interface passivation* solution to increase the interface resistivity by mitigating the PSC effect and retrieve large effective resistivity values of HR substrates. This solution is easily integrated in the FD-SOI fabrication process flow and has been applied to the industrial 22 nm FD-SOI technology.

Several PN patterns of different dimensions are fabricated to enhance the RF performance of HR substrates and are compared with HR suffering from PSC (without PN pattern) and standard resistivity substrates. Their performance is assessed via the measurements of several passives, i.e. CPW lines, inductors and a crosstalk structure. It is shown that, first, a high-resistivity substrate already significantly improves the substrate performance on all passives, and, second, all figures of merit are further greatly improved with the PN junctions passivation on high-resistivity substrates.

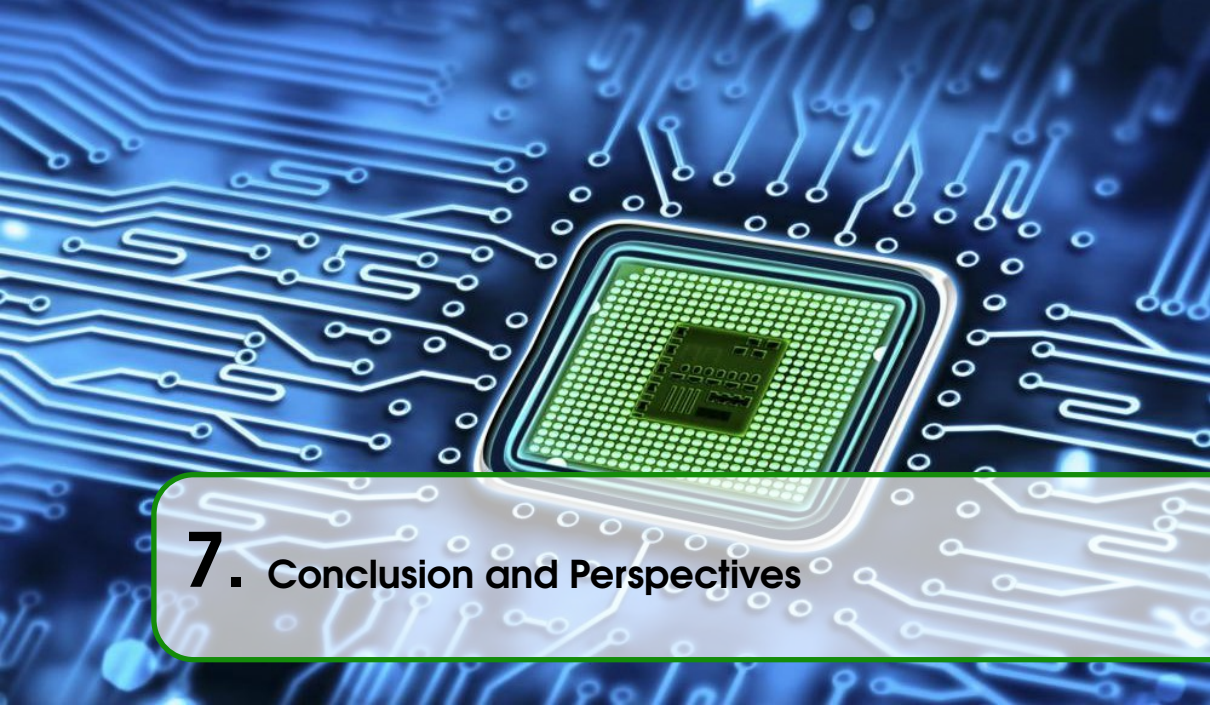
Indeed, from M1-M2 CPW line measurements, an effective resistivity

larger than $\sim 200\,\Omega$cm can be obtained up to 50 GHz in the best PN application scenario (with PiN diodes reverse biasing). Furthermore, great reduction in non-linearity generated by the substrate, reduction in substrate coupling and improvement of inductor quality factor (up to $\sim 60\,\%$) are also accomplished. Overall, the PN interface passivation solution was demonstrated to offer high quality RF substrates at RF and mm-wave frequencies for low-loss passives compatible with an industrial FD-SOI technology.

These very interesting results are then used to evaluate the potential performance improvement the designed circuits from **Chapter 5** can benefit from. Simulation-driven analyses are then performed for each circuit by replacing the EM stack substrate resistivity (for 2.5D EM simulations of passive elements), in order to quantify the impact of substrate losses reduction at circuit level.

While *little reduction in noise figure (up to* 0.06 dB*) for the designed LNA with a low-loss Si substrate* is expected from simulation analysis, *a substantial improvement can be expected for the designed PAs*. Indeed, the approximately 0.5 dB and 0.7 dB reductions in insertion loss of the output matching network and 90° hybrid coupler, respectively, thanks to the low-loss HR substrate, have a direct impact on the PAs' output power and efficiency. Even though a re-design of the PAs might be necessary to avoid stability issues (and correct unexpected behaviors as discussed in **Section 5.3.2** related to an earlier compression of the driver stage) and experimentally confirm the expected improvements, increases of 0.5 dB, 0.8 dB and 4 %, 5 % in P_{sat} and peak PAE for PA1, PA2, respectively, are demonstrated via simulations in CW large-signal conditions. Furthermore, 5G modulation signal simulations show a significant 0.6 dB and 1.3 % improvements in average P_{out} and efficiency for a target 5.5 % EVM.

These strong performance improvements in FD-SOI-based PAs are promising to narrow the existing performance gap between PAs in FD-SOI and PD-SOI (best-in-class CMOS-based PAs) technologies. It also opens the path to the investigation of other types of RF and mm-wave circuits or topologies that could benefit from improved RF substrate quality, to ultimately *motivate the adoption of high-resistivity substrates in industrial UTBB FD-SOI technology*.



7. Conclusion and Perspectives

FD-SOI technology, featuring high RF and mm-wave performance, together with high-integration density and new opportunities enabled by the back-gate bias control, is already a great contender for 5G mm-wave applications and beyond. Furthermore, the current technology's state leaves room for improvement at RF and mm-wave frequencies, in particular with respect to the standard resistivity substrate. This thesis has studied in a systemic way how and to which level FD-SOI technology can benefit from a low-loss silicon substrate at mm-wave frequencies.

Due to the high-frequency nature of this subject and the high sensitivity of the effects to be characterized, addressing it in a complete and accurate way has required to address several characterization and design challenges, related to different levels of an integrated circuit, i.e. low-level: substrate, active (MOSFET), passive (BEOL) devices, and high-level circuit features. These different aspects and the general topic of high-frequency technology improvement via the substrate are covered throughout this thesis' chapters.

7.1 Summary

In **Chapter 2**, we reviewed on-wafer *calibration methods commonly used* on commercial calibration substrates at mm-wave frequencies, and we showed that they *all suffer from systematic errors*. In *lumped element-based methods*

(SOLT and LRM-type) systematic errors mainly come from *user-related probe misplacement error* (already with a significant impact below 40 GHz) and from incorrect or incomplete model behavior description (usually dominant above 40 GHz).

We also demonstrated that *even the benchmark mTRL method performed on commercial calibration substrates also suffers from significant systematic errors* due to the assumptions of zero substrate losses and dispersionless CPW lines not being valid for the lines on the tested substrates in the whole measured frequency range (up to 110 GHz). These systematic errors, which have been identified in the reference impedance of the calibration, propagate after measurement correction and thus degrade the final measurement accuracy. The identification of these errors' origin and their reduction are novel results, and they have been essential to quantify some very sensitive parameters in the following of the thesis.

Chapter 3 has tackled the challenges related to *low levels of substrate loss characterization*. Building on **Chapter 2** results, we showed how the residual systematic error from probe misplacement during calibration process degrades the accuracy of substrate loss extraction and can lead to meaningless values. We proposed the *R-based method to correct the measurements and compensate for potential calibration-based errors*. It works relatively well for substrates with a moderate amount of loss, but it does not for low-loss substrates.

Therefore, we proposed *another direct extraction procedure for substrate loss parameter evaluation from lower frequency data* that is more reliable (less impacted by residual systematic errors). Its application to different *Si-based substrates* demonstrated that (except for one sample fully processed in our facilities) *conductive losses still dominate the overall substrate loss mechanisms*, which include dielectric losses in the frequency range used for extraction. In other words, we showed that dielectric losses are still negligible compared to conductive losses up to $\sim 15-20$ GHz, even for substrate effective resistivity above 10 kΩcm.

The *identification of mTRL as reference calibration procedure* from **Chapter 2** *has improved the frequency range for reliable effective resistivity extraction* up to $\sim 10-15$ GHz in case of very low-loss silicon substrate (with $\rho_{eff} > 10$ kΩcm). Finally, evaluation of the extraction procedure's accuracy according to the amount of substrate loss characterized showed that *a good extraction can still be achieved up to* $\sim 50-60$ GHz *for* ρ_{eff} *values of several*

100 Ω cm, in spite of the presence of residual systematic errors.

The work developed in this chapter and the previous one has thus been fundamental to accurately assess substrate losses at mm-wave frequencies. The pertinence of substrate loss characterization in this thesis is either direct, i.e. applied to the substrates presented in the final chapter, or indirect: via the characterization of a wide variety of substrate solutions that have been developed upstream targeting successful integration with FD-SOI technology (and not shown in this thesis).

Chapter 4 dealt with *accurate FD-SOI MOSFET characterization and model verification up to* 110 GHz, which is crucial for circuit design and further technology improvement. On the one hand, the chapter included wideband (from 100 kHz to 10 GHz) frequency characterization to *capture self-heating and substrate (drain-source coupling via the substrate) effects*. Since these two effects occur in the same frequency range for FD-SOI devices, an original technique has been proposed and successfully applied to unambiguously extract both effects for the first time in an FD-SOI transistor. Furthermore, we have shown that this technique extracts self-heating parameters with a much better accuracy (error lower than 20 % in thermal parameters extraction) than the usual methods (error can be as high as 60 %), which neglect the substrate effect.

On the other hand, the high frequency characterization presents different challenges related to measurement uncertainties due to probe-dependent and calibration errors. With a careful *'in-situ' calibration*[1] *procedure* performed on custom-designed standards, we achieved an *accurate MOSFET characterization up to* 110 GHz*, with as little as* $< 5\,\%$ *variation in the expected frequency response of some extrinsic parameters (source and drain resistances, transconductance, gate capacitance, cutoff frequency) up to* 110 GHz.

By comparing the measured wideband behavior of the FET with the process design kit compact model, besides the excellent agreement achieved in general, we mainly noticed as discrepancy an underestimation in self-heating effect, which might lead to inaccurate circuit design, and its impact was verified in the subsequent chapter at circuit level.

Chapter 5 presented the design and results of a *39 GHz low-noise amplifier*

[1] As explained in **Chapter 4**, in-situ calibration is a calibration realized on the same chip as the dut measurements, i.e. on standards sharing a similar environment than the dut, such that the dut and calibration standards are measurement under similar conditions.

and two 24-43 GHz power amplifiers in the 22 nm FD-SOI technology. Their design was first introduced, then their performance were characterized, with a special focus on their behavior with back-gate bias modulation. In their peak performance condition, they exhibit a noise figure as low as 2.5 dB for the LNA, saturated output power of 20.1 dBm and peak efficiency of 36.4 % for the PAs (for PA2 and PA1, respectively). In addition, we verified that the FET model underestimation of self-heating effect has a negligible impact on the designed circuits.

By varying the back-gate bias, we have seen that the circuit operating condition (or operating class for the PAs) changes, so that *we can trade-off noise, gain and linearity for power consumption for the LNA, and AM-AM for AM-PM distortion for the PAs*. Via 5G modulation signal simulations and measurements of the PAs, we have shown -for the first time to the best of our knowledge- how the system-level error vector magnitude figure of merit behaves with back-gate bias modulation. We have further shown that the back-gate bias can be fine tuned to *maximize the average output power and efficiency for a given EVM value*.

Thanks to a benchmarking to the state of the art in (SOI) CMOS technologies, we have demonstrated that, even though the designed circuits do not outperform the state of the art, *they are in line with the best-in-class circuits*. They are therefore pertinent circuits to quantify the degree of improvement that could be achieved with reduced substrate losses in FD-SOI technology.

Finally, **Chapter 6** evaluated the performance gains an FD-SOI technology can achieve with a substrate of higher resistivity. *The novel PN pattern interface passivation solution* -developed in our laboratory **[19]**- *is applied to the 22 nm FD-SOI technology fabricated on high-resistivity substrates* for the first time. It is shown that the *parasitic surface conduction effect*[2] *is locally and effectively cancelled, and a high effective resistivity is retrieved* in an industrial UTBB FD-SOI technology.

Experimental results demonstrated substrate loss and substrate-induced harmonic distortion reduction with this passivation solution. Additional benefits of lower substrate coupling and quality factor enhancement of passive devices have also been shown with these HR substrates. The observed increase in passives quality factor (up to $\sim 60\,\%$ for some inductor geometries) is particularly interesting for potential circuit-level improvement.

[2] See **Chapter 1** and **Chapter 3** for the explanation of this effect.

While *little reduction in noise figure for the designed LNA with a low-loss Si substrate* is expected from simulation analysis, *a substantial improvement is expected for the designed PAs*. Indeed, thanks to substrate-induced insertion loss reduction in passives present at the output matching network and power combiner, 4 %, 5 % *and* 0.5 dB, 0.8 dB *increases in peak PAE and saturated output power could be achieved in the designed PA1, PA2, respectively* (evaluated via simulations). This is a strong improvement that could narrow the existing performance gap between PAs designed in FD-SOI and PD-SOI (best-in-class CMOS-based PAs) technologies.

Therefore, enhancing the substrate RF quality in an FD-SOI technology can lead to substantial improvement of mm-wave circuits. Even though it is only shown for a single type of circuits (PA) in this thesis, it is also likely valid for other circuits, or the same circuits in a different topology than studied here. This is further detailed in the next section.

All the upstream work developed throughout the various chapters of this thesis has helped in the demonstration of the above statement. Interesting new procedures have thus been developed and results have been found that deserve more discussion. Prospects concerning this upstream work are also developed in the next section.

7.2 Perspectives

This conclusive chapter is purposefully intended to reach a broad audience. So, rather general, high-level perspectives are offered here. The interested reader can find more detailed on perspectives on a specific topic in the related chapter or in appendix when specified.

7.2.1 Residual systematic errors in mm-wave measurements

The first important topic is related to on-wafer measurement accuracy in the mm-wave spectrum and beyond, and it concerns residual systematic errors still present in measurements. Their origin must first be identified to be able to reduce their effect in a second step. We can classify the encountered errors in three main categories according to in which step they appear in the measurement process.

Reference calibration

As we have seen throughout the thesis, a reference calibration is essential for accurate mm-wave measurements and characterization. However, **Chapter 2** demonstrated that calibrations performed on commercial calibration substrates contain errors, even the benchmark mTRL. Another reference calibration substrate is therefore crucial to accurately pre-characterize the commercial calibration substrate standards. Such a reference substrate could be the one presented in **Section 2.5.3** from which CPW lines measurements on top of a metallic chuck yield encouraging results up to 90 GHz, free from dispersion and radiation, but with some ripples. More investigation to reduce the ripples is needed, and is further discussed in the next paragraph.

Ripples in CPW line measurements

some residual errros must still be removed or reduced as discussed in Chap 3.

To achieve an accurate substrate loss characterization at mm-wave frequencies, some residual errors must still be removed or reduced as discussed in **Chapter 3**. Indeed, mainly two remaining errors have been identified. A first error is associated to the first-tier, 'reference' calibration discussed above. A second error causes ripples in measurements and prevents accurate extraction above 10-20 GHz for substrate effective resistivity above a few kΩcm.

The origin of these ripples is discussed in **Section 3.5.2**, likely being either related to the measurement setup hardware, or to undesired substrate modes propagation excited by the RF probes. The identification of the errors' origin requires further investigation. According to its origin, reduction of the ripples might not be straightforward and require unconventional changes to the measurement setup.

So, a change in the extraction paradigm might be necessary to further increase the substrate loss extraction accuracy. Since the current evaluation of transmission line characteristic impedance is very sensitive to errors, different methods to extract it should be envisaged. Two methods already proposed in the literature seem promising: via full-wave EM simulations **[109]** or via a numerical-model-based optimization **[110]**. They are further discussed in **Section 3.5.3**.

Probe-dependent residual errors in IC chips

The last type of systematic error degrading the measurement accuracy was encountered in MOSFET characterization up to 110 GHz in **Chapter 4**, **Section 4.1**.

Some probe-dependent residual errors are still present in high frequency measurements and might lead to wrong or inaccurate MOSFET model parameter extraction. Although a high accuracy is achieved for most relevant parameters below 70 GHz, significant residual error induces a larger uncertainty for R_g (and f_{max}) and in general above 70 GHz. These probe-dependent errors have been identified in **[40]** to mostly come from un-wanted probe coupling with the on-wafer environment and probe to probe crosstalk. Two common strategies exist for dut and calibration standards layout design, which yield parasitic effects of different nature. They are further discussed in **Appendix H**, which also contains a more detailed description of perspectives for this type of measurement error.

The main recommendations to reduce these parasitic effects consists of spacing the structures by a large distance (from each other and from the chip edge) of $\sim 800\,\mu m$ to avoid parasitic coupling. However, this spacing is too large in practice for advanced CMOS technology as the chip area is proportional to the chip price. So, we might need to change the way we approach the problem.

Another way to deal with such parasitic coupling effects would be to include them in the calibration process, thus improve measurement accuracy. As briefly mentioned in **Chapter 2**, the 16-term error model should account for all possible port leakages and crosstalks. A simplified version and a full version have been applied to on-wafer measurements in **[31]** and **[213]**, respectively, showing improved measurement accuracy.

In parallel, another interesting approach to investigate is via extensive 3D EM simulations of the whole measurement environment, i.e. including an accurate 3D model of the probes, the whole chip and its test structures. This approach is extensively used by Fregonese *et al.* **[214]** with good measurement-simulation agreement for Si-based device at mm-wave and sub-THz frequencies. In this case, the measurement accuracy is not improved, but rather the pertinence of the simulation and measurement comparison.

Finally, due to the probe-dependent residual errors identified in all of the above measurement steps (first-tier calibration, substrate loss extraction, MOSFET characterization) that overall deteriorates measurement accuracy at high frequencies, it is also worth investigating the fabrication of new RF probes. As indicated in **[215]**, the design of RF probes has a strong impact on the associated residual errors, and with a careful probe structure engineering such detrimental effects could be reduced.

7.2.2 Further applications of ZTC-based self-heating parameter extraction

The new self-heating extraction approach developed in **Chapter 4**, **Section 4.2**, uses the zero-temperature-coefficient bias to properly characterize self-heating and substrate effects in an unambiguous way. A highly accurate extraction of self-heating parameters was demonstrated for a wide range of dissipated power levels. A MOSFET model including substrate and back-gate nodes was also extracted. Nevertheless, the validity of some back-gate- and substrate-related extracted parameters is questionable, as they do not agree with tcad simulations and preliminary 4-port measurements. Extraction of a more accurate and meaningful substrate and back-gate networks deserves further investigation either via a more representative distributed model as in **[164]**, or better with measurements of multi-port devices (> 2 ports) offering a larger amount of fitting parameters.

Even though the substrate and back-gate parameters extraction could be improved, the presented self-heating and substrate effects extraction method (and other aspects developed after) has demonstrated to be particularly interesting for the following points.

- To quantify the substrate effect (in this case, although it could be used for any other phenomenon inducing a frequency transition in the measured Y-parameters, such as floating body effect in PD-SOI technology) and unambiguously extract thermal parameters.
- To verify the assumption of power-, temperature- and therefore bias-independent thermal resistance and impedance (respectively R_{th} and $Z_{th}(f)$).
- To potentially extract the heat capacity at constant pressure property of materials present in the heat evacuation path.
- To extract a small-signal equivalent circuit of the back-gate and substrate nodes from 2-port measurements (at the zero-temperature coefficient bias).
- To extract temperature- (and power-) dependent R_{th} and $Z_{th}(f)$ profiles at cryogenic temperatures. As shown in **[115, 137]**, R_{th} is not constant with the device temperature at cryogenic temperatures. This method could therefore be applied at cryogenic temperatures to extract R_{th} and $Z_{th}(f)$ profiles as a function of device temperature with a wide and uninterrupted range (at different V_g biases) instead of a few points as in **[137]**.

7.2.3 Circuit performance enhancement via back-gate modulation

The unique feature of back-gate biasing available in UTBB FD-SOI technology opens new opportunities for RF circuits. As explained in **Chapter 5**, the back-gate terminal can be seen as a tuning knob that changes the circuit operating condition. It has attracted the attention of the RF community only recently, with few publications **[216–218]** that are mostly focused on *static variations of the back-gate bias* and report similar trends as the ones discussed in **Chapter 5**.

Application of *dynamic variations of back-gate bias* is more scarcely found at RF, in spite of its potentially huge impact on circuit performance. Indeed, dynamic control of the back-gate voltage, also called adaptive body-biasing (ABB), has already been implemented in digital and analog circuits, allowing (i) to dynamically trade-off power consumption for speed, (ii) to adjust for process, voltage and temperature variations **[219, 220]** and (iii) to compensate for aging degradation **[221]**. Instead, to the best of the authors' knowledge, the only use of adaptive back-gate biasing in the RF domain up to now[3] is presented in **[205]**. In this paper, the authors apply ABB to a power amplifier to improve linearity thanks to a reduction of the third harmonic output power, hence 3rd order intermodulation products, and it is used to reduce the amount of back-off power for high-order modulations, thereby increasing the average output power and efficiency.

7.2.4 Thermal imaging for circuit testing

Although the impact of a 30 % misestimation in device self-heating is negligible at the circuit level (cf. **Chapter 5**), heat dissipation also occurs in interconnects and passives due to resistive losses. A strong and local accumulation of heat locally increases the electrical resistance (degraded performance), modify the mechanical properties of the material and might lead to circuit failure.

Thermal effects are not necessarily a major problem when measuring on-wafer circuits (as long as some basic reliability rules are fulfilled in the design). However, thermal management is of utmost importance in a final product, especially for power amplifiers as large levels of power are in play. Furthermore, in case of beamforming, the combination of several FEMs, close to each other (determined by the spacing between antennas, proportional to the wavelength) -that can be as large as 128 to 1024 elements for base stations- implies stringent requirements in terms of power dissipation for each element, in order to comply

[3] Early 2023.

with thermal dissipation constraints of the whole beamformer.

Overall, a thermal map of the designed circuits (in particular the power amplifiers) is of interest. To this end, the thermo-reflectance technique -a contactless optical approach- is particularly interesting as (i) its maturity and high spatial resolution have already been demonstrated in the characterization of material thermal properties and circuit components [222–224], (ii) it is compatible with on-wafer probers. Moreover, this technique could also be applied to help building a heat evacuation path model for transistor self-heating and, eventually, extract the heat capacitance at constant pressure property of materials used in the FD-SOI architecture as mentioned above. Preliminary work at circuit level has already started via a collaboration in [225] and will be certainly expanded in the future.

7.2.5 Further works in FD-SOI-based circuit improvement via substrate engineering

Chapter 6 demonstrated that a substantial performance improvement in the designed FD-SOI-based PAs can be accomplished with the use of a low-loss Si substrate, whereas the potential improvement in the designed LNA is expected to be small. Extra works to complement these analyses are useful to (i) extend the analyses to other types of mm-wave circuit, (ii) experimentally confirm the expected improvements and (iii) further reduce measured substrate losses in FD-SOI technology.

Different types of mm-wave circuit

Only two mm-wave front-end module circuits have been explored in this thesis: LNA and PA, in a particular topology. Additional work is required to expand the analysis to (i) the same circuits with different topologies, (ii) or at different frequencies, and (iii) other types of mm-wave circuits.

As we have seen in Section 6.2.3, the substrate has a larger impact on passives with a larger concentration of electric field inside the substrate, i.e. unshielded passives with larger dimensions. So, circuits containing spiral inductors and transformers (e.g. LNA, PA, as well as voltage-controlled oscillator, travelling-wave switches, etc.), or CPW-line-based matching networks (distributed matching networks are usually encountered in the higher end of the mm-wave spectrum and beyond) are more prone to substrate losses. Furthermore, switches have already been shown to be particularly sensitive to the substrate quality [226].

Experimental validation

As stressed in **Chapter 6**, a meaningful comparison between the best performance achieved with a standard resistivity and a high-resistivity substrate requires two different circuit designs, each optimized according to the substrate used[4]. A newly designed chip following this double-design approach is under fabrication in the 22FDX® technology on HR substrates. This chip includes a similar PA to the presented wideband 24-43 GHz PA (PA1) and other types of circuits in order to, likely, experimentally demonstrate the expected circuit-level performance improvements with a low-loss substrate.

Further substrate loss reduction in FD-SOI

The application of the PN interface passivation solution to HR substrates on FD-SOI has resulted in effective resistivity of the order of 200 Ω cm up to 50 GHz. This achievement is already great, as it significantly reduces substrate losses. However, there is still room for improvement before achieving very low-loss levels as the ones from commercial trap-rich substrates described in **Chapter 3**. First, the same PN pattern passivation technique can still be enhanced with optimized energy levels and doses of doping implants as discussed in **[207]**. These parameters have not been optimized in the first fabrication run presented here[5].

Second, different substrate enhancement methods can be used.

- Another interface passivation technique that also uses available process steps (as the PN junctions technique) is currently under fabrication and will be soon investigated. It is also local, as it cancels out the parasitic surface conduction effect locally, not on the whole wafer. It is particularly promising at mm-wave frequencies, as it should not feature frequency-increasing substrate losses (contrarily to the PN junctions).
- Other low-loss substrate architectures compatible with UTBB FD-SOI technology can also be envisaged. We can cite:
  - the double BOX technique **[18]**, which consists of a trap-rich layer underneath a thin oxide layer fabricated below the back-gate doping

[4] Lower metallic losses can generally be achieved in passives on a HR substrate due to its negligible substrate losses, while a trade-off between substrate and metallic losses must be found for std substrate. In practice, the designer can more easily stack metal lines and end up with a larger concentration of electric field in the subtrate with a HR substrate thanks to negligible substrate losses.

[5] Additional split-process runs are being fabricated with different doping implant conditions to find an optimum for this technology.

wells;

- the post-process porous Si method, which porosifies the Si substrate locally (under some desired regions, such as passive elements) *after chip fabrication*. Porous Si is very interesting, because, in addition to yield negligible substrate losses, it also reduces the substrate permittivity, thus reducing capacitive couplings that are even more detrimental the higher the frequency. Furthermore, this post-process and local fabrication technique offers the advantage of avoiding or reducing the negative side effects of porous Si, i.e. reduced material thermal resistance and mechanical stability.

However, before being able to apply these new fabrication techniques to an industrial FD-SOI technology, further process development is needed to raise their fabrication maturity level.

7.2.6 Further technology improvement with strained channel

At last, another technique envisaged to further boost future FD-SOI technology performance and meet upcoming application requirements is strain channel engineering. It is already widely used in other advanced CMOS technologies, and even in pMOSFETs of the 22 nm FD-SOI technology [20]. Thanks to that boost, pMOSFETs with f_t and f_{max} in the range of 300 GHz can be achieved [9]. However, nMOSFETs in today's industrial FD-SOI technologies do not feature any mobility boost from strained channel.

An interesting method recently published proposes to strain channel of nMOSFETs via strain transfer structure (STS) of a SiGe buried stressor layer under the BOX [227]. In this paper, the authors estimate experimentally a mobility improvement of the order of $\sim 40-50\,\%$, which significantly boosts device-level figures of merit. These device-level improvements can also benefit to circuits and enhance their performance. A qualitative analysis for LNA and PA circuits is provided in **Appendix I**, as well as a quantitative study for the designed LNA and PA1 without re-design. It is shown that in a 20 % mobility boost scenario (limited by internal PDK compact model parameter), the LNA shows a small 0.6 dB increase in gain and negligible NF reduction (0.02 dB), but the PA1 benefits from $0.3-0.4$ dB and $1.3-1.5\,\%$ increases in P_{sat} and in peak PAE, respectively. These figures represent small improvements, but they could certainly be increased with further work involving circuit re-design and modification of the operating bias condition.

A. Paper: *New Method for Accurate Transmission Line Characterization on Low-Loss Silicon Substrate at Millimeter-Wave Frequencies*

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New Method for Accurate Transmission Line Characterization on Low-Loss Silicon Substrate at Millimeter-Wave Frequencies

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INTRODUCTION

The technological downscaling has improved the figures of merit of silicon-based technology, enabling a progressive replacement of conventional technologies at millimeter wave frequencies. The calibration and de-embedding techniques that involve on-chip transmission lines (TLs) were traditionally developed for non-conductive substrates. They need to be revised when applying them to silicon-based substrates at millimeter-wave frequencies.

The importance of accurate on-wafer probing pad de-embedding is twofold. First, their de-embedding requires the use of many dummy structures during FET characterization at high frequency (above 40 to 70 GHz depending on the device dimension), unless an accurate on-wafer calibration scheme is performed [1]. Second, different flavors of substrate are used in silicon-based technology. Their characteristics are not necessarily known after an industrial process. On-chip TLs provide a cheap and convenient method to extract those characteristics [2],[3], as long as the probing pads are accurately de-embedded.

A TL is characterized by two parameters: its propagation constant (γ) and its characteristic impedance (Zc), which enable us to calculate the lineic RLGC parameters. While the propagation constant is accurately extracted over a wide frequency range with the multiline TRL (mTRL) algorithm [4], it is very challenging to extract Zc of a TL that is mounted on a substrate of unknown conductive losses.

This paper reviews the most popular methods [5]-[13] to characterize TLs and presents a new method to extract Zc using only the measurements of lines of different lengths. The different methods are compared on the measurement of a coplanar waveguide (CPW) line. An explanation for the origin of the incorrect extraction of the imaginary part of Zc is determined based on a simulation-based analysis comparing the different methods. It is shown that the assumption of symmetric transmission elements is at fault.

METHODS FOR CHARACTERISTIC IMPEDANCE EXTRACTION

In [5], Zc is obtained from the measurement of the propagation constant and the assumption of a lossless substrate (G=0) as well as a constant value of the capacitance (C) with frequency. The other popular method from [6] considers the measured line as a homogeneous line with a perfect contact. We can also report two families of methods non-applicable to substrate characterization: (1) based on electromagnetic simulations [7] and (2) based on experimental fitting [8]. Finally, there are many methods developed for Si-based substrates. Their distinction relies on a different modeling of the transition between the probe tips and the middle of the shortest line (Thru), and on different sets of equations used to find Zc and the elements of the model. Fig. 1(b) summarizes the transition models (symmetric/asymmetric).

Presentation of the new method

The new method uses a different model of the transition displayed in Fig. 1(b). The left and right transitions are a priori asymmetric because of a different shunt admittance (Y_1 and Y_2, respectively). Analytical expressions for each shunt admittance, the Thru propagation constant (γ_t) and Zc are derived in terms of the ABCD matrix of the Thru and the transfer matrix of the error boxes. The analytical expressions and their derivation are explained in the Appendix.

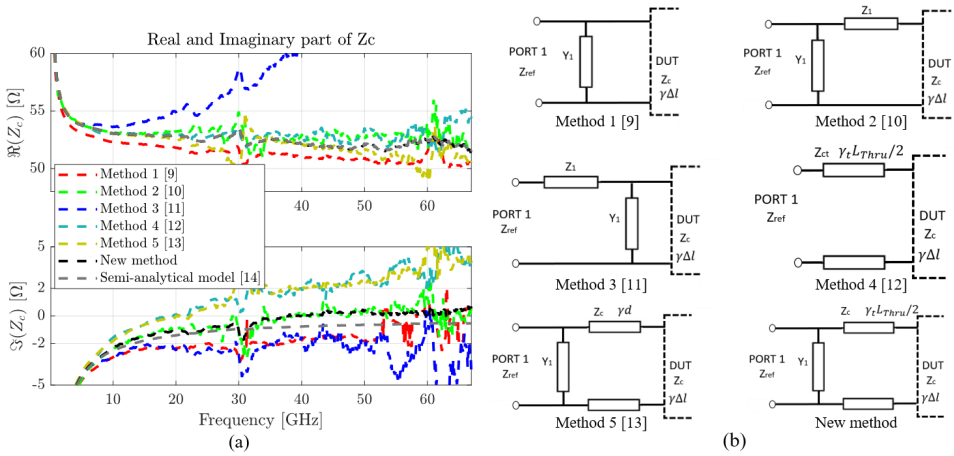


Fig. 1. Extracted characteristic impedance from CPW line measurements (a) for 6 different transition models (b).

Comparison among the different methods

CPW lines fabricated on top of a silicon-on-insulator trap-rich wafer are measured from 10 MHz to 67 GHz using an Agilent 2-port PNA-X vector network analyzer and a pair of GSG Infinity probes from Cascade Microtech. Their dimensions are a central signal width of 26 µm, a spacing of 12 µm between the signal and the ground lines. An open structure and three lines of different lengths (102.8 µm, 2102.8 µm, 8102.8 µm) are measured. A 43 µm-long taper is present between the probing pads and the line. The system is calibrated to 50 Ω at the probe tips via an SOLT calibration using an RF impedance standard substrate. The mTRL method is used to extract the propagation constant γ of the DUT. In Fig. 1(a), 6 different methods to extract Zc are compared. The resonances at 30 and 60 GHz are purely a consequence of the mTRL algorithm that is ill-conditioned around those frequencies. They could be avoided by having lines whose electrical lengths are not a multiple of a half wavelength at those frequencies. Even though almost all of them estimate well the real part of Zc, the extracted imaginary part varies quite significantly among the different methods. For most of them, the imaginary part of Zc becomes unphysically positive above a certain frequency. Indeed, as shown in Fig. 2, the equivalent *L* and *C* parameters are well estimated for almost all of the methods, while *G* and *R* exhibit an unphysical behavior above approximately 10 or 30 GHz, depending on the method. For some methods, *G* becomes negative. For others, *R* decreases with frequency whereas it should increase due to skin effect. It is related to a wrong estimation of the imaginary part of the characteristic impedance. Indeed, for low-loss transmission lines, the characteristic impedance is expressed as

$$Z_c \approx \sqrt{\frac{L}{C}} + j\frac{1}{\omega C}\left(\sqrt{\frac{L}{C}}\cdot\frac{G}{2} - \sqrt{\frac{C}{L}}\cdot\frac{R}{2}\right). \quad (1)$$

The new method provides a more accurate extraction of the imaginary part of Zc above 10 GHz compared to the other methods. The result is close to the one from method 5 [13], because a similar modeling of the transition is chosen. However, the new method outperforms it thanks to a description that is compatible with the mTRL algorithm, therefore benefitting from reduced noise and wide frequency band coverage, e.g. the resonance of 60 GHz disappeared.

Fig. 3 (a) shows the propagation constant of the Thru (dotted line) and the DUT (dashed line). As expected, the propagation constant is similar, but not exactly equal. The conductance $\Re(Y)$ and capacitance $\Im(Y)/\omega$ associated to each transition are displayed in Fig. 3 (b). While the difference in conductance is small, a difference of approximately 6.5 fF is observed in the capacitances, highlighting the relevance of the asymmetric modeling approach.

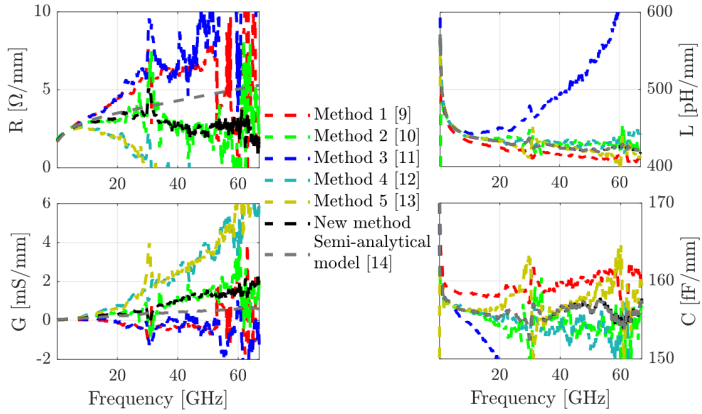


Fig. 2. Extracted RLGC parameters from CPW line measurements.

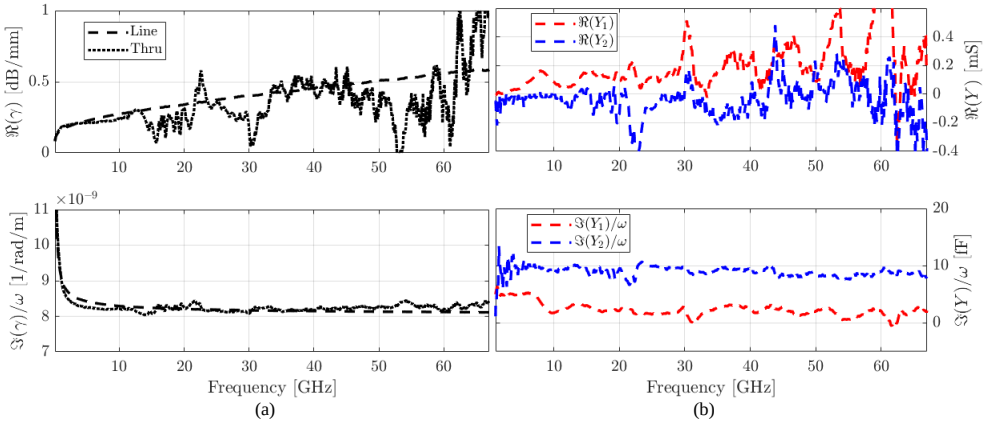


Fig. 3. Extracted transition parameters from the new method. Propagation constant of the Thru (dotted line) and the DUT (dashed line) on the left graph (a). Shunt admittance on the right (b).

TRANSITION MODELING SIMULATIONS

In order to reproduce the effect of the transition modeling, simulations using the Keysight ADS software are performed. First, the ideal DUT is simulated using the Momentum solver without transitions. Then, shunt admittances are added at both ports to create the non-ideal simulated DUT data. Finally, Zc is extracted using [6]. This approach is depicted in the inset of Fig. 4, where these shunt G and C elements model the imperfect transitions at the probe pads, reproducing the transition model 1. Transition models 2-3 and 5 (cfr. Fig. 1(b)) are also tested, but the results are not shown here, because the general conclusion remains the same. The fact that the imaginary part of Zc becomes unphysically positive above a certain frequency only occurs when the transitions are asymmetric (black lines). For symmetric transitions, an increasing imaginary part of Zc that becomes positive (above a certain frequency) is only ever obtained when a large error in its real part arises (green lines), which never occurs in practice during measurements.

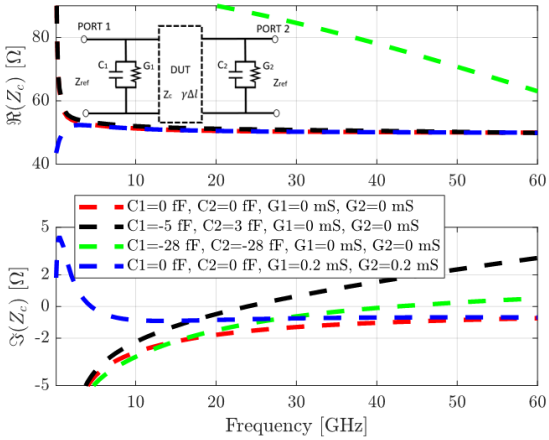


Fig. 4. Simulated characteristic impedance of the DUT including shunt admittances modeling the transitions.

CONCLUSION

A new method for the extraction of the characteristic impedance of TLs is proposed and validated through measurements. It requires 2 lines of different lengths and no reflect structure. Furthermore, its formulation is compatible with the mTRL technique, therefore benefitting from its advantages of noise reduction and wide frequency band coverage, essential at millimeter-wave frequencies. A comparison with other methodologies is carried out and an unphysical increase of the imaginary part of Zc is highlighted. Simulations demonstrate that this phenomenon origins in an asymmetry of the left and right transitions during measurements, which is taken into account by the new method. The new method can be applied to on-wafer TLs fabricated on any types of substrate, thus enabling accurate de-embedding for device or substrate characterization at millimeter-wave frequencies.

APPENDIX: DERIVATION OF THE NEW METHOD

The calibration comparison method has been the popular method for measuring the characteristic impedance of transmission lines on lossy substrates. It requires a first-tier calibration with a known reference impedance (Z_{ref}) and a second-tier calibration on the studied substrate with an unknown reference impedance. The error box obtained from the second calibration represents the differences between the two calibration substrates. Let *X* and *Y* be the transfer matrix of the left and right error boxes, respectively.

$$X \equiv \rho_x \begin{pmatrix} a_x & b_x \\ c_x & 1 \end{pmatrix}, \quad Y \equiv \rho_y \begin{pmatrix} a_y & b_y \\ c_y & 1 \end{pmatrix} \tag{2}$$

The second-tier calibration uses the mTRL method. In that case, the reference plane is located at the middle of the Thru structure and the unknown reference impedance corresponds to the characteristic impedance of the lines. The model chosen to represent the error box is displayed at Fig. 1(b). The unknown characteristic impedance of the Thru structure enables the correction of arbitrary reference plane shift due to non repeatable probes position on the pads. The parallel admittance takes into account the short stub behind the probes and the potential difference in permittivity and losses between the calibration substrates. The left and right error boxes have a priori different values of shunt admittances (Y_1 and Y_2, respectively). It is an important aspect needed to be considered for a better extraction of the imaginary part of Zc as stressed in the second Section.

While the mTRL calibration needs at least two lines of different lengths and a reflect structures, the present method does not need the reflect structure. Therefore, only the b_x, b_y, $\left(\frac{a}{c}\right)_x$ and $\left(\frac{a}{c}\right)_y$ elements are available. Two additional equations are obtained thanks to the ABCD representation of the Thru element ($ABCD_T$), such as

$$\begin{cases} B_T = Z_c \sinh\theta_T & (3) \\ D_T = Y_1 B_T + \cosh\theta_T = Y_1 B_T + \sinh^2\frac{\theta_T}{2} + \cosh^2\frac{\theta_T}{2}, & (4) \end{cases}$$

where

$$ABCD_T \equiv \begin{pmatrix} A_T & B_T \\ C_T & D_T \end{pmatrix} \text{ and } \theta_T \equiv \gamma_t L_{Thru}. \quad (5)$$

From the transfer matrix of the left and right error boxes, lengthy calculations lead to the second degree equations in Z_c which solutions are

$$\frac{Z_c}{Z_{ref}} = \frac{\left(1 + \left(\frac{a}{c}\right)_i\right)(1 + b_i) \pm \sqrt{\Delta_i}}{(1 + \cosh\theta_T)\left(\left(\frac{a}{c}\right)_i - b_i\right)}, \quad (6)$$

where

$$\Delta_i \equiv \left(1 + \left(\frac{a}{c}\right)_i\right)^2 (1 + b_i)^2 + \left(\frac{B_T}{Z_{ref}}\right)^2 \left(\left(\frac{a}{c}\right)_i - b_i\right)^2 \text{ and } i = x, y. \quad (7)$$

Taking the average from the left and right transitions and replacing Z_c in (4) gives

$$\gamma_t = \frac{2}{L_{Thru}} \operatorname{atanh}\frac{B_T}{\tau}, \quad (8)$$

where

$$\tau \equiv \frac{Z_{ref}}{2}\left[\frac{\left(\left(1 + \left(\frac{a}{c}\right)_x\right)(1 + b_x) \pm \sqrt{\Delta_x}\right)}{\left(\frac{a}{c}\right)_x - b_x} + \frac{\left(\left(1 + \left(\frac{a}{c}\right)_y\right)(1 + b_y) \pm \sqrt{\Delta_y}\right)}{\left(\frac{a}{c}\right)_y - b_y}\right]. \quad (9)$$

The two $\pm$ are independent from each other and, therefore, we end up with 4 solutions. The characteristic impedance is obtained from

$$Z_c = \frac{B_T}{\sinh\theta_T}. \quad (10)$$

Out of the 4 solutions, only 1 has to be selected at each frequency point. The selection consists of chosing the characteristic impedance that is the closest one from an initial guess. This initial guess can be obtained from another characteristic impedance extraction method. Finally, the shunt admittances are computed as

$$Y_1 = \frac{1}{Z_{ref}}\frac{1 - b_x}{1 + b_x} - \frac{1}{Z_c} \text{ and } Y_2 = \frac{1}{Z_{ref}}\frac{1 - b_y}{1 + b_y} - \frac{1}{Z_c}. \quad (11)$$

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B. Robust LRRM Calibration Procedure for Accurate Measurements

In the **Chapter 2**, we analyzed the effect of probe misplacement on standards for the LRRM calibration, but with *automatic Load inductance search disabled*. We have seen that probe misplacement on the Thru and Load standards are most problematic below 40 GHz for substrate evaluation as they strongly affect the imaginary part of the calibration reference impedance.

First, we show how the SOLT calibration reference impedance varies for the same probe misplacement on each standard. Then, we analyze how LRRM calibration reference impedance changes with again the same probe misplacement on standards *with automatic Load inductance search enabled*. Then, we also study how probe misplacement *with a constant probe-to-probe distance* on standards using the LRRM calibration affects the reference impedance. This is more representative of usual measurement conditions, where only the chuck is moved from one standard measurement to another.

Next, we show how the standards can be characterized with a minimal number of additional measurements. Finally, we propose different procedures to get a meaningful reference impedance according to the measurement conditions and requirements.

1. Measurement setup and procedure All measurements (except when explicitly mentioned) are performed with the same measurement setup as the one described in **Section 2.5.2**. It is repeated here to ease the reading. Open, Short, Load, Thru and Lines (0.45, 0.9, 1.8, 3.5, 2.25 mm) standards of the commercial AC-2 calibration substrate are measured with Ground-Signal-Ground (GSG), 110 GHz, 100 µm-pitch, MPI TITAN^{TM} probes and a Keysight N5291A VNA from 200 MHz to 110 GHz, with 100 Hz IF bandwidth and -5 dBm power at the VNA, on a semi-automatic MPI probe station, with East motorized posi-

tioner PMP80. The AC-2 substrate is placed on a ceramic chuck.

For the standards definition needed in the LRRM and SOLT calibration algorithms, each standard is preliminary characterized based on an mTRL calibration to compensate for manufacturing inaccuracies and variations in probe placement with respect to AC-2 substrate specifications. The extracted standard parameters are summarized in **Table 2.1**.

For all experiments in this appendix, raw measurements are saved for post-processing. The first-tier calibrations are performed with WinCal XE software. The second-tier calibration and subsequent post-processing is realized with in-house Matlab scripts implementing the mTRL algorithm described in **[37, 55]**. When available, the per-unit-length C term of transmission lines is determined with the Load method **[67]** explained in **Section 2.3.6** and confirmed with the calibration comparison method. Otherwise, the C term is directly obtained from the calibration comparison technique.

B.1 SOLT Sensitivity to Probe Misplacement

First, let us analyze the sensitivity of SOLT reference impedance to probe contact misposition. For the same contact variations as described in **Section 2.5.2** for the LRRM: the left probe (probe 1) contact position is varied by $\sim$10 µm to the right (toward the right probe) on each standard. **Figure B.1** shows the extracted Z_{ref} for an SOLT calibration performed with (i) measurements with no variation in contact position ('Nominal' in legend, red lines), (ii) measurements where contact position varies from the nominal contact for a single standard only (alternately the 'Load', 'Short' and 'Thru', in legend), (iii) measurements with varied contact position on all standards ('All standards' in legend, yellow lines).

As for the LRRM, SOLT Z_{ref} is most sensitive to probe contact misplacement on Thru and Load standards. However, the variations in $\mathrm{Im}(Z_{ref})$ are smaller up to 45 GHz than for LRRM: up to $+0.65\,\Omega$ for SOLT and $-0.95\,\Omega$ for LRRM (cf. **Section 2.5.2**, **Figure 2.14**). Whereas, when the same contact position (even if it is different from the nominal position) is used for all standards (yellow lines), the error in Z_{ref} is greatly reduced (as it was also the case for LRRM).

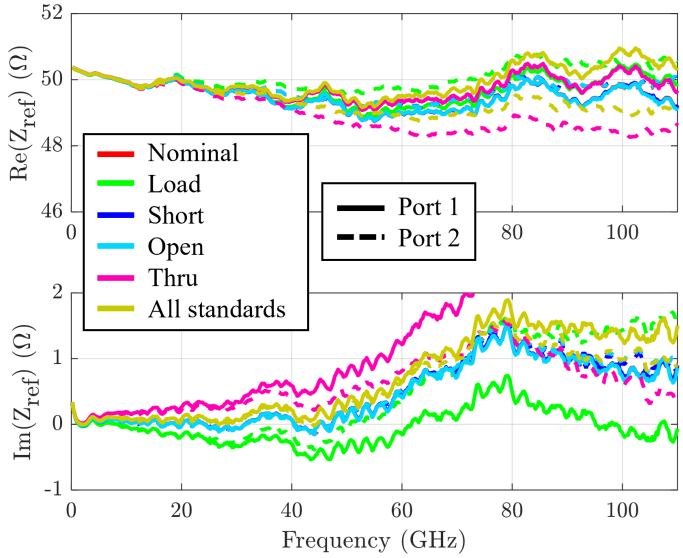


Figure B.1: $Z_{ref1,2}$ of SOLT calibration with different left probe placement on pad. Nominal position on all standards measurements in red lines. Variation of probe position from nominal in only one standard measurement: green, blue, cyan lines. Variation of probe position in all standards measurements in yellow lines.

B.2 LRRM With Automatic Load Inductance Search

In **Chapter 2**, when we have used LRRM, the automatic Load inductance search (also called 'auto-search' in the following for brevity) algorithm was disabled. This automatic Load inductance search (in LRRM) consists of an optimization algorithm and complicates the Z_{ref} dependence on measured standards. It was disabled for the previous experiments to ease results interpretation. However, the LRRM calibration uses this Load inductance search algorithm by default within the WinCal XE calibration program. It is therefore important to study how the full LRRM algorithm (including this Load inductance search) behaves when probe misplacement is present to get closer to usual measurement conditions. Therefore, the same experiment (with identical probe misplacement on standards) as above is repeated for the LRRM with automatic Load inductance search and shown in **Figure B.2**. The L_{load} term used by the LRRM calibration (and found with the automatic search) is shown in the caption for each case.

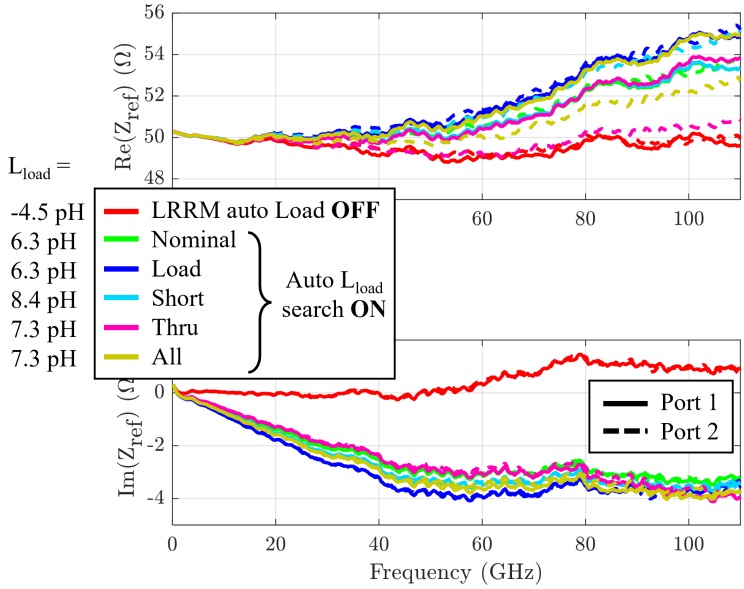


Figure B.2: $Z_{ref1,2}$ of LRRM calibration with automatic Load inductance search enabled, for different left probe placement on pad. Nominal position on all standards measurements in green lines. Variation of probe position from nominal in only one standard measurement: blue, cyan, pink lines. Variation of probe position in all standards measurements in yellow lines. LRRM with auto-search disabled (red lines) has been added for reference.

Several observations can be made out of **Figure B.2**.

1. First, all calibrations with automatic Load inductance search show a clear deviation in $\mathrm{Im}(Z_{ref})$, due to a very different L_{load} term calculated by the auto-search from the extracted value of L_{load} from mTRL. Indeed, the L_{load} can be extracted from the Load standard measurements corrected by the reference mTRL calibration and is shown in **Figure B.3a**. The automatic Load inductance search algorithm as described in **[57]** searches a value of L_{load} that yields a radiation-less corrected Open measurement. In other words, it finds an L_{load} value that yields a corrected Open measurements with $|S_{11}|$ and $|S_{22}| \approx 0\,\mathrm{dB}$ across the whole frequency range.

Corrected Open reflection coefficient measurements are shown in **Figure B.3b** with different calibrations. We observe that the LRRM with auto-search disabled does not feature $|S_{11}|$ and $|S_{22}|$ close to 0 dB, while it is the case for

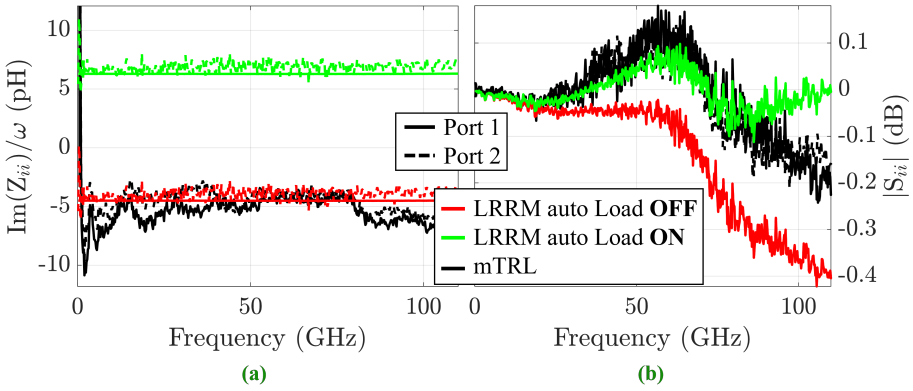


Figure B.3: Measurements of Load (a) and Open (b) standards with nominal contact position corrected by different calibration methods (mTRL, LRRM with and without automatic Load inductance search). Measurements with TITAN probes on AC-2 substrate.

mTRL and when auto-search is enabled. Nevertheless, the value found for L_{load} with automatic Load inductance search is very far from what is measured by mTRL (hence the deviation in $\mathrm{Im}(Z_{ref})$). This is very likely related to the fact that the auto-search algorithm requires a model for some standards. Since the TITAN probe and AC-2 calibration substrate are not known by WinCal XE, the software uses wrong pre-defined standards model that depends on both the probe and calibration substrate used. As there is no easy way to define it inside WinCal XE for common users, *using LRRM with automatic Load inductance search with WinCal XE and probes or calibration susbtrates that are not defined within can lead to a wrong calibration*. In that case, it is better to either disable the auto-search algorithm (and use the values specified by the probe manufacturer) in LRRM or to use a different calibration technique (such as mTRL).

The above problem does not occur for the tested Infinity probes (I110). Z_{ref} of LRRM with and without automatic Load inductance search are shown in **Figure B.4**, along with corrected Open reflection coefficient measurements. In this case, the L_{load} value is similar (less than 1 pH variation) and the $|S_{11}|$ and $|S_{22}|$ are close to 0 dB for the value measured with mTRL and the auto-search algorithm with LRRM.

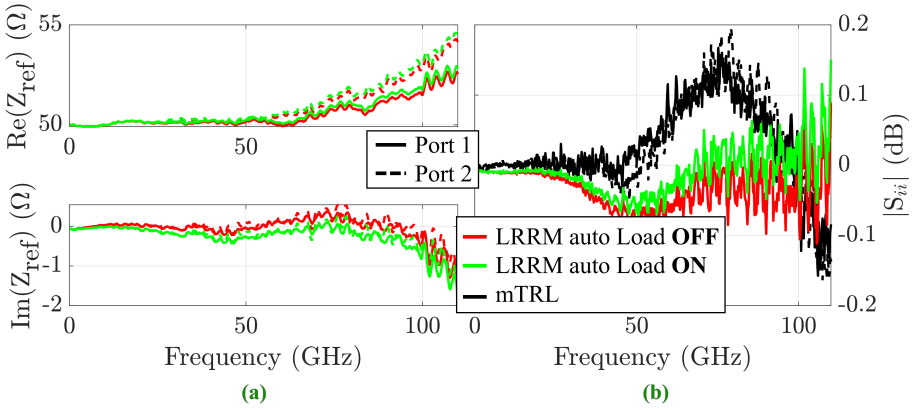


Figure B.4: ***I110 probes*** *measurements on 104-783A substrate*. Evaluated Z_{ref} (a) and Open standard measurements (b) with nominal contact position for different calibration methods (mTRL as reference for Z_{ref}, LRRM with and without automatic Load inductance search).

2. Second, concerning the variations due to probe misplacement on the standards, similar observations are made to the case when auto-search is disabled (shown in **Figure 2.14** and explained in **Section 2.5.2**). Namely they are:

- A contact position variation on the Load standard causes a significant variation in $\mathrm{Im}(Z_{ref})$ (below 45 GHz) of a similar intensity as the LRRM with auto-search disabled: up to $-\sim 1\,\Omega$. The auto-search algorithm does not depend (or weakly) on the measurement of the Load standard as the L_{load} is unchanged from the nominal case.
- An incorrect position on the Thru standard leads to deviations in $\mathrm{Re}(Z_{ref,1}) \neq \mathrm{Re}(Z_{ref,2})$, as well as a different L_{load} value.
- The contact position on the Short standard is also important as it also modifies the computed L_{load} value and $\mathrm{Im}(Z_{ref})$ mostly below 60 GHz.

The above observations have been confirmed experimentally for the TITAN probes on the AC-2 substrate (thus with the systematic deviation in L_{load} and $\mathrm{Im}(Z_{ref})$ due to wrong standard models in WinCal XE). Similar sensitivities with I110 probes have been observed when performing calibration, such that we could likely generalize these observations for different probe technologies, even though additional rigorous measurements are needed to confirm them (e.g.

I110 with appropriate standard model definitions in WinCal XE).

In the above sensitivity variations, the probe-to-probe distance is not equal for all standards. Such an error can only happen when the user moves the probes from standard to standard. It does not occur when the chuck is moved (which is more representative of manual probe stations). So, let us analyze the effect of a wrong contact position on different standards when the probe-to-probe distance is constant. **Figure B.5** illustrates the position of two contacts with equal probe-to-probe spacing. **Figure B.6** shows Z_{ref} and computed L_{load} for the different contact variations of the LRRM calibration with auto-search enabled.

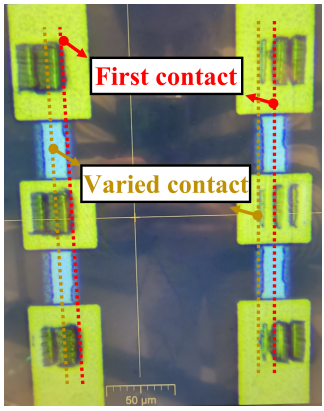


Figure B.5: Illustrations of different contact positions on the Load standards with contact probe-to-probe spacing, which is a typical error that can be made on manual probe stations. 'First contact' corresponds to the position 'Probe L $+10\,\mu$m'. 'Varied contact' corresponds to 'Probe R $-10\,\mu$m'.

We again see that $\mathrm{Im}(Z_{ref})$ is very sensitive to the probe position on the Load and Thru standards (up to $+0.85\,\Omega$ and $-0.5\,\Omega$ error at 40 GHz). However, we also see that if the Load and Thru standards are measured with the same probe contact position, $\mathrm{Im}(Z_{ref})$ is well calculated (close to the nominal measurement case).

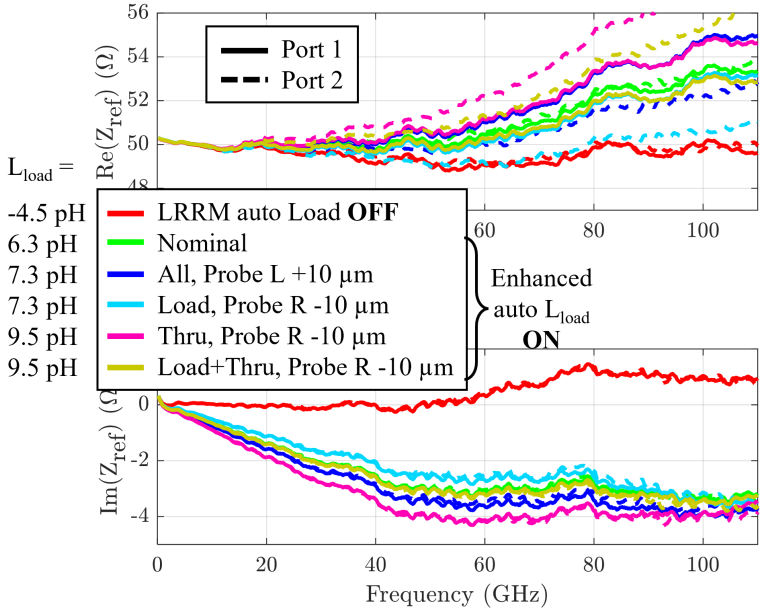


Figure B.6: $Z_{ref1,2}$ of LRRM calibration with automatic Load inductance search enabled, for different probe placements on pad (constant probe-to-probe spacing). Nominal position on all standards measurements in green lines for reference. 'Probe L $+10\,\mu$m' contact for all standards in blue. Variation of probe position from 'Probe L $+10\,\mu$m' in only one or two standards measurement: cyan, pink and yellow lines.

Finally, let us analyze the case when the contact position on all standards is the same, such that the user makes an error when aligning the probes. This is rather the case when a (semi-)automatic probe station is used. The sensitivity of Z_{ref} is shown in **Figure B.7**. In this case, we observe that the error on $\mathrm{Im}(Z_{ref})$ is still present but reduced compared to the case when the probe are incorrectly positioned on a single standard: up to $+SI0.2\Omega$ and $-0.45\,\Omega$ error at 45 GHz.

So, *even with the auto-search algorithm enabled, the reference impedance of the LRRM calibration is sensitive to probe contact position on standards, in particular on the Load standard, and when the position varies only for one standard.* Therefore, special care has to be dedicated when performing on-wafer calibrations, otherwise the calibration reference impedance used might lead to erroneous results.

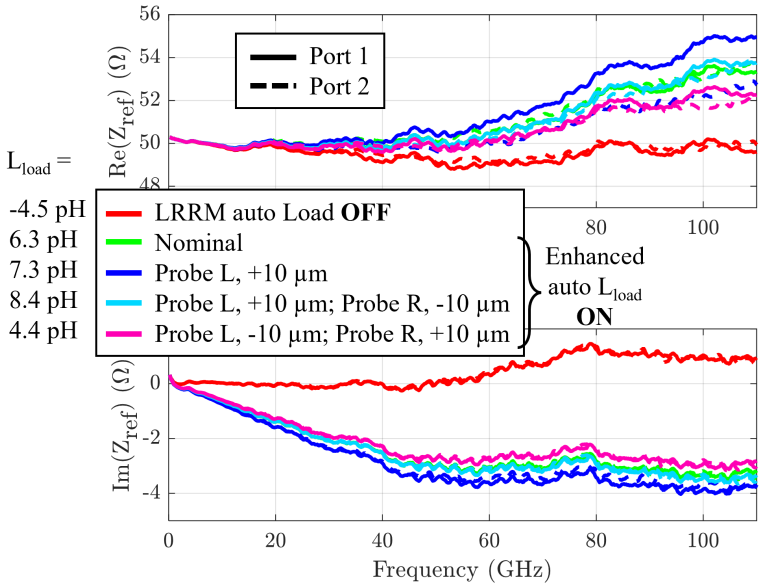


Figure B.7: $Z_{ref1,2}$ of LRRM calibration with automatic Load inductance search enabled, for different probe placements on pad (constant position for all standards, e.g. semi-automatic probe station). Nominal position on all standards measurements in green lines. 'Probe L $+10\,\mu$m' contact in blue lines (see 'First contact' in **Figure B.5**).

In the following we will explore different ways to perform a good lumped-based calibration that yields a correct reference impedance.

B.3 Contact Position Verification

As we have seen above, a good contact position on standards is crucial for a correct Z_{ref} of lumped-based calibrations (SOLT and LRRM). So, we propose here methods to verify the contact position on the different standards.

B.3.1 Load

The contact position on the Load is critical, as this element defines the reference impedance calibration [36]. In particular, the inductance term (*L-term*) defines the low-frequency (up to $\sim 40-50\,$GHz) behavior of $\mathrm{Im}(Z_{ref})$ and is very sen-

sitive to the probe contact position[1]. So, it is essential to characterize this term, which can be done via a (m)TRL calibration. Corrected Load standard measurements (with non-ideal contact position alignment) with an mTRL calibration are shown in **Figure B.8**. A minimum of two Lines (in addition to the Thru) is needed to get a good extraction with limited frequency variation, and the L_{term} can be extracted by averaging $\mathrm{Im}(Z_{ii})\omega$ from ~ 20 to 50 GHz. When the contact position on both Loads is not symmetric, different L_{load} can be extracted from port 1 and 2 as shown in **Figure B.8**. In this case, the Load measurements should be repeated for a good calibration to be obtained. Nevertheless, we can still have a $\mathrm{Im}(Z_{ref})$ that is rather well defined by taking an average on the values from ports 1 and 2 and use it as L_{load} in LRRM.

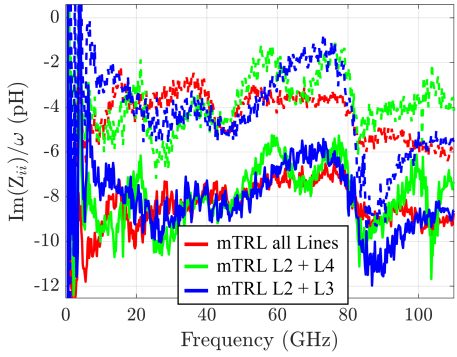


Figure B.8: Measured L_{load} term of Load standards with an incorrect probe contact position on port 1. Measurements corrected with different mTRL calibrations, either all Lines (red) or some of them (green and blue). L2, L3, L4 have lengths of 900 µm, 1800 µm, 3500 µm, respectively.

B.3.2 Thru

As we have seen in **Section 2.5.2**, $\mathrm{Re}(Z_{ref,1})$ and $\mathrm{Re}(Z_{ref,2})$ significantly diverge from each other when an asymmetric contact is made on the Thru standard. So, this result can be used to check the contact symmetry on the Thru. We only need a TRL calibration (with any line length) to get a good estimation of the contact symmetry as shown in **Figure B.9**.

[1]The Load impedance depends on the EM fields of the mode incident upon the device [36]. So, it is reasonable for its imaginary part to be sensitive to the probe contact position on the standard.

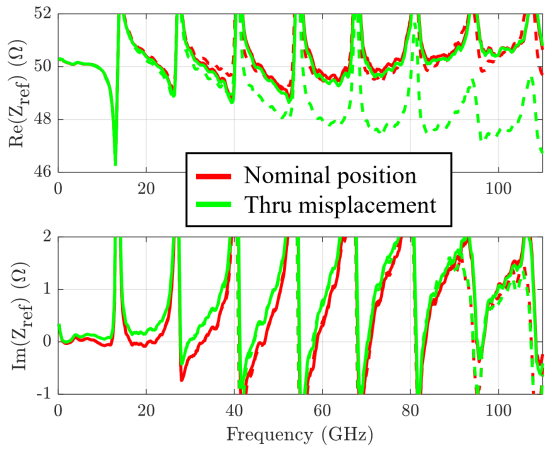


Figure B.9: Evaluated Z_{ref} of LRRM calibration using only TRL (with the 5250 µm-long Line standard) as reference second-tier calibration. Nominal probe contact position on all standards in red lines, incorrect (asymmetric) probe placement on Thru standard in green lines.

B.3.3 Short

It is usually modeled (available model in WinCal XE) by a constant inductance term, which value can be extracted from (m)TRL corrected measurements. In this case, a TRL with the shortest line (L1) is sufficient as shown in **Figure B.10**. Note that an incorrect model of the Short or probe position on the Short leads to smaller errors in Z_{ref} as we have seen previously.

The Open standard measurements show negligible variations up to 110 GHz when the probe contact changes on the standard. Thus, it does not induce any significant variations on the reference impedance of the calibration. Nevertheless, its model is required for SOLT calibration, which can be extracted in a similar way as the Short standard described above.

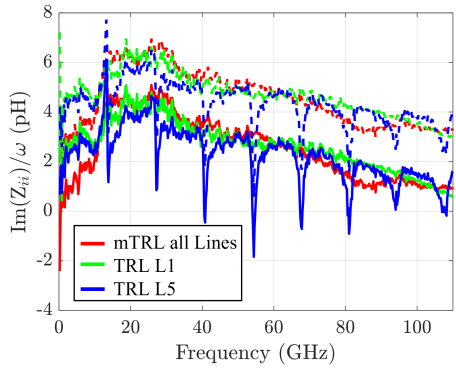


Figure B.10: Measured L_{short} term of Short standards with asymmetric probe contact position. Measurements corrected with mTRL and different TRL calibrations. L1, L5 have lengths of 450 µm, 5250 µm, respectively.

B.4 Good Calibration Procedure

Let us summarize the above results and propose different calibration procedures according to the measurement conditions and needs.

As we have seen above, all lumped-based calibration methods have a reference impedance that is sensitive to the probe position on standards. The error made on Z_{ref} is reduced when all standards are measured with the same contact position, which can be easily realized on a (semi-)automatic probe station. Still, a good SOLT or LRRM calibration requires a correct model for each standards. However, to identify a correct probe contact position and/or standard electrical model, a (m)TRL calibration is necessary (with at least two different Lines for the Load standard). So, a high-precision SOLT or LRRM calibration requires measurements of additional Line standards, such that the lumped-based calibration becomes cumbersome and irrelevant compared to the mTRL.

Therefore,

- When using a (semi-)automatic probe station, SOLT and LRRM can be used knowing that they can suffer from a little, yet significant, error in $\mathrm{Im}(Z_{ref})$. This error can be reduced with prior characterization of the electrical behavior of the standards (using mTRL calibration), which could be performed once in a while, as long as the user uses the *same contact position* in future calibrations (which requires some training and discipline from the user).
- Use only LRRM with automatic Load inductance search enabled for calibrations made with probes and calibration substrates available in the calibration software. Otherwise, there might be an error in the evaluated L_{load} term that leads to inconsistent $\mathrm{Im}(Z_{ref})$.
- When using a manual probe station, due to the higher probability of systematically making an error in probe contact position, we would recommend a common user to directly perform an mTRL calibration for measurements requiring a highly accurate Z_{ref} (for substrate characterization for instance as in **Chapter 3**).
- For the specific case of substrate losses characterization (effective resistivity extraction), an SOLT or LRRM (with automatic Load inductance search disabled), could be used for measurements. In that case, we propose to tune the L_{load} term used in the calibration by measuring the effective resistivity of a reference sample and find the L_{load} value yielding the expected behavior of $\rho_{eff}(f)$.

For the last point, CPW line measurements of a reference wafer are required (e.g. the eSI90 calkit sample presented in **Chapter 3** and featuring a constant effective resistivity up to $\sim 10-20\,\mathrm{GHz}$). This correction in L_{load} value for the calibration can be performed post process, as long as the measurements of the calibration standards and the first calibration error terms are saved. It should be noted that the 'corrected' calibration is not highly accurate (as $\mathrm{Re}(Z_{ref,1})$ could be different from $\mathrm{Re}(Z_{ref,2})$ if the Thru standard is measured asymmetrically for instance), but it provides a good $\mathrm{Im}(Z_{ref})$ close to $0\,\Omega$ up to $\sim 45\,\mathrm{GHz}$, which is sufficient for substrate effective resistivity characterization. Furthermore, it offers a faster calibration procedure than the mTRL calibration in a manual probe station, as measurement of a reference sample is usually part of measurement the campaign.

C. Procedure for High Contact Quality Verification

Contact quality is of uttermost importance for on-wafer S-parameter measurements. It can be monitored via dc measurements, but S-parameters are often more sensitive to a slightly worst contact than dc measurements. Detecting a problem in contact quality in S-parameters is not always straightforward and depends on the nature of the dut. In this appendix we provide a few pieces of advice to identify 'poor' quality contact directly during measurements, so that it can quickly be corrected before long post-process analyses. Some device figures of merit (such as the maximum oscillation frequency of a transistor, the quality factor of an inductor, thus the standards used in in-situ calibration as well) are *very sensitive* to the contact quality. So, the recommendations focus on *very high contact quality* needed for such measurements, and not on poor contact quality that can be more easily identified. These recommendations do not come from textbooks or publications, but they are the results of several years of measurement experience.

In general, the best way to ensure the contact is good is to have a reference measurement (or simulation). A reference is not always available (particularly for new designs), so the user might want to re-probe several times the same device, and monitor variations in key S-parameters.

Furthermore, the contact quality might be great at the beginning, then degrade over time (due to external vibrations whose intensity depends on the prober's mechanical stability). So, it is highly recommended to check S-parameter measurements accuracy over time when measuring for more than a couple of minutes. It can be accomplished by comparing the same measurements repeated at the beginning and at the end of a set of measurements performed on the dut.

In any case, checking for high contact quality should be accomplished by looking at some key S-parameters that depends on the nature of the dut. They are listed hereunder. Note that the frequency range of interest is up to a few GHz, because we are not interested in reactive elements, but on resistive ones, and several parasitic effects are present at higher frequencies, which complicates measurement interpretations (cf. **Chapter 2** to **Chapter 4**). So, the measurement interpretation is done in a frequency range where the S-parameters vary slowly with frequency (where a 'plateau' is observed). Note also that the recommendations are given for calibrated S-parameter measurements, for calibration aspects, the reader should refer to **Appendix B**.

Transmission lines

For transmission lines, check the magnitude of the transmission coefficient $|S_{12}|$ at low frequencies ($< 5-10\,\text{GHz}$ is sufficient). According the level of contact quality desired, a variation up to $0.01-0.02\,\text{dB}$ in $|S_{12}|$ from the reference is acceptable (for very high quality level).

For extra verification in multiline TRL, it is interesting to check the per-unit-length $R(f)$ line term at low frequency (up to a few GHz) extracted for each pair of lines (based on a common line), i.e. so applying TRL (and calibration comparison technique **[74]**) for the Thru + each different Line, and verify the consistency of the extracted $R(f)$. In ideal conditions, they should all converge at low frequencies. If the $R(f)$ of some pairs of lines deviate, they should be discarded for further data processing.

Inductor

For a two-port inductor measured in series, one should also look at $|S_{12}|$ at low frequencies, well below the inductor's resonance frequency.

MOSFET

For a common-source two-port MOSFET (port 1 at the gate, port 2 at the drain), a bad contact can be represented as a FET with larger gate resistance (R_g) or source-drain resistance (R_{sd}). Their effect is more easily noticeable at different bias conditions.

- For R_g. Both R_g and f_{max} are very sensitive to contact quality at the gate side. Therefore, *measurements in peak g_m or f_t bias should be monitored for port 1.* So, $|S_{21}|$ at low frequency (in practice up to $1-2\,\text{GHz}$) can be used to monitor the contact at port 1. Here again, variations as low as $0.01-0.02\,\text{dB}$ in $|S_{21}|$ with respect to the reference should be achieved

for very high contact quality.

- For R_{sd}. An interesting bias is cold FET ($V_{ds} = 0\,\mathrm{V}$) and in high inversion ($V_{gs} \gg V_{th}$). In this case, $|S_{22}|$ is dominated by R_{sd} (and a small term that depends on g_d) at low frequencies, and should be used for port 2 contact quality monitoring.

D. Equations of UTBB MOSFET Equivalent Circuit

This appendix contains two parts. In the first part, we report the equations modeling the small-signal equivalent circuit of **Figure D.1** used in **Chapter 4**, **Section 4.2** for substrate effect then self-heating extraction. Then, in the second part, we discuss the sensitivity of the extracted parameters to an error in R_g evaluation.

D.1 Substrate and back-gate node model

Y-parameters (Y'_{ij}) expressions of the circuit shown in **Figure D.1** have been derived and are reported in the following.

Equation 4.1 - **Equation 4.3**

$$Y'_{11} = j\omega C_{gd} + j\omega C_{gs}\xi + j\omega C_{gb}\left(1 - \frac{j\omega C_{gb} + j\omega C_{sb}(1-\xi)}{Y_1}\right), \quad (4.1)$$

$$Y'_{21} = g_m\xi + g_{mb}\left[\frac{j\omega C_{gb}}{Y_1} + (1-\xi)\left(\frac{j\omega C_{sb}}{Y_1} - 1\right)\right] - j\omega C_{gd} - (g_d + j\omega C_{ds})(1-\xi) - j\omega C_{db}\left(\frac{j\omega C_{gb}}{Y_1} + \frac{j\omega C_{sb}}{Y_1}(1-\xi)\right), \quad (4.2)$$

$$Y'_{12} = -j\omega C_{gd} - j\omega C_{gs}\zeta + \omega^2 C_{gb}(\zeta C_{sb} + C_{db})Z_7, \quad (4.3)$$

$$Y'_{22} = j\omega C_{gd} + (g_d + j\omega C_{ds})(1-\zeta) - g_m\zeta + g_{mb}\left[\zeta(j\omega C_{sb}Z_7 - 1) + j\omega C_{db}Z_7\right] + j\omega C_{db}(1 - j\omega C_{db}Z_7 - j\omega C_{sb}Z_7\zeta), \quad (4.4)$$

where

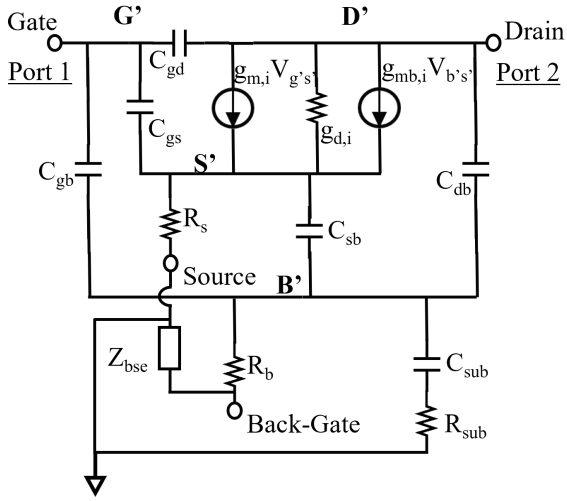


Figure D.1: FET small-signal equivalent circuit with substrate and back-gate networks, without gate and drain extrinsic series resistances.

$$Y_1 \equiv \frac{1}{R_b + Z_{bse}} + \frac{1}{R_{sub} + \frac{1}{j\omega C_{sub}}} + j\omega(C_{gb} + C_{sb} + C_{db}), \tag{4.5}$$

$$Z_7 \equiv \frac{1}{\frac{1}{Z_6} + j\omega(C_{sb} + C_{db})}, \tag{4.6}$$

$$Z_6 \equiv \frac{1}{j\omega C_{gb} + \frac{1}{R_b + Z_{bse}} + \frac{1}{R_{sub} + \frac{1}{j\omega C_{sub}}}}, \tag{4.7}$$

$$\xi \equiv \frac{\frac{1}{R_s} + g_d + j\omega C_{ds} + (g_{mb} + j\omega C_{sb})\left[1 - \frac{j\omega(C_{sb} + C_{gb})}{Y_1}\right]}{\frac{1}{R_s} + g_d + g_m + j\omega(C_{ds} + C_{gs}) + (g_{mb} + j\omega C_{sb})\left[1 - \frac{j\omega C_{sb}}{Y_1}\right]}, \tag{4.8}$$

$$\zeta \equiv \frac{g_d + j\omega C_{ds} + (g_{mb} + j\omega C_{sb}) \cdot j\omega C_{db} Z_7}{g_m + g_d + \frac{1}{R_s} + j\omega(C_{gs} + C_{ds}) + (g_{mb} + j\omega C_{sb})(1 - j\omega C_{sb} Z_7)}. \tag{4.9}$$

D.2 Parameters sensitivity to the gate resistance

To extract the back-gate and substrate parameters, we have extracted the series resistances using Bracale's method at a different bias (cold FET: $V_{ds} = 0\,\mathrm{V}$). However, as we have seen in **Section 4.1**, R_g is a particularly sensitive parameter and can commonly suffer from an uncertainty of $\pm 10\,\%$. So, we will estimate the robustness of the back-gate and substrate parameters extraction to variations in R_g.

Sensitivity of back-gate and substrate parameters to R_g variations

The electrical-only equivalent model shown in **Figure 4.19a** is extracted at ZTC bias in three different conditions according to the value of R_g: (i) nominal R_g from Bracale's method (same extraction as presented before), (ii) 10% reduction in R_g, (iii) 10% increase in R_g. **Figure D.2** shows the main extrinsic Y-parameters. The extracted substrate and back-gate related electrical parameters vary by up to 30%, while the other parameters vary less (up to 14% for C_{gs}). These variations are rather significant if one desires to extract accurate values of substrate-related electrical parameters. However, the impact on the modeled isothermal Y-parameters is negligible, meaning that it does not affect the self-heating effect characterization.

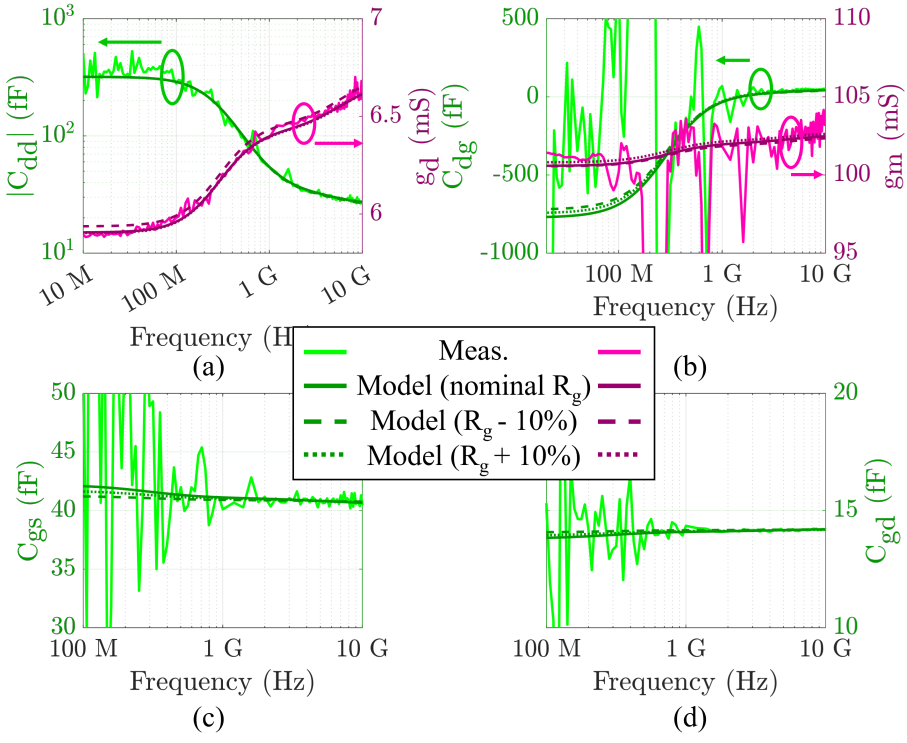


Figure D.2: $|C_{dd}|$ and g_d (a), C_{dg} and g_m (b), C_{gs} (c), C_{gd} (d). Measurements (light solid lines), final model (dark dahsed lines) of the extrinsic Y_{ij} parameters, at ZTC bias.

E. 100 kHz to 110 GHz Ultra-Wideband Modeling of UTBB FD-SOI nMOSFETs

In this appendix, the complete (quasi-static) small-signal equivalent circuit from **Chapter 4**, **Section 4.2**, including the substrate and back-gate nodes is used to extract a wideband model from the high-frequency (up to 110 GHz) transistor measurements of **Section 4.1**. Then, the extracted model is compared to the PDK's compact model.

E.1 Wideband model extraction

The high-frequency measurements used for model extraction are the ones obtained with the FormFactor Infinity I110 probes, because they yield the best overall agreement (small residual bumps and small deviation with respect to the extrinsic compact model simulations). Additional measurements are performed in the low-frequency range (from 100 kHz to 20 GHz) and a substrate model is extracted at the ZTC bias ($V_{ds} = 0.8\,\mathrm{V}, V_{gs} = 0.62\,\mathrm{V}, V_{bg} = 0\,\mathrm{V}$) following the procedure described in **Section 4.2**.

As the high-frequency extraction is only available at $V_{gs} = 0.6\,\mathrm{V}$, the same substrate and back-gate network parameters are assumed constant, and the remaining parameters are adjusted for the high-frequency measurements at the new bias (again following the procedure described in **Section 4.2**). The extracted small-signal equivalent circuit parameters are summarized in **Table E.1**. The model curves are shown in **Figure E.1** in dashed pink lines.

Figure E.1 shows the extrinsic parameters defined in **Section 4.1.3** for the different probe measurements, the extracted equivalent circuit that includes the back-gate and substrate networks shown in **Figure 4.19a** and the adjusted PDK compact model simulations. These adjusted PDK model simulations

include a 10 kΩ resistor in series with the back-gate terminal to improve the low-frequency agreement with measurements, as indicated in **Section 4.2**.

We observe that the adjusted PDK model simulations still exhibit a low-frequency discrepancy in g_m and f_t, whereas the substrate effect modeled by the extracted equivalent circuit better captures the sub-20 GHz transitions in g_m, f_t and C_{ds}.

To better analyze the high-frequency impact of the low-frequency substrate effect, let us extract a simplified small-signal equivalent circuit without the substrate and back-gate nodes, i.e. circuit in **Figure 4.19a** but without the elements in red. The extracted parameters are shown in **Table E.2**. Their associated curves are shown in **Figure E.2** in solid grey lines. From **Figure E.2**, we see that there is little deviation between the dashed pink and solid grey lines at high frequencies. So, the extracted substrate effect has little impact at higher frequencies.

Nevertheless, we still observe significantly different trends at higher frequencies (even at low frequencies in f_{max}) between the PDK compact model and the extracted equivalent circuit with substrate and back-gate nodes. Identification of which model best represents the actual FET behavior requires measurements at even higher frequencies, as the deviations are small and occur in the frequency range dominated by residual probe-dependent errors.

Yet, in both models (PDK compact model and equivalent circuit), the high-frequency (already above $\sim 20-30$ GHz) behavior of g_d distinctly deviates from measurements for all probe data. The excellent consistency among different probe measurements in g_d indicates that some physical phenomena are likely not well taken into account by the models. This high-frequency discrepancy in g_d could be a high-frequency drain-to-substrate coupling not well modeled as recently shown in **[228]** for heterojunction bipolar transistors. Further investigation is needed to confirm it.

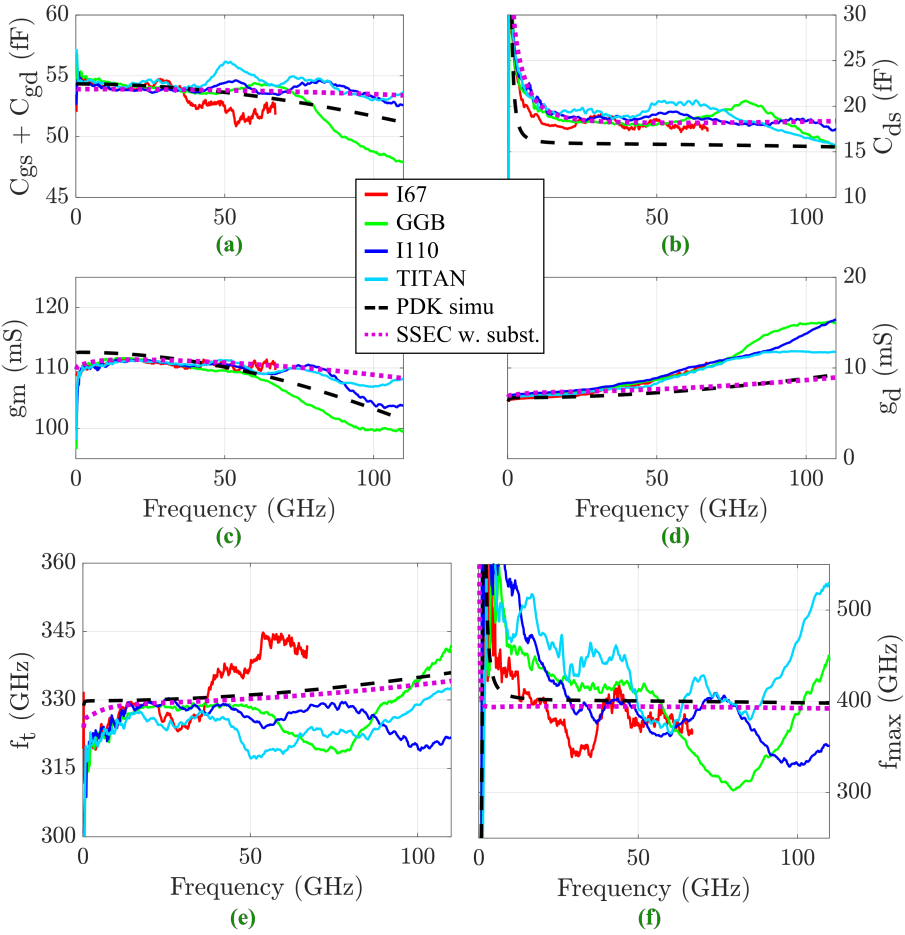


Figure E.1: Extrinsic FET parameters C_{gg} (a), C_{ds} (b), g_m (c), g_d (d), f_t (e) and f_{max} (f), measurements (solid lines) for different probe technologies, compact model (from PDK) simulations (black dashed lines), extracted equivalent circuit with back-gate and substrate networks (pink dashed lines). FET biased in saturation and peak f_t regime: $V_{ds} = 0.8\,\mathrm{V}$, $V_{gs} = 0.6\,\mathrm{V}$ and $V_{bg} = 0\,\mathrm{V}$. Reference plane in M1.

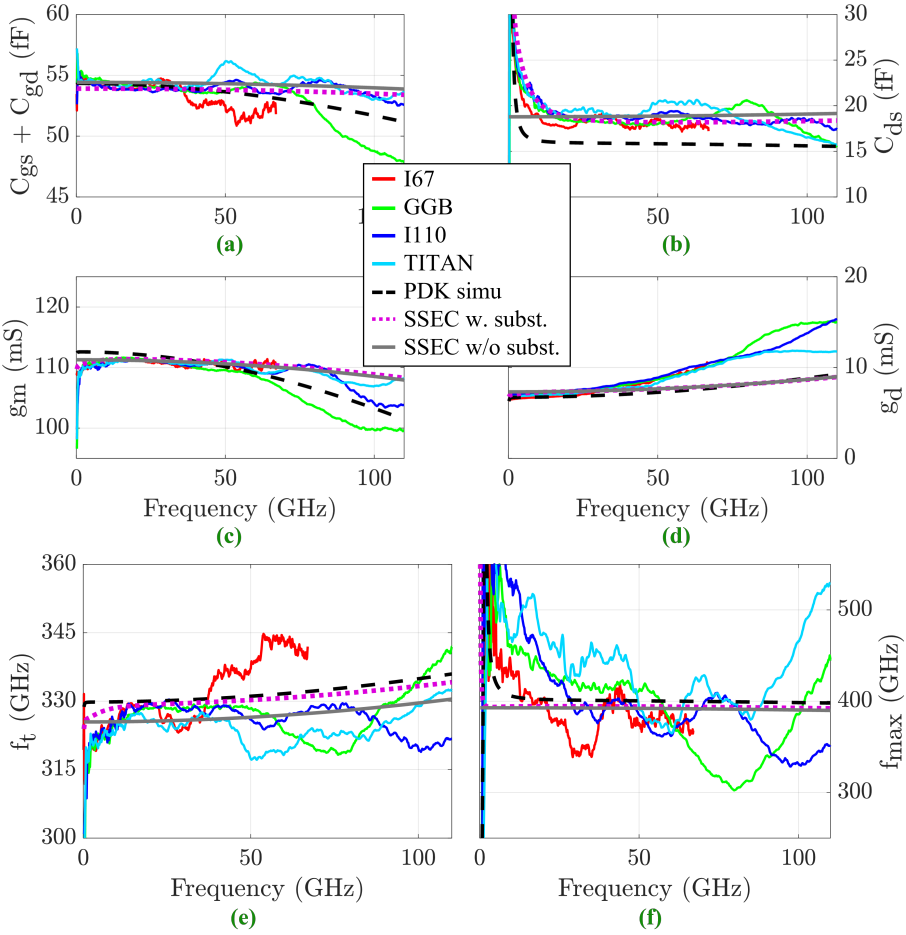


Figure E.2: Extrinsic FET parameters C_{gg} (a), C_{ds} (b), g_m (c), g_d (d), f_t (e) and f_{max} (f), measurements (solid lines) for different probe technologies and simulations of (i) PDK compact model (black dashed lines), (ii) extracted equivalent circuit with back-gate and substrate networks (pink dashed lines), (iii) extracted equivalent circuit without substrate or back-gate nodes (solid grey lines). FET biased in saturation and peak f_t regime: $V_{ds} = 0.8\,\mathrm{V}$, $V_{gs} = 0.6\,\mathrm{V}$ and $V_{bg} = 0\,\mathrm{V}$. Reference plane in M1.

Table E.1: Extracted values of electrical parameters of the equivalent circuit shown in **Figure 4.19a** with additional inductances (L_s, L_d, L_g) in series with the R_s, R_d and R_g resistances, respectively, at $V_g = 0.6\,\mathrm{V}$ and $V_d = 0.8\,\mathrm{V}$ from 'I110' probe measurements of the FET presented in **Section 4.1**.

	R_s	R_d	R_g	R_b	R_{sub}		
Ω	0.88	1.22	4.55	760	133		
	L_s	L_d	L_g				
pH	0	0.75	0.75				
	C_{sub}	C_{gb}	C_{sb}	C_{db}	C_{gs}	C_{gd}	C_{ds}
fF	35.2	0	560	13	41.8	14.2	3.6
	g_{mb}	g_m	g_d				
mS	29.2	125.7	7.6				

Table E.2: Extracted values of electrical parameters of the equivalent circuit *without substrate-related parameters*, i.e. **Figure 4.19a** but without the elements in red, (including additional inductances (L_s, L_d, L_g) in series with the R_s, R_d and R_g resistances, respectively), at $V_g = 0.6\,\mathrm{V}$ and $V_d = 0.8\,\mathrm{V}$ from 'I110' probe measurements of the FET presented in **Section 4.1**.

	R_s	R_d	R_g				
Ω	0.88	1.22	4.55				
	L_s	L_d	L_g				
pH	0	0.75	0.75				
					C_{gs}	C_{gd}	C_{ds}
fF					42.4	14.2	13.7
		g_m	g_d				
mS		125.5	8.3				

F. Background on LNA and PA Design

This appendix provides complementary information to **Chapter 5**. It gives a general design introduction of LNA and PA circuits, linking key figures of merit to device-level metrics.

F.1 Low-Noise Amplifier at MM-Wave Frequencies

F.1.1 Key figures of merit

As mentioned in **Chapter 5**, the two main figures of merit in an LNA are its noise figure and gain. As the first (amplifying) element after the switch in a front-end module, its noise figure, NF, being the ratio of output and input signal-to-noise ratio (SNR), directly contributes to the total receiver NF, which has to be minimized. In addition, the signal received at the input must be sufficiently amplified in order to avoid that subsequent circuitry (mixers) adds significant noise to the signal and further degrades the receiver SNR. This is a direct outcome from Frii's formula of cascaded devices total noise **[35]**.

Gain is determined by the cutoff and maximum oscillation frequencies (f_t and f_{max}, respectively) of the transistor, along with matching network. As shown in **Chapter 1** and **Chapter 4**, f_t & f_{max} in the 300-400 GHz range are attained in CMOS SOI thanks to the shrunk gate length, and optimized device accesses. Although most of the f_t & f_{max} reported in the literature refers to a reference plane at the first metal layer, with proper care in interconnects, f_t & f_{max} from 200 to 300 GHz can still be achieved **[173, 216, 229, 230]** including extrinsic parasitics of interconnects up to a higher-level metal reference plane, enabling sufficient gain for operation in the mm-wave range.

F.1.2 Transistor noise figure

The minimum noise figure is usually written as follows (Fukui formula [231])

$$NF_{min} = 1 + K_f \frac{f}{f_t} \sqrt{g_m + (R_g + R_s)}, \tag{6.1}$$

where K_f is a fitting parameter. From Equation 6.1, it is plain to understand that the NF_{min} increases with frequency . In order to reduce NF_{min}, the cutoff frequency has to be maximized and the series resistances must be minimized, particularly R_g (usually significantly larger than R_s).

Transistor noise models

There are many noise models for MOSFETs, namely the PRC, Van der Ziel and Pospieszalski models [232]. The above equation can be derived from the PRC model [233, 234], a similar expression can be derived from the Pospieszalski model [232, 235]. The Pospieszalski model shown in Figure F.1a is a simple model with good prediction at mm-wave frequencies and is commonly used at such high frequencies [232, 236, 237]. It contains a drain current noise source (i_{nd}) and a gate current noise source that are assumed to be uncorrelated. The gate current noise source is modeled as thermal noise from the non-quasi-static (NQS) resistance (R_{nqs}). The main contribution to the drain current noise source is channel thermal noise at high frequencies. A secondary noise source contribution to the drain at such frequencies comes from majority carriers in the substrate under the BOX [238]. Moreover, thermal noise sources for the extrinsic resistances (R_g, R_s and R_d) must also be included [146, 239] (additionally to Figure F.1a, not shown here). The thermal noise from the gate resistance has an important contribution to the minimum noise figure as expressed in Equation 6.1.

Total noise figure and equivalent noise source

In practice, it is convenient to represent the complex noisy 2-port by a noiseless 2-port preceded by two (voltage, v_n and current, i_n) correlated input noise sources (cf. Figure F.1b), which are characterized by an equivalent noise resistance (R_n), noise conductance (G_n), respectively, and a correlation term (G_c). This representation is often used for device characterization based on measurement data. The total noise figure is a function of the source impedance (Z_s or admittance Y_s) presented before the device. It can be expressed as [35, 232]

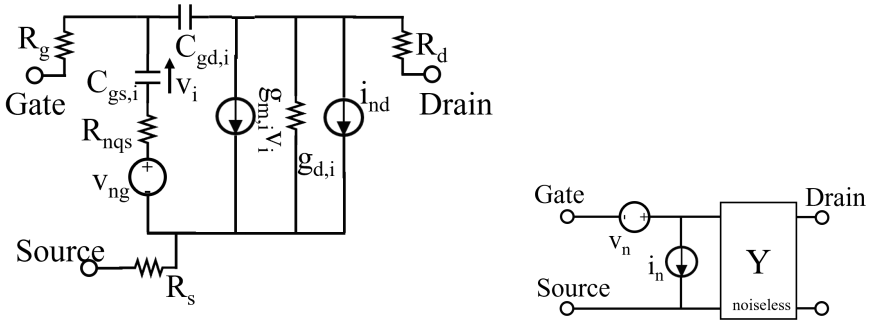


Figure F.1: Left (a): Pospieszalski noise model, complemented with noise sources from extrinsic resistances. Right (b): Equivalent noiseless 2-port with 2 noise sources: a current (i_n) and a voltage (v_n) noise source.

$$NF = NF_{min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2, \tag{6.2}$$

where Y_{opt} is the optimal source impedance leading to the NF_{min} and $Y_s = G_s + jB_s$ is the source admittance. By neglecting the gate current noise source compared with the drain current noise source (valid as long as $\omega R_g(C_{gs} + C_{gd}) \ll 1$), a simple expression of R_n is [235]

$$R_n = R_g + \frac{S_{id}}{4k_B T g_m^2}, \tag{6.3}$$

where S_{id} is the drain current noise power spectral density, k_B is the Boltzmann constant and T is ambient temperature. From Equation 6.2, R_n indicates how much NF increases from NF_{min} in case of noise mismatch, i.e. when $Y_s \neq Y_{opt}$. Therefore, R_n should be kept as low as possible to achieve the lowest NF when noise mismatch is present at the input of the device. R_n can be conveniently expressed as a function of the noise sheet resistance (R_{nsh}), which is defined as [240]

$$R_{nsh} \equiv \frac{S_{id}}{4k_B T g_m^2} \left(\frac{W_{tot}}{L} \right), \tag{6.4}$$

such that $R_n = R_g + R_{nsh} \cdot (L/W_{tot})$. R_{nsh} (with the normalization geometry factor) is a process-dependent figure of merit facilitating noise performance comparison among different technologies. R_{nsh} depends on several physical parameters, such as threshold voltage, effective mobility, critical field along the channel above which carriers travel at their saturation velocity and gate oxide capacitance per unit area. Although theoretically constant with device scaling, R_{nsh} increases as gate length scales down in sub-100-nm technologies due to short channel effects. As R_{nsh} has a complex dependence on geometry parameters (the relationship varies according to technology), the overall R_n relationship with device dimensions will not be discussed further. The interested reader can find more information about R_{nsh} and R_n and their values for different technologies in **[240, 241]**.

F.1.3 Practical design considerations in mm-wave LNAs

It should be first noted that design targets of $\sim 3\,\text{dB}$ in NF and $> 20\,\text{dB}$ in gain are common values for 5G 28 and 39 GHz user equipment applications **[166–168]**. An exact value would require a full link budget analysis of the exactly targeted application, which is out of scope of this thesis, but the above values are representative of targeted on-wafer designs.

As it is shown in **Section 5.2.5**, the noise generated by the active device is usually the main contribution to an LNA circuit. The noise factor coming from the device can be minimized according to the technology and the FET geometrical dimensions. However, it is important to keep in mind that gain is also a relevant factor in an LNA. The overall noise and gain performance for a given technology is primarily determined by the chosen topology and sizing of active devices. Both influence the noise and gain trade-off and deserve important considerations in the design. We will start discussing on the latter (FET sizing), then provide a quick overview of common topologies in mm-wave LNAs.

NF_{min} optimization, link with f_t and device geometry

There is a trade-off between f_t and R_g and thus between f_t and NF_{min} due to opposite dependence on finger width, as shown in **Figure F.3**. Usually in mm-wave technologies, the W_f leading to a minimum in achievable device NF_{min} does not lead to too strong reduction in f_t for proper operation at mm-wave frequencies, and such technologies are therefore still able to offer close to optimal NF_{min} designs above 100 GHz. Indeed, NF_{min} has benefited from

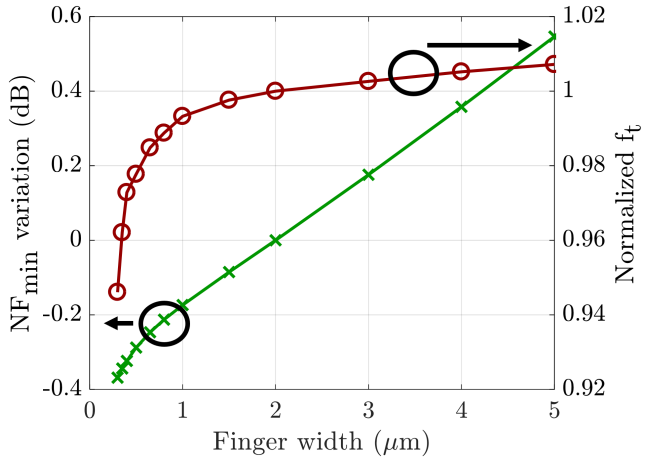


Figure F.2: Variation of NF_{min} at 28 GHz (left axis) and normalized f_t (right axis) for various finger widths. Peak f_t is typically in the 300-350 GHz range in advanced CMOS technologies and state-of-the-art values of NF_{min} are reported in **Figure F.3**.

devices scaling down. NF_{min} improved thanks to gate length scaling with increasing f_t and a controlled R_g at the same time as can be understood from **Equation 6.1**). **Figure F.3** summarizes NF_{min} values reported in the literature at mm-wave frequencies for recent FD-SOI and PD-SOI technologies **[10, 239, 242, 243]**.

In order for the final LNA's overall NF to be equal to NF_{min}, a proper impedance has to be presented to the LNA's input (corresponding to $1/Y_{opt}$ in **Equation 6.2**). Such impedance does not necessarily correspond to the maximum power transfer impedance (conjugate impedance matching). This represents the second main trade-off between NF and gain (S_{21}), which can be relaxed with an R_n as low as possible. Nevertheless, it is sometimes possible to bring the two optimum impedances (for noise and for gain) close to each other, with a careful choice of total transistor width **[244]**.

Topology review of state-of-the-art mm-wave LNAs

Here is a brief overview of topologies and main design choices of mm-wave LNAs at the state of the art.

1. Topology

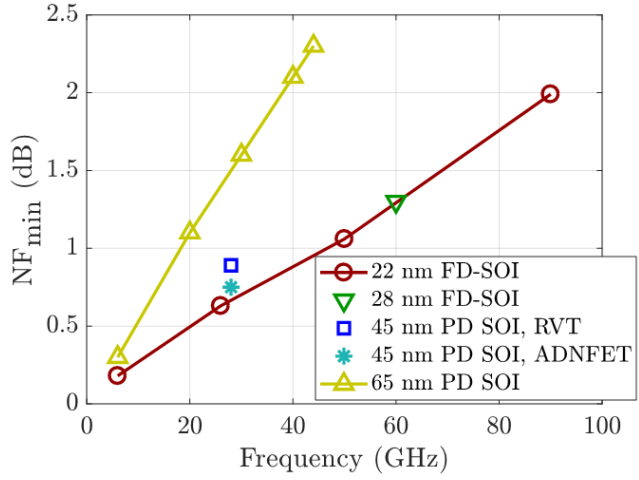


Figure F.3: NF_{min} versus frequency for recent FD-SOI and PD-SOI technologies.

- Millimeter-wave LNAs usually adopt a traditional architecture of common-source configuration for minimum noise; or a cascode or common gate topologies when noise can be traded-off with gain and/or bandwidth.
- For some specific designs, requiring ultra-wide bandwidth or at very high frequencies, more sophisticated architectures can be preferred, such as transformer-feedback for ultra-wideband behavior [245] or gain-boosting techniques with a transformer at the cascoded gate and drain sides to boost gain over a large bandwidth [229, 246].
- Inductance degeneration (series inductance between the source terminal and ground in common-source or cascode topologies) is often implemented to improve stability and ease input matching at the cost of some gain reduction. Despite the gain reduction, inductance degeneration is still implemented in LNAs working in the high mm-wave spectrum [229, 246].
- Single-ended as well as differential topologies can be found in recent literature. The differential topology usually includes neutralization capacitors to mitigate the feedback through C_{gd} and thereby improve stability at the cost of doubled power consumption [247].

2. Passives design

- Lumped metal-on-metal capacitors are still used with high quality factors

up to 100 GHz [229, 248].
- Spiral inductors are typically implemented as part of the matching network in circuit design up to roughly 60 GHz while transmission-line based matching are typically preferred above around 100 GHz [244].
- Transformers and baluns are commonly found in differential topologies, but not only [177, 229, 245]. Transformers can compact layouts at very high frequencies compared with pieces of transmission line to implement inductive elements.

F.2 Power Amplifier at MM-Wave Frequencies

This section provides a longer introduction to PA design, explaining the intrinsic limitations of CMOS technology to achieve high power and efficiency in PA circuits. Starting from the basic concept of loadline, then analyzing the contributors to the overall PA efficiency, this section investigates the main challenges faced by CMOS-based PAs linking circuit-level performance to device-level parameters and provides the main design solutions to increase power in today's PA designs in SOI technology.

F.2.1 Introduction to main PA design challenges

The last element in the transmission (TX) chain (before the switch) is the PA. This circuit block faces tremendous design challenges due to the stringent requirement of being able to deliver large amount of power at a high efficiency and with high linearity. Indeed, the transceiver's overall power consumption is usually dominated by the PA, which therefore has a major impact on battery-life in portable applications (such as mobile handsets).

The high-order digital modulations envisaged for 5G have a large peak-to-average power ratio (PAPR), of the order of 8-9 dB. This can be visually understood as a wide probability distribution function (PDF) such as illustrated in **Figure F.4c**, therefore requiring a high degree of linearity for a low bit error rate (BER) and error vector magnitude (EVM) (Acar, n.d.; Padaki & Reed, 2014). Due to the large signal bandwidth, digital predistortion (DPD) is power hungry and is not a solution of immediate interest, i.e. the requirements for 5G systems should be met without the use of digital predistortion (P. M. Asbeck et al., 2019). With more investigation in this topic, DPD could be envisaged in the future to improve 5G systems.

To achieve such high linearity, the average signal power is therefore backed-

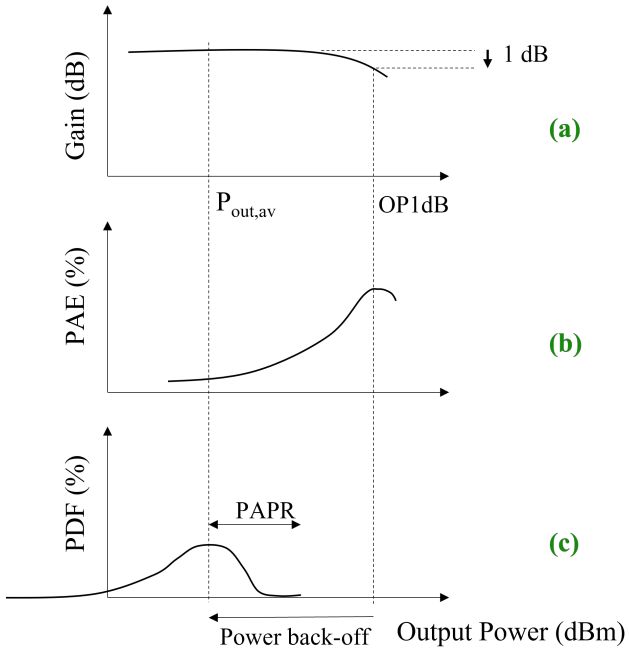


Figure F.4: Sketch of typical gain vs P_{out} (a), PAE vs P_{out} (b) curves and probability density function of high-order modulation (c).

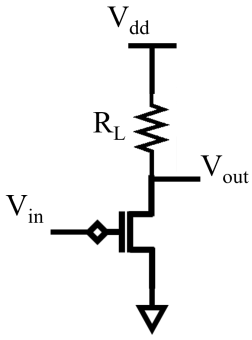


Figure F.5: Common-source FET loaded by a resistor R_L as a basic PA configuration.

off (from the 1-dB compression point), since the PA is always more linear the further away its regime is from compression: the average power of the PDF in **Figure F.4c** is shifted to lower values such that the PDF lies across a linear region in the gain vs P_{out} curve (shown in **Figure F.4a**). Using OFDM instead of single carrier also intensifies the need for high linearity, which is translated in an additional 1.5 to 2 dB of power back-off. The main drawback of working in power back-off is the loss in average efficiency of the PA, which is maximum at compression and decreases at lower power as shown in **Figure F.4b**. Despite the obvious advantages of Si-based technologies for high integration and the high performance demonstrated above in LNA, the PA still remains the bottleneck for these technologies due to their intrinsic device limitations to being able to deliver large amount of power at high efficiency. Detailed explanations are given below, revealing why GaN technologies are more suited to these circuits.

F.2.2 PA basics, the loadline concept

First, let us introduce the loadline concept useful to understand the main limitations. Let us consider the simple example depicted in **Figure F.5** showing a common-source transistor loaded by a resistor R_L biased for class A operation.

The loadline concept is illustrated in **Figure F.6** on top of the dc output characteristics of the transistor, i.e. V_{ds} vs I_d for different V_{gs}. At a given input power, the drain current follows the input signal and the V_{ds} swings accordingly with an amplitude that depends on the load as expressed below.

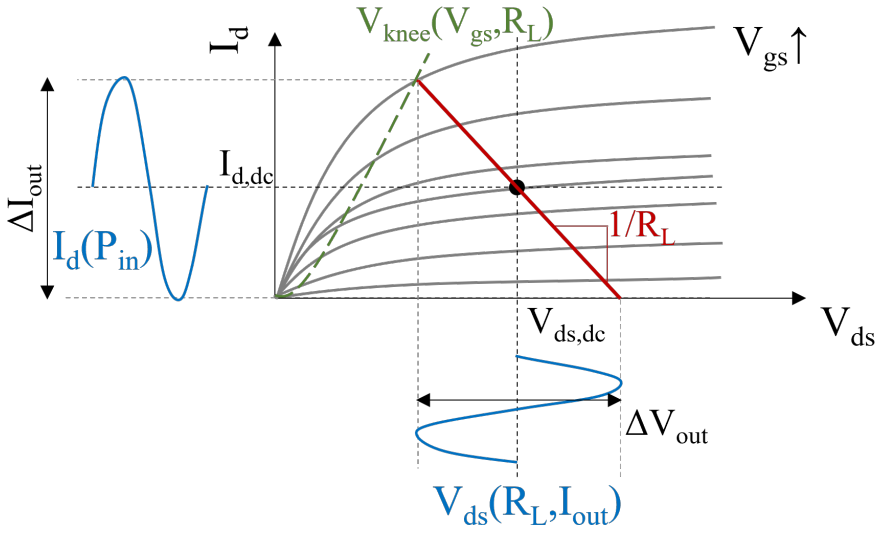


Figure F.6: dc output characteristics of a FET and illustration of loadline concept.

$$V_{ds} = V_{dd} - I_d R_L. \tag{6.5}$$

where V_{dd} is the supply voltage.

This $V_{ds}(I_d)$ is a straight line due to the purely resistive load, and is highlighted in red in **Figure F.6**. For high input power, the output V_{ds} will be clipped at a minimum value, where the transistor enters in the triode region, called knee voltage (V_{knee}, in green in **Figure F.6**) and the maximum value of V_{ds} is determined by the bias point and R_L when I_d reaches 0 A.

The output rms power is given by the product of the current and voltage rms amplitudes ($P_{out} = \Delta V_{out} \Delta I_{out}/8$). The ΔV_{out} and ΔI_{out} are a function of the bias and load. The output power can then be optimized by a careful choice of $(V_{ds,dc}, I_{d,dc})$ and R_L. A class A PA is biased at the point $(V_{ds,dc}, I_{d,dc})$ that corresponds to half of the maximum allowed I_d ($I_{d,max}$ is fixed by electromigration rules or corresponding maximum V_{gs} preventing oxide breakdown) and $V_{ds,dc}$ is half of the maximum allowed V_{ds} ($V_{ds,max}$ is a portion of the breakdown voltage, guaranteeing reliable operation throughout the circuit lifetime). The

corresponding optimum load maximizes the output voltage and current swings and is given by $R_L = V_{ds,max}/I_{d,max}$.

F.2.3 Power added efficiency: a detailed contributors analysis

The power added efficiency (PAE) figure of merit (FoM) metric of a PA is given by:

$$\text{PAE} \equiv \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out}}{P_{dc}}\left(1 - \frac{1}{G}\right), \tag{6.6}$$

where G is the forward gain of the amplifier: $G = P_{out}/P_{in}$.

The PAE can be re-written as a product of several factors [249]:

$$\text{PAE} = F_{\text{gain}} F_{\text{matching,Q}} F_{\text{waveform}} F_{\text{Vswing}}. \tag{6.7}$$

F_{waveform} describes the overlap function of the drain voltage and current. Depending on the class of operation (A, B, switching classes), its value can be from 0.5 to 1 for ideal switching. It depends on the biasing (class of operation) as well as harmonic matching and therefore not on technology (except perhaps for losses in harmonic termination, but this is accounted for in the $F_{\text{matching,Q}}$ term). In the class A example provided above, by assuming the PA is biased at an optimum point and an optimum impedance is presented to the FET, and by assuming $V_{knee} = 0\,\text{V}$ (thus $V_{ds,dc} = \Delta V_{out}/2, I_{ds,dc} = \Delta I_{out}/2$ and $R_L = \Delta V_{out}/\Delta I_{out}$), then the RF power delivered at the load at maximum power is

$$|P_{out}(t)| = \left|\frac{\Delta V_{out}\Delta I_{out}\cos^2(\omega t)}{4}\right|, \tag{6.8}$$

since $I_{out} = -I_d$ and the load and the RF V_{ds} and V_{out} are equal. Under these assumptions, the dc power is $V_{ds,dc}I_{ds,dc} = \Delta V_{out}\Delta I_{out}/4$, and the rms P_{out} at the load is $\Delta V_{out}\Delta I_{out}/8$. Therefore, it is plain to deduce that a maximum value of 0.5 in PAE (P_{out}/P_{dc}) is attained by class A PAs. This value can be enhanced to 0.78 with class B operation and even theoretically to 1 with class F or switching-mode amplifiers (class D and E). In these cases, the waveforms are such that the device does not dissipate power by having $I_d = 0$ on half of a period and $V_{ds} = 0$

on the other half. Switching-mode amplifiers are highly non-linear and therefore not suited to 5G waveforms, while class AB, B, C and F amplifiers require some harmonic matching. Due to the increased losses associated to additional passive elements required for harmonic matching, harmonic engineering beyond the second harmonic is usually not implemented at mm-wave frequencies.

$F_{\text{matching,Q}}$ is related to the losses in the output matching network, harmonic termination and power combining, thus to the quality factors (Q) of the matching elements. Provided the last stage features enough gain, the losses in matching circuits from input matching or previous stages will not affect the PAE. From **Equation 6.6**, if the gain of the last stage is large enough, PAE $\approx P_{out}/P_{dc}$ and does not depend on the input power delivered to the last stage. It implies that a reduction of power delivered at the input of the last stage (for instance due to low-Q matching circuits before the last stage) has little effect on the overall PAE of the PA. On the contrary, any losses at the output of the last stage will decrease the power delivered at the load (P_{out}) and thereby directly decrease the overall PAE. The quality factor of passive devices has greatly been improved in CMOS SOI technologies in reducing losses by (i) using thick Cu and Al metal layers in technologies targeting RF and mm-wave applications and (ii) replacing the underlying standard resistivity wafers (with a nominal resistivity of around 10 Ω cm) with high-resistivity (trap-rich) silicon wafer (resistivity of several kΩ cm).

The term F_{gain} in **Equation 6.7** corresponds to the $(1-1/G)$ term in **Equation 6.6**. It accounts for the amount of rms input power required to drive the PA, which might be non-negligible. The gain G is determined by the f_t and f_{max} of the transistor, along with matching network. As explained in **Section F.1**, f_t and f_{max} in the 300 GHz range can be found in CMOS SOI technologies thanks to the shrunk gate length, enabling sufficient gain for operation in the mm-wave frequency range.

The term F_{Vswing} in **Equation 6.7** describes the loss in efficiency due to the non-zero value of the knee voltage. F_{Vswing} is roughly equal to $1-V_{knee}/V_{dd}$, where V_{dd} is the supply voltage. This term can be evaluated from the dc I_d-V_{ds} curves of the transistor and the load resistance (cf. green dashed curve in **Figure F.6**). V_{knee} is related to the ON-resistance (R_{on}) of the transistor in linear region and the maximum current density. Decreasing V_{knee}, can be achieved with a sharp I_d-V_{ds} transition in the linear region (i.e. low R_{on}) or with a low maximum current. The efficiency is maximized by using a V_{dd} as high as possible, as long as reliability is guaranteed (breakdown, etc.). This F_{Vswing} is

governed by a FoM similar to Baliga's first FoM [4, 250]:

$$V_{bk}^2 R_{on} = \alpha' \mu' \varepsilon' E_{bk}^3 A_c. \tag{6.9}$$

A_c is the effective area for current flow, E_{bk} the breakdown electric field, which depends on the size of the bandgap. ε' is the permittivity, μ' the mobility and α' is a numerical coefficient of order unity. The inferiority of CMOS in PA application is clearly evidenced here due to low breakdown electric field (and mobility), with respect to III-V technologies, in particular GaN [251].

F.2.4 Techniques for increased output power

The other important requirement or FoM of the PA is the maximum or saturated output power (P_{sat}). Increasing the output power can be realized by (i) increasing the voltage swing and (ii) increasing the current swing (thus maximum current). The voltage swing is mainly limited by reliability issues linked to breakdown voltage of the transistor. The $I_{d,max}$ (and current swing) can be increased by increasing the transistor width. Despite the fact that increasing much the FET width reduces f_t and f_{max} (due to additional parasitics), the resulting optimal load resistance to be presented at the output decreases proportionally, to the point of making the impedance matching networks very difficult. Low values of load resistances below 10-20 Ω are difficult to implement, which has the effect of increasing losses originating in complex matching networks, thus reducing the power improvement and mostly the efficiency.

Transistor stacking

FET stacking is a technique that circumvents the low breakdown voltage of individual FETs and enables an increase in the output voltage swing as illustrated in Figure F.7. With a proper choice of the gate capacitances ($C_{g,k}, k = 2,3,...,N$), the drain-source voltage swing across each FET ($V_{ds,k}, k = 1,2,3,...,N$) is equal such that the total output voltage swing is multiplied by the number of stacked-FETs (N). Besides an increased power due to larger voltage swing, for a constant load impedance (R_{opt}), the FET widths can also be multiplied, such that the gain in power is proportional to N^2.

Unfortunately, the maximum number of FETs that can be stacked is limited to 2 or 3 in practice. First, by increasing the transistor width, additional parasitics lower the f_t and f_{max}, thus gain, and decreases the input impedance ($Z_{in,0}$), therefore complicates the input matching. Second, due to resistive losses

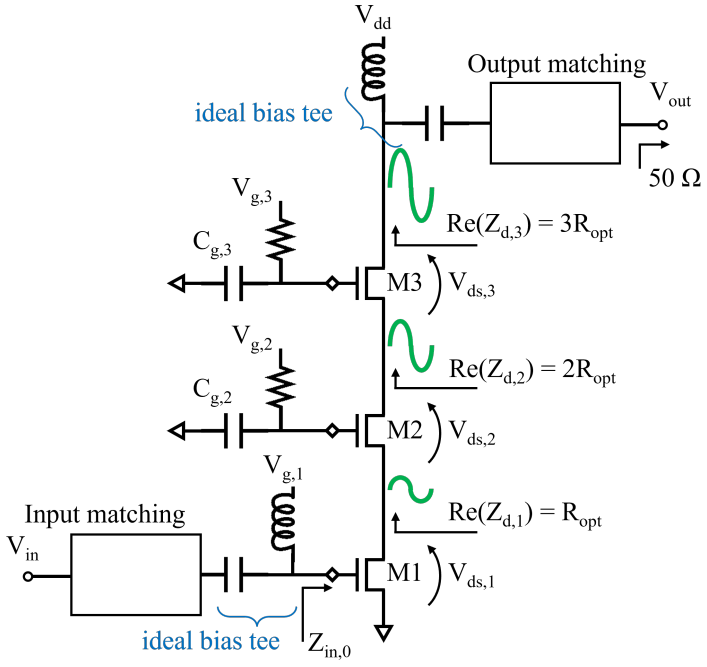


Figure F.7: FET stacking concept to increase output power (with ideal bias tee).

in the transistor, and to phase misalignment of the drain voltages, the effective power gain is limited in practice beyond $N = 3$ [180]. Phase misalignment arises from the fact that $C_{g,k}$ tunes out the real part of the impedance seen at each drain ($\mathrm{Re}(Z_{d,k})$, to achieve equal voltage drop across each FET), but not the imaginary part (an inductive load should be presented to compensate the total drain capacitance at each FET, whereas the above stacked transistor presents a capacitive load). Additional passive elements can be added to compensate the phase misalignment, but at the cost of additional losses through them. The interested reader can find more information in [180], which provides a detailed theoretical analysis of FET stacking for PA. SOI technologies are particularly suited to FET stacking compared to bulk thanks to reduced and more linear junction capacitances (reduced phase misalignment).

FET stacking is a common technique used, either alone or combined with other techniques, in practically all SOI-based PAs in recent literature. Many demonstrator circuits employing FET stacking have been published [180, 249, 252–254].

In PD-SOI (notably in 45RFSOI node at mm-waves), large P_{sat} values are achieved with good or outstanding peak PAE. Actual figures of state-of-the-art CMOS-based PA performance will be provided in the next section when benchmarking the designed PA. Due to their shorter gate lengths FD-SOI nodes are limited to lower breakdown voltages compared with PD-SOI technologies.

In FD-SOI conventional FET stacking is employed for single PA-cells, then, beyond that, the outputs of multiple PA cells are combined together using passive combiners to further increase the overall output power.

Power combining

Power combining can be implemented in many different ways.

- A (pseudo-) differential configuration is a very common and efficient technique, since it has the advantage of improving stability thanks to capacitance neutralization and can be combined with baluns (often implemented with transformers [255, 256] in a very compact way [257]).
- Additional (or distinct) power combining can be achieved with current [201] or voltage combining [258].
- A balanced PA topology also increases output power, with additional benefits in terms of third-order intermodulation product and VSWR robustness [216].
- In the case of an on-chip antenna, power combining can also be realized by feeding the antenna through multiple paths [259].

In practice, however, power combining is limited by (i) losses in the power combiner elements and (ii) area.

F.2.5 5G modulations, the challenges of high efficiency at high power back-off

It should be first noted that complex modulations with 64-QAM with OFDM are considered for uplink 5G handset applications [4, 171, 172]. The targets in rms EVM and ACLR to guarantee low bit error rate and manageable channel leakage are -25.2 dB and -30 to -25 dB, respectively. Moreover, according to the number of antennas used for beamforming (as well as interconnects loss, antenna gain, etc.), the average power to be delivered by each PA is expected to be around 11 to 15 dBm [4]. Whereas the target PA efficiency for 5G applications is around 20 %, which is critical for mobile applications as the PA is typically responsible for most of the power consumption of wireless transceivers.

In complex modulations such as the ones used or envisaged in 5G, the high PAPR of the signal (additionally to the OFDM) requires the PA to work with a large amount of back-off, thus operating less efficiently on average to meet signal integrity requirements. Several techniques are able to increase average PAE in back-off operation. The goal is not to present them in details here, but only to give an overview of their implementations in PD-SOI and FD-SOI technologies. For more details, the interested reader is invited to consult [260] for instance. The Doherty architecture is composed of a main PA, always active, and an auxiliary PA that turns on to give extra power close to compression. It has a much better efficiency at back-off, with a theoretical peak PAE at 6-dB of power back-off. Several PAs with this architecture have already been published in both PD-SOI [187, 261, 262] and FD-SOI technologies [202]. A Chireix out-phasing architecture was implemented in [263] using two 45RFSOI chips and performing the power combination and out-phasing at the antenna feed level on package.

G. Complete 24-43 GHz PA Design Description

This appendix provides the complete design description of the two wideband 24-43 GHz PAs designed and fabricated in GlobalFoundries 22FDX® technology. It complements the shorter design overviews presented in **Chapter 5**. The first PA (PA1) relies on a 3-stacked FET output stage with a distributed balun, covering the 24-43 GHz bands. The second one (PA2) uses PA1 in a balanced topology with configurable 90° hybrid couplers, enabling a multiband operation.

G.1 Instantaneously wideband PA (PA1)

PA1 is based on a pseudo-differential two-stage configuration, with the schematic shown in **Figure G.1a**. The power (second) stage uses a 3-stacked FET differential architecture **[180]**, while the driver (first) stage features no FET stacking. Their circuit schematics are shown in **Figure G.1b** and **Figure G.1c**. Both stages use cross-coupled neutralization capacitors to stabilize the amplifier in differential operation **[181]**. The single-ended to differential (and inversely) transformation is operated by the input and output baluns that also perform the required impedance matchings. An inter-stage transformer transforms the input impedance of the power stage into the required impedance of the driver stage for optimum large-signal performance. The gate and drain biases are fed to the transistors through the ac-common ground of the transformers' center-taps as shown in **Figure G.1a**. Large bias resistors are added in the gate bias lines to stabilize common-mode operation **[181]**. The back-gate terminals of all FETs are connected to dc pads via large bias resistors, to decouple RF and dc operation (not shown in **Figure G.1**).

The PA design is done in several steps. First, the output stage is designed,

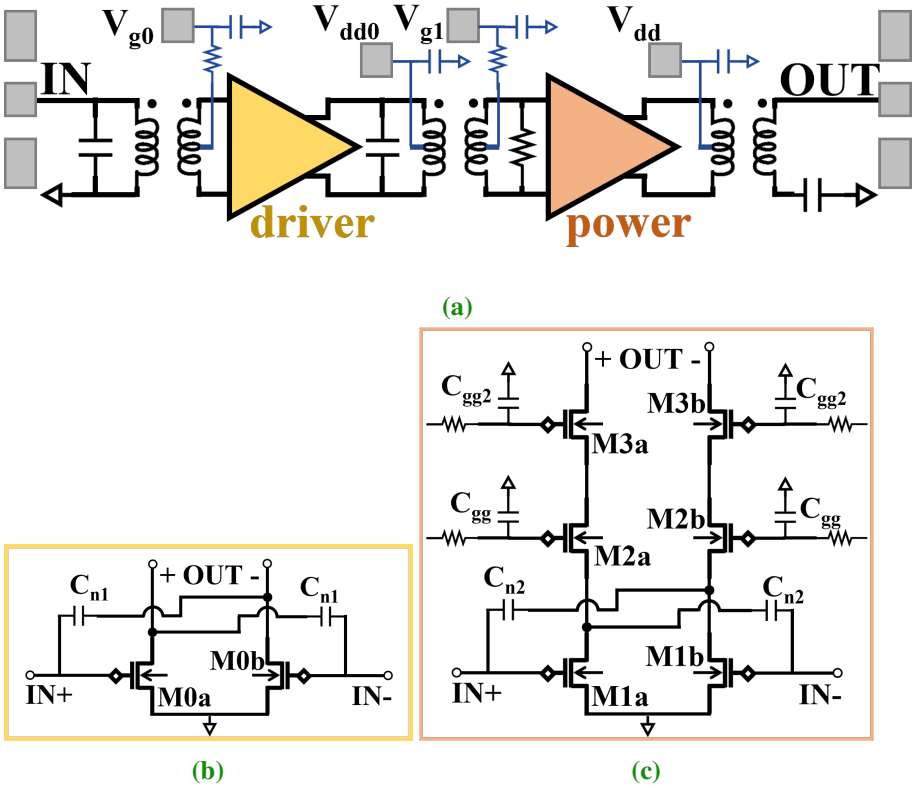


Figure G.1: Schematic of PA1 (a), the driver stage (b) and power stage (c).

thereby fixing the main large-signal, non-linear performances, such as saturated output power (P_{sat}), power added efficiency, compression, etc. Then, an output matching network is carefully designed. Since losses in this matching network reduces the output power, this matching network's performance has a direct impact on the overall performance of the PA. The driver stage and inter-stage matching network are subsequently designed to provide enough linear input power to the power stage for normal operation. Finally, the input matching is designed to match the input impedance to 50 Ω.

We first start detailing the design of the power stage. Then, the design of the output matching is described, and, finally, the design of the driver stage and input and inter-stage matching networks are briefly presented.

G.1.1 Power stage design

A detailed schematic of this stage is given in **Figure G.1c**. The output stage uses nMOSFETs super-low threshold voltage with a gate length of 20 nm and a total FET width of 160 µm for all FETs. The 20 nm gate length is a good trade-off between high RF performance (f_t and f_{max}) and reliability, for which the breakdown voltage is not significantly lower than other sub-30-nm gate lengths **[182]**. The total FET width results in a trade-off between high P_{out} and input impedance transformation over a large bandwidth.

Indeed, the differential input of the stage can be modeled as a resistance in series with a capacitance (gate resistance R_g and capacitance C_{gg} of the common source FET of each branch in series). The larger the FET, the lower R_g and the more complex the design of the inter-stage matching network. So, we fixed a limit of $R_g \lesssim 5\,\Omega$. With a total transistor width of 160 µm, it yields $R_g = 4.5\,\Omega$ and $C_{gg} = 80$ fF.

There are multiple ways to achieve a target total transistor width (W_{tot}). W_{tot} is the product of several factors:

$$W_{tot} = MW_{fet} = MN_fN_{vf}W_f, \tag{7.1}$$

where W_{fet} is the unit transistor cell width, N_f is the number of horizontal gate fingers, N_{vf} is the number of vertical gate fingers, W_f is the finger width, M is the multiplicity, i.e. the number of times a unit transistor cell is repeated. The goal is to find appropriate values for M, N_f, N_{vf} and W_f, such that (i) the pair (f_t, f_{max}) is maximized, (ii) reliability is under control: electromigration rules are passed with some margin (limit on W_{fet}), (iii) the overall interconnects

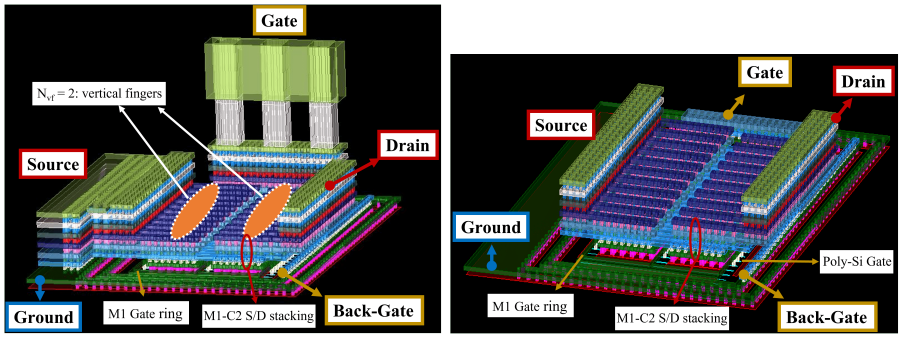
between each transistor cell are small, to reduce non-quasi-static effects as much as possible such that the signals are in phase at each unit FET cell.

A good optimum is found for $W_f = 1\,\mu m, N_f = 20, N_{vf} = 2$ and $M = 4$. Layout parasitics have been reduced, lower resistance implies lower losses, lower reactance means lower phase mismatch and ease in input/output impedance matching. The unit transistor cell layout in shown in **Figure G.2**, with interconnects from M1 up to C5 for the common-source FETs and the stacked FETs. The gate terminal comes from the upper metal layers from a single side, but contacts the poly-Si gates (largest contribution to the total gate resistance) from both sides, thus significantly lowering the gate resistance. A relaxed poly-pitch is used (CPPx2), which increases f_t and f_{max}, reduces the source and drain extrinsic resistances, and relaxes the electromigration constraints. The source and drain terminals are contacted via an M1-C2 stacking with staggered C1-C2 staggered stacking, thus significantly lowering the drain-source capacitance, for a negligible increase in drain-source resistance. This optimum design choice yields peak f_t and f_{max} of 320 and 280 GHz, respectively, and pass electromigration rules for a 5 years lifetime[1] lifetime operation at 125 °C.

The floorplan of the output stage is shown in **Figure G.3**. Dummy FET cells are added at the borders to reduce manufacturability variability. The neutralization capacitors ($C_n = 35.6\,fF$) are designed in high-Q metal-on-metal (mom) interdigitated capacitors. Only metals C2 to C5 are used, to reduce the shunt capacitance to ground. The capacitors at the gate of the stacked FETs (C_{gg} and C_{gg2}) act as voltage dividers to adjust the V_{ds} swings for each transistor **[180]**. Their values are selected to have equal V_{ds} drop across each FET, such that the voltage stress is equally distributed among the FETs when the PA is working in maximum power condition. $C_{gg} = 500\,fF$ and $C_{gg2} = 120\,fF$ yield equal V_{ds} drop across each FET for the optimal load determined from load-pull simulations. More details concerning the optimal load can be found in the next sub-section devoted to the output matching network design. The two large shunt gate capacitors (C_{gg} and C_{gg2}) are designed in M1 to C5 interdigitated mom capacitors to reduce their area. Although it is not shown in **Figure G.3**, the substrate is shielded with M1 and/or M2 metal layers below the high-level interconnects.

As mentioned in **Section F.2.4**, parasitic capacitances in the source and

[1] Based on an LTE product, a 5 years lifetime use-case scenario gives a mission profile of 2027 hours = 0.23 years, at a junction temperature of 125 °C (corresponds to ambient temperature for on-wafer measurements).



(a) **(b)**

Figure G.2: 3D view of M1-C5 (and JA for the Gate) FET interconnects for the common-source FETs (a) and stacked FETs (b). The shown parasitics are extracted with a PEX tool. The Source terminal is grounded locally for the CS FETs. A ring in M1 (dark green) surrounds the two sets of vertical fingers and contacts the poly-Si Gate (electric blue, pinpointed in b) on both sides. The stacked FETs Gate terminal does not go beyond M2 at the FETs' vicinity for reduced C_{ds} parasitic.

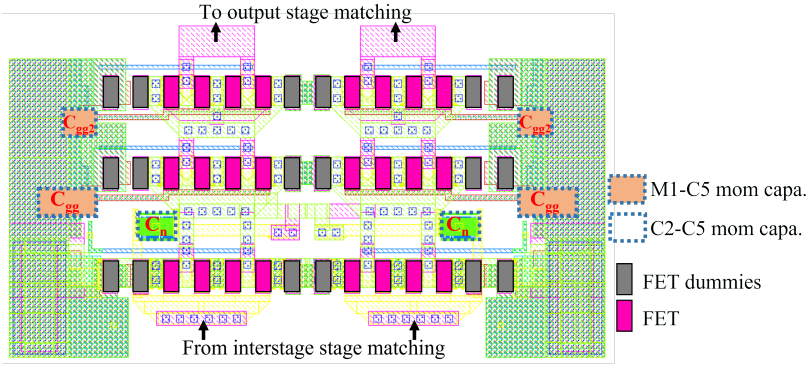


Figure G.3: Floorplan and higher-level interconnects of the output stage. Although it is not shown here, the empty spaces are filled with a metal shield in M1 and/or M2 to reduce signal propagation inside the substrate. The shown parasitics are extracted with a 2.5D EM simulator.

drain nodes between the stacked FETs contribute to phase misalignment (in V_{ds} and I_d of each stacked FET) and thereby lower the output power, but mostly lower the PAE. There are some methods to compensate for phase misalignment [180]. However, since they are all narrowband, they have not been used in this design.

Overall, the interconnects parasitics are extracted via a smart partitioning between Spice-netlist-based parasitic extraction (PEX) tool and 2.5D EM based simulations. The parasitics at the vicinity of each unit transistor cell (see Figure G.2) and the shunt gate capacitors (C_{gg} and C_{gg2}) are extracted with Quantus RC, including the bottom metal layers (M1 to C5 or JA, according to the FET terminal). The remaining parasitics (shown in the floorplan of Figure G.3) are extracted with a 2.5D EM solver on all metal layers for a more accurate description of distributed effects.

Biasing

The V_{dd} bias voltage is set to 2.4 V, to present a dc V_{ds} of 0.8 V to each FET, the nominal voltage in this technology. Small variations of V_{ds} around 0.8 V has little influence on the FET parameters, such that we can safely design with this V_{dd} bias and afterwards analyze the effect of V_{dd} variation at the PA level, while it is still operating in close to optimal designed conditions (with appropriate load impedance, same input impedance).

As both V_{gs} and V_{bg} modulates the drain current and class of operation, in the following paragraphs, the back-gate voltage is set to 0 V, to discuss the design choice of the V_{gs}. We will come back to the choice of V_{bg} later.

By modulating the drain current, the gate bias determines the operating class of the PA. At low and medium power ranges, class A linearity is better than class B. However, as power increases close to saturation, due to internal harmonic cancellations, class B features a sweet-spot in 3$^{\text{rd}}$ order harmonic (when linearity is higher) at a high input power, resulting in a better linearity at high power region than class A [183]. In addition, class A works inherently with lower efficiency (maximum 50 % in the ideal class A, instead of up to 78.5 % in the ideal class B, as explained in Section F.2.3). Therefore, by carefully choosing the gate bias that controls the PA operating class, we can simultaneously achieve high efficiency and linearity.

An analytical analysis of the large-signal behavior (neglecting memory effects) of a common-source CMOS FET as a power amplifier is explained in [184] and also applied in [183]. A full description of the large-signal model is beyond the scope of this chapter. The take-away messages are that some

sweet-spots in linearity (minimum in the generated 3rd harmonic, thus in the third-order intermodulation product, IMD3) exist (which can be traced back to the memoryless non-linear transfer function of a CMOS PA) and can be pushed to lower or higher input powers by varying the gate bias. Similar results can be found for this 22 nm FD-SOI technology. Simulations of the unit transistor cell designed above are reported in **Figure G.4**. **Figure G.4** shows the third-order intermodulation power of the unit transistor cell in a common-source topology, with 2 input tones spaced by 1 kHz at 1 MHz (to avoid memory effects) and loaded by a 50 Ω port. In addition, the analytical model from **[184]** is constructed from the simulated dc trans- and output characteristics of the FET. The third harmonic power (H3) computed from the model is plotted in **Figure G.4** in solid lines. The excellent agreement in model and simulation confirms here again the validity of the large-signal model. From **Figure G.4**, we observe that $V_{gs} = 0.3\,\mathrm{V}$ yields good linearity at medium power levels up to relatively large input power. Furthermore, $V_{gs} = 0.3\,\mathrm{V}$ is also a good compromise between high linearity and sufficient gain that is fundamental at mm-wave frequencies. Indeed, as shown in **Figure G.5**, the f_t and f_{max} (thus gain) quickly drops as the gate bias approaches the threshold voltage. A V_{gs} of 0.3 V still yields f_t = 141 GHz and f_{max} = 202 GHz, which is large enough for 28-39 GHz operation.

An appropriate V_{gs} bias enables a significant reduction of third harmonic level. Thanks to the differential topology, the even harmonics cancel out at the output, as long as symmetry is maintained. The main source of asymmetry in a pseudo-differential topology usually arises when converting the differential signal into a single-ended one, or inversely, at the output, or input, baluns. This is further discussed later. Despite the differential topology is able to remove the even harmonics from the output, even harmonics are still present in internal nodes of each branch and generate side-band asymmetries and other effects reducing the PA efficiency **[183, 185, 186]**. It is possible to introduce even harmonic terminations in a way that avoids disturbing the fundamental power operation. However, such harmonic terminations, which rely on an LC resonator, are inherently narrowband and therefore are not suited to a wideband PA design.

As for the back-gate voltage (V_{bg}), it is important to keep in mind its effect on the FET characteristics. V_{bg} changes the threshold voltage, thus the drain current (for a fixed V_{gs}) and thereby the class of operation. Thus, I_d is modified by both V_{gs} and V_{bg} variations, still I_d is much more sensitive to V_{gs} than to V_{bg} variation. Indeed, in the 22 nm FD-SOI technology, the relationship of

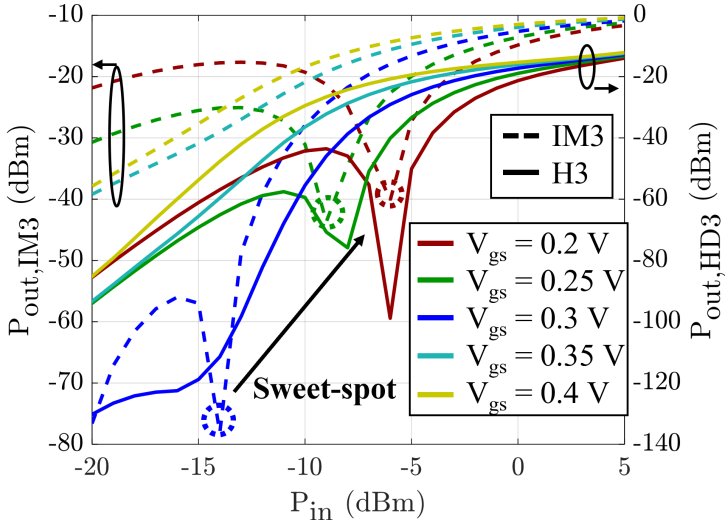


Figure G.4: Output third-order intermodulation product (IM3) power (dashed lines, left axis) from simulations and output third harmonic power (solid lines, right axis) from single-tone analytical model of **[184]** versus input power at different gate biases.

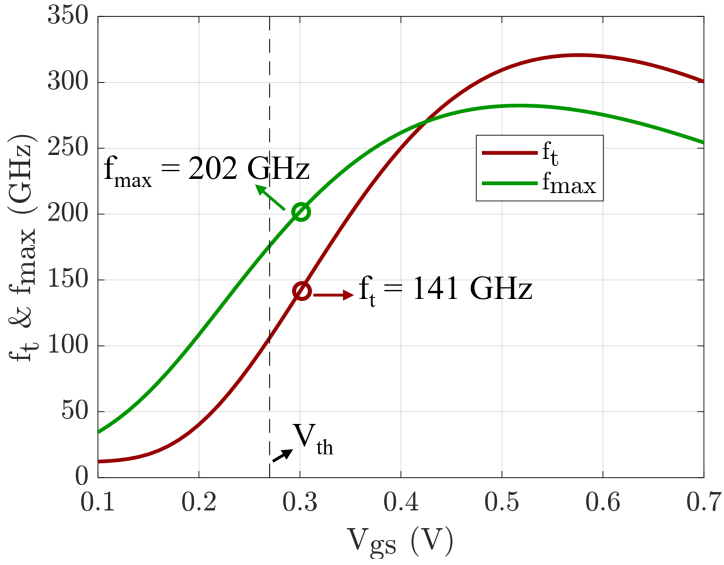


Figure G.5: f_t and f_{max} versus gate bias for the designed unit FET cell. The threshold voltage is 0.27 V. $V_{gs} = 0.3$ V and $V_{ds} = 0.8$ V yields f_t = 141 GHz and f_{max} = 202 GHz.

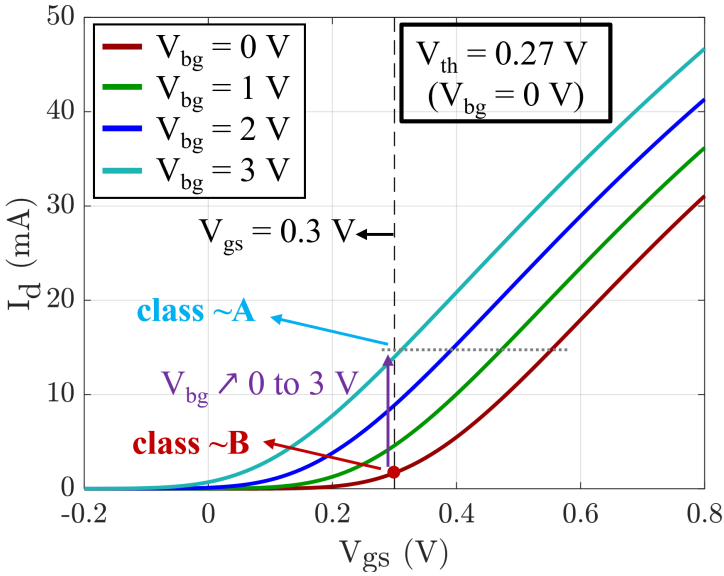


Figure G.6: Trans-characteristics of the designed unit cell FET for different back-gate voltages ($V_{ds} = 0.8\,\mathrm{V}$).

V_{th} variation according to V_{bg} variation is of $\sim -80\,\mathrm{mV/V}$ [161] for the SLVT FETs. So, for $+1\,\mathrm{V}$ increase in V_{bg}, V_{th} decreases by $80\,\mathrm{mV/V}$ and the overdrive voltage ($V_{ov} = V_{gs} - V_{th}$) increases by $80\,\mathrm{mV/V}$. The dc trans-characteristics of the unit transistor cell used in the PA design is shown in **Figure G.6**. Due to the back-gate n-doping in the SLVT transistor, only positive (from ~ -0.5 to $+3\,\mathrm{V}$) V_{bg} values are allowed to prevent forward biasing the P-N diode between the back-gate and substrate node (as for the LNA). Note that the V_{bg} values recommended by the PDK are 0 to 2 V.

We fix $V_{bg} = 0\,\mathrm{V}$ for the following. Such a value of V_{bg}, combined with the previously determined $V_{gs} = 0.3\,\mathrm{V}$ results in deep class AB operation with good trade-off between linearity and efficiency. Moreover, such a $V_{bg} = 0\,\mathrm{V}$ value can be adjusted after fabrication to compensate for process variation inducing small V_{th} variation. With V_{bg} varying from -0.5 to $+3\,\mathrm{V}$, it can compensate for -240 to $+40\,\mathrm{mV}$ of V_{th} variation. Finally, and more importantly, we can easily change the PA class of operation from deep class AB to class A, by simply increasing the V_{bg} bias, as shown in **Figure G.6**. So, $V_{bg} = 0\,\mathrm{V}$ is selected for this design but can be varied during characterization to (i) compensate for

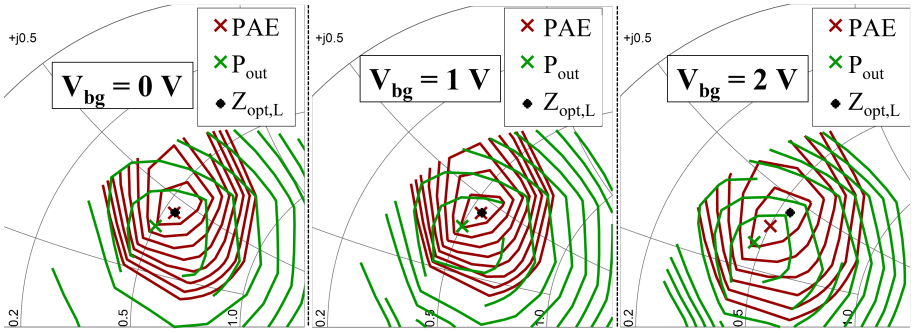


Figure G.7: Load-pull simulations at 39 GHz of the power stage for different V_{bg} biases, moving from a deep-class AB operation to class A. The selected load impedance for the output stage is $Z_{opt,L}$ (black dot). The Smith charts are normalized to a 100 Ω reference impedance.

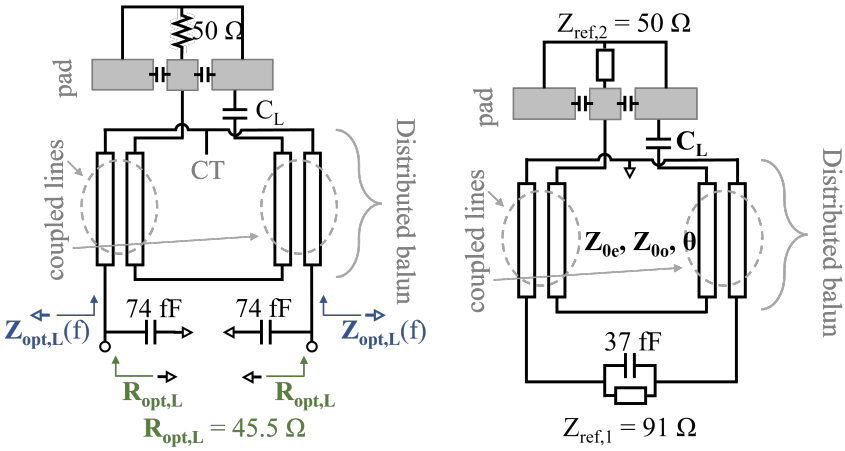
V_{th}-process variation and (ii) change the PA class of operation, at a small penalty of non-optimal load impedance. Indeed, load-pull simulations (**Figure G.7**) show that the optimal impedance remains roughly constant and close to the selected load impedance $Z_{opt,L}$ (black dot) with increasing V_{bg}.

G.1.2 Distributed output balun

Once the output stage is designed, load-pull simulations are performed at several frequencies to evaluate the optimal impedance to present at the output. Optimal large-signal power matching is achieved when reactive elements are compensated and the intrinsic loadline is purely resistive. Due to the nature of the output stage design, an equivalent impedance ($Z_{opt,L}$), made of a resistance and capacitance of 45.5 Ω ($R_{opt,L}$) and 74 fF in parallel (for each branch), maximizes the output stage large-signal performance over a large bandwidth, see **Figure G.8a**. The capacitance accounts for the overall capacitive couplings in the output stage that dominate the inductive ones and the resistance is related to the optimal loadline achieved for each stacked FET.

Design

The output matching circuit is shown in **Figure G.8a**. The design of the output balun is based on the slightly modified equivalent circuit shown in **Figure G.8b**, which converts a 50 Ω load in the required differential optimal load impedance (represented by the parallel 37 fF capacitance and 91 Ω reference impedance



(a) Sketch of output matching design with optimal load impedance. **(b)** Sketch of distributed balun design, along with design parameters.

Figure G.8

port). The impedance transformation criterion corresponds to minimizing $|S_{11}|$ in the configuration shown in **Figure G.8b**, which is easier to define in an optimizer tool.

The impedance transformation performed in **Figure G.8** takes into account the probe pad capacitive coupling and is realized with a series capacitor (C_L) at the output and a pair of (asymmetric) coupled transmission lines (TLs). The pair of coupled TLs forms a transformer. Using a distributed element (coupled TLs) to model a transformer, as in **[200]**, has the advantage of being more accurate over a large bandwidth than a lumped-based model. Furthermore, it contains few design parameters (even- and odd-mode characteristic impedance Z_{0e} and Z_{0o}, respectively, and electrical length θ), which is convenient for an optimizer tool.

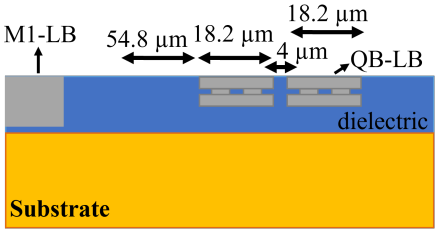
Initially, symmetric coupled lines are used, but due to the presence of ground on a single side, a more accurate asymmetric model is used afterwards for fine tuning. Once the design parameters for the coupled TLs are known, the lines are laid out and simulated via Keysight Momentum. Thanks to the rich BEOL available in this technology, several options to design the coupled TLs are possible. Lines made in 18.2 µm-wide stacked QB-LB with a gap of 4 µm and a distance of 54.8 µm to the stacked M1-LB ground resulted in the

lowest insertion loss. A sketch of the designed coupled lines cross-section is given in **Figure G.9a**. A top view of the output matching network is shown in **Figure G.9b**, with the distributed balun, output pad, series capacitor, bias feed and decoupling capacitors.

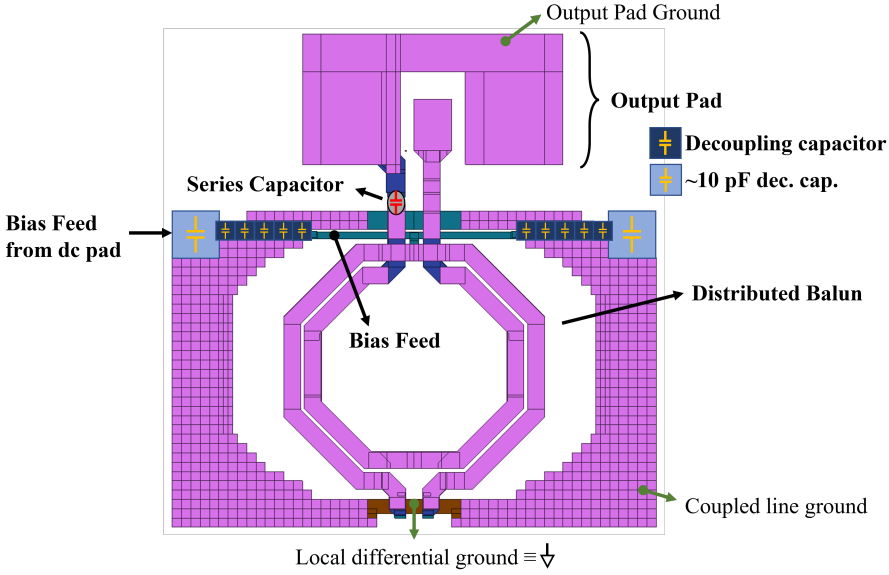
Sources of asymmetry

It is also interesting to note from **Figure G.9b** that the probe pad ground and the local coupled line ground (that is also connected to the differential ground) are not connected on-chip. This voluntary disconnection is made in order to reduce the asymmetry at the balanced ports **[188]**. Indeed, if the output pad ground were to be connected to the coupled line ground (blue ground symbols), as shown in **Figure G.10a**, one impedance would see a short connection to ground ($Z_{a,1}$) while the other would see a network of 50 Ω resistance and capacitances ($Z_{a,2}$), and they would be very different. In case that the output pad ground is disconnected from the coupled line ground, there is still capacitive coupling between the nodes as shown in **Figure G.10b**. Since the ground pads couple much more to the differential ground than the signal pad, there is still an imbalance in the differential impedances, but it is greatly reduced than if the grounds were connected ($|Z_{b,1} - Z_{b,2}| \ll |Z_{a,1} - Z_{a,2}|$). This imbalance in output differential impedances is transferred in unbalanced differential impedances at the output stage side due to interwinding capacitances of the transformer.

Another source of potential imbalance is asymmetric center tap connections. Indeed, in order to ensure a virtual differential ground at the center tap connection to the transformer winding the center tap connections should be symmetric. In that case, the PA differential operation is insensitive to any impedance connection at the center tap, as it would come in parallel to a shorted ground node. In practice, however, the transformer's center tap is used to bring the V_{dd} bias from a dc pad on a single side of the PA only. This is source to additional imbalance in the differential topology. In this PA, we have replicated the V_{dd} bias line, including decoupling capacitors along the bias line and the large $\sim 12\,\text{pF}$ capacitor under the dc pad, on both sides of the transformer to ensure the highest level of symmetry implementable on-chip. The remaining asymmetry consists of large additional decoupling surface-mount (SMD) capacitors ($\geq 1\,\text{nF}$) soldered on the dc probe needles, only present at one side of the PA. This option was preferred instead of adding series spiral inductors (to increase the bias line impedance and reduce the imbalance due to an asymmetry) in the bias line, because of a lower area consumption and because large-signal simulations showed better 2$^{\text{nd}}$ and 3$^{\text{rd}}$ harmonic linearity when the center tap of



(a) Sketch of designed coupled lines cross-section, with main dimensions.



(b) Top view of designed output matching.

Figure G.9

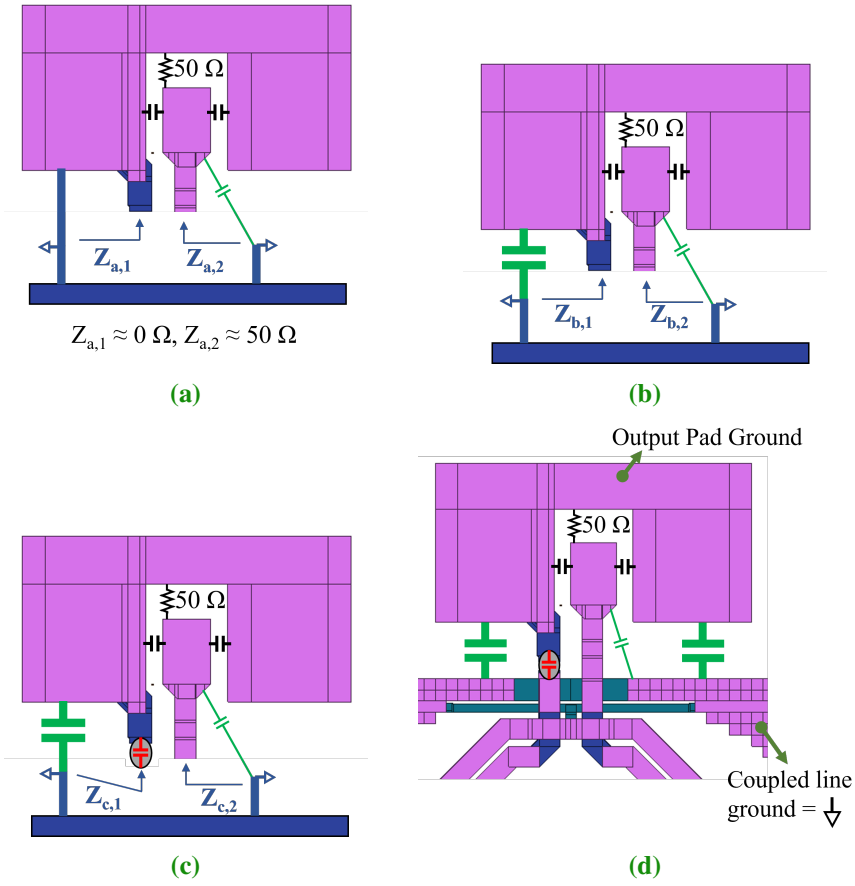


Figure G.10: Sketch of possible connections between probe pad ground and coupled line ground (blue bottom rectangle and blue ground symbols) and impedances seen from the output terminals to the differential local ground of the output stage. (a) shorted, (b) disconnected, coupling capacitively, (c) disconnected with series capacitor for matching, (d) overall sketch of final design.

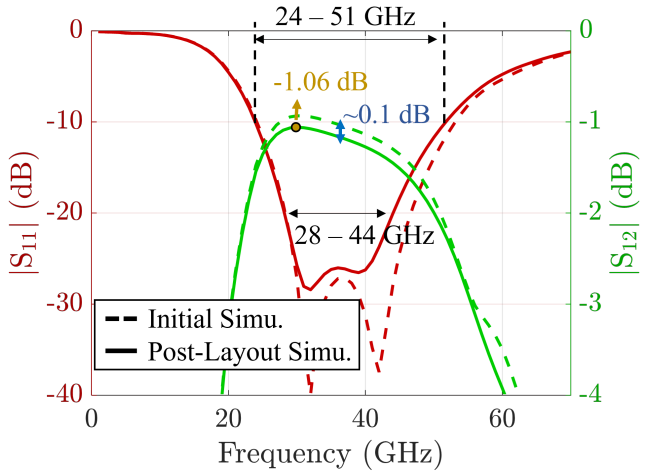


Figure G.11: $|S_{11}|$ (left axis) and $|S_{12}|$ (right axis) of the designed output matching network in the configuration shown in **Figure G.8b**. Initial design simulations in dashed lines. Adjusted post-layout simulations based on hardware in solid lines.

the designed output balun is connected to large decoupling capacitors.

Simulation results

The simulated 2-port S-parameters, corresponding to the equivalent circuit of **Figure G.8b**, including the bias feed line and decoupling capacitors up to the dc pad, are shown in **Figure G.11**.

The resulting output matching features a return loss larger than 10 dB from 24 to 51 GHz and above 20 dB from 28 to 44 GHz, therefore accurately achieving the desired impedance transformation. The insertion loss is non-negligible, but remains controlled over the entire designed frequency range: $\sim 1-1.5$ dB from 24 to 45 GHz. Furthermore, it should be reminded that these simulations include all losses from the output of the FETs up to the probe tips. Initial design simulations are shown in dashed lines. The distributed balun (along with the output probe pad) is also designed as a standalone structure for characterization. The results of this structure and adjusted simulations to better agree with measurements are described shortly after. These new simulations are in solid lines in **Figure G.11**.

Finally, a 3-port simulation is carried out in a configuration close to the

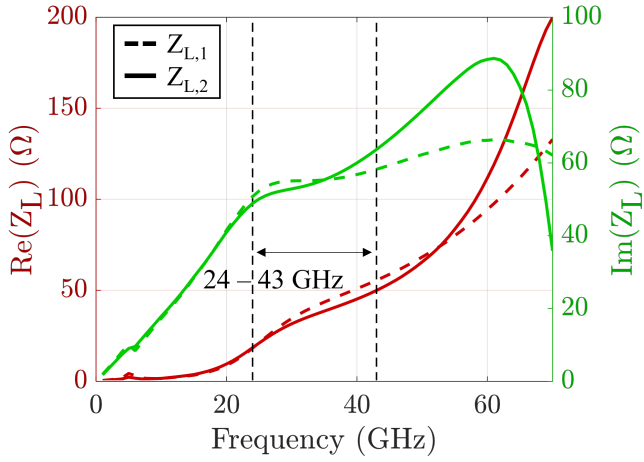


Figure G.12: Balance impedance simulation. Load impedance seen from the output of each branch to the common differential ground for the designed output matching.

one represented in **Figure G.8a**, including the bias feed line and decoupling capacitors, in order to check that the impedances seen by each branch of the output stage are well balanced. Results shown in **Figure G.12** indicate that the special care for symmetry described in the previous paragraphs has paid off, as only a small residual imbalance remains ($|2\Delta Z_L/(Z_{L,1}+Z_{L,2})| < 10\,\%$ from 24 to 43 GHz).

Measurements

The whole output matching, consisting of the distributed balun, the series output capacitor, output probe pad and bias feed with decoupling capacitors, is also designed as a standalone structure for 2-port characterization. A picture of the measured structure is provided in **Figure G.13**. A pad is inserted at the place of one of the PA's output stage branches and the other branch is replaced by a lumped 45.5 Ω resistor in parallel with a 74 fF capacitor. The input (port 1) pad is de-embedded with Open and Short structures. An additional fictitious shunt capacitor is mathematically added at port 1 after de-embedding and the port 1 reference impedance is transformed to 45.5 Ω. With such mathematical manipulations, from the resulting 2-port S-parameters, we can derive the actual transmission from the differential output stage to the output probe pad (assuming the two branches are balanced, which is not exactly the case as discussed above).

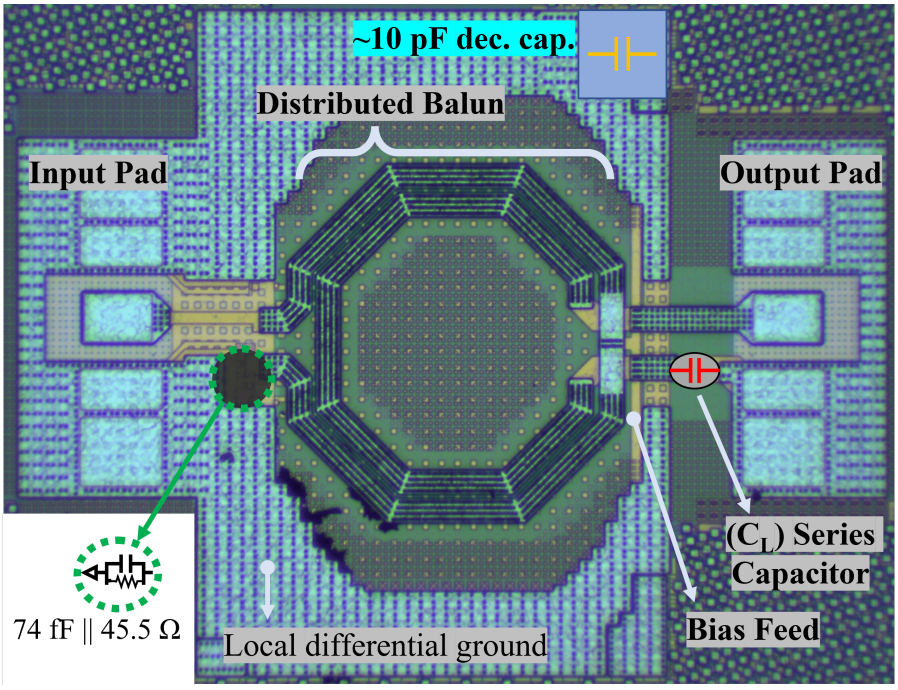


Figure G.13: Picture of the standalone output matching network structure.

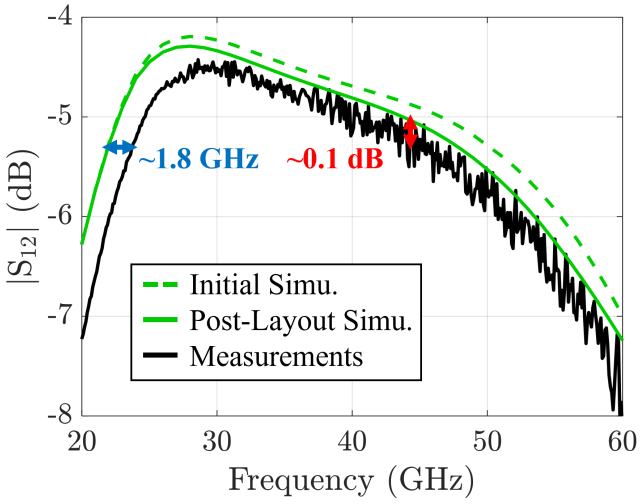


Figure G.14: Simulations (green) and measurements (black) of the standalone output balun and matching.

However, the output balun as a standalone structure and the actual one used in the PA have a few differences. In the PA, the left and right ground sides (at the output stage side) are connected via an under-bridge in M1-JA, which represents a non-negligible impedance, whereas in the standalone structure, the left and right ground sides are connected via the input pad ground pads through a low impedance path. Another significant difference is the absence of the large ($\sim 10\,\text{pF}$) decoupling capacitance on one side of the balun (as shown in **Figure G.13**), it is a mistake made during design. Due to these differences, this standalone structure is rather used to validate the EM model of the standalone structure that is also used in the final PA.

The structure measurements and simulations are shown in **Figure G.14**. A good agreement is obtained between the adjusted simulations (solid green lines) and measurements (black). There is still a slight underestimation of transmission loss ($\sim 0.1\,\text{dB}$ across the whole range) and a slight shift in frequency (1.8 GHz). The post-layout (adjusted) simulations describe better the frequency response of the output matching network, mainly at higher frequencies. The adjusted simulations result in a different EM stack from a non-typical corner simulation with the addition of an edge mesh at 200 nm that was not present in initial simulations.

Although the standalone structure and output matching in the PA are not exactly identical, thanks to the model-hardware correlation of **Figure G.14**, we can conclude that the adjusted simulations underestimate the transmission losses by 0.1 dB and the actual matching is shifted by ∼2 GHz toward higher frequencies.

G.1.3 Driver stage and input/inter-stage matching design

Driver stage

A schematic of the driver stage is shown above in **Figure G.1b**. The driver stage is designed with a differential pair of common source FETs and neutralization capacitors. The same unit FET cell as the output stage is used, but only repeated twice (total FET width of 80 µm). The overall interconnects and layout are similar to the output stage and are not shown here.

Inter-stage matching network

Load-pull simulations are performed to determine the appropriate wideband impedance to present at the output of the driver stage, in a similar fashion as the output load impedance of the power stage. It is found that the inter-stage matching network has to transform a 4.5 Ω resistance in series with a 80 fF capacitance (input of power stage as mentioned above) into the complex conjugate of a 46.4 Ω resistance in parallel to a 50 fF capacitance over the whole design bandwidth. As mentioned above, the inter-stage matching network is realized with a transformer, a lumped-based schematic can be found in **Figure G.15**. Due to the large resistance transformation ratio, to achieve such a wideband impedance transformation, a 365 Ω shunt resistor is added in parallel to the input of the driver stage.

This 365 Ω shunt resistor is designed as a parallel combination of several unit resistor cells of a given cross-section and length. The design of the unit resistor cell must take into account the large-signal power injected to the power stage. Increasing the resistor length makes it able to withstand larger power levels, but it increases its reactance (modeled by a series inductance in the PDK).

First, an unsilicided N+ diffusion type resistor in the SOI is selected to design the resistor, because of its low inductance value and high frequency model validation. Second, for a fixed resistor value, decreasing the resistor width, the resistor length decreases as well. The resistor reactance increases dramatically with larger resistor dimensions, so the minimum resistor width is

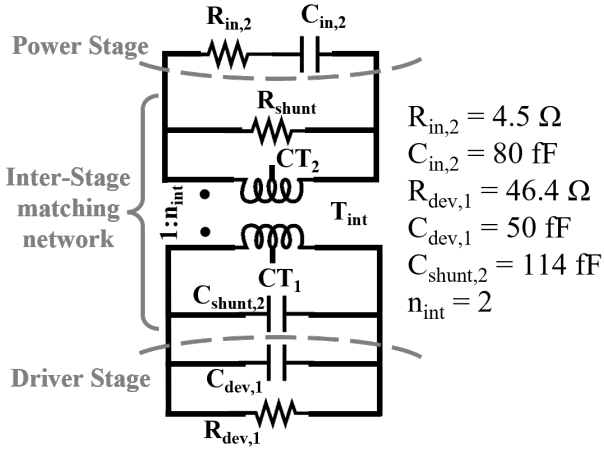


Figure G.15: Schematic of the inter-stage matching network.

chosen, i.e. 360 nm. Finally, the unit resistor length is selected as a trade-off between self-heating-induced local temperature increase and resistance-over-reactance ratio. To estimate the local temperature rise, we consider the worst-case situation, i.e. in saturated power condition. A resistor length below 3.7 µm leads to a $> 20\,^{\circ}$C increase in temperature as shown in **Figure G.16**. The shortest unit cell resistor giving a multiple of the targeted 365 Ω has a length of 4 µm, which still exhibits a dominance of the real part over the imaginary part (4 times larger) and suffer from a $\sim 17\,^{\circ}$C local temperature increase. Additional simulations show that this increased temperature results in only a 2 % increase in resistor value. So, the 365 Ω is made of a parallel combination of 6-unit resistor cells, each with a width of 360 nm and length of 4 µm.

Figure G.17 shows the simulated frequency response of the designed inter-stage matching network. A decent matching, implying a correct impedance transformation, is achieved from 26 to 44 GHz. This wideband impedance matching comes at the cost of low insertion loss caused by the presence of the shunt resistor.

Input matching network

The input matching network is designed in a similar way to the inter-stage matching (see **Figure G.18**). In this case, we aim at matching a 10 Ω resistance in series with a 41 fF capacitance (impedance seen at the input of the driver

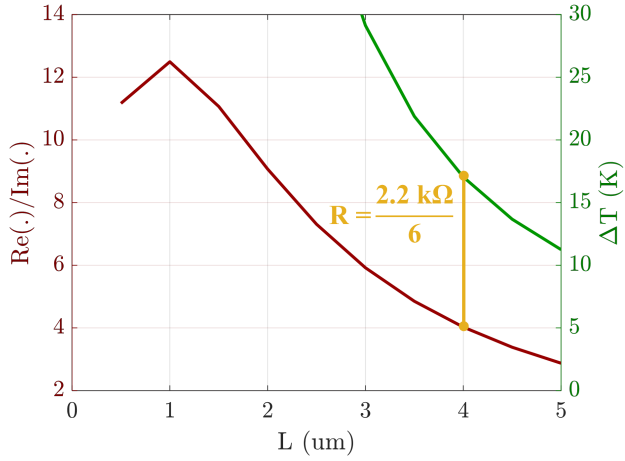


Figure G.16: Resistance-over-reactance ratio (left axis) and self-heating-induced local temperature rise (right axis) versus unit resistor length. Optimal length of 4 µm yielding a multiple of the target 365 Ω (2200/6).

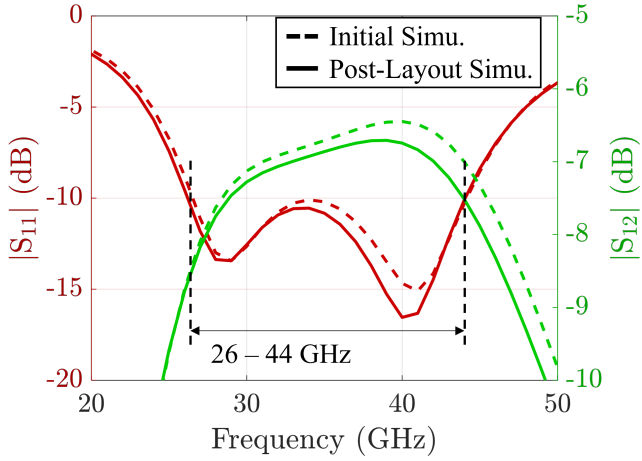


Figure G.17: $|S_{11}|$ (left axis) and $|S_{12}|$ (right axis) of the designed inter-stage matching network. Initial design simulations in dashed lines. Adjusted post-layout simulations in solid lines.

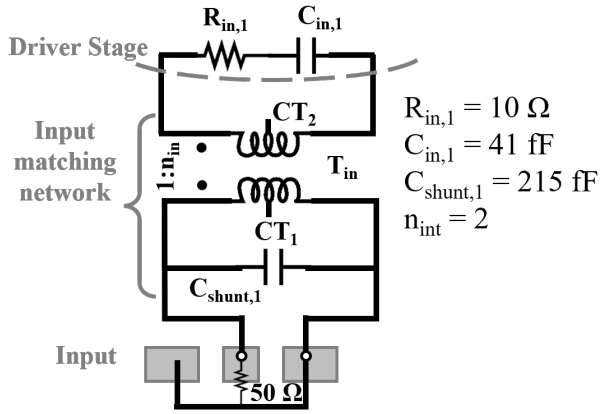


Figure G.18: Schematic of the input stage matching network.

stage) to the 50 Ω input port.

The simulated S-parameters of the input matching is shown in **Figure G.19**. The 10 dB input return loss is not met across the whole bandwidth, but the matching is designed to maintain a non-too steep amplifier gain drop at the 24 and 43 GHz bandwidth edges.

G.2 Configurable balanced PA (PA2): design

This section provides a detailed design overview of the configurable balanced PA (PA2). First, the high-power 50 Ω resistor design is explained. Then, we discuss about the hybrid coupler design, providing a procedure to converge toward an optimized design. After, we present the design of the switchable capacitor. Finally, we show how simulations are tuned with an equivalent substrate impedance to achieve a good agreement between measurements and simulations.

G.2.1 High power resistor

In case of load mismatch, a significant portion of the high power reflected at the load ends up dissipating in the 50 Ω resistor present in the output hybrid coupler. Thus, special care has to be taken when designing this resistor.

Assuming an ideal 90° hybrid coupler, the power dissipated in the 50 Ω resistor is

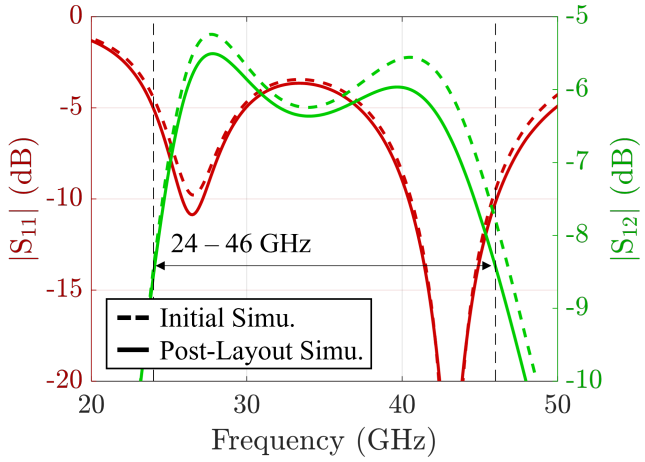


Figure G.19: $|S_{11}|$ (left axis) and $|S_{12}|$ (right axis) of the designed input stage matching network. Initial design simulations in dashed lines. Adjusted post-layout simulations in solid lines.

$$P_{50\,\Omega} = \frac{1}{2}|\Gamma_{\text{load}}|^2|\Gamma_{\text{amp}}|^2 P_{\text{amp}}, \tag{7.2}$$

where Γ_{load} is the reflection coefficient at the load, Γ_{amp} is the output reflection coefficient of the PA unit cell (assumed identical in both branches), and P_{amp} is the available power delivered by the PA unit cells. Considering the worst-case situation for a VSWR of 5 : 1 (Γ_{load} of -3.5 dB), a $\Gamma_{\text{amp}} = -1$ dB return loss at the PA unit (it corresponds to the worst $|S_{22}|$ measured value, which is very conservative, as the output should be matched in high power condition) and saturated power of 19 dBm, the maximum power dissipated in the resistor is 11.5 dBm. It corresponds to an rms current of 16.8 mA flowing through the 50 Ω resistor.

Due to the high current potentially flowing through the load, it has to be designed with metal lines that can better withstand electromigration. Thin and resistive metal layers in Cx with the widest allowable signal trace are used. They can support an rms current up to 10.5 mA. So, two parallel 100 Ω resistors are designed, such that the current flowing through each resistor is only half, reducing the electromigration stress on the metal lines.

To achieve a 100 Ω resistance, long metal lines must be used ($\sim$ 1 mm-long

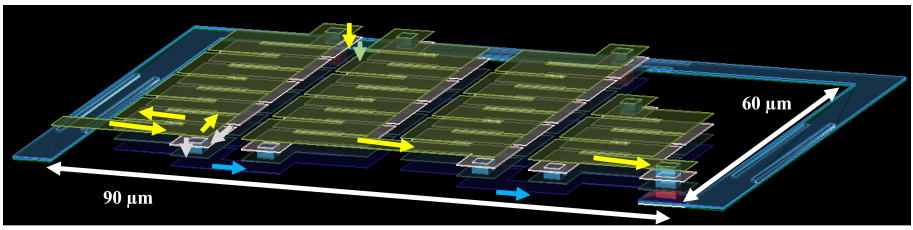


Figure G.20: 3D view of the designed high power 100 Ω resistor surrounded by a ground ring. Only half of the full 50 Ω resistor is shown, which consists of two parallel 100 Ω resistor with a common closed ground ring. The current flow on different metal layers is shown with arrows of different colors, The generated magnetic field is greatly reduced thanks to the current flowing in opposite directions in the meanders and on different metal layers. The vertical spacing between different metal layers has been magnified for better illustration.

straight line in Cx for 100 Ω), along with a strong reactive component. To design a compact and resistive high-power resistor, the strategy described in **[192]** is adopted. It consists of building a zigzag signal line (for a compact size) in several metal layers connected in series as depicted in **Figure G.20**. Negative mutual coupling (vertically between different metal layers and horizontally between different branches) largely compensates for inductive parasitics. Horizontal negative mutual coupling is however limited due the metal density being bounded to a maximum value. Nevertheless, the remaining inductive parasitics can be compensated by the capacitive coupling to the surrounding ground ring, with an appropriate branch length. The resulting 50 Ω resistor dimensions are shown in **Figure G.20**. The simulation results are shown in **Figure G.21**.

This structure is also designed as a standalone component for a detailed 1-port characterization. In this 1-port structure, the measured impedance includes a mainly inductive component accounting for the return path between the other end of the resistor (L_{ground}) and the ground reference plane after de-embedding (see **Figure G.22**). The initial simulation is performed with the nominal EM stack, while the post-layout simulation includes an edge mesh at 200 nm and uses a non-nominal EM stack that better fits the measurements. Despite a small variation with expected simulations, the achieved reflection coefficient (cf. **Figure G.21b**) remains around −20 dB from 20 to 50 GHz, well covering the PA operating bands.

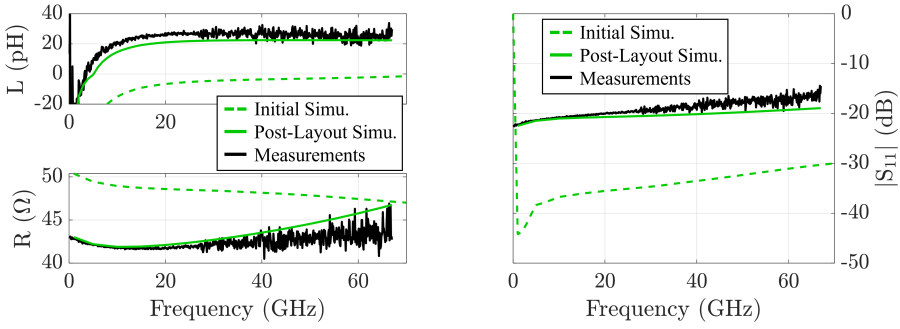


Figure G.21: High power 50 Ω resistor measurements (black) and simulations (green). Equivalent R-L series circuit (a) and reflection coefficient (b). Initial design simulations in dashed lines. Adjusted post-layout simulations in solid lines.

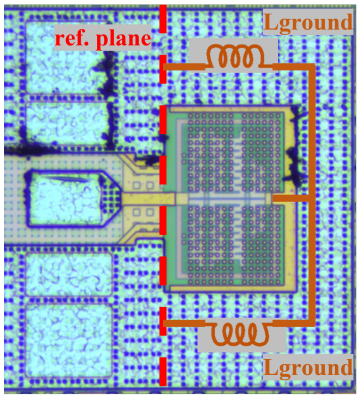


Figure G.22: Picture of fabricated high power 50 Ω resistor.

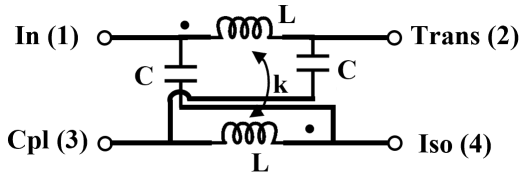


Figure G.23: Equivalent lumped element schematic of the hybrid coupler.

G.2.2 Quadrature hybrid coupler

The configurable hybrid coupler design is based on a topology made of coupled transmission lines and described in [191]. This topology has proven to (i) be compact, (ii) have low insertion loss and good robustness to at least 3 : 1 VSWR conditions, (iii) have appropriate ports position for integration in a balanced amplifier topology, and (iv) tunable capacitors can be easily integrated [191, 192].

Design

The design of the hybrid coupler is based on the topology described in [191]. The hybrid coupler is represented by the simple lumped element schematic of Figure G.23.

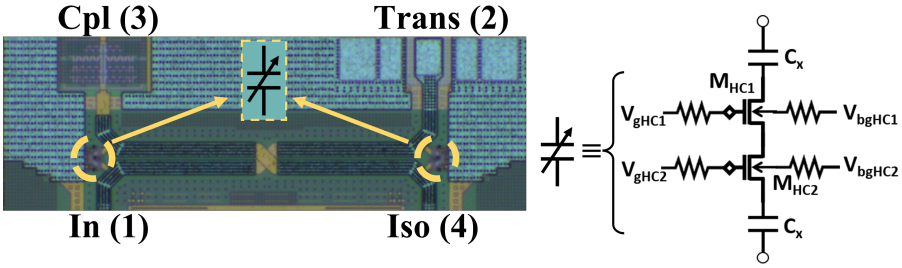
Design equations relating the (L,C,k) parameters to the operation frequency (ω_0) and the hybrid coupler's reference impedance (Z_0) are

$$Z_0 = \sqrt{\frac{L_0}{2C_0}}, \text{ and } \omega_0 = \frac{1}{\sqrt{(2L_0C_0}}. \tag{7.3}$$

Since the coupling between inductors is non-ideal ($k < 1$), both inductive and capacitive parts (L and C) should increase to compensate the lower k. A right approximation for $0.8 \leq k \leq 1$ linking L_0 and C_0 from Equation 7.3 to L and C is

$$L = (2-k)L_0, \text{ and } C = (2-k)C_0. \tag{7.4}$$

To reduce insertion loss due to mismatch, Z_0 should be as close as possible to $50\,\Omega$ (reference impedance of each port). In practice, the hybrid coupler is made of two pieces of coupled transmission lines connected together with



(a) (b)

Figure G.24: Configurable quadrature hybrid coupler description (a), schematic of tunable capacitor (b).

an odd number of twisted elements, in order to have the ports in a convenient position to connect two PA cells in a balanced topology, see **Figure G.24a**. The targeted L and C are proportional to the total length of the coupled transmission lines, i.e. the larger L and C, the longer the lengths. So, insertion loss can once again be minimized by reducing L and C, i.e. by increasing the coupling k. Nevertheless, since this hybrid coupler is designed to be embedded in a balanced PA topology using the wideband PA described above as the unit cell, a minimum length of the hybrid coupler is required, corresponding to the vertical distance of output ports from two distributed output baluns (from **Section 5.3.1**) stacked vertically (it is better visualized later in **Figure 5.36** showing a picture of the fabricated balanced PA2).

To cover all bands from 24 to 43 GHz, the hybrid coupler is made tunable with the addition of lumped switchable capacitors at each end (see **Figure G.24a**). The switchable capacitor is designed by the series combination of lumped mom capacitors and two FETs in a switch configuration (as shown in **Figure G.24b**), such that it switches between three states, each with distinct values of capacitors designed to work in one of the 24-29 GHz (FR2 n257 and n258), 30-33 GHz and 37-43 GHz (FR2 n259 and n260) bands.

The lowest capacitance value corresponds to the highest frequency of operation (39 GHz) and is achieved by turning both FETs off (State 1). Its value is therefore dominated by the C_{off} capacitance of the smallest FET (MHC2). For the other states, MHC2 is turned on and its on-resistance (R_{on}) induces losses in the overall hybrid coupler. For a given technology, the product $R_{on}C_{off}$, a switch FoM, is fixed. In 22FDX, its value is around 100 fs **[193, 264]**, but can

be further reduced with specific interconnect design as it will be shown later on. Therefore, to reduce losses caused by the smallest FET (with largest R_{on} and lowest C_{off}), the lowest capacitance value of the switchable capacitor is limited by the corresponding R_{on} from the smallest FET. From experience, this lowest value should be above 10 fs for a reasonable increase in loss at other states due to R_{on}.

The total L_0 and C_0 describing the behavior of the overall hybrid coupler are then

$$L_0 \approx \frac{L}{2-k}, \text{ and } C_0 \approx \frac{C}{2-k} + C_{tune}, \tag{7.5}$$

where C_{tune} is the switchable capacitor. When switching from one state to another, the L_0 term remains constant and C_0 (via C_{tune}) takes increasing values for states decreasing in frequency $f_{0,1} = 39\,\text{GHz}$ (state 1) $> f_{0,2} = 32\,\text{GHz}$ (state 2) $> f_{0,3} = 28\,\text{GHz}$ (state 3), respectively. The reference impedances also change with lower values at lower frequency states. The lowest frequency state (state 3, 28 GHz) features the lowest reference impedance, we do not want it to be too small, as it would cause mismatch and reduce the insertion loss. A reasonable value is $Z_{0,3} > 35\,\Omega$, which fixes a minimum bound for $Z_{0,1}$ of $49\,\Omega$ ($Z_{0,3}/Z_{0,1} = f_{0,3}/f_{0,1}$). As the wideband PA is performing better (with larger output power and efficiency) at the lower frequency bands, we design this hybrid coupler to minimize insertion loss at the highest frequency band (39 GHz) and allow some mismatch ($Z_{0,3} > 35\,\Omega$) at the lower frequency bands.

Furthermore, we define Z_h and f_h, the reference impedance and operation frequency of the hybrid coupler *without* the switchable capacitor.

$$Z_h = \sqrt{\frac{L}{2C}}, \text{ and } 2\pi f_h = \frac{2-k}{\sqrt{LC}}. \tag{7.6}$$

The design procedure consists in the following:

1. Based on a first estimation of k and C_{tune}, compute the required Z_h and f_h. For a desired hybrid coupler length d, compute the inductance (L_n) and capacitance (C_n) per unit length, such that $L = dL_n$ and $C = dC_n$.
2. With EM simulations, find a coupled transmission line cross-section that yields the target Z_h, k and L_n (or C_n, L_n and k, equivalently).
3. Perform an EM simulation of the coupled transmission line of length d, add lumped C_{tune} capacitors at each end and verify the correct operation

of the resulting hybrid coupler. In case the operating frequency is not 39 GHz, fine tune C_{tune} to shift the operation frequency to the target 39 GHz. Based on **Equation 7.4**, **Equation 7.5** and **Equation 7.6**, the reference impedance can be rewritten as

$$Z_0 = \sqrt{\frac{dL_n}{2(C_{tune}(2-k)+dC_n)}}. \tag{7.7}$$

   (a) If $C_{tune} < 10\,\text{fF}$ (significant losses due to R_{on} in the switchable capacitor), decrease k and go back to step 1. If not, go to 3.b.
   (b) Compute the hybrid coupler reference impedance, Z_0. If $Z_0 < 50\,\Omega$, increase k and go back to step 1.
   (c) Check the insertion loss and iterate with step 2 to find a cross-section that minimizes the insertion loss.

4. Design and simulate a twist element to be introduced in the middle of the pair of coupled transmission line. This twist element adds more capacitance than inductance compared to the remaining of the coupled transmission line, such that C_{tune} should decrease to keep the same operation frequency. If $C_{tune} < 10\,\text{fF}$, decrease k and go back to step 1.

The resulting hybrid coupler should work at the desired frequency range, with a lumped C_{tune} capacitor at each end. The final step to the configurable hybrid coupler is the design of the switchable capacitor.

Switchable capacitor

Once the hybrid coupler layout is designed, values of C_{tune} for each state can be determined to correctly fix the operation frequency. As shown in **Figure G.24b**, the switchable capacitor is made of two mom capacitors in series with two FETs in a switch configuration (with large bias resistors at the gate and back-gate accesses). In off- or on-state, each FET can be modeled by a C_{off} or R_{on} element, such that the switchable capacitor has the equivalent circuits shown in **Figure G.25** in each state. The low frequency state determines the value of the mom capacitors. The intermediate state fixes the C_{off} value (and therefore total width) of the larger FET (MHC1) and the high frequency state fixes the C_{off} (or width) of the smallest FET (MHC2). Super-low threshold voltage nFET are selected for MHC1 and MHC2, because they feature the lowest $R_{on}C_{off}$ FoM in this technology **[194]**.

Thanks to the mom capacitors, no dc current flows in the switchable capacitor. In that case, electromigration constraints are relaxed, since only rules

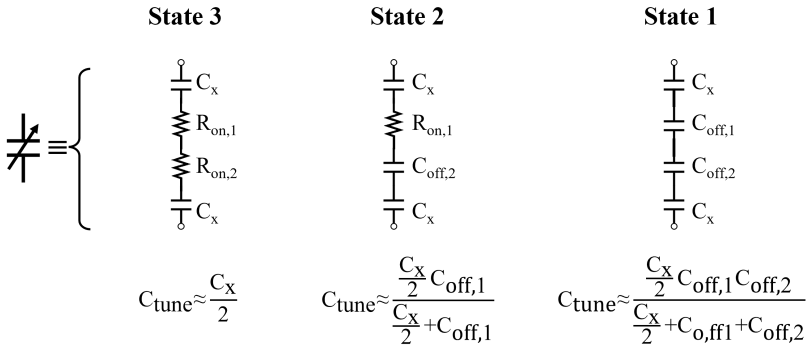


Figure G.25: Equivalent circuit of switchable capacitor for each state and equivalent capacitance value.

related to rms and peak current must be checked. Due to the low C_{off} value of MHC2, its interconnects are specially designed to reduce parasitic capacitance, while verifying electromigration rules, hence lowering the $R_{on}C_{off}$ FoM. With tapered M2-Cx interconnects at the drain and source terminals in a similar way to the FETs in the PA stages, a simulated $R_{on}C_{off}$ of $\sim 60\,\text{fs}$ could be achieved, thereby lowering the R_{on} for a specific C_{off}, which is essential to reduce losses at the low frequency states.

Furthermore, it has been previously shown that a simple R_{on} or C_{off} model of SLVT FETs is not accurate at mm-wave frequencies **[194]**. Indeed, due to the thin buried oxide and the moderately conductive standard silicon substrate ($10\,\Omega\text{cm}$), shunt elements must be added to accurately predict the behavior of a FET connected in switch configuration above a few tens of GHz. In **[195]**, the authors propose to add a BFMOAT region around the FET to increase the shunt impedance and therefore reduce its impact at high frequency, while keeping the advantages of a back-gate bias access. In this work, a BFMOAT ring is similarly designed around each element of the switchable capacitor and, more importantly, between these elements and the nearby ground. The substrate impedance connecting a common ground node of the switchable capacitor and a pin from the nearby hybrid coupler ground (it can visualized on the right side of **Figure G.26**) is represented by a parallel R_{sub} and C_{sub}, which values are discussed in the following.

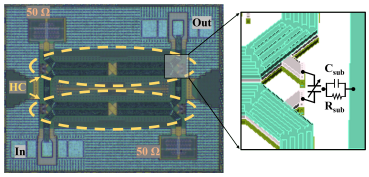


Figure G.26: Fabricated structure for standalone hybrid coupler (HC) characterization, with representation of equivalent substrate impedance ($R_{sub} \parallel C_{sub}$) between a common ground node of the switchable capacitor and a pin from the nearby hybrid coupler ground. The standalone structure consists of two cascaded hybrid couplers, dc pads are not shown.

Results

The hybrid coupler is also designed as a standalone structure for proper characterization. To that end, two identical hybrid couplers are cascaded to end up with a 2-port structure (the two other ports are connected to two specially designed 50 Ω high-power resistors described above) to replicate the hybrid coupler interconnections when integrated in the balanced PA structure. A picture of the structure is given in **Figure G.26**.

The measurement reference plane is at the probe tips, so only an LRRM calibration is performed (with Infinity I67 probes) on the 101-190C calibration substrate without additional de-embedding. Measurements and simulations of the cascaded hybrid couplers are shown in **Figure G.27**. Initial simulation of the hybrid coupler is shown in dashed lines, in which the substrate impedance is modeled by a large resistance ($R_{sub} = 10\,\text{k}\Omega$), thus with negligible shunt loss contributions. Adjusted EM simulations (with the addition of an edge mesh at 200 nm) are shown in dotted lines. Even with this adjustment in EM simulation setup (or with other EM stack corners), simulations do not closely fit measurements in all states.

Another parameter that was neglected (modeled by very large $10\,\text{k}\Omega\,\text{cm}$ resistance) at design time is the coupling between the switchable capacitor and the nearby ground from the hybrid coupler through the substrate. Here, we introduce an equivalent substrate impedance with parallel resistor and capacitor elements (R_{sub} and C_{sub}). By varying R_{sub} and C_{sub} values, we get a best agreement for $R_{sub} = 800\,\Omega$ and $C_{sub} = 6.6\,\text{fF}$, whose product is associated to an equivalent resistivity of the Si substrate of $5\,\Omega\,\text{cm}$. The simulations with these elements' values yield what we shall use as *adjusted post-layout simulations* in

the following.

Note that the initial to adjusted EM simulations have a $\sim 0.3\,\text{dB}$ of difference, and the addition of this non-negligible substrate impedance degrades the results by another $\sim 0.2\,\text{dB}$. Indeed, as soon as this substrate impedance is below a few kΩ, it has a strong impact on insertion loss: as seen by the dotted lines, mostly at the higher frequency bands when one or more FETs are in off-state. Although these degradations could partially be corrected by a re-design of the hybrid coupler, the substrate equivalent network impact could probably be neglected using a higher resistivity substrate.

The good agreement of post-layout simulations with measurements enables a confident extraction of the hybrid coupler characteristics via simulations as integrated in the balanced PA (the measured structure consists of two cascaded hybrid couplers). **Figure G.28** shows the post-layout simulated $|S_{13}|$ and $|S_{23}|$ as well as the phase difference for the different states. A good phase quadrature is achieved in post-layout simulations as well as insertion loss (1.2, 1.2 and 1.3 dB at 27, 32 and 39 GHz, respectively) in all states.

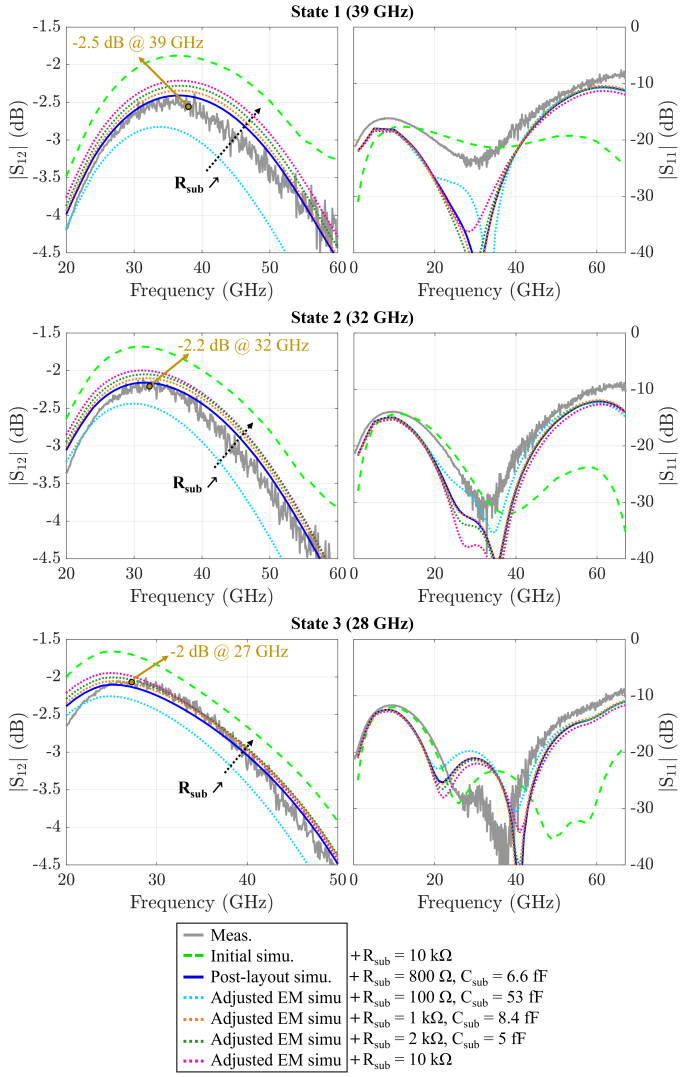


Figure G.27: Measurements (grey) and simulations of the cascaded hybrid couplers in three different states, state 1 (a), state 2 (b), state 3 (c) and legend.

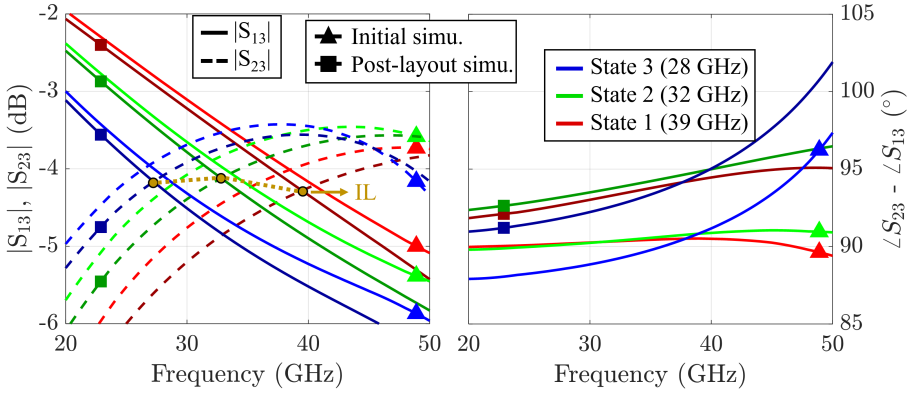


Figure G.28: Simulations of the resulting hybrid coupler performance: S_{13} and S_{12} magnitude (left) and phase difference (right).

H. 110 GHz MOSFET Characterization: Second Calkit Design Without Ground Plane

This appendix presents preliminary characterization results from a second calkit designed without a ground plane covering the whole chip for accurate MOSFET measurements. It also provides perspectives for future work to reduce the residual probe-dependent errors for MOSFET measurements.

H.1 Second Calkit Design

As we have seen in **Chapter 4**, significant residual error is present in high frequency measurements that might lead to wrong or inaccurate MOSFET model parameter extraction. Although a high accuracy is achieved for most relevant parameters below 70 GHz, the uncertainty is larger for R_g (and f_{max}) and in general above 70 GHz due to residual probe-dependent errors. Let us discuss about potential ways to improve the measurement accuracy.

These probe-dependent errors have been identified in **[40]** to mostly come from un-wanted probe coupling with the on-wafer environment (mainly for I110 probes) and probe to probe crosstalk.

Concerning probe to on-wafer test structures coupling, there are mainly two ways to approach it.

- Either there is no homogeneous ground plane covering the whole chip, connecting all structures. In that case, measurement accuracy is degraded by substrate modes propagation excited by the probes (already explained in details in **Chapter 2**) or slot modes between devices **[31, 116]**. General recommendations for calkit design in that case have also been provided in **Chapter 2**. It consists of using a dielectric chuck of permittivity larger than the test substrate and spacing each structure far away enough so that

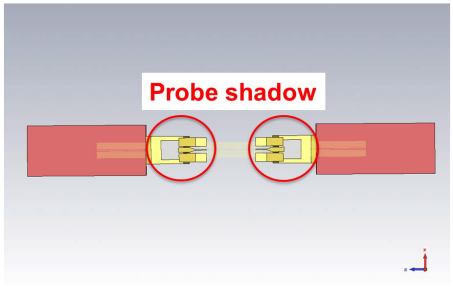


Figure H.1: 'Probe shadow': critical area below the probes [215].

neighboring structures are not under the 'probe shadow'.

- Or a ground plane covering the whole chip is designed. It was proposed in [31, 116]. The idea is to present a similar environment for the measurement of each structure. However, we have seen that the probe couples strongly with the on-wafer environment and that it changes significantly from one structure to another, and, because of that, the in-situ calibration fails at correcting the associated errors. In that case, [90] also provides as recommendation to not place structures below the 'probe shadow'.

In both cases, the main recommendations consists of spacing the structures by a large distance (from each other and from the chip edge) to avoid parasitic coupling. The 'probe shadow' (effective area on the lower side of the probe, shown in **Figure H.1**) is relatively large: the solder joint of the I110 probe is $\sim 500\,\mu m$ away from the probe tips for instance. So, they recommend spacing each structure by $\sim 800\,\mu m$. This spacing is too large in practice for advanced CMOS technology as the chip area is proportional to the chip price. So, other means for measurement accuracy improvement have to be investigated.

As we have identified probe coupling to the on-wafer ground plane to be harmful to I110 probes measurements, let us briefly investigate the ground plane removal. A second calkit design in the same technology has been realized in which there is no longer a ground plane covering the whole chip. The pads and transmission lines designs are slightly different. The Thru length is a bit longer too (probe-to-probe distance of $250\,\mu m$ instead of $105\,\mu m$ for the calkit presented here). A picture of the designed calkit is shown in **Figure H.2**. The spacing between each structure is of $110\,\mu m$ in x-direction and $40\,\mu m$ in y-direction.

The measurements of the transmission line standards are shown in **Figure**

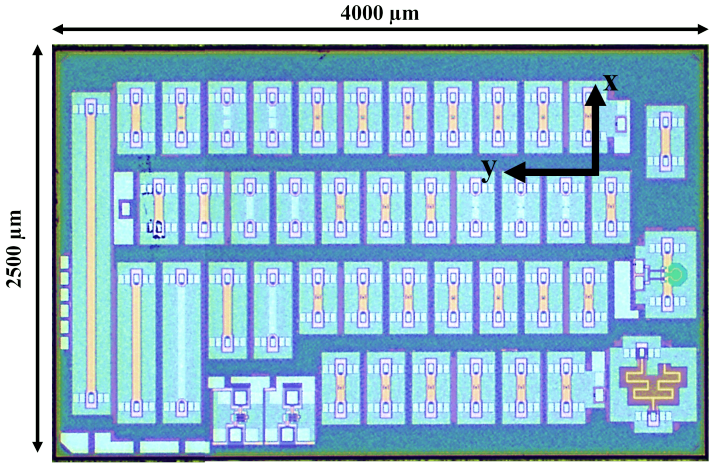


Figure H.2: Picture of the second calkit.

H.3 for two pairs of probes: I110 and TITAN. The measured propagation constant exhibits probe-dependent bumps that are not consistent with the expected intrinsic line behavior, in a similar way as the first calkit design.

A 20 nm gate length transistor from the same 22FDX® technology is measured. The extrinsic series resistances are used to evaluate the high-frequency measurement accuracy as in **Chapter 4**. The results for the I110 probe measurements are shown in **Figure H.4**. $\mathrm{Re}(Z_{22})$ and $\mathrm{Re}(Z_{11} - Z12)$ clearly still feature some unwanted bumps, without any evident improvement compared to the previous calkit in **Section 4.1**.

Even by removing the ground plane covering the whole chip, no significant improvement or degradation is observed in the extracted extrinsic series resistances. Additional experiments could be performed, for instance by placing the substrate on a ceramic chuck (ideally with similar or larger permittivity) to confirm the above observation.

H.2 Perspectives

In both layout design approaches, the main recommendations to reduce the parasitic probe-dependent effects consists of spacing the structures by a large distance (from each other and from the chip edge) of $\sim 800\,\mu$m to avoid parasitic coupling. However, this spacing is too large in practice for advanced CMOS

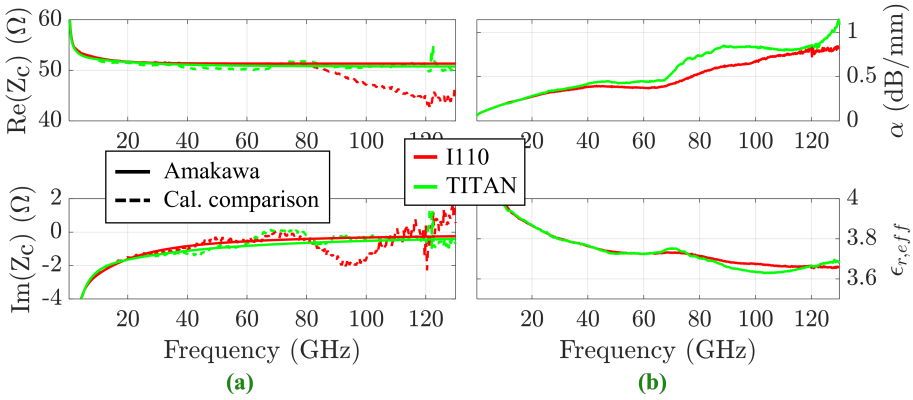


Figure H.3: Extracted characteristic impedance (a) and propagation constant (b) from transmission line standards measurements.

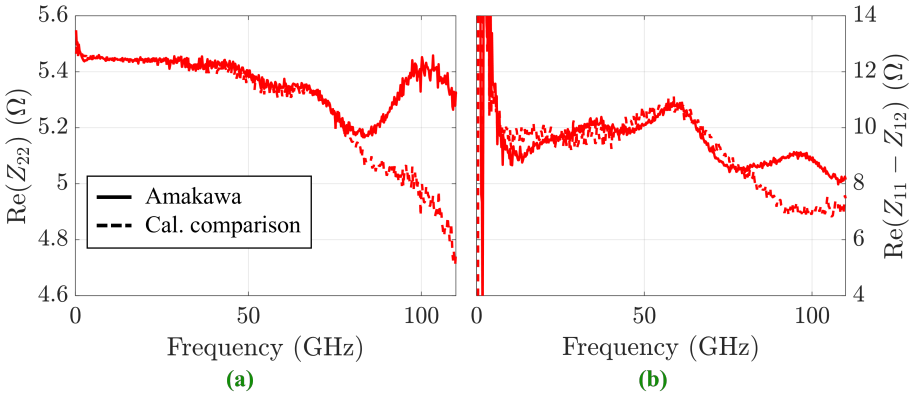


Figure H.4: Measurement of a *second chip version*. Re(Z_{22}) (a) and Re($Z_{11} - Z12$) (b) from cold FET measurement biased in strong inversion. Data corrected by 2-tier calibration with Open-M1-Short-M1 de-embedding. Comparison between different Z_c extraction (for second-tier calibration) methods **[74]** (dashed lines) and **[24]** (solid lines), for I110 probe measurements.

technology as the chip area is proportional to the chip price. So, we might need to change the way we approach the problem.

Another way to deal with such parasitic coupling effects would be to include them in the calibration process, thus improve measurement accuracy. As briefly mentioned in **Chapter 2**, the 16-term error model should account for all possible port leakages and crosstalks. A simplified version and a full version have been applied to on-wafer measurements in **[31]** and **[213]**, respectively. Both show great improvements in measurements, resulting in more well-behaved curves and better band-to-band[1] continuity at sub-THz frequencies.

In parallel, another interesting approach to investigate is via extensive 3D EM simulations of the whole measurement environment, i.e. including an accurate 3D model of the probes, the whole chip and its test structures. This approach is extensively used by Fregonese *et al.* **[214]** with good measurement-simulation agreement for Si-based device at mm-wave and sub-THz frequencies. In this case, the measurement accuracy is not improved, but rather the pertinence of the simulation and measurement comparison. Indeed, the dut model can be more accurately verified by comparing measurements with Spice simulations augmented with these complete 3D EM simulations that includes all aforementioned parasitic effects. Although it represents a significant effort dedicated to simulations, it would also help designing calkits in a *predictive* way to reduce parasitic effects and improve measurement accuracy ultimately.

Finally, due to the probe-dependent residual errors identified in all of the above measurement steps (first-tier calibration, substrate loss extraction, MOSFET characterization) that overall deteriorates measurement accuracy at high frequencies, it is also worth investigating the fabrication of new RF probes. As indicated in **[215]**, the design of RF probes has a strong impact on the associated residual errors, and with a careful probe structure engineering such detrimental effects could be reduced.

[1] Usually measurements in the sub-THz ($> 100\,\text{GHz}$) range are performed with different setups covering different bands: 110-170 GHz, 140-220 GHz, etc. Discontinuity from one band to another is an issue widely encountered **[265]**.

I. FET Channel Mobility Boost Impact at Circuit Level

This appendix provides first a qualitative analysis of potential circuit-level improvements in case of channel mobility boost of nMOSFETs. Two mm-wave circuits are studied: the LNA and PA. Then, a brief quantitative analysis is performed to evaluate the potential improvements of the designed LNA and PA1 presented in **Chapter 5**. The latter study is realized without circuit re-design and at the same voltage biases (as to the case when no mobility boost is present), even though it is not the most pertinent way to assess the circuit performance improvements.

I.1 Demonstrated Mobility Boost in FD-SOI Technology

An interesting method recently published proposes to strain channel of nMOSFETs via strain transfer structure (STS) of a SiGe buried stressor layer under the BOX **[227]**. In this paper, a 10 % improvement in saturated drain current and 15 % increase in transconductance is demonstrated for a 20 nm gate length FD-SOI nMOSFET. The estimated mobility improvement is of the order of $\sim 40-50\,\%$, but the impact on the overall FET performance is reduced due to the extrinsic source and drain resistances. Nevertheless, the observed 15 % improvement in extrinsic g_m is promising, as it implies an equivalent 15 % boost in f_t and overall improvement of FET performance at high frequencies.

I.2 Qualitative Analysis

Let us qualitatively analyze the impact of mobility boost to the cases of mm-wave LNAs and PAs.

I.2.1 LNA

In an LNA, the minimum noise figure and gain are related to the cutoff frequency. The noise figure in particular is linked to f_t according to Fukui formula in **Equation 6.1**:

$$NF_{min} - 1 = K_f \frac{f}{f_t} \sqrt{g_m + (R_g + R_s)} \propto \frac{1}{\sqrt{g_m}}. \tag{9.1}$$

So, an improvement in mobility increases f_t and g_m, which reduces the minimum noise figure.

The relationship between mobility or FET parameters and the equivalent resistance R_n is not straightforward, especially for short channel device. Nevertheless, with an appropriate matching, NF_{min} can be achieved whatever the R_n is.

I.2.2 PA

Concerning a power amplifier, the gain is related to f_{max}, which is related to the FET parameter as **[266]**

$$f_{max} \approx \frac{f_t}{2\pi f_t R_g C_{gd} + (R_s + R_d) g_d}. \tag{9.2}$$

As for the output power and power added efficiency figures of merit, they highly depend on the design strategy, such as the operating class and output impedance. For the simple class A example provided in **Section F.2.2**, the maximum output power (with optimal load impedance) is

$$P_{out,max} = V_{ds,max} I_{d,max} / 8. \tag{9.3}$$

So, an increase in mobility results in an increased output current for the same FET width, thus also improving the maximum output power, as long as an optimal impedance is presented at the output. So, a redesign of the PA is also needed to take full advantage of the mobility boost.

Finally, the power added efficiency can also benefit from a mobility improvement. As seen in **Equation 6.7**, the PAE depends on several factors.

- F_{gain} should not benefit from a significant improvement in mobility (at least in applications below 60 GHz, as usually non-boosted FETs have sufficient gain for proper operation.
- $F_{\text{matching,Q}}$ does not depend on the FET and is therefore not affected.
- F_{waveform} is related to the operating class of the PA. For an ideal class A, this term limits the theoretical PAE to 50 % and does not depend on the maximum current or voltage. So, this parameter is also unaffected.
- However, F_{Vswing} that is linked to the non-zero knee voltage is likely the parameter most impacted by a boost in mobility. A lower value of V_{knee} can be achieved with a sharper $I_d - V_{ds}$ transition in linear regime (low R_{on}), which is provided by an increase in mobility. Indeed, this F_{Vswing} term is linked to the FoM expressed in **Equation 6.9** and is explicitely improved with a larger mobility.

I.3 Quantitative Analysis

As indicated above, a boost in mobility would require circuit re-design to take full advantage of it. Nevertheless, we can evaluate a first-order impact on the presented circuits from **Chapter 5** by looking at NF_{min} and maximum available gain (G_{max}) for the LNA, and peak PAE and P_{sat} for the PA (although the output impedance should be adapted)[1], at the same designed nominal bias.

The FET parameter mobility multiplier, 'p_u0m', available in the PDK can be used to evaluate the impact of mobility boost at circuit level. Its value is however limited to $+1.2$, which only induces a $+8\,\%$ increase in f_t. Even though larger mobility boost could be obtained in **[227]**, let us limit the analysis to this 20 % increase.

Small-signal and noise simulations of the LNA show that a 0.6 dB increase in gain and a negligible 0.02 dB reduction in NF (or NF_{min}) can be achieved.

Large-signal CW simulations of the wideband PA shows an improvement of $0.3-0.4$ dB in P_{sat} and $1.3-1.5\,\%$ in peak PAE. Although these numbers could probably be increased (i) with a careful re-design and even further (ii) with a larger mobility boost, they are encouraging significant improvements.

[1] Since the PA is biased close to threshold voltage in nominal operation, a small change in bias condition (such as provided by a change in mobility) induces a strong variation in gain. So, the impact of mobility boost on the PA gain is not analyzed.



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