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Compositional Engineering of Cu-Doped SnO Film for Complementary Metal Oxide Semiconductor Technology

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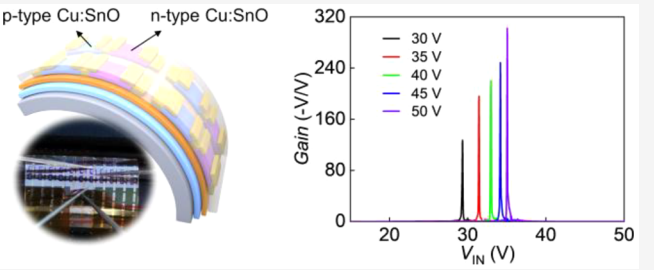
ABSTRACT: Metal oxide semiconductor (MOS)-based complementary thin-film transistor (TFT) circuits have broad application prospects in large-scale flexible electronics. To simplify circuit design and increase integration density, basic complementary circuits require both p- and n-channel transistors based on an individual semiconductor. However, until now, no MOSs that can simultaneously show p- and n-type conduction behavior have been reported. Herein, we demonstrate for the first time that Cu-doped SnO (Cu:SnO) with HfO_2 capping can be employed for high-performance p- and n-channel TFTs. The interstitial Cu^+ can induce an n-doping effect while restraining electron−electron scatterings by removing conduction band minimum degeneracy. As a result, the $Cu_{3\ atom\ \%}$:SnO TFTs exhibit a record high electron mobility of 43.8 $cm^2\ V^{-1}\ s^{-1}$. Meanwhile, the p-channel devices show an ultrahigh hole mobility of 2.4 $cm^2\ V^{-1}\ s^{-1}$. Flexible complementary logics are then established, including an inverter, NAND gates, and NOR gates. Impressively, the inverter exhibits an ultrahigh gain of 302.4 and excellent operational stability and bending reliability.



KEYWORDS: *flexible complementary logics, metal oxide semiconductor, Cu doping, SnO*

Because of their advantages, low power dissipation, wide noise margin (NM), and large-volume manufacturing, complementary metal oxide semiconductor (CMOS) logics have facilitated the growth of the integrated circuit industry.[1−3] However, traditional silicon-based CMOS circuits face fundamental challenges of rigidity and brittleness, which hinders their application in emerging flexible electronics, including wearable devices, artificial skins, flexible displays, etc.[4−6] In contrast, metal oxide semiconductors show the greatest potential for commercial applications in flexible electronics due to their high carrier mobility and low-temperature deposition processes on plastic substrates. For example, amorphous IGZO has been implemented for commercialization in flexible displays;[7] complementary logics based on p-type Cu_2O and n-type counterparts IGZO, ZTO, etc., have been demonstrated.[8,9] Nevertheless, incompatibility between multiple metal oxide semiconductor processes can lead to complex layouts and high costs that are not suitable for commercial applications.

Because of the co-contribution of spherically spread Sn 5p orbitals to the conduction band minimum (CBM) and 5s orbitals to the valence band maximum (VBM), SnO has been proved to be the only ambipolar oxide semiconductor that can be employed as thin-film transistor (TFT) channel conducting both electrons and holes.[10,11] Although the presented ambipolar SnO TFTs show potential in CMOS logics, the carrier mobility of ambipolar devices is lower than that of unipolar devices.[12,13] In addition, unlike those inverters integrating both n- and p-channel TFTs that perform distinctly on/off states, ambipolar SnO-based inverters are hard to switch off completely.[14,15] Accordingly, effective strategies for the development of high-performance unipolar n- and p-channel SnO devices should be pursued. In the case of SnO, the VBM comes from hybridized O 2p and Sn 5s orbitals, and the spherically spread Sn 5s orbital allows for high hole mobility. Meanwhile, the CBM is mainly composed of the Sn 5p orbital and the curve of partial density of states exhibits a free electron-like band, which is beneficial for electron transport.[11,16] Furthermore, due to the direct (optical) bandgap of 2.7 eV and the indirect (fundamental) bandgap of 0.7 eV in SnO, both a small ionization potential and a large electron affinity are achieved, which are requested criteria for p and n doping.[17−19] With this in mind, achieving p- and n-channel SnO TFTs by doping SnO with appropriate impurities and

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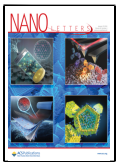

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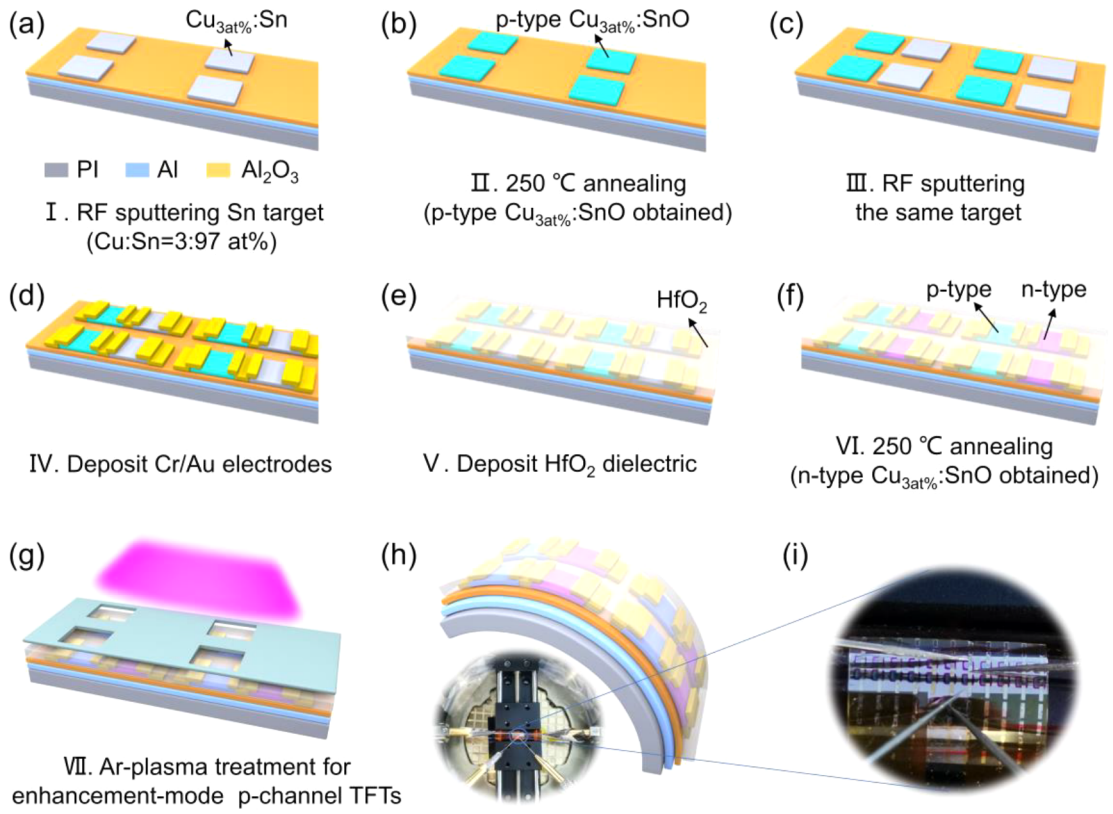

Figure 1. Fabrication of a flexible complementary inverter. (a) RF sputtering Cu:Sn film array. (b) Annealing in the atmosphere to afford a p-type film. (c) RF sputtering Cu:Sn film array adjacent to the p-type Cu:SnO. (d) Deposit Cr/Au electrodes. (e) Deposit HfO_2 capping layer. (f) Annealing in the atmosphere to afford a n-type Cu:SnO film. (g) Ar-plasma treatment for enhancement-mode p-channel TFTs. (h and i) Schematic illustration and photograph of a flexible inverter, respectively.

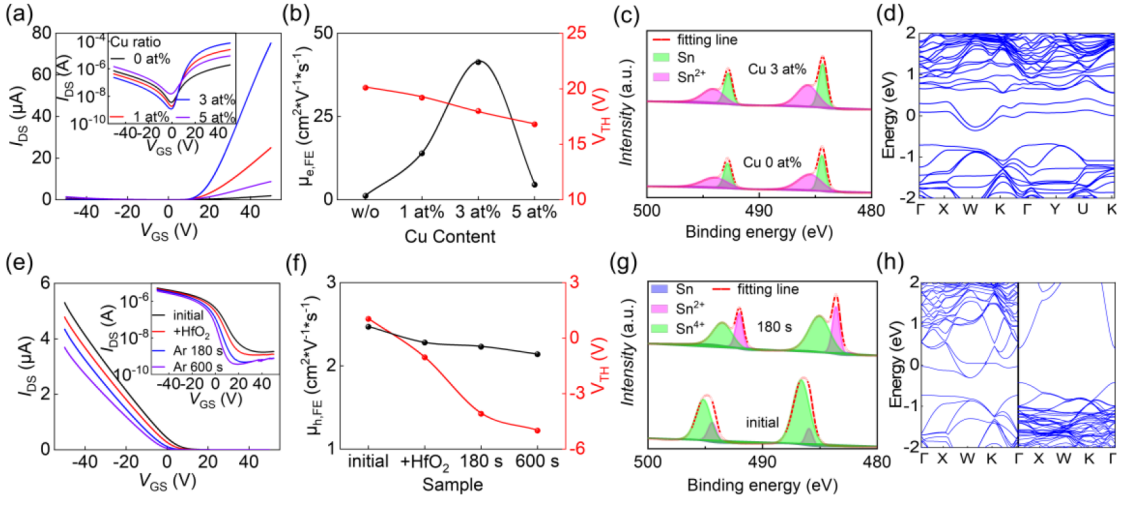

Figure 2. Electrical measurement, XPS characterization, and DFT computations. (a) Transfer curves of n-channel Cu:SnO TFTs with diverse Cu doping concentrations. (b) $\mu_{e,FE}$ and V_{TH} corresponding to panel a. (c) Sn 3d XPS spectrum for ambipolar SnO and n-channel $Cu_{3\ atom\ \%}$:SnO TFTs. (d) Band structure calculated for the Cu:Sn structure. (e) Transfer curves of p-channel Cu:SnO TFTs with different Ar-plasma treatment times. The initial sample refers to a TFT annealed in air without HfO_2. (f) $\mu_{h,FE}$ and V_{TH} corresponding to panel e. (g) Sn 3d XPS spectrum for the initial $Cu_{3\ atom\ \%}$:SnO TFT and plasma-180 s $Cu_{3\ atom\ \%}$:SnO TFT. (h) Band structure calculated for Hf:SnO (left) and Hf:SnO_2 (right) structures.

procedures for adjusting the conduction types are highly promising.

In this work, an efficient doping strategy with Cu is demonstrated for p- and n-channel Cu:SnO TFTs on a flexible polyimide (PI) substrate. The n-channel mode is obtained by annealing a $Cu_{3\ atom\ \%}$:SnO (Cu doping concentration of 3 atom % in Cu-doped SnO) film after HfO_2 capping. Due to the strong reducibility of Hf atoms, the O atoms near Sn vacancies would migrate to the HfO_2 layer, which significantly inhibits p-type conductance in SnO. Furthermore, the interstitial Cu^+ can induce the n-doping effect while improving electron mobility by removing conduction band minimum degeneracy. As a

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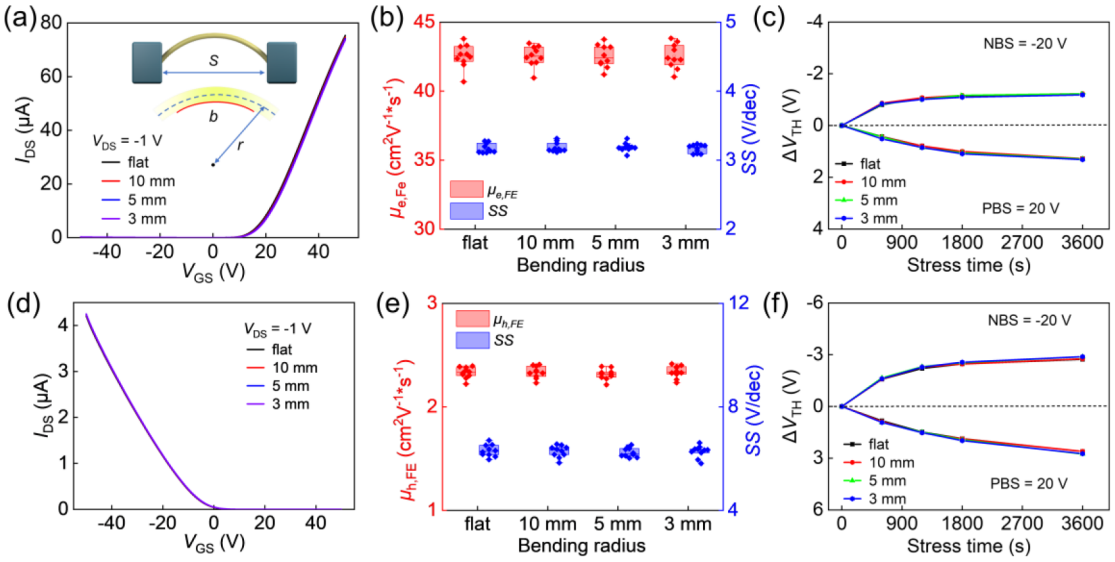

Figure 3. Flexibility and bias stress stability characteristics of n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs. (a) Transfer curves for n-channel $Cu_{3\ atom\ \%}$:SnO devices in the flat state, and bent with radii of 10, 5, and 3 mm. The inset is a schematic illustration of the bending radius. (b) Statistical distribution box plots of $\mu_{e,FE}$ (left vertical axis) and SS (right vertical axis). (c) Variation of ΔV_{TH} with a consecutive gate bias stress of 3600 s, under NBS = −20 V and PBS = 20 V. (d) Transfer curves for Ar-plasma 180 s TFTs in the flat state, and bent with radii of 10, 5, and 3 mm. (e) Statistical distribution box plots of $\mu_{h,FE}$ (left vertical axis) and SS (right vertical axis). (f) Variation of ΔV_{TH} with a consecutive gate bias stress of 3600 s, under NBS = −20 V and PBS = 20 V.

result, the n-channel $Cu_{3\ atom\ \%}$:SnO TFTs exhibit a record high electron mobility ($\mu_{e,FE}$) of 43.8 $cm^2\ V^{-1}\ s^{-1}$ and an on/off current ratio (I_{on}/I_{off}) of 6.8×10^4. The p-channel TFTs can be achieved by simply annealing the same $Cu_{3\ atom\ \%}$:SnO film before HfO_2 capping, which exhibits an ultrahigh hole mobility ($\mu_{h,FE}$) of 2.4 $cm^2\ V^{-1}\ s^{-1}$ and an I_{on}/I_{off} of 1.3×10^4. With additional Ar-plasma treatment after HfO_2 capping, the threshold voltage of the devices could be modulated through the n-type doping effect of injected Hf^{4+} to achieve an enhancement-mode device. On the n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs, flexible complementary logics (inverter, NAND, and NOR gates) are therefore established. The excellent operational stability is demonstrated by the bias stress and bending test. More importantly, the fabrication of p-channel $Cu_{3\ atom\ \%}$:SnO TFTs is compatible with the n-channel devices, which reveals the potential to achieve both p- and n-channel TFTs based on an individual metal oxide semiconductor.

The fabrication of a mechanically flexible complementary inverter configured with a bottom gate structure is depicted in Figure 1. To be specific, a Cu:Sn film array was first deposited on a 200.3 nm Al_2O_3 dielectric layer by radiofrequency (RF) sputtering (Figure 1a), followed by annealing at 250 °C in the atmosphere to afford a p-type Cu:SnO film (Figure 1b). Then, another Cu:Sn film array adjacent to p-type Cu:SnO was deposited via RF sputtering using the same target (Figure 1c). Then, metals Cr and Au (16.2 and 44.7 nm, respectively) were deposited as contact electrodes through vacuum thermal evaporation (Figure 1d). A 9.6 nm atomic layer-deposited (ALD) HfO_2 film (Figure 1e) was employed as the capping layer. The n-type Cu:SnO array is achieved by an annealing process, which ultimately leads to the successful integration of a complementary inverter array using an individual metal oxide semiconductor (Figure 1f). The threshold voltage (V_{TH}) of p-channel Cu:SnO TFTs can be modulated by Ar-plasma treatment (Figure 1g). The flexible schematic illustration and photograph are presented in panels h and i, respectively, of Figure 1. Detailed device preparation and cross-sectional images are presented in Methods and Figure S1, respectively.

Here, we tried different Cu doping concentrations (Figure S2) and annealing temperatures (Figure S3), where $Cu_{3\ atom\ \%}$:SnO TFTs annealed at 250 °C showed optimal n-channel characteristics with transfer curves ($I_{DS}-V_{GS}$) displayed in Figure 2a. In contrast, the initial (unpassivated) $Cu_{3\ atom\ \%}$:SnO TFT exhibits typical p-channel characteristics (Figure 2e). Room-temperature Hall measurements on the carrier type confirm that the $Cu_{3\ atom\ \%}$:SnO films exhibit p- and n-type conductivity through annealing before and after HfO_2 capping (Table S1). To identify the origin of the polarity conversion, material characterizations and density functional theory (DFT) computations were then performed. X-ray photoelectron spectroscopy (XPS) was carried out to assess the surface chemistry of p- and n-type Cu:SnO films. The results indicate that Sn and Sn^{2+} are dominant in the n-type $Cu_{3\ atom\ \%}$:SnO film (Figure 2c), which differs from the p-type $Cu_{3\ atom\ \%}$:SnO film mainly composed of Sn^{2+} and Sn^{4+} (Figure 2g). Grazing-incidence X-ray diffraction (GIXRD) results show that no Sn-related diffraction peak is observed in p-type Cu:SnO films (Figure S4a). In contrast, the Sn-related diffraction peak is found in n-type Cu:SnO films (Figure S4b). Meanwhile, the surface Sn/O atomic ratio of the p-type $Cu_{3\ atom\ \%}$:SnO film is lower than that of the n-type $Cu_{3\ atom\ \%}$:SnO film (Figure S5 and Table S2), indicating the O movement of SnO induced by HfO_2 passivation. Subsequently, DFT computations are conducted to reveal the polarity switching mechanism from p-type conductivity to n-type conductivity. Due to the strong reducibility of Hf atoms, the O atoms near Sn vacancies can move to the HfO_2 layer with a released energy of approximately 3−5 eV (Figure S6), which will suppress the p-type conductivity induced by Sn vacancies.[16]

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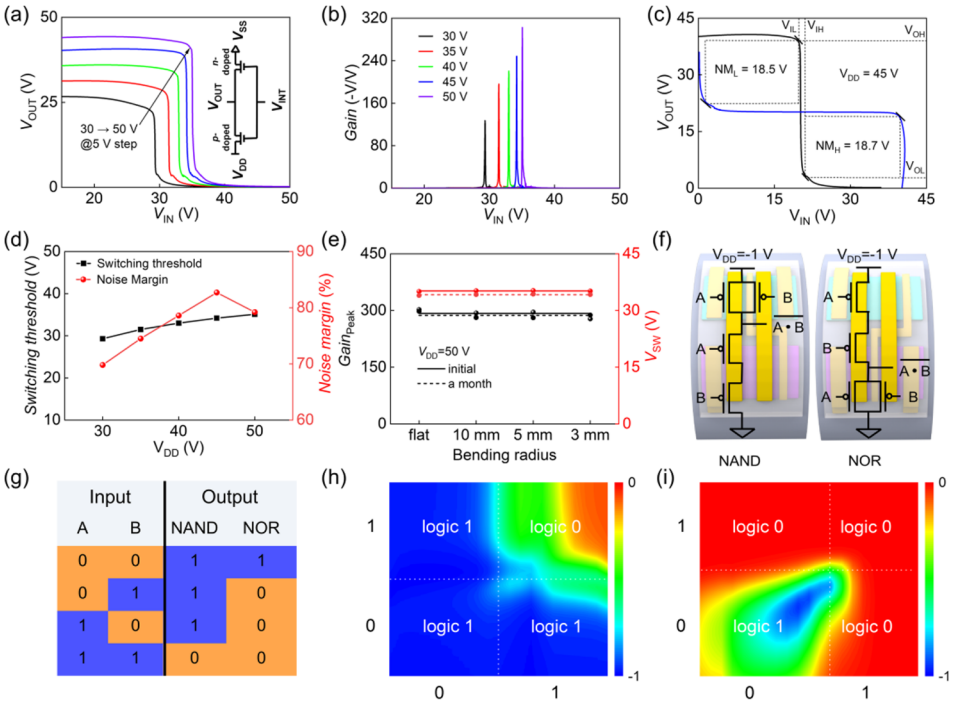

Figure 4. Flexible logic gates configured with n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs. (a) Output characteristics of the inverter at different V_{DD} values. The inset is an equivalent circuit of the inverter. (b) Voltage gains of the inverter. (c) NM of the inverter at a V_{DD} of 45 V. (d) V_{SW} and NM of the inverter corresponding to panel a. (e) At a V_{DD} of 50 V, the peak gain and V_{SW} variation after exposure to atmosphere for a month. (f) Schematic of layouts and equivalent circuit diagrams for two-input NAND and NOR gates. (g) Truth table of NAND and NOR gates with different V_{INA} and V_{INB} values. (h and i) Operation of NAND and NOR gates, respectively.

The transfer characteristics allow quantitative extraction of the field-effect mobility (μ_{FE}) and V_{TH} to evaluate the performance of TFTs. Here, μ_{FE} is given by[18,20]

$$\mu_{FE} = \frac{LG_m}{WV_{DS}C_{ox}} \quad (1)$$

where L (200 μm) and W (130 μm) are the channel length and width, respectively, G_m is the maximum transconductance, calculated by dI_{DS}/dV_{GS}, and C_{ox} is the specific capacitance of per unit area (the value is 38 nF cm^{-2} for the 200.3 nm thick Al_2O_3 dielectric layer). Figure 2b shows the V_{TH} and $\mu_{e,FE}$ of n-channel Cu:SnO TFTs; V_{TH} decreases with an increase in Cu concentration (Figure S7), and $\mu_{e,FE}$ increases to 41.3 cm^2 V^{-1} s^{-1} for the 250 °C-annealed $Cu_{3\ atom\ \%}$:SnO TFT (Figure S3). The output curves (I_{DS}−V_{DS}) of the $Cu_{3\ atom\ \%}$:SnO TFT are shown in Figure S8a, which presents ideal and highly conductive n-type behavior. According to DFT computations, the most stable position of Cu in SnO is the interstitial site (Figure S9) with a formation energy of −2 eV (Figure S10). The calculated defect transition energies of Sn and O vacancies are very similar to those from a previous report, except for the formation energies on the y-axis due to the different assumptions about the environment.[16] Here, Cu^+ is found in the Cu:SnO film (Figure S11). As demonstrated in Figure 2d, the interstitial Cu^+ induces the n-doping effect, in accordance with the experimental results. Moreover, the CBM degeneracy is removed, which can restrain electron−electron scatterings and be beneficial for electron mobility.[21,22] Therefore, both the improved mobility and the negative V_{TH} shift in n-channel Cu:SnO TFTs can be attributed to the Cu interstitial complex in SnO.

For the p-channel $Cu_{3\ atom\ \%}$:SnO TFT, $\mu_{h,FE}$ and V_{TH} are extracted and plotted in Figure 2f. Here, V_{TH} is negatively shifted with Ar-plasma treatment to achieve the enhancement-mode p-channel TFT. The I_{DS}−V_{DS} curves of the plasma-180 s TFT are shown in Figure S8b, confirming typical p-channel behavior. After plasma treatment, Hf has migrated into the $Cu_{3\ atom\ \%}$:SnO film (Figure S12), with a decrease in Sn^{4+} content and an increase in Sn^{2+} content (Figure S13). Here, Hf exhibits a strong reducibility and the most stable configurations are substitutional Sn sites at both SnO and tin oxide (SnO_2), with formation energies of −5.4 and −8.7 eV, respectively. The values are obtained by assuming that a Hf atom kicks out a Sn atom away from the perfect SnO and SnO_2 crystals (Figure S14). As shown in Figure 2h, except for the slight increases in the bandgap, the substitution in SnO_2 does not contribute to the doping effect because of the equivalency between Sn^{4+} and Hf^{4+}, while it induces the n-type doping effect in SnO, which is responsible for the negatively shifted V_{TH} in the p-type transport experiments.

The operational stability of n- and p-channel $Cu_{3\ atom\ \%}$:SnO devices is characterized by the bias stress and bending test with the schematic diagram presented in Figure 3a. The bending radius (r) can be calculated by[23,24]

$$S = 2r\sin\left(\frac{b}{2r}\right) \quad (2)$$

where S is the distance between two movable tables and b refers to the length of the arc. The transfer curves corresponding to n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs are shown in panels a and d, respectively, of Figure 3, which exhibit negligible deviation with diverse bending radii with a limited V_{TH} variation (ΔV_{TH}) of <1 V (Figure S15).

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Additionally, a statistical study of 10 devices is demonstrated under different bending radii (Figure 3b,e). Our fabricated n-channel $Cu_{3\ atom\ \%}$:SnO TFTs have $\mu_{e,FE}$ values centered between 40.7 and 43.8 $cm^2\ V^{-1}\ s^{-1}$, SS values $\left\{\left[\frac{d(I_{DS})}{d\log(V_{GS})}|_{max}\right]^{-1}\right\}$[18,25] centered between 3.0 and 3.3 V $decade^{-1}$, and I_{on}/I_{off} values centered between 5.5×10^4 and 6.8×10^4 (Figure 3b and Figure S16a). To the best of our knowledge, as shown in Table S3, the extracted $\mu_{e,FE}$ value is 1 order of magnitude higher than that of the SnO devices reported previously.[12,14,15] In addition, we presented the V_{TH} evolution under a consecutive gate bias for 3600 s, consisting of a negative bias stress of −20 V (NBS) and a positive bias stress of 20 V (PBS). ΔV_{TH} is restricted within a range of 1.5 V (Figure 3c), with detailed $I_{DS}-V_{GS}$ curves displayed in Figure S17, indicating excellent bias stress stability after HfO_2 encapsulation. Similarly, p-channel $Cu_{3\ atom\ \%}$:SnO TFTs also perform well in terms of uniformity and stability, with average $\mu_{h,FE}$ values centered between 2.2 and 2.4 $cm^2\ V^{-1}\ s^{-1}$, SS values centered between 5.8 and 6.6 V $decade^{-1}$, and I_{on}/I_{off} values centered between 1.1×10^4 and 1.3×10^4 (Figure 3e and Figure S16b). ΔV_{TH} is limited within a range of 3 V (Figure 3f) under a continuous gate bias for 3600 s, with detailed $I_{DS}-V_{GS}$ curves displayed in Figure S18. The small hysteresis of the device further confirms the excellent bias stress stability (Figure S19). In addition, we compare the bias stability of the device without a hydrophobic HfO_2 layer (Figure S20).[26,27] ΔV_{TH} is ∼5 V (Figure S21), which is higher than the value of $Cu_{3\ atom\ \%}$:SnO TFTs with HfO_2 encapsulation. Moreover, all n- and p-channel TFTs exhibit ultralow leakage currents [$I_{GS}-V_{GS}$ (Figures S22 and S23)] during the bias stress and bending test, indicating high reliability in flexible applications.

To verify the feasibility of the proposed doping strategy in complex logic circuits, functionally complementary logics (inverter, NAND, and NOR gates) configured with p- and n-channel $Cu_{3\ atom\ \%}$:SnO TFTs were further assessed. As the basic logic unit, the fabrication process of the inverter is shown in Figure 1 with the equivalent circuit exhibited in Figure 4a. The W and L values of n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs used in the inverter are 130 and 200 μm, respectively. The transfer characteristic curves shown in Figure 4a exhibit clear on/off states under different supply voltages (V_{DD}), unlike the ambipolar inverter that cannot be completely switched off.[12,15] Compared to other metal oxide semiconductor-based inverters (Table S4), the inverter presented here exhibits an ultrahigh voltage gain (dV_{OUT}/dV_{IN}) of 302.4 at a V_{DD} of 50 V (Figure 4b), which indicated excellent signal amplification capacity. Here, the operation voltage of the inverter could be reduced by decreasing the dielectric layer thickness.[28] The NM extracted from the butterflied transfer curves represents the threshold value for a circuit to distinguish the proper signal from "0" or "1". The high NM (NM_H) and low NM (NM_L) can be calculated as follows:[18]

$$NM_H = V_{OH} - V_{IH} \quad (3)$$

$$NM_L = V_{IL} - V_{OL} \quad (4)$$

where V_{OH} and V_{OL} refer to the output voltages at high and low levels, respectively, and V_{IH} and V_{IL} refer to the input voltages at high and low levels, respectively. Figure 4c shows the benchmarking of NM at a V_{DD} of 45 V; the calculated NM_L and NM_H are 18.5 and 18.7 V, respectively. The total NM ($NM = NM_H + NM_L$) reaches 82.7%V_{DD}, indicating the superior noise endurance.[29] Here, as supply voltage V_{DD} increases, the switching threshold voltage (V_{SW}) increases and the NM reaches its maximum at a V_{DD} of 45 V (Figure 4d). Surprisingly, the voltage gains and V_{SW} are almost unchanged at different bending radii and upon long-term exposure to the atmosphere (Figure 4e), indicating excellent mechanical flexibility and ambient stability.

Similarly, NAND and NOR gates were fabricated on the PI substrate by integrating p- and n-channel $Cu_{3\ atom\ \%}$:SnO TFTs. The layout diagrams of the two-input NAND and NOR gates are shown in Figure 4f. By assembling p-channel and n-channel devices, one can prepare more complex NAND and NOR gates. The contact electrodes and gate electrodes were deposited before and after HfO_2 encapsulation, respectively. Input terminals A and B (defined as V_{INA} and V_{INB}, respectively) are set to high voltage at logic "1" and low voltage at logic "0", respectively. Logic NAND displays a low output only when both inputs are high, and in other cases, the output is high. On the contrary, logic NOR displays a high output only when both inputs are low and a low output in other cases. Furthermore, outputs corresponding to all possible logic inputs were measured and verified against the truth tables (Figure 4g). Here, graphical demonstrations of NAND (Figure 4h) and NOR (Figure 4i) correspond to the expected response, with blue and red representing the "on" and "off" states, respectively. All of these results confirm the great potential of SnO TFTs in large-scale flexible electronics.

In summary, by adjustment of the doping concentration and annealing process, high-performance p- and n-channel SnO TFTs were demonstrated for the first time. Via the combination of electrical measurements, XPS characterizations, and DFT calculations, the doping mechanism of Cu and Hf in a HfO_2-encapsulated Cu:SnO film was identified. By optimizing the electrical properties of $Cu_{3\ atom\ \%}$:SnO TFTs, we have successfully implemented logics of a flexible inverter, a NAND, and a NOR. In particular, the inverter shows a high voltage gain of 302.4, a wide NM of ≤82.7%V_{DD}, and excellent bending reliability and ambient stability. The proposed doping strategy of adjusting carrier types, combined with improved electrical properties, demonstrates a viable way of constructing flexible complementary logic circuits based on an individual metal oxide semiconductor.

METHODS

Device Fabrication. All devices were fabricated on a customized PI substrate with metal Al as the bottom electrode and 200.3 nm Al_2O_3 as the gate dielectric layer. First, the PI substrate with a thickness of 18 μm was deposited on a clean glass carrier by spin-coating, which was not detached until the device was completed. An aluminum gate electrode was directly deposited on the PI substrate by sputtering and patterned by wet etching. The Al_2O_3 that followed was anodized on the surface of the Al film and acted as a gate dielectric layer. The Cu:Sn target (99.99% purity, HZAM) was RF-sputtered using a model JSD300 magnetron sputtering system auxiliary. Sputtering was performed with Ar/O_2 acting as the sputtering gas at a power of 38 W and room temperature under a pressure of 0.76 Pa. During the deposition, the oxygen partial pressure was 2.31% [$P_O = O_2/(O_2 + Ar)$%]. The sputtering deposition process was the same for both n-type and p-type Cu:SnO films. The Cr/Au electrodes (contact electrodes and connecting electrodes) were deposited by a vacuum

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thermal evaporation system. Annealing was carried out in an atmospheric environment using OTF-1200X. The HfO_2 dielectric layer was grown at 100 °C using an ALD system (TALD-150R), with dimethylamine hafnium and H_2O as precursors. Plasma processing was implemented in an Ar environment using a model CPC-B Plasma Cleaner.

Material Characterization and Device Measurement. All electrical characteristics of the TFTs, inverter, NAND, and NOR were measured with an Agilent 4155C semiconductor parameter analyzer by the Lake Shore TTPX in ambient atmosphere at room temperature. Film XPS was implemented using an EscaLab 250Xi instrument. The film GIXRD (0.5°) patterns were recorded using X'Pert PRO MPD. Hall measurements were taken using the van der Pauw method at 300 K (M91 system of Lake Shore). The cross-section image was taken with a field-emission transmission electron microscope (TEM) [Themis Z (3.2), Thermo Scientific].

Simulation Method. DFT calculation was carried out with open-source plane-wave package QUANTUM ESPRESSO.[30,31] The ultrasoft pseudopotentials obtained from pslibrary version 1.0.0 were used, in which the exchange-correlation functional type was the Perdew−Burke−Ernzerhof type and the kinetic energy cutoff is 47 Ry.[32] In defect studies, SnO_2 and SnO unit cells were enlarged to 2 × 2 × 2 and 3 × 3 × 2 supercells, respectively. The variable-cell Broyden−Fletcher−Goldfarb−Shanno quasi-Newton algorithm was adopted to optimize the structures of the systems before and after the induction of defects, until the forces on each atom and total energy variations were smaller than 1×10^{-3} Ry $Å^{-1}$ and 1×10^{-4} eV, respectively. The Fermi−Dirac distribution at room temperature was assumed, and the Brillouin zone *k*-point samplings at electronic ground-state computations were all 2 × 2 × 2.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.3c03953.

Cross-sectional TEM image of a Cu:SnO TFT; wide survey XPS spectra of Cu:SnO films with different Cu ratios; $I_{DS}-V_{GS}$ curves of n-type $Cu_{3\ atom\ \%}$:SnO TFTs as a function of annealing temperature; GIXRD spectra of Cu:SnO films; schematic diagram of the O atom moving from the Sn vacancy; $I_{DS}-V_{GS}$ curves of n-type Cu:SnO TFTs with different Cu concentrations; $I_{DS}-V_{DS}$ curves of n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs; model structure of SnO with Cu^+ acting as the interstitial; formation energy versus the Fermi level for interstitials and vacancies; Cu 2p XPS scan spectrum for pure SnO and n-type $Cu_{3\ atom\ \%}$:SnO; XPS profiling of the p-type $Cu_{3\ atom\ \%}$:SnO TFT; relative content of Sn, Sn^{2+}, and Sn^{4+} in the p-type $Cu_{3\ atom\ \%}$:SnO film; model structure of Hf-doped SnO/SnO_2; variation of ΔV_{TH} with bending radius ranging from flat to 3 mm; statistical values of I_{on}/I_{off} at different bending radii; bias stress stability measurement of n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs; $I_{GS}-V_{GS}$ curves of n- and p-channel $Cu_{3\ atom\ \%}$:SnO TFTs; hysteresis of the $Cu_{3\ atom\ \%}$:SnO TFT; Hall measurement of p- and n-type $Cu_{3\ atom\ \%}$:SnO films; atomic percentages of O and Sn elements of the SnO films obtained from XPS analysis; summary of the device performance for reported SnO TFTs; and summary of the device performance for the reported complementary inverter (PDF)

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Author Contributions

X.Z. and L.L. conceived and designed the experiments. Y.L. implemented DFT computations. R.H. fabricated and characterized the devices. P.H., S.Z., X.H., and Q.T. assisted with device fabrication experiments. C.L., T.B., and W.S. helped with the device measurements. X.L., G.L., and D.F. presented the suggestions for improving the quality of this work and revised the manuscript. All authors examined and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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