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Exploiting Forward Back-Biasing Capabilities of FDSOI CMOS Technology for Unified ULP Clock Generation and PVT Compensation

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Thesis submitted in partial fulfillment of the requirements for the degree of
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Contents

Acknowledgments	i
Abstract	v
Acronyms	vii
Publications	ix
Introduction	1
The Context of the Internet-of-Things	1
Ultralow-Power and Ultralow-Voltage IC Design	2
The Benefits of FDSOI CMOS Technology	4
Which Oscillators for Ultralow-Power IC Design?	6
Research Questions and Thesis Outline	10
1 Comparison of Voltage-Controlled Ring Oscillators	15
1.1 Introduction	16
1.2 Jitter and Phase Noise	16
1.2.1 Jitter Definitions	18
1.2.2 Phase Noise Definition	20
1.2.3 Link Between Jitter and Phase Noise	21
1.2.4 Figures of Merit	22
1.3 Considered Ring Oscillator Architectures	23
1.3.1 VCRO Topologies	23
1.3.2 Important Hypotheses About Simulation and Sizing	25
1.3.3 Remarks Concerning the Phase Noise FoM	26
1.4 Uncontrolled Ring Oscillator Analysis	27
1.4.1 Gate Length Scaling, the Best Way to Slow Down an RO	28
1.4.2 Impacts of the Device Multiplier	30
1.4.3 Proposed Ring Oscillator Optimization Process	31
1.5 Current-Starving Versus Back-Bias Control	35
1.5.1 VCROs Transfer Functions: Gain, Range, and Linearity	35
1.5.2 Impacts of PVT Variations on the VCROs Frequency Range	37
1.5.3 Comparison of CSROs and BBCOs at 2.45 GHz	41
1.5.4 Extension of the Comparison to Other Target Frequencies	43
1.5.5 PVT Robustness at Higher Temperatures	46
1.6 Conclusion	48

2	Leveraging Forward Back Biasing in Phase-Locked Loops	51
2.1	Introduction	52
2.2	Design Considerations Linked to PLLs	52
2.2.1	Conventional PLL Modeling	53
2.2.2	BBCO-Based PLLs: Design Implications	55
2.3	Clock Recovery for a UWB Transceiver	58
2.4	Proposed Clock Recovery Unit	61
2.4.1	Dual-PLL Architecture	61
2.4.2	Block Design: BBCO and BBP Driver	63
2.4.3	Clock Recovery Simulation Results	65
2.5	Prototyping and Measurement Results	70
2.6	Analysis of the BBCO Results	74
2.7	Conclusion	75
3	The Unified Frequency and Back-Bias Regulation Concept	79
3.1	Introduction	80
3.2	Adaptive Techniques for ULV Operation	81
3.3	First Generation of UFBRR Prototype	84
3.3.1	Proposed Dual-Loop UFBRR Architecture	84
3.3.2	Proposed Process Imbalance Sensors	88
3.3.3	Prototyping and Measurement Results	89
3.4	Second Generation of UFBRR Prototype	92
3.4.1	Unified Dual-Output UFBRR Architecture	93
3.4.2	UFBRR Design	98
3.4.3	Full-Loop UFBRR Modeling	108
3.4.4	Prototyping and Measurement Results	112
3.5	Comparison to the State of the Art	120
3.6	Conclusion	123
	Conclusions and Perspectives	125
	Contributions	125
	Recommendations	130
	Perspectives	131
A	Mathematical Developments Related to Ring Oscillators	137
A.1	Frequency and Power of an Inverter-Based RO	137
A.2	Phase Noise and FoM of an Inverter-Based RO	139
A.3	Frequency Gain and Linearity of VCROs	141
B	Clock Recovery Modeling	145
B.1	Phase Detectors Characteristics	145
B.2	LPF, BBP Driver, and BBCO Combination	146
B.3	Closed-Loop Modeling	151
	Bibliography	155

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*If you want to go fast, go alone.
If you want to go far, go together.*

African saying

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Abstract

Compared to the mainstream bulk CMOS counterpart, fully-depleted silicon-on-insulator (FDSOI) technology brings unique possibilities and degrees of freedom in the design of integrated circuits, in particular thanks to its forward back-biasing (FBB) feature. FBB reduces the transistors threshold voltage by increasing BBN (resp. decreasing BBP), the NMOS (resp. PMOS) back-bias voltage. In this dissertation, we exploit this feature for ultralow-voltage/ultralow-power (ULV/ULP) circuit operation and improved energy efficiency while compensating for the detrimental effects of process, voltage, and temperature (PVT) variations that are exacerbated at ULV/ULP operation. The additional silicon area required for the FBB circuitry must stay limited to enable highly integrable design solutions. These goals match the requirements of the Internet-of-Things (IoT) while being applicable also in other ULV/ULP applicative contexts. We pursue them in the domains of clock generation and frequency synthesis.

The FBB feature of FDSOI technology gives rise to a new voltage-controlled ring oscillator (RO) topology: the back-bias-controlled oscillator (BBCO). In the first part of this thesis, we compare this new RO architecture to the conventional current-starved ring oscillator (CSRO) in terms of minimum achievable power and the best power/phase noise trade-off they can reach. We also take practical design constraints such as PVT robustness, frequency tuning range, and frequency gains into account. In 28-nm FDSOI technology, the results demonstrate several advantages for the BBCOs compared to CSROs, such as lower minimum power consumption and slightly better power/phase noise compromises. However, the use of FBB also raises design challenges at the block and system levels. For instance, as BBP is negative and takes values from 0 to -3 V, its on-chip generation is challenging, and may have unknown side effects. Moreover, conventional FDSOI layouts share a deep N-well between NMOS and PMOS transistors, resulting in a parasitic BBN/BBP coupling capacitance which constitutes a threat to the stability of BBCO-based feedback loops, such as frequency- or phase-locked loops.

We tackle these two challenges in the second part of this thesis and exemplify the practical use of BBCOs by proposing three prototypes implemented on silicon in 28-nm FDSOI.

The first implementation consists of a clock recovery (CR) unit embedded within a 2.5-Gb/s ultra-wideband (UWB) radio for wireless low-power chip-to-chip communications over short distances. The CR circuit comprises two complementary phase-locked loops (PLLs) for fast frequency acquisition and high-bandwidth phase tracking. The PLLs share a single BBCO whose frequency depends on both BBN

and BBP voltages. A BBP driver generates BBP from BBN using process imbalance sensors (PISs) and a back-gate driven amplifier. The proposed independent BBN/BBP generation extends the natural PVT compensation capability of PLLs to the correction of N/PMOS process imbalance resulting from asymmetric skewed process corners. To avoid the parasitic BBN/BBP coupling challenge, we use a custom layout at the transistor level for both the BBCO and PISs. The proposed 2.5-GHz CR unit showcases competitive experimental results in terms of power (1.034 mW), performance (6.5 ps of RMS long-term jitter), and area ($< 0.043 \text{ mm}^2$). It achieves an energy value of 0.414 pJ/cycle and an excellent power/jitter trade-off. Besides, it helps the entire UWB transceiver achieve a measured energy value of 2.36 pJ/bit. These results demonstrate the relevance of FBB in the context of low-power PLLs.

The last two prototypes concern the implementation of a new adaptive technique: the unified frequency and back-bias regulation (UFBBR). As its name suggests, the UFBBR concept unifies clock generation with adaptive FBB for the PVT compensation of ULV/ULP logic circuits. We propose two UFBBR versions embedded in custom ULV/ULP microcontroller units (MCUs) for biomedical and IoT sensor applications. The UFBBR units correct both the logic speed and the N/PMOS process imbalance according to the desired target clock frequency and the experienced operating conditions. A BBCO simultaneously serves as a clock generator and logic speed sensor. The N/PMOS PISs are digital and comprise N/PMOS-sensitive delay lines or ROs. The sensors and the control part employ standard cells to ensure a good correlation and a deep integration with the digital logic to regulate. The FBB actuators use charge pumps to tune BBN and BBP. The first UFBBR version drives BBN with a frequency-locked loop (FLL) and BBP with a delay-locked loop (DLL), requiring an external decoupling capacitor on BBN to alleviate the parasitic BBN/BBP coupling challenge. The second UFBBR prototype tolerates the BBN/BBP coupling by relying on a unified dual-output FLL that is stable without requiring any external component. Both UFBBR implementations showcase a fast settling time ($< 10 \text{ }\mu\text{s}$) for limited power ($< 22 \text{ }\mu\text{W}$) and area overheads ($< 0.06 \text{ mm}^2$). They provide PVT compensation for the entire MCU digital logic and custom FBB-compatible ULP SRAMs (representing together a total biased area of $< 0.4 \text{ mm}^2$), including against asymmetric skewed process corners. Besides, they generate the MCU system clock up to 80 MHz and provide robustness to voltage droops. We demonstrate record energy values of 3-5.5 $\mu\text{W}/\text{MHz}$ in active mode at the MCU level. All these features illustrate the relevance of the UFBBR concept for ULV/ULP applications.

In light of these different contributions, the FBB feature of FDSOI proves to be an efficient and flexible tuning knob for the design of integrated circuits. It enables ULV/ULP circuits operation while extending their functionality to a broader range of PVT conditions, with limited power and area overheads.

Acronyms

ABB	Adaptive back biasing
AVS	Adaptive voltage scaling
BB	Back-gate bias, back-bias
BBCO	Back-bias-controlled oscillator
BBN	NMOS back-bias voltage
BBP	PMOS back-bias voltage
CP	Charge pump
CR	Clock recovery
CSRO	Current-starved ring oscillator
DCO	Digitally-controlled oscillator
DL	Delay line
DLL	Delay-locked loop
FBB	Forward back biasing
FDSOI	Fully-depleted silicon-on-insulator
FLL	Frequency-locked loop
FoM	Figure of merit
FSM	Finite-state machine
IoT	Internet-of-Things
LPF	Low-pass filter
LVT	Low V_{th}
MCU	Microcontroller unit
ML-BBPD	Multi-level bang-bang phase detector
PD	Phase detector
PFD	Phase-frequency detector
PIS	Process imbalance sensor
PLL	Phase-locked loop
PPM	Pulse-position modulation
PVT	Process, voltage, and temperature
PWM	Pulse-width modulation
RO	Ring oscillator
RVT	Regular V_{th}
RX	Receiver
SCCP	Switched-capacitor charge pump
SoC	System-on-chip
TRO	Tunable ring oscillator
TX	Transmitter
UFBBR	Unified frequency and back-bias regulation
UFVR	Unified frequency and voltage regulation
ULP	Ultralow power
ULV	Ultralow voltage
UWB	Ultra-wideband
VCRO	Voltage-controlled ring oscillator
ZBB	Zero back biasing

Publications

Related Journal Papers

- [JP1] M. Schramme, L. Van Brandt, D. Flandre, D. Bol, “Comprehensive Analytical Comparison of Voltage-Controlled Ring Oscillators in FDSOI Technology: Current Starving Versus Back-Bias Control,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022, *accepted*.
- [JP2] M. Schramme, C. Gimeno, A. Cathelin, D. Flandre, D. Bol, “A 2.5-GHz Clock Recovery Circuit Based on a Back-Bias-Controlled Oscillator in 28-nm FDSOI,” *IEEE Solid-State Circuits Letters*, vol. 3, pp. 478–481, 2020.
- [JP3] D. Bol, M. Schramme, L. Moreau, P. Xu, R. Dekimpe, R. Saeidi, T. Haine, C. Frenkel, D. Flandre, “SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6-3.6- μ W/DMIPS 40-80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode,” in *IEEE Journal of Solid-State Circuits*, 2021.
- [JP4] M. Schramme, D. Bol, “UFBBR: A Unified Frequency and Back-Bias Regulation Unit for Ultralow-Power Microcontrollers in 28-nm FDSOI,” in *IEEE Journal of Solid-State Circuits*, 2021, *submitted*.

Related Conference Papers

- [CP1] D. Bol, M. Schramme, L. Moreau, T. Haine, P. Xu, C. Frenkel, R. Dekimpe, F. Stas, D. Flandre, “A 40-to-80MHz Sub-4 μ W/MHz ULV Cortex-M0 MCU SoC in 28nm FDSOI with Dual-Loop Adaptive Back-Bias Generator for 20 μ s Wake-Up from Deep Fully Retentive Dleep Mode”, in *IEEE International Solid-State Circuits Conference*, pp. 322–324, 2019.
- [CP2] R. Dekimpe, M. Schramme, M. Lefebvre, A. Kneip, R. Saeidi, M. Xhonneux, L. Moreau, M. Gonzalez, T. Pirson, D. Bol, “SleepRider: A 5.5 μ W/MHz Cortex-M4 MCU in 28nm FD-SOI with ULP SRAM, Biomedical AFE and Fully-Integrated Power, Clock and Back-Bias Management,” in *IEEE Symposium on VLSI Circuits*, pp. 1–2, 2021.

Unrelated Journal Papers

- [UJP1] R. Dekimpe, P. Xu, M. Schramme, P. Gérard, D. Flandre, D. Bol, “A Battery-Less BLE Smart Sensor for Room Occupancy Tracking Supplied by 2.45-GHz Wireless Power Transfer,” *Integration*, vol. 67, pp. 8–18, 2019.
- [UJP2] C. Gimeno, D. Flandre, M. Schramme, C. Frenkel, D. Bol, “A 2.24-pJ/bit 2.5-Gb/s UWB Receiver in 28-nm FDSOI CMOS for Low-Energy Chip-to-Chip Communications,” *AEU-International Journal of Electronics and Communications*, vol. 114, p. 152996, 2020.

Unrelated Conference Papers

- [UCP1] R. Dekimpe, P. Xu, M. Schramme, D. Flandre, D. Bol, “A Battery-Less BLE IoT Motion Detector Supplied by 2.45-GHz Wireless Power Transfer,” in *28th International Symposium on Power and Timing Modeling, Optimization and Simulation*, pp. 68–75, 2018.

Introduction

The Context of the Internet-of-Things

Since their appearance in the 1960s, electronic integrated circuits (ICs) have radically changed our world by rapidly spreading to all sectors of today's society. Nowadays, IC devices are all around us, with growing impacts on our daily life. Indeed, we find transistors in our pockets and homes, phones and laptops, cars and trains, boats and planes, companies and industries, schools and hospitals, rockets and satellites, in peace and wars. In other words, the semiconductor industry has modified the way we communicate and cooperate, the way we compute, search, design, and work, the way we travel on Earth or in space, the way we play and entertain ourselves, the way we cure and heal, the way we do business and trade.

This drastic transformation of our world has been extremely quick. In just a few decades, the worldwide semiconductor market skyrocketed from \$26 billion in 1986 to more than \$440 billion in 2020 [1]. At the same time, the number of devices integrated on the same chip grew exponentially, doubling every two years according to Moore's law [2]. This density increase led to an astounding reduction of the average cost of a transistor, from around \$1 in 1970 to less than \$0.00000001 (10 nano dollars) in 2004 [2]. Packing more devices per chip also resulted in added functionality and led to a diversification of the IC applications. These are the benefits of the *technology scaling* trend, which denotes the shrinking of the transistors sizes over the years and is experienced by the mainstream complementary metal-oxide-silicon (CMOS) technology. Smaller transistors are not only cheaper, they are also faster and more energy efficient [3].

More recently, the advent of the *Internet-of-Things* (IoT) marked the beginning of a new wave of technological innovation and target applications [4]. Indeed, the IoT aims at connecting ubiquitous objects to the cloud, which become able to interact with each other and cooperate towards common goals without human intervention [5]. This new paradigm is also sometimes referred to as *machine-to-machine* communications [4, 6]. It promises to broaden the range of current applications thanks to the deployment of billions of *wireless sensor nodes* in our environment [4, 7]. As conceptually represented in Fig. 1, these *things* or *smart objects* can sense data from their environment, process them locally to extract meaningful information, and communicate the results wirelessly to the cloud. Needless to say that none of these actions would be possible without a proper clock and power management.

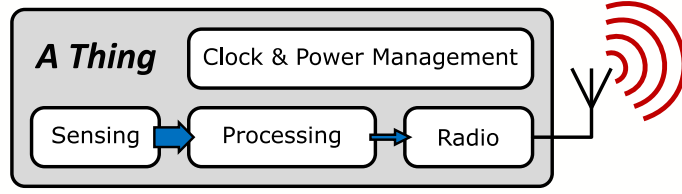


Fig. 1 Conceptual representation of a wireless sensor node.

The number of possible IoT applications is almost unlimited [4, 5, 7]: smartwatches and wearable monitoring devices for e-health; connected cars for intelligent transportation of people; smart homes with connected televisions, fridges, appliances, and lights; smart parking, smart road lighting, and smart cities; intelligent tracking and transportation of goods; anomaly detection in supply chains for smart manufacturing of goods; intelligent transport of energy through smart grids; detection of forest wildfires, deforestation, floods, or poaching; air quality and pollution control for smart environmental monitoring; yield optimization in agriculture through smart farming; monitoring of the biodiversity in remote places; smart supervision of underground infrastructures such as sewers, mines, or subway networks; and this list could extend on several additional pages.

Ultralow-Power and Ultralow-Voltage IC Design

The IoT does certainly bring new opportunities; yet, it also highlights several important challenges. Namely, the deployment and operational costs as well as the ecological footprint of the entire IoT ecosystem are of critical importance given the tremendous number of smart devices considered [8]. Ultimately, these challenges sharply constrain the design of the devices.

In a global approach, powering each smart sensor with wires is totally nonpractical. Moreover, the use of batteries raises concerns related to their ecotoxicity and their periodic replacement. Therefore, one option for the IoT nodes is to rely on *energy harvesters* collecting energy from ambient RF, solar, or thermal sources, for instance. A first goal could be to maximize the efficiency of such scavenging parts to make more energy available to the rest of the system [UJP1]. Unfortunately, ambient energy is often accessible in limited quantities and greatly constrains the available power budget. A second goal thus concerns the minimization of the power consumption of IoT objects. In other words, wireless sensor nodes should operate at ultralow power (ULP) without deteriorating their performance.

An efficient technique to operate at ULP is to supply ICs at ultralow voltage (ULV) [9, 10]. Indeed, the *voltage scaling* technique favorably impacts both the dynamic and static power consumptions of digital circuits.

When neglecting the short-circuit contribution, the *dynamic power* P_{dyn} corresponds

to the power consumed when switching the N_{nodes} circuit nodes between ground voltage level and the supply voltage V_{DD} at a clock rate f_{clk} . It can thus be approximated as follows [9]:

$$P_{dyn} = \frac{1}{2} N_{nodes} \alpha_F C_L V_{DD}^2 f_{clk}, \quad (1)$$

where C_L is the average load capacitance per node and α_F denotes the average activity factor. As shown in (1), reducing the supply voltage V_{DD} reduces the dynamic power *quadratically*.

Furthermore, *static power* comes from the transistor leakage and equals:

$$P_{stat} = I_{leak} V_{DD}, \quad (2)$$

where I_{leak} is the total leakage current of the circuit. This equation shows a linear static power decrease with the supply voltage V_{DD} . As I_{leak} also depends on V_{DD} in practice¹, the relation between static power and supply voltage is in fact *superlinear* rather than linear.

Unfortunately, scaling down the voltage does also introduce detrimental effects. Indeed, at ULV, the transistors current is reduced, which ultimately leads to circuit speed and performance degradations. Besides, the transistors operate in their near/subthreshold regime, where their current has an exponential dependence on voltages. The result is a higher sensitivity to *process, voltage, and temperature* (PVT) variations [11]. Obtaining the expected power savings brought by voltage scaling while ensuring a good circuit performance and a functional and robust operation is hence challenging.

As previously mentioned, CMOS technology scaling can also enable power savings [3]. However, two serious drawbacks affect the use of advanced technology nodes. The first limitation comes from increased leakage: on one hand, the gate oxide thickness shrinking increases the transistors gate leakage by tunneling; on the other hand, the reduction of the transistor gate length and threshold voltage $V_{th,0}$ increases the subthreshold leakage current. The second limitation concerns the increased variability experienced by short transistors. Indeed, as their sizes come closer to the size of atoms, random dopant fluctuations create significant variations in terms of the threshold voltage.

Combining technology and voltage scaling is even worse, as it exacerbates the circuit sensitivity against variability [12]. The conventional way of covering devices variability by using fixed margins on the supply voltage, for instance, is no longer practical [13]. Indeed, the needed guard bands become so large that the overhead they imply in terms of performance or power consumption annihilates the gains brought by technology and voltage scaling.

¹For the subthreshold leakage current, this dependence can come from the drain-induced barrier lowering (DIBL) effect, for instance.

The Benefits of FDSOI CMOS Technology

In this context of IoT and ULV/ULP IC design, the use of *fully-depleted silicon-on-insulator* (FDSOI) CMOS technology might considerably help to address the associated challenges [14, 15]. Indeed, compared to their conventional bulk CMOS counterparts, FDSOI devices benefit from several advantages. The physical differences in their transistor structure explain these benefits, as illustrated in Fig. 2.

Unlike in conventional bulk CMOS technology [Fig. 2(a)], FDSOI transistors have a thin buried-oxide (BOX) layer isolating the ultra-thin undoped channel from the wells underneath [Figs. 2(b)-(c)]². Many positive impacts in terms of electrostatic characteristics result from these technological features [14–16]: reduced leakage, reduced variability, smaller parasitic diodes, lower capacitances, improved mobility, and complete control of the channel. Compared to its bulk CMOS counterpart, the manufacturing costs in 28-nm FDSOI technology are 10% cheaper, thanks to fewer process steps and fewer lithography masks needed [16].

Besides, the BOX layer has another important implication [16]: the transistors become equivalent to dual-gate devices. The main gate is the regular *front gate*, like in bulk technology. The second gate is the FDSOI-enabled *back-side gate* or *back gate*, which is a unique feature in FDSOI technology as it gives an extra degree of freedom for the design.

Indeed, changing V_B (referred to as the body voltage in bulk and back-gate voltage in FDSOI, respectively) modifies the threshold voltage V_{th} of the transistors as follows:

$$V_{th} = V_{th,0} - \gamma_b V_B, \quad (3)$$

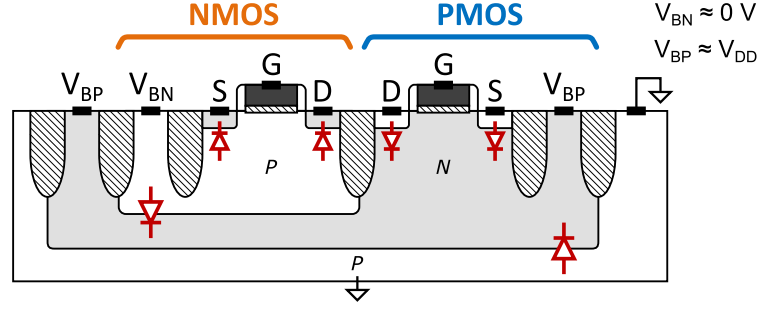
where $V_{th,0}$ is the nominal zero-bias threshold voltage and γ_b the linearized body-effect coefficient.

In bulk technologies, the parasitic source-to-body/drain-to-body diodes constrain the body voltage V_B , as shown in Fig. 2(a), which typically spans from 0 to around 0.3 V (in absolute value) [16]. In addition, as the body factor γ_b is small with a value around 25 mV/V in 28-nm bulk CMOS, this results in a limited threshold voltage variation of about 10 mV. With such an advanced technology node, the so-called *body-biasing* technique is thus not very effective³ in bulk and therefore not often used.

However, for FDSOI technologies, the *back-gate biasing* or *back-biasing* (BB) technique is much more effective [16]. Indeed, the back-gate voltage V_B can vary on

²For this reason, the FDSOI technology is also referred to as an *ultra-thin body and buried oxide* (UTBB) FDSOI technology [16].

³Note that both the body voltage range and the body factor highly depend on the technology node, the transistor flavor, and the gate length. As an example, the 45-nm bulk technology exhibits a larger range for its body voltage (from -0.6 to 0.4 V) and higher body factor values (85 mV/V with general-purpose transistors, 120 mV/V for low-power ones) [17], leading to a larger threshold voltage modulation range compared to 28-nm bulk CMOS.



(a) Transistors in conventional bulk CMOS technology.

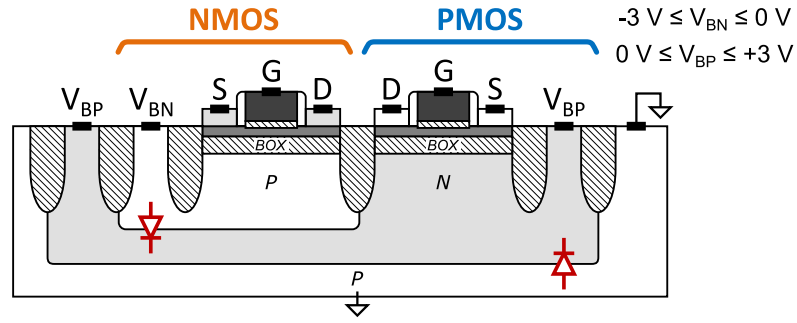
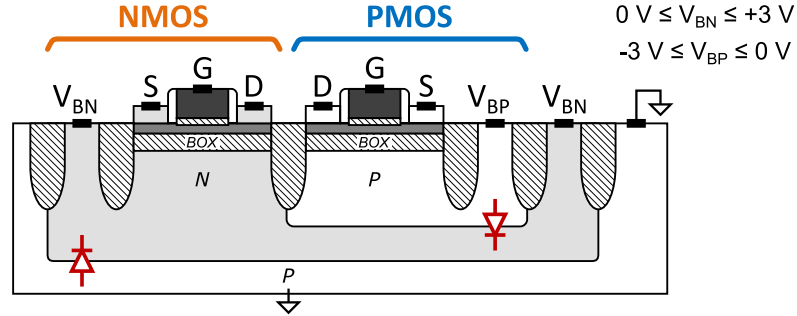
(b) Regular- V_{th} (RVT) transistors in 28-nm FDSOI technology.(c) Low- V_{th} (LVT) flipped-well transistors in 28-nm FDSOI technology.

Fig. 2 Comparison of the cross-sections of transistors in conventional bulk and FDSOI technologies. The voltage range of the transistors body-bias/back-bias nodes (V_{BN} and V_{BP}) is constrained by the parasitic diodes.

a significantly broader range, spanning from 0 to 3 V (in absolute value) in 28-nm FDSOI, and constrained this time by the parasitic N-well/P-substrate or N-well/P-well Zener-type diodes, as shown in Figs. 2(b)-(c). Moreover, the body factor γ_b is larger and takes values around 70-85 mV/V in 22/28-nm FDSOI [14, 16, 18]. The larger back-gate voltage range and body factor value thus ultimately lead to an unprecedented threshold voltage modulation range of about 250 mV for such an

advanced technology node.

Generally, semiconductor foundries propose different device flavors for a given technology, each type featuring a different nominal threshold voltage. For instance, in mature bulk CMOS technology nodes such as 45 or 65 nm, the general-purpose (GP) and low-power (LP) device flavors are usually well-known [12]. In 28-nm FDSOI CMOS technology, as shown in Figs. 2(b) and 2(c), respectively, *regular- V_{th}* (RVT) and *low- V_{th}* (LVT) devices are available [16]. The LVT transistors have a lower threshold voltage thanks to their flipped-well structure (PMOS on a P-well, NMOS on an N-well). The two different transistor flavors in 28-nm FDSOI lead to distinct BB mechanisms. Indeed, the threshold voltage tuning of RVT and LVT transistors is done through *reverse back biasing* (RBB) and *forward back biasing* (FBB), respectively, as represented in Fig. 3. The differences in the voltage range of these two BB mechanisms come from the location of the parasitic N-well/P-substrate and N-well/P-well Zener-type diodes.

Compared to a nominal situation ($V_B = 0$) and considering absolute values, the threshold voltage V_{th} increases with the BB voltage V_B when applying an RBB scheme, as depicted in Fig. 3(a). As a consequence, the transistors current decreases. The RBB technique thus lowers circuit leakage at the cost of circuit speed. For the FBB scheme illustrated in Fig. 3(b), the threshold voltage V_{th} decreases when the BB voltage V_B increases. The corresponding transistors current thus grows. Therefore, the FBB technique increases the circuit speed at the cost of additional leakage.

Besides reducing the power consumption or increasing the circuit speed in a static way with fixed BB voltages, these two BB techniques can also work dynamically and compensate for PVT variations, e.g., by continuously tuning the threshold voltage of the transistors to the circuits operating conditions. The resulting devices thus become adaptive thanks to *adaptive back biasing* (ABB) [19–21].

Which Oscillators for Ultralow-Power IC Design?

Most circuits require a certain cadence or rhythm to perform their function. Our monitors typically refresh their screen 60 times per second (i.e., at a frame rate of 60 Hz). The central processor units (CPUs) in our laptops and smartphones execute billions of instructions per second (i.e., they operate at clock rates comprised between 1 and 4 GHz). We wirelessly connect our devices to the internet through WiFi and can download hundreds of millions of bits of websites, videos, or music, per second (i.e., at data rates up to 900 Mbps). Our global positioning system (GPS), our connections through Bluetooth or universal serial bus (USB), our phone calls through our cellular networks, our low-power wide-area networks (LPWAN) such as SigFox or LoRa, all these examples operate at a certain rhythm. They thus all use a *clock signal* as metronome, whose frequency depends on both the circuits type and the corresponding applications requirements.

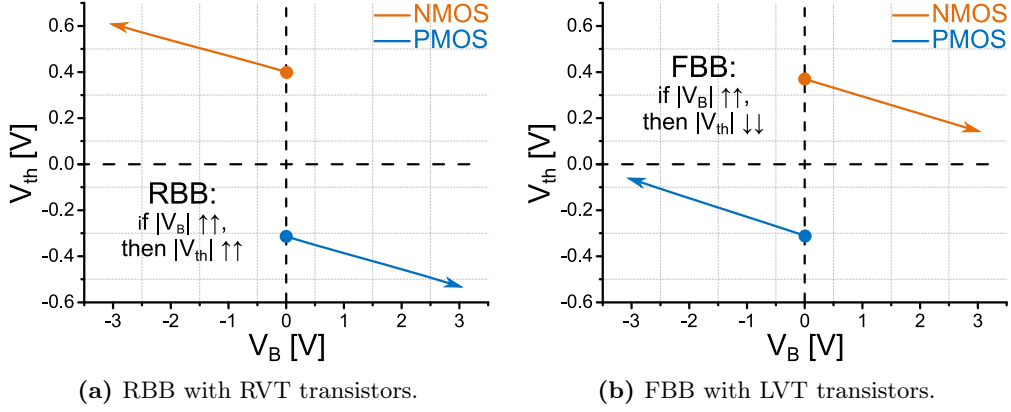


Fig. 3 Evolution of the threshold voltage V_{th} with the back-bias voltage V_B . Illustration of the effect of reverse back biasing (RBB) and forward back biasing (FBB) in 28-nm FDSOI technology.

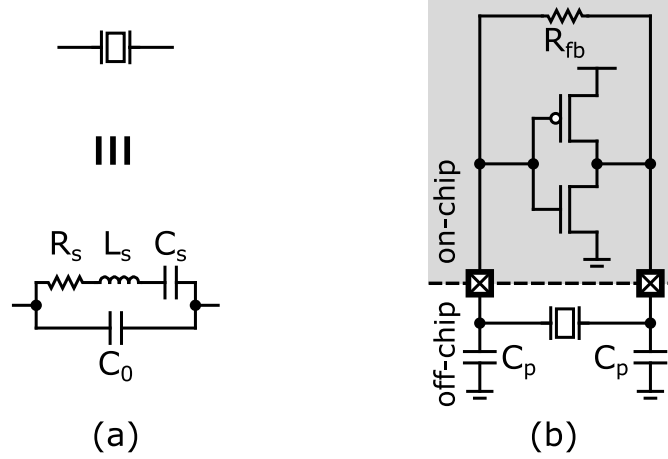


Fig. 4 Crystal oscillator illustration: (a) quartz symbol and equivalent electrical model, (b) Pierce crystal oscillator.

Clock signals are, by definition, periodic, and we need a specific kind of circuit to generate them: *oscillators*. There exist different ways to create and sustain an oscillation and thus different types of oscillators. We now briefly review in a qualitative way the main CMOS oscillators families.

Crystal Oscillators

A *crystal oscillator* (XO) uses the mechanical resonance of a quartz crystal [22]. Such a material generates an electric voltage difference at its electrodes in response to mechanical deformations and conversely. This phenomenon is known as the piezoelectric effect. Fig. 4 shows an example of XO.

A quartz crystal possesses excellent mechanical and chemical stabilities, ensuring

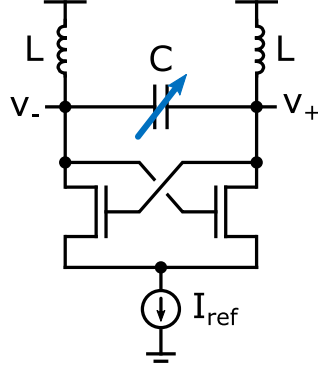


Fig. 5 Inductor-Capacitor (LC) oscillator example.

a precise and reliable resonance frequency with low sensitivity to PVT variations [22,23]. It also exhibits an extremely high quality factor Q [22,24] and has excellent jitter performance [25]. Therefore, XOs generally serve as very precise reference frequency generators. However, crystals are off-chip components and thus bulky [25]: they defeat the purpose of on-chip integration. Moreover, XOs suffer from poor tunability [24]. The typical fundamental frequency range of XOs goes from 10 kHz to 100 MHz [24,26].

LC Oscillators

An *inductor-capacitor* (LC) oscillator uses an LC tank as a resonant element. Fig. 5 shows an example of a cross-coupled LC oscillator. The energy continuously transfers back and forth between the capacitor (which stores energy in the form of an electrostatic field) and the inductor (which stores energy in the form of an electromagnetic field), thus creating a periodic oscillation whose frequency equals:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (4)$$

Like for XOs, LC oscillators also exhibit excellent jitter/phase noise performance [25]. However, high- Q inductors are difficult to integrate (at high frequencies) or take a large silicon area (at low frequencies) [27,28]. Besides, LC oscillators have limited tunability [27] and suffer from long start-up times. The practical frequency range of LC oscillators roughly covers 100 kHz to 100 GHz [26,29] for RF applications requiring high-precision high-frequency carrier generation.

Relaxation Oscillators

A *relaxation oscillator* uses only one energy storage element (typically a capacitor) continuously charged and discharged in a controlled manner using additional circuitry to produce a periodic signal. The oscillation period depends on the capacitor value and the time constants of the circuit. Fig. 6 shows an example of a

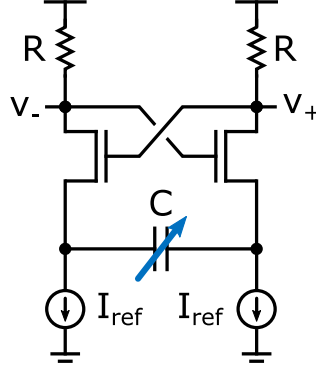


Fig. 6 Relaxation oscillator example.

CMOS relaxation oscillator.

As they usually avoid inductors, relaxation oscillators are compact and can be fully integrated on silicon [23]. They also have a low start-up time and are low power [23]. However, they suffer from higher jitter levels [23, 25]. This family of oscillators can produce various signal shapes, including square, triangular, or pulses, for instance [24]. Relaxation oscillators typically serve in low-frequency, low-power clock generation applications.

Ring Oscillators

A *ring oscillator* (RO) uses a series of N delay elements connected in a ring fashion to produce a periodic signal. Fig. 7 shows several examples of ROs. The oscillation period is $2N$ times the stage delay t_d , or equivalently, the oscillation frequency equals:

$$f_0 = \frac{1}{2Nt_d}. \quad (5)$$

Thanks to their simplicity, compactness, speed, flexibility, and low power, ROs are widely adopted [27, 30, 31]. They have a wide tuning range and a short settling time. Besides, they can intrinsically generate multiple clock phases [30]. Their main drawbacks lie in their poor jitter/phase noise performance [30] and their higher sensitivity to PVT variations [23]. These last two reasons do not prevent them from having tremendous success as they serve in an increasing number of applications, including (but not limited to) processor clock generation or wireless-communications frequency synthesis, for instance.

There are various types of ROs: they can be *single-ended*, as illustrated in Fig. 7(a), or *differential*, as represented in Fig. 7(b). In addition, several techniques exist to control the RO frequency and obtain a *voltage-controlled ring oscillator* (VCRO). For example, we can modify the frequency by tuning the supply voltage [32] or the load capacitors [33]. However, the most conventional technique is *current starving* and controls the RO frequency by varying the current flowing in its constitutive

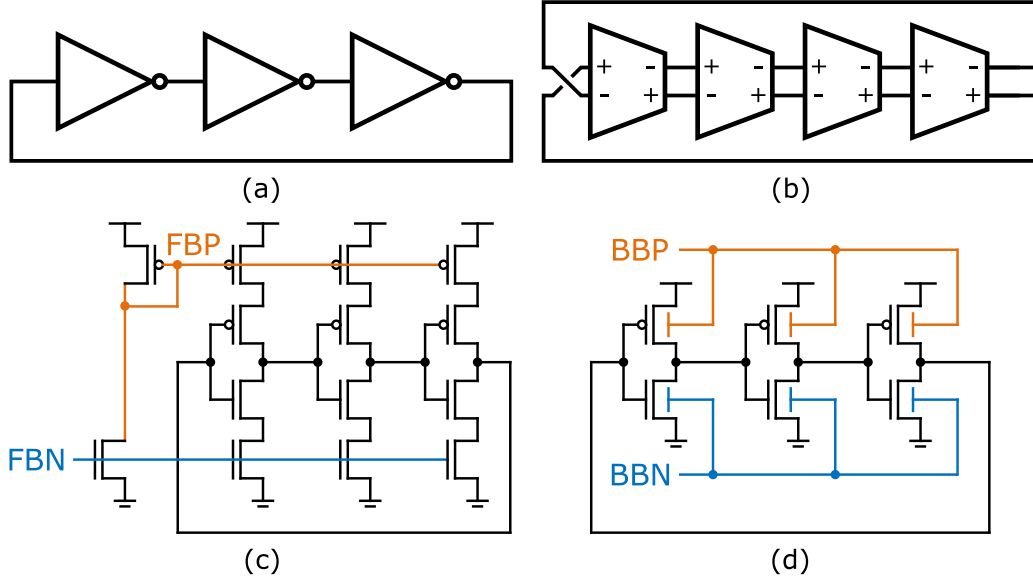


Fig. 7 Ring oscillator (RO) examples: (a) 3-stage single-ended RO, (b) 4-stage differential RO, (c) conventional current-starved RO, (d) back-bias-controlled RO in FDSOI technology.

delay stages. The resulting VCRO architecture, called a *current-starved ring oscillator* (CSRO), appears in Fig. 7(c). In FDSOI CMOS technologies, the BB feature is an alternative to control the RO frequency by modulating its transistors threshold voltage V_{th} , as done in [34]. It gives rise to a new kind of VCRO topology, called a *back-bias-controlled oscillator* (BBCO), as represented in Fig. 7(d).

Throughout this dissertation, we will focus on ROs. Thanks to their compactness and low power, ROs are, indeed, perfect candidates in the context of IoT applications. In addition, IoT and ULP applications usually target relaxed performance levels, for which the higher phase noise of the ROs is not an issue. Finally, their broader tuning range can compensate for their higher sensitivity to PVT variations.

Research Questions and Thesis Outline

After this general introduction, we now present the objectives of this dissertation together with its outline.

This thesis explores the various possibilities enabled by the FBB feature of the FDSOI CMOS technology and applies them to the domains of clock generation and frequency synthesis. In particular, we focus on lowering the power consumption to improve the energy efficiency and compensating for PVT variations to improve the circuits robustness. In addition, we look for highly integrable design solutions for minimizing chip area and footprint. These objectives line up with the requirements of the IoT without being limited to this particular applicative context.

We divide our contributions into three chapters, each of them related to particular

research questions. Our dissertation comprises a mixture of theoretical/simulation-based analysis and experimental results obtained from 3 chip prototypes fabricated in 28-nm FDSOI technology from STMicroelectronics.

Question 1: *How do FDSOI-enabled BBCOs compare to conventional CSROs?*

Our first chapter proposes a comprehensive comparison between the recent FDSOI-enabled BBCOs and conventional CSROs, taking a block-level perspective. In particular, we focus on two fundamental limits: the minimum power consumption and the best power/noise trade-off these oscillators can achieve. In addition, we also take practical design constraints such as PVT robustness, frequency tuning range, and frequency gains into account. Our analysis uses compact analytical models derived from conventional RO theory and extensive pre-layout simulation results applied to the specific 28-nm FDSOI technology node. The contents of this first chapter are adapted from [JP1].

The results showcase engaging advantages brought by BBCOs. Indeed, in 28-nm FDSOI, they can reach lower power levels and better power/phase noise trade-offs than their CSRO counterparts. Besides, BBCOs exhibit a more linear transfer function, which is of interest in phase-locked loops (PLLs), for instance. These benefits mostly come from the FBB feature, which appears to be an excellent tuning knob for ULP/ULV VCROs. However, Chapter 1 also highlights some design challenges concerning the BBCO topology, that need to be addressed at the system level during design time.

Question 2: *How to exploit FBB in BBCO-based PLLs?*

Chapter 2 builds upon the learning outcomes of Chapter 1 by analyzing with a system-level perspective the use of FBB and BBCOs inside PLLs. In addition to the block-level advantages identified in Chapter 1, FBB might also benefit at the PLL level but raises additional system-level challenges. We exemplify how to tackle these challenges by designing a chip prototype in 28-nm FDSOI: we propose a dual-PLL clock recovery (CR) unit embedded within a 2.5-Gb/s ultra-wideband (UWB) radio. The proposed UWB transceiver, named WiXpress, aims at wireless low-power chip-to-chip communications over short distances.

The CR comprises two complementary PLLs: the first one for fast frequency acquisition and the second for high-bandwidth phase tracking. Both PLLs share the same BBCO and use the FBB voltage nodes as frequency control knobs. Besides, the FBB feature enables a low-voltage and low-power operation. It also extends the CR functionality to a wide PVT variations range, including asymmetric skewed process corners. The corresponding experimental results are competitive in power, performance, and area: the CR unit locks in less than 1.1 μ s, consumes 1.034 mW in lock conditions, generates 6.5 ps of RMS long-term jitter, and occupies a limited silicon surface of 0.043 mm². Compared to the state of the art, the CR unit is highly energy-efficient and exhibits an excellent power/jitter trade-off, demonstrating the relevance of FBB in the context of low-power PLLs. The contents of this chapter

are adapted from [JP2].

Question 3: *How to fully exploit FBB in adaptive regulation loops for unified clock generation/PVT compensation in ULV/ULP circuits?*

Our last chapter focuses on the clock generation and PVT compensation in ULV/ULP microcontroller units (MCUs) in the context of IoT applications. From the review of several adaptive techniques commonly used to cover the PVT variations, Chapter 3 proposes a *unified frequency and back-bias regulation* (UFBBR), a new adaptive mechanism that combines clock generation with adaptive FBB for the PVT compensation in a single loop. The UFBBR compensates for PVT variations, affecting both the logic speed and the N/PMOS process imbalance of the circuit to regulate, using asymmetric adaptive FBB. It is thus a closed-loop system comprising sensors, a control unit, and FBB actuators. A BBCO simultaneously serves as clock generator and logic speed sensor.

We experimentally demonstrate the benefits of the UFBBR technique with two chip prototypes manufactured in 28-nm FDSOI technology. Our two UFBBR designs are integrated in two different MCU systems on chips (SoCs), respectively named SleepRunner [CP1, JP3] and SleepRider [CP2].

Compared to other ABB generators in the literature, our proposed UFBBR designs appear very competitive, showcasing a fast settling time ($< 10 \mu\text{s}$) for limited power ($< 22 \mu\text{W}$) and area overheads ($< 0.06 \text{ mm}^2$). They also greatly benefit at the MCU level. Their adaptive FBB generation enables an energy-efficient MCU operation at ULV/ULP in active mode ($3\text{-}5.5 \mu\text{W}/\text{MHz}$), in addition to PVT compensation and tolerance against sudden voltage droops. In sleep mode, our UFBBR circuits disable the clock generation and drive the FBB voltages towards 0 V to save power. Thanks to fast transitions between sleep and active modes, they also minimize the wake-up/going-to-sleep overheads. All these features demonstrate the relevance of the UFBBR concept for ULV/ULP applications. The contents of this chapter are adapted from [JP3, JP4, CP1, CP2].

Comparison of Voltage-Controlled Ring Oscillators

Contents

1.1	Introduction	16
1.2	Jitter and Phase Noise	16
1.3	Considered Ring Oscillator Architectures	23
1.4	Uncontrolled Ring Oscillator Analysis	27
1.5	Current-Starving Versus Back-Bias Control	35
1.6	Conclusion	48

Abstract Back-bias control is a new degree of freedom brought by FDSOI CMOS technologies, which can be used to control the oscillation frequency of voltage-controlled ring oscillators (VCROs). The resulting VCRO architecture is called a back-bias-controlled oscillator (BBCO). This first chapter compares it with the conventional current-starved ring oscillator (CSRO) topology in terms of power consumption and phase noise figure of merit (FoM), while taking practical design constraints of process, voltage, and temperature (PVT) robustness and frequency tuning range into account. The proposed comprehensive analysis takes advantage of relevant and compact analytical models, as well as extensive pre-layout simulation results. The comparison is made at four different target oscillation frequencies, which are representative of frequency synthesis for WiFi/Bluetooth/LPWAN wireless communications and of clock generation for smartphone/Internet-of-Things processors: 300 MHz, 868 MHz, 2.45 GHz, and 5.18 GHz. In 28-nm FDSOI technology, the results demonstrate that BBCOs can intrinsically reach $1.69\times$ to $4.63\times$ lower minimum power consumption and slightly better phase noise figure-of-merit (FoM) values than CSROs [JP1].

1.1 Introduction

This first chapter compares back-bias-controlled oscillators (BBCOs) to conventional current-starved ring oscillators (CSROs), with a focus on the corresponding power consumption and on the trade-off between power and phase noise. The comprehensive analysis proposed here relies on relevant and compact analytical models derived from conventional ring oscillator (RO) theory, as well as extensive pre-layout simulation results applied to the particular 28-nm FDSOI technology node. Practical design constraints, such as process, voltage, and temperature (PVT) robustness and frequency tuning range, are also taken into account.

This chapter is adapted from [JP1] and structured as follows. Firstly, Section 1.2 introduces the concepts of jitter and phase noise. Then, Section 1.3 presents the RO architectures under study as well as the hypotheses made in this work. Section 1.4 explains our analysis methodology applied to simple uncontrolled ROs, which are used as starting examples. Section 1.5 follows with a comparison of current starving and back-bias control, for a target oscillation frequency of 2.45 GHz. An extension to 300 MHz, 868 MHz, and 5.18 GHz target frequencies is also provided, to broaden the discussion. These frequency values are representative of a broad range of applications, ranging from frequency synthesis for WiFi/Bluetooth/LP-WAN wireless communications to clock generation intended for smartphone/IoT processors. Useful mathematical developments are gathered in Appendix A and are used in this chapter to support the proposed analysis.

1.2 Jitter and Phase Noise

In the context of clock generation and frequency synthesis, *jitter* and *phase noise* are very important nonidealities to take into account. This section introduces and defines these concepts, with the help of Fig. 1.1. The link existing between them is also explained, before presenting two very common figures of merit. This section takes inspiration from the book of Nicola Da Dalt [29], which in our opinion provides the most comprehensive treatment of the subjects of jitter and phase noise to date.

Let us consider an *ideal clock signal* with period T_0 , as depicted in Fig. 1.1(a). The corresponding oscillation frequency is denoted by $f_0 = 1/T_0$. Such a signal can mathematically be expressed as follows [29, 35, 36]:

$$v(t) = A \operatorname{sgn} [\sin (2\pi f_0 t)], \quad (1.1)$$

where A is the signal amplitude, and the sgn function is defined as:

$$\operatorname{sgn}(x) = \begin{cases} +1 & \text{for } x > 0, \\ 0 & \text{for } x = 0, \\ -1 & \text{for } x < 0. \end{cases} \quad (1.2)$$

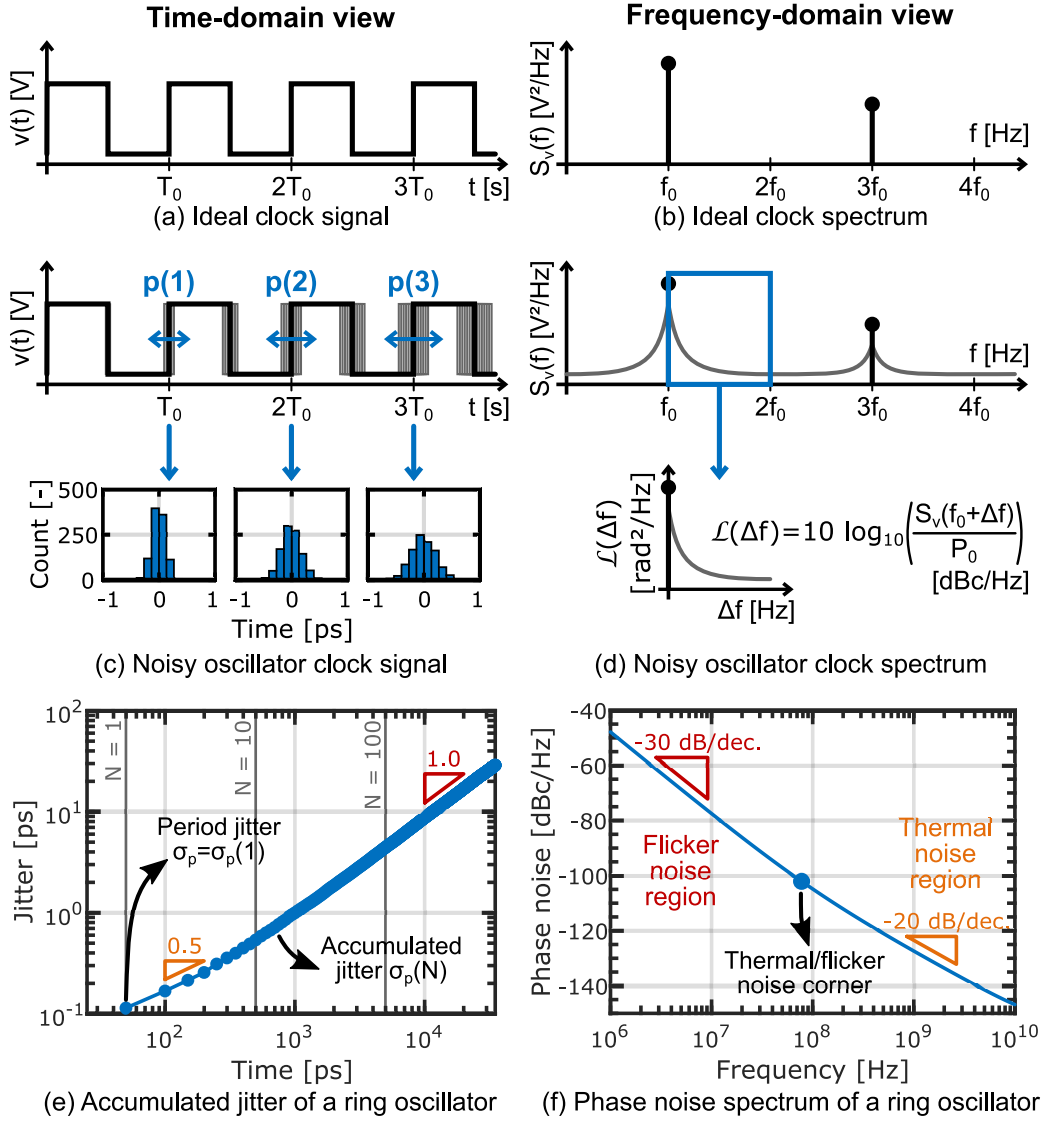


Fig. 1.1 Illustration of the jitter and phase noise concepts. The simulated curves given in (e)-(f) are obtained with a 20-GHz 5-stage inverter-based ring oscillator.

This clock is considered ideal because all its successive rising edges are separated in time by exactly T_0 . In the frequency domain, this translates into spectral lines exactly located at odd multiples of f_0 [29, 37] in the power spectral density (PSD) of the clock signal¹, as represented in Fig. 1.1(b).

In practice, noise is present and can affect the clock signal $v(t)$ [29, 35, 36], through its phase and amplitude, as follows:

$$v(t) = (A + \varepsilon(t)) \operatorname{sgn} [\sin (2\pi f_0 t + \varphi(t))]. \quad (1.3)$$

¹Assuming that $v(t)$ is an odd zero-mean clock signal with a perfect duty-cycle of 50% in the time domain, only odd harmonics appear in its spectrum.

The quantity $\varphi(t)$ is named *excess phase* [29] and it affects the zero crossings of the clock signal. In other words, it deviates the clock edges from their ideal positions and creates *jitter*. As a consequence, successive rising edges of the clock are not always perfectly separated by T_0 in the time domain, they are separated by T_0 only *in average*, as illustrated in Fig. 1.1(c). It is important to notice that each deviation affecting a particular edge of an oscillator clock will also impact all its subsequent edges, leading to *jitter accumulation*, as can be observed with the histograms in Fig. 1.1(c). The second quantity, $\varepsilon(t)$, is generally called *amplitude noise* or *amplitude distortion* [29]. We neglect it in this work because it usually does not contribute significantly to the jitter/phase noise generation², compared to the excess phase [29, 35].

In the frequency domain, instead of being concentrated exactly at multiples of the nominal frequency f_0 , the power of a noisy oscillator clock is now spread around its harmonics [37], as shown in Fig. 1.1(d), and is at the origin of the *phase noise* generation.

At this point, without having rigorously defined what jitter and phase noise are, we can already grasp a link existing between them: they are both quantifying the impact of noise affecting a clock signal, but observed from different views; jitter is observed in the time domain while phase noise is essentially a frequency-domain nonideality.

1.2.1 Jitter Definitions

In the context of this work, the jitter can be defined as the time interval separating the position of a rising edge of the clock relative to a chosen reference time frame [29]. It is intrinsically a discrete-time random process, as it can only be measured when a clock transition is occurring. As an arbitrary time frame can be chosen as reference, there exist several types of jitter. We will only focus on two of them here, namely the *period jitter* and the *N-period jitter*.

Period Jitter

The period jitter of a noisy clock is the deviation of the clock period with respect to its nominal value [29]. In other words, it is a random process $\mathbf{p}$ where the sample $\mathbf{p}_k$ designates the variation around its nominal value of the position of a rising edge with respect to the previous one. Mathematically, if t_k denotes the k^{th} rising edge of the clock, this gives:

$$\mathbf{p}_k = \underbrace{(t_{k+1} - t_k)}_{k^{\text{th}} \text{ period}} - T_0. \quad (1.4)$$

Generally, the wording *period jitter* refers to the root mean square (RMS) value of $\mathbf{p}$,

²Indeed, as long as $A + \varepsilon(t)$ does not reach zero, amplitude noise cannot affect the zero crossings of the clock signal $v(t)$.

or, equivalently, its standard deviation $\sigma_{\mathbf{p}}$ because it is a zero-mean random process. The period jitter is also sometimes called *cycle jitter* in the literature [29].

N -period Jitter

The period jitter quantifies the variation of the time interval between successive rising edges, nominally separated by one period T_0 . In a similar manner, the N -period jitter quantifies the variation of the time interval between rising edges nominally separated by N periods (NT_0) [29]. It is a random process $\mathbf{p}(N)$ where the sample $\mathbf{p}_k(N)$ is the variation around its nominal value of the position of a rising edge with respect to the N^{th} previous one. This translates to the following mathematical relation:

$$\mathbf{p}_k(N) = (t_{k+N} - t_k) - NT_0. \quad (1.5)$$

It is easy to prove that the realized N -period jitter is the sum of the period jitter samples over N consecutive periods:

$$\mathbf{p}_k(N) = \sum_{i=k}^{k+N-1} (t_{i+1} - t_i - T_0) = \sum_{i=k}^{k+N-1} \mathbf{p}_i, \quad (1.6)$$

which is the reason why the N -period jitter is also called *accumulated jitter* in the literature [29]. When N takes very large values (ideally, when it tends towards infinity), the accumulated jitter is also called *long-term jitter* [29]. Being also a zero-mean random process, the wording *N -period jitter* generally designates the RMS value of $\mathbf{p}(N)$, or, equivalently, its standard deviation $\sigma_{\mathbf{p}}(N)$.

As an example, Fig. 1.1(e) shows the evolution in time of the accumulated jitter of a 20-GHz ring oscillator clock. The first point of the curve corresponds to the period jitter ($N = 1$). As can be observed, the long-term jitter of the oscillator is unbounded, as jitter accumulates indefinitely. This justifies the practical need of feedback loops, such as phase-locked ones (see Chapter 2), to limit this accumulation.

Besides, depending on the dominant noise source type, the slope of the jitter accumulation differs. On one hand, when *thermal noise* dominates, the RMS N -period jitter grows with the square root of N [29, 36]:

$$\sigma_{\mathbf{p}}(N) = \sqrt{N} \sigma_{\mathbf{p}}. \quad (1.7)$$

In logarithmic scale, this gives a slope of 0.5, as can be observed in Fig. 1.1(e) (in orange). Indeed, as the thermal noise is white with a uniform spectral distribution of its PSD, all periods have uncorrelated and identically distributed period jitter values. The N -period variance is thus the sum of the N individual period jitter variances.

Table 1.1 Summary of fundamental jitter definitions (replicated from [29]).

Jitter	Symbol	Definition	Formula
Absolute	$\mathbf{a}_k$	Deviation of the clock edge position from the ideal one	$t_k - kT_0$
Relative	$\mathbf{r}_k$	Difference of the corresponding edge positions of two clocks (A and B)	$t_k^A - t_k^B$
Period	$\mathbf{p}_k$	Deviation of the clock period from its nominal value	$t_{k+1} - t_k - T_0$
N -period	$\mathbf{p}_k(N)$	Deviation of the duration of N consecutive periods from its nominal value	$t_{k+N} - t_k - NT_0$
Cycle-to-cycle	$\mathbf{cc}_k$	Difference between two consecutive clock periods	$t_{k+2} - 2t_{k+1} + t_k$

Table 1.2 Summary of fundamental jitter relationships (replicated from [29]).

Jitter	Symbol	Versus Absolute Jitter	Versus Period Jitter
Absolute	$\mathbf{a}_k$	—	—
Relative	$\mathbf{r}_k$	$\mathbf{a}_k^A - \mathbf{a}_k^B$	—
Period	$\mathbf{p}_k$	$\mathbf{a}_{k+1} - \mathbf{a}_k$	—
N -period	$\mathbf{p}_k(N)$	$\mathbf{a}_{k+N} - \mathbf{a}_k$	$\sum_{i=k}^{k+N-1} \mathbf{p}_i$
Cycle-to-cycle	$\mathbf{cc}_k$	$\mathbf{a}_{k+2} - 2\mathbf{a}_{k+1} + \mathbf{a}_k$	$\mathbf{p}_{k+1} - \mathbf{p}_k$

On another hand, when *flicker noise* dominates, consecutive periods become correlated. Therefore, the RMS period jitter values add up rather than their variances, and the RMS N -period jitter thus grows linearly with the number of periods N [29, 36]:

$$\sigma_{\mathbf{p}}(N) = N\sigma_{\mathbf{p}}. \quad (1.8)$$

This observation is confirmed by the slope of 1 (in log-log scale) shown in Fig. 1.1(e) (in red). Flicker noise is also called $1/f$ noise and has most of its energy at low frequencies. It thus becomes dominant over thermal noise for large measurement times.

Other Types of Jitter

There exist several other types of jitter that we will not cover here. As an overview, Tables 1.1 and 1.2 respectively give the definition of the most common jitter types and the relations existing between them. Please refer to [29] for more details.

1.2.2 Phase Noise Definition

The concept of phase noise, despite being very common, is less intuitive than jitter. Rigorously speaking, it is defined as half the one-sided PSD S_φ of the excess phase φ [29] and takes units of rad^2/Hz :

$$\mathcal{L}(\Delta f) = \frac{S_\varphi(\Delta f)}{2}. \quad (1.9)$$

In practice, the phase noise at an offset frequency Δf of the carrier f_0 is obtained as the power of the voltage signal within 1-Hz band normalized by the carrier power [29,35]. This is the operation performed by a spectrum analyzer, for instance. Mathematically, this translates to the following definition:

$$\mathcal{L}(\Delta f) = \frac{S_v(f_0 + \Delta f)}{P_0}, \quad (1.10)$$

which is illustrated in Fig. 1.1(d). The term P_0 designates the power of the fundamental tone (or the carrier power in wireless communications):

$$P_0 = \int_{0.5f_0}^{1.5f_0} S_v(f) df. \quad (1.11)$$

Under some assumptions (please refer to [29] for a complete discussion), the two phase noise definitions given above are equivalent. Note that both the random excess phase and the phase noise are continuous-time random processes.

The phase noise is usually quantified with logarithmic units, in decibels below the carrier per Hz (dBc/Hz). An example of phase noise spectrum is shown in Fig. 1.1(f) for a 20-GHz ring oscillator. As can be observed, two distinct regions appear, depending on the type of the dominant noise source. On one hand, the phase noise generated by a *thermal noise* source typically exhibits a $1/f^2$ profile [29,35,36,38,39], which translates into a slope of -20 dB/decade in Fig. 1.1(f) (in orange). On another hand, at low frequencies, *flicker noise* dominates and upconverts into a $1/f^3$ phase noise profile [29,35,38], leading to a slope of -30 dB/decade in Fig. 1.1(f) (in red). The frequency at which the contributions of thermal noise and flicker noise are equal in the phase noise spectrum is named the *thermal/flicker noise corner frequency*.

1.2.3 Link Between Jitter and Phase Noise

Now that both the jitter and the phase noise are properly defined, we can understand more deeply the link existing between them. This relationship lies in the excess phase φ [29]. We will explicit it for the case of N -period jitter.

The N -period jitter definition given in (1.5) can be rewritten in terms of excess phase as follows [38]:

$$\mathbf{p}_k(N) = \frac{\varphi(t_k + NT_0) - \varphi(t_k)}{2\pi f_0} - NT_0. \quad (1.12)$$

We thus move from a continuous-time random process φ to the discrete-time random process $\mathbf{p}_k(N)$ through a sampling operation. The one-sided PSD of the N -period

Table 1.3 Link between N -period jitter and phase noise expressions.

Noise Type	Profile	From Phase Noise to N -period Jitter	From N -period Jitter to Phase Noise
Thermal Noise	$\mathcal{L}(\Delta f) = \frac{\mathcal{L}_1 \Delta f_1^2}{\Delta f^2}$	$\sigma_{\mathbf{p}}(N) = \sqrt{\frac{\mathcal{L}_1 \Delta f_1^2}{f_0^3}} \sqrt{N}$	$\mathcal{L}(\Delta f) = \frac{\sigma_{\mathbf{p}}^2(N)}{N} \frac{f_0^3}{\Delta f^2}$
Flicker Noise	$\mathcal{L}(\Delta f) = \frac{\mathcal{L}_2 \Delta f_2^3}{\Delta f^3}$	$\sigma_{\mathbf{p}}(N) \approx 5 \sqrt{\frac{\mathcal{L}_2 \Delta f_2^3}{f_0^4}} N$	$\mathcal{L}(\Delta f) \approx \frac{1}{25} \frac{\sigma_{\mathbf{p}}(N)}{N^2} \frac{f_0^4}{\Delta f^3}$

jitter can now be obtained as follows:

$$S_{\mathbf{p}}(f, N) = \frac{1}{4\pi^2 f_0^2} \left| 1 - \exp^{-j2\pi f N T_0} \right|^2 S_{\varphi}(f) = \frac{\sin^2(\pi f N T_0)}{\pi^2 f_0^2} S_{\varphi}(f). \quad (1.13)$$

As the phase noise and the excess phase PSD are directly linked by (1.9), this becomes:

$$S_{\mathbf{p}}(f, N) = \frac{2}{\pi^2 f_0^2} \sin^2(\pi f N / f_0) \mathcal{L}(f). \quad (1.14)$$

By application of the Wiener-Khinchin theorem, the N -period variance can now simply be found by integration, finally linking phase noise to jitter [29, 38]:

$$\sigma_{\mathbf{p}}^2(N) = \int_0^{+\infty} S_{\mathbf{p}}(f, N) df = \frac{2}{\pi^2 f_0^2} \int_0^{+\infty} \sin^2(\pi f N / f_0) \mathcal{L}(f) df. \quad (1.15)$$

This equation shows that minimizing the phase noise spectrum also minimizes the N -period jitter. Table 1.3 applies (1.15) in the case of thermal noise or flicker noise dominance, and obtains closed-form expressions for the N -period jitter from the phase noise spectrum, and vice-versa.

1.2.4 Figures of Merit

To conclude this section about jitter and phase noise, we propose to take a look at two common *figures of merit* (FoMs). They arise from the well-known trade-off existing for oscillators between jitter/phase noise and power [29, 30, 35–41], and appear useful in practice for oscillator comparison purposes.

Phase Noise FoM

The *phase noise FoM* is very often used to compare oscillators [29, 30, 40] and is defined as follows:

$$\text{FoM} = \mathcal{L}(\Delta f) \left(\frac{\Delta f}{f_0} \right)^2 \left(\frac{P}{1 \text{ mW}} \right). \quad (1.16)$$

It normalizes the oscillator phase noise $\mathcal{L}(\Delta f)$ value (in linear scale) by the power consumption P consumed by the oscillator (in mW), the oscillation frequency f_0 (in Hz), and the offset frequency Δf (in Hz) at which the phase noise is measured

within the $1/f^2$ region dominated by the thermal noise. It thus has units of rad^2/Hz , as the phase noise.

However, the FoM is preferably expressed in logarithmic scale, in dBc/Hz :

$$\text{FoM} = \mathcal{L}(\Delta f) + 20 \log_{10} \left(\frac{\Delta f}{f_0} \right) + 10 \log_{10} \left(\frac{P}{1 \text{ mW}} \right), \quad (1.17)$$

with $\mathcal{L}(\Delta f)$ also expressed in dBc/Hz . The lower its value, the better the power/phase noise trade-off.

The phase noise FoM is not only an interesting metric for the comparison of different oscillator designs (different types of oscillators, or different oscillation frequencies, for instance), but can also be applied to larger systems used for clock generation or frequency synthesis, such as phase-locked loops (PLLs).

Jitter FoM

A second popular FoM concerns the jitter. This *jitter FoM* is defined as follows [40]:

$$\text{FoM}_{\text{jitter}} = \frac{\sigma_{\text{lt-jitter}}^2}{1 \text{ s}^2} \frac{P}{1 \text{ mW}}. \quad (1.18)$$

It normalizes the long-term jitter $\sigma_{\text{lt-jitter}}$ by the power consumption, and is unitless. It can also be used in logarithmic scale (in dB), thus yielding:

$$\text{FoM}_{\text{jitter}} = 10 \log_{10} \left(\frac{\sigma_{\text{lt-jitter}}^2}{1 \text{ s}^2} \frac{P}{1 \text{ mW}} \right). \quad (1.19)$$

The lower its value, the better the oscillator power/jitter trade-off. As discussed previously, the long-term jitter of oscillators is unbounded because of jitter accumulation. Therefore, the jitter FoM cannot be applied to oscillators alone. It is rather used for the comparison of PLLs (see Chapter 2).

1.3 Considered Ring Oscillator Architectures

This section presents the three RO architectures studied in this chapter and the corresponding hypotheses. The focus is on simple single-ended ring architectures, but the analysis described in this work could be extended to more sophisticated topologies, such as differential and multi-path topologies.

1.3.1 VCRO Topologies

As shown in Fig. 1.2, a simple single-ended inverter-based N -stage RO is composed of an odd number N of inverting delay elements with a supply voltage V_{DD} [30]. Different types of inverting cells result in different RO architectures. An *uncontrolled*

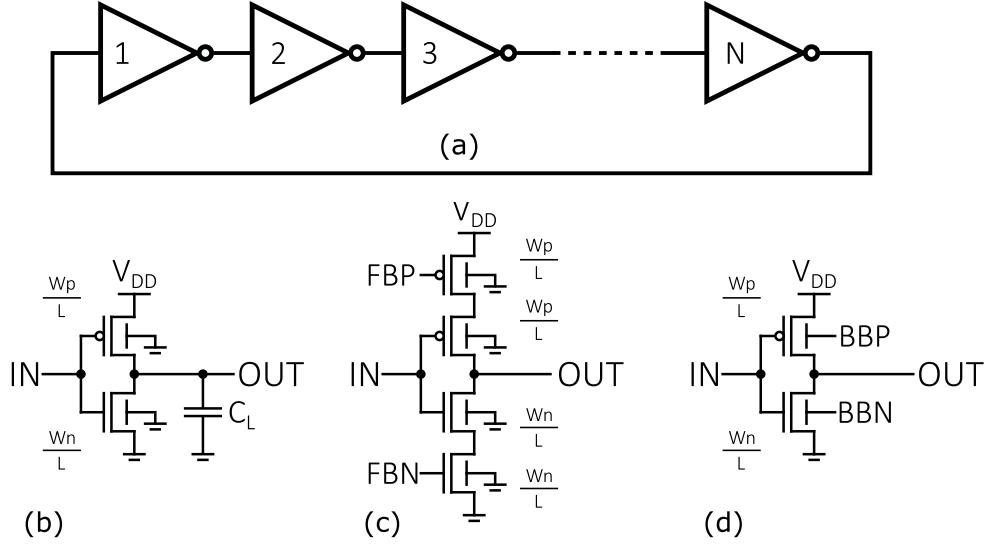


Fig. 1.2 (a) Schematics of a single-ended N -stage RO supplied by V_{DD} and three different kinds of inverting stages in FDSOI technology using LVT flipped-well devices: (b) uncontrolled, (c) current-starved, and (d) back-bias-controlled inverter.

RO is composed of simple inverters [Fig. 1.2(b)], possibly loaded with additional capacitors. A *current-starved ring oscillator* (CSRO) uses current-starved inverters [Fig. 1.2(c)] and features two frequency control nodes, FBN and FBP . Finally, a *back-bias-controlled oscillator* (BBCO) is made of back-bias-controlled inverters [Fig. 1.2(d)] and its two control voltages are the back-gate voltages, BBN and BBP . The CSRO and the BBCO topologies are two types of voltage-controlled ring oscillators (VCROs).

Symmetrical Biasing

In practice, VCROs are usually controlled by only one control node instead of two. This is the reason why we assume a *symmetrical biasing* in this work.

For the CSRO topology, FBN is chosen as primary control and FBP is defined as its symmetrical voltage with respect to V_{DD} [42]:

$$FBP = V_{DD} - FBN. \quad (1.20)$$

This can simply be generated with a current mirror branch as in [43] for instance. Both FBN and FBP have a voltage range comprised between 0 V and V_{DD} .

For BBCOs, BBN is the main control voltage and BBP has an opposite value (symmetrical to BBN with respect to the ground level):

$$BBP = -BBN. \quad (1.21)$$

This means BBP is negative, and is usually generated with on-chip charge pumps [JP3, 20]. The voltage range of BBN (resp. BBP) goes from 0 V to +3 V (resp. from 0 V to -3 V) [16].

Oscillation Frequency

The oscillation frequency f_0 of an N -stage VCRO supplied by V_{DD} can be obtained as follows [38]:

$$f_0 = \frac{I}{N V_{DD} C}, \quad (1.22)$$

where C denotes the total capacitance seen at the output of each inverting stage (sum of the intrinsic parasitic capacitance of the transistors and the possibly added loading capacitor C_L). Equation (1.22) assumes a perfect current matching between NMOS and PMOS devices as well as a perfect capacitance matching among the N inverting stages.

By definition, the oscillation frequency of VCROs is tunable. For the CSRO and BBCO architectures considered in this work, the frequency is tuned through the variation of the delay element current I , which is function of FBN for CSROs and of BBN for BBCOs. In other words, assuming a strong inversion regime, we have:

- For uncontrolled ROs: $I = \beta (V_{DD} - V_{th,0})^2, \quad (1.23)$

- For CSROs: $I(FBN) = \beta (FBN - V_{th,0})^2, \quad (1.24)$

- For BBCOs: $I(BBN) = \beta (V_{DD} - V_{th,0} + \gamma_b BBN)^2. \quad (1.25)$

In Equations (1.23)-(1.25), the term β regroups the devices dimensions W and L , the mobility and the gate-oxide capacitance per unit of area, γ_b is the body factor parameter which takes values around 70-85 mV/V in 22/28-nm FDSOI technology [14, 16, 18], and $V_{th,0}$ designates the zero-bias threshold voltage. Second-order effects, such as V_{th} roll-off, drain-induced barrier lowering (DIBL), and velocity saturation, are neglected in this work.

These equations show that an increase of FBN for CSROs or BBN for BBCOs leads to an increase of their corresponding stages current, which in turn results in a frequency increase. The main difference between both VCRO types thus lies in the way the current is affected by their respective control voltage: CSROs act on the gate-to-source voltage FBN of the header/footer transistors used, while BBCOs act on the decrease of the threshold voltage $V_{th} = V_{th,0} - \gamma_b BBN$ of the inverting transistors by the use of forward back biasing through BBN .

1.3.2 Important Hypotheses About Simulation and Sizing

Each of the three aforementioned RO architectures has numerous design parameters available (i.e., number of stages, transistor sizes, voltages). For clarity in the subsequent analysis and for simulation efficiency, several hypotheses related to

their sizing are made in this work to decrease the number of free parameters while enabling a fair objective comparison.

As mentioned in the chapter introduction, the RO comparison presented in this work uses pre-layout SPICE simulation results. They are obtained with steady-state analysis (SST and SSTNOISE) from Eldo simulator piloted by Matlab.

In order to have back-bias control capability, the 28-nm FDSOI CMOS technology from STMicroelectronics is selected. Only low- V_{th} (LVT) flipped-well devices are used, to be able to scale down the supply voltage more aggressively.

Concerning the sizes, the same gate length L is used for all the transistors of a given RO, for layout regularity concern. The width ratio W_p/W_n between PMOS and NMOS devices is set to 2.5 for matched rising/falling edges. The width of all NMOS transistors W_n is fixed to 200 nm. Instead of the transistor width, the device multiplier M (equal to the number of devices placed in parallel) is used to increase the inverter current. This can be implemented at the layout level with multiple fingers.

With all these assumptions in hand, the number of degrees of freedom for each RO architecture considered in this work reduces to 6: the supply voltage V_{DD} , the number of stages N , the optional loading capacitor value C_L , the transistors gate length L , the device multiplier M , and the control voltage FBN or BBN .

1.3.3 Remarks Concerning the Phase Noise FoM

The developments carried out in the next sections focus particularly on the trade-off existing between power and phase noise experienced by all kinds of oscillators [29, 35–39]. The phase noise FoM presented in Section 1.2 with (1.16) quantifies this trade-off and is used in this work.

However, it is necessary to choose an adequate value for the offset frequency Δf . In this work, we fixed it to 100 MHz, to be well above the thermal/flicker-noise corner frequency f_c . Indeed, the FoM formula of (1.16) is only valid in the $1/f^2$ region of the phase noise spectrum, resulting from the up-conversion of thermal noise. Besides, the flicker noise contribution can effectively be filtered out in practice when corresponding VCROs are used within Type-II second-order PLLs with a sufficiently high bandwidth [44, 45].

Fig. 1.3 represents two examples of RO phase noise profiles, respectively obtained at 2.2 and 35.1 GHz of oscillation frequencies. The figure shows that the phase noise taken at the chosen 100-MHz offset frequency is dominated by flicker noise when the corresponding oscillation frequency f_0 is high. At lower oscillation frequency values as the ones targeted in this work (300 MHz to 5.18 GHz), however, thermal noise dominates in both the phase noise and corresponding FoM, as desired, thanks to this choice of 100 MHz of offset frequency.

It is interesting to understand that the FoM cannot be infinitely improved. Indeed,

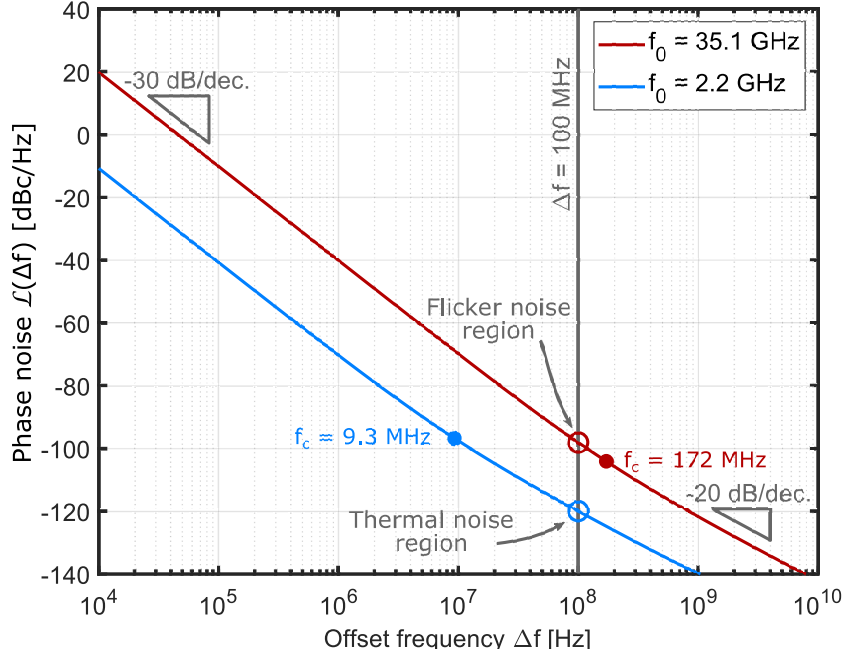


Fig. 1.3 Simulated phase noise profiles for 3-stage ROs supplied at 1.0 V, respectively oscillating at 2.2 GHz ($L = 300$ nm) and 35.1 GHz ($L = 30$ nm). The 100-MHz offset frequency line respectively intersects these profiles in their thermal and flicker noise regions.

some theoretical limits exist depending on the oscillator architecture, as represented in Fig. 1.4. For inductor-capacitor (LC) oscillators, the best achievable FoM, which mostly depends on the inductor quality factor Q , can easily achieve values lower than -180 dBc/Hz at low Q values ($Q < 5$) [29]. For single-ended inverter-based ROs as the ones studied in this chapter, the *theoretical best achievable FoM* value is -165 dBc/Hz [29] (also demonstrated in Appendix A.2) and is shown in red in Fig. 1.4. One goal in the subsequent sections is thus to determine which of the studied VCRO architectures goes closest to this FoM limit.

1.4 Uncontrolled Ring Oscillator Analysis

This section presents an analysis of the uncontrolled RO depicted in Fig. 1.2(b), in order to get more intuition about the impact of its parameters on power consumption, phase noise and corresponding FoM. The uncontrolled RO is used as a preliminary example to describe the analysis framework used in this work, which is then applied to the CSRO and BBCO topologies in Section 1.5. With the hypotheses made in Section 1.3 and as the uncontrolled RO has no control voltage, only 5 degrees of freedom are left: the supply voltage V_{DD} , the number of stages N , the load capacitor value C_L , the transistor length L , and the device multiplier M . All of them have an influence on the RO frequency, except for M as discussed in Section 1.4.2. It is thus useful to determine which of these parameters is the best tuning knob to

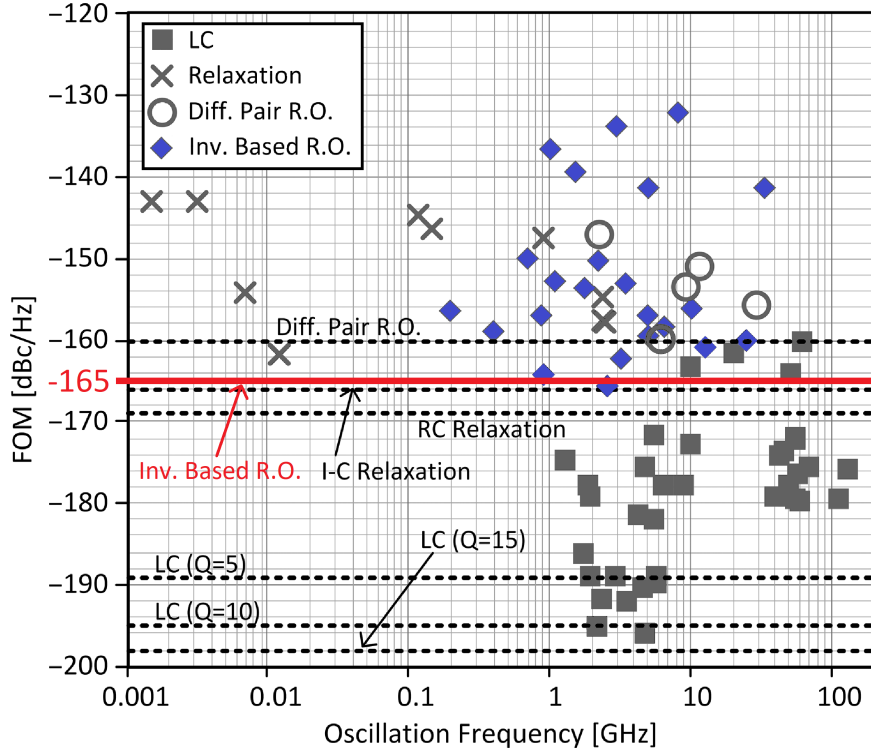


Fig. 1.4 State of the art of oscillator FoM as a function of oscillation frequency and theoretical FoM limits (modified from [29]).

achieve a given target oscillation frequency while minimizing the FoM value. This is explained in Section 1.4.1. The effect that the remaining parameter M has on power consumption, phase noise, and FoM is studied in Section 1.4.2. Finally, the uncontrolled RO is optimized for a target frequency of 2.45 GHz and the different steps of the analysis are summarized in Section 1.4.3.

1.4.1 Gate Length Scaling, the Best Way to Slow Down an RO

In the context of this chapter, the fastest uncontrolled RO is obtained at maximal supply voltage ($V_{DD} = 1.0$ V), with minimal length value ($L = 30$ nm), with minimal number of stages ($N = 3$), and without any additional loading capacitors ($C_L = 0$ fF). The corresponding oscillation frequency is 35.1 GHz and its FoM value is -158.4 dBc/Hz. This point is highlighted in black in Fig. 1.5. From that point, by decreasing V_{DD} or by increasing L , N or C_L , the oscillation frequency can be lowered to the desired target frequency (300 MHz, 868 MHz, 2.45 GHz, or 5.18 GHz in this work). Fig. 1.5 shows the evolution of the phase noise FoM value when slowing down the RO with each of these parameters separately. The theoretical FoM limit of -165 dBc/Hz is also added.

As demonstrated in Appendix A.2, the FoM expression of a single-ended inverter-

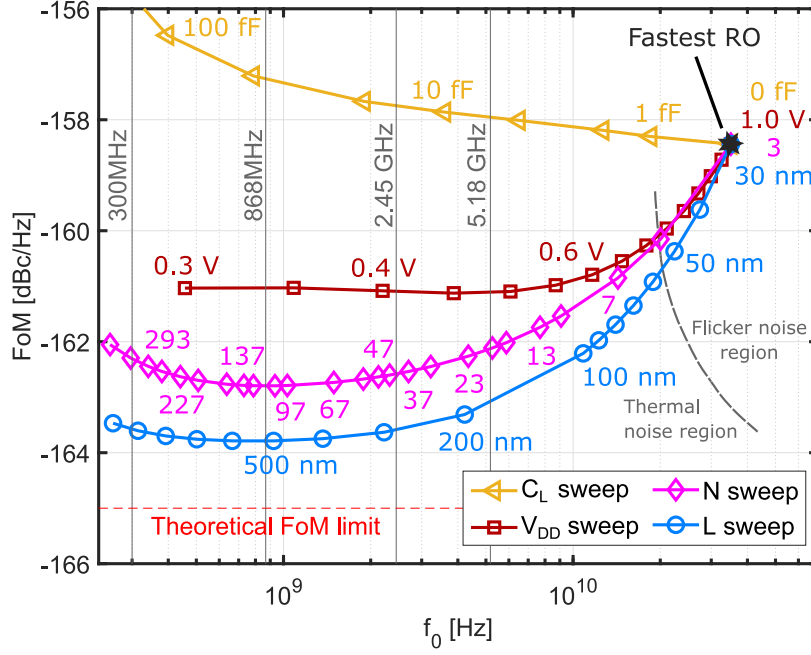


Fig. 1.5 Evolution of phase noise FoM with oscillation frequency. Each curve represents a different way of slowing down a 3-stage RO with maximal supply voltage, minimal transistor length and without loading capacitors.

based N -stage RO supplied by V_{DD} can be written in linear scale as:

$$\text{FoM} = \underbrace{2000k_B T \left(1 + \frac{2\gamma V_{DD}}{V_{DD} - V_{th,0}} \right)}_{\text{Thermal}} + \underbrace{250 \frac{\mu \kappa_f V_{DD}}{NL^2} \frac{1}{\Delta f}}_{\text{Flicker}}, \quad (1.26)$$

with k_B the Boltzmann constant, T the temperature in Kelvin, and μ the devices mobility. The γ coefficient is equal to $2/3$ for long-channel devices in saturation and takes higher values for short-channel devices [36]. The parameter κ_f is a process-dependent constant [29]. Note that this formula does not take into account second-order effects (such as V_{th} roll-off, DIBL, or velocity saturation), assumes an operation in strong inversion, and supposes a purely dynamic RO power consumption (see also the explanations given in Appendix A.1). Nonetheless, it can still be useful to validate some observations made from the results of Fig. 1.5.

At high oscillation frequencies in Fig. 1.5 (right side), the phase noise taken at a 100-MHz offset frequency is dominated by flicker noise and the corresponding FoM value decreases with V_{DD} or when increasing L or N . These trends are confirmed by Eq. (1.26) (right term). At lower oscillation frequencies in Fig. 1.5 (left side), around the target frequency values of this work (300 MHz to 5.18 GHz), the phase noise at 100-MHz offset is dominated by thermal noise. The corresponding FoM stays relatively independent from L or N , as can once again be predicted from

Eq. (1.26) (left term). The FoM plateau observed when decreasing V_{DD} cannot be predicted by (1.26) as the strong inversion hypothesis might not hold for V_{DD} values below 0.4 V.

The impact of the loading capacitor is also not well captured in (1.26) because a C_L increase slows down the stages transitions and increases the time during which both the NMOS and the PMOS transistors are on. A short circuit power thus adds to the purely dynamic power consumption assumed to develop (1.26), and it can only degrade the FoM. Using loading capacitors to slow down an RO thus appears inefficient. This is the reason why loading capacitors are totally avoided in the remaining part of the chapter (thus removing one degree of freedom). This also means that any additional parasitic capacitance (e.g., coming from interconnect routing or output buffers) should negatively impact the oscillation frequency, the power, and the corresponding FoM. In practice, parasitic capacitances coming from routing³ can typically take values between 1 and 10 fF, which translates into a limited phase noise FoM degradation below 1 dB according to Fig. 1.5. Note, however, that the FoM sensitivity towards parasitic capacitances might be more pronounced at lower supply voltages. In conclusion, parasitic capacitances should be minimized and their impacts should be carefully assessed with post-layout simulations. These considerations fall out of the scope of this chapter.

From Fig. 1.5, it is also clear that the most efficient way to slow down an RO is by upsizing the length L , as it gives the most important FoM improvement which goes closer to the theoretical limit. Consequently, in the remaining part of the chapter, the length L is used to fine tune the oscillation frequency to the desired target value.

1.4.2 Impacts of the Device Multiplier

In this part, the effect that the device multiplier M has on power, phase noise and corresponding FoM is studied. Intuitively, using M devices in parallel takes more area and increases both the inverter stage current and parasitic capacitances by a factor M . Consequently, the oscillation frequency at the first order does not vary, whereas the power increases with M . Moreover, spending more power for the same oscillation frequency decreases the phase noise by the same factor [29, 30, 35–39, 41]. Ultimately, the phase noise FoM thus stays constant. These considerations are confirmed in Fig. 1.6. The parameter M can thus be used to directly *trade phase noise for power and area* at constant frequency and FoM. It can thus be chosen a posteriori and is fixed ($M = 1$) for the remaining part of this work, as we focus on reaching the lowest power or best FoM at the target frequency.

³As an example, the BBCO design of Chapter 2 experiences a routing parasitic capacitance of around 5 fF at the output of each of its stages.

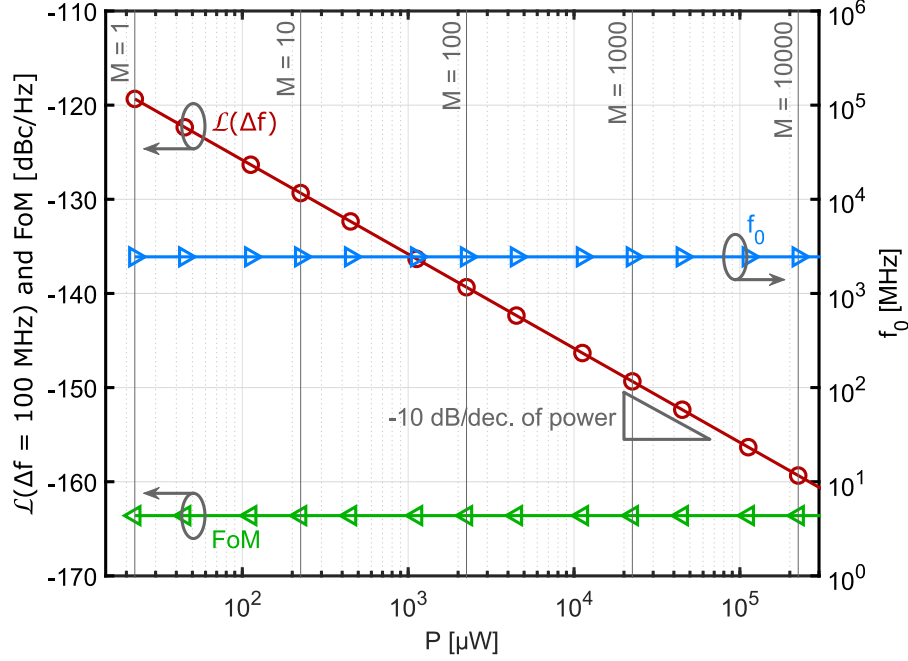


Fig. 1.6 Effect of the device multiplier M on the oscillation frequency, the power consumption, the phase noise level and the corresponding FoM of a 2.45-GHz RO (3 stages, with gate lengths of 283 nm, and supplied at 1.0 V).

1.4.3 Proposed Ring Oscillator Optimization Process

The uncontrolled RO is now left with only three free parameters, namely the supply voltage V_{DD} , the numbers of stages N , and the gate length L . This part optimizes the RO for a target frequency of 2.45 GHz, for different number of stages N and different supply voltage values V_{DD} . For each configuration, the gate length L is adjusted to reach the desired target frequency.

Fig. 1.7(a) shows the transistor gate length value required for 2.45-GHz operation, as a function of the supply voltage and for different number of stages. Each point of the figure can be seen as a different 2.45-GHz RO design. As can be expected, to compensate for the speed decrease when decreasing the supply voltage or increasing the number of stages, the required length decreases as well. We show in Appendix A.1 that the required L is inversely proportional to $\sqrt{N}$ at a fixed supply voltage V_{DD} , and proportional to $(V_{DD} - V_{th,0})/\sqrt{V_{DD}}$ at a fixed N value. The results of Fig. 1.7(a) are in good agreement with these predictions. As can be observed in Fig. 1.7(b), the corresponding oscillation frequency is well (yet coarsely) tuned to the target frequency. The corresponding power consumption is given in Fig. 1.7(c). It increases with both the supply voltage and the number of stages. As shown again in Appendix A.1, the power is proportional to $\sqrt{N}$ at a fixed supply voltage V_{DD} , and to $V_{DD}^{3/2}(V_{DD} - V_{th,0})$ at a fixed number of stages N .

Computing the FoM value for each of these different 2.45-GHz ROs, and relating

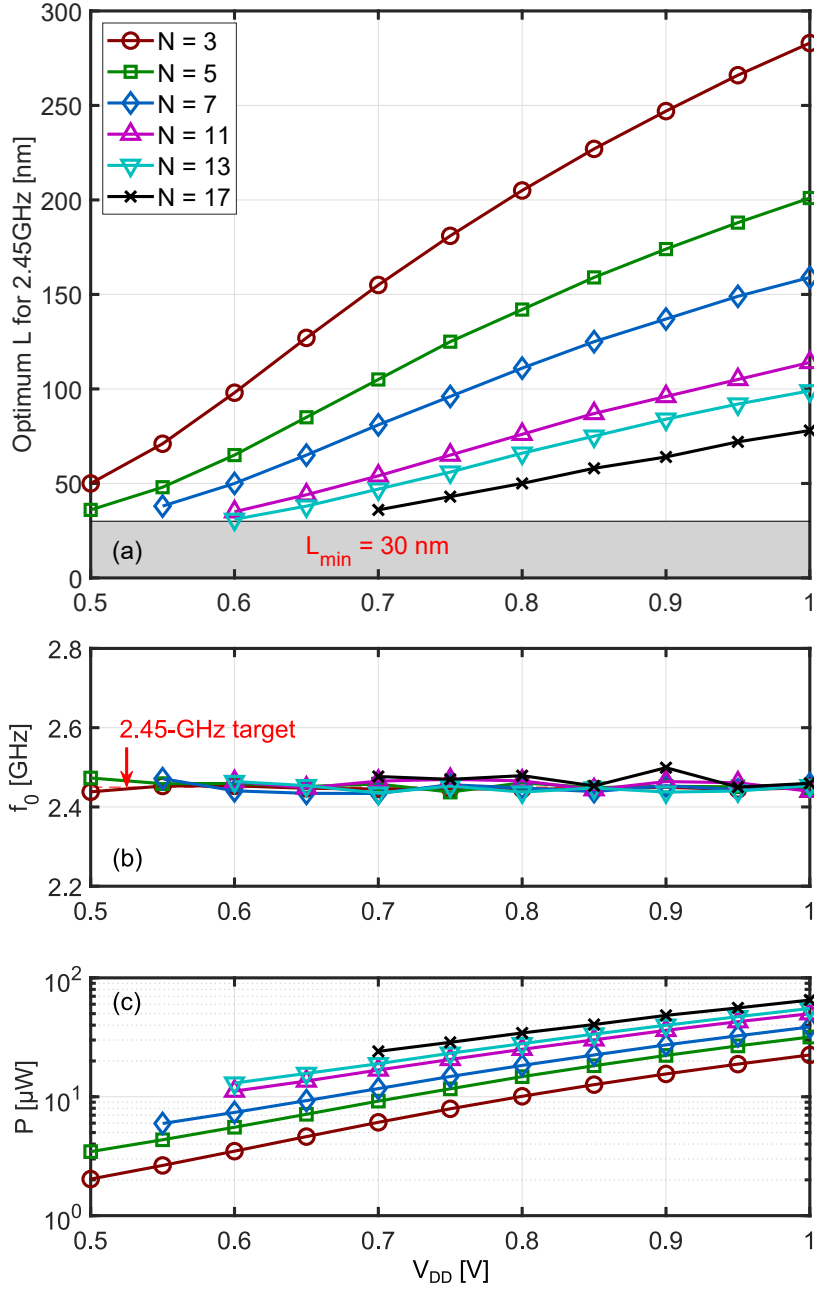


Fig. 1.7 Effect of the number of stages and the supply voltages on: (a) the required gate length for 2.45-GHz operation, (b) the RO oscillation frequency, and (c) the power consumption. Each point represents a different 2.45-GHz RO design, characterized by a given number of stages N , a given supply voltage V_{DD} , and a given transistor gate length L .

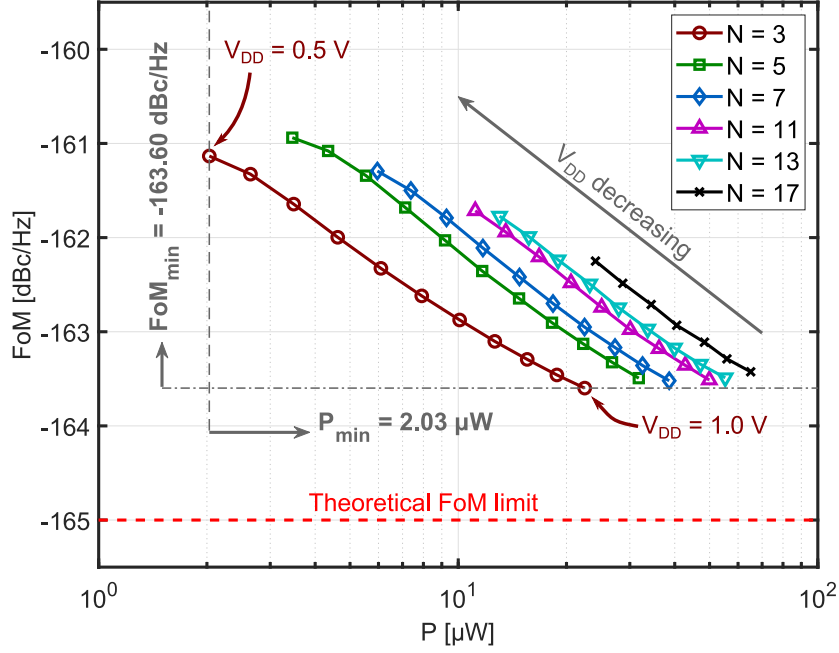


Fig. 1.8 Effect of the number of stages and the supply voltages on the phase noise FoM of 2.45-GHz uncontrolled ROs. Each point represents a different 2.45-GHz RO design, characterized by a given number of stages N , a given supply voltage V_{DD} , and a given transistor gate length L .

it to the power consumption, leads to Fig. 1.8. Each curve corresponds to a different number of stages N , while each point on a curve corresponds to a different supply voltage value V_{DD} . ROs with 3 stages appear to be the best, as they can achieve lower power values at fixed FoM, or better FoM values at fixed power level. Two *fundamental limits* appearing in Fig. 1.8 characterize the uncontrolled RO topology for 2.45 GHz operation: the lowest achievable power $P_{\min}$, and the best achievable power/phase noise compromise $\text{FoM}_{\min}$. As reported, power levels as low as $2.03 \mu\text{W}$ and FoM values as low as -163.6 dBc/Hz can be reached.

It is interesting to see that the analytical FoM expression developed in Appendix A.2 and recalled in (1.26) can also be used to predict the FoM evolution of Fig. 1.8, with respect to N and V_{DD} , respectively. For instance, increasing the number of stages N only shifts the curves towards higher power values, without impacting (at first order) the FoM value. Assuming thermal noise only, the formula in (1.26) confirms this observation as the FoM is in theory independent from N . In addition, if we look for instance at the case $N = 3$ (red curve), moving from 0.5 V to 1.0 V of V_{DD} improves the FoM by 2.5 dB (from -161.1 to -163.6 dBc/Hz). Using (1.26) with thermal noise only and assuming $\gamma = 2/3$ and $V_{th,0} = 0.35 \text{ V}$, the FoM reduction can be estimated as follows and shows a good agreement with the

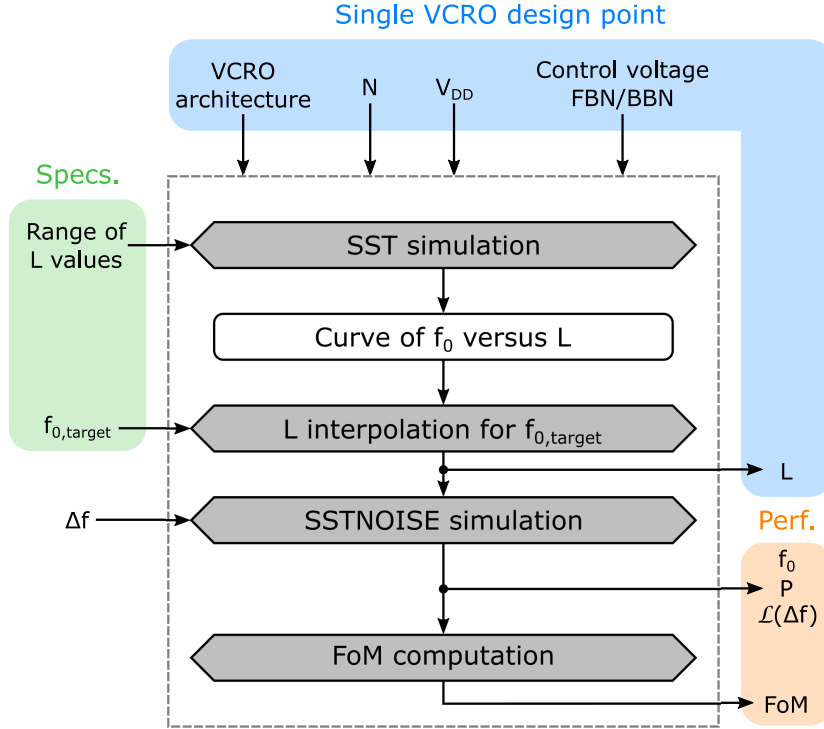


Fig. 1.9 Sizing methodology used for the design of ROs in nominal conditions (TT 25°C). Simulations of SST (steady-state) and SSTNOISE types are performed with Eldo and piloted with Matlab. In practice, parallelism is used to speed up the simulations.

simulation results:

$$\Delta \hat{\text{FoM}} \approx 10 \log_{10} \left(\frac{1 + \frac{2\gamma}{1 - V_{th,0}}}{1 + \frac{\gamma}{0.5 - V_{th,0}}} \right) = -2.51 \text{ dB}. \quad (1.27)$$

The general VCRO sizing methodology used in this section is summarized in Fig. 1.9. For a set of chosen design parameters values (i.e., supply voltage, number of stages), the oscillation frequency is obtained from simulation as a function of gate length values. Then, to reach a specific target frequency, the required length value L is determined by interpolation. This results in a single VCRO design point, properly sized for the target frequency. In order to obtain its performance, a second simulation is performed and extracts the oscillation frequency, the power, and the phase noise value, from which the corresponding FoM can be derived. The next section uses this procedure with CSRO and BBCO topologies in order to compare them fairly in terms of $P_{\min}$ and $\text{FoM}_{\min}$.

1.5 Current-Starving Versus Back-Bias Control

Compared to an uncontrolled RO, the CSRO and BBCO architectures feature an additional degree of freedom: their control voltage. This tuning knob allows to stay functional on a broader range of operating conditions, thanks to a fine adjustment of the frequency. In this work, we define the *functionality of an RO* as its ability to correctly generate the desired target frequency. This section compares the design of CSROs and BBCOs, taking into account the effect that *process, voltage, and temperature* (PVT) variations have on their functionality. Slow NMOS/slow PMOS (SS) and fast NMOS/fast PMOS (FF) are considered instead of typical NMOS/typical PMOS (TT) process, with $\pm 5\%$ supply voltage variation, and temperatures ranging from 0 to $+55^\circ\text{C}$. A brief comparison of the transfer function of CSROs and BBCOs is provided in Section 1.5.1. The effects of PVT variations on the VCROs functionality are then studied in Section 1.5.2. A comparison of their corresponding $P_{\min}$ and $\text{FoM}_{\min}$ follows and is carried out at 2.45 GHz in Section 1.5.3, before extending the methodology to 300 MHz, 868 MHz, and 5.18 GHz in Section 1.5.4. Finally, Section 1.5.5 discusses the impacts of higher temperatures on the VCRO PVT robustness.

1.5.1 VCROs Transfer Functions: Gain, Range, and Linearity

The VCROs studied in this work differ by the type of control they use. As described in Section 1.3, CSROs are controlled by the front-gate voltage FBN , while BBCOs are controlled by the back-gate voltage BBN . Their corresponding transfer functions, i.e., the oscillation frequency versus the control voltage, thus possess significant differences. Intuitively, the tuning of the CSROs frequency involves the gate-to-source transconductance g_m , while for BBCOs it involves the body-to-source transconductance g_{mb} . The link between these two quantities is γ_b , the body factor of (1.25) whose value is small and lies in the 70-to-85 mV/V range in 22/28-nm FDSOI technology [14, 16, 18]:

$$g_{mb} = \gamma_b g_m. \quad (1.28)$$

We can thus expect a lower *frequency gain* for BBCOs. Figs. 1.10 and 1.11 respectively depict the transfer function of a CSRO and a BBCO, both oscillating at 2.45 GHz. They confirm the aforementioned expectation. Indeed, CSROs can easily achieve frequency gain values of 8 GHz/V while the BBCOs reach lower gains of around 400 MHz/V. The analytical developments of Appendix A.3 demonstrate that the BBCO gain is indeed at least $1/\gamma_b \approx 13\times$ lower than the CSRO counterpart. As a consequence, BBCOs have also a lower *frequency range* than CSROs, despite the larger voltage range of BBN (limited to $+3$ V) compared to FBN (limited to V_{DD}).

Another observation that can be made from Figs. 1.10 and 1.11 concerns the

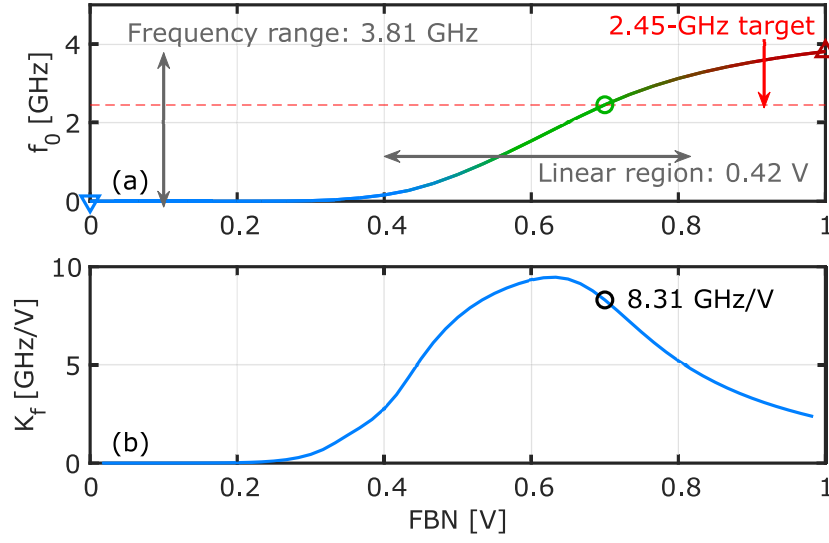


Fig. 1.10 Characteristics of a 2.45-GHz 3-stage CSRO with a nominal control voltage of $FBN = 0.7$ V and supplied at 1.0 V: (a) transfer function and (b) frequency gain.

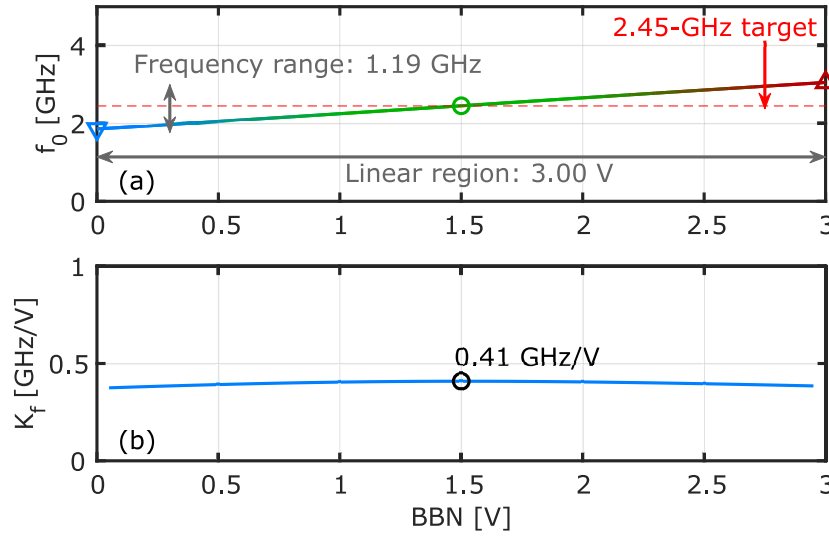


Fig. 1.11 Characteristics of a 2.45-GHz 3-stage BBCO with nominal control voltage of $BBN = 1.5$ V and supplied at 1.0 V: (a) transfer function and (b) frequency gain.

linearity of the VCRO transfer functions. Compared to BBCOs, the CSROs exhibit a highly non linear transfer function. Appendix A.3 again confirms this observation using a Taylor series expansion of the oscillation frequency formula. It is demonstrated that the first non-linear term is $1/\gamma_b^2 \approx 169\times$ lower for BBCOs with respect to CSROs.

Both the frequency gain and the linearity are important points to consider for designers. For instance, the linearity in the transfer function is important for

time-based ADCs relying on VCROs [CP2, 18], while a high and stable gain is necessary when implementing PLLs.

1.5.2 Impacts of PVT Variations on the VCROs Frequency Range

The choice of the nominal control voltage value is important in the design of VCROs, as it impacts both the oscillator frequency range and its PVT compensation capability.

Fig. 1.12 shows the oscillation frequency of CSROs [Fig. 1.12(a)] and BBCOs [Fig. 1.12(b)] as a function of their nominal control voltage. All these oscillators feature 3 stages and are sized for 2.45-GHz operation in nominal conditions (TT 25°C) and at 1.0 V supply voltage following the procedure of Fig. 1.9. Each point on the x-axis thus corresponds to a different oscillator design with a particular control voltage and a particular gate length value. As can be seen in Fig. 1.12, each of these oscillators has a 2.45-GHz nominal frequency (green circles) when operated at the nominal control voltage for which they have been designed for. Increasing (resp. decreasing) the control voltage allows to speed up (resp. slow down) the oscillators. The spread between maximal (red triangles, obtained at maximal control voltage) and minimal frequency (blue triangles, corresponding to minimal control voltage) determines the VCROs frequency range. As discussed in Section 1.5.1, the CSRO topology achieves a higher frequency range thanks to a higher frequency gain with respect to its BBCO counterpart.

With variations of the PVT conditions, the speed of the VCROs is changed. As can be seen in Fig. 1.13, the nominal frequency limits (dashed lines) of the VCROs are shifted upwards or downwards, depending on the PVT conditions. This impacts the VCROs functionality, as illustrated with the gray shaded areas. Indeed, an oscillator designed with a too high nominal control voltage might not be able to compensate the frequency decrease resulting from slow operating conditions (SS, $-5\% V_{DD}$). Similarly, a VCRO which has a too low nominal control voltage might not be able to compensate fast operating conditions (FF, $+5\% V_{DD}$). The PVT variations forces the use of control voltage values closer to mid-range and limits the range of possible nominal control voltage values. It is important to notice also that, due to *temperature effect inversion* [46–48], the effect of temperature is not the same at high or low supply voltage and depends also on the VCRO topology (due to transistor stacking). That is why we consider four extreme corners (instead of two). For information, in the example shown in Fig. 1.13 for 1-V supply voltage, the two limiting PVT corners are FF, $+5\% V_{DD}$, 0°C (in dark blue) and SS, $-5\% V_{DD}$, $+55^\circ\text{C}$ (in dark red).

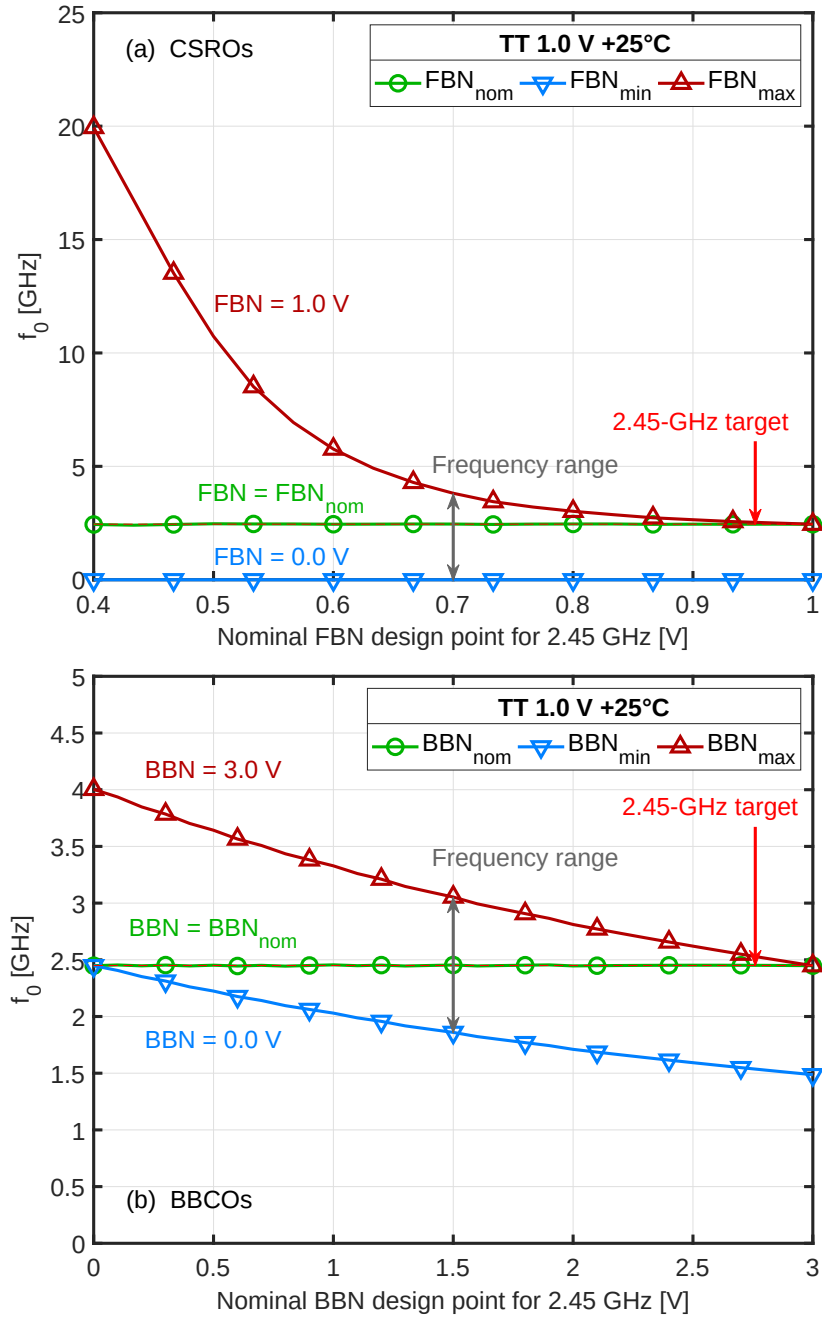


Fig. 1.12 Frequency range comparison of 3-stage CSROs (a) and BBCOs (b) in typical conditions, as a function of their nominal control voltage. All these VCROs are nominally designed for 2.45 GHz at 1.0 V supply voltage. Each point on the x-axis thus corresponds to a different VCRO design with particular control voltage and gate length values.

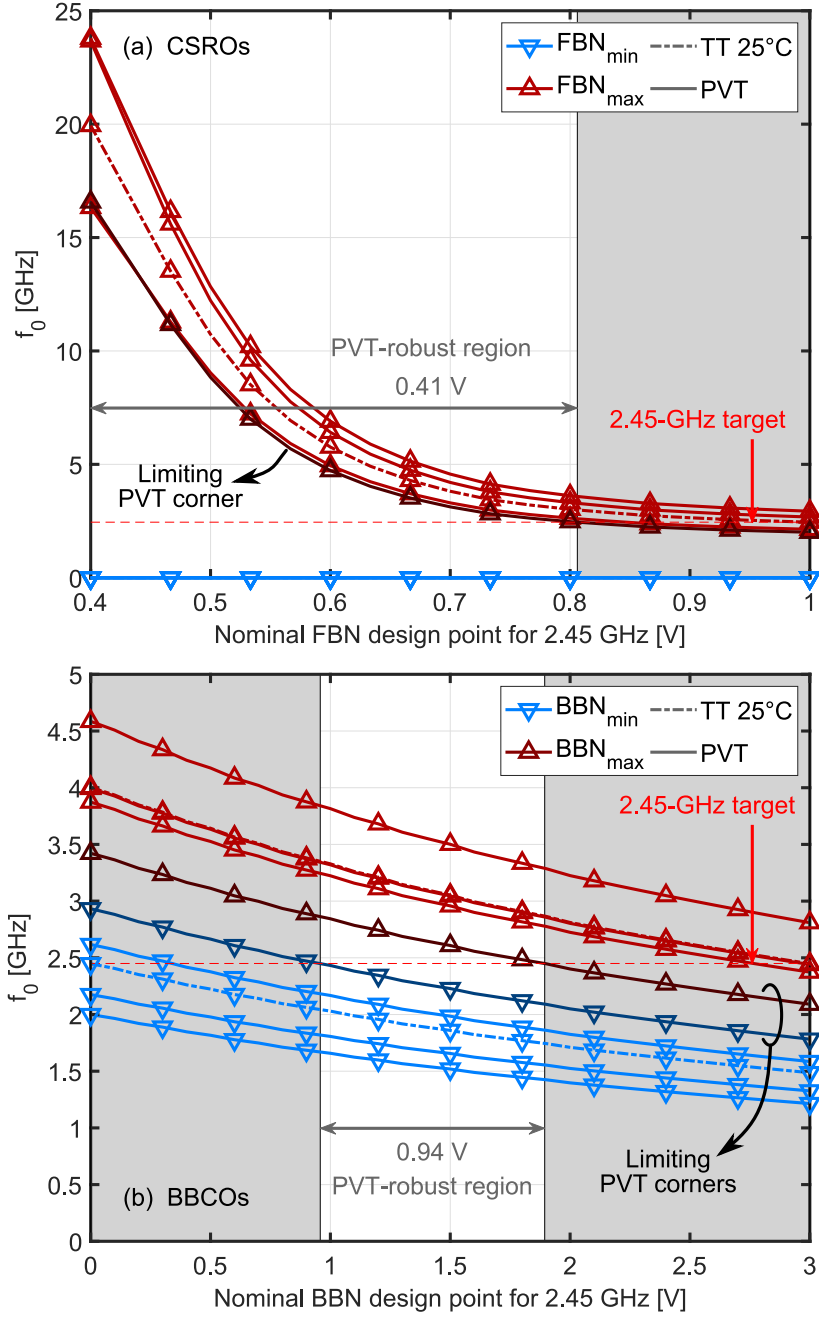


Fig. 1.13 Frequency range comparison of 3-stage CSROs (a) and BBCOs (b) in PVT corners as a function of the nominal control voltage. All these VCROs are nominally designed for 2.45 GHz at 1.0 V supply voltage. Each point on the x-axis thus corresponds to a different VCRO design with particular control voltage and gate length values. The PVT variations reduce the range of available nominal control voltage values.

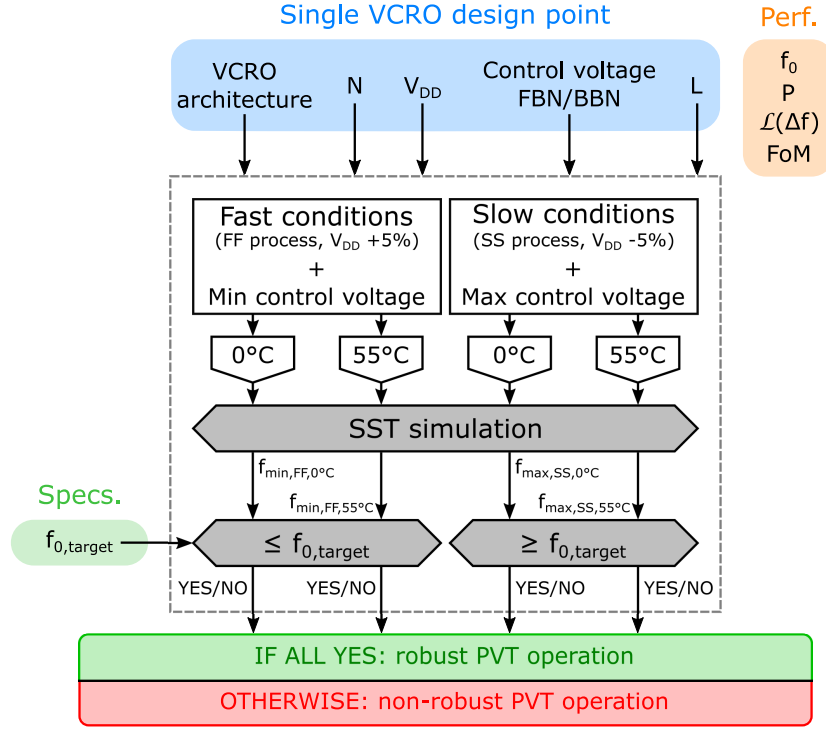


Fig. 1.14 Methodology used to verify the design of ROs under extreme PVT variations. Simulations of SST (steady-state) type are performed with Eldo and piloted with Matlab. In practice, parallelism is used to speed up the simulations.

For the remaining part of this chapter, to verify the functionality of a given VCRO design under extreme PVT variations, the methodology of Fig. 1.14 is followed. The design to verify is put under fast conditions (FF, +5% V_{DD}) using minimum control voltage. The corresponding oscillation frequencies are obtained from simulations at two extreme temperatures (0 and +55°C). The same procedure is applied with slow conditions (SS, -5% V_{DD}) and maximum control voltage. The VCRO is considered to have robust PVT operation if its ability to generate the target frequency is preserved under all four aforementioned PVT conditions.

Table 1.4 Range of design parameter values used for the comparison of fundamental limits of CSROs and BBCOs.

Parameters	Units	Min	Max	Resolution
V_{DD}	V	0.3	1.0	0.05
N	—	3	17	prime numbers
L	nm	30	500	1
FBN	V	0	V_{DD}	$V_{DD}/30$
BBN	V	0	3	0.1

1.5.3 Comparison of CSROs and BBCOs at 2.45 GHz

In this part, using the sizing methodology of Fig. 1.9, several CSROs and BBCOs are designed for 2.45 GHz, at several supply voltage values and with different number of stages. For each of these design points, the oscillator functionality is verified under PVT variations with the procedure of Fig. 1.14. Each design parameter is limited to a fixed range of values, and swept with a fixed resolution, as shown in Table 1.4.

Fig. 1.15 compares the obtained phase noise FoM and power consumption. Performance in nominal (light crosses) and after verification in extreme conditions (bold circles) are shown, for both the CSRO [Fig. 1.15(a)] and BBCO topologies [Fig. 1.15(b)]. The two fundamental limits $P_{\min}$ and $\text{FoM}_{\min}$ are highlighted, for both nominal and non-nominal cases. As can be observed, ensuring functionality under extreme PVT conditions tends to degrade these limits. This is linked to the discussion of Section 1.5.2 that showed that PVT variations forces the use of mid-range nominal control values.

Several conclusions can be drawn from this comparison made at 2.45 GHz. In terms of lowest achievable power, $P_{\min}$, BBCOs can go as low as 0.66 μW , while CSROs are limited to 2.19 μW (1.81 μW if considering nominal conditions only). In other words, BBCOs outperform CSROs by a factor $3.31\times$. This is explained by the fact that BBCO can operate at a lower supply voltage (down to 0.3 V), as they avoid the stacking of transistors and benefit from a threshold voltage reduction through their back-bias control. BBCOs also benefit from the lower number of devices they are made of, which limits the number of noise sources and parasitics. In terms of best achievable power/phase noise trade-off, $\text{FoM}_{\min}$, both architectures are very close (within 1 dB), with values around -164 dBc/Hz. Compared to its CSRO counterpart, the BBCO topology exhibits a lower vertical spread in its FoM levels, which seem thus less sensitive to the choice of nominal control voltage. This can be explained by the lower frequency gain of BBCOs, as previously discussed in Section 1.5.1 and shown in Appendix A.3. For both architectures, the fundamental limits $P_{\min}$ and $\text{FoM}_{\min}$ are respectively achieved with the lowest number of stages ($N = 3$) and at the highest supply voltage ($V_{DD} = 1.0 \text{ V}$).

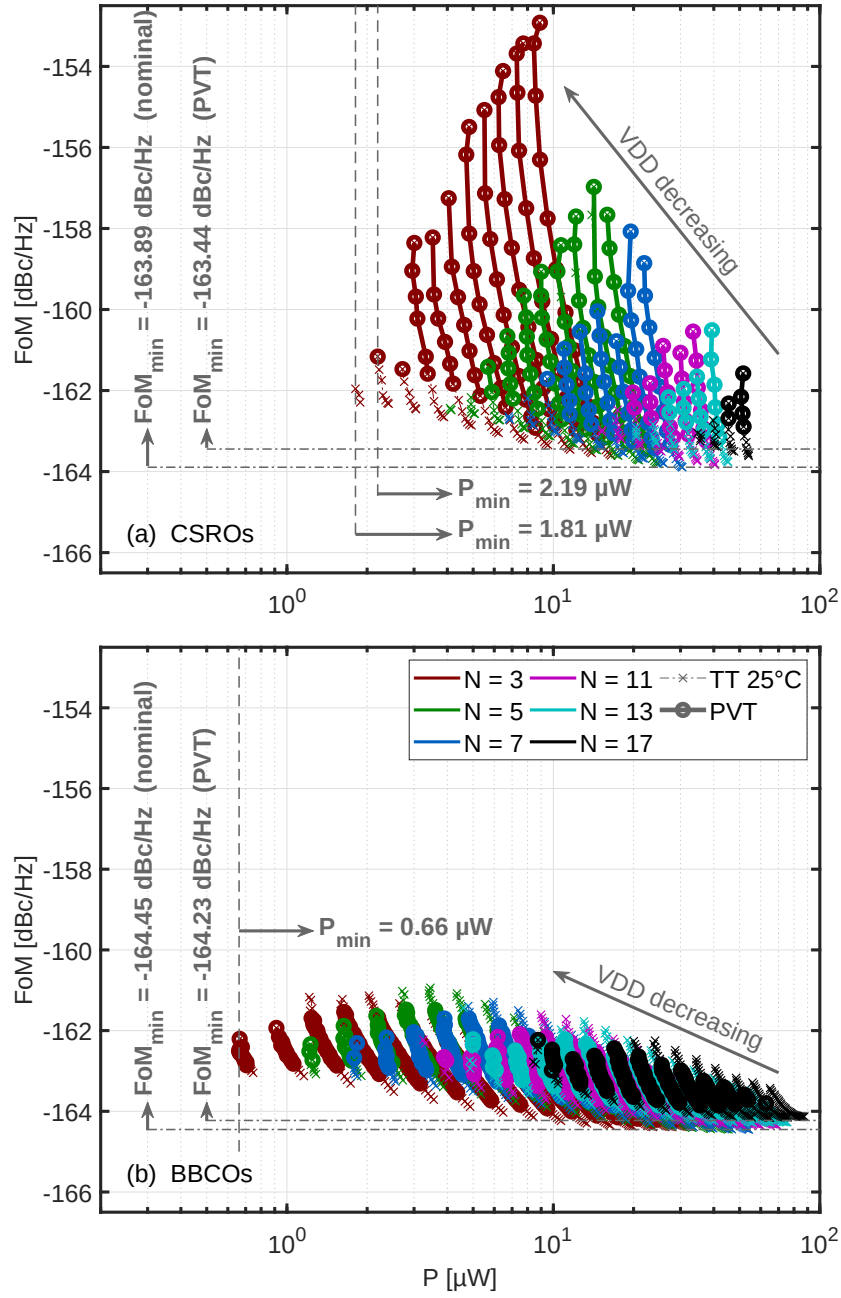


Fig. 1.15 Comparison of 2.45-GHz CSROs (a) and BBCOs (b) in terms of phase noise FoM and power consumption, in nominal conditions and under PVT variations. All these oscillators differ by the number of stages N (different curve colors), the nominal supply voltage V_{DD} (different curves), and the nominal control voltage FBN/BBN (different points of a curve). Corresponding oscillation frequency is tuned to 2.45 GHz using the transistor gate length L .

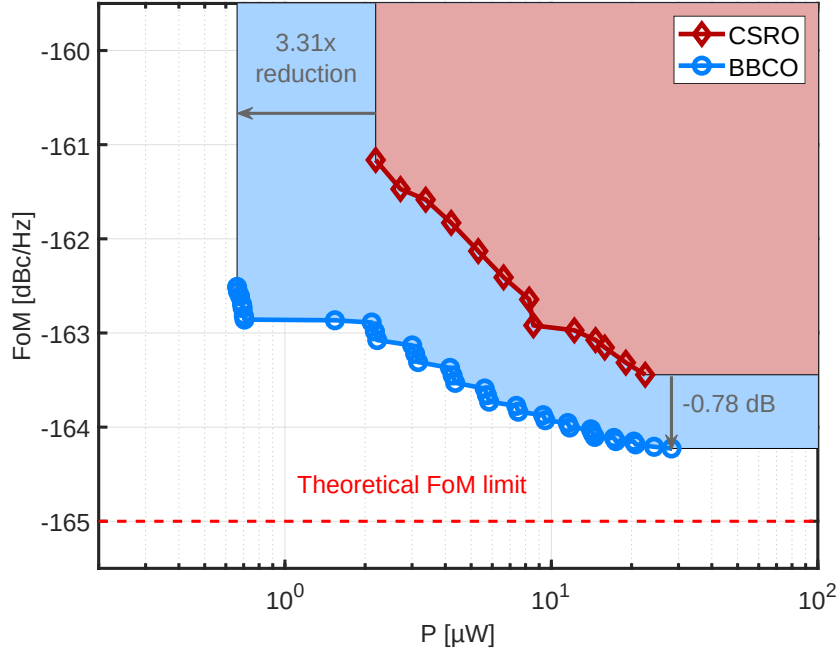


Fig. 1.16 Comparison of FoM Pareto-optimal fronts as a function of the power consumption for 2.45-GHz CSROs and BBCOs whose functionality is verified under PVT variations.

An additional way to compare both architectures is illustrated in Fig. 1.16, where only the optimum VCROs with robust PVT operation are kept to obtain Pareto-optimal fronts. This figure clearly shows the advantages of the BBCO topology over its CSRO counterpart, as at a fixed power level it achieves better FoM values, and at a fixed FoM level it consumes less power.

1.5.4 Extension of the Comparison to Other Target Frequencies

Table 1.5 summarizes the results obtained at 2.45 GHz, and extends them to 300-MHz, 868-MHz, and 5.18-GHz target frequencies. The CSRO and BBCO topologies are compared in terms of the values of $P_{\min}$ and $\text{FoM}_{\min}$ they can achieve, and their corresponding design parameters are also provided. Fig. 1.17 graphically shows the evolution of the fundamental limits with respect to frequency.

The conclusions previously drawn at 2.45 GHz hold both at higher and lower frequencies. BBCOs reach significantly lower $P_{\min}$ values. The power reductions range from a factor $1.69\times$ at 300 MHz to a factor $4.63\times$ at 5.18 GHz with respect to CSRO counterparts [Fig. 1.17(a)]. In addition, BBCOs achieve slightly better $\text{FoM}_{\min}$ values than CSROs (still within 1 dB) [Fig. 1.17(b)]. Back biasing is thus an efficient frequency tuning knob and is well suited for ULP/ULV applications.

Table 1.5 Comparison of fundamental limits for CSROs and BBCOs at four different target oscillation frequencies and validated under extreme PVT variations (FF/SS process, $\pm 5\%$ voltage variation, and $0^\circ\text{C}/+55^\circ\text{C}$ temperature). Corresponding design parameters (N , V_{DD} , FBN/BBN , L) are also provided, together with the associated phase noise level $\mathcal{L}(\Delta f)$ obtained at an offset frequency Δf of 100 MHz.

f_0	Metrics	Units	$P_{\min}$		$FoM_{\min}$	
			CSRO	BBCO	CSRO	BBCO
300 MHz	P	μW	0.14	0.08	8.86	14.24
	FoM	dBc/Hz	-160.84	-160.98	-163.15	-163.84
	$\mathcal{L}(100 \text{ MHz})$	dBc/Hz	-112.60	-110.63	-133.06	-135.83
	N	—	3	3	11	11
	V_{DD}	V	0.40	0.30	0.95	0.90
	FBN	V	0.29	-	0.79	-
	BBN	V	-	1.00	-	1.90
	L	nm	32	55	261	493
868 MHz	P	μW	0.63	0.24	21.65	34.69
	FoM	dBc/Hz	-160.80	-161.86	-163.69	-164.45
	$\mathcal{L}(100 \text{ MHz})$	dBc/Hz	-110.03	-106.89	-128.26	-131.10
	N	—	3	3	13	11
	V_{DD}	V	0.50	0.30	1.00	1.00
	FBN	V	0.38	-	0.80	-
	BBN	V	-	1.30	-	1.80
	L	nm	38	45	122	287
2.45 GHz	P	μW	2.19	0.66	22.51	28.23
	FoM	dBc/Hz	-161.16	-162.51	-163.44	-164.23
	$\mathcal{L}(100 \text{ MHz})$	dBc/Hz	-106.73	-103.06	-119.21	-120.94
	N	—	3	3	5	3
	V_{DD}	V	0.55	0.30	1.00	1.00
	FBN	V	0.42	-	0.80	-
	BBN	V	-	1.80	-	1.80
	L	nm	31	39	116	344
5.18 GHz	P	μW	6.52	1.41	35.93	59.15
	FoM	dBc/Hz	-161.18	-162.41	-162.84	-163.69
	$\mathcal{L}(100 \text{ MHz})$	dBc/Hz	-105.06	-99.66	-114.15	-117.09
	N	—	3	3	5	5
	V_{DD}	V	0.65	0.30	1.00	1.00
	FBN	V	0.50	-	0.77	-
	BBN	V	-	2.00	-	1.80
	L	nm	31	31	60	147

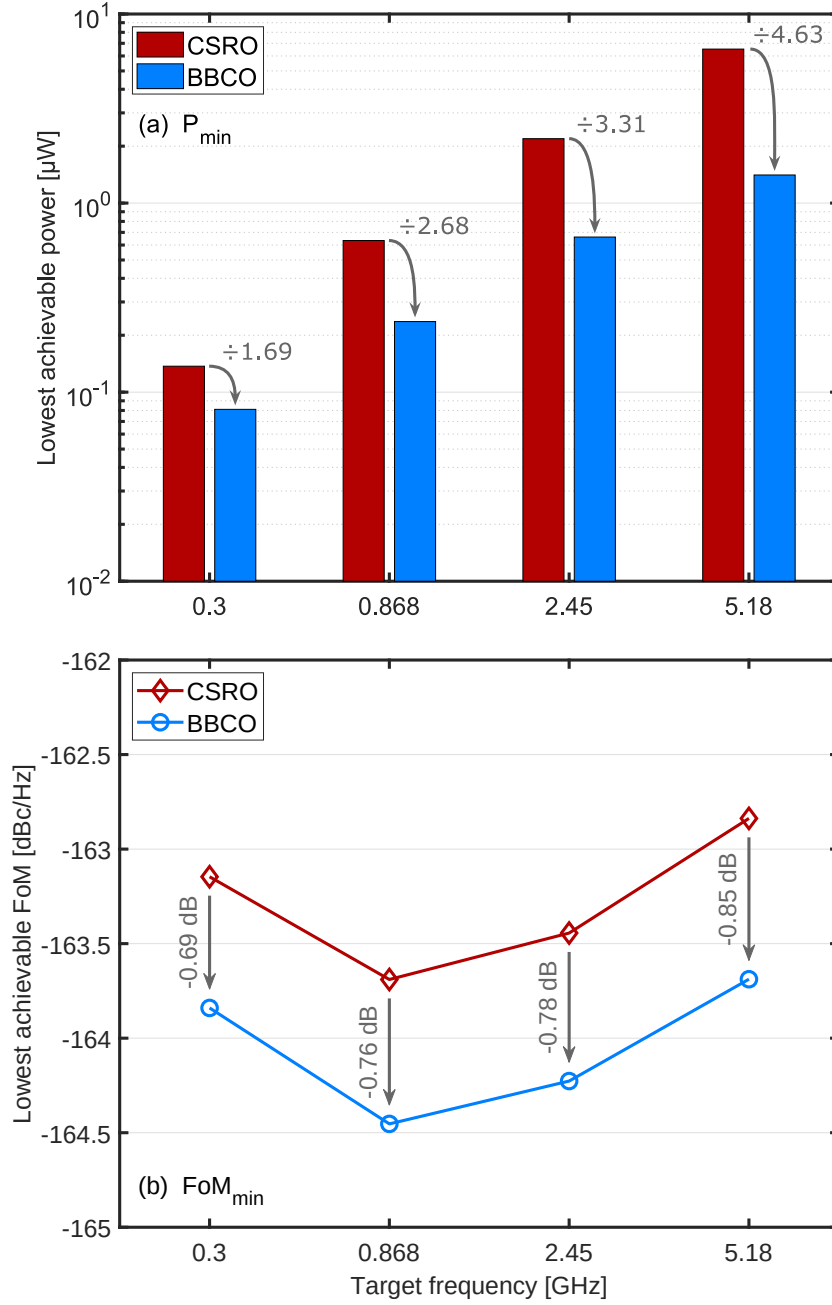


Fig. 1.17 Comparison of CSROs and BBCOs in terms of (a) $P_{\min}$ and (b) $\text{FoM}_{\min}$ fundamental limits, while ensuring PVT robustness.

1.5.5 PVT Robustness at Higher Temperatures

Before concluding this chapter, we broaden the discussion by briefly analyzing the robustness of CSROs and BBCOs to PVT variations when considering a higher temperature, e.g., at $+85^\circ\text{C}$. We can identify three different impacts coming from a temperature increase.

A first impact concerns the oscillation frequency of the VCROs. Linked to the temperature effect inversion [46–48], a higher temperature will slow down or speed up the considered VCRO, depending on its supply voltage value and on its topology. Section 1.5.2 already discussed this matter. Secondly, a higher temperature leads to a higher thermal noise generation, coming from a higher thermal agitation of the electrons. Consequently, the corresponding phase noise spectrum increases [see (A.13) in Appendix A] and ultimately degrades the phase noise FoM [as captured in (1.26)]. Additionally, the FoM is also degraded by the leakage power which rises with temperature. As a reminder, the FoM formula in (1.26) does not capture that effect as it only assumes a purely dynamic power. Depending on the leakage contribution to the total VCRO power, corresponding impacts on the phase noise FoM can be more or less significant.

We can now wonder if these observations impact the VCROs comparison results of last sections, in terms of PVT compensation capability and fundamental limits, when considering a maximal temperature of $+85^\circ\text{C}$ instead of $+55^\circ\text{C}$. For this purpose, the comparison results of Fig. 1.15 obtained at 2.45 GHz are drawn in a different manner in Fig. 1.18. The green contour contains all the points functional in nominal conditions ($\text{TT} + 25^\circ\text{C}$). Among these points, a subset of them remain functional at $+55^\circ\text{C}$, as shown in orange. Among the latter, another subset of points stay functional also at $+85^\circ\text{C}$, as shown in red. For both the $+55$ and $+85^\circ\text{C}$ cases, the VCRO PVT robustness is verified with the procedure of Fig. 1.14 in fast (FF, $+5\% V_{DD}$) and slow conditions (SS, $-5\% V_{DD}$).

At 2.45 GHz, the results of Fig. 1.18 that most of the VCROs which are robust at $+55^\circ\text{C}$ (in orange) are also robust at $+85^\circ\text{C}$ (in red). Increasing the temperature does not impact the minimal achievable power $P_{\min}$ (this VCRO fundamental limit is degraded by low temperatures), for both the CSRO and BBCO topologies. In terms of the best achievable power/phase noise trade-off, the $\text{FoM}_{\min}$ degradation is limited when considering $+85^\circ\text{C}$ instead of $+55^\circ\text{C}$ for the analysis of the PVT robustness. An increase of 0.02 dB and 0.1 dB in $\text{FoM}_{\min}$ is observed for CSROs and BBCOs, respectively, when considering $+85$ instead of $+55^\circ\text{C}$. The VCRO $\text{FoM}_{\min}$ values seem not impacted by the leakage increase with temperature. In fact, corresponding VCRO designs operate at maximal supply voltage, as shown in the $\text{FoM}_{\min}$ column in Table 1.5, and their leakage contribution to their total power is negligible (less than 0.02%).

Similar observations can be made when considering target frequencies of 300 MHz, 868 MHz, or 5.18 GHz. Indeed, for these frequencies as well, an increase of

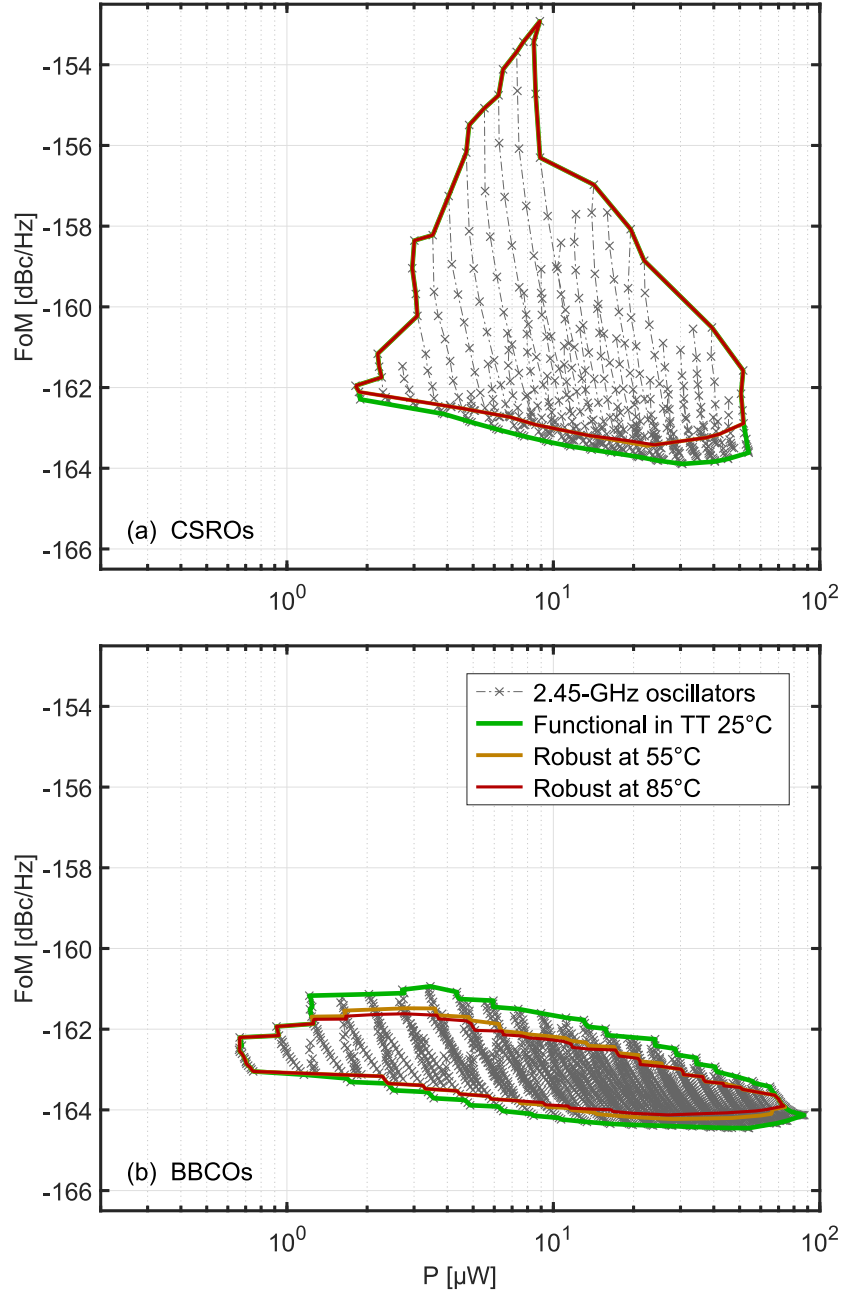


Fig. 1.18 Comparison of 2.45-GHz CSROs (a) and BBCOs (b) in terms of phase noise FoM and power consumption, illustrating the impacts of considering higher temperatures when evaluating the VCRO PVT robustness. Each point corresponds to a given oscillator design, with a certain number of stages N , a certain nominal supply voltage V_{DD} , a certain nominal control voltage FBN/BBN , and a certain gate-length value L .

temperature from $+55$ to $+85^\circ\text{C}$ does not affect $P_{\min}$. It only impacts $\text{FoM}_{\min}$ but with limited degradations of less than 0.15 dB and 0.18 dB for CSROs and BBCOs, respectively. Corresponding VCRO designs exhibit a negligible leakage contribution of less than 0.09% with respect to their total power consumption.

The conclusions of last section thus hold: for the frequency range considered in this chapter, BBCOs stay better than CSROs in terms of $P_{\min}$ and $\text{FoM}_{\min}$.

1.6 Conclusion

In this first chapter, we used extensive simulation results supported by compact analytical models to analyze and compare two types of VCROs: conventional CSROs and FDSOI-enabled BBCOs. At fixed oscillation frequency, oscillators can be characterized by two fundamental limits: the minimum achievable power $P_{\min}$ and the best power/phase noise trade-off $\text{FoM}_{\min}$ they can intrinsically achieve. In this work, we objectively characterized these fundamental limits for CSROs and BBCOs built in 28-nm FDSOI technology and oscillating at four different target frequencies: 300 MHz, 868 MHz, 2.45 GHz, and 5.18 GHz. The chosen frequency values are representative of frequency synthesis for WiFi/Bluetooth/LPWAN wireless communications and of clock generation for smartphone/IoT processors. The impact of PVT variations on the VCROs functionality is also taken into account.

Compared to the conventional current starving technique, a VCRO frequency tuning based on back biasing offers many advantages: in 28-nm FDSOI technology, BBCOs reach $1.69\times$ to $4.63\times$ lower $P_{\min}$ than their CSRO counterparts and offer slightly better $\text{FoM}_{\min}$ values. These improvements are related to the low degree of transistor stacking, yielding a lower device count and therefore reduced associated noise/parasitics, as well as to the threshold voltage reduction induced by forward back biasing. These features help the BBCO topology operate at lower supply voltages, and thus lower power. Therefore, back-bias control appears to be an excellent tuning knob for VCROs targeting ULP/ULV applications, such as wake-up radios [49], for instance.

Despite the discussed advantages, the use of back biasing in VCROs also raises some design challenges. For instance, if a symmetrical biasing is used as assumed here⁴, BBCOs need a negative control voltage BBP , whose range can theoretically go down to -3 V. It is usually generated on-chip with charge pumps as in [20]. Another possibility is to generate a fixed negative DC voltage to supply a BBP generator, as done in [34]. Nevertheless, related power overheads and impacts on the phase noise performance of the BBCOs should be carefully evaluated, in comparison to current mirrors typically needed for CSROs. The lower frequency gain value obtained with BBCOs is also an important design metric to take into

⁴Let us mention that asymmetrical control strategies could be chosen, for both current-starved and back-bias techniques. They may lead to different benefits and disadvantages at the system level, that must be properly assessed in future designs and in future works.

account, for instance in PLL design.

The following chapters illustrate the use of BBCOs and address the previously discussed challenges with their implementation on silicon in chip prototypes and targeting applications linked to clock generation and frequency synthesis.

Leveraging Forward Back Biasing in Phase-Locked Loops

Contents

2.1	Introduction	52
2.2	Design Considerations Linked to PLLs	52
2.3	Clock Recovery for a UWB Transceiver	58
2.4	Proposed Clock Recovery Unit	61
2.5	Prototyping and Measurement Results	70
2.6	Analysis of the BBCO Results	74
2.7	Conclusion	75

Abstract As learned from Chapter 1, back-bias-controlled oscillators (BBCOs) bring several advantages with respect to conventional current starved ring oscillators (CSROs) but also several design challenges. This second chapter examines the benefits and challenges in the design of BBCO-based phase-locked loops (PLLs) and takes a system-level perspective. We then apply the resulting design considerations by prototyping a 2.5-GHz clock recovery (CR) unit within WiXpress, an efficient 2.5-Gb/s ultra-wideband (UWB) transceiver [JP2]. The proposed circuit fabricated in 28-nm FDSOI targets low-power chip-to-chip communications over short distances. The CR circuit comprises two complementary PLLs, a first one for fast frequency locking and another one for high-bandwidth phase tracking. Forward back biasing (FBB) controls the BBCO frequency to recover a 2.5-GHz clock. This feature reduces the CRs minimum supply voltage and its power consumption while preserving functionality over a wide range of process, voltage, and temperature (PVT) variations, including skewed process corners. The CR occupies a silicon area of 0.043 mm², locks in less than 1.1 μ s, generates an RMS long-term jitter of 6.5 ps, and consumes 1.034 mW while in lock. These performance levels result in an energy value of 0.414 pJ/cycle and a jitter figure of merit (FoM) of -224 dB.

2.1 Introduction

The analysis performed in Chapter 1 teaches us several lessons regarding the design and the use of back-biased-controlled oscillators (BBCOs). Benefiting from the forward back-biasing (FBB) feature offered by FDSOI technology, they exhibit several advantages for ultralow-voltage/ultralow-power (ULV/ULP) designs. However, they give rise to several design challenges as well. This second chapter builds upon the learning outcomes of Chapter 1 and analyzes the use of BBCOs inside *phase-locked loops* (PLLs), which are major building blocks in the context of clock generation and frequency synthesis.

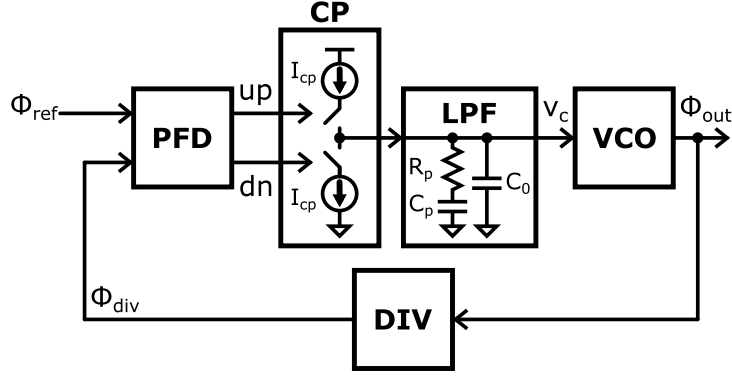
The chapter is structured as follows. Section 2.2 introduces the concept of PLLs and examines the benefits and challenges associated with BBCOs from a system-level perspective. The remaining sections then illustrate the use of BBCOs inside PLLs by presenting a chip prototype manufactured in 28-nm FDSOI technology: a dual-PLL clock recovery (CR) unit embedded in an efficient 2.5-Gb/s ultra-wideband (UWB) radio codenamed WiXpress for chip-to-chip communications over short distances. Section 2.3 explains the applicative context and introduces the proposed UWB transceiver. The next parts of the chapter focus on the CR unit: Section 2.4 details its architecture and its simulation-based design; Section 2.5 then follows with experimental results and a comparison to other works from the literature. Finally, Section 2.6 discusses the results obtained with the CR BBCO in regards with the considerations of Chapter 1. The contents of this chapter are adapted from [JP2].

2.2 Design Considerations Linked to PLLs

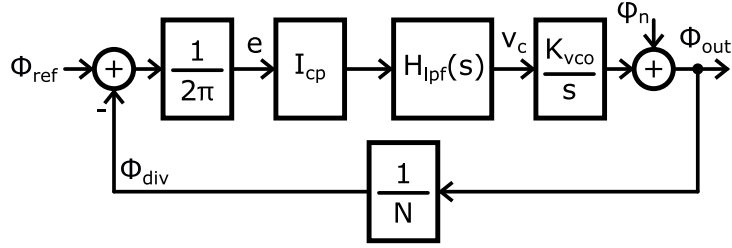
A PLL is a feedback system built around a *voltage-controlled oscillator* (VCO) to align its output clock in frequency and in phase with respect to an input reference clock, as depicted in Fig. 2.1(a). The common Type-II PLL architecture uses a *phase-frequency detector* (PFD) and a charge pump (CP) to convert the phase error into a current, followed by a lead-lag low-pass filter (LPF) to generate the VCO control voltage. A frequency divider (DIV) is inserted in the feedback path when the application requires frequency multiplication between input and output clocks¹.

This section briefly introduces the modeling of conventional PLLs before examining the benefits and challenges associated with the design of PLLs in FDSOI technology. In particular, we investigate the design implications of using a back-bias-controlled oscillator (BBCO) to implement a VCO.

¹Linear voltage-domain feedback systems similarly amplify voltages by placing a resistive divider in the feedback path of an operational amplifier, for instance.



(a) PLL architecture.



(b) Linear PLL model.

Fig. 2.1 Conventional Type-II PLL architecture and corresponding model in the Laplace domain.

2.2.1 Conventional PLL Modeling

Knowing the transfer function of each constitutive block of the PLL, we can construct a linear model of the entire loop in the Laplace domain, as shown in Fig. 2.1(b). Note that the PLL model uses the phase as state variable, which is obtained by integrating the VCO frequency and is function on the VCO control voltage(s). The term I_{cp} denotes the CP current value, N refers to the frequency division factor, K_{vco} is the VCO frequency gain, and φ_n represents the VCO phase noise. The transfer function $H_{lpf}(s)$ of the lead-lag LPF shown in Fig. 2.1(a) is given by:

$$H_{lpf}(s) = \frac{1}{s(C_0 + C_p)} \frac{1 + sR_pC_p}{1 + sR_p\frac{C_0C_p}{C_0 + C_p}} \approx \frac{1 + sR_pC_p}{sC_p}, \quad (2.1)$$

where R_p , C_p , and C_0 are the constitutive resistor and capacitors of the LPF. The components R_p and C_p are responsible for the low-pass behavior of the filter. Capacitor C_0 filters the voltage ripple at the VCO input induced by CP charge injection into the LPF resistor. It is usually sized 5 to 10× smaller than C_p to avoid disturbing the loop stability [50].

From there, neglecting C_0 , the *closed-loop transfer function* of the PLL is obtained

as follows:

$$H_T(s) = \left. \frac{\Phi_{out}}{\Phi_{ref}}(s) \right|_{\varphi_n=0} = N \frac{I_{cp}K_{vco} (1 + s R_p C_p)}{2\pi N C_p s^2 + I_{cp}K_{vco}R_p C_p s + I_{cp}K_{vco}}. \quad (2.2)$$

This equation corresponds to a second-order low-pass transfer function. Two important metrics, the *natural pulsation* ω_n and the *damping factor* ζ , are associated with (2.2) and are related to the PLL stability and speed. They are respectively defined as:

$$\omega_n = \sqrt{\frac{I_{cp}K_{vco}}{2\pi N C_p}}, \quad (2.3)$$

$$\zeta = \frac{R_p}{2} \sqrt{\frac{I_{cp}K_{vco}C_p}{2\pi N}}. \quad (2.4)$$

The term ω_n represents the frequency at which the system naturally tends to oscillate. The damping ratio ζ represents the system ability to prevent or reduce these natural oscillations. It also gives information about the poles location in the complex plane: the system is undamped and purely oscillatory for $\zeta = 0$ as its the two poles lie on the imaginary axis; for $0 < \zeta < 1$, the system is underdamped and has two complex conjugate poles; for $\zeta = 1$, the system is critically damped and has two identical real poles; finally, for $\zeta > 1$, the system is overdamped and has two distinct real poles. Finally, the product $\zeta\omega_n$ is also important as it is directly related to the PLL bandwidth or time constant. As such, it highlights a first important trade-off between the PLL settling time on one hand and the suppression of high-frequency components on the VCO control voltage on the other hand [50].

The closed-loop transfer function H_T in (2.2) is also named the *jitter transfer function* [29]. Indeed, any noise on the input reference clock transfers to the output after being shaped by H_T . Similarly, the *jitter generation function* H_G links the output-referred VCO noise and the PLL output [29] and equals:

$$H_G(s) = \left. \frac{\Phi_{out}}{\varphi_n}(s) \right|_{\Phi_{ref}=0} = \frac{2\pi N C_p s^2}{2\pi N C_p s^2 + I_{cp}K_{vco}R_p C_p s + I_{cp}K_{vco}}. \quad (2.5)$$

Unlike the jitter transfer function, the jitter generation function behaves like a high-pass filter. However, these two functions share the same corner frequency. Consequently, PLLs thus experience a second important trade-off between input-referred noise and VCO-referred noise [29,45]. Indeed, the lower the PLL bandwidth, the lower the jitter transfer from input to output, but the higher the jitter generation from the VCO to the PLL output. The following equation highlights this trade-off by expressing the full-loop phase noise $S_{\Phi_{out}}$ at the PLL output as a linear combination of the input-referred noise power spectral density (PSD) $S_{\Phi_{ref}}$ and

the VCO-referred noise PSD S_{φ_n} , respectively shaped by H_T and H_G [29]:

$$S_{\Phi_{out}}(f) = |H_T(f)|^2 S_{\Phi_{ref}}(f) + |H_G(f)|^2 S_{\varphi_n}(f). \quad (2.6)$$

2.2.2 BBCO-Based PLLs: Design Implications

This section examines the benefits and challenges associated to the design of BBCO-based PLLs in FDSOI technology.

Benefits

Compared to CSROs, BBCOs can operate at a lower supply voltage, thanks to a lower degree of transistors stacking and the FBB feature enabled by FDSOI technology. This is an interesting feature because in terms of power, the lower supply voltage and the application of FBB do not only impact the BBCO itself, at the block level, but can also benefit other parts of the PLL, at the system level.

Also, although being naturally able to compensate for process, voltage, and temperature (PVT) variations, a conventional PLL is limited to the compensation of symmetric process corners as it can not fully correct the N/PMOS imbalance² arising from asymmetric process ones. Symmetric process corners include typical NMOS/typical PMOS (TT), fast NMOS/fast PMOS (FF), and slow NMOS/slow PMOS (SS), while asymmetric ones designate fast NMOS/slow PMOS (FS) and slow NMOS/fast PMOS (SF). A BBCO-based PLL finds an advantage there: with an asymmetric FBB generation and the sensing of the N/PMOS imbalance, it extends the PLL PVT compensation capability to the correction of the NMOS/PMOS process imbalance due to asymmetric process corners.

Chapter 1 also showcases that BBCOs are more linear than their CSRO counterparts. An enhanced VCO linearity improves the matching between the PLL real dynamics and its linearized model. A linear transfer function also implies a constant frequency gain and results in the same jitter generation at all frequencies within the VCO frequency range [51].

Finally, as demonstrated in Chapter 1 as well, a BBCO can intrinsically reach a better power/noise trade-off, which can ultimately benefit the entire PLL as well.

Challenges

BBCOs have a lower frequency gain compared to their CSRO counterparts. In order to achieve similar PLL settling time and stability, this reduced frequency gain

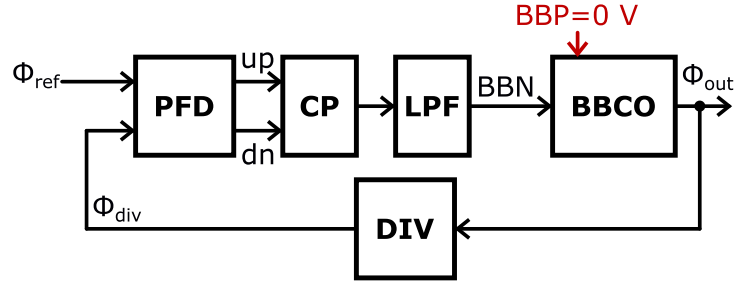
²As an example, the N/PMOS process imbalance increases the mismatch between rising and falling transition times, resulting in pulse width degradations. Other detrimental impacts are briefly discussed in Section 3.2.

must be compensated for by increasing the CP current [see Eqs. (2.3) and (2.4)], for instance. To withstand this higher current, corresponding supply rails must be sized with attention to avoid internal voltage drops. Moreover, the current increase may also indirectly result in excessive power consumption at the PLL level, which needs a careful assessment.

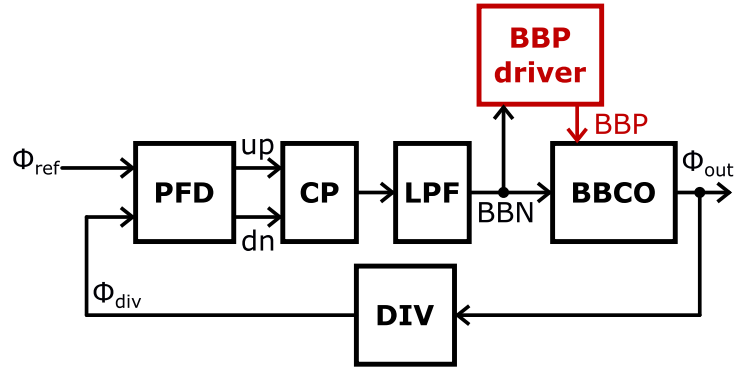
In addition, using a BBCO implies that the back-bias voltages now become the PLL control voltages, namely BBN (resp. BBP) for NMOS (resp. PMOS) transistors. As a reminder, with low- V_{th} (LVT) devices benefiting from FBB, BBN is positive and ranges from 0 to +3 V while BBP is negative and ranges from 0 to -3 V. The generation of BBP thus appears challenging. We identify three different possible design choices, as illustrated in Fig. 2.2:

1. **No BBP generation:** A first possibility is to tie BBP to 0 V and thus avoid its generation [Fig. 2.2(a)] as explored in [52]. The PLL uses a unique control voltage BBN, resulting in a low design complexity, and its implementation is thus very close to conventional PLLs based on CSROs. However, the PLL does not fully exploit the PVT compensation capability offered by FBB, as it cannot fully compensate for the detrimental effects due to asymmetric skewed process corners. In addition, using only BBN might lead to degradations in terms of BBCO frequency gain or linearity.
2. **Generation of BBP from BBN:** A second possibility is to generate BBP from BBN with a *BBP driver* located between the LPF and the BBCO [Fig. 2.2(b)] as done in [34]. This second proposal has a medium design complexity. The resulting PLL preserves its full PVT compensation capability enabled by the FDSOI technology, including against asymmetric process corners. However, the BBP driver requires careful sizing. For instance, it has to be fast compared to the PLL dynamics to avoid disturbing the PLL stability. The BBP node being negative, the BBP driver needs a negative supply voltage preferably generated on-chip [34] or must rely upon switched-capacitor charge-pumps (SCCPs) [20]. Once again, these thoughts thus raise concerns regarding the overall PLL power consumption. We adopt this second strategy in the clock recovery design described in Section 2.4.
3. **Parallel generation of BBN and BBP:** The last possibility is to generate BBN and BBP in parallel, by providing two independent actuation paths to the BBCO [Fig. 2.2(c)]. While adding a dedicated BBP actuation branch rises the design complexity, the resulting PLL can also compensate for the detrimental effects due to asymmetric process corners. Nonetheless, this third solution also raises concerns regarding the overall PLL power consumption, area, and implementation. We explore this strategy in Chapter 3 in the context of frequency-locked loops.

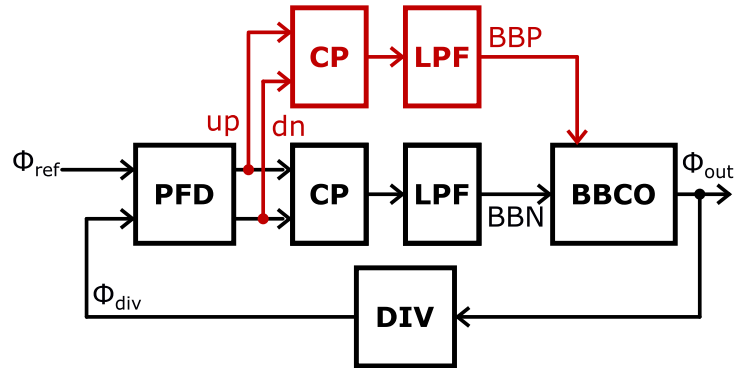
Last but not least, proposals 2 and 3 suffer from a parasitic coupling between BBN and BBP. Indeed, as seen in the general introduction, transistors in FDSOI



(a) No BBP generation.



(b) Generation of BBP from BBN.



(c) Parallel generation of BBN and BBP.

Fig. 2.2 Ideas concerning the generation of the control voltages of BBP-based PLLs in FDSOI technology.

conventionally share a deep N-well. This situation is shown again in Fig. 2.3(a). A reverse-biased N-well/P-well parasitic diode thus exists between BBN and BBP and is equivalent to a parasitic capacitance. It creates a parasitic coupling or crosstalk between the two PLL control voltages. Because the PLL drives them in opposite directions, this issue threatens its global stability. We identify two possible strategies to deal with this challenge:

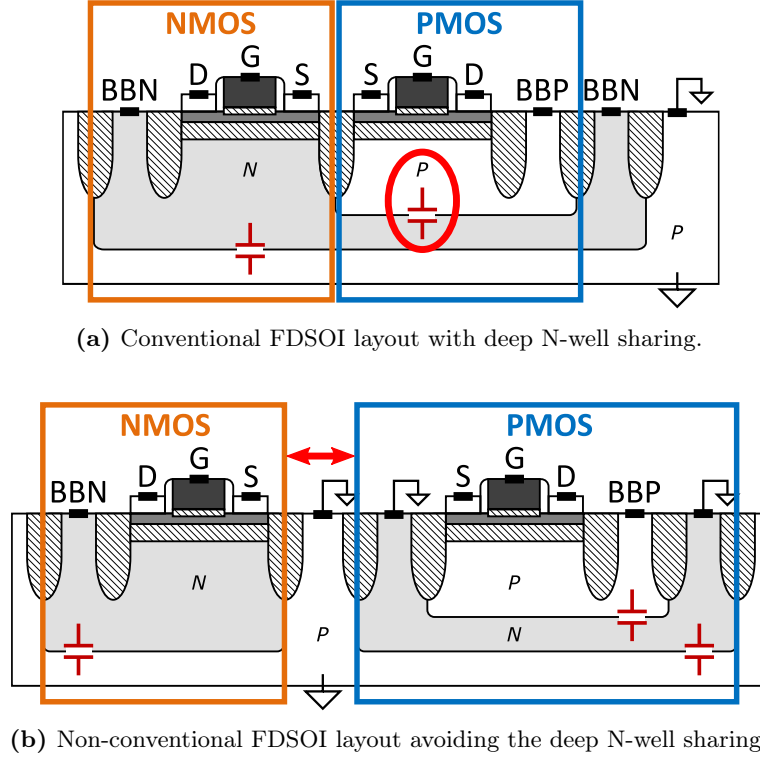


Fig. 2.3 Comparison of cross-sections of low- V_{th} (LVT) transistors in FDSOI technology to illustrate the BBN/BBP parasitic coupling challenge.

- A. **Tolerance to the BBN/BBP coupling:** A first possibility consists in tolerating the BBN/BBP coupling. This requires the estimation of the amount of parasitic coupling during the design phase (with post-layout parasitic extractions) to size the PLL accordingly. This solution increases the design effort (requiring several iterations between schematic and layout) and possibly the power consumption. We explore this solution in the prototypes described in Chapter 3.
- B. **Avoidance of the BBN/BBP coupling:** Alternatively, we can cancel the parasitic coupling by avoiding the deep N-well sharing between NMOS and PMOS transistors, at the cost of silicon area. This situation is represented in Fig. 2.3(b), and we will see an implementation example in Section 2.4.

2.3 Clock Recovery for a UWB Transceiver

Building upon the design considerations given in previous section, we now propose to apply them in practice through a concrete implementation. The chosen application falls in the domain of high-performance chip-to-chip communications. This section introduces the applicative context and presents the proposed circuit architecture.

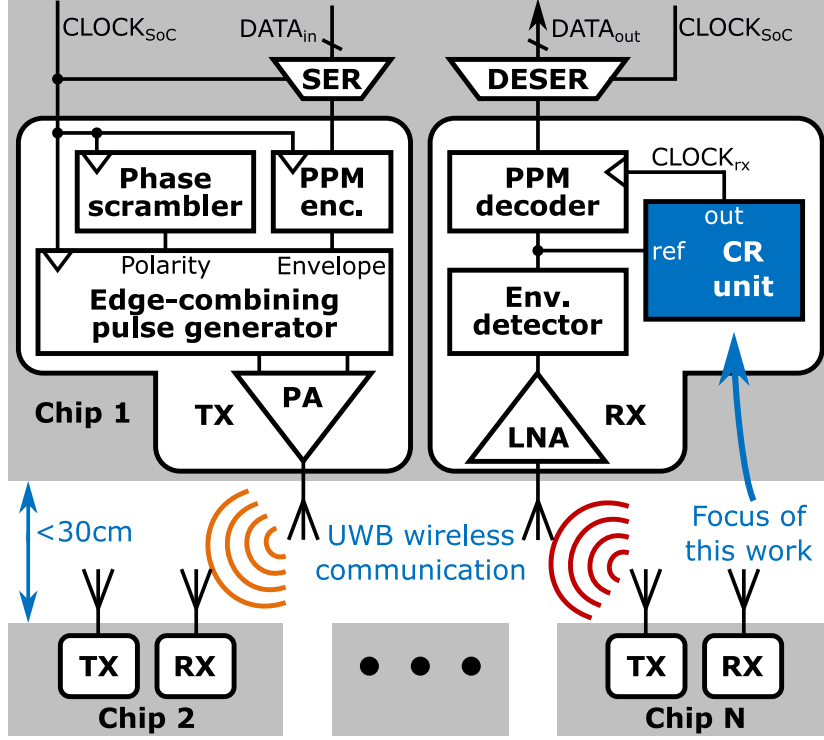


Fig. 2.4 Proposed UWB transceiver architecture.

High-performance chip-to-chip communications mostly rely on wireline serial links for the interconnection of different components in modern computers, data centers, or multi-core processors. Their success stems from many advantages they have over parallel alternatives, such as lower pin count, simpler routing, lower noise, and lower power. At high data rates, however, the energy efficiency of wireline protocols becomes limited by the RC characteristics of copper interconnects [53]. Wireless schemes thus appear as valuable alternatives to overcome this challenge, as they can provide better energy efficiency, lower latency, and lower system complexity [UJP2, 54].

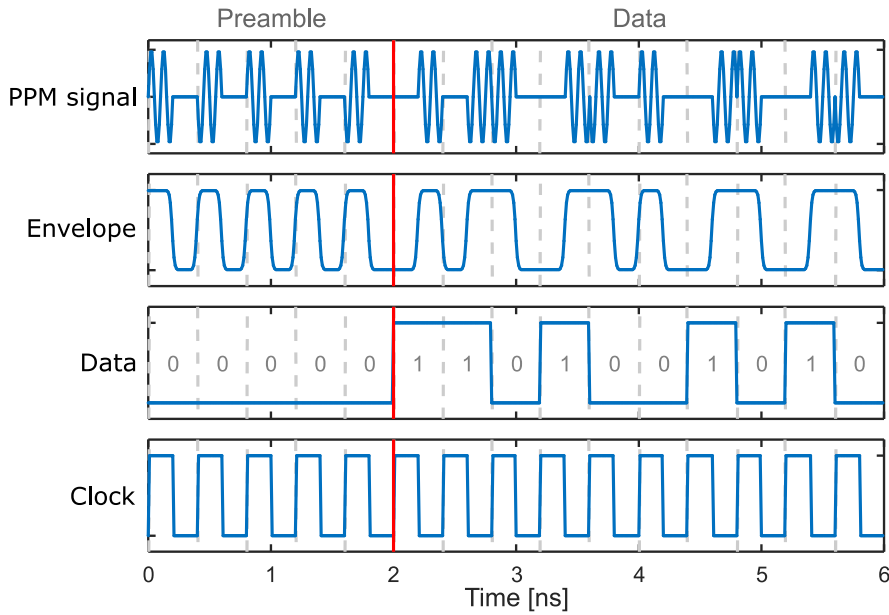
In this context, we design a *clock recovery* (CR) unit for a highly energy-efficient 2.5-Gb/s *ultra-wideband* (UWB) radio transceiver in 28-nm FDSOI. The proposed transceiver, codenamed WiXpress, is intended for integration into processor/memory systems-on-chip (SoCs), with chip-to-chip wireless communications over short distances, as illustrated in Fig. 2.4. Two applicative examples are in-chassis server-to-server communications (bypass of the layer-2 switch) or die-to-die communications in 3D integrated circuits (avoidance of through-silicon vias).

The proposed transceiver contains a transmitter (TX) and a receiver (RX) with CR, as depicted in Fig. 2.4. Table 2.1 gathers the transceiver specifications, which result from a system-level analysis presented in [54]. We use the 28-nm FDSOI technology from STMicroelectronics to design the chip and favor LVT flipped-well

Table 2.1 Specifications for the full UWB transceiver and its clock recovery unit [54].

Full Transceiver	
Modulation	UWB binary PPM
Data rate	2.5 Gb/s
Bandwidth	2.5 GHz
Central frequency	10 GHz
Range	10-30 cm
Power budget	< 15 mW
Energy	< 6 pJ/bit

Clock Recovery Unit	
Clock frequency	2.5 GHz
RMS period jitter (BER < 10^{-3})	< 12 ps
Power budget	< 5 mW
Energy	< 2 pJ/cycle

**Fig. 2.5** Example of 2.5-Gb/s UWB PPM modulation with a 10-GHz carrier frequency, divided into a preamble and a data payload.

devices to benefit from FBB. Data are transmitted from TX to RX using a binary pulse position modulation (PPM). Fig. 2.5 shows an example of an UWB PPM-modulated signal together with its envelope, the corresponding bit sequence, and the associated clock.

The TX generates the PPM-modulated signal from the 2.5-Gb/s input bit sequence and the 2.5-GHz generic SoC clock to avoid the need for an external crystal. A

pulse generator followed by a power amplifier (PA) achieves this purpose. A phase scrambler attenuates spectral lines in the frequency domain.

The RX receives the UWB signal and has to recover the corresponding bit sequence. Its architecture is similar to the implementation presented in [UJP2]. The main difference lies in the addition of the CR unit, which is thus the focus of this chapter. As reference, the CR takes the envelope of the incident UWB PPM signal obtained by the RF front-end (RFFE) consisting of a low-noise amplifier (LNA) followed by an envelope detector. The PPM decoder uses the CR recovered clock to demodulate and sample the data. As the SoC clock can suffer from high jitter and represents the time reference at the TX side, the CR unit performs high-bandwidth phase tracking at the RX side. For synchronization purposes, the CR needs a preamble made of all-zeros symbols before receiving the data payload.

2.4 Proposed Clock Recovery Unit

In this section, we focus on the architecture of the CR unit, whose design targets the performance levels detailed in Table 2.1. In particular, we desire a high efficiency with energy levels below 2 pJ/cycle. In addition, for a correct data decoding at the RX level with a bit error rate (BER) below 10^{-3} , the CR must exhibit a root mean square (RMS) period value below 12 ps [54]. Assuming thermal noise only, this translates into a phase noise specification of -57 dBc/Hz at an offset frequency of 1 MHz (please refer to Table 1.3 in Chapter 1). It is an easy target for a CR based on a ring oscillator (RO) and thus justifies our use of a BBCO (instead of a resonant oscillator).

We present the design of the CR in three steps. We first introduce its dual-loop architecture in Section 2.4.1. The block-level design then follows in Section 2.4.2. Finally, we verify the CR functionality and performance with simulation results in Section 2.4.3. Additionally, we propose a continuous-time model of the CR unit in Appendix B.

2.4.1 Dual-PLL Architecture

Recovering a clock often relies on PLLs, which usually need to achieve fast locking while consuming a low in-lock power. The CR block presented here relaxes these two conflicting requirements by using two complementary feedback loops, taking inspiration from other works [52, 55]. A start-up PLL first targets fast settling time and frequency acquisition during the preamble. A second PLL (main PLL) aims for high-bandwidth low-jitter phase tracking during the data payload. Fig. 2.6 presents this dual-loop architecture. The CR main supply voltage is 0.8 V, except for FBB generation, which requires +1.8 V and -1.8 V.

As shown in Fig. 2.6, the two PLLs share an oscillator, an LPF, and a BBP driver but differ by the type of phase detector (PD) they use and by the strength of

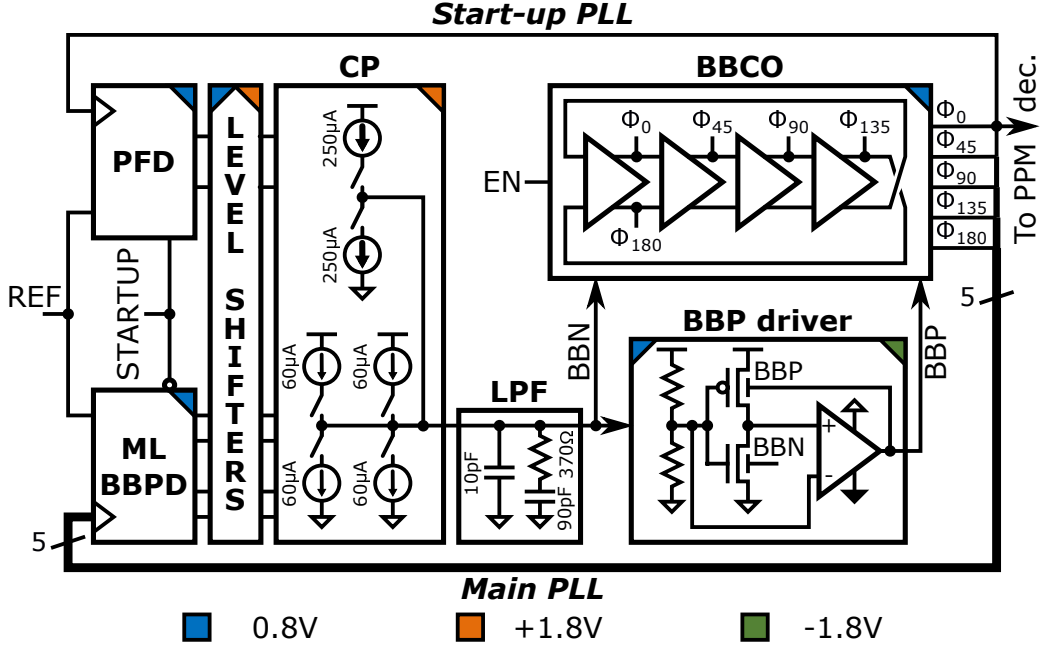


Fig. 2.6 Proposed dual-loop clock recovery architecture. The PLL selection is externally controlled with the **STARTUP** signal.

their respective CPs. As a reminder, the envelope of the UWB PPM signal serves as reference. During the preamble, this reference is a periodic 2.5-GHz signal. Therefore, a conventional phase-frequency detector (PFD) can act as detector in the start-up PLL. However, during the UWB data portion, the envelope signal is data-dependent due to the PPM modulation and looks like 5-Gb/s data (see Fig. 2.5). The PFD can consequently not keep the lock in these conditions.

For this reason, the main PLL needs a half-rate (HR) PD to accurately track the data phase. We choose a bang-bang phase detector (BBPD) for its simplicity, high-speed operation, and better phase alignment with respect to a linear counterpart [52]. Due to its highly non-linear nature [56], this kind of PD exhibits a high gain value for small phase errors. This high gain greatly enhances the main PLL bandwidth for better tracking of the input phase. However, it can also lead to marginal stability as well as excessive power consumption.

In order to avoid these two drawbacks, we lowered the main PLL CP current by $2\times$ compared to the start-up PLL. In addition, we replaced the BBPD with a multi-level BBPD (ML-BBPD) version as in [57], further reducing the CP branch current by $2\times$ while keeping the same CP current range. Altogether, the resulting $4\times$ smaller CP branch current leads to $\sim 70\%$ CP average power savings and a $\sim 75\%$ reduction of RMS period jitter. Furthermore, the ML-BBPD needs five clock phases (0° , 45° , 90° , 135° , and 180°) for its operation.

The start-up and main PLLs are complementary, as the former cannot track the

phase within the data payload, while the latter cannot acquire the frequency, even within the preamble. For testing purposes, an external signal named **STARTUP** controls the PLL selection. In the complete application context [54], we can automate the switch by detecting the lock of the PFD-based start-up PLL using the most significant output bits of the ML-BBPD, whose absence of activity indicates the main PLL is in range for phase locking. In this work, the preamble length is fixed to $1.5\ \mu\text{s}$ (3750 symbols) to cover circuit variability (see the simulation results of Section 2.4.3) while limiting latency/power overheads. Indeed, the phase tracking capability of the CR unit allows the use of very long packets to easily amortize the overheads associated with the preamble.

2.4.2 Block Design: BBCO and BBP Driver

In this part, we focus on the design of the BBCO and the BBP driver, as they are the most essential blocks of the CR unit. The other constitutive blocks, such as the PDs, the level shifters, the CPs, and the LPF, are more classical and thus not explained in detail.

Low-power PLLs conventionally use CSROs [55, 58], but we rely on a BBCO instead [CP1, 34]. As shown in Chapter 1, a BBCO stacks fewer transistors and exploits the FBB capability offered by the FDSOI technology. It allows generating a 2.5-GHz clock with a lower supply voltage and thus lower power. According to our estimates, we obtain 250 mV of supply voltage scaling in that way (200 mV thanks to FBB, 50 mV when moving from a CSRO to a BBCO). As will be shown in Section 2.4.3, the proposed BBCO-based CR unit supplied at 0.8 V consumes less than 800 μW in simulations. As a comparison, our initial CR design based on a CSRO was requiring 1-V of supply voltage to operate properly and its (non-optimized) power consumption was around 2 mW in simulations.

The BBCO has a multi-path architecture, as represented in Fig. 2.7(a). Four feed-forward differential stages allow the generation of the five required clock phases. They are similar to the ones used in [34] and proved to be excellent for limited jitter at low power. Fig. 2.7(b) depicts their transistor-level schematic. We use a non-minimal length of 50 nm, leading to a power reduction of $\sim 8\%$ without any penalty. Multiplexers are used to correctly kick-start the oscillator.

Both BBN and BBP control the BBCO oscillation frequency. We limit their generation to $+1.8\ \text{V}/-1.8\ \text{V}$ (instead of $+3.0\ \text{V}/-3.0\ \text{V}$) for BBN/BBP, respectively, and their default values are $+0.9\ \text{V}/-0.9\ \text{V}$ in nominal conditions.

The CPs regulate BBN through the lead-lag LPF and use a $+1.8\ \text{V}$ external supply voltage. They are made of thick-oxide I/O transistors to withstand this higher voltage. We use level shifters to transfer the 0.8-V signals coming from the PDs to the 1.8-V domain of the CPs. Concerning the negative BBP voltage, we choose to generate it from BBN with a BBP driver. As previously discussed in Section 2.2.2, this independent FBB generation makes the CR tolerant to PVT

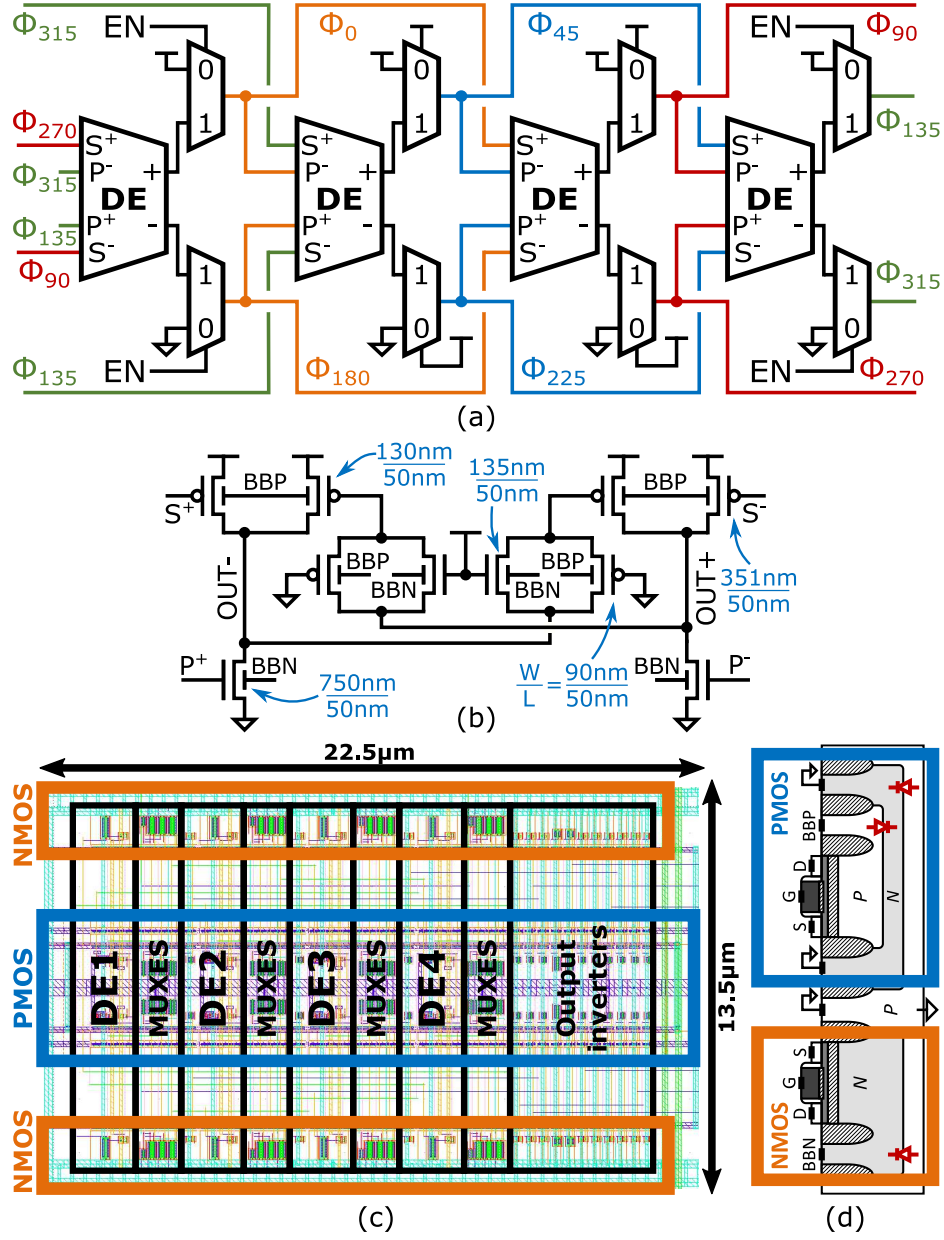


Fig. 2.7 Details about the back-bias-controlled oscillator: (a) 4-stage differential architecture, (b) transistor-level schematic of one delay element (DE), (c) abstract layout without sharing of the deep N-well between NMOS and PMOS transistors, and (d) corresponding transistor cross-sections.

conditions, including asymmetric skewed process corners, while keeping the design complexity moderate.

The BBP driver reuses an idea implemented in [34]: it generates BBP by continuously matching the effective currents of NMOS and PMOS transistors. It comprises a back-gate-driven RC Miller amplifier and N/PMOS process imbalance sensors.

The amplifier uses a supply voltage of -1.8 V and thus employs I/O devices, while the process imbalance sensors operate at 0.8 V and use core LVT transistors, as the BBCO and PDs. They are designed to have matched NMOS/PMOS currents at the nominal BBN/BBP point of +0.9 V/-0.9 V.

The use of the BBP driver creates an inherent delay between the actuation on BBP and the generation of BBN, which threatens the PLLs stability. We strengthen the back-gate-driven amplifier to sufficiently increase its bandwidth compared to the dual-loop PLL so as to avoid this issue.

The parasitic coupling between BBN and BBP existing in conventional FDSOI layouts also threatens the PLLs stability (see our discussion in Section 2.2.2). We prevent this issue by avoiding the deep N-well sharing between NMOS and PMOS transistors for the BBCO and the process imbalance sensors. This solution leads to a BBCO area overhead of +50%, as illustrated in Fig. 2.7(c)-(d). At the transceiver level, this cost is negligible as it only represents an area overhead of less than 0.3%.

We end this section by verifying the functionality of the BBCO and the BBP driver. Fig. 2.8 depicts their simulated transfer functions and demonstrates their robustness to process and temperature (PT) variations, including asymmetric process corners. In nominal conditions (TT process, 25°C), the BBP driver matches the N/PMOS imbalance with symmetrical BBN/BBP values (in other words, $BBP = -BBN$). The picture changes with skewed process corners. For instance, for FS/SF corners (in orange/light blue in Fig. 2.8(a), respectively), the BBP driver generates a higher/lower magnitude for BBP than BBN and compensates for the slowness/fastness of the PMOS transistors compared to the NMOS ones. In terms of BBCO oscillation frequency, Fig. 2.8(b) shows a functional behavior as the BBCO reaches the 2.5-GHz frequency target in all considered PT corners, except for FF corners (in red) which are slightly borderline. The BBCO is thus a little bit faster than required, which gives some safety margins for possible additional degradations in measurements (coming from IR drops or additional parasitics, for instance). The BBCO exhibits a good linearity in its transfer function, as discussed in Chapter 1. In terms of post-layout performance, the BBCO consumes 236 μ W of power in typical conditions and achieves a low phase noise level of -121.1 dBc/Hz at an offset frequency of 100 MHz. This translates into a phase noise figure of merit (FoM) of -155 dBc/Hz.

2.4.3 Clock Recovery Simulation Results

It is time to look at the CR unit functionality and performance. Complete CR start-up sequences are shown in Fig. 2.9, simulated under nominal (TT +25°C) and extreme PT corners. Instead of TT, SS and FF process corners are considered here, with temperatures going from -40 to +85°C. The reported in-lock power values below 800 μ W are for the nominal case and meet the specifications of Table 2.1.

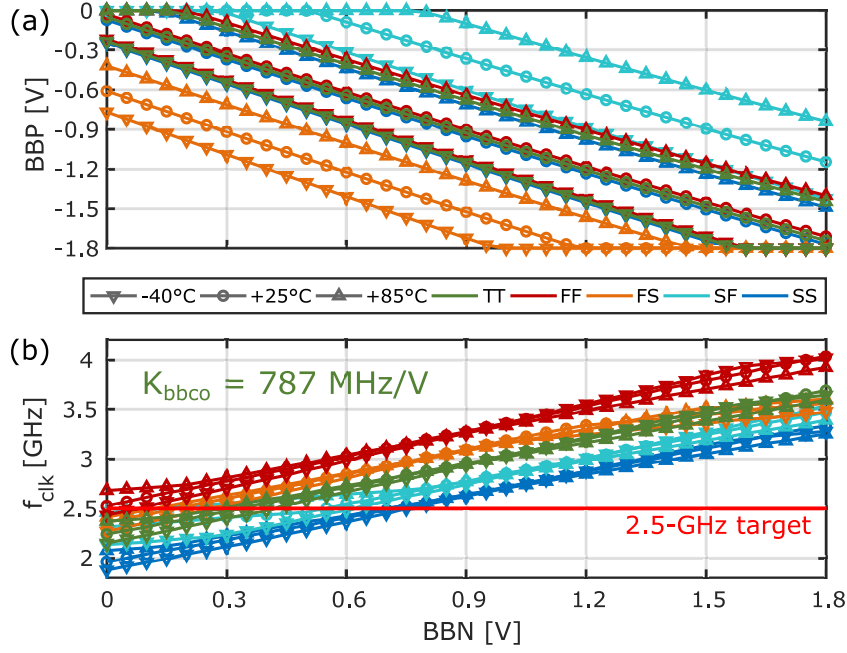


Fig. 2.8 Simulated transfer function of the BBP driver and BBCO combined. The BBCO gain is extracted in nominal conditions (TT +25°C).

The start-up is composed of three phases, and the CR unit thus has three operational modes:

1. **Start-up PLL within the preamble:** The CR first acquires the frequency in $< 1.0 \mu\text{s}$ with its start-up PLL ($\text{STARTUP} = 1$) within the preamble [Fig. 2.9(a)-(b)].
2. **Main PLL within the preamble:** It is then switched to the main PLL ($\text{STARTUP} = 0$) and stays phase-locked with the reference signal [Fig. 2.9(c)].
3. **Main PLL within the data payload:** Finally, the data starts, and the CR stays locked again [Fig. 2.9(d)].

The CR preserves its functionality under all considered PT corners (albeit with 0.75 V of supply voltage instead of 0.80 V for the FF +85°C case). Fig. 2.10 also validates the CR behavior under skewed process corners.

Fig. 2.11 gathers the simulated jitter performance level of the CR unit in its three operational modes (blue curves) and compares them to the BBCO taken alone (in orange). The BBCO generates an RMS period jitter of around 635 fs and a phase noise level of -69.27 dBc/Hz at a 1-MHz offset frequency. At the CR level, the RMS period jitter levels (in red) are below 1 ps for all the CR modes and thus satisfy the system-level specification of 12 ps provided in [54] and Table 2.1.

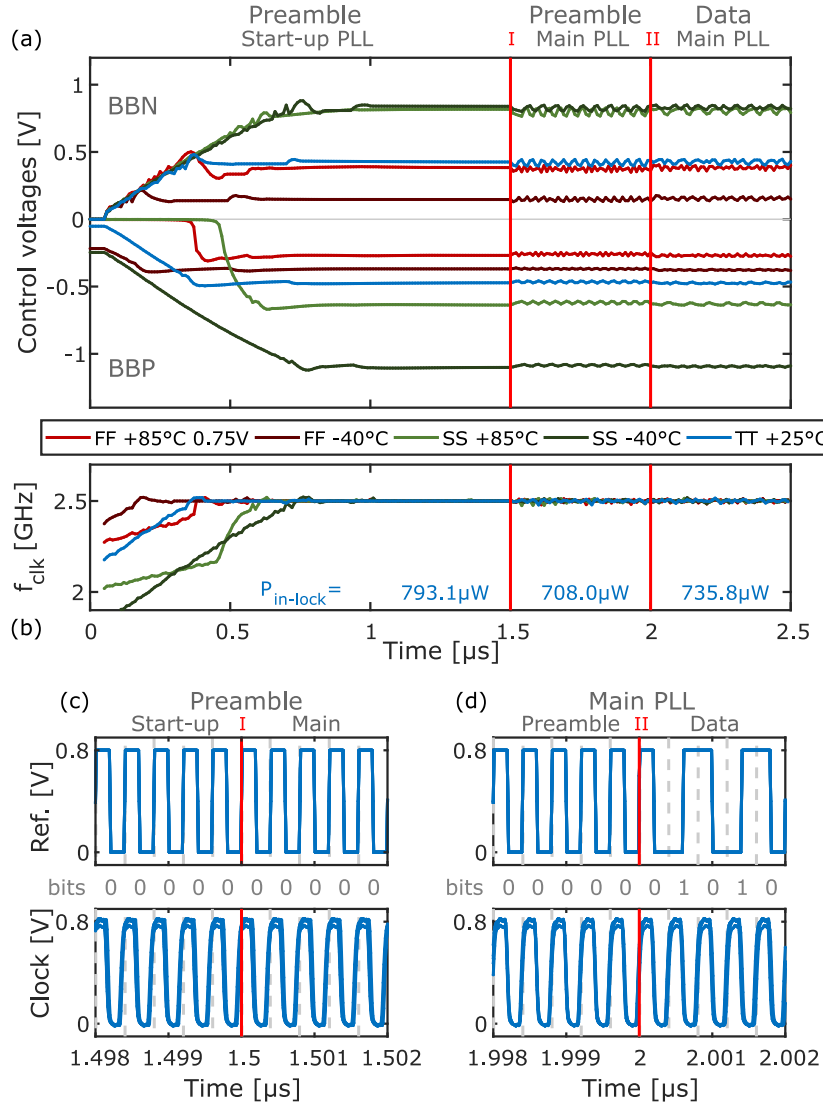


Fig. 2.9 Post-layout simulations of the proposed clock recovery unit under nominal and extreme PVT conditions (symmetric process corners): (a)-(b) complete start-up sequences, (c) zoom on the transition from start-up to main PLL within the preamble, and (d) zoom on the transition from preamble to data payload.

The effect of the implemented feedback loops is clearly visible in Fig. 2.11, as the PLLs stop the jitter accumulation after some time related to their respective bandwidth. While the bandwidth of the start-up PLL is around 12 MHz, the main PLL reaches >100 MHz (thanks to the high gain value of its ML-BBPD), which improves phase tracking capability and TX jitter tolerance coming from the noisy SoC clock. These bandwidth differences explain the obtained RMS long-term jitter levels (black annotations), which reach 14.9 ps and 10.4 ps for the start-up and main PLLs, respectively.

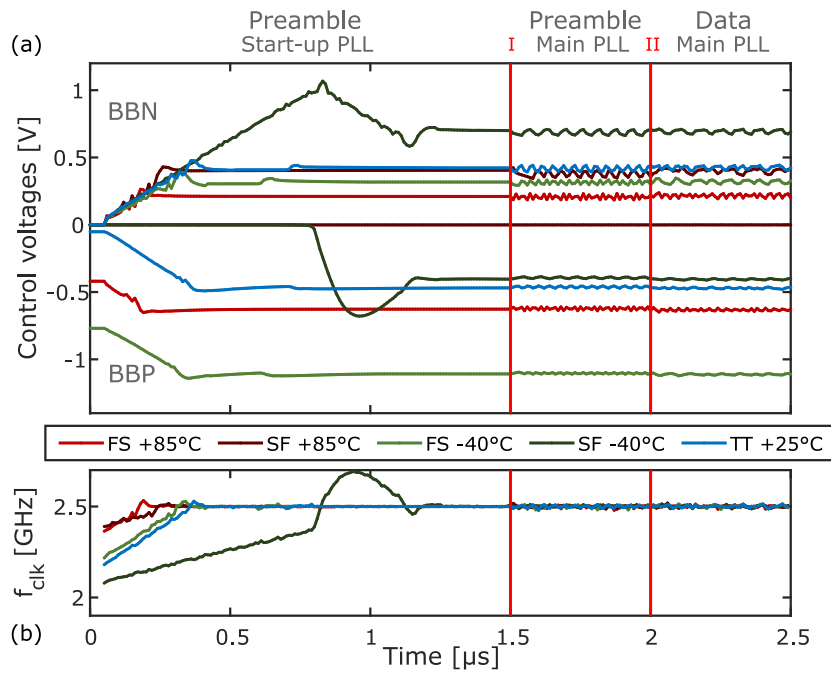


Fig. 2.10 Post-layout simulations of the proposed clock recovery unit under nominal and extreme PVT conditions (asymmetric skewed process corners).

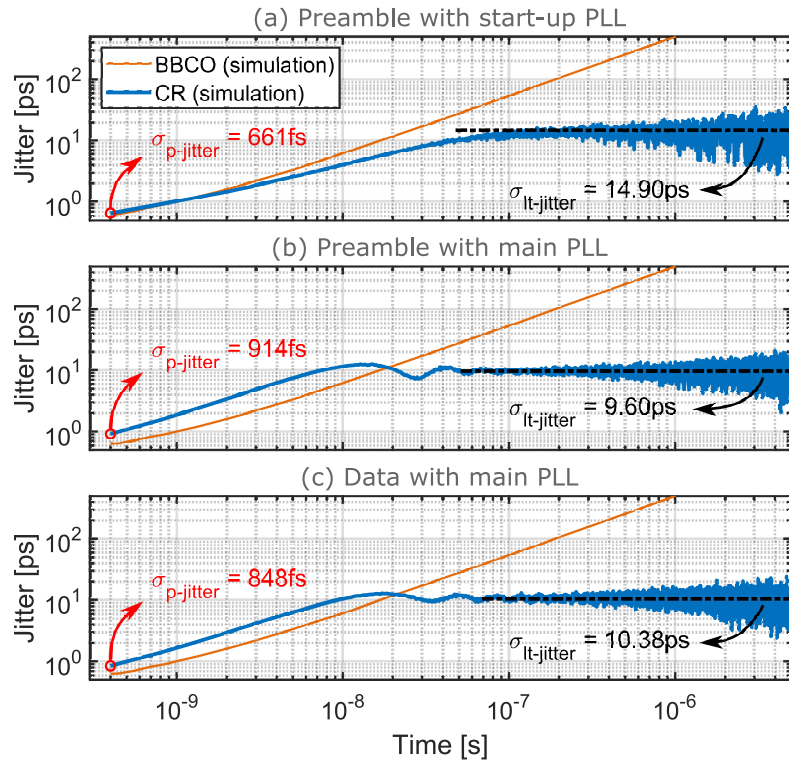


Fig. 2.11 Jitter performance obtained with the clock recovery in simulation.

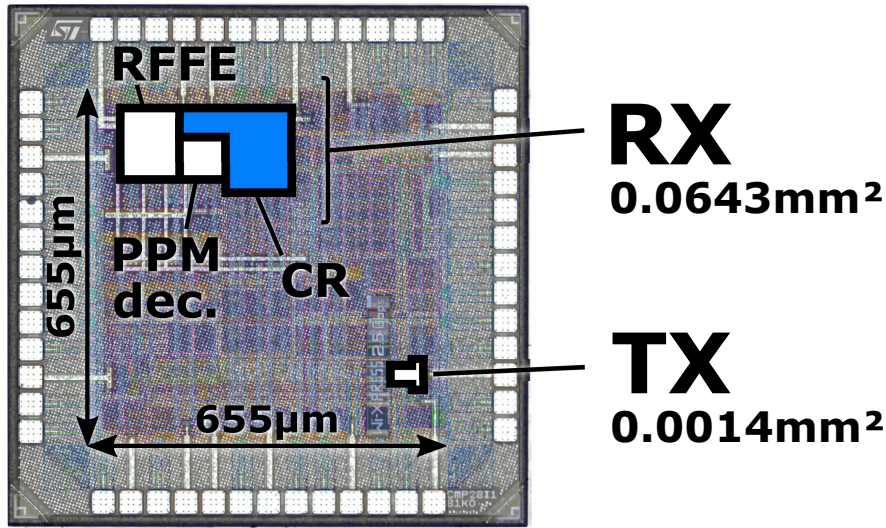


Fig. 2.12 Die microphotograph.

2.5 Prototyping and Measurement Results

This section presents experimental results obtained with the CR unit. The entire UWB transceiver containing the CR is fabricated in 28-nm FDSOI technology and occupies an effective silicon area of 0.066 mm^2 . Fig. 2.12 shows a die photograph and highlights its constituting parts. The CR occupies less than 0.043 mm^2 , dominated by the LPF which represents 85% of the total CR area.

The CR functionality and performance are verified in measurements in Fig. 2.13, with a testing setup similar to [UJP2]. The three CR supply voltages (0.8, +1.8, and -1.8 V) are externally provided. The phase alignment between the envelope signal (in blue) and the CR output clock (in green) stays constant in the three CR operational modes. The frequency acquisition using the start-up PLL within the preamble takes less than $1.1 \text{ } \mu\text{s}$. The power consumption of the start-up PLL is 1.049 mW, resulting in an energy level of 0.420 pJ/cycle. The main PLL consumes 1.034 mW within the data payload. This power consumption corresponds to an energy value of 0.414 pJ/cycle.

These power numbers are higher than in the simulations of Section 2.4.3. Experimental causes, such a slow corner, can explain this observation, as they can force the CR to lock at higher BBN/lower BBP values, thus pushing the CR deeper into the FBB regime and increasing power consumption. Nonetheless, the results stay competitive and help the full UWB transceiver achieve a measured energy value of 2.36 pJ/bit (0.70 pJ/bit for the TX, 1.66 pJ/bit for the full RX).

Fig. 2.14 shows the experimental jitter performance levels of the CR unit for its three modes of operation and compares them with the simulation results of Fig. 2.11. We observe a good agreement between simulations and measurements.

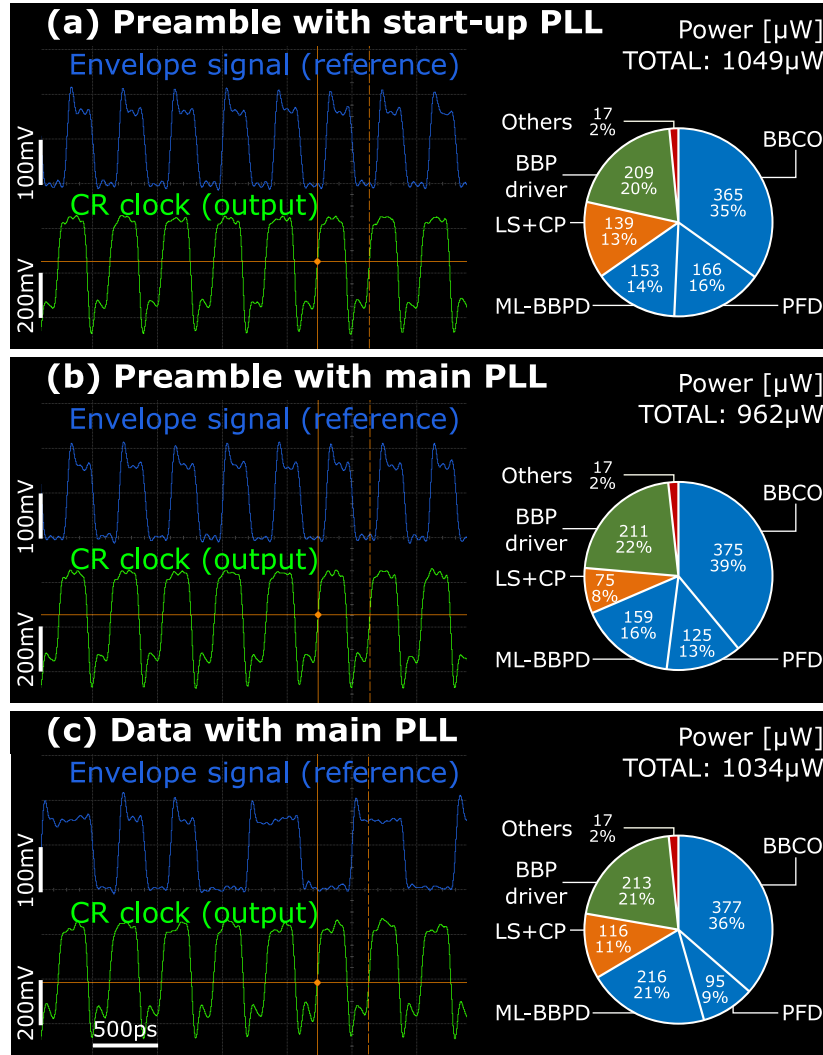


Fig. 2.13 Measurement results of the proposed clock recovery unit. Power breakdowns of each supply domain are estimated from post-layout simulations.

As in simulations, the CR unit reaches RMS period jitter values (red annotations) below 1 ps. It achieves its best long-term jitter performance (black annotations) with its main PLL within the data payload, reaching an RMS value of 6.5 ps.

Compared to other works from the literature in Table 2.2, the proposed CR appears very competitive in terms of energy and area and achieves the best power/jitter trade-off, highlighted by a jitter FoM value of -224 dB. In addition, we demonstrate robustness to a wide range of PVT conditions. However, we need a negative supply voltage but efficient solutions exist for an on-chip generation [34]. The best energy number is achieved by [58], explained by a constant-frequency PPM modulation scheme, which allows recovering the sub-GHz clock with a simple PFD-based low-bandwidth PLL.

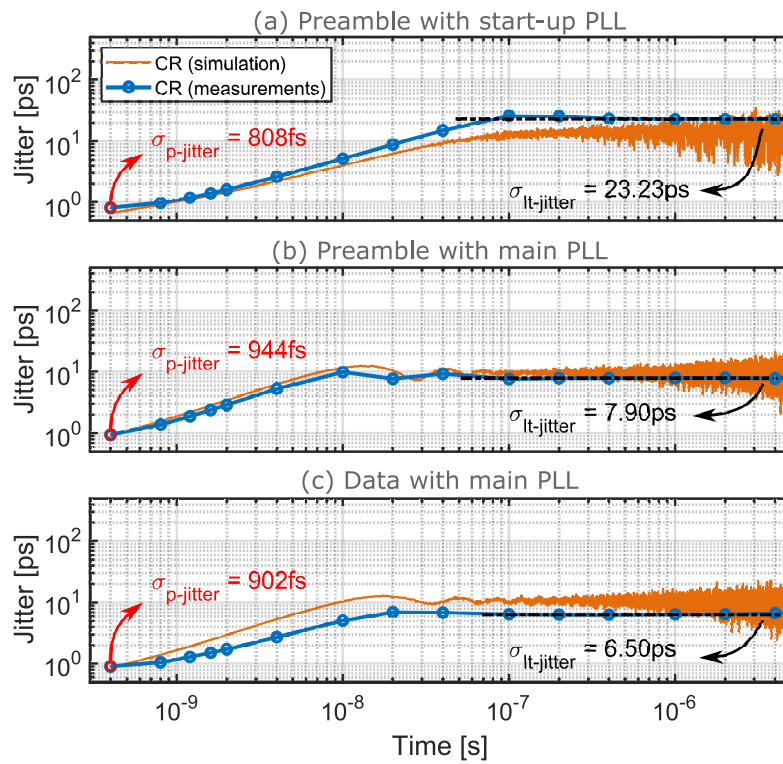


Fig. 2.14 Jitter performance obtained with the clock recovery in measurement.

Table 2.2 Performance comparison of low-energy (< 5.5 pJ/cycle) clock recovery circuits for sub-4 GHz embedded-clock systems.

Metrics	Units	Shu, 2014 [55]	Ju, 2016 [58]	Lee, 2016 [59]	Gimeno, 2018 [52]	This work [JP2]
Status	-	Silicon	Silicon	Silicon	Pre-layout sim.	Silicon
CMOS Technology	-	90-nm bulk	65-nm bulk	65-nm bulk	28-nm FDSOI	28-nm FDSOI
Supplies	V	1.0/1.3	0.9	1.2	1.0/1.8	0.8/+1.8/-1.8
Area	mm ²	0.62	0.25 ⁺	0.018	N-A	0.043
Clock Frequency	GHz	2.5	0.8	3.25	2.5	2.5
Settling Time	μs	N-A	N-A	N-A	< 0.5	< 1.1
In-Lock Power	mW	13.1	0.268	15.6	1.43	1.034
Energy	pJ/cycle	5.24	0.335	4.8	0.572	0.414
RMS Long-Term Jitter	ps	5	N-A	4.04	N-A	6.5
Jitter FoM [†]	dB	-215	N-A	-216	N-A	-224
Topology	-	FLL+PLL CSRO in PRPLL FD+BBPD	PLL CSRO PFD	CFD+DPTL ILO+DCDL BBPD	FLL/PLL BBCO FD/ML-BBPD	PLL BBCO PFD/ML-BBPD

Notations: FLL: frequency-locked loop. PLL: phase-locked loop. PRPLL: phase-rotating PLL. CFD: coarse frequency detector. DPTL: digital phase tracking loop. CSRO: current-starved ring-oscillator. ILO: injection-locked oscillator. DCDL: digitally-controlled delay-line. BBCO: back-biased-controlled oscillator. FD: frequency detector. BBPD: bang-bang phase detector. PFD: phase frequency detector. ML: multi-level.

⁺ Estimated from layout.

$$^{\dagger}\text{FoM}_{\text{jitter}} = 10 \log_{10} \left[(\sigma_{\text{lt-jitter}}^2 \cdot P) / (1\text{s}^2 \cdot 1\text{mW}) \right].$$

Table 2.3 Summary of the BBCO performance and possible improvement.

		Sim. Results		Meas.		Extrapolation (constant FoM)
		Schematic	Layout	Results		
f_0	GHz	4.25 ⁺	2.45	2.5	×1	2.5
P	[μW]	223.91	236.18	377*	/10	37.7
σ_P	[ps]	0.368	0.637	0.902 [§]	×10	9.02
$\mathcal{L}(1 \text{ MHz})$	[dBc/Hz]	-67.4	-69.3	-69 ^{†‡}	×10	-59
FoM		-146	-143	-140	×1	-140
$\mathcal{L}(100 \text{ MHz})$	[dBc/Hz]	-120.0	-121.1	-119 [†]	×10	-109
FoM		-159	-155	-150	×1	-150

⁺Over-constrained to account for post-layout parasitics. *BBCO power share estimated from post-layout simulations. [§]Assumes the BBCO is the only source of jitter in the CR. [†]Estimated from the period jitter value (see Table 1.3) assuming purely thermal noise. [‡]Assumes also a 10-dB contribution from flicker noise.

2.6 Analysis of the BBCO Results

As demonstrated in previous sections, the CR unit achieves competitive results with a significant contribution coming from its BBCO. Before concluding this chapter, we thus propose to put the BBCO results in perspective with the considerations of Chapter 1.

Table 2.3 summarizes the performance levels achieved with the BBCO design of this chapter, such as the oscillation frequency, the power, and the RMS period jitter. It also indicates the phase noise levels at two different offset frequencies, as well as the corresponding phase noise FoM values. Both simulation (pre- and post-layout) and measurements results are included. Several remarks can be made.

The first remark concerns the phase noise FoM. Note that for a differential RO architecture, the theoretical FoM limit is -160 dBc/Hz [29] (see also Fig. 1.4). In Table 2.3, the pre-layout results are very close to that limit. The BBCO schematic thus appears excellent in terms of power/phase noise trade-off. However, we can observe a FoM degradation when moving to post-layout results and to experimental results. This increase can partially be explained by the parasitic capacitances coming from the metal routing (as briefly discussed in Section 1.4.1). We can also expect extra impacts coming from the experimental setup due to additional noise sources or circuit board parasitics, for instance. Finally, note that the period jitter of the entire CR unit is attributed to the BBCO in the measurement results shown in Table 2.3, as there is not way to experimentally determine the exact contribution of the BBCO.

The second remark concerns the jitter and phase noise levels. As a reminder, the jitter specification at the system level is 12 ps of RMS period jitter [54] and corresponds to a target BER below 10^{-3} . Assuming only thermal noise, this translates to a phase noise specification of -57 dBc/Hz at a 1-MHz offset frequency and -97 dBc/Hz at a 100-MHz offset frequency (see Section 2.4). Both in terms of

jitter and phase noise levels, the BBCO results of Table 2.3 are at least one order of magnitude below the corresponding specifications.

This last observation leaves margin to reduce the BBCO power contribution. Indeed, it should be possible to trade power for jitter and phase noise while keeping constant the oscillation frequency and the power/noise trade-off. We can thus expect reducing the power by a factor 10 while increasing the noise level by 10. The last column in Table 2.3 illustrates this perspective and shows we can reasonably hope reaching a BBCO power below 50 μW while satisfying the system-level specifications in terms of jitter and phase noise.

2.7 Conclusion

In this second chapter, we analyzed the benefits and challenges of BBCOs in the context of PLL design. Rather than a block-level perspective (at the oscillator level) as done in Chapter 1, this chapter thus took a system-level point of view (at the PLL level).

We identified two important challenges linked to the design of BBCO-based PLLs. Firstly, as BBP takes negative value, its on-chip generation is not straightforward. Secondly, a parasitic coupling appears between BBN and BBP due to the deep N-well sharing between NMOS and PMOS devices in conventional layouts, and it threatens the loop stability. To experience and illustrate how to tackle these challenges, we proposed a concrete design implemented within a silicon prototype manufactured in 28-nm FDSOI technology. The targeted application concerns wireless short-distance chip-to-chip communications for which we present an efficient CR unit within a 2.5-Gb/s UWB transceiver.

The CR uses a dual-PLL architecture built around a BBCO. The PFD-based start-up PLL first acquires the frequency within the preamble. The main PLL then takes over and requires an ML-BBPD for correct phase alignment within the data payload. Thanks to these two complementary PLLs, the low-power CR achieves fast locking and high-bandwidth phase tracking. We exploit the FBB capability of FDSOI technology to generate the required 2.5-GHz frequency using a BBCO and operate at a low supply voltage to save power. In that manner, we obtain 250 mV of supply voltage scaling compared to a solution based on a CSRO. The FBB feature also allows maintaining the CR functionality over a wide range of PVT conditions, including skewed process corners, thanks to an independent BBN/BBP generation. We generate BBP from BBN using a BBP driver comprising N/PMOS process imbalance sensors and a back-gate driven amplifier. To avoid any stability issue, i) we strengthened the amplifier in the BBP driver to sufficiently increase its bandwidth compared to the PLLs one, and ii) we avoided the deep N-well sharing between NMOS and PMOS transistors in the BBCO and process imbalance sensors to alleviate the BBN/BBP coupling challenge.

These innovations resulted in competitive power, performance, and area results: the CR unit locks in less than 1.1 μs , consumes 1.034 mW in lock, generates 6.5 ps of RMS long-term jitter, and occupies a limited area of 0.043 mm². The proposed CR is efficient with an energy value of 0.414 pJ/cycle and exhibits an excellent power/jitter trade-off with a jitter FoM value of -224 dB.

The Unified Frequency and Back-Bias Regulation Concept

Contents

3.1	Introduction	80
3.2	Adaptive Techniques for ULV Operation	81
3.3	First Generation of UFBBR Prototype	84
3.4	Second Generation of UFBBR Prototype	92
3.5	Comparison to the State of the Art	120
3.6	Conclusion	123

Abstract In this chapter, we propose a new adaptive technique to cover the variability of ultralow-voltage/ultralow-power (ULV/ULP) circuits. It is called unified frequency and back-bias regulation (UFBBR) and combines the system clock generation with asymmetric adaptive back biasing (ABB) to compensate for process, voltage, and temperature (PVT) variations. The regulation loop corrects both the logic speed and the mismatch between rising and falling transition times due to N/PMOS process imbalance, according to the target clock frequency and the operating conditions. A back-bias-controlled oscillator (BBCO) serves as clock generator and logic speed sensor. The N/PMOS process imbalance sensors (PISs) are digital and made of delay lines or ring oscillators. The back-bias actuators are based on charge pumps. Two different UFBBR versions are respectively incorporated in custom ULV/ULP microcontroller unit (MCU) prototypes manufactured in 28-nm FDSOI technology [CP1, JP3, CP2, JP4]. These MCUs are based on a processor from the Cortex-M family of ARM, embed custom ULP SRAM memory macros, and target ULV/ULP applications for the Internet-of-Things (IoT). We demonstrate the benefits brought by an UFBBR macro using extensive simulation and measurement results. At the block level, our UFBBR designs showcase an excellent trade-off between settling time ($< 10 \mu\text{s}$), power ($< 22 \mu\text{W}$), and area ($< 0.06 \text{ mm}^2$) overheads compared to other ABB systems from the literature. At the system level, energy values of 3-5.5 $\mu\text{W}/\text{MHz}$ and sleep power levels of 7.7-12.7 μW with logic state and memory retentions are demonstrated. In addition, the UFBBR prototypes generate the MCU system clock up to 80 MHz, compensate for PVT variations including asymmetric skewed process corners and on a wide range of temperatures, i.e., from -40 to $+85^\circ\text{C}$, and give robustness against voltage droops. These features demonstrate the relevance of the UFBBR concept for ULV/ULP applications.

3.1 Introduction

As explained in the general introduction of this dissertation, the deployment of the Internet-of-Things (IoT) requires to design ultralow-power (ULP) wireless sensor nodes, so as to extend their autonomy/lifetime. In this quest towards minimizing the power consumption of integrated circuits, combining nanometer CMOS technologies together with ultralow-voltage (ULV) circuit operation proves to be very effective to lower the power consumption [60–62] at the cost of a severely degraded robustness against process, voltage, and temperature (PVT) variations [12]. Ensuring a functional ULP circuit operation while preserving this functionality over a wide range of PVT corners thus appears challenging. Hopefully, FDSOI technologies can help in this context, thanks to the improved electrostatic characteristics of their transistors and, more importantly, the *back-biasing* (BB) feature they offer [16].

In this final chapter, we focus on the clock generation and PVT compensation in ULV/ULP microcontroller units (MCUs) in the context of IoT applications. From the review of several adaptive techniques commonly used to cover the PVT variations, we propose a new adaptive mechanism: the *unified frequency and back-bias regulation* (UFBBR). As its name suggests, this new technique unifies the MCU clock generation with adaptive forward back biasing (FBB) for the PVT compensation.

The UFBBR compensates for PVT variations, affecting both the logic speed and the N/PMOS process imbalance of the circuit to regulate, using asymmetric adaptive FBB. It is thus a closed-loop system comprising sensors, a control unit, and FBB actuators. A back-bias-controlled oscillator (BBCO) simultaneously serves as clock generator and as logic speed sensor. Dedicated process imbalance sensors (PISSs) sense the N/PMOS process imbalance.

We experimentally demonstrate the benefits of the UFBBR technique with two chip prototypes manufactured in 28-nm FDSOI technology. Our two UFBBR designs are integrated in two different MCU systems on chips (SoCs), respectively named SleepRunner [CP1, JP3] and SleepRider [CP2]. As will be demonstrated in the remaining part of this chapter, the UFBBR units play a key role in improving the energy efficiency and robustness of both MCU SoCs, with limited power and area overheads.

The chapter is structured as follows. Firstly, Section 3.2 reviews various adaptive techniques and introduces the UFBBR concept. We then present two successive implementations of UFBBR. Section 3.3 describes our first prototype, while Section 3.4 focuses on our second UFBBR version. Both our designs are finally compared to the state of the art in Section 3.5. The contents of this chapter are adapted from [CP1, CP2, JP3, JP4].

Table 3.1 Impact of process, voltage, and temperature (PVT) variations on logic delay and leakage. Results obtained from SPICE simulations of low- V_{th} inverter chains in 28-nm FDSOI, with $BBN = +1$ V and $BBP = -2$ V. SS, TT and FF processes are considered.

Process	Voltage	Temperature	Normalized delay	Normalized leakage
SS	0.36 V	-40°C	6.40×	0.01×
SS	0.36 V	+25°C	2.44×	0.39×
SS	0.40 V	+25°C	1.41×	0.42×
TT	0.40 V	+25°C	1×	1×
FF	0.40 V	+25°C	0.69×	3.89×
FF	0.44 V	+25°C	0.50×	4.40×
FF	0.44 V	+85°C	0.41×	33.72×

3.2 Adaptive Techniques for ULV Operation

This section introduces various system-level techniques commonly used to ensure robustness against PVT variations when operating at ULV and compares them qualitatively. These techniques are depicted in Fig. 3.1.

Conventional digital designs, i.e., operating at nominal supply voltage (or close to it) and thus in superthreshold regime, mostly rely on *independent clock and supply regulations* [Fig. 3.1(a)] and the devices variability is usually covered with *fixed design margins* by ensuring correct timing closure at the worst-case PVT corner. These margins can be taken by applying a higher supply voltage, a lower clock frequency, or a stronger fixed FBB biasing. At ULV however, the PVT sensibility is exacerbated. Table 3.1 illustrates this point by presenting the impacts of PVT on the logic delay and leakage. Typical NMOS/typical PMOS (TT), fast NMOS/fast PMOS (FF), and slow NMOS/slow PMOS (SS) process corners are considered, together with $\pm 10\%$ of supply voltage variation, and a temperature range between -40 and +85°C. Compared to nominal conditions, the worst-case delay is increased by 6.4× and the worst-case leakage current by 33.72×. This exacerbated PVT sensibility imposes excessive guard bands, as shown in Table 3.2, whose overheads annihilate the gains expected from voltage scaling [13,17]. Instead, adaptive techniques have the ability to minimize these design margins.

A first popular technique is *adaptive voltage scaling* (AVS) [63,64]. It requires sensors embedded in the ULV domain, placed alongside the digital circuit to be adapted, in order to determine which operating conditions (fast or slow) are experienced. As illustrated in Table 3.3, the supply voltage is then dynamically adapted by an appropriate control of the voltage regulator. The voltage regulator is thus placed in a closed-loop involving the ULV domain [Fig. 3.1(b)] and typically requires a high power conversion efficiency and a large voltage range [65].

Similarly, the *adaptive back-biasing* (ABB) technique tunes the back-bias (BB) voltages (BBN and BBP for NMOS and PMOS transistors, respectively) instead

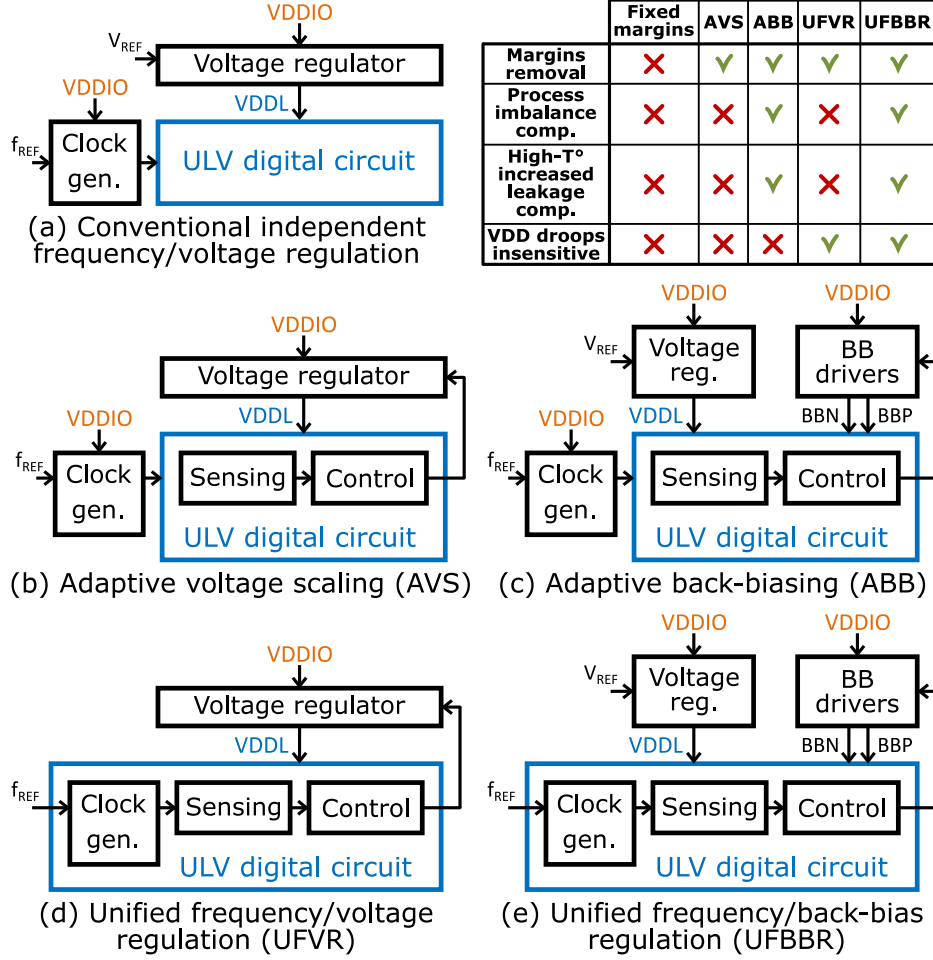


Fig. 3.1 Common techniques to ensure robustness against a wide range of PVT conditions. Note that the control part of (b)-(e) is represented inside the ULV domain but could in practice be supplied at a higher voltage.

of the supply voltage which is assumed fixed [Fig. 3.1(c)], and requires the use of FDSOI technology [19–21]. The adaptive closed-loop regulation now involves BB drivers to dynamically generate appropriate BBN/BBP voltages from the ULV sensors. When using FBB with low- V_{th} (LVT) flipped-well devices [16], BBP is negative, which imposes the use of switched-capacitor charge-pumps (SCCPs) to generate it on-chip the need of an external negative supply voltage [20].

Both AVS and ABB techniques reduce the design margins required to ensure robustness across a wide range of PVT conditions, with limited overheads compared to fixed margins. However, ABB comes with two important advantages compared to AVS. Firstly, ABB has the capability to extend the PVT compensation range to the correction of N/PMOS process imbalance due to asymmetric skewed process corners (FS and SF), by tuning the BB voltages in an asymmetric manner. Mismatch between NMOS and PMOS devices is indeed a serious concern for ULV digital

Table 3.2 Impacts of using static margins on the supply voltage (0.47 V instead of 0.40 V) to cover process, voltage, and temperature (PVT) variations. Results obtained from SPICE simulations of low- V_{th} inverter chains in 28-nm FDSOI, with $BBN = +1$ V and $BBP = -2$ V. SS, TT and FF processes are considered.

Process	Voltage	Temperature	Normalized delay	Normalized leakage
SS	0.47 V	-40°C	1×	0.01×
TT	0.47 V	+25°C	0.54×	1.20×
FF	0.47 V	+85°C	0.35×	36.22×

Table 3.3 Impacts of using the adaptive voltage scaling (AVS) technique to cover process, voltage, and temperature (PVT) variations. Results obtained from SPICE simulations of low- V_{th} inverter chains in 28-nm FDSOI, with $BBN = +1$ V and $BBP = -2$ V. SS, TT and FF processes are considered.

Process	Voltage	Temperature	Normalized delay	Normalized leakage
SS	0.47 V	-40°C	1×	0.01×
TT	0.40 V	+25°C	1×	1×
FF	0.32 V	+85°C	1×	25.37×

circuits due to its numerous impacts: pulse width degradations [66–68], noise margins reductions, increase of the minimum operating voltage and leakage energy per cycle [69], and increase of crosstalk noise [70]. The use of asymmetric FBB can compensate these effects [69,71], in which case the N/PMOS process imbalance must also be sensed and corrected. Secondly, the AVS technique fails at compensating for the leakage increase at high temperature, despite a small reduction of the supply voltage [72] (see also Table 3.3). Only the ABB strategy is able to compensate for both the low-temperature delay increase and the high-temperature leakage increase [73]. Nonetheless, as the clock generation is out of the ULV domain for both AVS and ABB systems, they are both sensitive to sudden voltage droops, because the clock generator is unaware of the dynamic variations experienced by the ULV logic.

To tackle this last issue, the *unified frequency/voltage regulation* (UFVR) technique has been proposed [Fig. 3.1(d)] and extends AVS by combining it with clock generation [72,74]. The clock is generated by a tunable ring oscillator (TRO) lying in the ULV domain and becoming the logic speed sensor of the AVS regulation scheme. In other words, the TRO period tracks the PVT-induced variations of the delays in the logic. Because the delays in the critical paths of the logic and in the TRO vary in a similar way, the UFVR technique gives robustness against fast supply voltage droops [13,72,74]. As for AVS systems however, the UFVR technique cannot compensate for N/PMOS process imbalance nor the high-temperature increased leakage.

We propose a new adaptive technique, named *unified frequency/back-bias regulation*

(UFBBR) [Fig. 3.1(e)], which takes inspiration from UFVR systems and combines the ABB-based PVT compensation technique with the clock generation [JP3, CP2]. Note that a back-bias-controlled oscillator (BBCO) must be used as TRO. The UFBBR technique takes the best of ABB and UFVR worlds, by i) being able to correct the N/PMOS process imbalance, ii) compensating for the increased leakage due to high temperatures, and iii) being robust to fast supply voltage droops. All these reasons justify the choice of implementing UFBBR units in this work. Two UFBBR versions are presented in the next sections.

In addition to these different adaptive regulation strategies, there is a variety of sensing approaches for speed and imbalance. Information about the *logic speed* can for instance be obtained from timing error detectors [64, 75, 76], critical path replicas and process monitors built with delay-lines [21, 63] or ring oscillators [72, 77–79]. Tunable ring oscillators are favored in UFVR/UFBBR systems for the clock generation [JP3, 74, 80–83]. On the other hand, most *process imbalance* sensors for ABB/UFBBR systems are analog and based on a comparison of N/PMOS I_{on} currents (taken at $|V_{GS}| = V_{DD}$) [84] or I_{eff} ones (taken at reduced V_{GS} and V_{DS} , as done in Section 2.4.2) [85]. In this chapter, we propose digital alternatives based on delay-lines (see Section 3.3.2) or ring oscillators (see Section 3.4.2.1). Finally, several works also add *thermal* sensors [21, 77].

3.3 First Generation of UFBBR Prototype

In this part, we describe our first UFBBR prototype. As represented in Fig. 3.2, it is embedded in SleepRunner, a custom highly-integrated ULP MCU SoC in 28-nm FDSOI, previously introduced in [JP3]. SleepRunner embeds an ARM Cortex-M0 processor with a custom 32-kB ULP FBB-compatible SRAM memory and a high-density (HD) 32-kB foundry SRAM memory, a fast Fourier transform (FFT) accelerator, and several digital interfaces. Switched-capacitor voltage regulators (SCVRs) generate all internal supplies from a single 1.8-V supply voltage.

This part is structured as follows. Section 3.3.1 introduces the proposed UFBBR architecture. Section 3.3.2 focuses on the design of its process imbalance sensor. Finally, Section 3.3.3 presents measurement results.

3.3.1 Proposed Dual-Loop UFBBR Architecture

This section describes the architecture of our first UFBBR generator. Its primary goal is to compensate for PVT variations, which affect both logic speed and N/PMOS imbalance, using asymmetric ABB. At the same time, the UFBBR is responsible for the generation of the main system clock (MCLK) in active mode. The default frequency is 64 MHz, but is made programmable to span from 40 to 80 MHz. The UFBBR circuit thus adapts BBN and BBP to the operating conditions and to the target clock frequency. The regulation of BBN (resp. BBP) covers a range going from 0 to +1.8 V (resp. from 0 to -3 V), with a nominal value of 1 V (resp.

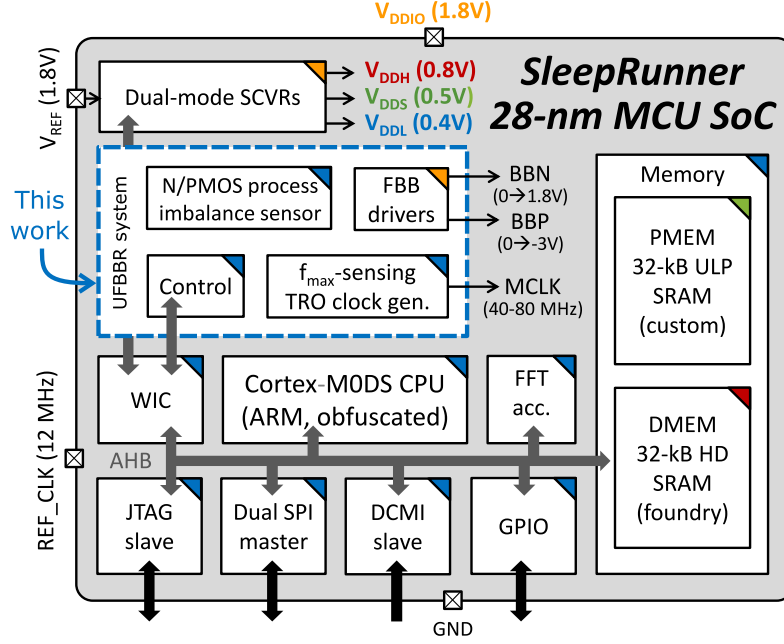


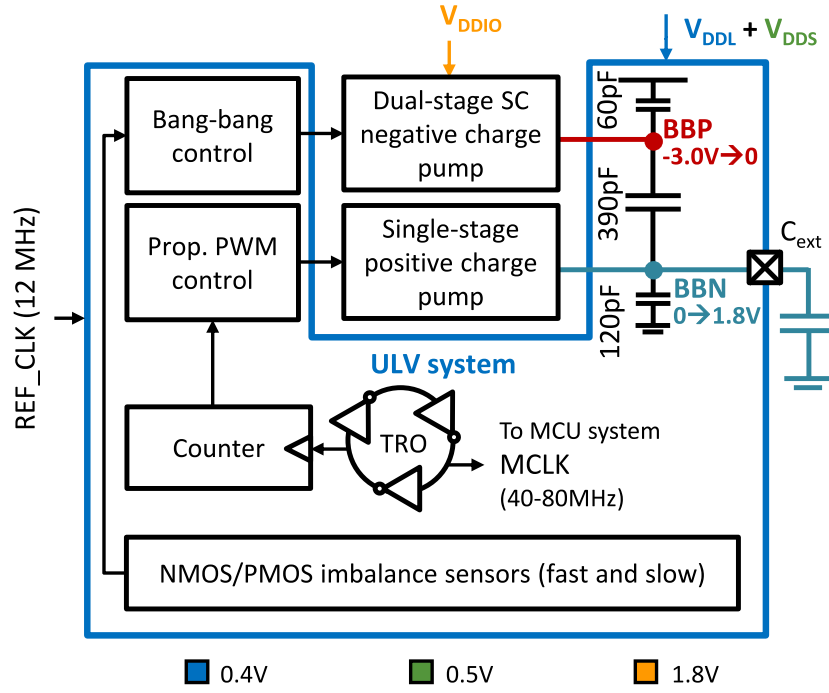
Fig. 3.2 SleepRunner MCU SoC architecture embedding our first UFBBR prototype [JP3].

-2 V). In sleep mode, the MCLK generation is disabled and BB voltages are driven towards 0 V. Besides, fast transitions between sleep and active modes are needed to minimize the wake-up energy overheads. We target a wake-up time below 20 μ s in this work. These specifications come from system-level considerations described in [JP3].

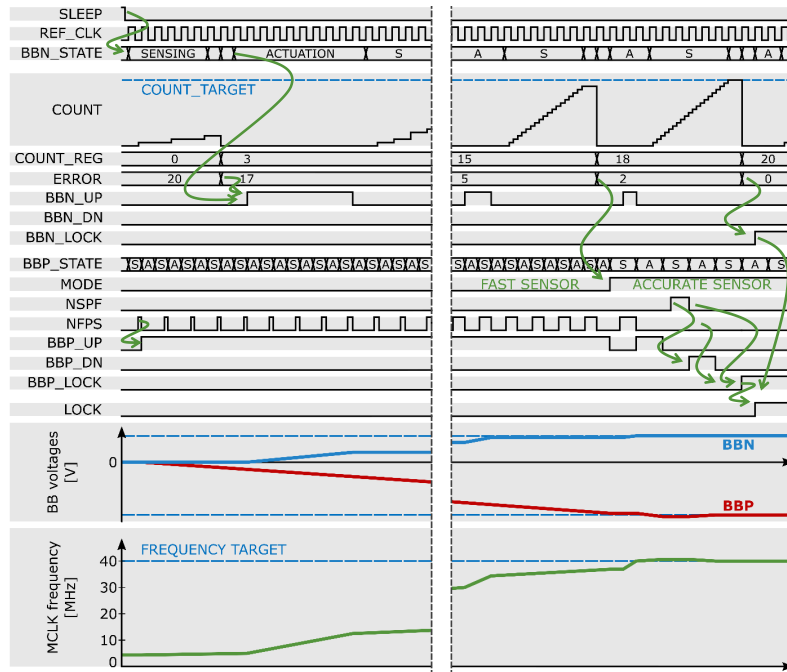
The proposed UFBBR architecture is represented in Fig. 3.3(a). It comprises two distinct feedback loops: a *frequency-locked loop* (FLL) regulates BBN while a *delay-locked loop* (DLL) tunes BBP.

In the BBN FLL, a BBCO serves as TRO and simultaneously acts as MCLK generator and logic speed sensor. The functional timing diagram of Fig. 3.3(b) illustrates the UFBBR regulation steps. Firstly, a counter senses and digitizes the TRO frequency during six REF_CLK cycles. As seen in Fig. 3.2, REF_CLK is an externally-provided 12-MHz reference clock. Secondly, a proportional controller actuates BBN in a pulse-width modulated (PWM) mode by activating a current charge pump (CP) during a variable number of REF_CLK cycles.

As far as the BBP DLL is concerned, it consists of N/PMOS process imbalance sensors (PISs) and a bang-bang controller. In order to cover a voltage range between 0 and -3 V, the BBP actuator comprises a two-stages cross-coupled *switched-capacitor charge pump* (SCCP) and a two-stages *switched-capacitor discharge pump* (SCDP), according to the voltage doubler topology [20].



(a) Proposed architecture.



(b) Functional timing diagram at wake-up.

Fig. 3.3 Description of the first version of UFBBR.

All constitutive blocks used for sensing (BBCO and PISs) and control are made of standard cells and share the ULV supply (0.4 V) with the MCU digital logic, to ensure a good matching with the logic to be calibrated. The BB drivers are using I/O transistors supplied at 1.8 V to achieve wide-range BBN (from 0 to 1.8 V) and BBP (from 0 to -3 V). Level shifters are used to go from the ULV to the 1.8-V power domain but are not shown in the block diagram of Fig. 3.3.

The UFBBR system generates BBN and BBP for both the ULV logic (supplied at 0.4 V) and the ULP SRAM (supplied at 0.5 V). These parts account for a significant portion of the MCU area, which translates into a significant capacitive load for the UFBBR. Indeed, as discussed in Chapter 2, there is a strong parasitic coupling existing between BBN and BBP nodes when sharing the deep N-well between NMOS and PMOS LVT devices.

With an estimated value of 390 pF, this BBN/BBP parasitic coupling capacitance is large enough to create parasitic charge injections between BBN and BBP nodes. This situation makes the dual loop unstable: when the FLL tries to increase the TRO frequency by pumping positive charges on BBN, it results in a spurious BBP charge up, which counteracts the TRO frequency increase; similarly, when the DLL tries to decrease BBP for balancing the N/PMOS imbalance, it results in a spurious BBN charge down, counteracting the imbalance correction; the parasitic coupling capacitance makes the FLL and DLL loops counteract each other, in a sense. It is important to understand that, unlike the custom transistor-level design proposed in Chapter 2, the prototypes of this chapter involve standard cells in which the deep N-well sharing and associated parasitic capacitances are not avoidable. Digital standard cells are required for the processor and MCU logic.

For this first UFBBR prototype, we adopt a simple solution to this issue: we add an external capacitor on BBN, large enough to stabilize the dual-loop system. However, the capacitor should not be too large neither, to avoid excessive energy overheads associated with its charge/discharge when transitioning from sleep to active mode and conversely. We stabilize BBN and not BBP because BBN has a lower voltage swing than BBP, which thus results in a lower wake-up/going-to-sleep energy. The added decoupling capacitor adds inertia to BBN. In a sense, it favors the frequency-regulation FLL with respect to the imbalance-corrective DLL.

Fig. 3.4(a) shows the UFBBR wake-up with external decoupling capacitance values from 0.5 to 2 nF. Low capacitance values lead to overshoot because of low stability. Increasing the capacitance value to 2 nF kills the overshoot, which actually reduces the wake-up energy by 10% despite the larger switched capacitance. Fig. 3.4(b) also shows that the proposed architecture can generate independent asymmetric BBN/BBP voltages to compensate for skewed process corners.

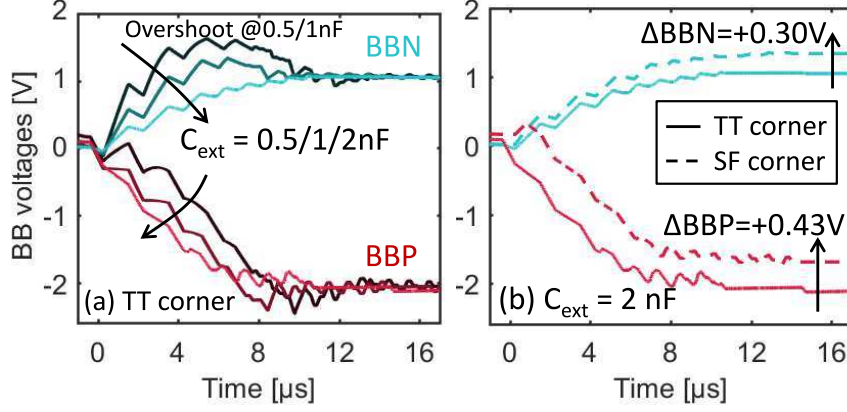


Fig. 3.4 Simulated UFBBR start-up sequences: (a) influence of the external BBN decoupling capacitor value on locking time and overshoot, (b) illustration of the compensation of a slow NMOS/fast PMOS (SF) skewed process corner.

3.3.2 Proposed Process Imbalance Sensors

In this section, we describe the N/PMOS process imbalance sensors (PISs) used in our UFBBR system.

Most PISs proposed in the literature are based on analog N/PMOS current comparison, which leads to a hard trade-off between DC power and response time [34, 78]. For the BBP DLL of the UFBBR system, we rather propose a digital PIS to overcome this challenge. The PIS only uses digital standard cells for a good correlation with the MCU logic to be calibrated. Fig. 3.5(a) shows the sensor schematic. Binary information on the process imbalance is extracted by comparison of the propagation delay of two delay lines (DLs), respectively sensitive to NMOS and PMOS logic delay.

To obtain this N/PMOS sensitivity, the DLs are built with delay stages made of alternating strong ($\times 38$) and weak ($\times 2$) logic cells and stimulated with a particular edge type (either rising or falling edge). Consequently, the time taken by weak cells (low current, low parasitic capacitances) to charge the stronger ones (high current, high parasitic capacitances) dominates the total DLs delay. In that manner, we obtain a selective sensitivity $3\times$ higher to NMOS V_{th} variations (9%/10 mV) than to PMOS V_{th} variations for the NMOS-sensitive delay line, and vice-versa, as demonstrated in Fig. 3.5(b). The figure also shows that using NAND2/NOR2 gates with shorted inputs as weak cells in NMOS- and PMOS-sensitive DLs, respectively, further improves their respective selective sensitivity thanks to transistor stacking.

However, due to mismatch, particularly in the weak cells, strong die-to-die closed-loop BBP variability can be induced, which can translate in significant leakage overhead. By increasing the number of delay stages in the DLs, this effect can be

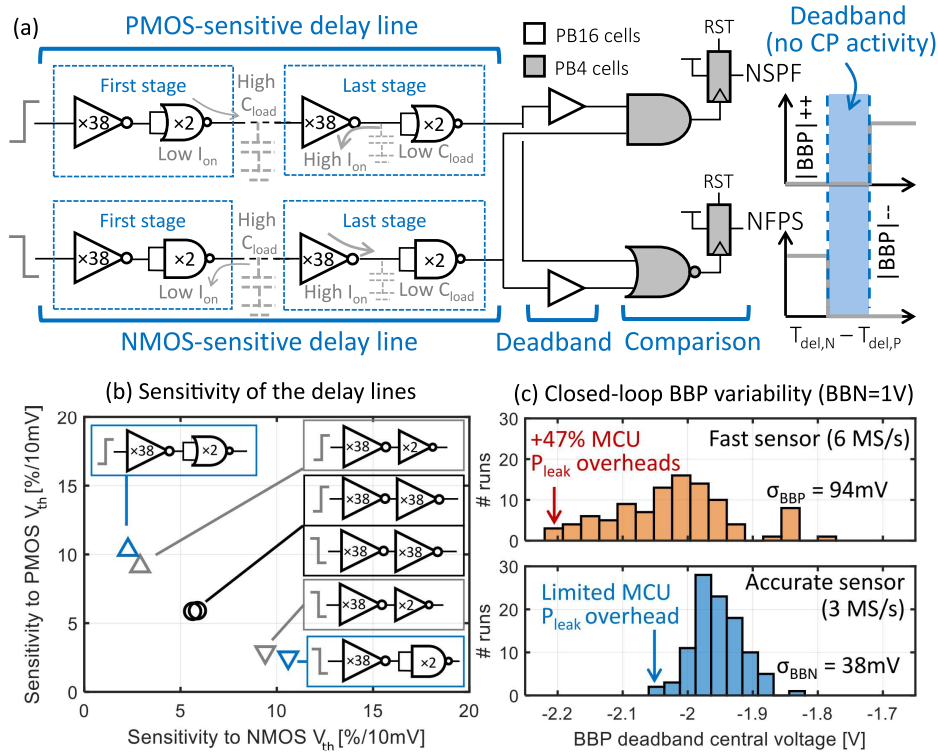


Fig. 3.5 Proposed N/PMOS imbalance sensor: (a) schematic, (b) sensitivity to NMOS/PMOS independent V_{th} variations and (c) die-to-die variability of the closed-loop BBP voltage (100-run Monte Carlo SPICE simulation results at TT corner, 25°C).

limited thanks to averaging at the cost of sensing speed. This is the reason two versions of PISs are used in practice in our UFBBR design: a fast but inaccurate sensor with a low number of stages is used for a fast start-up, and an accurate but slower sensor with a higher number of stages is used for better locking. Fig. 3.5(c) shows their respective closed-loop BBP variability. The fast and accurate sensors can be sampled up to 6 and 3 MS/s, respectively, therefore significantly improving the loop response time compared to the state of the art, e.g., 200 μ s in [78].

Finally, by adding additional delays in the sensor comparison logic, we create a small dead-band in the accurate sensor, to avoid spurious CP activity due to the bang-bang control in the BBP DLL while in lock, and thus reduce the associated active power overhead.

3.3.3 Prototyping and Measurement Results

This section presents experimental results concerning our first UFBBR prototype. We start by verifying the UFBBR functionality, before validating its temperature compensation capability between -40 and $+85^{\circ}$ C.

The proposed UFBBR is embedded in SleepRunner MCU SoC, which was proto-

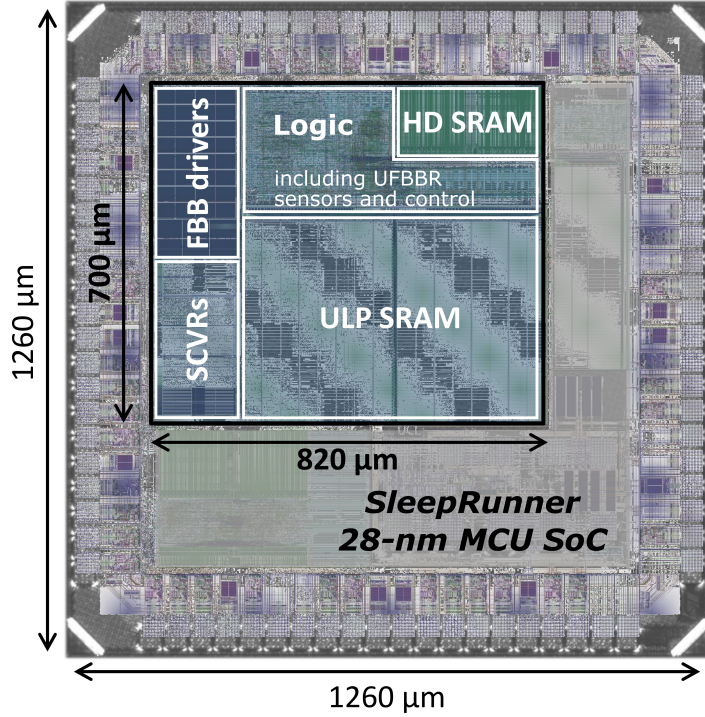


Fig. 3.6 Die microphotograph of SleepRunner with post-shrink dimensions.

typed in 28-nm FDSOI technology. Fig. 3.6 shows the 1.6-mm^2 die microphotograph. The MCU area is below 0.6 mm^2 including all digital and mixed-signals blocks from Fig. 3.2. The UFBBR unit occupies an area of less 0.060 mm^2 .

3.3.3.1 Closed-Loop Behavior

Fig. 3.7(a) shows the typical UFBBR transitions between active and sleep modes and vice-versa. A divided-by-64 version of `MCLK` is visible together with the corresponding `BBN` and `BBP` voltages. At wake-up, the closed-loop UFBBR system locks in less than $10\text{ }\mu\text{s}$, with `MCLK` stabilizing at 64 MHz and `BBN`/`BBP` stabilizing at around $+0.75/-1.8\text{ V}$, respectively. The total MCU wake-up time is less than the $20\text{-}\mu\text{s}$ target.

The time required to go to sleep mode is similar. `BBN` is quickly discharged to 0 V by its CP. For `BBP`, it takes more time to drive it towards 0 V. This comes from the `BBP` actuation, which is gated after a few μs . Indeed, as the `BBP` SCCP is not a static circuit, it cannot be kept active in sleep mode for power concern. This is not an issue as the leakage is dominated by NMOS transistors in sleep mode and the impact of incomplete `BBP` discharge does not significantly affect the leakage power. Note that in sleep, the TRO-generated `MCLK` is disabled: the visible 750-kHz clock in Fig. 3.7 corresponds to a divided-by-16 version of `REF_CLK`.

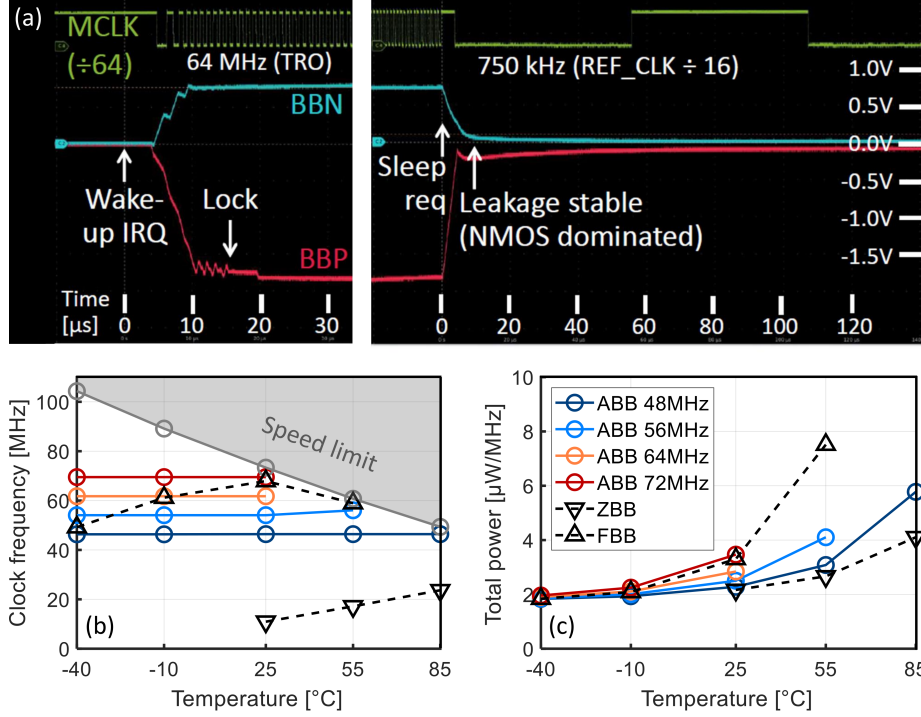


Fig. 3.7 UFBBR system measurement results: (a) wake-up and going-to-sleep power mode transitions, (b) generated frequency and (c) active power as a function of the temperature.

The short mode transition times demonstrated here are very competitive compared to previous designs using adaptive FBB in closed loop (200 μ s in [34], 200 μ s in [78]). Let us mention that this time depends on the biased load area, which is around 0.4 mm² in this chip.

3.3.3.2 Temperature Compensation Capability

The functionality of the UFBBR unit has been tested at temperatures ranging from -40 to +85°C. The corresponding measurement results are shown in Figs. 3.7(b)-(c).

Fig. 3.7(b) shows the MCLK frequency as a function of temperature. The ABB generation provided by the UFBBR for several target frequencies is compared to static zero back bias (ZBB) and static asymmetric FBB (BBN = 1 V, BBP = -2 V). The application of static external FBB can be seen as fixed design margins (as discussed in Section 3.2).

With both ZBB and static asymmetric FBB, the MCLK frequency generated by the TRO decreases significantly when lowering the temperature, resulting from the associated V_{th} increase [46]. However, with static FBB, the MCLK frequency also drops above +25°C. At +85°C, the MCU is even not functional anymore with static

FBB because robustness issues appear. We can attribute this to prohibitive resistive drops due to excessive leakage current and/or undersized power rails, for instance. Moreover, we observe a degradation of the absolute maximum frequency with the temperature increase, even with ABB, as represented in Fig. 3.7(b) with the gray shaded area. Once again, we can attribute this to prohibitive IR drops.

In any case, Fig. 3.7(b) shows that the MCU remains functional over a wide temperature range when using the adaptive FBB generated by the UFBBR system. The UFBBR also preserves the target frequency over this temperature range.

Fig. 3.7(c) shows the evolution of the power consumed by both the digital logic and the ULP SRAM as a function of the clock frequency. When using a static asymmetric FBB, the power explodes at high temperature because of the leakage power that becomes dominant. Unlike AVS/UFVR techniques [72] (see Section 3.2), the adaptive FBB generation provided by our UFBBR is capable of keeping the active power constant at low temperatures. It also significantly limits the active power overhead of high-temperature operation compared to static FBB. For instance, at $+55^{\circ}\text{C}$, an energy level of $3\text{--}4\text{ }\mu\text{W}/\text{MHz}$ is enabled by adaptive FBB versus $7.5\text{ }\mu\text{W}/\text{MHz}$ for static FBB. Of course, static ZBB also preserves very low active power up to $+85^{\circ}\text{C}$ but this comes at the cost of lower and uncontrolled clock frequency and even functional failure at low temperature, as shown in Fig. 3.7(b).

There is a final limitation to be discussed concerning this first UFBBR prototype. Indeed, at extremely low temperatures, the delay in the DLs of the PISs is too large at start-up. Consequently, the BBP actuation cannot start correctly at these temperatures. Without actuation, BBP is even reaching positive values (due to the coupling with BBN), further increasing the delays in the PISs. To obtain the low-temperature measurements in Figs. 3.7(b)-(c), we thus had to start the chip at, e.g., $+25^{\circ}\text{C}$ before lowering the temperature. This is a clear robustness issue and the second UFBBR prototype avoids it by relying on ring oscillators instead of DLs in its PISs, as explained in next section.

3.4 Second Generation of UFBBR Prototype

In this section, we present a second version of UFBBR. It is an enhanced version of the first UFBBR prototype described in last section, sharing similar specifications and implementation aspects but also diverging in several ways.

As represented in Fig. 3.8, our second UFBBR prototype is a key component of SleepRider, another custom highly-integrated ULP MCU SoC in 28-nm FDSOI, previously introduced in [CP2]. SleepRider embeds an ARM Cortex-M4 processor with two custom 16-kB FBB-compatible SRAM memories, two high-density (HD) 32-kB foundry SRAM memories, an analog front-end (AFE), and several digital interfaces. Switched-capacitor voltage regulators (SCVRs) generate all internal

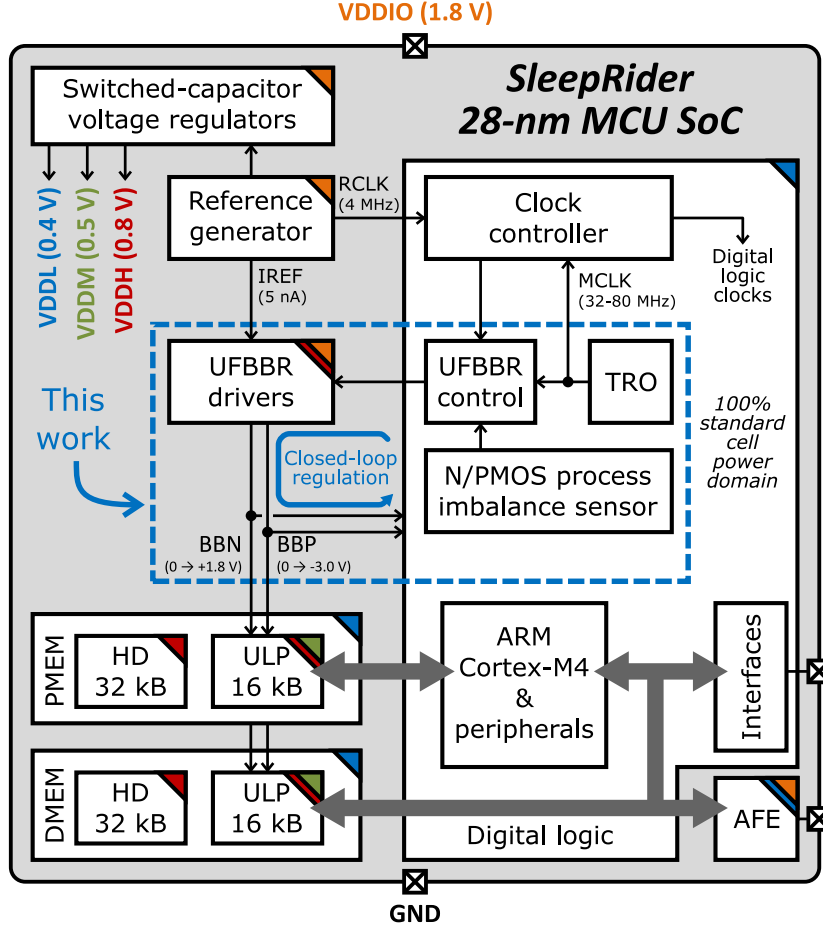


Fig. 3.8 SleepRider MCU SoC architecture embedding our second UFBBR prototype [CP2].

supplies from a single 1.8-V supply voltage.

This part is structured as follows. Sections 3.4.1 and 3.4.2 respectively present the proposed UFBBR architecture and its design. Section 3.4.3 then provides the corresponding continuous-time model of the entire UFBBR unit. Finally, Section 3.4.4 presents extensive measurement results.

3.4.1 Unified Dual-Output UFBBR Architecture

In this section, we describe the architecture of our second UFBBR generation. We start by defining its block-level specifications and the specific constraints it encounters.

This second UFBBR design shares similar specifications with the first version presented in Section 3.3. Its primary goal is also to compensate for PVT variations while being responsible for the generation of the main system clock (MCLK) in active mode. The default frequency is 64 MHz and is made programmable to span from

32 to 80 MHz. As for the previous UFBBR design, the regulation of BBN (resp. BBP) covers a range going from 0 to +1.8 V (resp. from 0 to -3 V), with a nominal value of 1 V (resp. -2 V) in active mode. In sleep mode, the MCLK generation is disabled and BB voltages are driven towards 0 V. We once again target a wake-up time below 20 μ s in this work. As a reminder, these specifications come from system-level considerations described in [JP3].

As can be seen in Fig. 3.8, the BB voltages are provided to both the digital logic (supplied at 0.4 V) and to the custom ULP FBB-compatible SRAM memories (supplied at 0.5 V). Due to the parasitic well capacitances, this translates again into a significant capacitive load for the UFBBR. As in the first version, this new UFBBR experiences the following challenge: there is a strong parasitic coupling existing between BBN and BBP nodes, which comes from the deep N-well sharing between NMOS and PMOS devices, and threatens the closed-loop stability. From post-layout parasitic extractions and extrapolations from the first UFBBR prototype (see Section 3.3), the BBN/BBP coupling capacitance is estimated around 462 pF. For this second UFBBR prototype, we set an additional objective, which is to ensure a stable closed-loop behavior without using any external component.

This new objective constitutes a challenging task, especially for an architecture based on a phase-locked loop (PLL). Due to the unavoidable existence of these parasitic capacitances¹, stabilizing a PLL with a conventional lead-lag low-pass filter would indeed require at least 5 nF of on-chip capacitor. Assuming an optimistic density of 4 fF/ μ m² using metal-oxyde-metal capacitors, this translates to at least 1.25 mm² of silicon area. In addition, to cover the 32-to-80 MHz frequency range and guarantee 20 μ s of maximal wake-up time, the PLL charge-pump current must be above 1.2 mA.

Instead of a PLL, this new UFBBR unit consists of a *unified dual-output frequency locked-loop* (FLL), as depicted in Fig. 3.9. This type of topology is stable without the need for additional on-chip filtering nor off-chip capacitors (see Section 3.4.3). The constraint related to the actuation current is also relaxed. Besides, phase lock is not really needed here, only frequency locking. The UFBBR can be seen as the superposition of two separated FLLs, the first one adapting the logic speed to the operational conditions, the second loop correcting the N/PMOS imbalance.

BBCOs followed by asynchronous counters are used as sensors. A TRO serves as clock generator as well as logic speed sensor. N/PMOS imbalance is sensed from the frequency difference at the output of N/PMOS-sensitive ring oscillators (ROs). The sensors outputs are sampled at a rate of 4 MHz given by a reference clock (RCLK). A controller follows the sensors and combines their output to generate adequate control signals for the BB drivers. The target frequency (through FMULT) as well as the proportional loop gains (G_f , G_i , G_n , and G_p) are all configurable

¹As a reminder, the prototypes of this chapter involve the use of standard cells, for which the deep N-well sharing and the associated parasitic capacitances cannot be avoided.

in software by the processor unit through memory-mapped registers. Gains G_n and G_p are used to match the BB drivers strengths, while G_f and G_i control the gain of the frequency- and imbalance-regulation loops, respectively. This gives flexibility and adaptability to a wide range of operating conditions. The BB drivers consist of digitally-controlled oscillators (DCOs) followed by switched-capacitor charge-pumps (SCCPs) to perform fast proportional current actuation on a wide voltage range.

Most parts of the UFBBR lie in the ULV 0.4-V domain and are made of standard cells, ensuring a good correlation and a deep integration with the digital logic. The UFBBR drivers being analog, they are the only parts designed at the transistor-level and using higher supply voltages: the DCOs are supplied at 0.8 V while the SCCPs lie in the 1.8-V domain.

The UFBBR is a dual-output system because it simultaneously adapts the circuit speed as well as N/PMOS imbalance. In other words, it minimizes two error signals: **freq_err** and **imbl_err** for frequency and imbalance regulation, respectively.

Firstly, the *frequency-regulation FLL* tends to minimize **freq_err** by actuating *symmetrically* on BBN and BBP. For instance, a positive **freq_err** value means the circuit is not fast enough. It leads to an increase of the absolute value of both BBN (becoming more positive) and BBP (becoming more negative), thus going deeper in the FBB regime to make both NMOS and PMOS devices faster.

Secondly, the *imbalance-regulation FLL* tends to minimize **imbl_err** by actuating *asymmetrically* on BBN and BBP. A positive **imbl_err** value means that PMOS devices are faster than NMOS ones. This is corrected with an increase of the absolute value of BBN (becoming more positive) and in a decrease of the absolute value of BBP (becoming less negative), thus balancing the strength of NMOS and PMOS devices.

In this second UFBBR version, both feedback loops thus act on both BBN and BBP (unlike the BBN FLL and the BBP DLL of the first version which are dedicated to the BBN and BBP generation, respectively, as explained in Section 3.3). This architectural feature, together with matched BBN/BBP actuation paths, explain the stability and tolerance to the parasitic BBN/BBP coupling capacitance achieved with this second UFBBR generation.

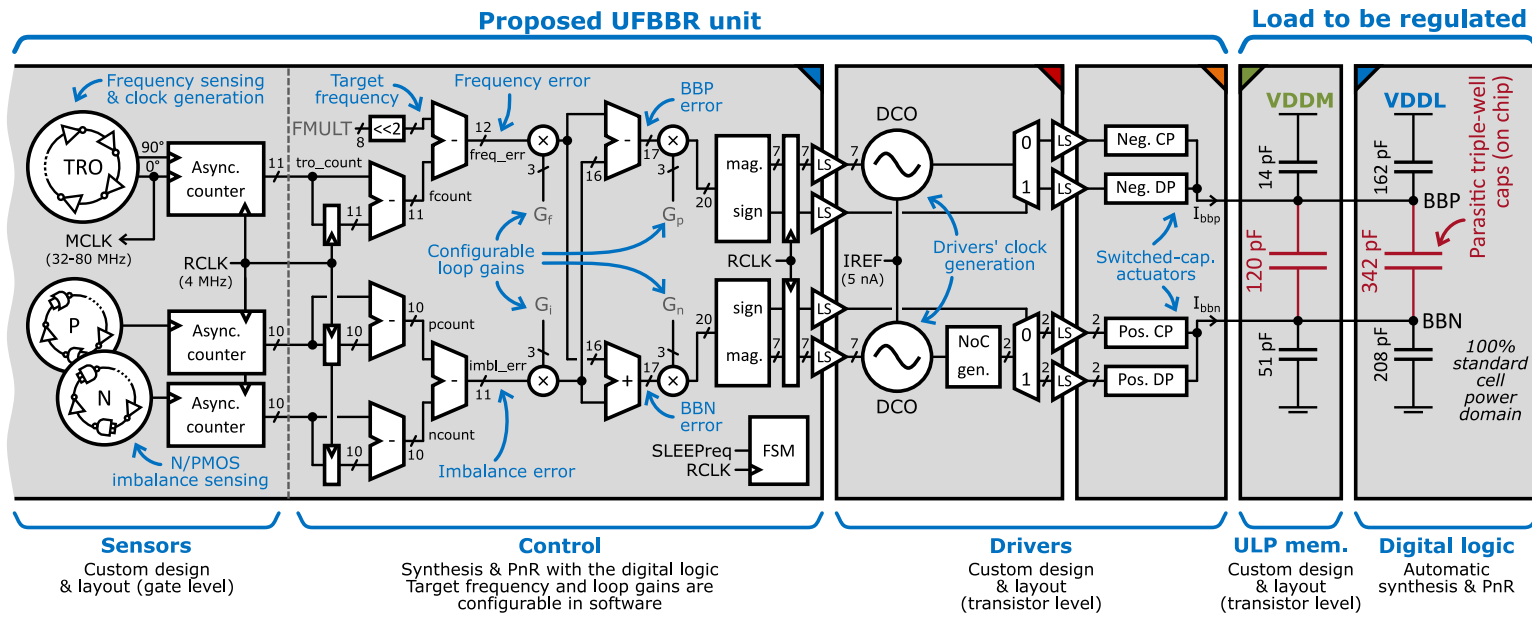


Fig. 3.9 Proposed architecture for the unified frequency and back-bias regulation (UFBBR) unit.

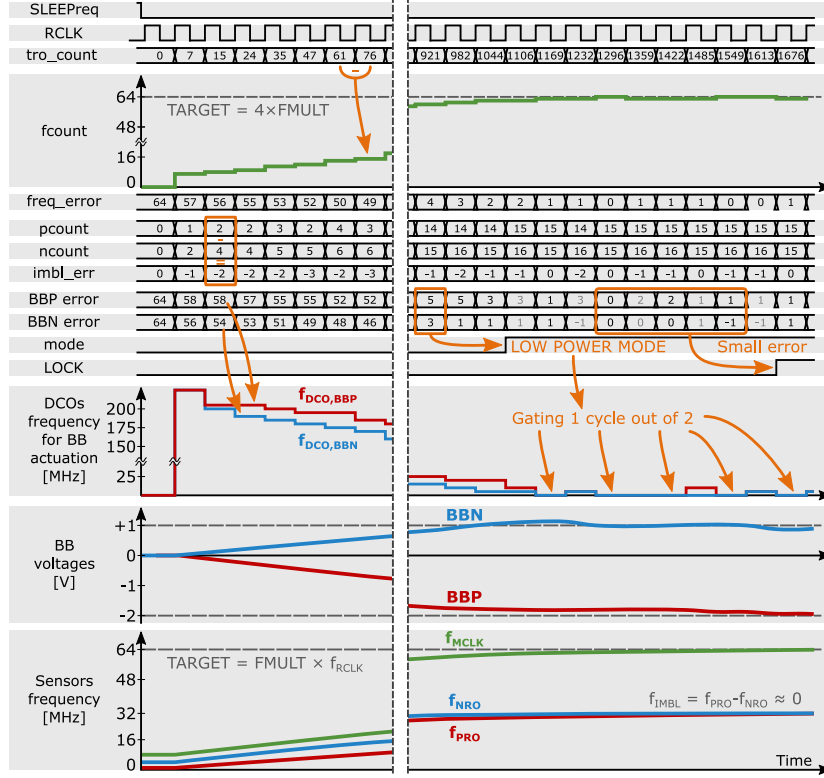


Fig. 3.10 Functional timing diagram showing the UFBBR operation at wake-up.

A functional timing diagram during the wake-up of the UFBBR is represented in Fig. 3.10. As soon as the sleep request is going low, the sensors are enabled and the asynchronous counters start being continuously incremented. Their output is then sampled by RCLK. A difference operation is performed on two successive counter samples to retrieve the frequency information (from `tro_count`).

The frequency error signal `freq_err` is obtained by comparison between the TRO frequency count increment `fcount` and the desired count target $4 \times FMULT$, with `FMULT` being the desired multiplicative factor from RCLK to MCLK frequency. The factor $4 \times$ comes from the frequency sensing resolution which is increased by 2 bits, as explained in Section 3.4.2.1.

Similarly, the imbalance error signal `imbl_err` is obtained after subtracting the NMOS-sensitive BBCO count increment from the PMOS-sensitive one, to measure the frequency difference at the output of these process-sensitive ROs. Separate error signals are then obtained for BBN and BBP actuation, by addition and subtraction of `freq_err` and `imbl_err`. The larger the BB error, the larger the corresponding DCO output frequency, and the larger the output current of the corresponding switched-capacitor actuator.

After some time, both BBN and BBP have increased (in absolute value) and the

corresponding MCLK frequency goes closer to the target. When the total error (sum of BBN and BBP error) goes lower than a given threshold, the UFBBR switches to a *low power mode*. As its name suggests, this mode enables power savings by gating the actuation one cycle out of two. According to our simulations, the actuation power is decreased by 24% at the cost of a limited jitter increase from $\sigma/\mu = 0.31\%$ to 0.48%. When the total error goes even lower and stays below a second threshold for at least five clock cycles, the UFBBR is finally considered as *locked*.

When entering sleep mode and to save leakage power, BBN is directly switched to 0 V while the negative BBP is actuated back towards 0 V during a programmable number of clock cycles `SLEEP_COUNT`. The MCLK generation is also disabled. This situation is not represented in Fig. 3.10 but is described in more details in Section 3.4.2.4.

3.4.2 UFBBR Design

After the general description of the UFBBR architecture given in Section 3.4.1, this part focuses on the design of the constitutive blocks of the UFBBR, from the sensors to the actuators. Closed-loop simulation results are also provided.

Furthermore, to ensure a stable behavior and ease the design phase, the UFBBR is also modeled in continuous-time in the Laplace domain thanks to a state-space representation. The full description of this model falls outside the scope of this work, but is briefly explained later, in Section 3.4.3.

3.4.2.1 Sensing Part

The UFBBR sensing part contains two different sensors: a *speed sensor* and a *process imbalance sensor* (PIS). Both of them are made of BBCOs followed by asynchronous counters. Their architecture is purely digital and built with standard cells, to have a good correlation with the digital logic to be calibrated. However, their design was done in a custom fashion, at the gate-level, and the cell placement as well as the routing were performed manually, for a fine control of the matching and of the wire lengths.

Taking inspiration from UFVR systems, a TRO is used simultaneously as the main clock MCLK generator and as speed sensor. The TRO architecture is represented in Fig. 3.11 and its frequency can be trimmed with 4-bit resolution via `NSEL`. To improve the sensing resolution, two matched clock phases (0° and 90°) are generated. A copy of the 0° phase is used as MCLK. The ring-connected delay line (DL) that constitutes the TRO consists in two different parts: a fixed delay portion built with NOR2/NAND2 standard cells for a good correlation with the digital logic, and an incremental delay portion of inverters for finer time resolution. The output frequency of the TRO is represented in Fig. 3.12 as a function of BBN and BBP voltages.

The N/PMOS imbalance sensor is also built from BBCOs. While it could rely upon DLs as in our first UFBBR prototype (see Section 3.3.2), using ROs instead

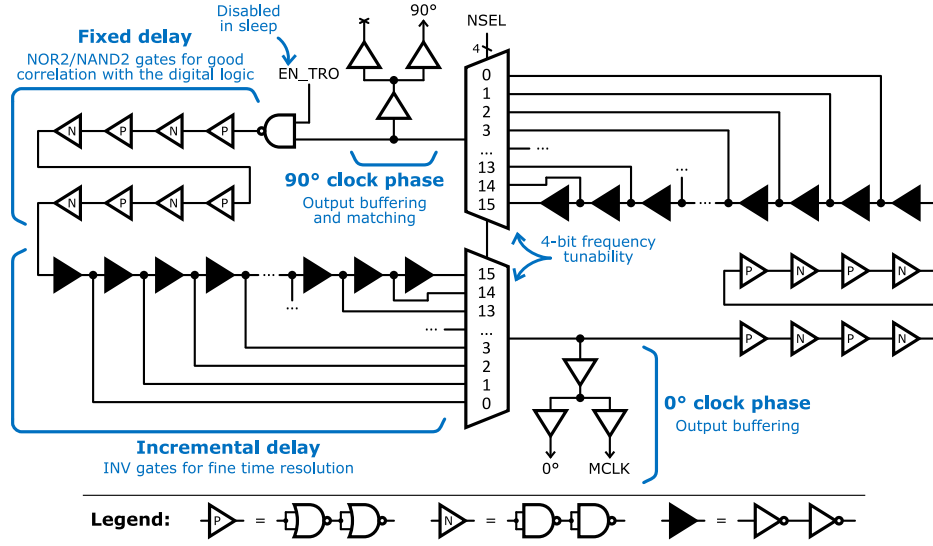


Fig. 3.11 Schematic of the tunable ring oscillator (TRO) simultaneously used as logic speed sensor and clock generator.

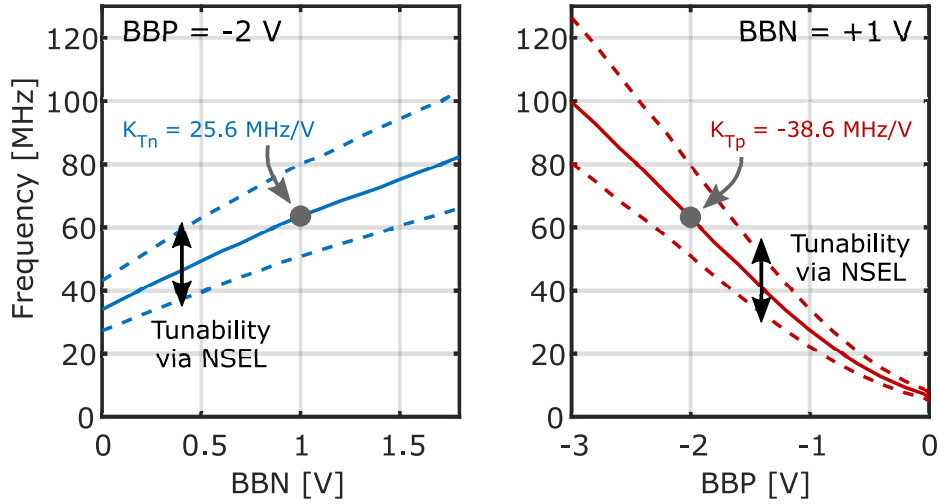


Fig. 3.12 Simulated transfer function of the tunable ring oscillator (TRO) versus BB voltages. At fixed BB voltages, the frequency can be tuned via NSEL.

brings several advantages. Namely, ROs can run continuously and autonomously, they do not need to be reset or fed with particular input edges as required by DLs. The sensed information can also simply be recovered with counters, as done for the frequency sensing. This contributes to have a good matching between the frequency- and the imbalance-regulation loops, as well as a good integration within the FLL-based UFBBR unit.

The PIS schematic is shown in Fig. 3.13. Its two constitutive ROs, namely PRO and NRO, are respectively made PMOS- and NMOS-sensitive. Reusing some

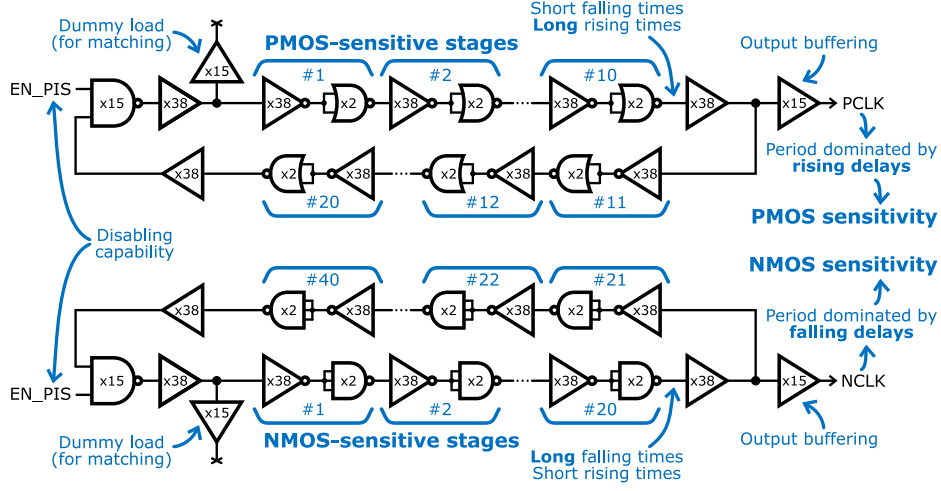


Fig. 3.13 Schematic of the N/PMOS process imbalance sensor (PIS). It uses two BBCOs, respectively sensitive to NMOS and PMOS transistors delays.

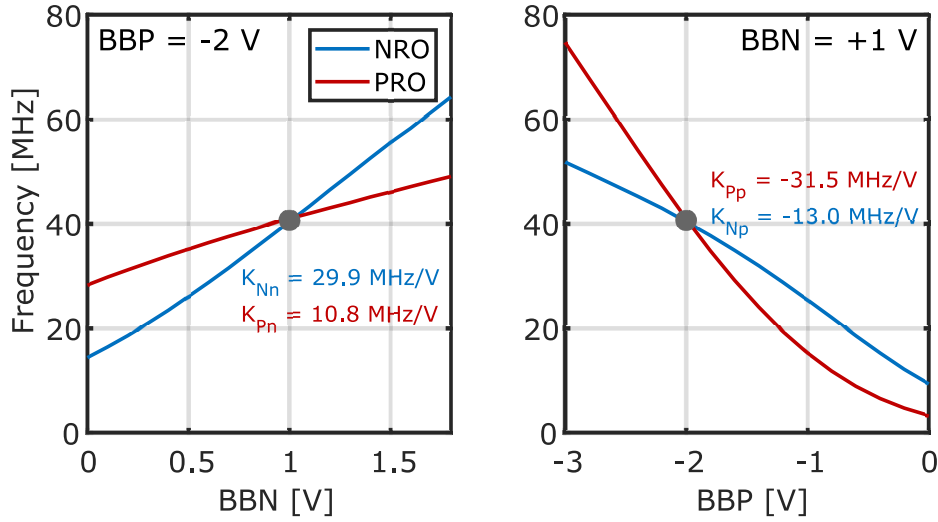


Fig. 3.14 Simulated transfer functions of the process-sensitive BBCOs of the process-imbalance sensor (PIS) versus BB voltages.

ideas of Section 3.3.2, this selective sensitivity is obtained by: i) alternating strong ($\times 38$) and weak ($\times 2$) driving cells, and ii) using NOR2 and NAND3 gates as weak cells to increase the respective sensitivity to PMOS and NMOS devices thanks to transistors stacking. Several stages in series are used in each ROs to decrease the variability by averaging. By comparing the output frequency of PRO and NRO, the imbalance-corrective loop can determine which type of device (PMOS or NMOS) is faster than the other and compensate for the imbalance. The oscillation frequencies of PRO and NRO are compared in Fig. 3.14 as a function of BBN and BBP voltages. Their frequency gains with respect to BBN and BBP showcase their selective sensitivity to either PMOS or NMOS devices.

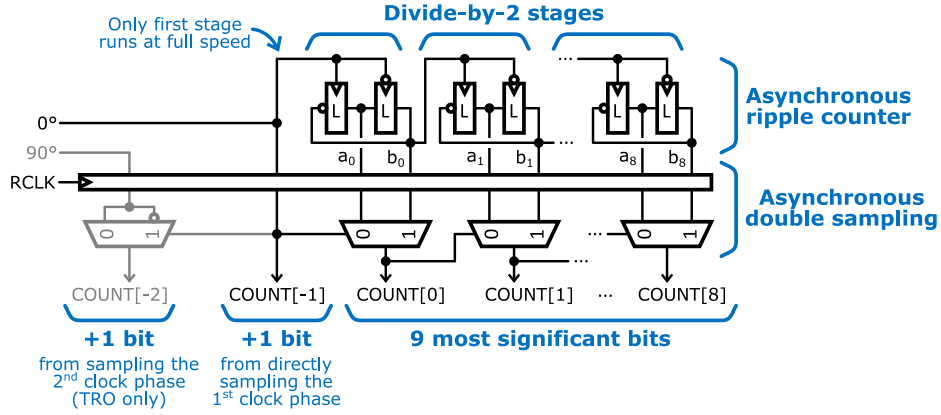


Fig. 3.15 Schematic of the asynchronous counters inspired from [86].

In order to be adequately used by the controller part, the sensed information obtained by the TRO and the PIS need to be digitized and sampled. This is done by asynchronous counters performing asynchronous double sampling. Their schematic is represented in Fig. 3.15 and is inspired from [86]. While being fast and energy efficient, this type of counter avoids metastability errors thanks to the double sampling technique. Two versions of the counter bits are made available by latching them on positive and negative edges of the input clock. This mechanism ensures that at least one of the two versions is stable at all times and selected at the counter output. An extra output bit is obtained by directly sampling the input clock. Moreover, the speed sensing resolution at the TRO output earns one additional bit through the use of the TRO second clock phase.

3.4.2.2 Control Part

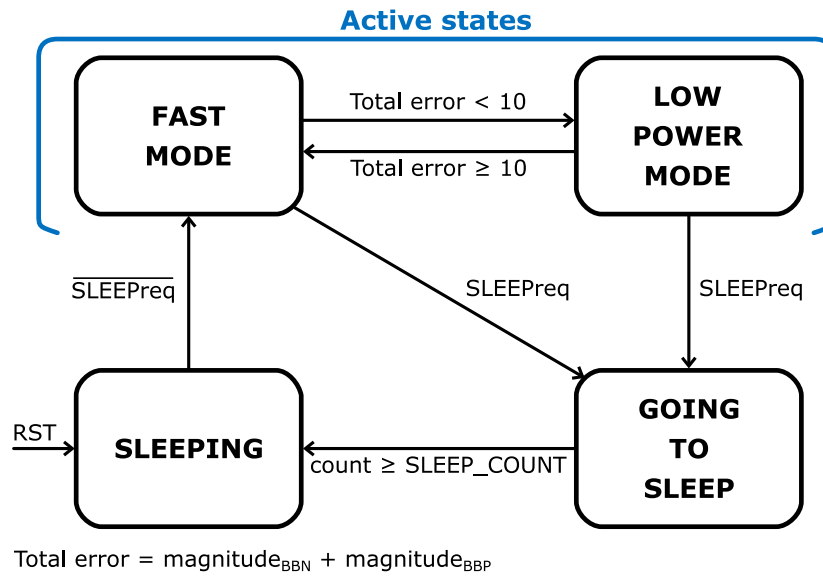
From the sensors outputs, the controller generates adequate sign-magnitude control signals for the UFBBR drivers. Its architecture is visible in Fig. 3.9 and is made of standard cells, automatically placed and routed with the MCU digital logic.

For versatility and adaptability to a wide range of operating conditions, the UFBBR control part possesses many tuning knobs, all configurable in software. Their names as well as their values are given in Table 3.4. All of them were already introduced before, except for two. Firstly, the `IMBL_OFFSET` configuration allows to modify the N/PMOS imbalance target, which by default is 0 (no imbalance is desired). A positive value for `IMBL_OFFSET` shifts the process corner towards a FS process corner while a negative value moves it towards a SF one. This feature is only used for experimental purposes. Secondly, the `EN_PIS` variable allows to disable the PIS, shutting off the imbalance-corrective part to save power.

The UFBBR unit has four operation states. The controller takes in charge the transitions from one state to another according to the finite-state machine (FSM) depicted in Fig. 3.16. At wake-up, the UFBBR starts in **FAST MODE** and the

Table 3.4 Configuration registers accessible from software.

Names	Values	
	Range	Default
FMULT	From 0 to 255	<u>16</u>
IMBL_OFFSET	From -128 to 127	<u>0</u>
NSEL	From 0 to 15	<u>12</u>
G_p, G_n	0, 0.5, 0.75, 0.875, <u>1</u> , 1.125, 1.25, 1.5	
G_f, G_i	0, 0.25, 0.5, <u>1</u> , 2, 4	
SLEEP_COUNT	From 0 to 255	<u>16</u>
EN_PIS	0 or <u>1</u>	

**Fig. 3.16** Finite-state machine (FSM) diagram for the UFBBR controller.

actuation and sensing are performed 100% of the time without interruptions. In other words, the sensing of sample k is done while actuating for sample $k - 1$. When the total error (defined as the sum of the magnitude signals provided to the BB drivers) falls below a value of 10, the FSM switches to the **LOW POWER MODE**, during which actuation and sensing are performed one at a time. When a sleep request is received from the MCU, the FSM goes first in its **GOING TO SLEEP** state before reaching the **SLEEPING** state. This intermediate step is needed to drive the BBP voltage towards 0 V, with a full-magnitude reverse actuation during a configurable number of cycles determined by **SLEEP_COUNT**.

The controller is also responsible for the generation of the **LOCK** signal, which indicates to the rest of the system that the UFBBR is properly locked, both in terms of clock frequency generation and process imbalance correction. As shown in Fig. 3.10, the **LOCK** signal is asserted when the total error falls below 4 for at least 5 cycles. It goes low when the total error exceeds that threshold for at least 3

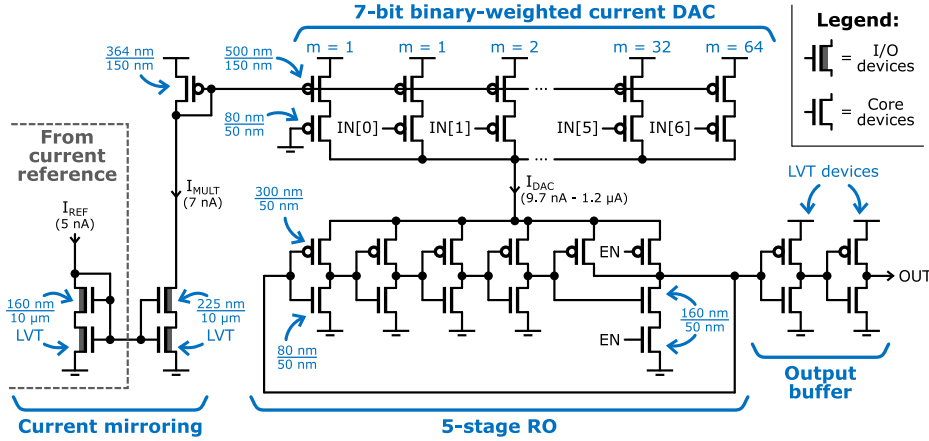


Fig. 3.17 Schematic of the digitally-controlled oscillators (DCOs) used in the UFBBR drivers part.

cycles. In the context of this work, the UFBBR wake-up time is thus defined as the time interval separating the falling edge of a sleep request and the rising edge of the lock signal.

3.4.2.3 Actuation Part

Based on the sign-magnitude control signals given by the controller, the BB drivers perform the appropriate current actuation. This is achieved by the use of DCOs driving SCCPs. A high-magnitude signal results in a faster DCO frequency, which in turn leads to a higher actuation current. The sign signal selects which SCCP is fed with the DCO output, to charge or discharge the BB voltage accordingly. SCCPs are commonly used when the actuation needs to be performed on a wide voltage range, outside the supply rails or at negative values as required for BBP.

The schematic of the DCOs is provided in Fig. 3.17. The chosen topology is built around a 5-stage current-starved RO drawing current from a 7-bit binary-weighted current digital-to-analog converter (DAC) based on a 5-nA current reference I_{REF} . This reference current is mirrored from the reference generator (see Fig. 3.8), which lies in the 1.8-V domain and uses LVT thick-oxide I/O transistors. Regular- V_{th} (RVT) core devices are used for the DAC and the current-starved RO. For a good signal sharpness, LVT core devices are used for the output buffer. There are two reasons to use a current-starved RO here over a BBCO. Firstly, the use of FBB is limited to the ULV domain, where it has the highest value. The actuators operate at a higher voltage without FBB, which prevents the use of BBCO. Secondly, a current-starved topology can easily be tuned in a digital manner and get interfaced with the digital control.

Given the difference in the ranges over which BBN (from 0 to 1.8 V) and BBP (from 0 to -3 V) need to be regulated, their corresponding SCCPs possess some

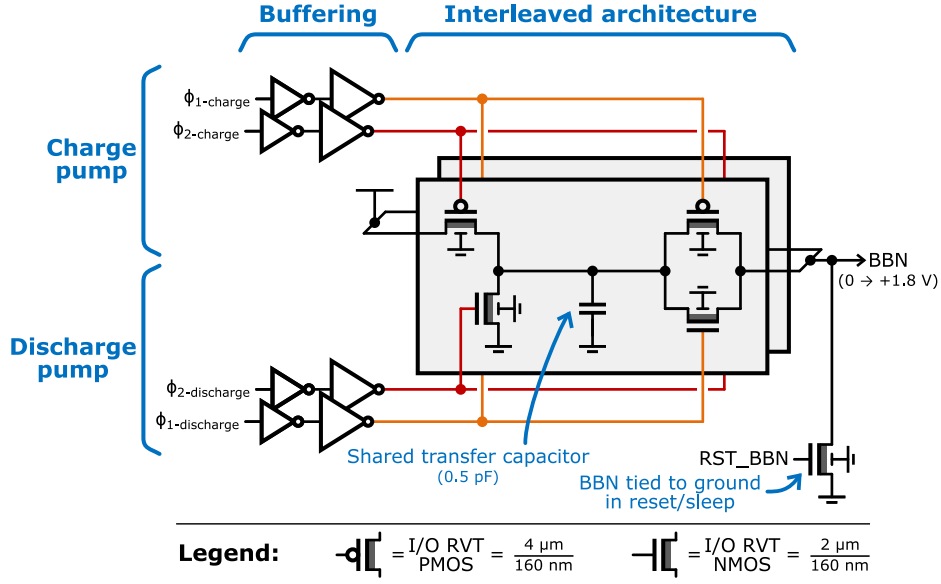


Fig. 3.18 Schematic of the switched-capacitor charge pumps (SCCPs) used for BBN actuation.

differences. The schematic of the SCCPs used to drive BBN is shown in Fig. 3.18. An interleaved architecture with unity-voltage conversion ratio is used. The two transfer capacitors are shared between charge- and discharge-pumps. For a proper reset to 0 V when going in sleep mode, a reset switch is also added on BBN. A non-overlapping clock (NOC) generator between the BBN SCCPs and the corresponding DCO avoids direct short circuit currents between the 1.8-V supply and BBN. For the BBP actuation, cross-coupled topologies with two stages are used as SCCPs, as done in our first UFBBR prototype and in [20]. Their schematic is represented in Fig. 3.19.

Both BBN and BBP drivers use I/O RVT transistors. To maximize their matching, the same device dimensions are used and the same value of 0.5 pF is used for the transfer capacitors. At the output of the BBP SCCPs, two diodes (diode-connected LVT I/O NMOS transistors) in series connect BBP and ground. They are not shown in Fig. 3.19 and are not actually needed in the UFBBR design. They are added as protection devices, driving BBP to ground in case it increases beyond 0 V due to the reverse actuation mechanism used when going to sleep.

Finally, the DCOs output frequency as well as the corresponding SCCPs output currents are displayed in Fig. 3.20, as a function of the magnitude control signals provided by the controller. As desired, a good matching is obtained between charge and discharge modes, as well as between BBN and BBP drivers, especially at low magnitude input values.

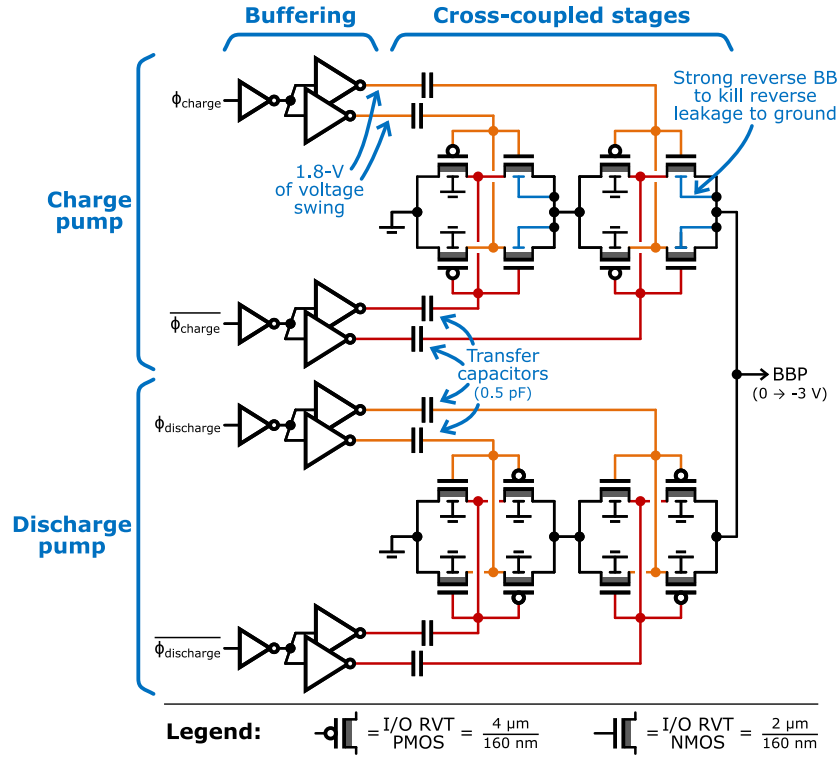


Fig. 3.19 Schematic of the switched-capacitor charge pumps (SCCPs) used for BBP actuation.

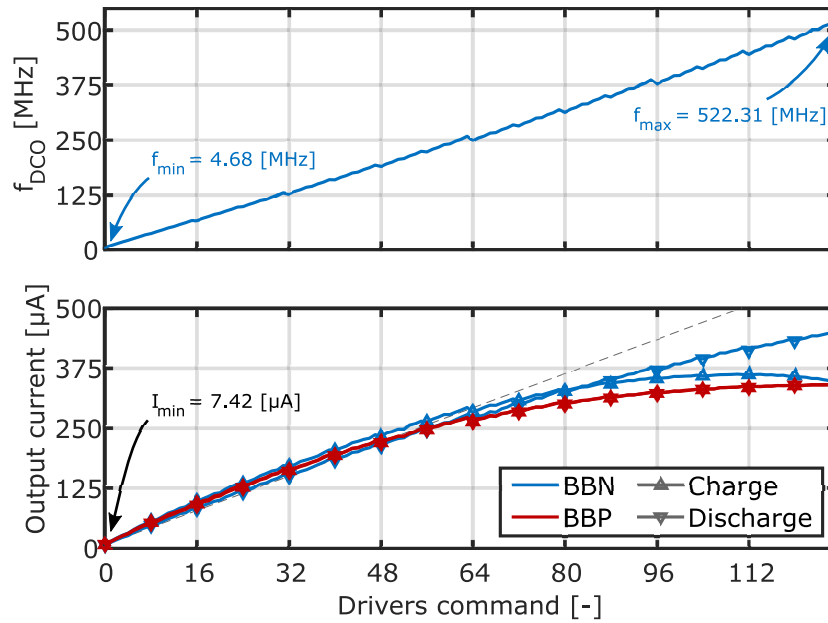


Fig. 3.20 Simulated transfer function of the UFBBR drivers. In charge mode, BBN/BBP are initialized at 0 V. In discharge mode, BBN/BBP are initialized at +1.8 V/-3.0 V.

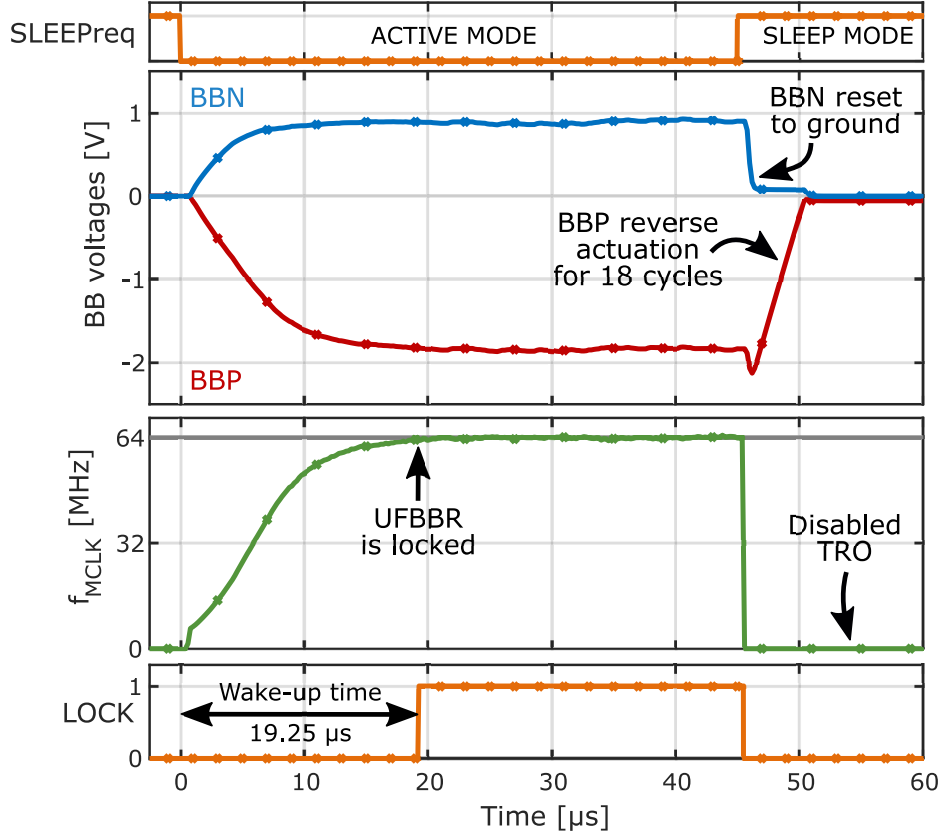


Fig. 3.21 Closed-loop UFBBR behavior at wake-up and when going-to-sleep obtained from post-layout simulations. The frequency target is 64 MHz, default loop gains are used.

3.4.2.4 Closed-Loop Behavior

The constitutive parts of the UFBBR can now be put together and its closed-loop behavior analyzed. The simulated wake-up and going-to-sleep sequences of the UFBBR in typical conditions are both shown in Fig. 3.21. In active mode, the UFBBR successfully generates the 64-MHz target frequency and locks in less than 20 μs . In sleep, the MCLK generation is disabled and the BB voltages are driven towards 0 V to save leakage. BBN is simply switched to ground using an NMOS switch, as previously described. This technique cannot be applied to BBP as it is negative. Instead, BBP is driven towards ground in open loop with a full-magnitude reverse-actuation for a programmable number of cycles.

Moreover, the UFBBR ability to compensate for the effects of PVT variations is demonstrated in Fig. 3.22, which shows the in-lock BB voltages to which the UFBBR locks for different process and temperature (PT) corners, and for several target clock frequencies. All five process corners are considered, from TT to FF and SS, including the skewed SF and FS corners. The temperature range considered in this work goes from -40 to $+85^\circ\text{C}$. The UFBBR successfully locks in all these different operating conditions.

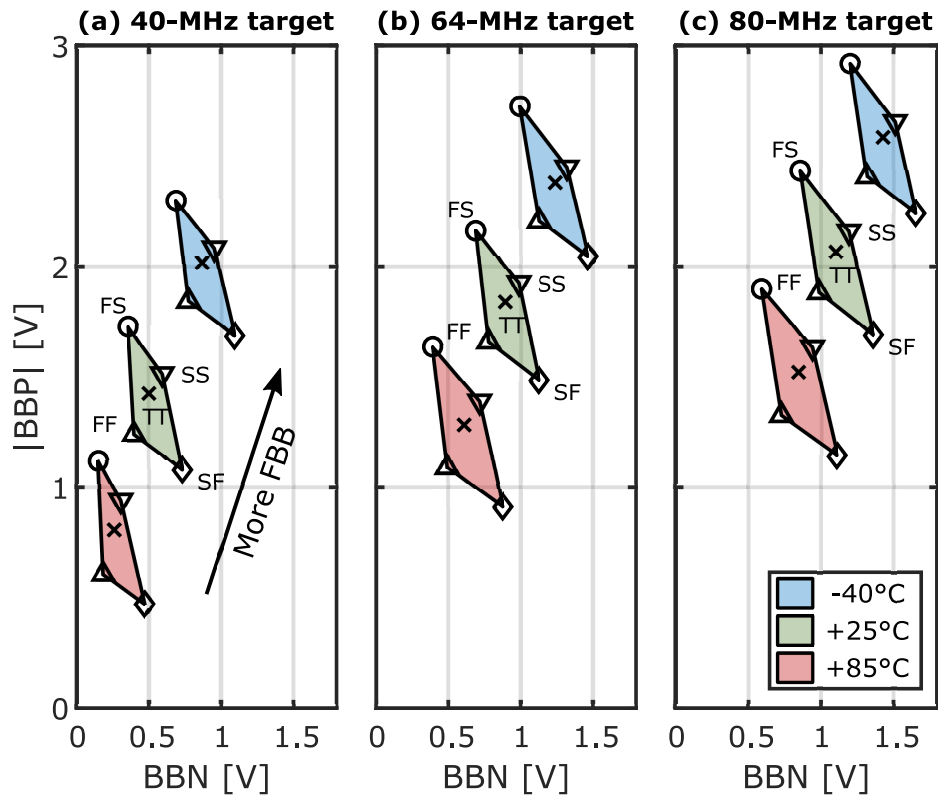


Fig. 3.22 In-lock BB voltages across all PVT variations obtained from post-layout simulations for three different target frequencies.

3.4.3 Full-Loop UFBBR Modeling

In this section, we provide a continuous-time model of the proposed UFBBR system. A block diagram of the UFBBR is shown in Fig. 3.23 and is used as a basis for the development of its equivalent state-space representation in the Laplace domain. It regroups the linearized transfer functions of the UFBBR constitutive parts, previously described in Section 3.4.2. We first obtain the state-space representation, before briefly analyzing the corresponding transfer functions and their implications regarding closed-loop stability.

The UFBBR input, error, and output signals are respectively gathered in $\mathbf{r}$, $\mathbf{e}$, and $\mathbf{y}$ vectors as follows:

$$\mathbf{r} = \begin{bmatrix} \text{FMULT} \\ \text{IMBL_OFFSET} \end{bmatrix}, \quad (3.1)$$

$$\mathbf{e} = \begin{bmatrix} \text{freq_err} \\ \text{imbl_err} \end{bmatrix}, \quad (3.2)$$

$$\mathbf{y} = \begin{bmatrix} f_{MCLK} \\ f_{imbl} \end{bmatrix}, \quad (3.3)$$

where f_{imbl} designates the PIS output frequency and is defined as:

$$f_{imbl} = f_{PRO} - f_{NRO}. \quad (3.4)$$

It is also useful to define two additional vectors, namely $\mathbf{i}$ and $\mathbf{b}$, respectively gathering the charge-pumps output currents and BBCCO control voltages:

$$\mathbf{i} = \begin{bmatrix} I_{bbn} \\ I_{bbp} \end{bmatrix}, \quad (3.5) \quad \mathbf{b} = \begin{bmatrix} BBN \\ BBP \end{bmatrix}. \quad (3.6)$$

From the diagram depicted in Fig. 3.23, the relation between these two vectors can be expressed as:

$$\mathbf{i} = s \begin{bmatrix} C_n + C_{pn} & -C_{pn} \\ -C_{pn} & C_p + C_{pn} \end{bmatrix} \mathbf{b} = s \mathbf{C}_{eq} \mathbf{b}, \quad (3.7)$$

$$\mathbf{b} = \frac{1}{s} \mathbf{C}_{eq}^{-1} \mathbf{i}. \quad (3.8)$$

Assuming matched UFBBR drivers, i.e.:

$$G_n I_{cp,n} \approx G_p I_{cp,p} \approx I_{cp}, \quad (3.9)$$

the charge-pumps output currents $\mathbf{i}$ are obtained from the error signals $\mathbf{e}$ in the

following way:

$$\mathbf{i} = I_{cp} \begin{bmatrix} G_f & G_i \\ -G_f & G_i \end{bmatrix} \mathbf{e} = \mathbf{G} \mathbf{e}. \quad (3.10)$$

The error vector $\mathbf{e}$ is linked to the inputs $\mathbf{r}$ and outputs $\mathbf{y}$ as follows:

$$\begin{aligned} \mathbf{e} &= \begin{bmatrix} 4 & 0 \\ 0 & 1 \end{bmatrix} \mathbf{r} + \frac{1}{f_{RCLK}} \begin{bmatrix} -4 & 0 \\ 0 & 2 \end{bmatrix} \mathbf{y} \\ &= \mathbf{B} \mathbf{r} + \mathbf{S} \mathbf{y}. \end{aligned} \quad (3.11)$$

Finally, the output vector $\mathbf{y}$ is obtained from the BBCO control voltages $\mathbf{b}$ as expressed here:

$$\mathbf{y} = \begin{bmatrix} K_{Tn} & K_{Tp} \\ K_{PNn} & K_{PNp} \end{bmatrix} \mathbf{b} = \mathbf{K} \mathbf{b}, \quad (3.12)$$

where the frequency gains of the BBCOs constituting the imbalance sensor are combined in the following way:

$$K_{PNx} = K_{Px} - K_{Nx}. \quad (3.13)$$

With Equations (3.1)-(3.13) in hand, and by defining the state vector $\mathbf{x}$ as:

$$\mathbf{x} = \frac{1}{s} \mathbf{e}, \quad (3.14)$$

the following state-space representation of the UFBBR can be obtained:

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A} \mathbf{x} + \mathbf{B} \mathbf{r}, \\ \mathbf{y} = \mathbf{C} \mathbf{x}, \end{cases} \quad (3.15)$$

where the matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$ are respectively given by:

$$\mathbf{A} = \mathbf{S} \mathbf{K} \mathbf{C}_{eq}^{-1} \mathbf{G}, \quad (3.16)$$

$$\mathbf{B} = \begin{bmatrix} 4 & 0 \\ 0 & 1 \end{bmatrix}, \quad (3.17)$$

$$\mathbf{C} = \mathbf{K} \mathbf{C}_{eq}^{-1} \mathbf{G}. \quad (3.18)$$

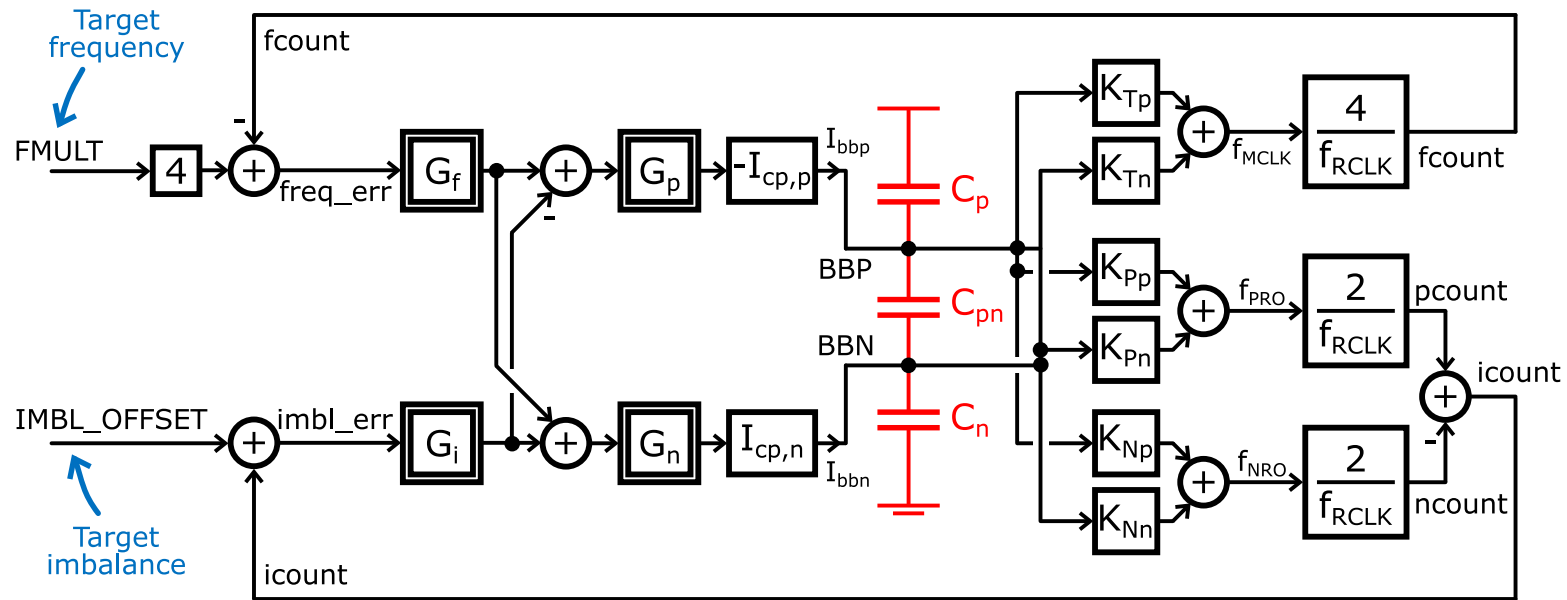


Fig. 3.23 Block diagram in the Laplace domain used as continuous-time model for the UFBBR unit.

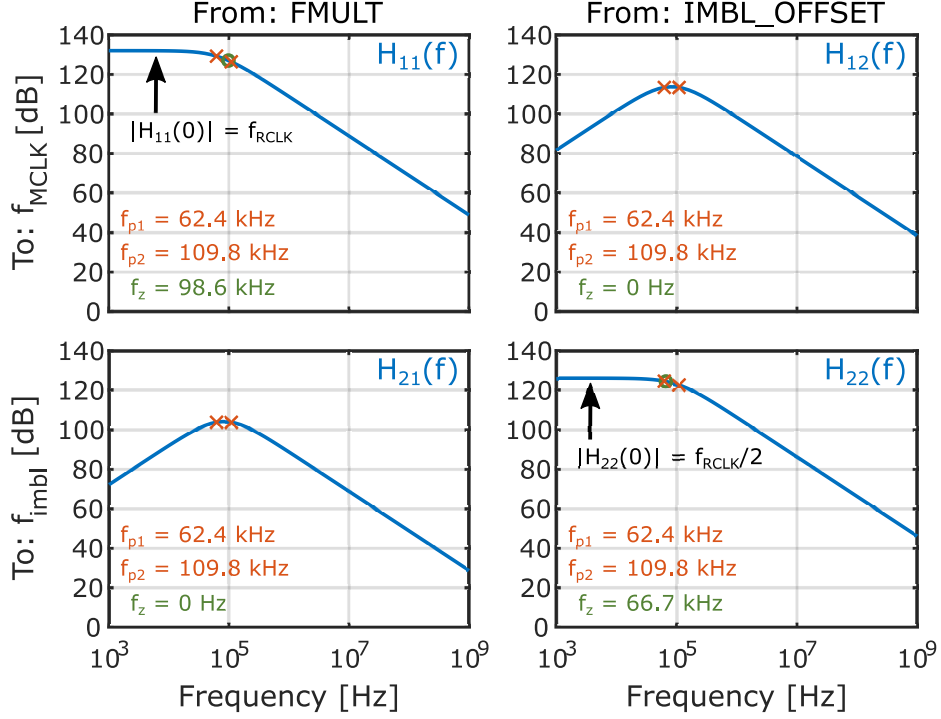


Fig. 3.24 Closed-loop transfer functions obtained from the UFBBR model.

As the UFBBR system is a 2×2 system (two inputs and two outputs), there are four different closed-loop transfer functions, which are gathered in the transfer matrix $\mathbf{H}(s)$:

$$\mathbf{H}(s) = \mathbf{C} (s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B}. \quad (3.19)$$

Because of the number of variables involved, expanding and developing the full analytical expressions for each of these four transfer functions is heavy and falls out of the scope of this work. However, they can easily be manipulated numerically. They are represented in Fig. 3.24 and the corresponding closed-loop step responses are shown in Fig. 3.25, with default gain values and for a default target frequency of 64 MHz. Thanks to a pole at 0 Hz in the open-loop transfer functions (coming from the parasitic capacitance integration), the phase margin is 90° which ensures a stable behavior in closed loop. Besides, the poles of the closed-loop transfer functions all have a negative real part, which thus confirm the inherent stability of the proposed UFBBR system.

To end this analysis, we propose to take a look at a particular case: the transfer function from FMULT to f_{MCLK} without imbalance correction ($\mathbf{G}_i = 0$). It can be

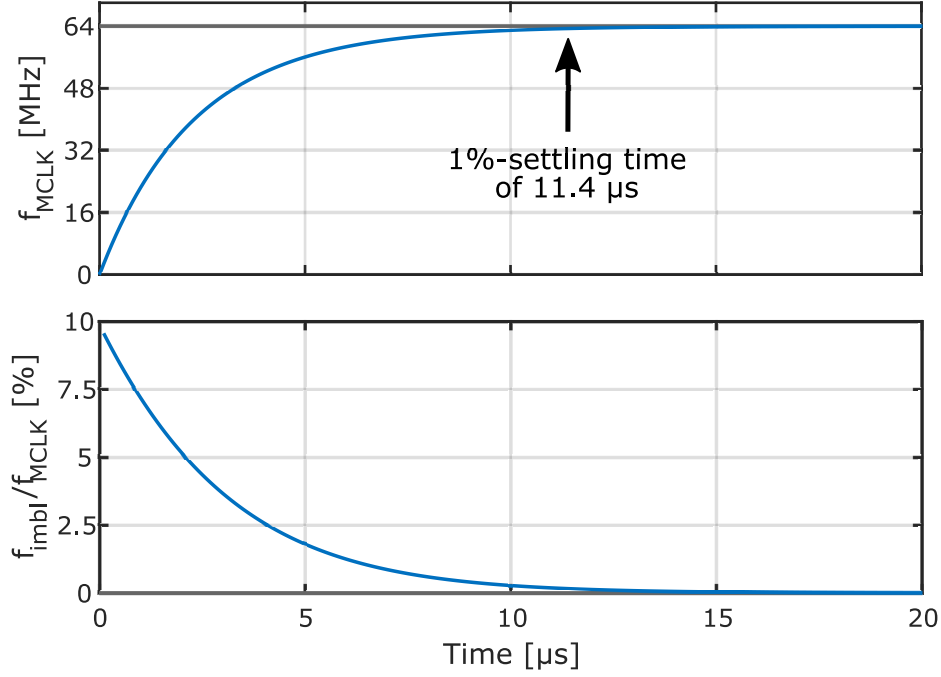


Fig. 3.25 Closed-loop step responses obtained from the UFBBR model.

shown that this transfer function has the following first-order form:

$$\begin{aligned} H_{11}(s)|_{G_i=0} &= \frac{f_{MCLK}}{FMULT}(s) \Big|_{G_i=0} \\ &= H_{11}(0)|_{G_i=0} \frac{1}{1 + s/2\pi f_{p1}}, \end{aligned} \quad (3.20)$$

with:

$$H_{11}(0)|_{G_i=0} = f_{RCLK}, \quad (3.21)$$

$$f_{p1} = \frac{2G_f I_{cp}}{\pi f_{RCLK}} \frac{K_{Tn} C_p - K_{Tp} C_n}{C_n C_p + C_{pn}(C_n + C_p)}. \quad (3.22)$$

The UFBBR steady-state gain is equal to f_{RCLK} , which means that f_{MCLK} tends to $FMULT \times f_{RCLK}$, as desired. The pole frequency is function of the gain G_f , which can be increased to lower the settling time at the cost of extra in-lock power consumption.

3.4.4 Prototyping and Measurement Results

This section presents the chip prototype and provides experimental results that validate the functionality and the performance of the proposed UFBBR unit. Unless explicitly indicated, the measurements are obtained at the default 64-MHz

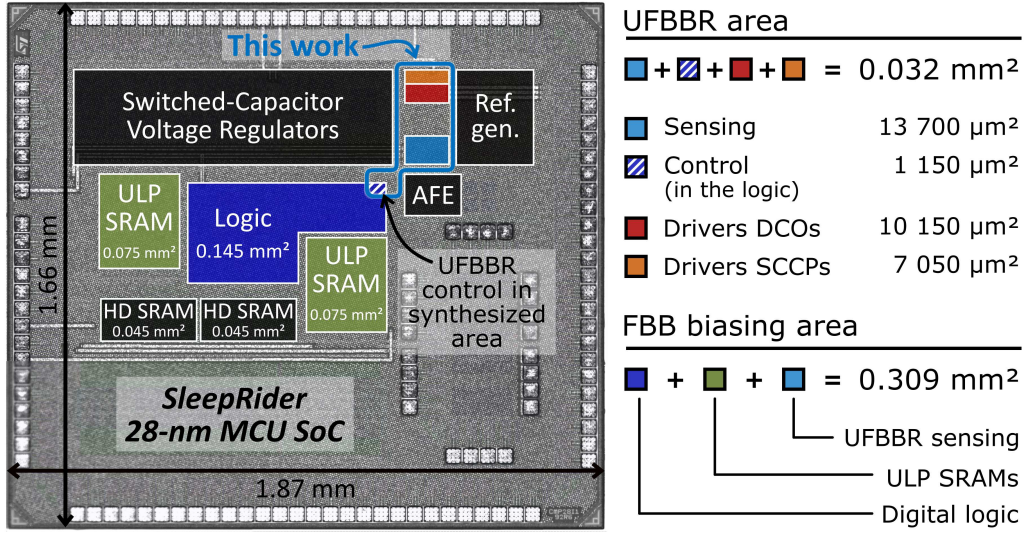


Fig. 3.26 Die microphotograph of SleepRider with post-shrink dimensions.

frequency. In some cases, the UFBBR limits are also tested, at 40 or 80 MHz for instance.

The proposed UFBBR system is embedded in SleepRider MCU SoC, which was fabricated in 28-nm FDSOI technology. The die microphotograph is given in Fig. 3.26 and shows the main constitutive parts of the chip. The UFBBR occupies a silicon area of less than 0.032 mm², with a total FBB biasing area of 0.309 mm², including the core logic and the ULP SRAMs. The total parasitic coupling capacitance existing between BBN and BBP was measured to be around 290 pF, which is lower than estimated prior to the design phase.

3.4.4.1 Closed-Loop Behavior and Performance

The measured UFBBR wake-up and going-to-sleep sequences are both shown in Fig. 3.27. A divided-by-64 version of MCLK is visible, together with the generated BB voltages and the corresponding UFBBR lock signal. The measured wake-up time is 11 μs, which is shorter than in simulations thanks to the lower experimental values for the parasitic coupling capacitances.

Compared to a situation which does not exploit FBB (zero BB voltages), the UFBBR unit provides two important benefits, as illustrated in Fig. 3.28. On one hand, for a fixed desired operational speed, the UFBBR allows to reduce the minimum supply voltage. A 180 mV reduction (from 0.56 to 0.38 V) is demonstrated for the default 64-MHz target frequency. Alternatively, for a fixed supply voltage, the UFBBR unit provides a significant frequency boosting. At the default supply voltage value of 0.4 V, a 15× frequency boosting is achieved (from 5 to 75 MHz). These benefits are obtained at room temperature for a typical die.

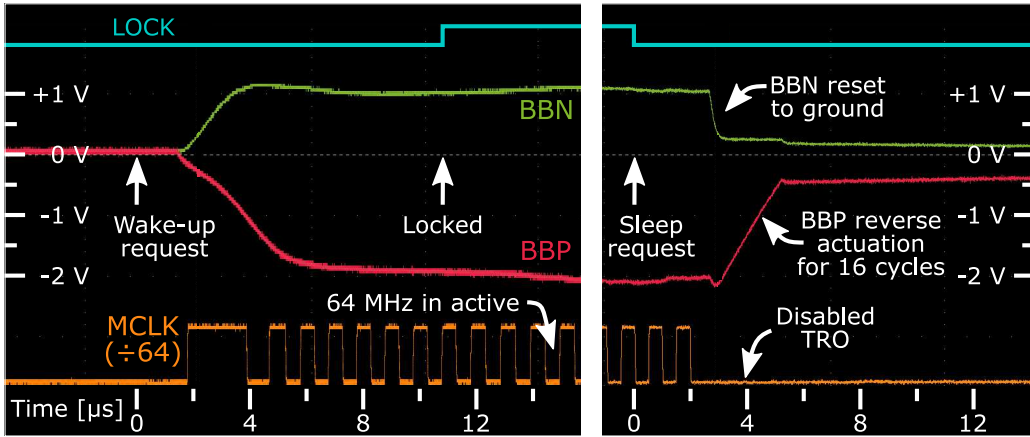


Fig. 3.27 Measured UFBBR wake-up and going-to-sleep sequences.

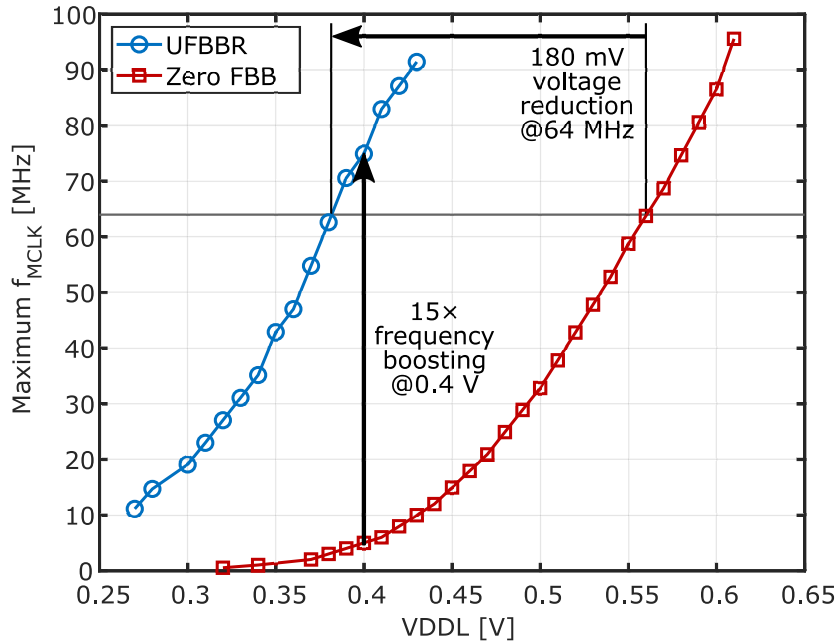


Fig. 3.28 Frequency boosting and supply voltage reduction enabled by the UFBBR and obtained in measurements, for a typical die at room temperature.

In active mode, the power overhead related to the UFBBR unit namely depends on the target frequency and on the loop gain values. Fig. 3.29 shows the UFBBR power breakdown for the default target frequency and for different configurations. The power of the sensing and control parts (ULV domain) appear in blue, while the power contributions of the DCOs (0.8-V domain) and the SCCPs (1.8-V domain) appear in orange and yellow, respectively. As shown in Fig. 3.29, the total UFBBR power consumption can typically be reduced by decreasing the loop gain values G_f and G_i , at the cost of a longer settling time. This mechanism keeps constant

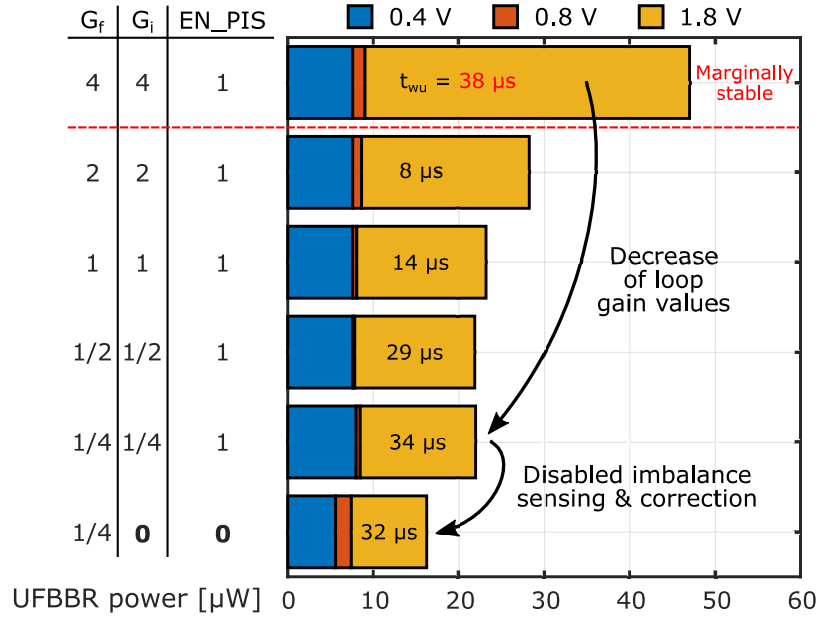


Fig. 3.29 Measured UFBBR power overhead at 64-MHz target frequency.

the power of the sensing and control parts, but effectively reduces the actuation power of the SCCPs. Besides, more power savings can be obtained by disabling the imbalance-corrective loop and turning off the PISs. Software configurations can be easily changed after waking-up and before going to sleep to reach both a low settling time and a low in-lock power in active mode, without additional penalty. At the default MCLK frequency of 64 MHz, the lowest measured UFBBR power consumption is 22 μW (resp. 16.3 μW) with frequency and process imbalance correction (resp. with frequency correction only).

3.4.4.2 Temperature Compensation Capability

The functionality of the UFBBR unit has been tested at temperatures ranging from -40 to $+85^\circ C$. The corresponding measurement results are shown in Figs. 3.30 and 3.31.

Fig. 3.30 qualitatively shows the temperature compensation capability of the UFBBR, for several target frequencies between 32 and 80 MHz. For a wide range of temperatures, the UFBBR is properly locked and the MCU stays functional (in green in the figure). However, two limitations appear for high target frequency values.

The first issue appears at low temperatures (in yellow) and due to the BBP protection diodes briefly described in Section 3.4.2.3. Their leakage was erroneously neglected during the design phase but appears significant in practice for very low BBP values. Simulations show that the diode leakage current is around 2 μA at -2.5 V of BBP for a TT process at $-40^\circ C$, and rises up to 15 μA at -3.0 V of BBP.

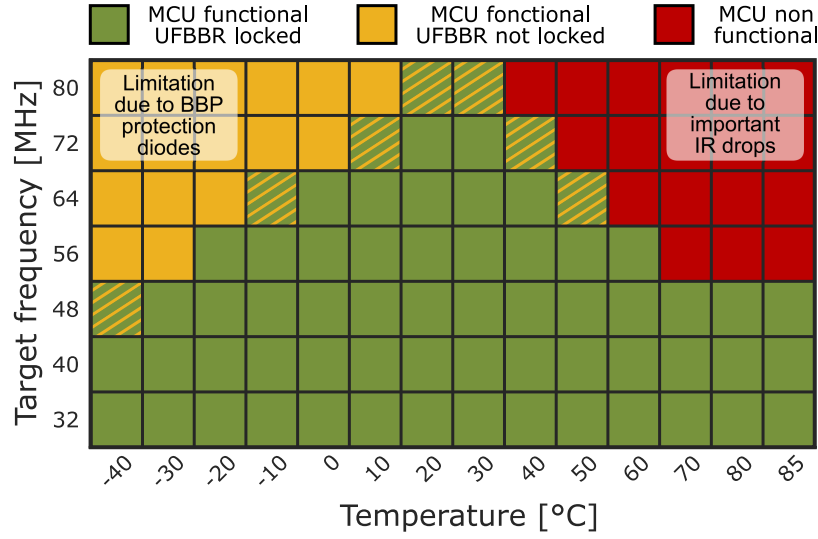


Fig. 3.30 Qualitative evaluation of the temperature compensation capability of the UFBBR obtained in measurements.

The situation is even worse in FS or FF processes. Indeed, the UFBBR is not able to cope with such current levels and thus cannot properly keep the lock. The MCU stays functional but at a lower clock frequency. This problem could easily be fixed by using protection diodes made of one PMOS and one NMOS transistor in series (instead of two NMOS transistors as currently used). The second issue appears at high temperature (in red), where the leakage current of the transistors in the logic (the regulated circuit) is not only increased by the high BB values required to reach the high target frequencies, but also exacerbated by the temperature increase. This prohibitive leakage results in significant supply voltage drops, and the MCU loses its functionality in these conditions.

In Fig. 3.31, the temperature compensation achieved with the UFBBR is quantitatively compared to static external FBB, for three target frequencies. The application of static external FBB can be seen as fixed design margins (as discussed in Section 3.2). To cover the widest range of temperatures with static external FBB, maximal FBB values (i.e., BB values generated by the UFBBR at -40°C) are needed, in order for the ULV logic to be fast enough in all temperature cases. However, the corresponding power overhead is extremely high at higher temperatures, due to the leakage current increase with temperature. For instance, at a fixed 40-MHz target frequency, the UFBBR is able to reduce the logic power by 15%, 37%, and 64%, respectively at $+25$, $+50$, and $+85^{\circ}\text{C}$, compared to the maximal static FBB case. At higher target frequencies, the power savings enabled by the UFBBR are even more important. Using moderate static FBB values (i.e., BB values generated by the UFBBR at 20°C) limits the power overhead at high temperatures, but does not preserve the functionality at low temperatures. The adaptive behavior brought by the UFBBR gives both a wide functionality range as well as low power overhead for the logic.

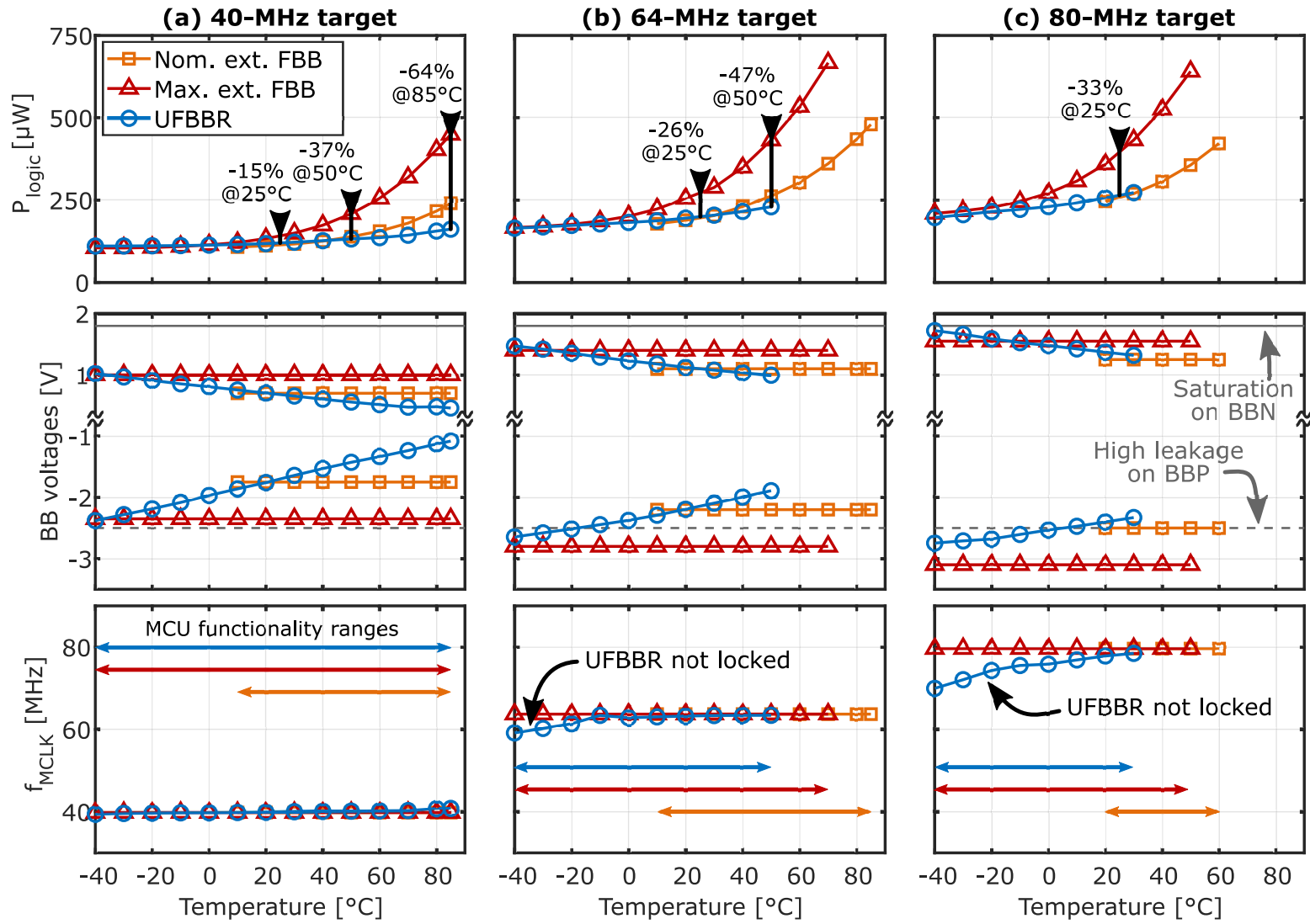


Fig. 3.31 Quantitative evaluation of the temperature compensation capability of the UFBBR obtained in measurements.

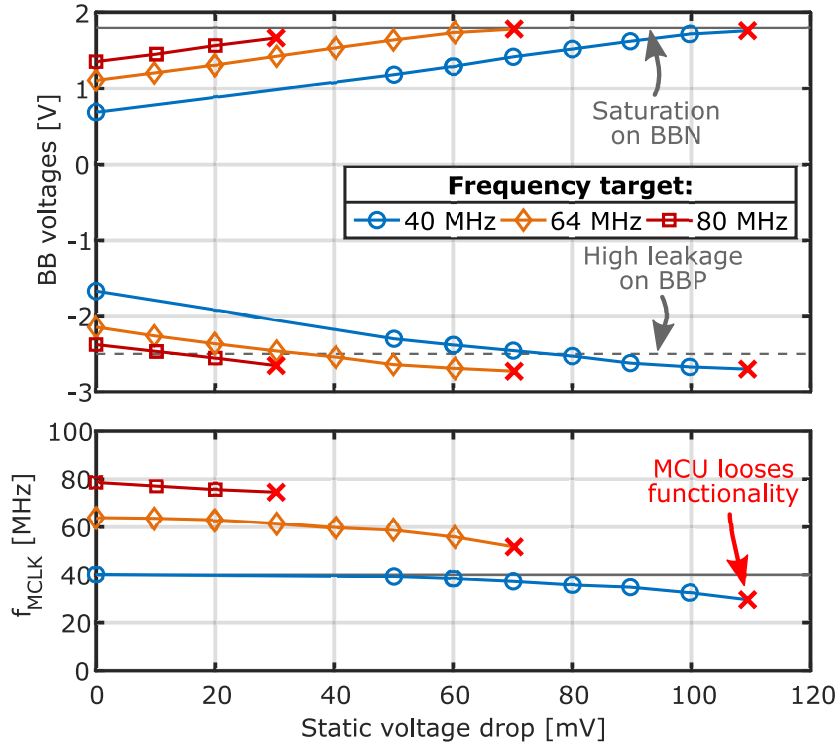


Fig. 3.32 Measured robustness to static supply voltage drops.

3.4.4.3 Sensitivity to Supply Voltage Droops

Like with UFVR systems and as mentioned in Section 3.2, the proposed UFBBR unit should, by design, give robustness to supply voltage droops, as the TRO lies in the same voltage domain as the logic and its frequency drops instantaneously with the supply voltage.

Fig. 3.32 shows the robustness brought by the UFBBR in presence of static drops, for three different target frequencies. For 40-, 64-, and 80-MHz target frequencies, the logic can respectively withstand up to 100, 60, and 20 mV of static voltage drop on its 0.4-V supply, albeit with a loss of the frequency lock. This lock loss is caused by the saturation of BBN and by the leakage of BBP protection diodes (see Section 3.4.4.2). After resetting the supply voltage to its nominal 0.4-V value, the UFBBR relocks properly while the MCU remained functional during the whole experience. The higher the target frequency, the higher the sensitivity to voltage drops.

Dynamic voltage drops can also be induced by transitioning from one mode to another. For instance, when the MCU moves from idle (with gated processor clock) to active mode, the current consumption suddenly increases and, coupled with the resistive losses of the supply routing, causes voltage drops in the logic. This situation is shown in Fig. 3.33. Fig. 3.34 shows the UFBBR robustness to such

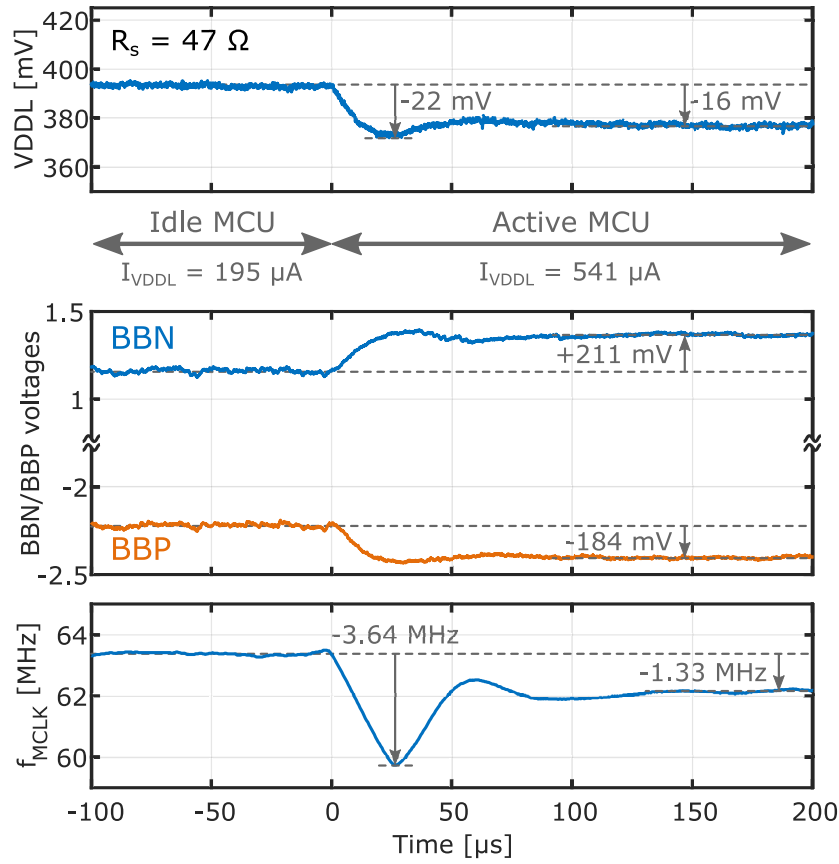


Fig. 3.33 Example of dynamic voltage drop induced by a change of MCU mode (from idle to active) obtained in measurements.

dynamic voltage drops, for three different target frequencies. A series resistor is added between the 0.4-V external voltage source and the chip to extend the sensitivity evaluation. In addition to the internal supply routing (whose resistance is unknown), the MCU can tolerate 100, 100, and 20Ω of extra resistance on its 0.4-V supply, respectively for 40-, 64-, and 80-MHz targets. Once again, the higher the target frequency, the higher the sensitivity to voltage drops.

In conclusion, these results demonstrate a good robustness against both static and dynamic sudden voltage droops.

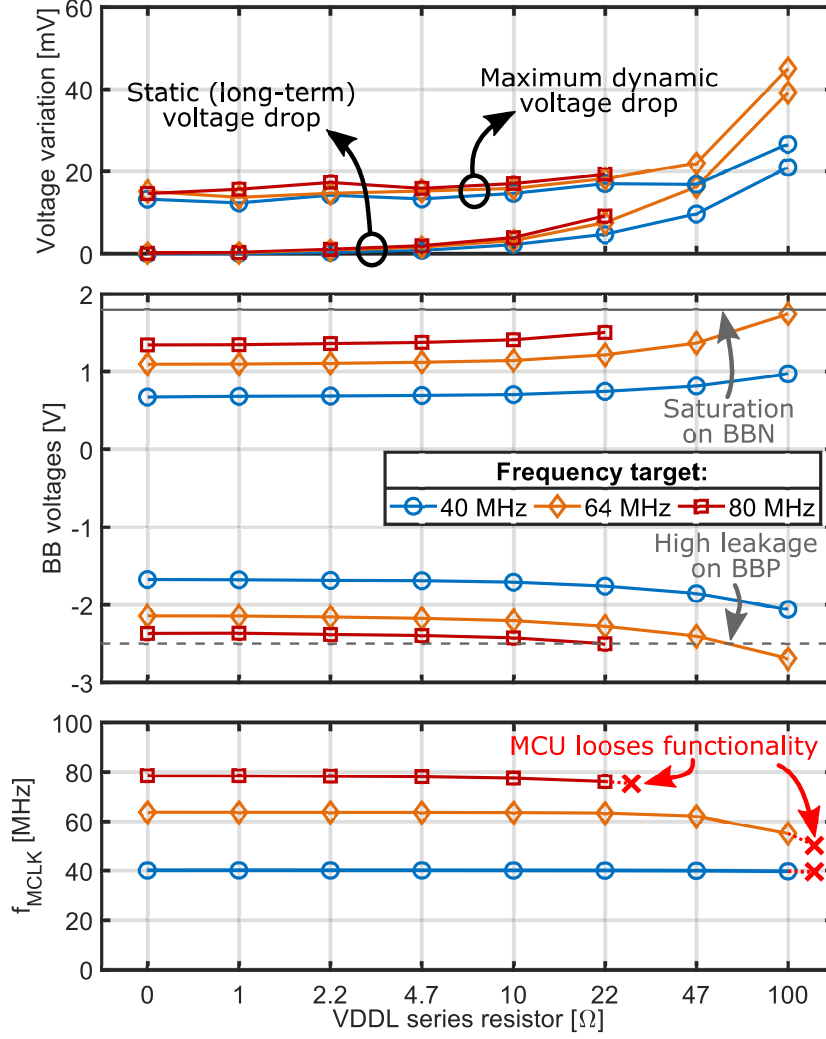


Fig. 3.34 Measured robustness to dynamic voltage drops induced by the MCU transition from idle to active mode.

3.5 Comparison to the State of the Art

Our two UFBBR prototypes, previously detailed in Sections 3.3 and 3.4, respectively, are now extensively compared to other closed-loop ABB-based systems in Table 3.5. Our comparison comprises details on the corresponding applicative context and the BB generation itself, including information concerning the regulation loop topology and the type of sensing/actuation.

Compared to other ABB generators in the literature, our proposed UFBBR designs appear competitive, showcasing a fast settling time for a limited area overhead. Indeed, our two UFBBR generations demonstrate wake-up times of 10 and 8 μs , respectively, and occupy a silicon area of 0.060 and 0.032 mm^2 , respectively. The biased well areas seen as a load by our designs are 0.4 and 0.31 mm^2 , respectively.

In terms of power consumption, it was not possible to accurately measure the power of our first UFBBR version. For the second one, the measured power level reaches 22 μW in lock. Although this value is the highest of the comparison table, two important remarks must be kept in mind. Firstly, duty-cycling the imbalance-corrective loop of the UFBBR can reduce the power consumption, as shown in Section 3.4.4.1. Secondly, it also includes the 32-to-80 MHz system clock generation, unlike ABB systems. Altogether, our proposals exhibit an excellent trade-off between settling time, power, and occupied and biased areas.

We did not include jitter performance in Table 3.5 for two reasons. Firstly, other works do not generate a clock. Secondly, only period or cycle-to-cycle jitter matters for digital logic [29, 87–90] and corresponding specification is relaxed. In our prototypes for instance, the uncertainty coming from jitter is easily absorbed at the clock tree synthesis step.

Compared to our first version, the second UFBBR prototype does not need any off-chip decoupling capacitors on the regulated BB voltages. It is also far more flexible thanks to numerous configuration registers, all accessible from software. Note also that the power of [85] in Table 3.5 is optimistic because the negative BBP voltage is not fully generated on-chip like in our works but rather from an external negative -1.2 V supply voltage.

Perhaps the most significant benefits brought by the UFBBR units lie at the system level. Indeed, their adaptive FBB generation provides PVT compensation for the entire MCU digital logic and the ULP SRAMs. This robustness to PVT also concerns asymmetric skewed process corners, as our adaptive loops also correct N/PMOS process imbalance. In addition, FBB enables an efficient MCU operation at ULV/ULP in active mode. Our two MCU prototypes, SleepRunner and SleepRider, achieve record energy values, reaching 3 $\mu\text{W}/\text{MHz}$ at 40 MHz and 5.5 $\mu\text{W}/\text{MHz}$ at 56 MHz, respectively. In sleep mode, our UFBBR units disable the system clock generation and drive the FBB voltages towards 0 V to reduce leakage. This mechanism helps lower the sleep power of our two proposed MCUs down to 12.7 μW and 7.7 μW , respectively, with logic state and memory retention. Thanks to fast transitions between sleep and active modes, our two implementations also minimize the wake-up/going-to-sleep overheads.

All these results demonstrate the relevance of the UFBBR concept for ULV/ULP applications.

Table 3.5 Performance comparison of closed-loop adaptive back biasing and unified frequency and back-bias regulation units.

											This work	
			Clerc 2015 [21]	Rossi 2017 [77]	Quelen 2018 [78]	Hoppner 2019 [91]	Hoppner 2019 [79]	Lee 2019 [85]	Walter 2020 [92]	Moursy 2021 [84]	SleepRunner UFBBR 1 [JP3]	SleepRider UFBBR 2 [CP2]
General	Metrics	Units										
	Technology	-	28-nm FDSOI	28-nm FDSOI	28-nm FDSOI	22-nm FDSOI	22-nm FDSOI	55-nm DDC	22-nm FDSOI	22-nm FDSOI	28-nm FDSOI	28-nm FDSOI
	Supplies	V	0.45 1	1 1.8	0.35 1.8	0.5 0.8 1.8	0.5 0.8 1.8	1.2 -1.2 2.4	0.55 0.8 1.8	0.5 1.8	0.4 0.8 1.8	0.4 0.8 1.8
	Regulation	-	ABB	ABB	ABB	ABB	ABB	AVS+ABB	ABB	ABB	UFBBR	UFBBR
Applicative Context	Core	-	SPARC v8	OpenRISC	N-A	CM4F	CM4F	CM0	CM4F	CM4F	CM0 DS	CM4
	Memories	-	20 kB RAM	112 kB RAM	N-A	84 kB SRAM	512 kB SRAM	8 kB SRAM	256 kB SRAM	512 kB SRAM	64 kB SRAM	96 kB SRAM
	Operating Range	V	0.33 - 0.45	0.5 - 0.7	0.35 - 1	0.4 - 0.8	0.44 - 0.6	0.4 - 0.75	0.35 - 0.85	0.38 - 0.95	0.4	0.4
		MHz	1 - 20	20 - 200	N-A	60 - 180	60 - 140	0.1 - 6	10 - 65	10 - 1050	40 - 80	32 - 80
	MEP	pJ/ cycle	26 @20 MHz	N-A	N-A	6.88 @100 MHz	11.5 @140 MHz	6.4 @0.5 MHz [†]	6.3 @40 MHz	5.6 @70 MHz	3.3 @40 MHz	5.5 @56 MHz
	Biased Well Area	mm ²	0.25 ⁺	0.9	0.6	0.193	0.918	N-A	0.64 ⁺	2	0.4	0.31
Back-Bias Generation	Area	mm ²	> 0.25⁺	0.009	0.007	0.003 ⁺	0.006	N-A	0.022 ⁺	0.021	0.060	0.032
	Power	μW	N-A	4.15	2.5	N-A	5.3	< 1⁺	6	14	N-A	22[†]
	Settling	μs	N-A	11.5	< 200	N-A	> 200⁺	N-A	N-A	< 200	10	8
	BBN/BBP Range	V	0 to 1.4 0 to -1.4	0 to 1.8 0.4 to -1.5	0 to 1.5 0 to -1.5	-0.2 to 2.4 0.2 to -2.4	-0.2 to 2.4 0.2 to -2.4	0 to 2.2 0.3 to -1	N-A N-A	0 to 1.5 0 to -1.5	0 to 1.8 0 to -3	0 to 1.8 0 to -3
	Asym. Bias	-	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Topology	-	DLL	FLL	PLL	ABB	FLL (PI control)	MEP tracking	ABB	FLL (PI control)	FLL+DLL	FLL (P control)
DL CPR +T ^o sensor			RO monitors +T ^o sensor	RO CPR +Middle sensor	N/PMOS monitors	N/PMOS RO monitors	CPR +I _{eff} PIS	N/PMOS monitors	Timing monitors +I _{on} PIS	BBCO +DL PIS	BBCO +RO PIS	
N-A			CP+SCCP	CP+SCCP	N-A	SCCPs	CPs Ext. supply	CPs	SCCPs	CP+SCCP 2 nF ext. cap.	DCOs+SCCPs	

⁺Estimated from publication. [†]ULV domain supplied at 0.55 V. [‡]Including the 64-MHz clock generation. Duty-cycling the imbalance correction can reduce this power level.

Notations: ABB: adaptive back biasing. AVS: adaptive voltage scaling. UFBBR: unified frequency and back-bias regulation. MEP: minimum energy point. DLL: delay-locked loop. FLL: frequency-locked loop. PLL: phase-locked loop. P control: proportional control. I control: integral control. DL: delay line. RO: ring-oscillator. BBCO: back-bias controlled oscillator. CPR: critical path replica. T^o: temperature. PIS: process imbalance sensor. CP: charge-pump. SC: switched-capacitor. DCO: digitally-controlled oscillator.

3.6 Conclusion

In this final chapter, we focus on the clock generation and PVT compensation in ULV/ULP MCUs in the context of IoT applications.

We first review several system-level adaptive techniques commonly used to cover the PVT variations in ULV circuits, such as adaptive voltage scaling (AVS), adaptive back biasing (ABB), and unified frequency and voltage regulation (UFVR). We then propose a new adaptive mechanism enabled by FDSOI technology: the unified frequency and back-bias regulation (UFBBR). As its name suggests, this new technique unifies the MCU clock generation with adaptive FBB for the PVT compensation. It is similar to UFVR but relies on ABB instead of AVS for the PVT compensation. Consequently, it uses a BBCO as TRO. The UFBBR technique takes the best of ABB and UFVR worlds, by: i) being able to correct the N/PMOS process imbalance, ii) compensating for the increased leakage due to high temperatures, and iii) being robust against fast supply voltage droops.

We experimentally demonstrate the UFBBR benefits with two chip prototypes manufactured in 28-nm FDSOI technology. Our two UFBBR designs lie in two different MCU SoCs, respectively named SleepRunner [JP3] and SleepRider [CP2]. Compared to other ABB generators in the literature, our UFBBR proposals showcase an excellent trade-off between settling time, power, and area. However, the most significant benefits brought by the proposed UFBBR mechanism lie at the MCU level.

The UFBBR macros provide PVT compensation for the entire MCU digital logic and ULP SRAMs, including against asymmetric skewed process corners. Measurements demonstrate a wide-range temperature compensation capability. But unlike ABB systems, the UFBBR units also generate the MCU system clock up to 80 MHz and provide robustness to voltage droops.

Our UFBBR prototypes also enable an energy-efficient MCU operation at ULV/ULP in active mode. Record energy values of 3 $\mu\text{W}/\text{MHz}$ at 40 MHz and 5.5 $\mu\text{W}/\text{MHz}$ at 56 MHz are reached by SleepRunner and SleepRider, respectively. In addition, in sleep mode, the UFBBR macros disable the clock generation and drive the FBB voltages towards 0 V to save power. The resulting sleep power at the MCU level is lowered to 12.7 and 7.7 μW for SleepRunner and SleepRider, respectively, with logic state and memory retention. Finally, thanks to fast transitions between sleep and active modes, they also minimize the wake-up/going-to-sleep overheads.

All these results demonstrate the relevance of the UFBBR concept for ULV/ULP applications.

Conclusions and Perspectives

Compared to the mainstream bulk CMOS counterparts, the FDSOI technology brings new possibilities and degrees of freedom in the design of integrated circuits, in particular thanks to its forward back-biasing (FBB) feature. FBB reduces the transistors threshold voltage by increasing BBN (resp. decreasing BBP), the NMOS (resp. PMOS) back-bias voltage. In this dissertation, we exploit this feature for ultralow-voltage/ultralow-power (ULV/ULP) circuit operation to improve the energy efficiency while compensating for the detrimental effects of exacerbated process, voltage, and temperature (PVT) variations to improve circuit robustness. The corresponding silicon area must stay limited to enable highly integrable design solutions. These goals match the requirements of the Internet-of-Things (IoT) while being applicable also in other ULV/ULP applicative contexts. We pursue them in the domains of clock generation and frequency synthesis by raising the three following research questions:

Question 1: *How do FDSOI-enabled BBCOs compare to conventional CSROs?*

Question 2: *How to exploit FBB in BBCO-based PLLs?*

Question 3: *How to fully exploit FBB in adaptive regulation loops for unified clock generation/PVT compensation in ULV/ULP circuits?*

We respectively address these three questions in three different chapters. Their conclusions rely on analytical developments, modeling, and simulation-based analysis, reinforced by experimental results from the design of three chip prototypes manufactured in 28-nm FDSOI technology. Let us take a step back, outline answers, provide recommendations, and draw perspectives.

Contributions

The first research question concerns two ring oscillator (RO) topologies: the FDSOI-enabled back-bias-controlled oscillator (BBCO) and the conventional current-starved ring oscillator (CSRO). Chapter 1 takes a block-level perspective to compare them. Based on extensive simulation results supported by compact analytical models, our comprehensive analysis focuses on the minimum power consumption and the best power/phase noise achievable in 28-nm FDSOI technology. We also take practical design constraints such as PVT robustness, frequency tuning range, and frequency gains into account.

As outcomes of the proposed comparison, we observe numerous advantages for the

BBCO architecture. Indeed, BBCOs benefit from a low degree of transistor stacking, yielding a lower device count and reduced associated noise/parasitics compared to CSRO counterparts. They also experience a threshold voltage reduction induced by FBB. These features help the BBCO topology i) operate at lower supply voltages and thus lower power, and ii) reach better power/phase noise trade-offs. In addition, BBCOs also exhibit a more linear transfer function.

Claim 1: *Benefiting from the efficient FBB of FDSOI technology, BBCOs can operate at lower power levels, reach better power/phase noise trade-offs, and have more linear transfer functions than their CSRO counterparts.*

However, the use of FBB also raises design challenges at the block and system levels. Indeed, despite their linear gains, BBCOs have a lower frequency gain and, therefore, a lower frequency tuning range than CSROs. There is also a challenge concerning BBP because it takes negative values and ranges from 0 to -3 V. Its on-chip generation usually requires charge pumps (CPs), with unknown system-level impacts in terms of power and phase noise performance. Finally, due to the deep N-well sharing between NMOS and PMOS transistors, there is a parasitic coupling capacitance between BBN and BBP voltages. It constitutes a threat to the stability of BBCO-based feedback-loops, such as phase-locked (PLLs) or frequency-locked loops (FLLs), for instance. In Chapters 2 and 3, we illustrate the use of BBCOs and address the previously discussed challenges with their implementation on silicon in concrete prototypes and targeting applications linked to clock generation and frequency synthesis.

The second research question relates to the design implications of using a BBCO inside PLLs. We cover this topic in Chapter 2 by presenting an efficient dual-PLL clock recovery (CR) embedded within a 2.5-Gb/s ultra-wideband (UWB) radio. The proposed UWB transceiver aims at wireless low-power chip-to-chip communications over short distances. The CR comprises two complementary PLLs: the first uses a phase-frequency detector (PFD) to achieve a fast frequency acquisition within the preamble; the second relies on a half-rate multi-level phase detector (HR ML-BBPD) for high-bandwidth phase tracking. Both PLLs share the same BBCO and use the FBB voltage nodes as frequency control knobs.

As in conventional PLLs, the CR drives BBN with its CPs through a lead-lag low-pass filter (LPF). We generate BBP from BBN by adding a BBP driver comprising process imbalance sensors (PISs) and a back-gate driven amplifier. The proposed independent BBN/BBP generation extends the natural PVT compensation capability of the PLLs to asymmetric skewed process corners. Besides, FBB enables a low-voltage and low-power operation at the system level. However, the inherent BBP driver delay and the parasitic BBN/BBP coupling capacitance of conventional FDSOI layouts threaten the CR stability. We prevent this issue by i) sufficiently strengthening the amplifier in the BBP driver to increase its bandwidth compared to the PLLs one and ii) avoiding the deep N-well shared between NMOS and PMOS transistors at the origin of the unwanted parasitic BBN/BBP coupling.

The proposed CR unit showcases competitive experimental results in terms of power, performance, and area. The CR unit locks in less than 1.1 μs , consumes 1.034 mW in lock conditions, generates 6.5 ps of RMS long-term jitter, and occupies a limited silicon surface of 0.043 mm². Consequently, it is energy-efficient and exhibits an excellent power/jitter trade-off. Besides, it helps the entire UWB transceiver achieve a measured energy value of 2.36 pJ/bit. These results demonstrate the relevance of FBB in the context of low-power PLLs.

Claim 2: *Thanks to FBB, PLLs efficiently operate at low voltage and are low power and robust to PVT variations. We achieve these goals in a concrete CR prototype example incorporating the following innovations:*

- a) *a dual-PLL architecture to alleviate the trade-off between start-up time and low in-lock power;*
- b) *a BBCO serving as a voltage-controlled oscillator for its low-power feature and its good power/phase noise compromise;*
- c) *a BBP driver comprising PISs and a back-gate driven amplifier for the independent generation of BBP from BBN and the compensation of PVT variations, including asymmetric skewed process corners;*
- d) *a custom layout for the BBCO and PISs to avoid the parasitic BBN/BBP coupling challenge.*

The last research question focuses on the clock generation and PVT compensation in ULV/ULP circuits. Chapter 3 covers this topic in the context of ULV/ULP microcontroller units (MCUs) for the IoT. Taking inspiration from other system-level adaptive techniques commonly used to cover PVT variations in ULV circuits, we propose a new adaptive concept: the unified frequency and back-bias regulation (UFBBR). As its name suggests, it unifies MCU clock generation with adaptive FBB for the PVT compensation. We demonstrate the benefits of this new technique with its implementation in two MCU prototypes.

A UFBBR unit compensates for PVT variations, affecting both the logic speed and the N/PMOS process imbalance of the circuit to regulate, using asymmetric adaptive FBB. Our second UFBBR version (the most advanced of the two proposed prototypes) uses a unified dual-output FLL comprising sensors, a control unit, and FBB actuators. A BBCO simultaneously serves as a clock generator and logic speed sensor. We propose a digital N/PMOS PIS made of N/PMOS-sensitive ROs. The sensors and the control unit employ standard cells and lie within the MCU digital logic. Digitally-controlled oscillators (DCOs) followed by switched-capacitor charge pumps (SCCPs) serve as BBN/BBP actuators. Their design is custom and done at the transistor level. Due to the use of standard cells in the MCU digital logic, the parasitic BBN/BBP coupling challenge is not avoidable. The design of the UFBBR takes it into account, and its FLL architecture is stable without requiring any external component.

Compared to other adaptive back-biasing (ABB) generators in the literature, our UFBBR prototypes appear very competitive, showcasing a fast settling time ($< 10 \mu\text{s}$) for limited power ($< 22 \mu\text{W}$) and area ($< 0.06 \text{ mm}^2$) overheads. They provide PVT compensation for the entire MCU digital logic and custom FBB-compatible ULP SRAMs, including against asymmetric skewed process corners. Measurements demonstrate a wide-range temperature compensation capability. Unlike ABB systems, the UFBBR units also generate the MCU system clock up to 80 MHz and provide robustness to voltage droops. We demonstrate minimum energy values of 3-5.5 $\mu\text{W}/\text{MHz}$ in active mode at the MCU level. In sleep mode, the UFBBR macros disable the clock generation and drive the FBB voltages towards 0 V, resulting in an MCU sleep power of 7.7-12.7 μW with logic state and memory retention. Thanks to fast transitions between sleep and active modes, they also minimize the wake-up/going-to-sleep overheads. All these features demonstrate the relevance of the UFBBR concept for ULV/ULP applications.

Claim 3: *The unification of clock generation and PVT compensation through adaptive FBB provides crucial system-level benefits, such as an efficient circuit operation at ULV, a wide-range PVT compensation, and robustness against supply voltage droops. We reach these objectives with the implementation of UFBBR units embedded in ULP/ULV MCU prototypes and featuring the following innovations:*

- a) *a unified dual-output FLL regulating both the circuit speed and the N/PMOS process imbalance through adaptive FBB;*
- b) *a BBCO serving as a clock generator and logic speed sensor and a digital N/PMOS PIS made of N/PMOS-sensitive BBCOs;*
- c) *sensors and a control part employing standard cells to ensure a good correlation and a deep integration with the digital logic to regulate;*
- d) *DCOs followed by SCCPs for a fast proportional current actuation and a matched parallel BBN/BBP generation;*
- e) *a stable and robust architecture that takes the unavoidable parasitic BBN/BBP coupling capacitance into account without requiring any external component.*

In light of these three different contributions, graphically summarized in Fig. S.1, the FBB feature of FDSOI proves to be an efficient and flexible tuning knob for the design of integrated circuits. It enables ULV/ULP circuits operation while extending their functionality to a broader range of PVT conditions, with limited power and area overheads. It is thus perfect for IoT and biomedical applications. Besides the applicative examples covered in this dissertation (PLLs, FLLs, ULP MCUs), the FBB can also benefit to other circuit types including RO-based ADCs [CP2, 18] or wake-up radios [49], for instance. We also see a potential benefit of FBB and UFBBR in multiprocessor system on chips (MPSoCs) using multiple FBB islands [93, 94], which would definitely require further improvements and analysis.

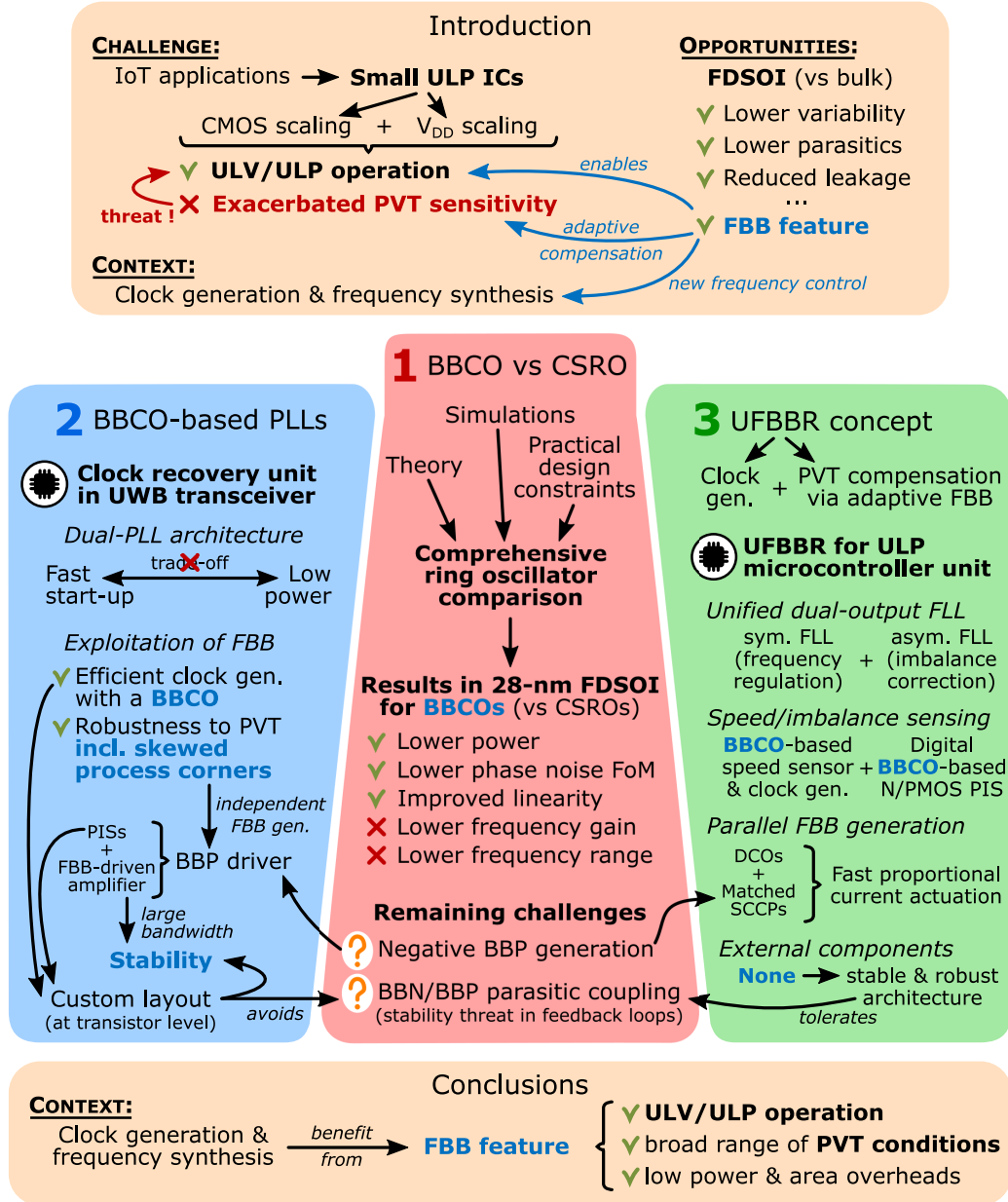


Fig. S.1 Summary of the thesis contributions.

Table S.1 Comparison of three possibilities for the negative BBP generation.

	Strategy 1 No BBP Generation	Strategy 2 Linear BBP Driver	Strategy 3 SCCP BBP Driver
Advantages	+ simple design + no BBN/BBP coupling	+ N/PMOS process imbalance correction + low ripple + low noise + simple design	+ N/PMOS process imbalance correction + fast + high efficiency + no negative supply
Drawbacks	- low BBCO linearity - low BBCO gain/range - no N/PMOS process imbalance correction	- low efficiency - negative supply - high sensitivity to BBN/BBP coupling	- high ripple - higher switching noise - complex design
Applications	High supply voltage, high-performance ap- plications, with no sensitivity to N/PMOS process imbalance	Medium supply voltage, noise-sensitive applica- tions, with relaxed power requirements (e.g., PLLs, radios, analog circuits)	Low supply voltage, low- power applications, with relaxed noise constraints (e.g., ULP MCUs and dig- ital circuits, IoT)

Recommendations

Building upon the learning outcomes of this dissertation, we can propose several recommendations regarding the two encountered design challenges associated with the use of BBCO, i.e., the negative BBP generation and the BBN/BBP parasitic coupling.

As a reminder, we identified two strategies to tackle the BBN/BBP parasitic coupling challenge: A) estimate and tolerate the experienced parasitic coupling and size the circuit accordingly; or B) cancel the coupling by avoiding the deep N-well sharing between NMOS and PMOS transistors. Choosing between these two possibilities mainly depends on the presence (or not) of digital standard cells in the design, the requirements of the circuit (speed, area, settling time, stability), and the type of BBP² actuation. This brings us to the discussion of the second challenge.

According to the literature and as experienced in our works, we identify three possible strategies to generate the negative BBP voltage: 1) avoid generating BBP by tying it to ground as in [52]; 2) rely on a linear BBP actuator as in [JP2, 34]; 3) use BBP SCCPs as in [JP3, JP4]. Table S.1 qualitatively compares these three solutions³.

Avoiding the generation of BBP (strategy 1) is easy to implement and naturally

²If a circuit employs FBB, we assume it uses BBN for sure because the latter is positive and thus easier to generate than BBP. There remains, therefore, the choice to also generate BBP (or not).

³We can draw a parallel with the comparison of on-chip positive voltage regulation provided in [95].

avoids the BBN/BBP coupling challenge, but it comes with several drawbacks which we must consider. Indeed, using BBN as a unique BBP tuning knob might negatively impact its linearity, frequency gain, and frequency range, as mentioned in Section 2.2.2. Of course, strategy 1 is unable to correct the N/PMOS process imbalance. We thus recommend strategy 1 for high-voltage high-power circuits, for which these drawbacks are of lower importance.

The second possibility (strategy 2) is to use a linear BBP driver. Chapter 2 gives an example comprising a back-gate driven amplifier in a closed-loop with N/PMOS PISs. This analog solution exhibits a low ripple and noise but suffers from a low power conversion efficiency. Moreover, it requires a negative supply voltage, whose on-chip generation would further degrade the efficiency. Furthermore, from our experience, this strategy seems to be more sensitive to the BBN/BBP parasitic coupling challenge (compared to strategy 3), which forced us to oversize our BBP driver design in Chapter 2 to maintain the stability at the expense of power consumption. There is thus a trade-off between power, settling time, stability, and BBN/BBP parasitic capacitances, which must absolutely be taken into account. We recommend opting for strategy 2 in noise-sensitive applications with relaxed power requirements. Examples can include PLLs or radios. We also recommend cancelling the BBN/BBP parasitic coupling challenge with a custom layout at the transistor level, to avoid the deep N-well sharing between NMOS and PMOS transistors (strategy B), as done in Chapter 2, provided there is no stringent constraint on the silicon area.

The final solution (strategy 3) relies on SCCPs for the BBP generation, as done in Chapter 3 and many other works in the literature (see Table 3.5). It does not require a negative supply voltage and exhibits higher efficiency than a linear BBP driver counterpart. Its principal drawbacks are higher noise and ripple (due to the capacitors switching). We recommend choosing strategy 3 for low-voltage low-power applications with relaxed noise requirements, such as ULP MCUs and other types of digital circuits. If the application involves digital standard cells, then there is no choice but to tolerate the BBN/BBP parasitic coupling challenge (strategy A).

Note that this analysis could be extended to the BBN generation, for which we must also consider solutions based on current CPs as in [JP3] or digital-to-analog converters (DACs) as in [34].

Perspectives

To end this dissertation, we broaden the discussion by proposing several areas for improvement and perspectives for future works. We list our ideas following the thesis outline, as represented in Fig. S.2.

Extension of the RO comparison: The RO comparison of Chapter 1 concerns

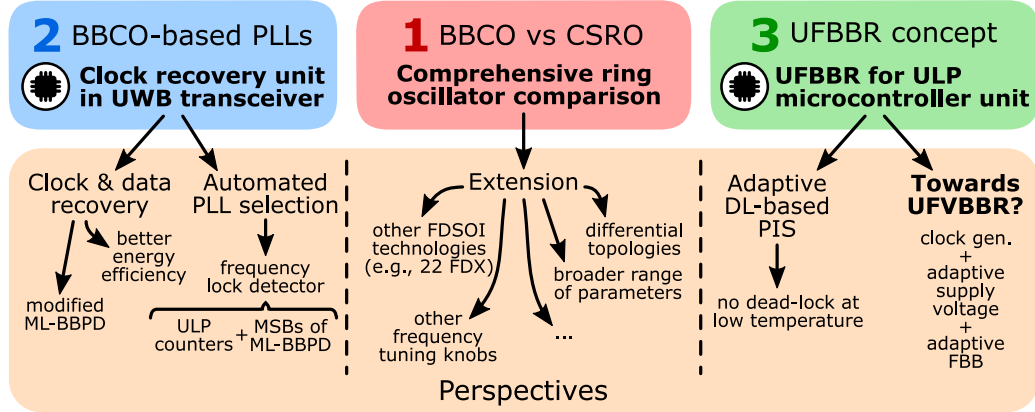


Fig. S.2 Thesis perspectives.

single-ended topologies, focuses on BBCOs and CSROs, considers a limited range of values for the RO parameters (transistors dimension, number of stages, target frequencies), and is limited to the 28-nm FDSOI technology from STMicroelectronics. For more universality and completeness in the comparison results, future works may extend our analysis in the following ways: 1) include differential RO structures; 2) combine back-bias control and current starving; 3) consider other frequency tuning knobs, such as supply voltage or loading capacitors; 4) broaden the range of considered RO parameter values; 5) apply the analysis to 22-nm FDSOI technology node from Global Foundries; 6) consider regular- V_{th} devices and a reverse back-biasing scheme.

Clock and data recovery instead of clock recovery: The CR unit we propose in Chapter 2 operates with high energy efficiency benefiting the entire UWB transceiver. As a reminder, the radio uses a binary pulse-position modulation (PPM). From the envelope of the received PPM UWB signal, the CR recovers a 2.5-GHz clock. The transceiver then utilizes it to demodulate the received data. We believe that changing the proposed CR unit into a clock and data recovery (CDR) unit could bring additional energy reductions at the system level in a future prototype version. The idea would be to modify the HR ML-BBPD to recover the hidden data. Indeed, as the ML-BBPD samples the envelope signal multiple times, it should be possible to recover the corresponding data from its internal nodes with limited overheads.

Automated switching from start-up PLL to main PLL in the CR unit: In our CR prototype presented in Chapter 2, an external signal (**STARTUP**) controls the switching from the start-up PLL to the main PLL. In a more advanced system, we could automate this switching. To reach this goal, the CR unit would need to detect when its PFD-based start-up PLL is properly locked. As mentioned in Chapter 2, an idea would be to use the most significant output bits (MSBs) of the ML-BBPD, whose absence of activity indicates the main PLL is in range for

phase locking. Therefore, we could use a simple lock detector comprising low-power counters clocked by the CR output clock and reset by the MSBs of the ML-BBPD. We expect little power and area overheads for such a solution.

Adaptive PIS based on delay lines: For the compensation of asymmetric skewed process corners, UFBBR systems need to sense the N/PMOS process imbalance. In Chapter 3, for our first UFBBR prototype, we propose digital N/PMOS PISs made of N/PMOS-sensitive delay lines (DLs). Comparing the propagation delay of these two DLs provides binary information concerning the process imbalance. The UFBBR control obtains this information by periodically triggering the PIS using a falling (resp. rising) edge at the input of the NMOS-sensitive DL (resp. PMOS-sensitive DL). In-between two successive sensing steps, the UFBBR control must reset the PIS by feeding the NMOS-sensitive DL (resp. PMOS-sensitive DL) with a rising (resp. falling) edge. This periodic triggering and reset mechanism creates an issue at low temperatures because of too long delays for the DLs compared to the PIS refreshment period, especially at start-up ($BBN = BBP = 0$ V), as mentioned in Section 3.3.3. A simple solution would be to use an adaptative scheme instead of a periodic one. The DL-based PISs could inform the UFBBR controller when to be sampled or reset by detecting when the input edges have fully propagated through their DLs. This solution would require minimal modifications of the PISs, resulting in limited power and area overheads.

Towards a unified frequency, voltage, and back-biasing regulation?

In the literature, combining the clock generation with adaptive voltage scaling (AVS) proves to be useful for robustness against symmetric PVT variations and tolerance to voltage droops in ULV/ULP circuits. This technique is referred to as unified frequency and voltage regulation (UFVR). In Chapter 3, we take inspiration from UFVR by combining the clock generation with ABB instead of AVS, assuming a fixed supply voltage. This leads to the UFBBR concept. The advantages over UFVR systems are the robustness against asymmetric PVT variations and the compensation of the increased leakage at high temperatures. In this dissertation, when we study the UFBBR concept, we assume an ideal and perfect voltage regulator (VR) for the ULV voltage generation. However, an issue could appear in practice from the interaction of the UFBBR with the VR, for instance at high temperature inducing high leakage. In this situation, if the leakage is too excessive compared to the VR maximal output current, IR drops appear. Consequently, the ULV voltage drops, and the digital logic becomes slower. The UFBBR unit then reacts by increasing the FBB voltages (in absolute value) to compensate for this logic speed drop. Unfortunately, by doing so, the leakage becomes even more important, resulting in even higher voltage drops, ultimately making the entire system unstable. Crossing the current limits of the VR thus creates a detrimental positive feedback loop. To prevent this issue, we thus need a study of the interactions between the UFBBR and the VR. The results of such a study might call for the unification of UFVR and UFBBR strategies, resulting in a *unified*

frequency, voltage, and back-bias regulation (UFVBBR) scheme. This technique might extend the generated clock frequency range and adapt the ULV/ULP circuits to a broader range of operating conditions, compared to UFVR/UFBBR taken alone. In terms of implementation details, this UFVBBR concept would necessitate the sensing of a third variable, in addition to logic speed and N/PMOS imbalance. We recommend finding a variable that is easily detectable with digital circuits, to ease the interfacing and integration at the UFBBR architectural level. An idea could be to track the MEP by measuring the ratio of leakage power to dynamic power as in [85] or through a digital power meter as in [96]. Nevertheless, the study and design of this new UFVBBR technique promise exciting challenges to tackle.

Mathematical Developments Related to Ring Oscillators

This appendix gathers the mathematical developments needed to support analytically the simulation-based observations made in Chapter 1. Firstly, Appendix A.1 derives formulas for the oscillation frequency as well as for the power consumption of inverter-based ring oscillators (ROs). Secondly, Appendix A.2 obtains analytical expressions for the phase noise and corresponding figure of merit (FoM) of ROs. Finally, Appendix A.3 compares the frequency gain and linearity of two topologies of voltage-controlled ring oscillators (VCROs).

A.1 Frequency and Power of an Inverter-Based RO

Oscillation Frequency

Assuming a perfect current matching between NMOS and PMOS devices as well as a perfect capacitance matching among the inverting stages, the oscillation frequency f_0 of an N -stage RO supplied by V_{DD} can be expressed as in [38]:

$$f_0 = \frac{I}{N V_{DD} C}, \quad (\text{A.1})$$

where C denotes the total capacitance seen at the output of each inverting stage (sum of the intrinsic parasitic capacitance of the transistors and the possibly added loading capacitor).

Without considering back biasing, the inverters current I taken in strong inversion is given by:

$$I = \beta (V_{DD} - V_{th,0})^2 = \frac{1}{2} \mu C'_{ox} \frac{W}{L} (V_{DD} - V_{th,0})^2. \quad (\text{A.2})$$

The term β regroups the devices dimensions W and L , the mobility μ and the gate-oxide capacitance C'_{ox} per unit of area. The term $V_{th,0}$ denotes the zero-bias threshold voltage. Second-order effects, such as V_{th} roll-off, drain-induced barrier lowering (DIBL), and velocity saturation, are neglected in this work.

Power Consumption

When a given RO inverter switches, it charges to V_{DD} or discharges to ground its output capacitor C , depending on the edge type it sees at its input. Let us briefly describe this process to obtain the RO power consumption.

When a *falling edge* comes at its input, a particular RO inverter *charges* its output capacitor from ground to V_{DD} through its PMOS transistor. The amount of charge taken from V_{DD} is thus equal to:

$$\Delta Q = C V_{DD}. \quad (\text{A.3})$$

Half a period later, the same inverter experiences a *rising edge* at its input and thus *discharges* its output capacitor from V_{DD} back to ground through its NMOS transistor. Consequently, the same amount of charge ΔQ previously taken from V_{DD} is now returned to ground. This charging/discharging process starts again half a period later, with a new falling edge at the inverter input.

Over a complete period $T_0 = 1/f_0$, not one but N inverting stages go through the previously described charging/discharging cycle. The *average RO current* can thus be obtained as follows:

$$I_{RO} = N \frac{\Delta Q}{T_0} = N C V_{DD} f_0 = I. \quad (\text{A.4})$$

We retrieve there the inverter current I defined in (A.2). As only one stage switches at a time, this equation shows that having N stages each consuming a current I during a time interval T_0/N , is equivalent to one stage consuming the same current I but during the entire period T_0 .

The RO power consumption is now easily found:

$$P = I_{RO} V_{DD} = N C V_{DD}^2 f_0 = I V_{DD}. \quad (\text{A.5})$$

It is important to notice that this formula considers only purely *dynamic power* (switching power). It thus neglects static power coming from leakage as well as eventual short-circuit power contributions.

Power Trends at Fixed Oscillation Frequency

In Chapter 1, several ROs are built with different stages N and supplied at different supply voltage values V_{DD} . Their gate length L is tuned to make them all oscillate at a fixed frequency of 2.45 GHz. In this context, this section analyzes the resulting power trends that can be expected, in order to compare them with the simulation results of Section 1.4.3.

In absence of explicit loading capacitor at the output of each inverting stage, the total capacitance C is equal to the sum of the intrinsic parasitic capacitances of the transistors. It is thus proportional to the gate-oxide capacitance per unit of area C'_{ox} and to the devices dimensions W and L :

$$C \propto C'_{ox} W L. \quad (\text{A.6})$$

Plugging (A.2) and (A.6) into (A.1) yields the following relation for the oscillation frequency f_0 :

$$f_0 \propto \frac{(V_{DD} - V_{th,0})^2}{N V_{DD} L^2}. \quad (\text{A.7})$$

As the RO comparison of Section 1.4.3 is made at a fixed oscillation frequency f_0 , this yields the following trends for the gate length L :

- At a fixed V_{DD} value: $L \propto 1/\sqrt{N}$, (A.8)

- At a fixed N value: $L \propto (V_{DD} - V_{th,0})/\sqrt{V_{DD}}$. (A.9)

For the RO power consumption P , the definition given in (A.5) can be rewritten as follows:

$$P = \frac{1}{2} \mu C'_{ox} \frac{W}{L} (V_{DD} - V_{th,0})^2 V_{DD}, \quad (\text{A.10})$$

and a comparison at fixed oscillation frequency f_0 thus yields the following power trends:

- At a fixed V_{DD} value: $P \propto \sqrt{N}$, (A.11)

- At a fixed N value: $P \propto V_{DD}^{3/2} (V_{DD} - V_{th,0})$. (A.12)

They are in good agreement with the results of Figs. 1.7 and 1.8 and confirm the observations made in Section 1.4.3.

A.2 Phase Noise and FoM of an Inverter-Based RO

Phase Noise Induced by Thermal Noise

As shown in [38], the phase noise induced by the *thermal noise* of an N -stage inverter-based RO supplied by V_{DD} and taken at an offset frequency Δf from the carrier frequency f_0 can be expressed as:

$$\mathcal{L}_{wn}(\Delta f) = \frac{2k_B T}{I} \left[\frac{2\gamma}{V_{DD} - V_{th,0}} + \frac{1}{V_{DD}} \right] \left(\frac{f_0}{\Delta f} \right)^2, \quad (\text{A.13})$$

with k_B the Boltzmann constant, T the temperature in Kelvin, and $V_{th,0}$ the zero-bias threshold voltage of the devices. The γ coefficient is equal to $2/3$ for long-channel devices in saturation and takes higher values for short-channel devices [36]. The term I designates the inverting stages current as defined in (A.2). Equation (A.13) assumes matched currents, threshold voltages, and an equal noise contribution between NMOS and PMOS devices.

Phase Noise Induced by Flicker Noise

As shown in [38], the phase noise spectrum induced by the *flicker noise* of an N -stage inverter-based RO supplied by V_{DD} and taken at an offset frequency Δf

from the carrier frequency f_0 can be expressed as:

$$\mathcal{L}_{1/f}(\Delta f) = \frac{1}{8NI^2} S_i^{1/f}(\Delta f) \left(\frac{f_0}{\Delta f} \right)^2, \quad (\text{A.14})$$

where I is the stages current defined in (A.2) and $S_i^{1/f}(f)$ denotes the flicker noise current power spectral density (PSD). For long-channel devices in saturation, the latter is obtained from the flicker noise PSD referred to the gate voltage $S_v^{1/f}(f)$ as follows:

$$S_v^{1/f}(f) = \frac{\kappa_f}{C'_{ox}WL} \frac{1}{f}, \quad (\text{A.15})$$

$$\begin{aligned} S_i^{1/f}(f) &= g_m^2 S_v^{1/f}(f) \\ &= 2I \frac{\mu\kappa_f}{L^2} \frac{1}{f} \propto \frac{1}{L^3} \frac{1}{f}. \end{aligned} \quad (\text{A.16})$$

The parameter κ_f is a process-dependent constant [29], C'_{ox} is the gate-oxide capacitance per unit of area, W and L are the devices dimensions, and μ designates the devices mobility. The term g_m denotes the transistors gate-to-source transconductance. Note that in FDSOI technology, the flicker noise current PSD also has a $1/L^3$ dependence, as verified with simulations and confirmed in [97]. The conclusions drawn from the formulas of this section thus hold for FDSOI as well.

Combining (A.14) and (A.15)-(A.16) yields:

$$\mathcal{L}_{1/f}(\Delta f) = \frac{1}{4NI} \frac{\mu\kappa_f}{L^2} \left(\frac{f_0^2}{\Delta f^3} \right), \quad (\text{A.17})$$

which assumes matched parameters and equal flicker noise current PSDs between NMOS and PMOS devices.

Phase Noise FoM

As defined in Chapter 1 with (1.16), the *phase noise figure of merit* (FoM) normalizes the phase noise $\mathcal{L}(\Delta f)$ by the offset frequency Δf , the oscillation frequency f_0 , and the power consumption P as follows:

$$\text{FoM} = \mathcal{L}(\Delta f) \left(\frac{\Delta f}{f_0} \right)^2 \left(\frac{P}{1 \text{ mW}} \right). \quad (\text{A.18})$$

The total phase noise is naturally obtained by summation of thermal and flicker noise contributions:

$$\mathcal{L}(\Delta f) = \mathcal{L}_{un}(\Delta f) + \mathcal{L}_{1/f}(\Delta f). \quad (\text{A.19})$$

Combining (A.1), (A.5), (A.13), (A.17), (A.19), and (A.18) results in the following

FoM expression for a N -stages inverter-based RO supplied by V_{DD} :

$$\text{FoM} = \underbrace{2000k_B T \left(1 + \frac{2\gamma V_{DD}}{V_{DD} - V_{th,0}} \right)}_{\text{Thermal}} + \underbrace{250 \frac{\mu \kappa_f V_{DD}}{NL^2} \frac{1}{\Delta f}}_{\text{Flicker}}. \quad (\text{A.20})$$

Assuming that $V_{DD} - V_{th,0} = V_{DD}/2$ and $\gamma = 2/3$ as done in [29], the *theoretical best achievable FoM value* for a single-ended RO is thus -165 dBc/Hz at room temperature and in absence of flicker noise.

Different dependences with respect to the RO parameters are observed for (A.20), depending on the noise contribution considered. At the first order, the thermal noise contribution in (A.20) is independent of the number of stages N , the gate length L , and the capacitance C seen at the output of each stage, but increases when decreasing the supply voltage V_{DD} . The flicker noise contribution of (A.20) is at the first order independent of C , and decreases with L , V_{DD} , or when increasing N . These analytical trends are compared to simulation results in Sections 1.4.1 and 1.4.3. A good agreement between analytical and simulation data is generally observed in Chapter 1, despite the first order nature of Equation (A.20).

A.3 Frequency Gain and Linearity of VCROs

Oscillation Frequency of VCROs

Compared to an uncontrolled RO, the oscillation frequency f_0 of a VCRO can dynamically be tuned through a control voltage v_c . For the RO topologies studied in Chapter 1, this control voltage v_c changes the frequency by varying the current I :

$$f_0(v_c) = \frac{I(v_c)}{N V_{DD} C}. \quad (\text{A.21})$$

The control voltage v_c thus corresponds to the gate-to-source voltage FBN and to the body-to-source voltage BBN , respectively for the *current-starved ring oscillator* (CSRO) and *back-bias controlled oscillator* (BBCO) topologies considered here. These VCROs are described in Section 1.3.

The current I is now function of v_c as follows:

- For CSROs: $I(v_c) = I(FBN) = \beta (FBN - V_{th,0})^2$, (A.22)

- For BBCOs: $I(v_c) = I(BBN) = \beta (V_{DD} - V_{th,0} + \gamma_b BBN)^2$. (A.23)

The term β regroups the devices dimensions W and L , the mobility μ and the gate-oxide capacitance C'_{ox} per unit of area. The term $V_{th,0}$ denotes the zero-bias threshold voltage while γ_b designates the body factor parameter which typically ranges from 70 to 85 mV/V in 22/28-nm FDSOI technology [14, 16, 18]. Second-order

effects, such as V_{th} roll-off, drain-induced barrier lowering (DIBL), and velocity saturation, are once again neglected.

The oscillation frequency formula given in (A.21) can be approximated with a second-order Taylor series expansion around a nominal control value v_c^* like this:

$$f_0(v_c) \approx f_0(v_c^*) + k_1 (v_c - v_c^*) + k_2 (v_c - v_c^*)^2. \quad (\text{A.24})$$

The parameter k_1 designates the *VCRO frequency gain* while k_2 is the first non-linear term and is thus linked to the *linearity of the VCRO transfer function*. They are respectively defined as:

$$k_1 = \frac{\partial f_0}{\partial v_c}(v_c^*) = \frac{1}{N V_{DD} C} \frac{\partial I}{\partial v_c}(v_c^*), \quad (\text{A.25})$$

$$k_2 = \frac{1}{2} \frac{\partial^2 f_0}{\partial v_c^2}(v_c^*) = \frac{1}{2 N V_{DD} C} \frac{\partial^2 I}{\partial v_c^2}(v_c^*). \quad (\text{A.26})$$

Frequency Gain Comparison

For CSRO and BBCO topologies respectively, applying (A.25) to (A.22)-(A.23) results in the following expression for their corresponding frequency gain:

$$k_{1,\text{CSRO}} = \frac{2 \beta}{N V_{DD} C} (FBN - V_{th,0}), \quad (\text{A.27})$$

$$k_{1,\text{BBCO}} = \frac{2 \gamma_b \beta}{N V_{DD} C} (V_{DD} - V_{th,0}). \quad (\text{A.28})$$

As can be observed, there is at least a factor $1/\gamma_b \approx 13\times$ of frequency gain decrease for BBCOs compared to CSROs. Similar developments were conducted in [18] and lead to the same observation. These analytical developments confirm the observations made in Section 1.5.1 from the results of Figs. 1.10 and 1.11. The conclusions also hold if weak inversion is assumed for (A.22)-(A.23) instead of strong inversion.

Linearity Comparison

For CSRO and BBCO topologies respectively, applying (A.26) to (A.22)-(A.23) results in the following expression for their corresponding first nonlinear term:

$$k_{2,\text{CSRO}} = \frac{\beta}{N V_{DD} C}, \quad (\text{A.29})$$

$$k_{2,\text{BBCO}} = \frac{\gamma_b^2 \beta}{N V_{DD} C}. \quad (\text{A.30})$$

The ratio of these two quantities is equal to $1/\gamma_b^2 \approx 169$, which means that, all other things being similar, BBCOs have a more linear transfer function than their

CSRO counterparts. These analytical developments confirm the observations made in Section 1.5.1 from the results of Figs. 1.10 and 1.11. The conclusions also hold if weak inversion is assumed for (A.22)-(A.23) instead of strong inversion.

Clock Recovery Modeling

This appendix provides a continuous-time model of the clock recovery (CR) unit proposed in Chapter 2. It demonstrates how to model in the Laplace domain phase-locked loops (PLL) comprising a back-bias-controlled oscillator (BBCO) and a BBP driver to fully exploit the forward back-biasing (FBB) feature of FDSOI technology. Firstly, Appendix B.1 briefly analyzes the phase detectors (PDs) characteristics. Appendix B.2 then provides a model combining the BBCO, the BBP driver, and the low-pass filter (LPF) together. Finally, Appendix B.3 presents the entire CR closed-loop model.

B.1 Phase Detectors Characteristics

As described in Section 2.4, the CR unit proposed in Chapter 2 comprises two complementary PLLs. On the one hand, the start-up PLL uses a conventional phase-frequency detector (PFD) for a fast frequency acquisition within the preamble. On the other hand, the main PLL employs a half-rate (HR) multi-level bang-bang phase detector (ML-BBPD) for a high-bandwidth phase tracking within the data payload.

This section focuses on the PDs and obtains their linearized gain value from their transfer function, as illustrated in Fig. B.1. Both PDs output an error signal $e(t)$ whose average value depends on the phase difference $\Delta\Phi = \Phi_{ref} - \Phi_{out}$ between input and output PLL clocks.

Conventional Phase-Frequency Detector

The conventional PFD has two output signals, **up** and **dn** (see Figs. 2.1 and 2.6, for instance) and its error signal $e(t)$ is simply given by:

$$e(t) = \text{up}(t) - \text{dn}(t). \quad (\text{B.1})$$

Fig. B.1(a) shows the corresponding transfer function. As can be observed, when the input and output PLL clocks are perfectly aligned (i.e., when $\Delta\Phi = 2\pi k$, with k being an integer), there is no activity on **up** and **dn** signals, and the PFD average error is ideally zero. When the input reference clock leads the output clock (i.e., when $\Delta\Phi > 0$), there is more activity for **up** than for **dn**, which results in a positive PFD average error and indicates the PLL must speed up the output clock. Similarly, when the input reference clock lags the output clock (i.e., when $\Delta\Phi < 0$), there is more activity for **dn** than for **up**, which results in a negative PFD average error and indicates the PLL must slow down the output clock. The PFD exhibits

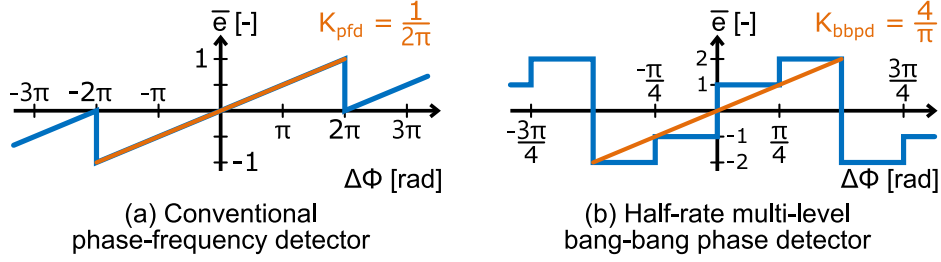


Fig. B.1 Transfer functions of the phase detectors used in the clock recovery unit.

a linear characteristic on the range between -2π and $+2\pi$, and its gain simply equals:

$$K_{pfd} = \frac{1}{2\pi} \text{ rad}^{-1}. \quad (\text{B.2})$$

Half-Rate Multi-Level Bang-Bang Phase Detector

The HR ML-BBPD uses five BBCO clock phases to produce four outputs (see Fig. 2.6) respectively named **up1**, **up2**, **dn1**, and **dn2**¹. The corresponding PD error signal $e(t)$ is:

$$e(t) = \text{up2}(t) + \text{up1}(t) - \text{dn1}(t) - \text{dn2}(t). \quad (\text{B.3})$$

Fig. B.1(b) shows the HR ML-BBPD transfer function. The non-linear bang-bang nature of this type of PD gives this stair-like shape with discretized values for the average error. For the purpose of obtaining a linear model for the entire PLL-based CR, we linearize the ML-BBPD characteristic on the range between $-\pi/2$ and $+\pi/2$ to obtain its gain:

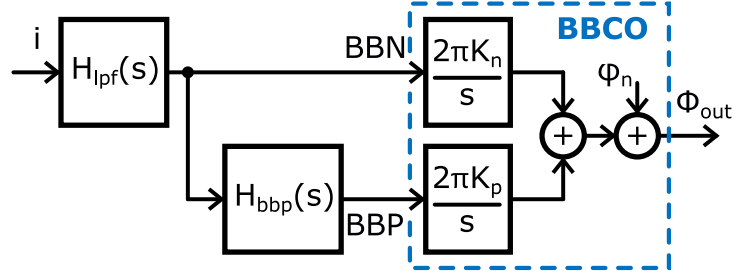
$$K_{bbpd} = \frac{4}{\pi} \text{ rad}^{-1}. \quad (\text{B.4})$$

We can interpret this value as being the PD gain *averaged* on its input phase range. The ML-BBPD thus exhibits an $8\times$ higher gain than its PFD counterpart, enlarging the main PLL bandwidth compared to the start-up PLL one. In practice, for low input phase errors (for $\Delta\Phi \approx 0$), the ML-BBPD gain is even broader and theoretically tends towards infinity, further increasing the main PLL bandwidth.

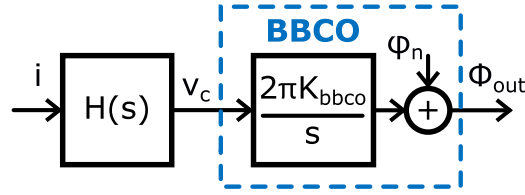
B.2 LPF, BBP Driver, and BBCO Combination

In our CR design proposed in Chapter 2, our PLLs exploit the FBB feature of FDSOI technology by two means. They firstly rely on a BBCO for the clock generation, whose frequency is thus dependent on BBN and BBP, the NMOS and PMOS back-bias voltages, respectively. Consequently, BBN and BBP are the PLLs

¹In [57], they are respectively named **late1**, **late2**, **early1**, and **early2**.



(a) Full model.



(b) Equivalent representation.

Fig. B.2 Block diagram representations of the LPF, BBP driver, and BBCO.

control voltages. Secondly, the CR PLLs generate the negative BBP voltage from BBN using a BBP driver located between the LPF and the BBCO.

This section thus focuses on the BBCO and the BBP driver because they lead to significant differences in the PLL topology and behavior compared to a conventional counterpart. We also analyze and model their interaction with the LPF. Note that the LPF, the BBP driver, and the BBCO are the three blocks shared by the two CR constitutive PLLs.

Fig. B.2(a) represents a block diagram in the Laplace domain comprising the LPF, the BBP driver, and the BBCO. The LPF is a lead-lag filter described in Section 2.2.1, and its transfer function $H_{lpf}(s)$ is given in (2.1). For the BBCO, $K_n \approx 315$ MHz/V and $K_p \approx -487$ MHz/V are its frequency gains relative to BBN and BBP, respectively, and φ_n represents its phase noise level. Finally, $H_{bbp}(s)$ denotes the BBP driver transfer function. Let us analyze a little bit more the latter with the help of Fig. B.3.

BBP Driver

Ideally, BBP should be the exact opposite of BBN relative to the ground level, at all frequencies. In other words, we should have $\text{BBP} = -\text{BBN}$ or, equivalently:

$$H_{bbp,ideal}(s) = \frac{\text{BBP}}{\text{BBN}}(s) = -1, \quad (\text{B.5})$$

as shown in blue in Fig. B.3.

However, the BBP driver cannot perform this function for all frequencies in practice.

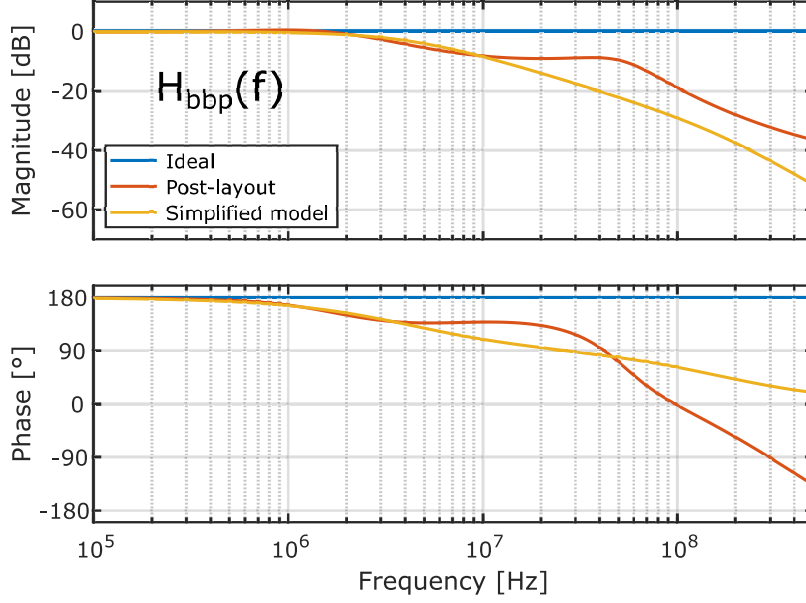


Fig. B.3 Transfer function of the BBP driver.

This situation is shown in orange in Fig. B.3 from a pole-zero analysis performed on a post-layout netlist of the BBP driver. Its characteristic is rather complex as it contains more than 13 poles and 13 zeros. Considering all these poles and zeros in an analytical analysis is not practical. Therefore, we use a simplified model for the BBP driver by reducing its full characteristic to a second-order system. In other words, we assume:

$$\begin{aligned}
 H_{bbp}(s) &= H_{bbp}(0) \frac{1}{(1 + s/p_1)(1 + s/p_2)} \\
 &= H_{bbp}(0) \frac{1}{(1 + s/2\pi f_{p1})(1 + s/2\pi f_{p2})},
 \end{aligned} \tag{B.6}$$

with $H_{bbp}(0) = -0.97$, $f_{p1} = 4.17$ MHz, and $f_{p2} = 170.82$ MHz. This simplified model is illustrated in yellow in Fig. B.3 and approximates well the full BBP driver characteristic up to 10 MHz.

Modeling the LPF, BBP Driver, and BBCO Together

Let us now obtain the transfer function for the block diagram depicted in Fig. B.2(a). In absence of phase noise, we can write:

$$\begin{aligned}
 \left. \frac{\Phi_{out}}{i}(s) \right|_{\varphi_n=0} &= \frac{2\pi}{s} H_{lpf}(s) [K_n + K_p H_{bbp}(s)] \\
 &= \frac{2\pi}{s} H_{lpf}(s) \left[K_n + K_p H_{bbp}(0) \frac{p_1 p_2}{s^2 + s(p_1 + p_2) + p_1 p_2} \right].
 \end{aligned} \tag{B.7}$$

We can now define two new quantities:

$$K_{bbco} = K_n + K_p H_{bbp}(0), \quad (\text{B.8})$$

$$\alpha_k = \frac{K_n}{K_{bbco}}, \quad (\text{B.9})$$

whose respective values are $K_{bbco} = 787 \text{ MHz/V}$ and $\alpha_k = 0.4$, and rework (B.7) as follows:

$$\begin{aligned} \left. \frac{\Phi_{out}}{i}(s) \right|_{\varphi_n=0} &= \frac{2\pi K_{bbco}}{s} H_{lpf}(s) \left[\alpha_k \frac{s^2 + s(p_1 + p_2) + p_1 p_2 \alpha_k^{-1}}{s^2 + s(p_1 + p_2) + p_1 p_2} \right] \\ &= \frac{2\pi K_{bbco}}{s} H_{lpf}(s) \left[\alpha_k \frac{s^2 + s(z_1 + z_2) + z_1 z_2}{s^2 + s(p_1 + p_2) + p_1 p_2} \right] \\ &= \frac{2\pi K_{bbco}}{s} H(s). \end{aligned} \quad (\text{B.10})$$

The zeros z_1 and z_2 appearing in (B.10) are simply obtained as follows:

$$z_{1,2} = \frac{p_1 + p_2}{2} \left(1 \pm \sqrt{1 - \frac{4p_1 p_2}{\alpha_k (p_1 + p_2)^2}} \right). \quad (\text{B.11})$$

Equation (B.10) shows a crucial result. Indeed, we can reduce the combination of the LPF, BBP driver, and BBCO to just two equivalent blocks: an oscillator with a frequency gain K_{bbco} and a filter whose transfer function is $H(s)$. In other words, we can simplify the block diagram of Fig. B.2(a) into the one depicted in Fig. B.2(b). Consequently, from this point, the analysis of BBCO-based PLLs becomes similar to that of conventional PLLs.

Equivalent Filter

We now analyze $H(s)$ in more details, whose expression is fully developed here:

$$\begin{aligned} H(s) &= H_{lpf}(s) \left[\alpha_k \frac{s^2 + s(z_1 + z_2) + z_1 z_2}{s^2 + s(p_1 + p_2) + p_1 p_2} \right] \\ &= \frac{\alpha_k}{s(C_0 + C_p)} \frac{1 + sR_p C_p}{1 + sR_p C_0 C_p / (C_0 + C_p)} \frac{s^2 + s(z_1 + z_2) + z_1 z_2}{s^2 + s(p_1 + p_2) + p_1 p_2} \\ &= \frac{1}{s(C_0 + C_p)} \frac{(1 + s/2\pi f_{z0})}{(1 + s/2\pi f_{p0})} \frac{(1 + s/2\pi f_{z1})}{(1 + s/2\pi f_{p1})} \frac{(1 + s/2\pi f_{z2})}{(1 + s/2\pi f_{p2})}, \end{aligned} \quad (\text{B.12})$$

and whose poles and zeros frequencies are equal to:

$$\begin{array}{l|l} f_{p0} = 47.79 \text{ MHz}, & f_{z0} = 4.78 \text{ MHz}, \\ f_{p1} = 4.17 \text{ MHz}, & f_{z1} = 10.80 \text{ MHz}, \\ f_{p2} = 170.82 \text{ MHz}, & f_{z2} = 164.16 \text{ MHz}. \end{array} \quad (\text{B.13})$$

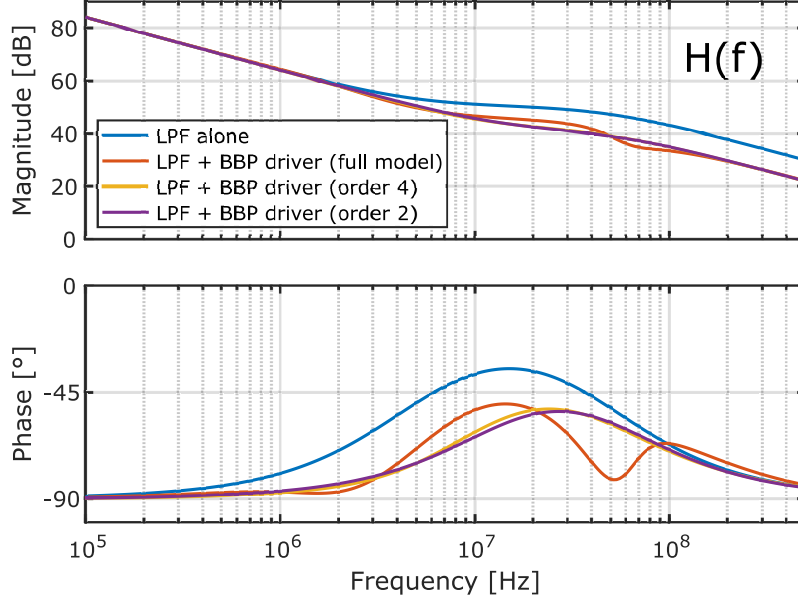


Fig. B.4 Transfer functions of the LPF and of its combination with the BBP driver.

As can be seen, some poles and zeros have very close frequencies and cancel each other. This observation suggests simplifying $H(s)$ further and reducing it to a second-order system:

$$H(s) \approx \frac{1}{s(C_0 + C_p)} \frac{(1 + s/2\pi f_{zd})}{(1 + s/2\pi f_{pd})}, \quad (\text{B.14})$$

with the dominant pole and zero respectively lying at frequencies of:

$$f_{pd} = 54.15 \text{ MHz}, \quad f_{zd} = 13.57 \text{ MHz}. \quad (\text{B.15})$$

Fig. B.4 summarizes our last thoughts. In blue, we see the transfer function of the LPF taken alone. The other curves show the equivalent filter function $H(s)$ and thus illustrate the impact of combining the LPF with the BBP driver. The orange curve considers the full BBP driver model (of order 13). The yellow curve employs the BBP driver second-order model of (B.6), which results in a fourth-order model for $H(s)$ as given in (B.12). The last curve in purple shows the simplified second-order model for $H(s)$ as obtained in (B.14).

As can be observed in Fig. B.4, the main effect of the BBP driver is to move some poles and zeros at higher frequencies. However, the dominant pole and zero of the equivalent filter $H(s)$ in (B.14) are only separated in frequency by a factor of 4. This observation contrasts with the LPF characteristic of (2.1), whose dominant pole and zero are separated by one decade, allowing to neglect the pole and simplifying the PLL analysis. Therefore, despite having a form similar to $H_{lpf}(s)$, we can less

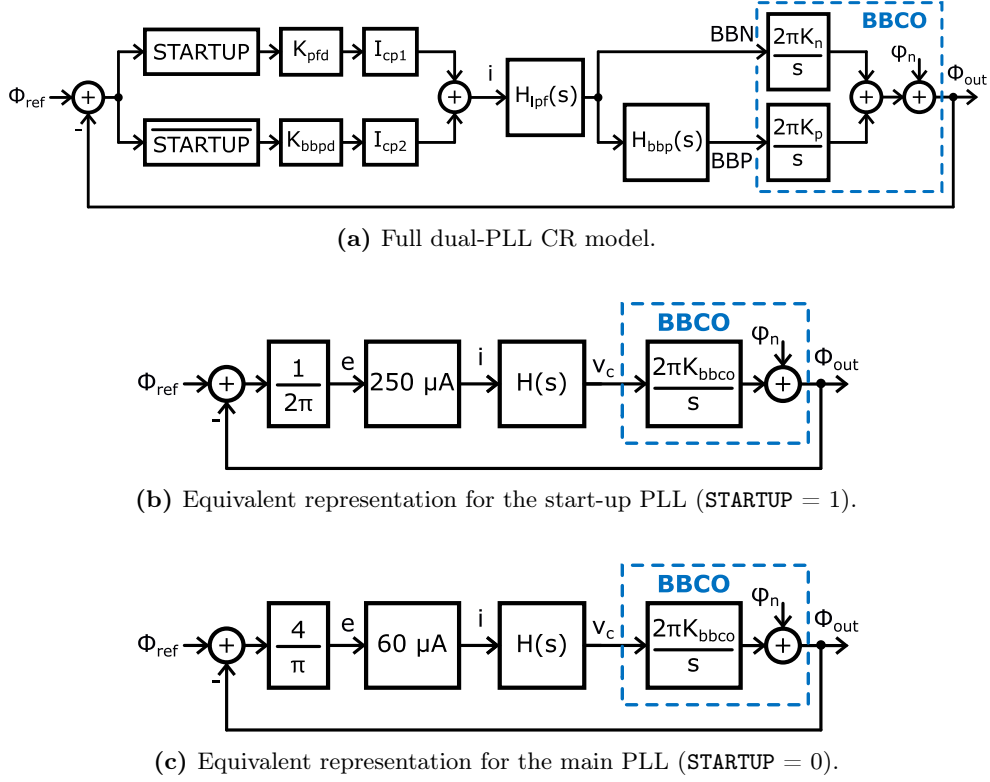


Fig. B.5 Block diagram in the Laplace domain for the CR unit.

easily neglect the dominant pole of $H(s)$.

B.3 Closed-Loop Modeling

We can now obtain a model for the entire closed-loop PLLs of the CR unit. From the CR architecture depicted in Fig. 2.6, we build its detailed block diagram in the Laplace domain, as shown in Fig. B.5(a). As a reminder, the CR unit possesses two complementary PLLs: a start-up PLL and a main PLL. The **STARTUP** signal controls the switching between both PLLs.

With the analysis proposed in the last sections, it is easy to simplify the full block diagram and obtain simple models for each PLL constituting the CR unit. The closed-loop model for the start-up PLL is represented in Fig. B.5(b), while B.5(c) gives the model of the main PLL.

The developments to obtain the corresponding PLLs transfer functions are similar to those of Section 2.2.1, and we thus do not provide them here. Instead, we numerically compute the CR transfer functions and display them in Figs. B.6(a) and B.6(b) for the start-up PLL and the main PLL, respectively. The open-loop transfer function appears in blue, the closed-loop jitter transfer function in orange, and the closed-loop jitter generation function in yellow.

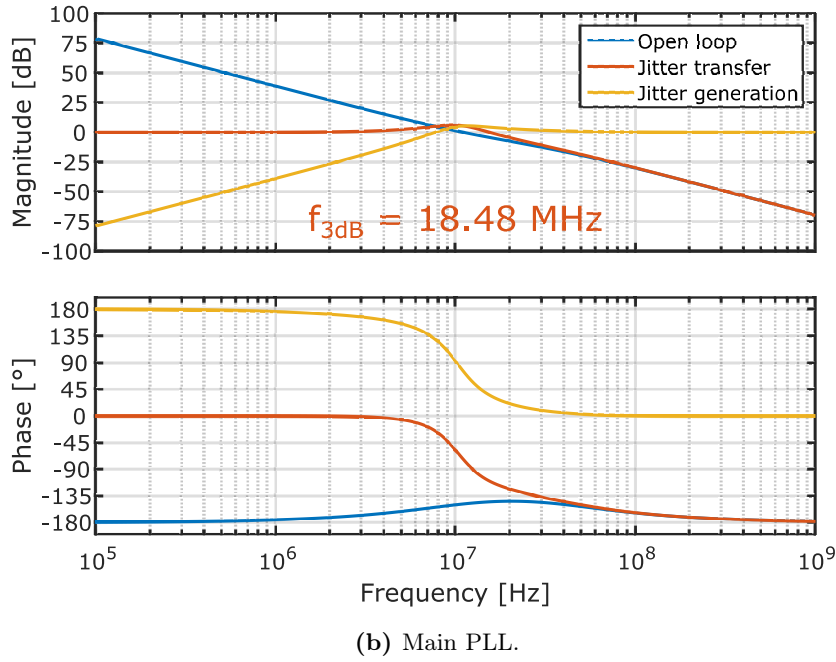
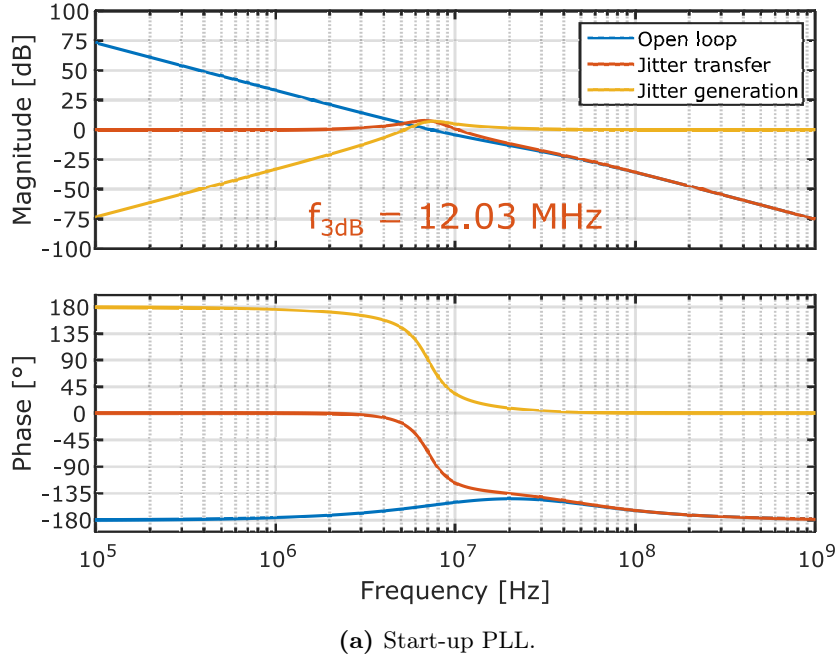


Fig. B.6 Transfer functions of the CR unit obtained from its linear model.

The main difference existing between both CR PLLs lies in their bandwidth. Indeed, our linear model predicts a bandwidth value of 12.03 MHz for the closed-loop start-up PLL. This value is in good agreement with the post-layout simulation and measurement results of Sections 2.4.3 and 2.5. The main PLL reaches a higher

bandwidth thanks to the higher gain of its PD and despite a lower charge-pump current. Its linear model predicts a bandwidth of 18.48 MHz. Compared to the simulation and measurement results of Sections 2.4.3 and 2.5, this value appears rather low and is explained by the linearization of the ML-BBPD characteristic that underestimates its gain value, as discussed in Section B.1.

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