Porous Si as a substrate material for RF passive integration

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Abstract – **Thick porous Si layers locally formed on a low resistivity Si wafer were studied for their application in on-chip RF device integration. A comparison was made between the above porous Si substrate and trap-rich high resistivity Si (trap-rich HR Si), which constitutes a state-of-the-art substrate for RF integration, by integrating identical co-planar waveguide transmission liness (CPW TLines) on both porous Si layer/low resistivity Si and trap-rich high resistivity Si. It was showed that signal attenuation on the porous Si layer is 30% lower than on trap-rich HR Si. This suggests lower losses or better RF shielding in the case of porous Si. In addition, CPW TLines were designed and realized on porous Si substrate for the frequency range 1-110GHz. The measured attenuation constant at 60 and 110GHz was respectively 0.33 and 0.55 dB/mm. This result competes very well with the best literature results on CMOS integrated transmission lines, even though the metal lines in the case of the porous Si substrate were not optimized.**

Keywords – Porous Si; RF passives; RF substrates; coplanar wave–guide transmission lines

I. INTRODUCTION

Passive devices (inductors, transmission lines, filters etc) are essential elements for any RF circuit. On-chip or integrated passives are preferred as a simpler, more cost effective and more efficient alternative to off-chip passives that require complicated interconnects to active circuits and are, in general, bulky. The fabrication of high performance RF integrated passives on the Si wafer is challenging due to losses in the Si substrate. Many different solutions have been applied in the literature to produce high quality on-chip RF passive devices. Solutions that are CMOS compatible are the most promising, as they allow for the integration of RF passives along with the active elements of the RF circuit. Recent state-of-the-art results in the literature were obtained using CMOS processing combined with advanced topologies as the slow-wave shielded co-planar waveguide transmission line (s-CPW TLine) topology [1, 2], or advanced substrate technologies like the thin SOI CMOS technology on high resistivity (HR) SOI substrate [3, 4]. The use of bulk HR Si substrate can be also used, in combination with a trap-rich polysilicon layer underneath the dielectric isolation layer [5, 6]. However, this last solution is not compatible with the low resistivity Si substrate used in CMOS.

A promising solution investigated in this work is the use of a thick porous Si layer as a local substrate on the low resistivity Si wafer, on which the RF passive devices can be integrated. This local substrate can be co-planar with the rest of the wafer and provides a local platform for the co-integration of RF passives with the rest of CMOS ICs. In co-planar wave guide (CPW) transmission lines, the use of a local porous Si substrate is very promising not only for improving the quality factor and reducing the attenuation loss [7-10], but also for offering a very large choice of characteristic impedances, from 20 to more than 150 Ω, due to its low dielectric permittivity. This allows for designing special circuits, like baluns, power dividers, filters, etc. The processing steps on the localized porous Si substrate are CMOS compatible.

In this paper we will present results on the shielding properties of porous Si by integrating CPW TLines on the poprous Si layer and measuring their RF properties. A comparison of this substrate with a trap-rich HR Si substrate will be made by comparing identical CPW TLines on both substrates. CPW TLines on porous Si will be also designed and realized for the frequency range up to 110 GHz and their performance will be compared with that of state-of-the art CMOS substrate technologies and transmission line topologies.

II. EXPERIMENTAL RESULTS AND DISCUSSION

A. Porous Si formation and CPW TLine fabrication

The local formation of porous Si layers on the Si wafer has been described in detail elsewhere [11-12]. Through a masking layer, porous Si is formed locally on the Si wafer by electrochemical etching of Si. Bulk p+ Si wafers with resistivity ~ 5 mΩ.cm were used and the . electrolyte was a mixture of HF/ethanol. A constant

current density of 20mA/cm^2 was applied. The thickness of the porous Si layers used in this work was 150μm. The porosity of the layers was 70%. A schematic of a locally produced porous Si layer on a Si substrate is presented in figure 1 along with a scanning electron microscopy (SEM) picture of the porous Si. It is worth noting that the thickness, the porosity and the structure of the porous Si layer can be tuned by changing the electrochemical conditions used for its formation (time, current, electrolyte concentration etc.). So, the porous Si dielectric properties such as its resistivity and permittivity are easily tunable.

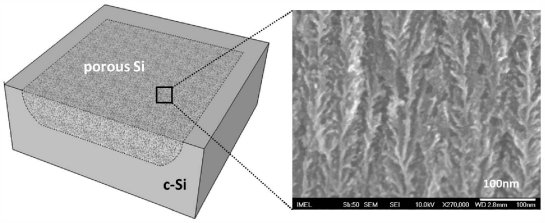

Figure 1. Schematic of a locally produced porous Si layer on the Si substrate. The picture on the right is an SEM picture of the porous Si structure.

CPW TLines were fabricated on the porous Si layers using 1 μm thick Al metallization with a length of 2146μm.

B. Comparison of the porous Si substrate with a trap-rich HR Si substrate

Trap-rich HR Si is a state-of-the art substrate for the integration of high performance RF passive devices [5-6]. A comparison is made between this substrate technology and the local porous Si substrate technology investigated in this work by integrating on both of them identical CPW TLines and measuring in each case their effective permittivity and signal attenuation in the frequency range from 1 to 40 GHz. The nominal resistivity of the HR Si was 10KΩ.cm and a 500 nm thick trap-rich poly-Si layer was deposited on top of it. The use of a trap-rich layer reduces the resistivity degradation at the surface of the HR-Si substrate in the presence of fixed charges in the oxide [5, 6]. On top of both substrates a 500nm thick SiO_2 layer was deposited, on top of which the metal lines were integrated. A schematic representation of the CPW TLines on both substrates is presented in figure 2. The length of the fabricated lines was 2146μm.

The values of the relative permittivity and attenuation constant were then extracted from measurements of the S-parameters of the CPW TLines. It was revealed that the porous Si layer shows reduced relative permittivity ($\varepsilon_{r,eff}$) compared to the trap-rich HR Si substrate. The attenuation constant α. of the CPW TLine on porous Si is also significantly lower than that of the trap-rich HR Si. In fig. 3 the measurements of $\varepsilon_{r,eff}$ and α as a function of frequency are depicted. As it can be seen, the attenuation constant is almost 30% lower in the case of porous Si compared to the trap-rich HR Si. This lower attenuation level is partly related to the higher resistivity of PSi and partly to the higher characteristic impedance of the CPW on porous Si. It is also worth noticing that the substrate losses reduction in the case of the trap-rich HR-Si substrate is limited by the nominal resistivity of the Si wafer, which is not the case for porous Si. It can therefore be inferred that the reduced substrate losses together with the higher achievable characteristic impedance of the CPWs on the porous Si substrate make this material very promising for RF passive integration.

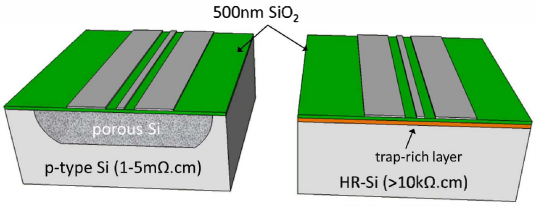

Figure 2. Schematic representation of a CPW TLine on a thick porous Si layer (left) and on HR-Si with a trap-rich layer (right). The signal and ground metal lines (w and w_g respectively) are in grey color.

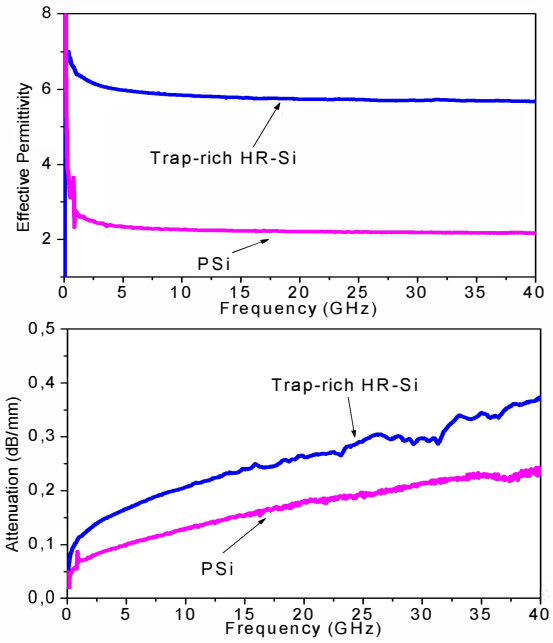

Figure 3. Effective dielectric permittivity ($\varepsilon_{r,eff}$) and attenuation constant α as a function of frequency of the CPW TLine on the trap-rich HR-Si substrate (blue line) and porous Si (pink line).

C. Broadband electrical characterization of CPW TLines on porous Si in the frequency range 1-110 GHz

We designed and characterized CPW TLines up to 110GHz in order to further demonstrate the RF shielding properties of porous Si up to mm-wave frequencies, but also to demonstrate the ability to create CPW TLines that compete with corresponding state-of-the-art devices. CPW TLines with two different values of characteristic impedance, namely 50 Ω (CPW1) and 145 Ω (CPW2), were realized. More details about the fabricated CPW TLines and their corresponding de-embedding structures can be found in ref. [11].

The CPW TLines were measured from DC up to 110 GHz. The methods used for the extraction of the electrical parameters from the measured S-parameters are described in [9] and [11]. Fig. 4 shows the extracted values of the characteristic impedance of both CPW TLines (solid lines), versus frequency, as well as simulation results (symbols) carried out with a 3-D FEM tool based on HFSS software. Clearly, the simulation results are in excellent agreement with the measured ones. The length of the transmission lines was 2146μm. The resonance of both transmission lines appears at ~ 40 GHz. The extraction of the characteristic impedance beyond the first resonance frequency becomes inaccurate. Also, the ripples that appear beyond 65 GHz are attributed to the lack of precision and dynamic range of our measurement system in the 65-110 GHz band, and some inaccuracies in the de-embedding procedure.

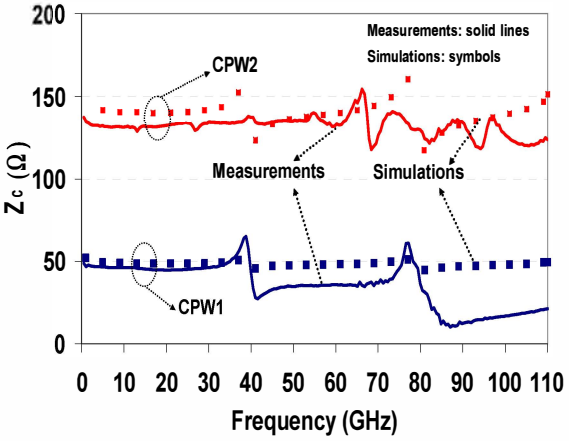

Fig. 4. Measured (solid lines) and simulated (symbols) characteristic impedance of the two CPW TLines versus frequency.

Fig. 5 shows the extracted (solid lines) and the simulated (symbols) effective relative permittivity of the two CPW TLines used in this work versus frequency, in the frequency range 0-110 GHz. Excellent agreement is obtained between simulated and measured values. The effective relative permittivity value is constant at 2.5 throughout the whole investigated frequency range. Fig. 6 shows the extracted (solid lines) and simulated (symbols) attenuation constant versus frequency for the two measured CPW TLines. Once again, measurement and simulation results show a very good agreement. The measured attenuation loss is as low as 0.32-0.35 dB/mm at 60 GHz and around 0.55 dB/mm at 110 GHz for both CPW TLines.

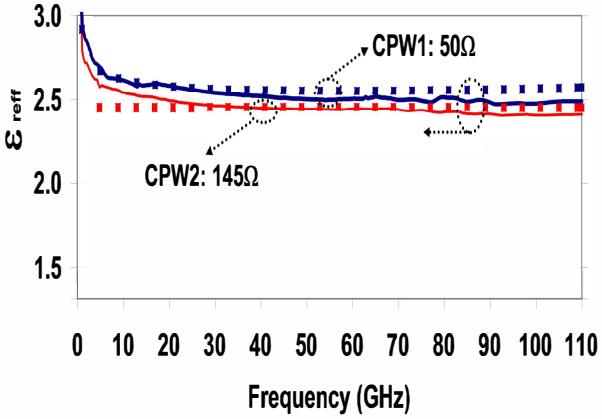

Fig. 5. Extracted (full lines) and simulated (dotted lines) of the $\varepsilon_{r\ effective}$ of the two CPW TLines versus frequency.

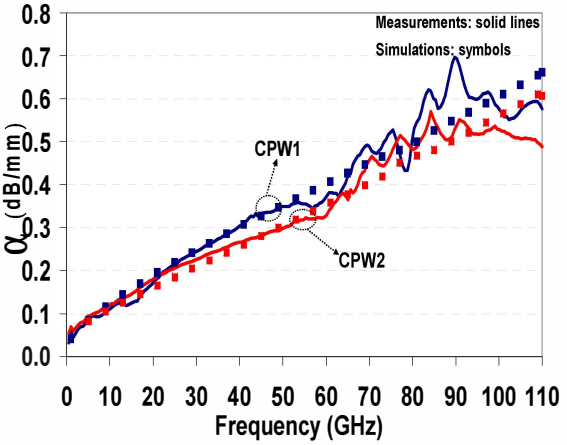

Fig. 6. Measured (symbols) and simulated (solid lines) attenuation loss of the two transmission lines investigated in this work versus frequency.

These values are very good compared with the present state-of-art of CMOS CPW TLines. Table 1 presents a comparison between the attenuation constant obtained for the CPW TLines in this work at 60 and 110GHz against 4 examples of CMOS state-of-the-art CPW TLines that can be found in the literature. In ref. [3] and [4] CPW TLs use thin SOI CMOS technology on high resistivity (HR) SOI substrate by SOITEC using 130nm SOI CMOS technology by ST Microelectronics. The metallization is Cu with use of metal layers M1-M6 and a total thickness of 5μm. The obtained attenuation is 0.6dB/mm at 60GHz and 1.3dB/mm at 110GHz in [4] and 1dB/mm at 110GHz in [3]. Both results are a factor of 2 higher than the attenuation of the CPW TLines of this work on porous Si, even though a simple one Al metallization layer of 1μm thickness was used in this work.

Device	Description	Attenuation (dB/mm)	Ref.
CPW	150um PoSi, 1um Al, p+ (0.001-0.005Ωcm)	0.33 @60GHz 0.6 @110GHz	This work
CPW	1kΩcm HR-SOI 130nm SOI CMOS using HR Unibond Substrate by SOITEC	1.0 @110GHz	[3] (2006)
CPW	Cu M1-M6 (~5um) 130nm HR-SOI (SOITEC) Advanced CMOS (>1kΩ.cm)	0.6 @60GHz 1.3 @110GHz	[4] (2007)
S-CPW	Al 2.34μm on M6 S-lines 500nm Al on ground metal CMOS 0.18μm	0.73@60GHz	[2] (2011)
S-CPW	Al 3um on M6, Shield Cu 500nm on M1, BiCMOS-9MW 130nm ST	0.7 @110GHz	[1] (2012)

Table1. Comparison between state-of-the-art attenuation values in the literature and in this work. In each case, the device type, the technology and the attenuation are given.

The other disadvantage of the above thin SOI CMOS technology on HR Si is the increased cost of the wafers, which move away from the standard bulk CMOS technology. The only available way to achieve low attenuation CPW TLines using standard bulk Si CMOS technology is to use alternative topologies as the slow-wave shielded CPW TLines (s_CPW TLines) [1, 2]. In references [1] and [2] the shielding lines are in M1 (500nm Al on M1 of 0.18μm CMOS in [2] and 500nm Cu on M1 of 130nm BiCMOS in [1]). The signal line is integrated in the last metallization step (2.34μm of Al in M6 in [2] and 3μm of Al in M6 in [1]). However, in spite of the complicated technology used, as it can be seen from table 1, both devices depict higher attenuation values than the CPW TLines on porous Si presented in this work. The attenuation at 60 GHz in reference [2] is more than twice the attenuation obtained in the present work. Moreover, the trend for standard CMOS processes is to reduce the thickness of the back-end metallization. So porous Si offers an additional advantage towards this trent. Clearly porous Si offers an exciting alternative since it produces excellent results, it is low cost and it is compatible with CMOS processing.

CONCLUSIONS

The RF-shielding properties of porous Si layers locally formed on the Si wafer were investigated. Identical CPW TLines were integrated on porous Si and on trap-rich HR Si and the characterization results were compared. The comparison showed that the CPW TLines integrated on porous Si had a 30% lower attenuation and a lower permittivity than the ones integrated on the trap-rich HR Si substrate. To further demonstrate the effectiveness of the shielding provided by the porous Si layers at mm-wave frequencies, CPW TLines were designed and realized on porous Si for use in the frequency range 1-110GHz. In particular, two different designs of 50 and 145 Ω characteristic impedance were realized. The measured attenuation loss was as low as 0.32-0.35 dB/mm at 60 GHz and 0.55 dB/mm at 110 GHz, for both CPW TLines. These results are comparable with the best results in the literature for CMOS RF CPW TLines using very advanced topologies or advanced substrates. In conclusion we have demonstrated that porous Si layers locally formed on the Si wafer provide an effective shielding from the lossy Si substrate for on-chip RF passive integration. Their superior performance is achieved in the whole frequency range from 1 GHz up to 110 GHz.

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