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Analysis and Design of RF Energy-Harvesting Systems with Impedance-Aware Rectifier Sizing

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***Abstract*—Because of the interaction between the internal blocks of an RF energy harvesting (RFEH) system, sizing a rectifier only for high power conversion efficiency (PCE) is insufficient for improving global power harvesting efficiency (PHE). This paper analyzes and sizes the rectifier by taking its input and output impedances into account with a two-port model that combines the rectifier AC and DC characteristics. The AC characteristic in this model is used for impedance-aware rectifier sizing. We target a low input-impedance rectifier for better impedance matching between the receiver antenna and the rectifier. The DC characteristic describes the rectifier power loss allocation and estimates its maximum power point. A proposed parasitic-aware matching network sizing methodology predicts the PHE is finally limited by Ohmic loss in the matching network at a low incident power level. For overcoming this limitation, this paper also analyzes the impact of multiple rectifier stages on RFEH with a high peak-to-average power ratio (high-PAPR) incident waveform for improving the PHE. We design an RFEH prototype with a sized 28nm CMOS two-stage cross-coupled rectifier. Measurement results show sensitivity as low as -28.3 dBm with a peak PHE of 31.1% at -16.5 dBm 2.45-GHz high-PAPR incident power. It has sufficient high output impedance to prevent reverse leakage without the need for an additional self-gating circuit.**

***Index Terms*—RF energy harvester (RFEH), power harvesting efficiency (PHE), maximum power point, impedance-aware, two-port rectifier model.**

I. Introduction

Radiative wireless power transfer (WPT) is an alternative solution for far-field power supply of ultra-low-power (ULP) Internet-of-Things (IoT) sensors. It is composed of an RF power generator as transmitter (TX) and an RF energy harvester (RFEH) as receiver (RX) [1]. Improving the power harvesting efficiency (PHE) of the RFEH is a key factor to increase the effective distance between TX and RX, which is the primary goal of the far-field WPT.

As depicted in Fig. 1, the RFEH includes four main blocks: receiving antenna, impedance matching network (MN), AC/DC rectifier and power management unit (PMU). Off-the-shelf PMUs for energy harvesting feature maximum power point tracking (MPPT) helps to improve the PHE by regulating the rectifier output voltage $V_{\text{out.rec}}$ to a given ratio γ_{MPPT} of its open circuit voltage $V_{\text{out.rec.OC}}$.

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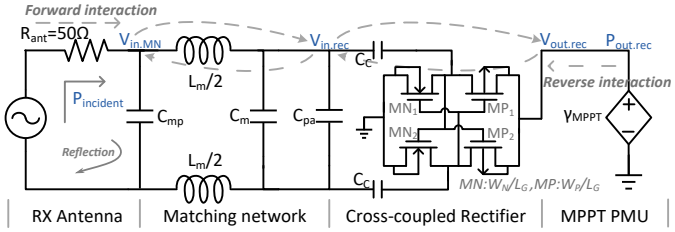

Fig. 1. RFEH architecture and its interaction between the internal block. PHE = $\text{PEE}_{\text{ant}} \times \text{PCE}_{\text{MN}} \times \text{PCE}_{\text{rec}}$, where PEE_{ant}, PCE_{MN} and PCE_{rec} are respectively the power extraction efficiency of the receiving antenna ($=P_{\text{in.MN}}/P_{\text{incident}}$), power conversion efficiency of the matching network ($=P_{\text{in.rec}}/P_{\text{in.MN}}$) and power conversion efficiency of the rectifier ($=P_{\text{out.rec}}/P_{\text{in.rec}}$). For avoiding AC voltage attenuation, the corner frequency of the high pass filter which is composed by C_{C} and rectifier should be far lower than the input RF power frequency [2].

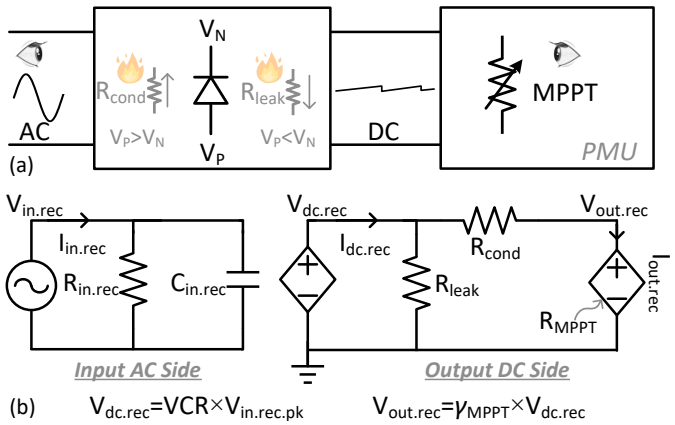

Fig. 2. (a) The architecture and perspectives of the rectifier with MPPT regulation. (b) The proposed two-port rectifier model and corresponding parameters expressions for impedance-aware rectifier sizing. In far-field RFEH application with low P_{incident}, the $R_{\text{in.rec}}$ is far larger than the antenna impedance.

There are interactions between these four blocks. Indeed, because the rectifier is a non-linear circuit, the voltages between the different blocks $V_{\text{in.MN}}$, $V_{\text{in.rec}}$ and $V_{\text{out.rec}}$ have forward (power transfer direction) impact on its corresponding downstream stage. MN input power $P_{\text{in.MN}}$, rectifier input power $P_{\text{in.rec}}$ and rectifier output power $P_{\text{out.rec}}$ increase at high incident power P_{incident}. The node voltages also have reverse impact in opposite direction to the power transfer on its upstream stage. Even with a fixed input P_{incident}, the $P_{\text{in.MN}}$, $P_{\text{in.rec}}$ and $P_{\text{out.rec}}$ vary with γ_{MPPT}. The interactions are mainly due to the fact that rectifier power conversion efficiency PCE_{rec} and input-impedance $Z_{\text{in.rec}}$ are function of both the rectifier input and output voltages. They further have impact on the receiving antenna return loss and matching network Ohmic loss [3]. Therefore, rectifier acts as a "bridge" of these

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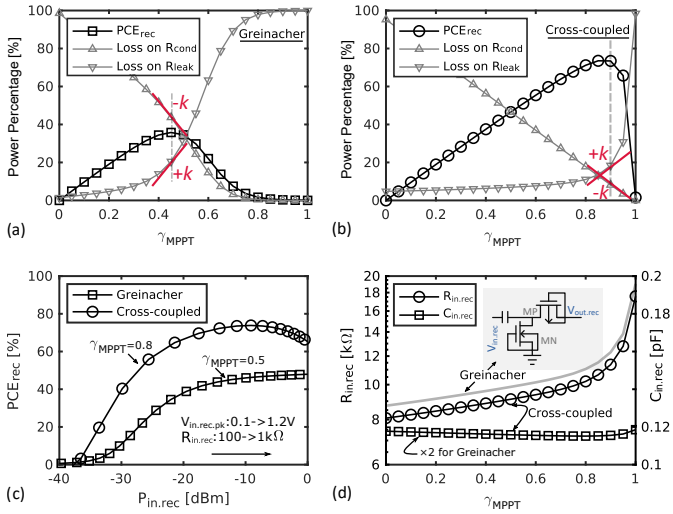

Fig. 3. PCE_{rec} and power loss on R_{cond}/R_{leak} depending on γ_{MPPT} for (a) a Greinacher rectifier and (b) a cross-coupled rectifier. (c) Comparison of PCE_{rec} depending on $P_{in.rec}$. (d) Rectifier input-impedance depending on γ_{MPPT}. (28nm FDSOI CMOS, LVT RF transistors, both rectifier types sized with L_G=30nm, W_N/L_G=17, W_P/L_N=2 and m_{rec}=40).

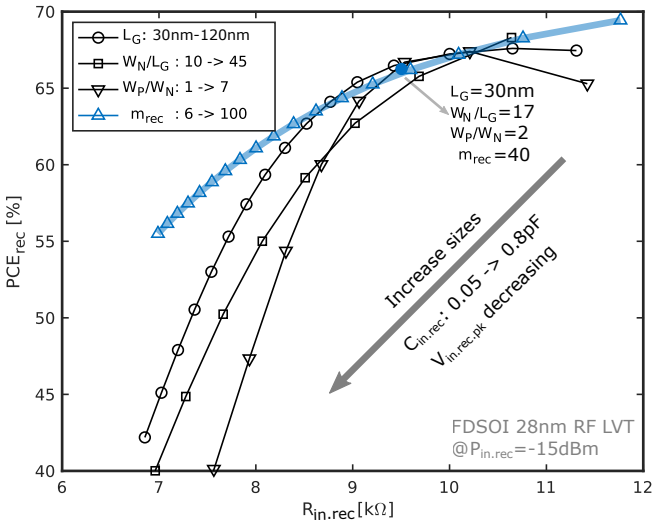

Fig. 4. Cross-coupled rectifier PCE_{rec} depending on $R_{in.rec}$ by sweeping its sizes, i.e. L_G, W_N/L_G, W_P/L_N and m_{rec}, with given amount of $P_{in.rec}$.

interactions. It needs impedance-aware analysis and sizing for taking its input AC and output DC characteristics into consideration to improve the global PHE of RFEH.

Instead of individual PCE optimization, in Section II, the rectifier is sized in an impedance-aware manner with a trade-off between PCE_{rec} and Z_{rec} by a two-port model. The matching network is parasitic-aware sized in Section III. The impacts of multiple number of rectifier stages in series on the RFEH with high peak-to-average power ratio (high-PAPR) waveform are discussed in Section IV with an RFEH prototype and corresponding measurement results.

II. Impedance-aware Rectifier Sizing

We propose to size the rectifier not only for high PCE_{rec}, but also for low $Z_{in.rec}$ with the two-port rectifier model in Fig. 2(a). A large $R_{in.rec}$ raises the MN design challenge and increases its Ohmic loss [3]. A large $C_{in.rec}$ narrows the

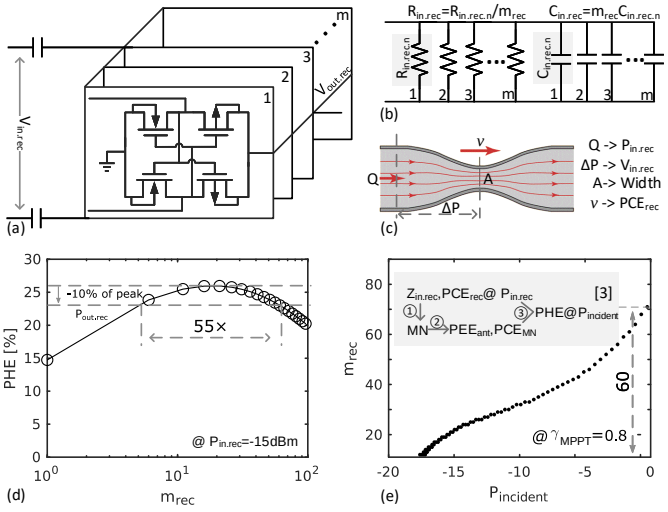

Fig. 5. Multiple rectifier in parallel (a) schematic, (b) impedance modeling and (c) its analogy to pipe fluid. Q is volumetric flow rate. Δ P is the pressure difference between the two ends. A is the cross section of pipe. v is the flow velocity. (d) The m_{rec} sizing for given $P_{in.rec}$. (e) Optimal m_{rec} for $P_{incident}$.

parasitic capacitance C_{pa} margin since C_{pa}=C_m-$C_{in.rec}$, where C_m is the required MN capacitance value in Fig. 1.

As depicted in Fig. 2(a), the discrete diode or the diode-connected MOS transistor in the rectifier has two main power loss sources: forward conduction loss $P_{loss.cond}$ and reverse leakage loss $P_{loss.leak}$. As illustrated in Fig. 2(b), from the input-side view, the rectifier has an AC equivalent impedance $Z_{in.rec}$ modeled by $R_{in.rec}$ in parallel with $C_{in.rec}$. From the output-side view, we can analyze its DC status with an voltage source $V_{dc.rec}$ controlled by the AC input voltage amplitude $V_{in.rec.pk}$. The $V_{dc.rec}$ value equals to the value of $V_{out.rec.OC}$ (=VCR×$V_{in.rec.pk}$), where VCR is the rectifier voltage conversion ratio between its output open-circuit voltage and its input AC voltage amplitude. For a single-stage cross-coupled rectifier used in Fig. 1, the rectifier VCR is around 0.85. The output power extracted by the MPPT PMU is modeled as a $V_{dc.rec}$ controlled voltage source. It has an equivalent resistance R_{MPPT}(=$V_{out.rec}/I_{out.rec}$). The power consumption on the R_{cond} and R_{leak} represent $P_{loss.cond}$ and $P_{loss.leak}$ respectively.

The link between the input-side AC model and the output-side DC model is power conservation. In other words, the power consumed on $R_{in.rec}$ is the sum of the power losses on R_{cond} and R_{leak} and the power extracted by MPPT PMU. It can be expressed as $P_{in.rec} = P_{loss.cond} + P_{loss.leak} + P_{out.rec}$, namely

$$\frac{V_{in.rec.pk}^2}{2R_{in.rec}} = \frac{V_{dc.rec}^2}{R_{leak}} + \frac{(V_{dc.rec} - V_{out.rec})^2}{R_{cond}} + \frac{V_{out.rec}^2}{R_{MPPT}}. \quad (1)$$

Simplifying Eq. (1) by applying Kirchhoff's circuit laws in Fig. 2(b), we have the $R_{in.rec}$ expression as

$$\frac{1}{R_{in.rec}} = 2VCR_{rec}^2\left[\frac{1}{R_{leak}} + \frac{(1-\gamma_{MPPT})^2}{R_{cond}} + \frac{\gamma_{MPPT}^2}{R_{MPPT}}\right]. \quad (2)$$

Normally, R_{leak} and R_{MPPT} are far larger than R_{cond}, thus $R_{in.rec}$ mainly depends on R_{cond}.

The rectifier is designed in 28nm FDSOI CMOS at 2.45GHz. As depicted in Fig. 3(a) and (b), at low γ_{MPPT}, the forward conduction losses dominate, i.e. $P_{loss.cond} > P_{loss.leak}$. On the other side, at a high γ_{MPPT}, the reverse leakage

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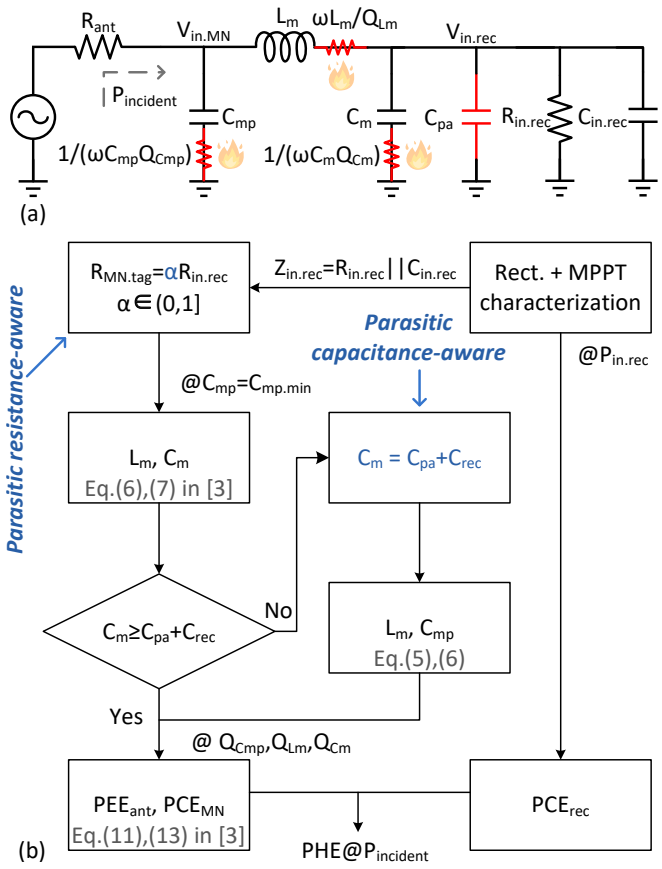

Fig. 6. (a) Parasitic-aware matching network first-order model. (b) Proposed parasitic-aware matching network sizing and power efficiency estimation methodology. Parasitic inductance, e.g., due to bonding wire, should be subtracted from L_m [3].

losses become dominant. The optimal rectifier output voltage $V_{\text{out.rec.opt}}$ for the highest PCE_{rec} is the one that meets the following conditions

$$\frac{\partial P_{\text{loss.cond}}}{\partial V_{\text{out.rec}}} = -\frac{\partial P_{\text{loss.leak}}}{\partial V_{\text{out.rec}}}. \tag{3}$$

Thanks to its dynamic self-V_{th}-compensation ability [4,5], the power loss on R_{leak} is suppressed in the cross-coupled rectifier compared to the Greinacher rectifier. So, the cross-coupled rectifier has a higher $\gamma_{\text{MPPT.opt}}$ ($= V_{\text{out.rec.opt}}/V_{\text{out.rec.OC}}$=0.8) than the Greinacher rectifier. As depicted in Fig. 3(c) and (d), the cross-coupled rectifier has higher PCE_{rec} and lower $R_{\text{in.rec}}$ compared to the Greinacher rectifier at the same input power $P_{\text{in.rec}}$ level.

As depicted in Fig. 3(c) and (d), γ_{MPPT} has a weaker influence on $R_{\text{in.rec}}$ than $V_{\text{in.rec}}$. It can be explained with Eq. (2), that R_{leak} and R_{cond} mainly depend on gate-source voltage V_{GS} which is bounded by $V_{\text{in.rec}}$. $V_{\text{out.rec}}$ has no prominent influence on $R_{\text{in.rec}}$ since it is at the drain node of PMOS $\text{MP}_{1/2}$. High γ_{MPPT} decreases the source-drain voltage V_{SD} of PMOS and increases R_{cond}. But as there is a (1-γ_{MPPT}) factor with power of two at the numerator in Eq. (2), $R_{\text{in.rec}}$ eventually increases slightly at high γ_{MPPT}.

$C_{\text{in.rec}}$ is dominated by the bias-independent access and fringing capacitances of the transistor. It is thus essentially proportional to the total transistor width and has less variation with both $V_{\text{in.rec}}$ and $V_{\text{out.rec}}$. At the same given rectifier

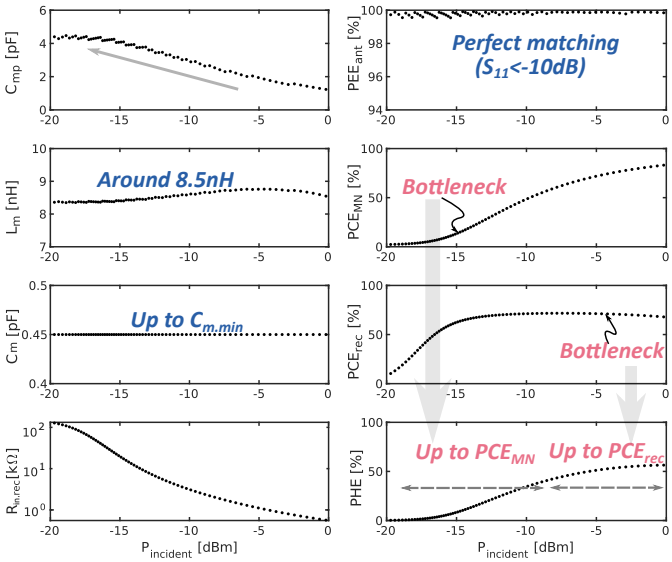

Fig. 7. The sizing results of the matching network and the power efficiency depending on P_{incident}.

input power $P_{\text{in.rec}}$, a lower $R_{\text{in.rec}}$ causes a lower $V_{\text{in.rec.pk}}$ ($= \sqrt{2P_{\text{in.rec}} \times R_{\text{in.rec}}}$). So, as depicted in Fig. 4, both PCE_{rec} and $R_{\text{in.rec}}$ decrease at large rectifier sizes with low $V_{\text{in.rec.pk}}$ at given amount of $\text{P}_{\text{in.rec}}$. Thanks to the fact that high V_{th} decreases reverse leakage, upsizing the gate length until 45nm does not degrade the PCE_{rec}. As depicted in Fig. 4, the curve of m_{rec} almost covers all the optimal PCE_{rec} points at the same $R_{\text{in.rec}}$ level. This means that rectifier sizing can be simplified into m_{rec} with fixed optimal L_{G}, $W_{\text{N}}/L_{\text{G}}$ and $W_{\text{P}}/W_{\text{N}}$.

The m_{rec} effect can be simplified into multiple rectifiers in parallel as illustrated in Fig. 5(a). Fig. 5(b) shows that $R_{\text{in.rec}}$ and $C_{\text{in.rec}}$ are m_{rec} repetitions of unitary $R_{\text{in.rec.n}}$ and $C_{\text{in.rec.n}}$ in parallel. It matches with the simulation results shown in Fig. 4. At given rectifier input power $P_{\text{in.rec}}$, the larger m_{rec}, the lower $V_{\text{in.rec.pk}}$, which degrades PCE_{rec}. It is similar to a pipe fluid as illustrated in Fig. 5(c). The pressure difference ΔP ($\Rightarrow V_{\text{in.rec}}$) decreases as the cross section of pipe A ($\Rightarrow m_{\text{rec}}$) increases with given amount of input fluid.

So, there is a tradeoff between PCE_{rec} and $Z_{\text{in.rec}}$ on the m_{rec} for PHE optimization. As depicted in Fig. 5(d), the optimal m_{rec} can be found by sweeping m_{rec} for maximizing PHE at given $P_{\text{in.rec}}$. The corresponding matching network sizes and P_{incident} can be calculated based on RFEH reverse global analysis methodology in [3]. As shown in Fig. 5(e), the optimal m_{rec} gradually decreases at low P_{incident} since less m_{rec} with high $R_{\text{in.rec}}$ boosts $V_{\text{in.rec.pk}}$ at given $P_{\text{in.rec}}$. However, as depicted in Fig. 5(d), m_{rec} has a 55× variation range for only a relative drop in the PHE from its peak value. Considering the difficulty of configuration switch and control for the adaptive m_{rec}, a fixed m_{rec} at average value (=40) is chosen for the RFEH design in this paper without apparent PHE drop.

III. Parasitic-Aware Matching Network Sizing

There are parasitic resistors in the lumped capacitor and inductor due to limited element quality factor (Q), as depicted in Fig. 6(a). It causes both Ohmic loss and impedance mismatch in the matching network. The parasitic capacitors from die

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pads, packaging and PCB impose a constraint on the minimum C_m value. We could increase C_{mp} to release the minimum C_m limitation. However, as discussed in [3], a larger C_{mp} causes a higher current amplitude in the matching network and degrades PCE_{MN}. So, as illustrated in Fig. 6(b), we propose a parasitic-aware matching network sizing methodology for maximizing PHE. To avoid iteration in forward RFEH analysis, it uses the reverse RFEH analysis and starts from the rectifier with MPPT PMU characterization by the proposed dual-end rectifier model. Instead of directly sizing the matching network from $R_{in.rec}$, the parasitic-aware sizing targets a resistance $R_{MN.tag}$ that is proportional to $R_{in.rec}$ by a factor α. If lumped elements have infinite quality factor Q, the factor α should be equal to 1. We gradually increase C_{mp} until C_m meets its minimum constraint $C_{m.min}$ (=$C_{in.rec}+C_{pa}$) or directly size C_{mp} from $C_{m.min}$ with the following equations (4) and (5). The virtual resistance R_{vir} used for the matching network sizing can be expressed as a function of $C_{m.min}$,

$$R_{vir} = \frac{R_{MN.tag}}{[\omega(C_{m.min}+C_{rec})]^2+1} \tag{4}$$

The C_{mp} and L_m are given by

$$C_{mp} = \frac{\sqrt{R_{ant}/R_{vir}-1}}{\omega R_{ant}} \tag{5}$$

$$L_m = (\sqrt{R_{ant}-R_{vir}}+\sqrt{R_{MN.tag}-R_{vir}})/\omega \tag{6}$$

The maximum PHE can be found by sweeping the parasitic-aware sizing factor α. The perfect matching or highest PEE_{ant} is obtained with optimal α in the range of (0 1]. The optimal parasitic-aware sizing factor α for maximizing PHE is mainly up to PEE_{ant}. A lower $P_{incident}$ with a higher $R_{in.rec}$ has a lower optimal α. As depicted in Fig. 7, with the proposed parasitic-aware sizing, we can achieve perfect matching even at low $P_{incident}$ which is a challenge for the matching network due to extremely high $R_{in.rec}$, e.g. $R_{in.rec}\approx$1MΩ @ $P_{incident}$=-20dBm. From 0dBm to -20dBm, the C_{mp} gradually increases to meet the $C_{m.min}$ constraint at large $R_{in.rec}$. As a result, the PCE_{MN} gradually decreases due to high AC current in the matching network. The L_m and C_m values are relatively stable. It is interesting in practice since we can reconfigurable the matching network just by tuning C_{mp}. As Buckets effect reveals, the capacity of a bucket depends on the shortest board. Finally, the PHE is limited by PCE_{MN} due to limited elements quality factors, especially at low $P_{incident}$. The high-PAPR waveform used in Section IV can help to improve the PHE at low $P_{incident}$.

IV. RFEH Prototype Design and Measurement

A large rectifier output voltage is good for improving the PCE of the MPPT PMU. In order to boost the rectifier output voltage, we can connect multiple rectifiers in series as shown in Fig. 8. The m_{rec} as shown in Fig. 5(a) can be uniformly distributed on each stage, i.e., each stage has the same number of fingers. From Kirchhoff's current law, we know that each stage has the same output current. Fig. 8(b) shows that the rectifier output voltage gradually increases with the number of rectifier stages. Its output current decreases and the product of

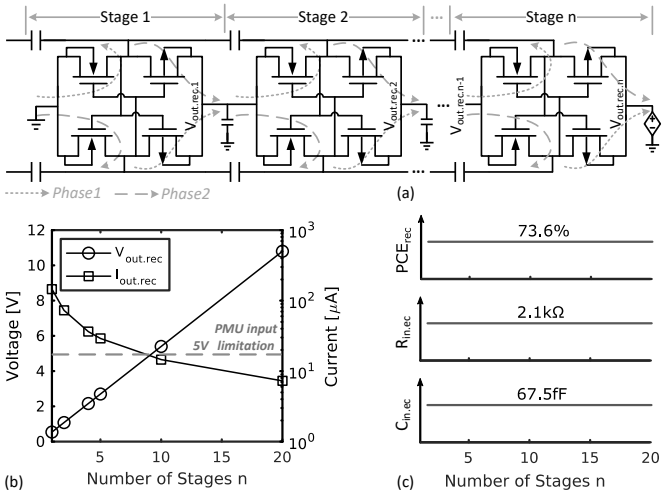

Fig. 8. (a) The schematic of multiple number of cross-coupled rectifier stages in series. Multi-stage rectifier characterization of (b) output voltage and current, and (c) PCE and $Z_{in.rec}$ at different number of stages with a fixed $P_{in.rec}$(=-15dBm) and optimal γ_{MPPT}(=0.8).

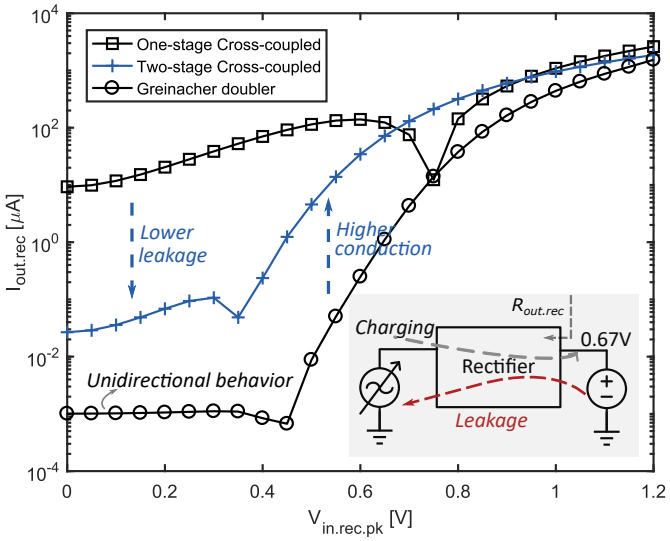

Fig. 9. Rectifier forward current and reverse leakage by sweeping its input voltage at a fixed output voltage. Greinacher doubler rectifier has a lower leakage thanks to its unidirectional behavior.

output voltage and current (i.e. $P_{out.rec}$) remains constant. From the AC input view of the rectifier, the input impedance does not change compared to the parallel rectifier structure. As a result, the number of stages has no impact on the rectifier PCE_{rec} and $Z_{in.rec}$ as illustrated in Fig.8(c). The matching network sizing results from a single-stage rectifier stage can be directly used for a multi-stage one. However, the rectifier output voltage is limited by the range of MPPT PMU input voltage (50mV-5V for the PMU we chose). Here, we choose a two-stage rectifier for our RFEH prototype design.

As depicted in Fig. 9, the two-stage cross-coupled rectifier has similar forward current compared to the single-stage rectifier. But, its reverse leakage is much less which is good for high-PAPR waveform for improving PHE at low incident power level. As depicted in Fig. 2, the rectifier output resistance $R_{out.rec}$ is approximated to R_{cond} and can be expressed as

$$R_{out.rec} \approx R_{cond} = 2VCR_{rec}^2(1-\gamma_{MPPT})^2 R_{in.rec}. \tag{7}$$

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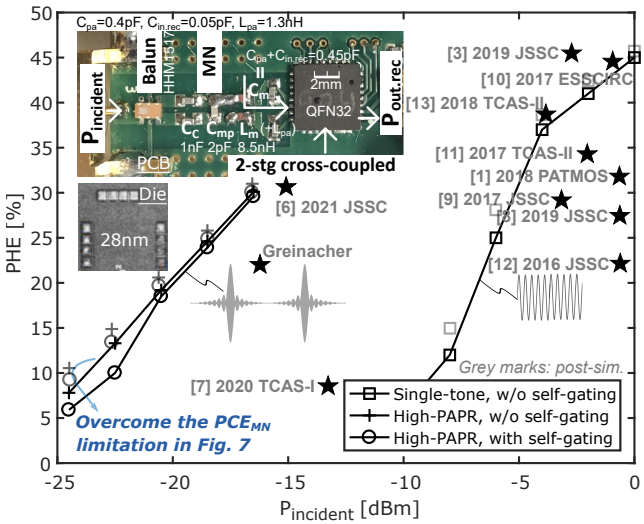

Fig. 10. RFEH prototype and measurement results at 2.45-GHz operational frequency, and peak PHE comparison with the state-of-art works. Except [6], the other works are with single-tone RF incident power. [1][3][6][12][13] work in 2.45-GHz band. [7]-[11] work in sub-GHz band.

The two-stage cross-coupled rectifier has 2× VCR compared to the single-stage. For reaching a given output voltage level, its $V_{\text{in.rec.pk}}$ is only half of the single-stage one. Let us notice here, the $R_{\text{in.rec}}$ exponential increases with low $V_{\text{in.rec.pk}}$ as transistors enter sub-threshold region. As a results, the two-stage rectifier has a much higher $R_{\text{out.rec}}$ to prevent reverse leakage. Although, the Greinacher doubler rectifier has the lowest reverse leakage thanks to its unidirectional behavior, its forward current is the lowest as depicted in Fig. 9.

The RFEH prototype is built with an off-chip Balun and MN. The two-stage cross-coupled rectifier is designed and fabricated in FDSOI 28nm CMOS based on the sizing results in Section II. It includes a self-gating circuit [6] which can be enabled (or disabled) by turning up (or down) its power supply. As depicted in Fig. 10, the RFEH with 2.45-GHz high-PAPR waveform can reach very good PHE at low P_{incident} even without self-gating compared to state-of-art works with zero-V_{th} rectifier [7], reconfigurable rectifier [8][9], MPPT [10], dual-path RFEH [11] co-design [12] and power recycling [13]. It reaches a sensitivity (positive output power criterion) of -28.3dBm and peak PHE of 31.1% at -16.5dBm.

V. Conclusion

There are interactions between the internal blocks of an RFEH. The AC/DC rectifier is the critical part of RFEH and acts as "bridge" of these interactions. For improving global PHE, we propose a two-port rectifier model to analyze both its input AC and output DC characteristics. In additional of improving the PCE_{rec}, impedance-aware rectifier sizing methodology also targets for a low $Z_{\text{in.rec}}$ which is friendly to parasitic-aware matching network. Multi-stage rectifier has high output impedance. It helps to prevent reverse leakage for intermittent input power and can improve PHE at low incident power level. We designed an RFEH prototype with a sized two-stage cross-coupled rectifier in FDSOI 28nm CMOS. Measurement results show a sensitivity of -28.3 dBm and peak PHE of 31.1% at -16.5 dBm with high-PAPR waveform.

References

[1] R. Dekimpe, P. Xu, M. Schramme, P. Gérard, D. Flandre, and D. Bol, "A Battery-Less BLE IoT Motion Detector Supplied by 2.45-GHz Wireless Power Transfer," in *International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*. IEEE, 2018, pp. 68–75.

[2] P.-A. Haddad, J.-P. Raskin, and D. Flandre, "Automated Design of a 13.56 MHz Corner-robust Efficient Differential Drive Rectifier for 10 μA Load," in *International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2016, pp. 1822–1825.

[3] P. Xu, D. Flandre, and D. Bol, "Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 10, pp. 2717–2729, 2019.

[4] S. M. Noghabaei, R. L. Radin, Y. Savaria, and M. Sawan, "A High-Efficiency Ultra-Low-Power CMOS Rectifier for RF Energy Harvesting Applications," in *IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–4.

[5] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency Differential-drive CMOS Rectifier for UHF RFIDs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, 2009.

[6] P. Xu, D. Flandre, and D. Bol, "A Self-Gating RF Energy Harvester for Wireless Power Transfer With High-PAPR Incident Waveform," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1816–1826, 2021.

[7] S. Schmickl, T. Faseth, and H. Pretl, "An RF Energy Harvester and IR-UWB Transmitter for Ultra-low-power Battery-less Biosensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 5, pp. 1459–1468, 2020.

[8] Z. Zeng, S. Shen, X. Zhong, X. Li, C.-Y. Tsui, A. Bermak, R. Murch, and E. Sánchez-Sinencio, "Design of Sub-gigahertz Reconfigurable RF Energy Harvester from-22 to 4 dBm with 99.8% Peak MPPT Power Efficiency," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2601–2613, 2019.

[9] M. A. Abouzied, K. Ravichandran, and E. Sánchez-Sinencio, "A Fully Integrated Reconfigurable Self-startup RF Energy-Harvesting System with Storage Capability," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 704–719, 2017.

[10] J. Wang, Y. Jiang, J. Dijkhuis, G. Dolmans, H. Gao, and P. Baltus, "A 900 MHz RF Energy Harvesting System in 40 nm CMOS Technology with Efficiency Peaking at 47% and Higher than 30% over a 22dB Wide Input Power Range," in *European Solid State Circuits Conference (ESSCIRC)*. IEEE, 2017, pp. 299–302.

[11] Y. Lu, H. Dai, M. Huang, M.-K. Law, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "A Wide Input Range Dual-path CMOS Rectifier for RF Energy Harvesting," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 2, pp. 166–170, 2017.

[12] J. Masuch, M. Delgado-Restituto, D. Milosevic, and P. Baltus, "Co-Integration of an RF Energy Harvester into a 2.4 GHz Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1565–1574, 2016.

[13] Y. Y. Xiao, Z.-X. Du, and X. Y. Zhang, "High-efficiency Rectifier with Wide Input Power Range based on Power Recycling," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 6, pp. 744–748, 2018.

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