CHAPTER 5

PASSIVE ELEMENTS ON SOI TECHNOLOGIES

5.1 Introduction

Passive elements are one of the major limiting factors to realize high performances and low power system-on-chip microwave circuits. It is then necessary to understand the mechanism affecting the performances of passive elements, and to optimize their structure in order to increase the circuit performances.

In the following section, a brief analysis of transmission line topology is presented. Then, we show a complete analysis of square spiral inductors made on SOI technology. A model of integrated inductor is given, and some design rules of integrated inductors are provided.

5.2 Properties of transmission lines

5.2.1 Introduction

Transmission lines are widely used in MMIC's as interconnects and matching networks. As explained in Chapter 2, they are also key elements in the required calibration procedure used to measure integrated components. There are various lines topologies that can be used in modern microelectronic. In the next paragraphs, a brief comparison of transmission line topologies is presented. The classical coplanar waveguide (CPW) is described. Its performance, in terms of attenuation coefficient, is compared for various under-laying substrates. Second, the performance of thin film microstrip (TFMS) and strip line, made on a state of the art technology using six metal layers is presented. The advantages, and drawbacks of both topologies are compared, and discussed.

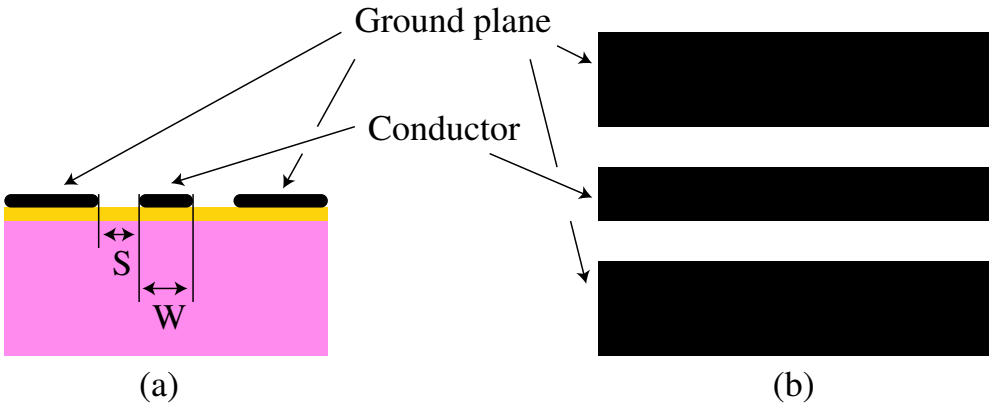


Figure 5.1: Top view (a) and cross section (b) of CPW

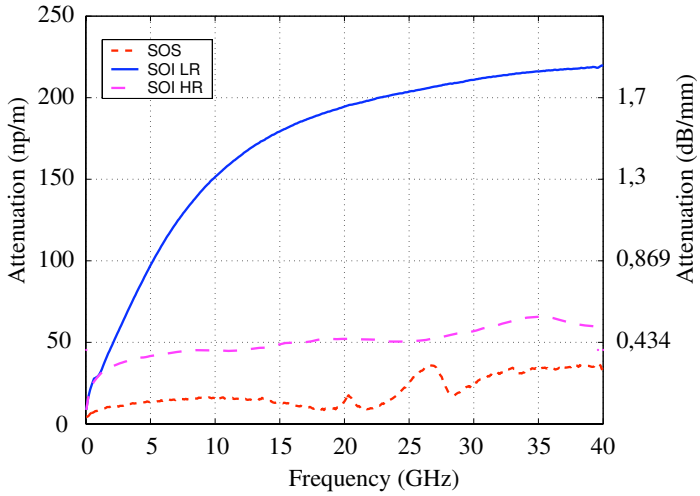


Figure 5.2: Attenuation coefficient of CPW lines ($W = 68\mu m$, $S = 38\mu m$)

5.2.2 *Coplanar waveguide (CPW)*

Coplanar waveguides are made of a central conductor, surrounded by two ground planes. It is usually laying between two mediums, the mechanical substrate, and air. Figure 5.1 shows a cross section and a top view of the CPW structure used in SOI technology. The characteristic impedance of CPW can be fixed on a wide range by changing the width of the central conductor (W), or the spacing between the central conductor and the ground planes. Coplanar waveguides have been used for several years in SOI technologies. Since RF measurements were made on that technology, CPWs were used for calibration purpose. Nowadays, as the

transistor operating frequency is increasing, transmission lines are now used for circuit design, such traveling wave amplifiers [1]. It is then necessary to have low loss CPWs.

The losses in CPWs are of two kinds:

- Conductor losses, due to the resistivity of the metal
- Substrate losses, due to the coupling between the line and the substrate

Figure 5.2 shows the attenuation coefficient of CPW lines made on standard SOI wafer, high resistivity SOI wafer, and SOS wafer. The width and the spacing of the CPW were $68\mu m$ and $18\mu m$ for each wafer. These dimensions allow us to obtain characteristic impedances close to 50Ω above 20 GHz. The CPW was fabricated using a $0.5\mu m$ thick aluminum layer, isolated from the substrate by an oxide layer ($\approx 3..4\mu m$).

By comparing, the attenuation coefficient (α) of the two lines made on SOI, the importance of the substrate losses is highlighted. The substrate losses dominate in the case of standard resistivity substrate.

The difference between the HR SOI and SOS is small, and is probably function of the conductor resistance.

5.2.3 Thin film microstrip line (TFMS)

TFMS are made of a conductor, laying above a ground plane. Figure 5.3 shows the cross section of the line. TFMS lines were realized on high resistivity and standard resistivity SOI wafers. Six metal layer were available on that process. The ground planes were composed of the two first metal layers, connected together by using vias. The conductor was made on the sixth metal layer using a $0.5\mu m$ thick aluminum. A $3.6\mu m$ thick Silicon dioxide layer separates the ground plane and the conductor. The dimensions of the lines have been determined by simulation to ensure characteristic impedance of 50Ω. The width of the conductor, is equal to $7\mu m$.

The lines are embedded between CPW to TFMS transitions. Their effects are cancelled by a TRL calibration. The attenuation coefficients of TFMS are

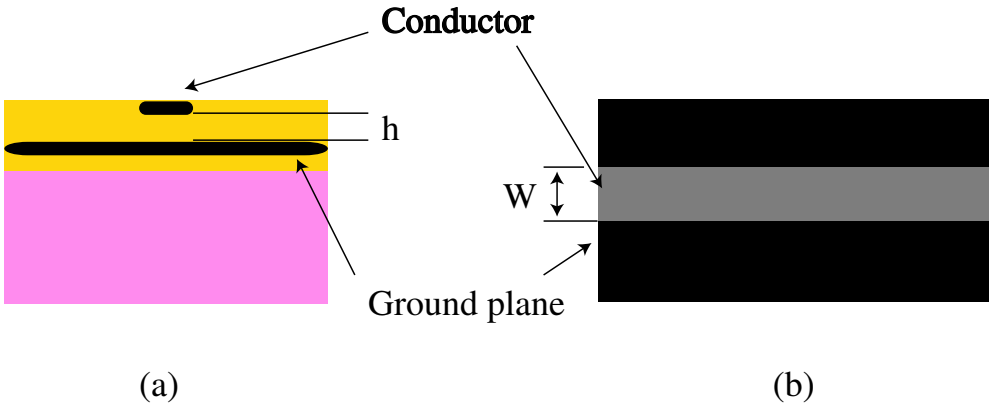


Figure 5.3: Top view (a) and cross section (b) of TFMS

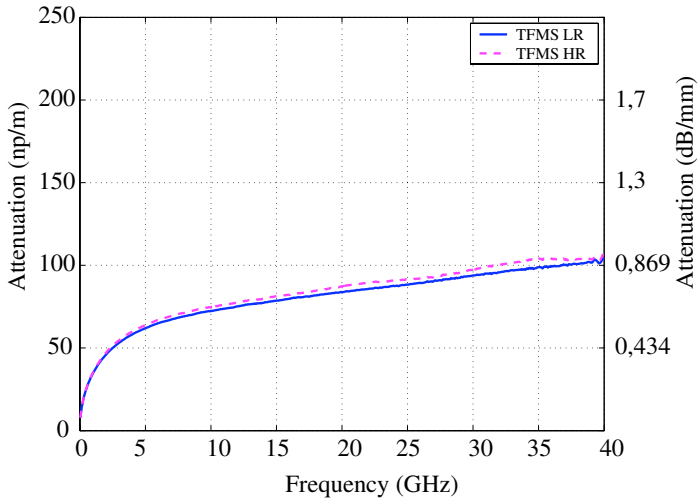


Figure 5.4: Attenuation coefficient of TFMS lines ($W = 7\mu m$, $h \approx 3.6\mu m$)

compared in Figure 5.4. No significant differences are observed between the two lines. In fact, the ground plane avoids coupling between the signal and the substrate. Thus, the properties of TFMS lines are independent of the substrate used, and the conductor losses are dominant.

5.2.4 Strip line

Strip lines are made of a conductor, embedded in a rectangular waveguide. Figure 5.5 shows the cross section of the line.

Strip lines were made on the same technology than the TFMS presented ear-

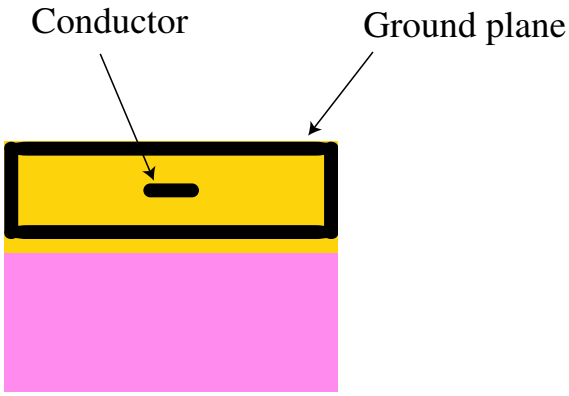


Figure 5.5: Cross section of a strip line

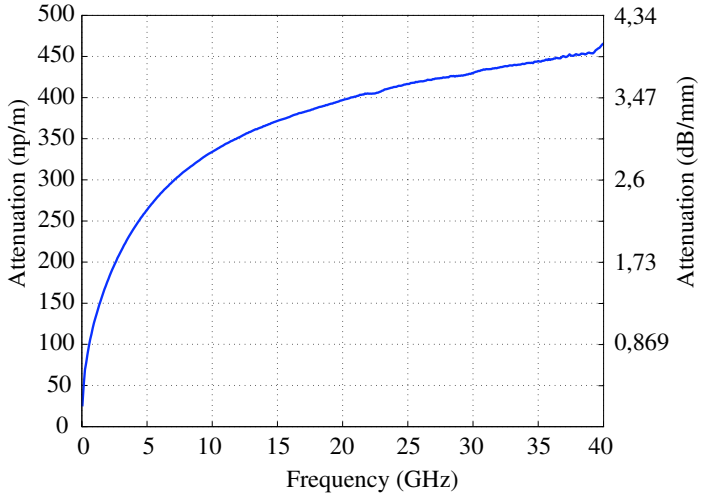


Figure 5.6: Attenuation coefficient of a strip lines ($W = 3\mu m$)

lier. To ensure a characteristic impedance close to 50Ω, the width of the conductor has been fixed to $3\mu m$. The strip line is embedded in CPW to Strip line transitions. Their effects are cancelled by the TRL calibration. Figure 5.6 shows the measured coefficient of a strip line. The huge conductor losses of these lines avoid their uses in circuits. Thus, we will not discuss further about that kind of lines.

5.2.5 Discussion

By comparing the results presented in Figure 5.2 and 5.4, CPWs made on HR SOI or SOS exhibits better performances than TFMS for impedances close to

50Ω. In both structure, the losses are dominated by the conductor losses. But TFMS lines are independent of the substrate used. Then good performances can be reached when TFMS are made on cheap, standard resistivity SOI substrate. TFMS can then be an interesting topology if the losses can be lowered to the same level than CPW made on HR SOI or SOS.

To reduce the attenuation coefficient of TFMS lines, the width and the thickness of the conductor must be increased, but the capacitance between the conductor and the ground plane must be kept constant ensuring the same characteristic impedance. To achieve this goal, the thickness of the dielectric layer must be increased, or low-k dielectric must be used instead of silicon dioxide.

These solutions are in agreement with the tendencies of semiconductor industries. Indeed, more and more metal levels are used, allowing a thicker isolator layer between the conductor, made with the top metal layer, and the ground plane. Furthermore, low-k dielectric will be used as insulator between the different metal layers to reduce the capacitive coupling between metal lines.

TFMS lines have been simulated using the IE3D software [2] for various substrate dimensions, in order to confirm these assumptions. The characteristic impedance of the line has been kept close to 50Ω by changing the conductor width. Figures 5.7-5.8 show the attenuation coefficient and the characteristic impedance for the simulated TFMS lines. The thickness of the oxide layers was equal to 3.5 and $5.5\mu m$ respectively. To ensure a characteristic impedance close to 50Ω, the width of the strip was set to $7\mu m$ for the line made on the thinner substrate and $11\mu m$ for the line made on the thicker.

A substrate thickness of $5.5\mu m$ allows us to obtain TFMS lines with nearly the same attenuation coefficient than CPW made on High resistivity silicon substrate. Such substrate thickness could be used shortly, when 8- or 9-metal level will be available in microelectronics.

Thus, the evolution of microelectronics allows us to consider TFMS lines as the most interesting topology for transmission line in the near future. It would allow us to design low loss transmission lines, in a homogenous medium, on cheap, standard resistivity silicon substrate.

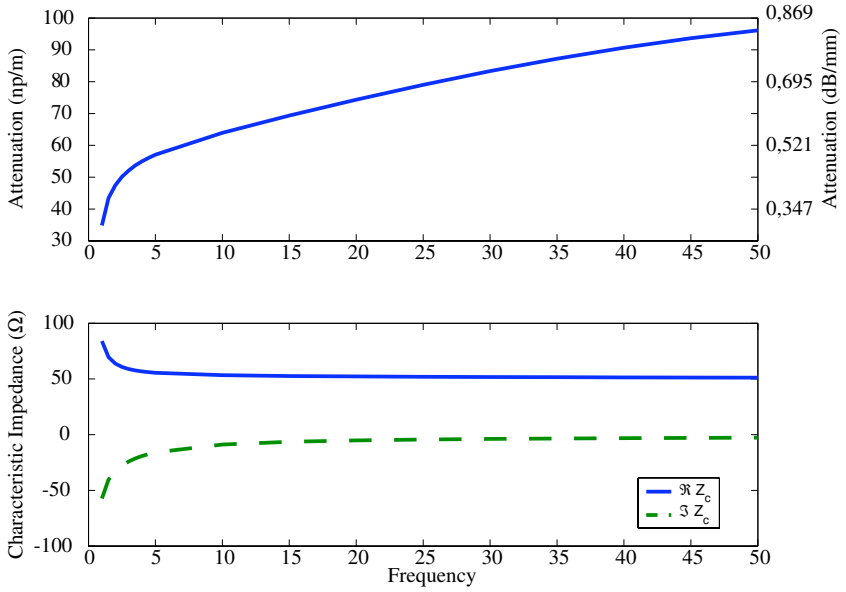


Figure 5.7: Attenuation coefficient (top) and characteristic impedance (bottom) of simulated TFMS ($W = 7\mu m$, $h = 3.5\mu m$)

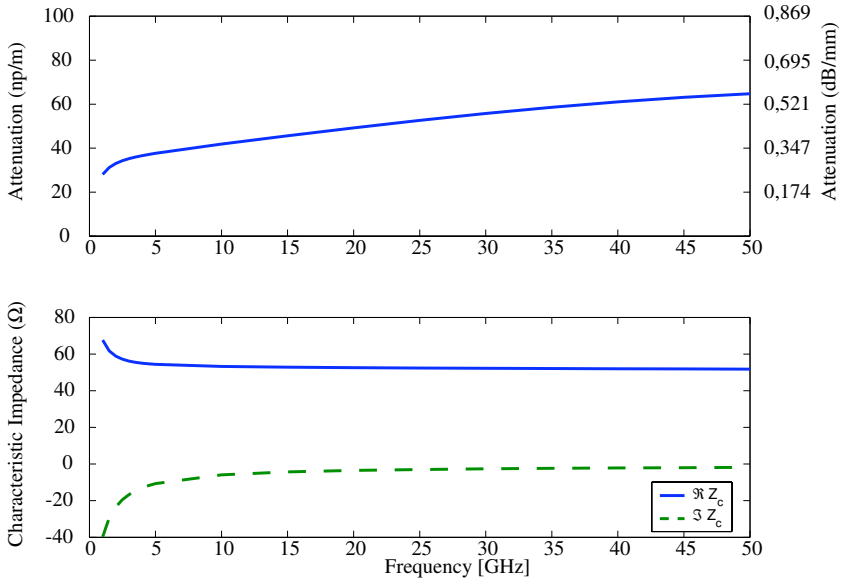


Figure 5.8: Attenuation coefficient (top) and characteristic impedance (bottom) of simulated TFMS ($W = 11\mu m$, $h = 5.5\mu m$)

5.3 Modeling of integrated inductors

5.3.1 Topology under scope

A lot of different topologies for integrated inductors exist in the literature. These topologies can be divided into two general groups of inductors: the meander inductors using only one metal layer and the spiral inductors using more than one layer. Only the spiral inductor will be discussed in this chapter. The spiral inductor consists of several aluminum strips connected together, drawing a spiral above a substrate. In SOI technology, the substrate is composed by a thick silicon layer ($\approx 500 \ldots 700 \mu m$), and a relatively thin layer of S_iO_2 ($\approx .4 \ldots 3 \mu m$) used to isolate the metal strips of the inductor from the silicon substrate. The outer end of the spiral is directly connected to a port, whereas the inner end of the spiral is connected to a port by using another metal level. This connection is referred to as the underpass. The whole structure is surrounded by a ground plane and connected to CPW pads. Figure 5.9 shows a top view and a cross section of the spiral inductor topology. This topology is commonly named square spiral when compared to octagonal or circular spirals. The characteristic geometrical parameters are the following

N : The number of turns.

W : The strip width.

W_p : The underpass width.

S : The spacing between lines.

$E\nu$: The vertical dimension of the hole in the middle of the spiral.

Eh : The horizontal dimension of the hole in the middle of the spiral.

t : The thickness of the silicon layer.

t_{ox} : The thickness of the oxide layer.

t_{uox} : The thickness of the oxide between the strip and the underpass

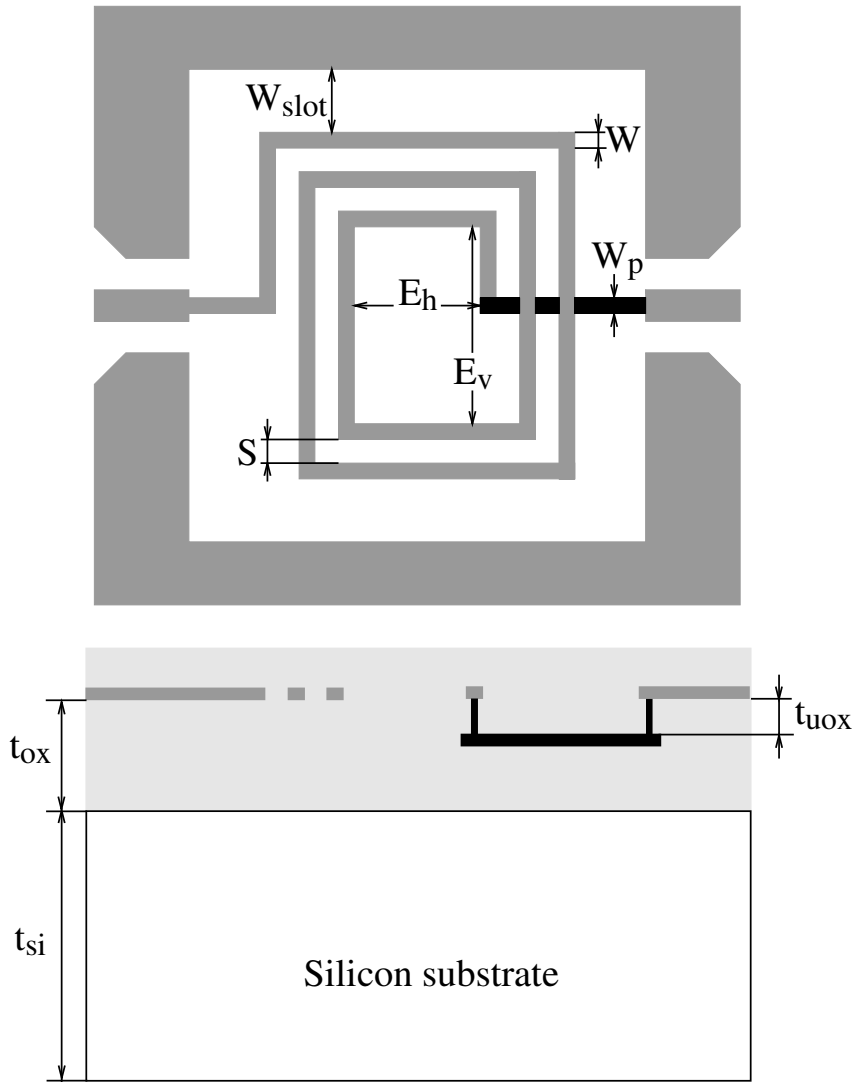


Figure 5.9: Top view and cross-section of the analyzed inductors.

5.3.2 Definitions

In order to compare simulations and measurements obtained in this work with some of the literature, some concepts, as the quality factor or the inductance of an inductor, must be defined. These concepts are commonly used in the literature, but, sometimes, based on different definitions. This results into some incoherences when results from different authors are compared.

Furthermore, a simple equivalent circuit of an integrated inductor will be introduced. This circuit can be directly deduced from measurements without any kind of fitting and is used to define the inductance and the resonant frequency of the inductor. Different definitions of the quality factors will be presented, one of them will be used further in this work.

5.3.2.1 Equivalent circuit

The equivalent circuit of the inductor is shown in Figure 5.10. The elements of this simple π equivalent circuit are straightforwardly obtained from the Y-parameters of a measured inductor as follows:

$$L_s = -\frac{\Im\left(\frac{1}{Y_{12}}\right)}{\omega} \tag{5.1}$$

$$R_s = \Re\left(\frac{1}{Y_{12}}\right) \tag{5.2}$$

$$R_{p_1} = \frac{1}{\Re\left(Y_{11}+Y_{12}\right)} \tag{5.3}$$

$$C_{p_1} = \frac{\Im\left(Y_{11}+Y_{12}\right)}{\omega} \tag{5.4}$$

$$R_{p_2} = \frac{1}{\Re\left(Y_{22}+Y_{21}\right)} \tag{5.5}$$

$$C_{p_2} = \frac{\Im\left(Y_{22}+Y_{21}\right)}{\omega} \tag{5.6}$$

Obviously, this is not a “physical" equivalent circuit, in the sense that all these components are variable versus frequency as shown in Figure 5.11. As it can be expected, the difference between C_{p_1} and C_{p_2} and between R_{p_1} and R_{p_2} being very small, these components will be referenced as C_p and R_p for both ports in the following sections. With this representation of the inductor, the

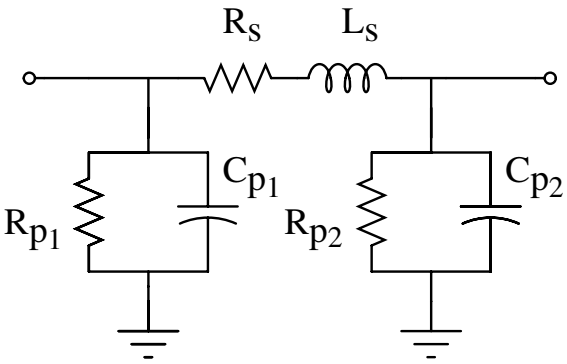


Figure 5.10: Simple π equivalent circuit of an integrated inductor.

effect of the substrate is separated from the effect of the strips [3]. Indeed, the R_p and C_p elements are directly related to the substrate characteristic. This is not the case of L_s and R_s in a first order analysis.

As it is shown in Figure 5.11a, L_s is nearly constant at low frequencies. Then, the inductance value will be defined as the value of L_s at low frequency, where it is constant. The resonant frequency is defined as the frequency at which L_s crosses the x-axis and becomes negative.

5.3.2.2 Quality factor

High performance on-chip inductors are needed for satisfying advanced demands in wireless communication circuits meaning a high quality factor and a high self-resonant frequency. There are various definitions of quality factor used in the literature, all of them giving different values for the maximum quality-factor, and making difficult the comparison between the models and measurements of the various authors. In the following paragraphs, five different definitions of quality factor, commonly used in the literature, are described. To explain the expression of the Q-factor, a physical equivalent circuit of the integrated inductor is introduced (Figure 5.12). The elements of this equivalent circuit are frequency independent. Some of them are related to the energy stored inside of the inductor.

Common definition This definition is the most widely used. It is based on the evaluation of the input impedance of an inductor having one port connected to

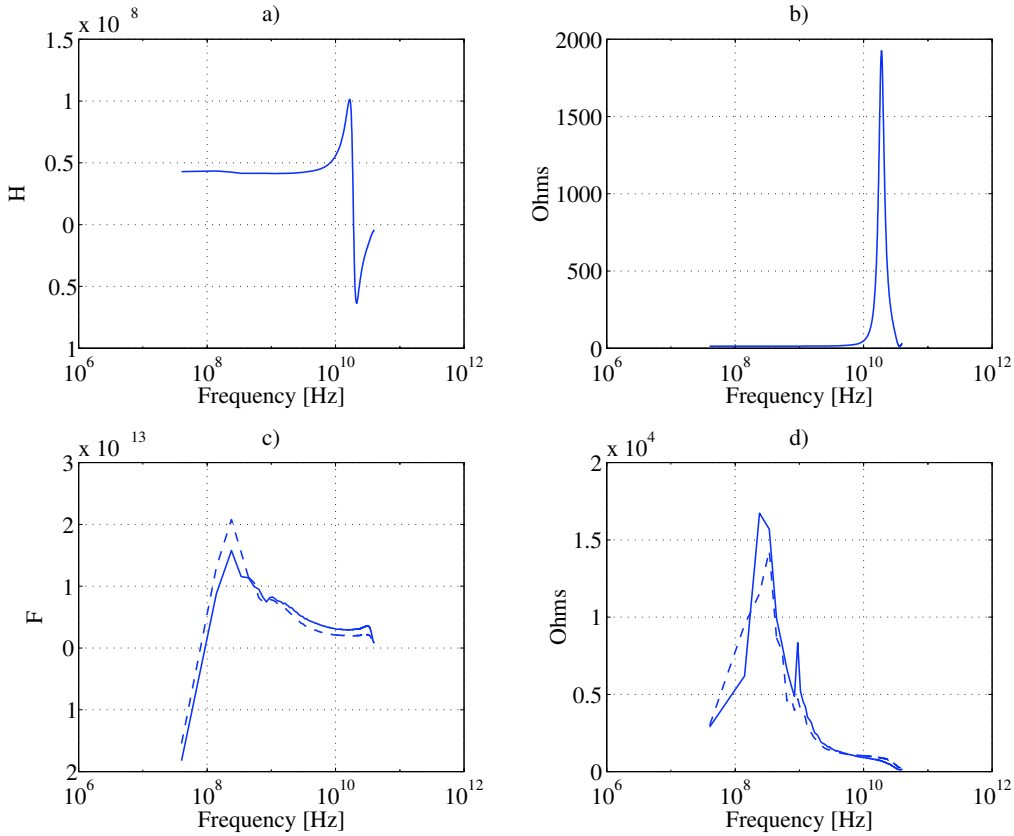


Figure 5.11: Extracted components from an integrated inductors with 5.5 turns, a strip width of $10\mu m$ and a spacing of $1\mu m$. (a) the inductance L_s, (b) the serial resistance R_s, (c) the substrate capacitance (— : C_{p_1}, - - : C_{p_2}) and (d) the substrate resistance (— : R_{p_1}, - - : R_{p_2})

the ground. The physical equivalent circuit proposed by YUE in [4] is used.

Figure 5.12 shows the equivalent circuit when the inductor is used as a 2-ports, when one port is connected to the ground and the energy equivalent model of the latter.

The theoretical definition of the quality factor of an inductive element is given by

$$Q = 2\pi \frac{Peak\ Magnetic\ Energy - Peak\ Electric\ Energy}{Energy\ loss\ in\ one\ oscillation\ cycle} \tag{5.7}$$

The energy equivalent model of the inductor (Figure 5.12c) is used to determine the values of the energy stored and lost in the inductor.

$$E_{E\,PEAK} = \frac{V_0^2 C_0}{2} \tag{5.8}$$

$$E_{M\,PEAK} = \frac{V_0^2 L_s}{2((\omega L_s)^2 + R_s^2)} \tag{5.9}$$

$$E_{LOSS} = \frac{2\pi}{\omega} \frac{V_0^2}{2} \left[\frac{1}{R_p} + \frac{R_s}{(\omega L_s)^2 + R_s^2}\right] \tag{5.10}$$

$$\text{where} \quad C_0 = C_p + C_s$$

$E_{E\,PEAK}$, $E_{M\,PEAK}$, and E_{LOSS} are the peak electric energy, the peak magnetic energy, and the energy losses respectively.

By combining these three equations, and after some basic manipulations, the quality factor can be rewritten as

$$Q = \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + [(\omega L_s / R_s)^2 + 1] R_s} \times \left(1 - \frac{R_s^2 C_0}{L_s} - \omega^2 L_s C_0\right) \tag{5.11}$$

where $\frac{\omega L_s}{R_s}$ accounts for the magnetic energy stored, the second term represents the losses in the silicon substrate, and the third term is called the self-resonance factor, which describes the reduction of Q when the frequency is close to the resonant frequency. At low frequency, the first term ($\frac{\omega L_s}{R_s}$) is dominant.

Equation (5.11) can be written in terms of Y-parameters as follows (Figure **??**c)

$$Q = -\frac{\Im\,(Y_{11})}{\Re\,(Y_{11})} \tag{5.12}$$

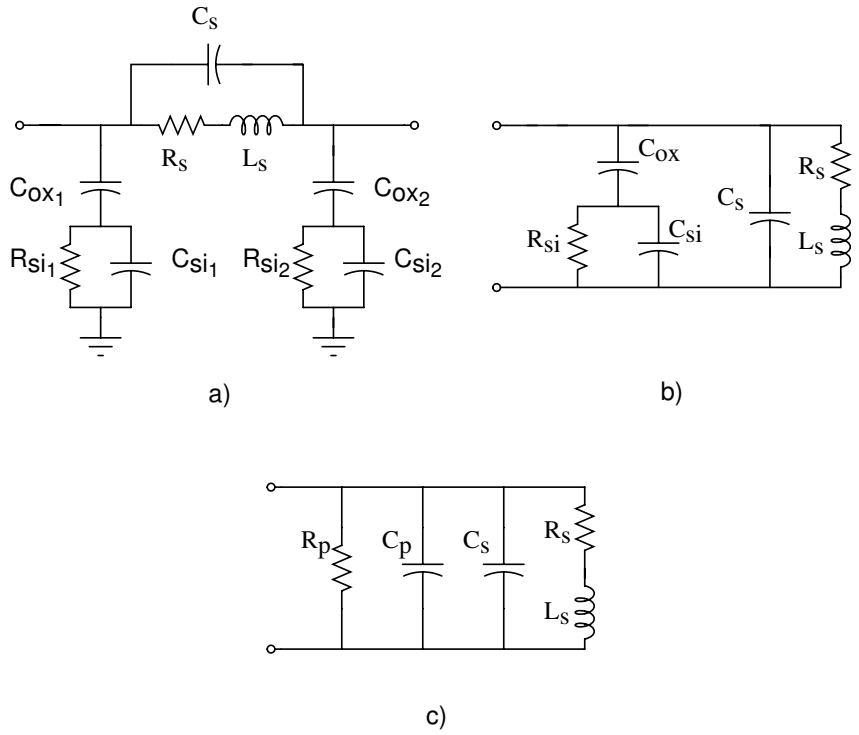


Figure 5.12: Simple equivalent circuit of an inductor (a), with one port connected to the ground (b) and its equivalent energy model (c).

First order definition. This definition is only valid at low frequencies, when the capacitive coupling to the substrate is negligible. The quality factor is then defined as:

$$Q = -\frac{\Im(1/Y_{12})}{\Re(1/Y_{12})} \tag{5.13}$$

Used by MAHMOUD in [5], this definition corresponds more or less to the first term of the previous one. It takes into account the conductor losses, which are dominant when the frequency is well below the resonance [4][6].

S-based definition. Several authors have developed theoretical expressions of the quality factor using S-parameters [7]. Most of them simply use the transposition of the definitions based on Y-parameters to S-parameters. In [8], the Q-factor is defined as a function of the S_{11} parameter. The load seen from the port 1 is deduced from S_{11}:

$$Z_{in} = Z_r \times \frac{1 + S_{11}}{1 - S_{11}} \tag{5.14}$$

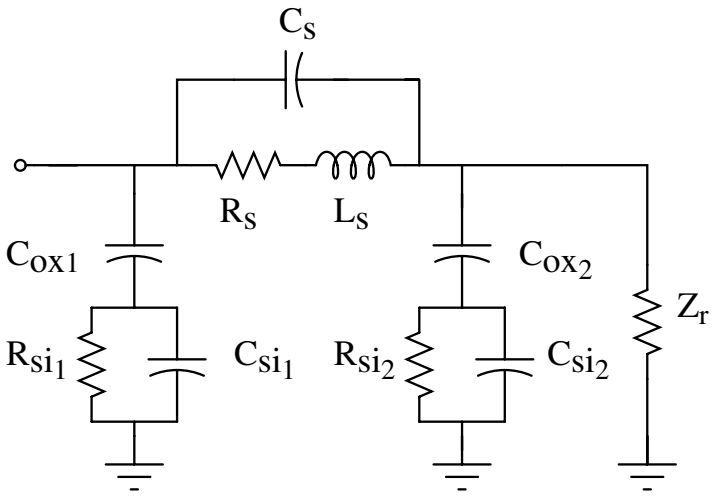


Figure 5.13: Equivalent circuit of an inductor used in the S-based definition of the Q-factor

The author assumes that the reference impedance (Z_r) is equal to 50Ω.

The Q-factor is then defined as:

$$Q = \frac{\Im(Z_{in})}{\Re(Z_{in})} \tag{5.15}$$

This definition looks similar to the common definition, but instead of connecting the port 2 to the ground, it is connected to the reference impedance (Z_r).

The equivalent circuit of the inductor equivalent circuit device used to evaluate the quality factor is given in Figure 5.13. At low frequency, when the effect of the substrate is insignificant, the value of the Q factor is nearly equal to $\omega Ls/(Rs + \Re(Z_r))$. This value can be more than one order of magnitude lower than the value obtained using the classical definition.

Phase definition. Recently, some authors introduced an original definition of the quality factor of an inductor [9][10]. This definition is based on the fact that integrated inductors are usually used in a LC tank. According to YUE [11], who highlights that the best definition of the quality factor must depend on the application, these authors propose to extend the Q-factor definition of a LC tank to an inductor.

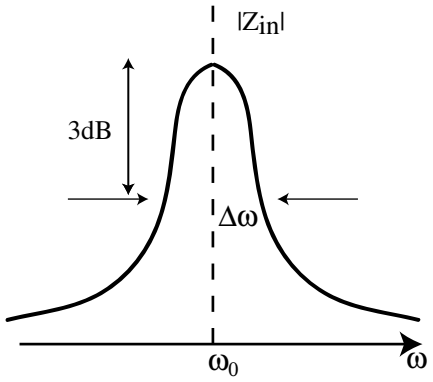


Figure 5.14: Magnitude of the input impedance of a LC tank used in the quality factor definition

The quality factor of a LC tank is defined by

$$Q = 2\pi \frac{\text{energy stored per cycle}}{\text{energy dissipated per cycle}} \tag{5.16}$$

The quality factor can be deduced from the frequency response of the tank. Figure 5.14 shows the impedance magnitude of a LC tank. Based on that measurement, the quality factor is obtained by using the following relation

$$Q = \frac{\omega_0}{\Delta\omega_{3dB}} \tag{5.17}$$

The quality factor can also be expressed by using the rate of change of phase when the device is resonating [12]

$$Q = \frac{\omega_0}{2} \frac{d\phi}{d\omega}\Big|_{\omega_0} \tag{5.18}$$

Equation (5.18) will be used to evaluate the inductor quality factor.

An ideal capacitor is inserted in parallel with the inductor for each ω_0 to cancel the imaginary part of the total input admittance. Then, the new admittance becomes

$$\begin{aligned} Y'(\omega) &= j\omega C + Y_{11} \\ C &= -\frac{\Im(Y_{11}(\omega_0))}{\omega_0} \end{aligned} \tag{5.19}$$

The admittance Y' resonates at the frequency of interest ω_0. By examining

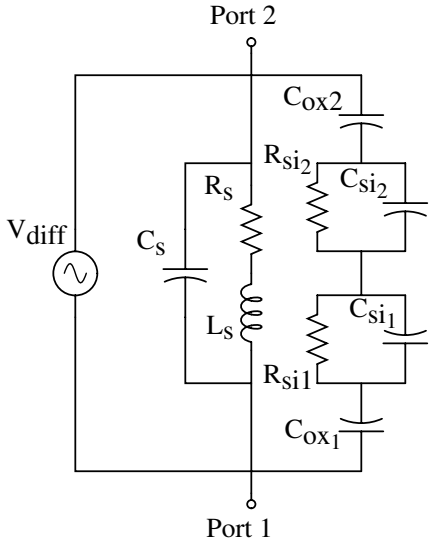


Figure 5.15: Equivalent circuit of an inductor used in the differential mode

the rate of change of phase, the Q factor can be deduced by using the following equation

$$\frac{d\phi}{d\omega}\Big|_{\omega_0} = \frac{2Q_{\angle}}{\omega_0} = \frac{\angle Y'(\omega_0 + \delta\omega) - \angle Y'(\omega_0 - \delta\omega)}{2\delta\omega} \tag{5.20}$$

Differential definition. The quality factor of an inductor can be evaluated when the inductor is excited in a differential mode [13]. This is the case in most of the oscillators topologies [14][15]. The inductor equivalent circuit used to evaluate the quality factor is slightly modified (Figure 5.15). The input impedance in differential mode is given by

$$Y_{in} = -Y_{12} + \frac{Y_{11} + Y_{12}}{2} \tag{5.21}$$

And the quality factor definition is defined by

$$Q = -\frac{\Im\,(Y_{in})}{\Re\,(Y_{in})} \tag{5.22}$$

Summary Various kinds of definitions of quality factors exist in the literature. Some of them have been presented in the previous paragraphs. For a given topology and substrate, these definitions give different values of the max-

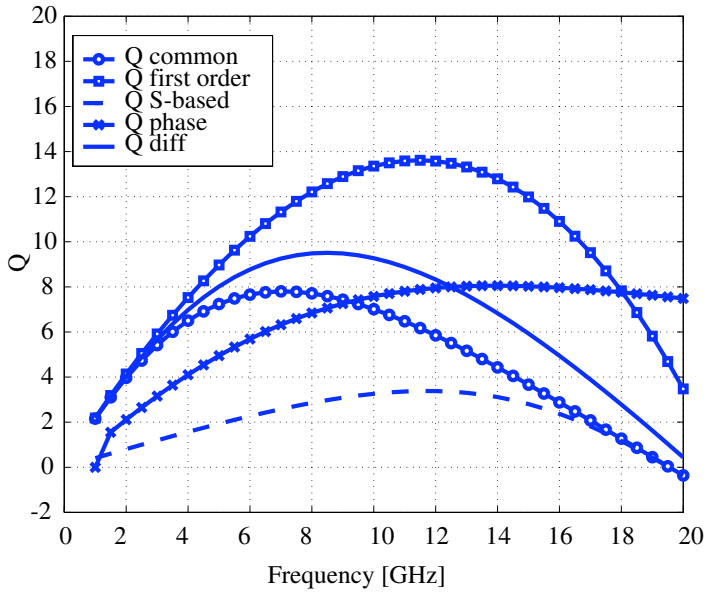


Figure 5.16: Comparison of the quality factors obtain by various definition for an inductor of 4.5 turns, a strip width of $10\mu m$ and a spacing of $1\mu m$.

imum quality factor, and the frequency where it occurs. Figure 5.16 shows a comparison of all quality factors defined in this section.

The comparison of publicized values must be done carefully as the difference between results obtained from different definitions can be really significant. In this work, the common definition has been chosen. It is the most used one, and it is not linked to any special application.

5.3.3 Modeling of square spiral inductors

5.3.3.1 Introduction

Computer Aided Design (CAD) for spiral inductors can be divided into two main categories: (1) the full-wave electromagnetic simulators (EMS) and (2) simple π-models for which the lumped element values are determined by semi-empirical equations or by fitting process on measured data. Hence, EMS are mainly used to generate pre-computed multi-dimensional databases, used for interpolations by the interactive CAD tool [16]. Their scalability is thus strongly limited. Many EMS's are also unable to take into account the frequency dependence of the bulk semiconductor substrate resistivity [17]. To overcome those drawbacks,

MMIC designers prefer to build a lumped element π-equivalent circuit for the spiral inductor as shown in Table (5.1). The values of the elements are mostly obtained by fitting S-parameters of the π-circuit to measured data [23][24][25]. As an advantage, the computation time is very reduced, since fitting is reported to be much faster than other numerical methods [26]. Users also argue that the π-model is easily inserted into commercial circuit-oriented simulators, and that some of the lumped elements have a physical interpretation [20]. Some of these lumped elements are described by analytical or semi-empirical formulas [19], while the others are determined by fitting using an EMS [27] or a CAD software [23][28]. MOHAN *et al.* present in [18] a very extensive work on simulations and measurements for extracting expressions of planar spiral inductances. They have derived several new simple and accurate expressions for the DC inductance of square, hexagonal, octagonal and circular inductors. The accuracy of these semi-empirical expressions has been evaluated by comparison with 3-D field solver predictions and by comparison with several measurements. The expressions predict inductance values for several geometry with an error of about 5% or less. These expressions are monomial equations containing geometrical variables (inner and outer dimensions of the spiral, strips width, and spacing between strips) and coefficients which are layout- and technology-dependent. These coefficients are obtained by various regressions or data-fitting techniques. Unfortunately, since these coefficients are optimized for a given technology, the impact of innovative solutions such as the use of pattern grounded shields, heavily doped *epi* substrate or high permeability magnetic layers, on the inductance cannot be easily established. A re-optimization of each coefficient is needed for each technology used. Moreover, Mohan *et al.* did not extract semi-empirical expressions for the other elements of the equivalent circuit (C_s, C_{ox}, C_{si} and R_{si}). Ronkainen *et al.* in [19] present semi-empirical expressions for the inductance L and resistance R (Table 5.1). The values of the other equivalent circuit elements (capacitances between strips and substrate parameters) are obtained by fitting techniques applied on a set of measured data. The disadvantage of this model is still the use of an optimization procedure to obtain the values of some model parameters. CROLS *et al.* define semi-empirical ex-

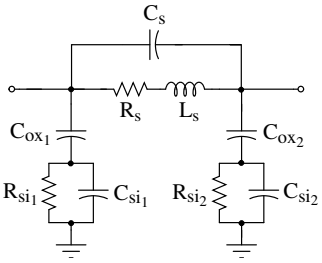
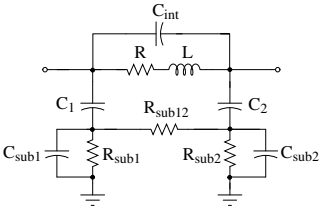
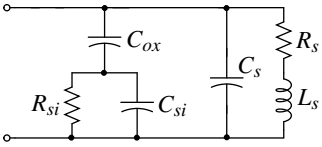
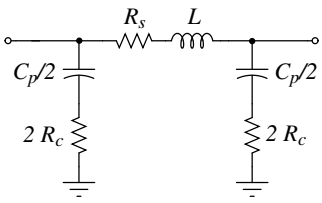
Author	Equivalent Circuit	Comments
Mohan *et al.* [18]		Simple and accurate empirical expressions for the DC inductance of square, hexagonal and circular spiral inductors. No expression is defined for the other equivalent lumped elements.
Ronkainen *et al.* [19]		R and L are obtained from semi-empirical expressions, the other elements by fitting.
Yue *et al.* [20]		All of the lumped elements are obtained from analytical expressions, except the inductance L_s which is calculated using the Greenhouse algorithm [21].
Crols *et al.* [22]		All the elements are obtained from semi-empirical expressions. The model validity is limited up to 3 GHz.

Table 5.1: Inductor models described in the literature.

pressions for the inductance and the resistance of the spiral inductor and also some for the substrate equivalent parameters [22]. Unfortunately, these expressions are technology-dependent and moreover only valid up to 3 GHz. In [20], LAU *et al.* present a physical model for spiral inductors on silicon. The series inductance L_s is computed using the Greenhouse algorithm [21], and analytical expressions depending on geometrical dimensions and material nature are defined for the other equivalent lumped elements. This model is scalable with the inductor geometry, allowing the designers to predict and optimize the quality factor. This model seems to be a very interesting candidate for the simulation of spiral inductors. However, as it will be shown later, it is not very accurate for modeling the substrate parameters.

All of these models suffer from various limitations: they are not valid above the resonant frequency (then not suitable for accurate simulations of non-linear circuits), they are generally scalable versus some parameters, not all of them, and they are only accurate for the technology, the type of substrate, the range of dimensions of the measured inductors and the measurements frequency range.

In order to overcome some of these limitations, an efficient design method has been developed by HUYNEN for MMIC's inductors [29]. It has the particularity to be directly related to the geometry of the spiral inductor and the electrical parameters of the substrate and, as a consequence, can be used with the same accuracy for various technologies and topologies. This model was developed for inductances with low line width to line spacing ratio (W/S). This preliminary model is extended and optimized in this section for large inductors with high quality factor.

This section is divided into five parts. First, the analysis of 3-coupled microstrip lines will be presented. Second the results obtained are extended for a structure composed by n-coupled microstrip lines. Then, based on this last method, the new model is presented and is compared with measurements and results obtained with other models. At the end, the advantages and the drawbacks of the model are summarized in a conclusion.

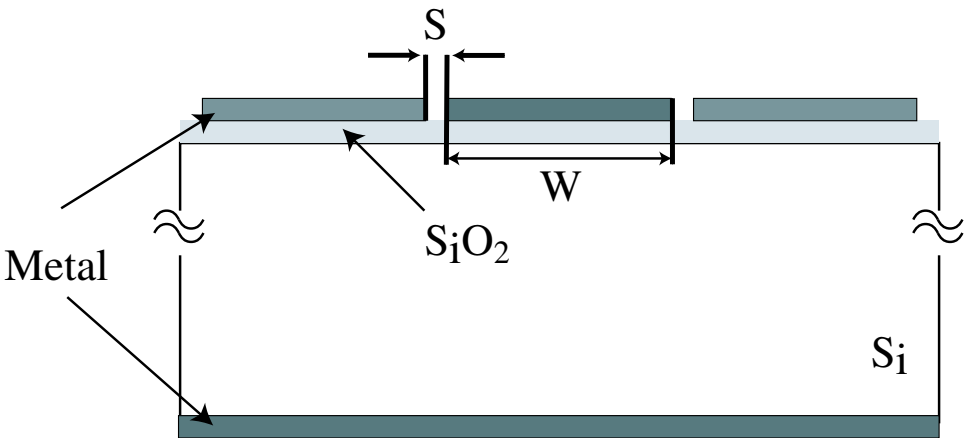


Figure 5.17: Cross section of three coupled microstrip lines. The Substrate is composed by a huge silicon layer ($\approx 750\mu m$), and a thin insulator layer ($2..3\mu m$ of SiO_2)

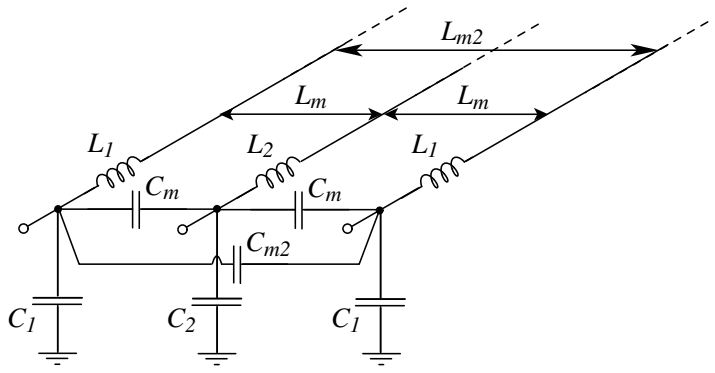


Figure 5.18: Equivalent circuit of an infinetezimal length (dz) of 3 coupled microstrip lines

5.3.3.2 Modeling 3-coupled lines on multilayered silicon substrate

In order to limit the complexity of the model and the computation time, the evaluation of the full coupling matrix of 3 lines, is done for three microstrip lines with a 10 μm width and separated by one micron. The lines are laying on a classical SOI substrate. The bottom of the wafer is made of a metallic ground plane. Figure 5.17 shows an schematic view of the structure.

Since the structure is symmetrical, the transmission line parameters (TLP) of the two outer microstrip lines will be the same as well as their coupling coefficient with the central line.

The general equivalent circuit of this line is shown in Figure 5.18. Based on this equivalent circuit, the differential equations describing the evolution of the voltage and the current along the lines can be written as follows

$$\begin{cases} \frac{\partial I_1(z,t)}{\partial z} = -C_1\frac{\partial V_1(z,t)}{\partial t} - C_m\frac{\partial (V_1(z,t)-V_2(z,t))}{\partial t} - C_{m2}\frac{\partial (V_1(z,t)-V_3(z,t))}{\partial t} \\ \frac{\partial I_2(z,t)}{\partial z} = -C_2\frac{\partial V_2(z,t)}{\partial t} - C_m\frac{\partial (V_2(z,t)-V_1(z,t))}{\partial t} - C_m\frac{\partial (V_2(z,t)-V_3(z,t))}{\partial t} \\ \frac{\partial I_3(z,t)}{\partial z} = -C_1\frac{\partial V_3(z,t)}{\partial t} - C_m\frac{\partial (V_3(z,t)-V_2(z,t))}{\partial t} - C_{m2}\frac{\partial (V_3(z,t)-V_1(z,t))}{\partial t} \\ \\ \frac{\partial V_1(z,t)}{\partial z} = -L_1\frac{\partial I_1(z,t)}{\partial t} - L_m\frac{\partial I_2(z,t)}{\partial t} - L_{m2}\frac{\partial I_3(z,t)}{\partial t} \\ \frac{\partial V_2(z,t)}{\partial z} = -L_2\frac{\partial I_2(z,t)}{\partial t} - L_m\frac{\partial I_1(z,t)}{\partial t} - L_m\frac{\partial I_3(z,t)}{\partial t} \\ \frac{\partial V_3(z,t)}{\partial z} = -L_1\frac{\partial I_3(z,t)}{\partial t} - L_m\frac{\partial I_2(z,t)}{\partial t} - L_{m2}\frac{\partial I_1(z,t)}{\partial t} \end{cases} \tag{5.23}$$

We can rewrite these equations in the spectral domain assuming that $V_i(z,t) = V_i(z) \times e^{j\omega t}$ and $I_i(z,t) = I_i(z) \times e^{j\omega t}$

$$\begin{cases} \frac{dI_1(z)}{dz} = -j\omega C_1 V_1(z) - j\omega C_m(V_1(z) - V_2(z)) - j\omega C_{m2}(V_1(z) - V_3(z)) \\ \frac{dI_2(z)}{dz} = -j\omega C_2 V_2(z) - j\omega C_m(V_2(z) - V_1(z)) - j\omega C_m(V_2(z) - V_3(z)) \\ \frac{dI_3(z)}{dz} = -j\omega C_1 V_3(z) - j\omega C_m(V_3(z) - V_2(z)) - j\omega C_{m2}(V_3(z) - V_1(z)) \\ \\ \frac{dV_1(z)}{dz} = -j\omega L_1 I_1(z) - j\omega L_m I_2(z) - j\omega L_{m2} I_3(z) \\ \frac{dV_2(z)}{dz} = -j\omega L_2 I_1(z) - j\omega L_m I_2(z) - j\omega L_m I_3(z) \\ \frac{dV_3(z)}{dz} = -j\omega L_1 I_3(z) - j\omega L_m I_2(z) - j\omega L_{m2} I_1(z) \end{cases} \tag{5.24}$$

the derivation of the last three equations versus z gives the following equation

system

$$\begin{cases} \frac{d^2V_1(z)}{dz^2} &= C_{1,1}V_1(z) + C_{1,2}V_2(z) + C_{1,3}V_3(z) \\ \frac{d^2V_2(z)}{dz^2} &= C_{2,1}V_1(z) + C_{2,2}V_2(z) + C_{2,1}V_3(z) \\ \frac{d^2V_3(z)}{dz^2} &= C_{1,3}V_1(z) + C_{1,2}V_2(z) + C_{1,1}V_3(z) \end{cases} \tag{5.25}$$

where the symmetry has been considered. The coefficients $C_{m,l}$ are given by

$$\begin{aligned} C_{1,1} &= \omega^2(-L_1C_m - L_1C_{m2} + L_mC_m + L_{m2}C_{m2} - L_1C_1) \\ C_{1,2} &= \omega^2(L_1C_m + L_{m2}C_m - L_mC_2 + 2L_mC_m) \\ C_{1,3} &= \omega^2(-L_{m2}C_{m2} + L_1C_{m2} + L_mC_m - L_{m2}C_1 - L_{m2}C_1 - L_{m2}C_m) \\ C_{2,1} &= \omega^2(L_2C_m - L_mC_m - L_mC_1) \\ C_{2,2} &= \omega^2(2L_mC_m - 2L_2C_m - L_2C_2) \end{aligned} \tag{5.26}$$

By assuming propagation along the z-axis ($V_i(z) = V_i \times e^{-j\beta z}$, $I_i(z) = I_i \times e^{-j\beta z}$), solving Equation (5.25) reduces to the evaluation of eigen values and eigen vectors [30] for voltage or for current

$$\begin{pmatrix} C_{1,1} & C_{1,2} & C_{1,3} \\ C_{2,1} & C_{2,2} & C_{2,1} \\ C_{1,3} & C_{1,2} & C_{1,1} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = -\beta^2 \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} \tag{5.27}$$

$$\begin{pmatrix} C_{1,1} & C_{1,2} & C_{1,3} \\ C_{2,1} & C_{2,2} & C_{2,1} \\ C_{1,3} & C_{1,2} & C_{1,1} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ I_3 \end{pmatrix} = -\beta^2 \begin{pmatrix} I_1 \\ I_2 \\ I_3 \end{pmatrix} \tag{5.28}$$

The three eigen vectors of equation (5.27) or (5.28), as well as their eigen values are evaluated by using the variational principle proposed by HUYNEN in [29] (Appendix (D)). The coefficient $C_{1,1}$, $C_{1,2}$, $C_{1,3}$, $C_{2,1}$ and $C_{2,2}$ are then extracted. The next step is the calculation of TLP by using Equations (5.26). This is however a system of 5 equations with 8 unknowns. Three other equations have to be added to find out all the parameters.The three equations are obtained by expressing the power associated with each propagation mode as function of the

Capacitance	Direct extraction	Silvaco
C_1	110	29.5
C_2	44.6	3
C_m	59.5	170
C_{m2}	-8	6

Table 5.2: Simulated and extracted capacitances in pf/m of 3 coupled lines with $W = 10\mu m$, $S = 1\mu m$, $t_{ox} = 4\mu m$, $t_{si} = 500\mu m$.

distributed elements of the lines. The power is defined by

$$P_i = \sum_{j=1}^{3} \frac{Z_{c_{i,j}} |I_{i,j}|^2}{2} \tag{5.29}$$

$$Z_{c_{i,j}} = \frac{V_{i,j}}{I_{i,j}} \tag{5.30}$$

where i and j correspond to the propagation mode and to the microstrip.

The three last equations are given by

$$\begin{cases} P_1 = \omega \frac{L_1 + L_{m2} + \left(\frac{C_{2,1}^2 L_2}{2}\right) + 2L_m C_{2,1}}{\beta_1} \\ P_2 = \omega \frac{L_1 + L_{m2} + \left(\frac{C_{2,2}^2 L_2}{2}\right) + 2L_m C_{2,2}}{\beta_2} \\ P_3 = \omega \frac{L_1 - L_{m2}}{\beta_3} \end{cases} \tag{5.31}$$

The value of the power associated with each propagation modes is computed by the variation principle.

The TLP's are finally extracted by using Equations (5.26) and (5.31). However, the extraction of all the lineic parameters are not straightforward, because they appear as products in Equation (5.26) and the possibility to recover them depends on their respective order of magnitude, which is directly related to the coupled lines geometry. To ensure a better extraction of the lineic parameters, it is suitable to perform some preliminary evaluation of the line parameters, and especially capacitances. Their values, given in Table (5.2), have been obtain by using a commercial 2-D simulator ATLAS from Silvaco [31] and extracted from our multi-line analysis, without precaution.

Due to the large distance h between the lines and the ground plane, only C_1 has to be taken into account. Actually, C_1 is significantly higher than C_2 due to

Capacitance	3-Lines	2-Lines	Inductance	3-Lines	2-Lines
C_1	29.5	35	L_1	1.16	1.2
C_2	3		L_2	1.4	
C_m	170	150	L_m	1.04	.98
C_{m2}	6		L_{m2}	0.76	.74

Table 5.3: Simulated inductances in $\mu H/m$ and capacitances in pf/m of 2 coupled lines with $W = 10\mu m$, $S = 1\mu m$ and $S = 12\mu m$, $t_{ox} = 4\mu m$, $t_si = 500\mu m$ and 3 coupled lines having the same dimension. The capacitances have been simulated using the Atlas simulator from Silvaco

the important fringing capacitance associated to outer strips. The high aspect ratio of the coupled lines (W/S=10) induces a high value for C_m, which is the dominant element, and a negligible value for the coupling capacitance between non-adjacent elements (C_{m2}). These conclusions are also valid for 4-coupled lines: only capacitances between the external lines and the ground plane and the capacitances between adjacent strips have to be considered. As a consequence, C_2 and C_{m2} are too small to be accurately extracted from (5.26) as shown in the column called "Direct extraction" in Table 5.2. The other coupling parameters (L_1, L_2, L_m, L_{m2}, C_1 and C_m) are then extracted from equations (5.26) and (5.31) by using the results of the multiline simulated with the variational principle. The extracted values of the TLPs are given in Table 5.2. In practice C_2 and C_{m2} will be fixed to zero. It is clear from the measurements that all the inductive couplings are in the same order of magnitude, even for the non-adjacent lines, and then none can be neglected. This has been checked by applying a sensitivity analysis to the model and has also been proved by Shepherd in [32].

This preliminary step is necessary in order to avoid trying to extract capacitances which are so small that the calculated S-parameters are completely insensitive to their value.

We compare the extracted values of inductances and capacitances with the values extracted from the computation of two coupled lines in Table (5.3). The values of the inductances are nearly the same and also the values of the capacitances C_1 and C_m. If the capacitance C_2 and C_{m2} are neglected, all the used TLP's can be deduced from the calculation of 2-coupled lines.

5.3.3.3 *Modeling of the admittance matrix of n-coupled lines*

This section presents the method used in our model to determine the admittance matrix associated with a group of n-coupled lines.

In accordance with the previous section, the capacitive coupling between non-adjacent lines is neglected, as well as the lineic capacitance of the lines, which are surrounded by others. The inductive coupling is considered between all the lines.

In this case, the equations describing the current and the voltage in the spectral domain are given by

$$\begin{pmatrix} \mathcal{Z} & -j\omega\mathcal{L} \\ j\omega C & \mathcal{Z} \end{pmatrix} \begin{pmatrix} \mathcal{V} \\ \mathcal{I} \end{pmatrix} = j\beta \begin{pmatrix} \mathcal{V} \\ \mathcal{I} \end{pmatrix} \tag{5.32}$$

where

$$\mathcal{V} = \begin{pmatrix} V_1 \\ \vdots \\ V_n \end{pmatrix} \quad \mathcal{I} = \begin{pmatrix} I_1 \\ \vdots \\ I_n \end{pmatrix} \quad \mathcal{Z} = \begin{pmatrix} 0 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & 0 \end{pmatrix}_{n\times n}$$

$$\mathcal{L} = \begin{pmatrix} L & L_{m12} & \cdots & L_{m1\,j} & \cdots & L_{m1\,n} \\ L_{m21} & L & L_{m23} & & & \vdots \\ \vdots & & & & & \vdots \\ \vdots & & & & & \vdots \\ L_{mn1} & L_{mn2} & \cdots & L_{mn\,j} & \cdots & L \end{pmatrix}$$

$$C = \begin{pmatrix} C + C_{m12} & -C_{m12} & 0 & \cdots & 0 \\ -C_{m21} & C_{m21} + C_{m23} & -C_{m23} & & \vdots \\ 0 & & & & 0 \\ \vdots & & & & -C_{mn-1\,n} \\ 0 & \cdots & \cdots & 0 \; -C_{mn\,n-1} & C + C_{mn\,n-1} \end{pmatrix}$$

The coefficient L, C, $L_{m_{ij}}$ and $C_{m_{ij}}$ are obtained from the calculation of 2-coupled lines, with a spacing equal to the distance between the i^{th} and the j^{th}

strip line.

The solutions of Equation (5.32) are the $2n$-propagation coefficients and the associated values of the voltage and current waves which are travelling through the n-lines (Eigen values and eigen vectors of the matrix).

The voltage and the current, at any point along the propagation direction, are a linear combination of the existing $2n$ modes. In order to obtain the admittance matrix of the group of lines, the coefficient of the linear combination must be calculated with the appropriate boundary conditions [16]. To achieve this goal, the scattering matrix of n-lines is calculated first. Then the scattering matrix will be transformed in an admittance matrix.

The power waves associated with each mode can be defined as follows

$$a_{i_m} = \frac{V_{i_m} + Z_c I_{i_m}}{\sqrt{\Re(Z_c)}} \qquad b_{i_m} = \frac{V_{i_m} - Z_c^* I_{i_m}}{\sqrt{\Re(Z_c)}} \tag{5.33}$$

The first index i specifies the access, and the second m specifies the propagation mode . These waves are calculated by using the solutions of Equation (5.32). Whatever the boundary conditions are, the global power waves are a linear combination of the a_{i_m} and b_{i_m} waves

$$\begin{pmatrix} a_1 \\ \vdots \\ a_{2n} \end{pmatrix} = \begin{pmatrix} a_{1_1} & \cdots & a_{1_n} \\ \vdots & \ddots & \vdots \\ a_{2n_1} & \cdots & a_{2n_1} \end{pmatrix} \begin{pmatrix} k_1 \\ \vdots \\ k_{2n} \end{pmatrix} \tag{5.34}$$

$$\begin{pmatrix} b_1 \\ \vdots \\ b_{2n} \end{pmatrix} = \begin{pmatrix} b_{1_1} & \cdots & b_{1_n} \\ \vdots & \ddots & \vdots \\ b_{2n_1} & \cdots & b_{2n_1} \end{pmatrix} \begin{pmatrix} k_1 \\ \vdots \\ k_{2n} \end{pmatrix} \tag{5.35}$$

where $k_1 \ldots k_{2n}$ are the coefficients determining the proportions of each mode at each access.

The scattering parameters of the n-coupled lines will now be calculated. The

definition of the S-parameters being

$$S_{ij} = \frac{b_i}{a_j}\Big|_{\forall\ j\neq i, a_j=0} \quad a_i = \frac{V_i + Z_c I_i}{\sqrt{\Re(Z_c)}} \quad b_i = \frac{V_i - Z_c^* I_i}{\sqrt{\Re(Z_c)}}$$

specific boundary conditions ($a_i = 1$ and $\forall\ j \neq i\ a_j = 0$) are imposed successively for each access. Solving for each cases Equation (5.34) yields to the determination of the k_i coefficients. By injecting this result into Equation (5.35) gives the value of the "b" waves corresponding to the imposed boundary condition. Thus, the coefficients of the i^{th} column of the scattering matrix is obtained.

In the present case, this procedure must be done only n-times. Transmission lines being reciprocal devices, the scattering matrix of the n-coupled lines must be symmetrical.

At the end, the admittance matrix of the n-coupled lines are calculated from the scattering matrix by using the relationship presented in Chapter 2.

5.3.3.4 Modeling of the inductor

The model described in this section is a transmission line model. For solving the multiline analysis, the square spiral is first divided into sections of n-coupled lines, "n" varying with the position in the spiral (Figure 5.19). Each strip in the section is supposed to be influenced by all parallel strips, including those located at the opposite side of the middle hole of the spiral. As a result of the study of 3-coupled lines (section 5.3.3.2), the inductive coupling between all the strips and capacitive coupling between adjacent strip must be taken into account. The lineic capacitance of the lines surrounded by two other are neglected, and set to zero. The coupling effects are evaluated with the variational principle as explained in the previous section. The effect of the underpass is taken into account by considering a section of coupled microstrip lines: the underpass is considered as the ground plane and the length of the microstrip section corresponds to the width of the underpass. Parasitic resistances corresponding to the conductors and the underpass are also added to the model, using Equation 5.36. This equation describes the resistances of a rectangular

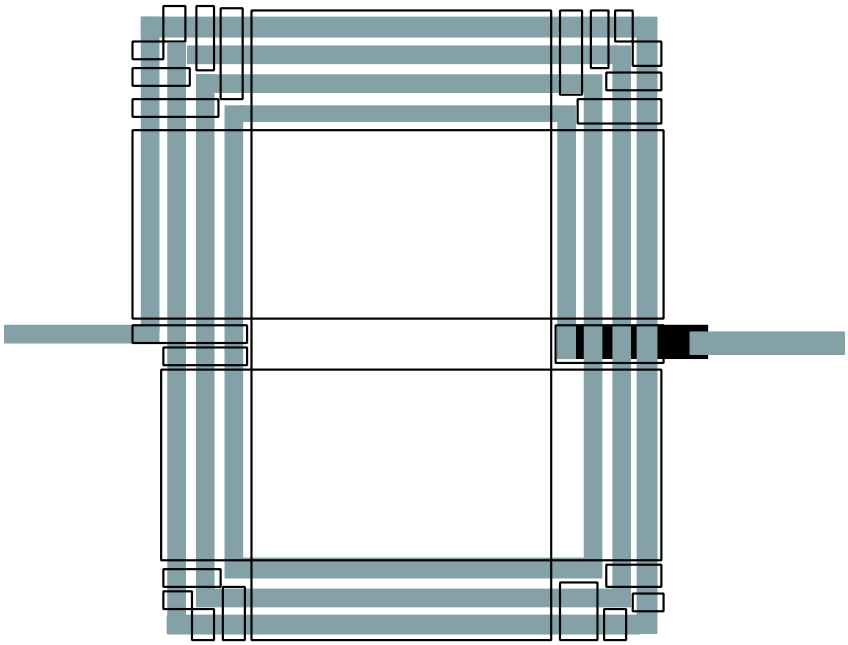


Figure 5.19: Division of the spiral inductor into sections of coupled microstrip lines.

conductor versus frequency [20].

$$R = \frac{\rho l}{W\delta\left(1 - e^{-t/\delta}\right)} \tag{5.36}$$

where $\delta = \sqrt{\frac{2\rho}{\omega\mu}}$ is the skin depth, ρ, W, t are the resistivity of the conductor, the strip width and its thickness respectively.

The Y-matrices of all sections are calculated using the method described previously. Then, these matrices are connected together to form the inductor (Figure 5.20). The global solution is obtained using sparse matrix technique [33] applied to floating admittance matrices [34].

Figure 5.21 shows schematically the simulation procedure from the geometrical and electrical characteristics of a given spiral inductor (inputs) to the inductor S-parameters or lumped RLGC equivalent circuit (ouputs) computed by the new simulator. These outputs can then be used by a microwave circuit designer to optimize the RF integrated circuit performance.

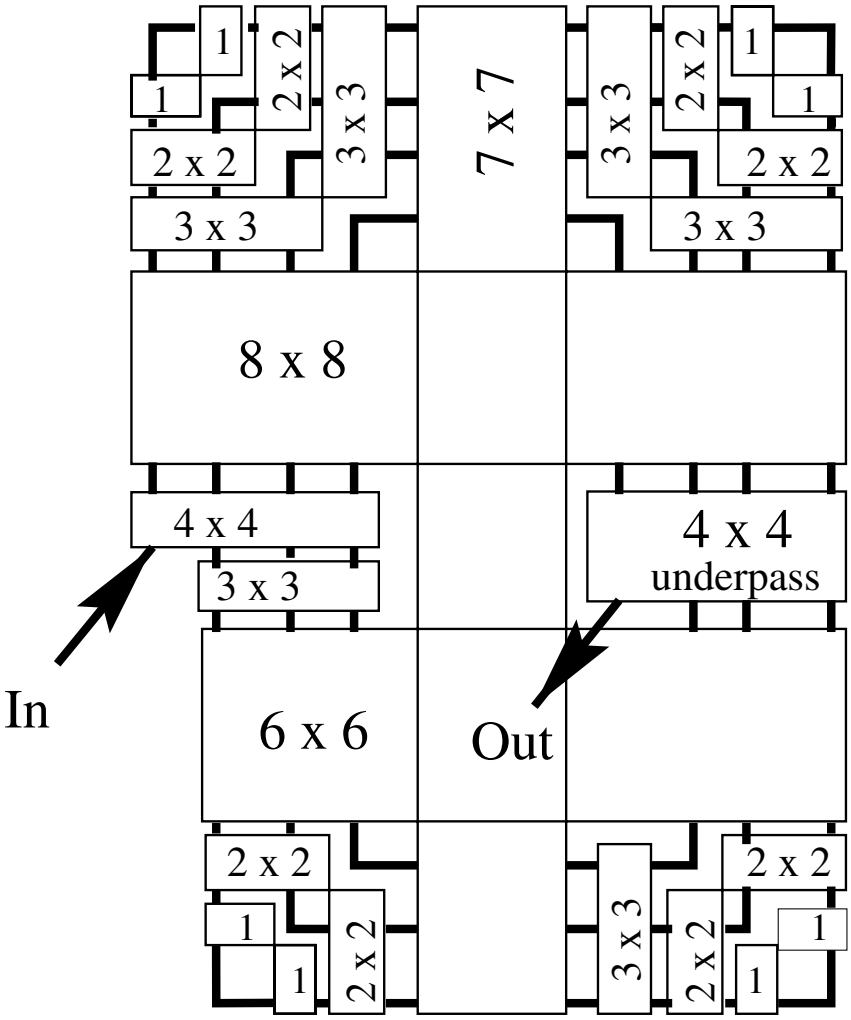


Figure 5.20: Connection of the admittance matrices for all coupled line sections.

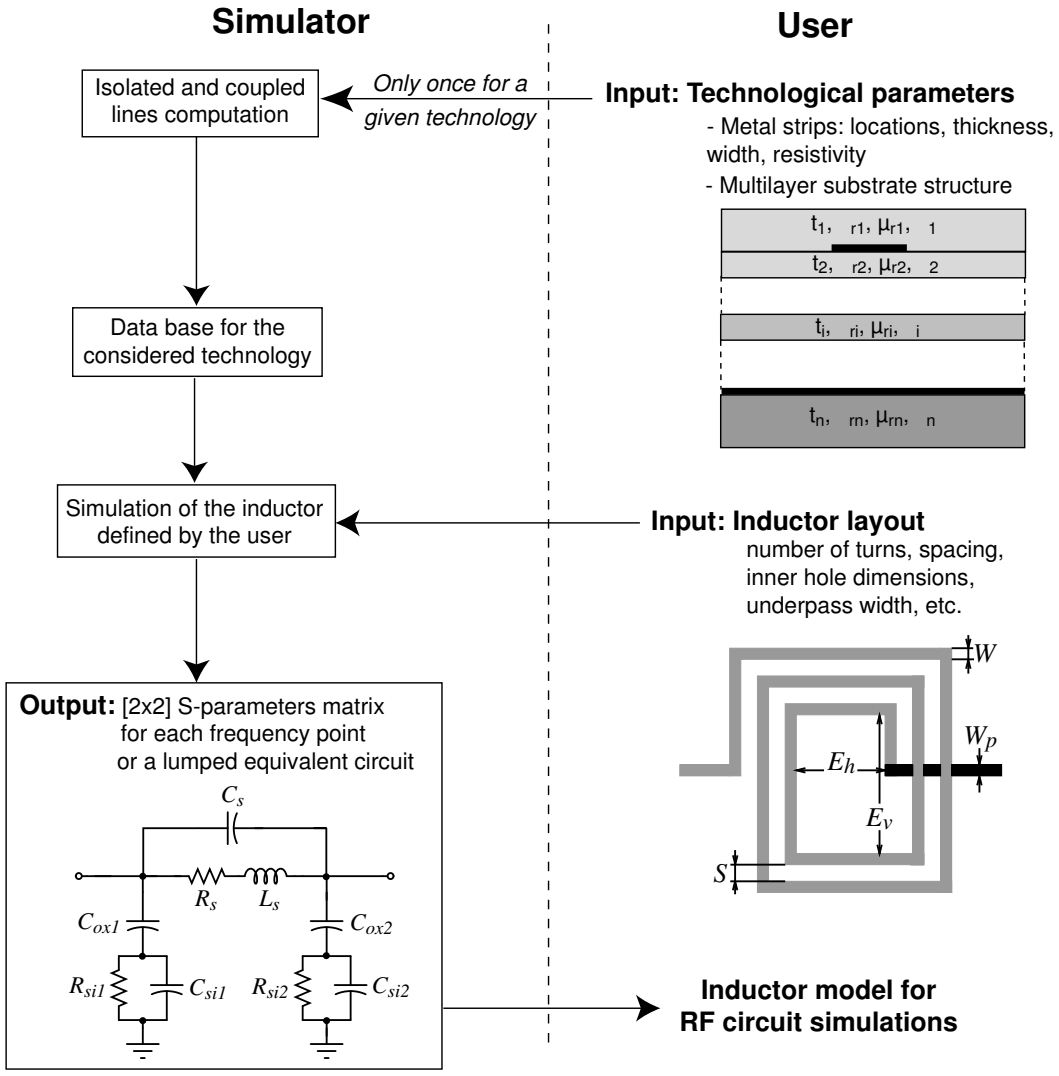


Figure 5.21: Simulation procedure: from the technological inputs and inductor layout to the high frequency simulated characteristics of the inductor.

Label	n	W (μm)	S (μm)	W_p (μm)	E_h (μm)	E_v (μm)	$Length$ (μm)
35T	3.5	10	1	5	50	50	1266
45TS5	4.5	10	5	5	50	50	2098
45TEH10	4.5	10	1	5	10	90	1826
45TEH30	4.5	10	1	5	30	70	1826
55T	5.5	10	1	5	50	50	2472
85T	8.5	10	1	5	50	50	4942
35TCsT	3.5	10	1	5	289	289	4612
45TCsT	4.5	10	1	5	141	141	3464
$W_{slot} = 50\mu m$, $t = 500\mu m$, $t_{ox} = 3\mu m$, $t_{uox} = 1\mu m$							

Table 5.4: Geometrical dimensions of analyzed spiral inductors.

5.3.3.5 Validation

The measurement of a battery of inductors implemented on a low resistivity SOI substrate has validated this model. The geometrical parameters, as defined in section 5.3.1, are given in Table 5.4. The distance between the inductance and the ground plane (W_{slot}) was chosen sufficiently large to prevent exciting the slot line which is surrounding the inductor. This slotline can introduce a spurious resonance in the frequency behavior of the component [6]. If this dimension (W_{slot}) is kept small, the admittance matrix of the slot line must be added in the structure following sparse matrix technique. Table 5.5 compares the measured inductance value with the one extracted from our transmission line model and these presented in the introduction (Table 5.1). The difference between measurements and simulated results is small. But instead of the other models, the new model shows, as the measurements, a variation of the inductance when the dimensions of the inner hole are changed (45EH10, 45EH30). This is in agreement with the measurements.

The real improvement of the model compared to the others is a better modeling of the frequency behavior of all the components, without any fitting or optimization. A comparison between the measurement of the inductor 55T and results from simulations on a $40MHz - 40GHz$ frequency band is shown in Figure (5.22). Only the models giving analytical expressions of the components of their equivalent circuit are plotted.

Label	35T	45TS5	45TEH10	45TEH30	55T	85T	35TCsT	45TCsT
L_{meas}	1.65nH	2.9nH	2.51nH	2.68nH	4.14nH	11.4nH	9.4nH	6.8nH
$L_{Ronkainen}$	1.929nH	3.5nH	3.23nH	3.23nH	4.954nH	13.34nH	9.5nH	7.4nH
ε_r	+17%	+21%	+29%	+21%	+20%	+17%	+9%	+9%
L_{Yue}	1.52nH	2.8nH	2.3nH	2.55nH	4.05nH	10.8nH	9.3nH	6.74nH
ε_r	-8%	-3%	-8%	-5%	-2%	-5%	-1%	-1%
L_{Crols}	1.72nH	3.3nH	3.03nH	3.01nH	4.77nH	13.6nH	10.5nH	7.48nH
ε_r	+4%	+14%	+21%	+12%	+15%	+20%	+12%	+10%
L_{Mohan}	1.48nH	2.75nH	2.55nH	2.55nH	3.98nH	11.17nH	8.81nH	6.56nH
ε_r	-10%	-5%	+2%	-5%	-4%	-2%	-6%	-4%
$L_{New\ model}$	1.8nH	3.2nH	2.56nH	2.94nH	4.49nH	12.2nH	10.0nH	7.4nH
ε_r	+9%	+10%	+2%	+10%	+8%	+7%	+6%	+9%

Table 5.5: Comparison between measured and simulated inductance values obtained with different inductor models for various square spiral inductors built on silicon substrate.

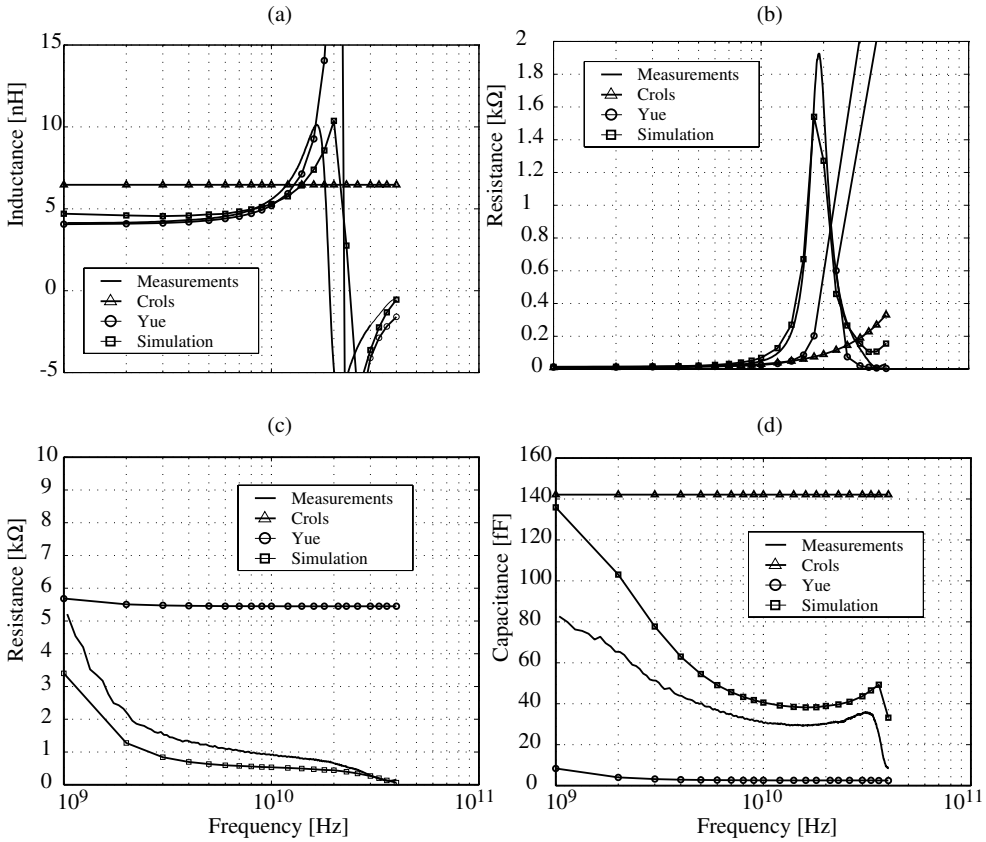


Figure 5.22: Measured and simulated equivalent π-model lumped elements Ls (a), Rs (b), Cp (c), and Rp (d) for a square spiral inductor of 5.5turns (called 55T in Table 5.4)

Contrary to the other presented models, all of the simulated equivalent parameters (L_s, R_s, C_p, and R_p) are fairly evaluated over the whole frequency band. As our model uses the physical structure of the substrate, it is not technology dependent. Indeed, Figures 5.23 and 5.24 show the good agreement between the measurement and the simulation results of an inductor made on a lossy and on a lossless substrate. Very good agreement is obtained for both inductors.

Furthermore, as the model reproduces fairly the behavior of the substrate, the quality factor of the inductor is correctly estimated, not only in terms of its maximal value but also in the whole frequency band (Figure 5.25).

5.3.3.6 Discussion

Due to a more accurate modeling of the substrate, and the transmission line approach, a wideband model of integrated inductor has been developed. Our

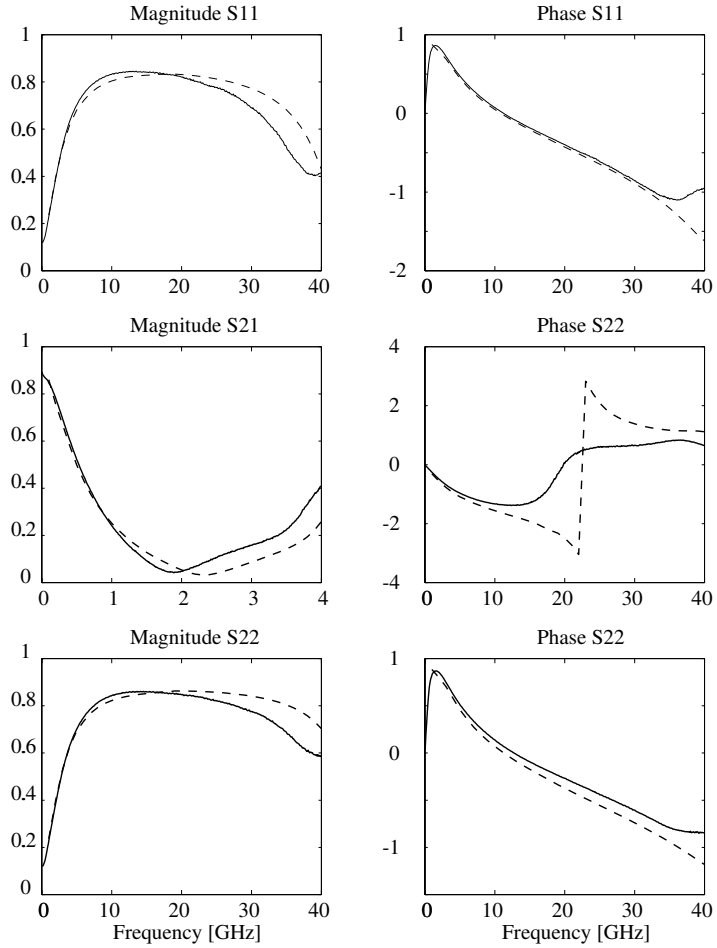


Figure 5.23: Measured and simulated S-parameters from 40MHz to 40 GHz for a square spiral inductor of 5.5 turns (called 55T in Table 5.4) built on a low resistivity silicon substrate.

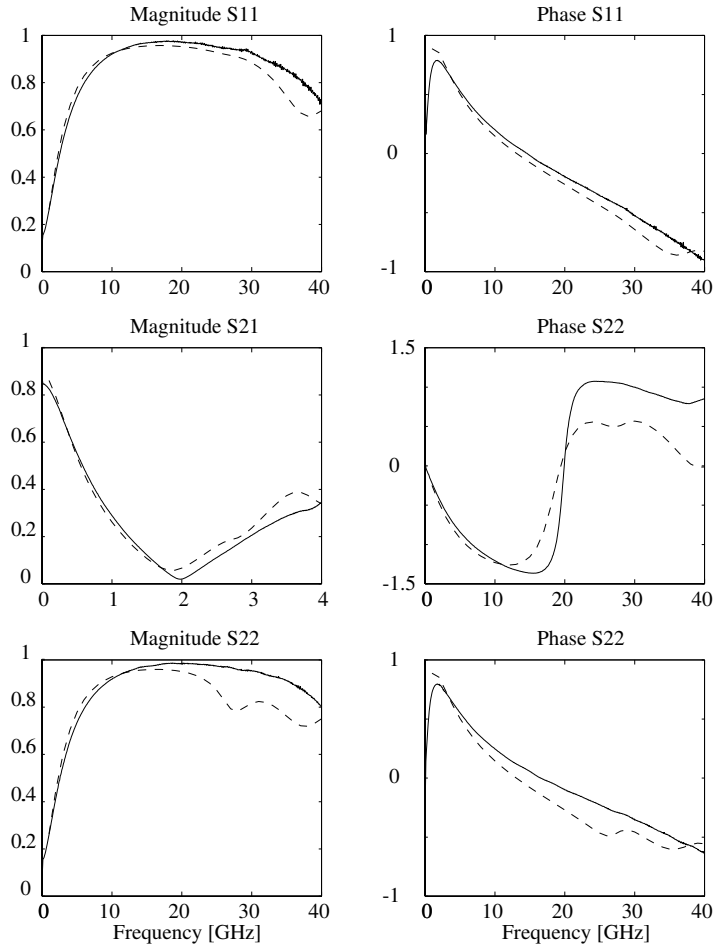


Figure 5.24: Measured and simulated S-parameters from 40MHz to 40 GHz for a square spiral inductor of 5.5 turns (called 55T in Table 5.4) built on a quartz wafer.

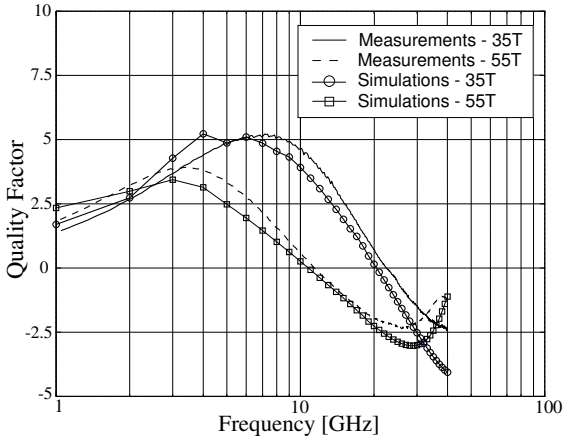


Figure 5.25: Measured and simulated quality factor from 40MHz to 40GHz for a square spiral inductor of 5.5 turns (called 55T in Table 5.4) built on quartz and low resistivity silicon wafers.

model has been validated with several measurements of square spiral integrated inductors having an inductance value situated between 1.6 and 12 nH. The better results in the frequency band are obtained for the inductors up to 5.5 turns. For higher number of turns, the effect of the bends becomes more and more significant.

Thereby, the accuracy of this model will decrease as the number of turn increases. Moreover, the non-modeling of the bends can be responsible of the systematic overestimated values of the inductors. Indeed, GETSINGER has demonstrated in [35] that a right angle bend produces an equivalent negative inductance, which reduce the total inductance of an inductor. In order to increase the performances of our model, a correct modeling of the bends should be introduced.

Also, the accuracy of this model is directly linked to the precision obtained for the calculation of the transmission line parameters. This calculation implies the evaluation of several integrals of oscillating functions with an infinite limit of integration (Appendix D). Depending on all of the geometrical parameters, the evaluation of these integrals is a challenging numerical problem, which needs to be checked when a new technology is used.

The time consumption necessary to model an inductor is relatively small (less than half an hour for the biggest one) compared to those necessary for a 2.5 or 3D electromagnetic solver (some hours for the smallest). This result is

achieved thanks to a previous calculation of the transmission line parameters used in the model. This calculation requires nearly 3 days of computing by using Matlab from MATHWORKS CORP. on an UltraSparc2 workstation, but it must only be done once for a given strip width. After that preliminary calculation, the time required to simulate the biggest inductor (85T) between 40MHz and 40GHz was less than 30 minutes

The model developed has some real interest for the RF designer, because it models accurately all the equivalent circuit elements of the inductor, whatever technology is used. For the simple models, the value of the inductance cannot be easily linked to the geometrical parameters. As a consequence, an optimization of the design of an inductor under some constraints, as minimum area with maximum Q for a given value of inductance, is not easily obtained.

The best method to design an inductor is probably a mixing of empirical formulae, like those proposed by MOHAN or GREENHOUSE [18][21], to determine the inductor layout, followed by simulation with our model to evaluate accurately the losses.

5.3.4 Prospective design of square spiral inductor.

5.3.4.1 Introduction

Using the developed model, some guidelines for the design of integrated inductors can be deduced. Some new technological solutions can also be investigated easily before processing, thanks to the use of the variational principle.

In the following section, some general guidelines for the design of inductors are provided. And some simulations of inductors made one alternative substrate are shown in order to illustrate the potency of our model.

5.3.4.2 Design rules

The design rules proposed here give some idea of the effect of the geometrical parameters and how to set these parameters to maximize the Q factor, as defined by Equation (5.12), below the resonant frequency. These rules are deduced from several simulations made for inductors built on SOI substrate and can be

extrapolated to other silicon based technologies.

Dimension of the inner hole The influence of the inner hole of the inductor is directly linked to the mutual inductance between the strips. Indeed, as it is presented in Table 5.5, the mutual inductance between strips laying on both sides of the hole reduces the overall inductance of the inductor. Then, the dimension of the hole should be maximized under certain limit, as the size of the inductor must remain relatively “small" ensuring a high circuit density on die.

Before dealing with the dimension of the hole, the shape of the inductance must be determined. The measurement and the simulation have highlighted the influence of the negative coupling with the inductance called 45TH10 and 45TH30 in Table 5.5. Figure 5.26 shows the variation of the inductance of simulated inductors when the dimension of the hole is changed, keeping constant the perimeter of the inductance. The mutual inductance between strips is function of the total strips length, and is also function of the distance between the strips. Considering the four strips of Figure 5.27a, if the vertical dimension is reduced (Ev), the distance between these strips is reduced and the length of the horizontal strips will increase ($Length = Eh$). Then the negative mutual inductance ($Mh\_$) between these strips will also increase (Figure 5.27b). Meanwhile the opposite phenomenon happens to the vertical strips. The mutual inductance ($Mv\_$) between two strips is reducing quickly when the distance between the strip increases (Figure (5.28)). Then the optimal design for a square spiral inductor will be the one minimizing the ratio between the length of the strips and the distance between the strips. This design will be rectangular with Eh just larger than Ev ($\approx Ev + 2W$), simply because of the difference between the shape of the horizontal and vertical lines.

After determining the optimal shape of the inductor, the dimensions of the inner hole must be specified in order to maximize the Q-factor in the frequency band of interest.

In order to maximize the Q-factor for a given inductance value, the positive mutual inductance must be maximized with a sufficient number of turns, the

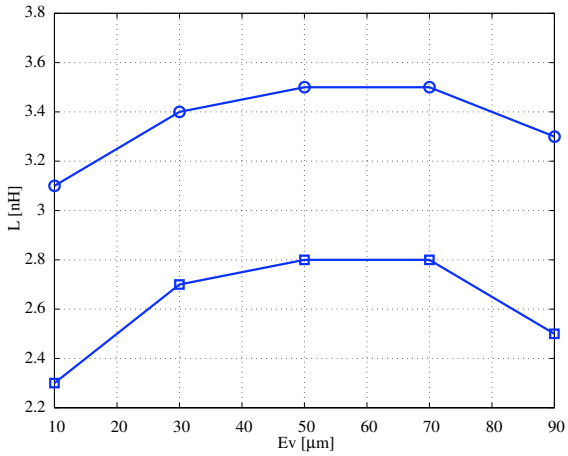


Figure 5.26: Variation of the inductance value of an integrated inductors with 4.5 turns and a spacing of $1\mu m$ (-square) and $10\mu m$ (-circle) for various dimension of the inner hole.

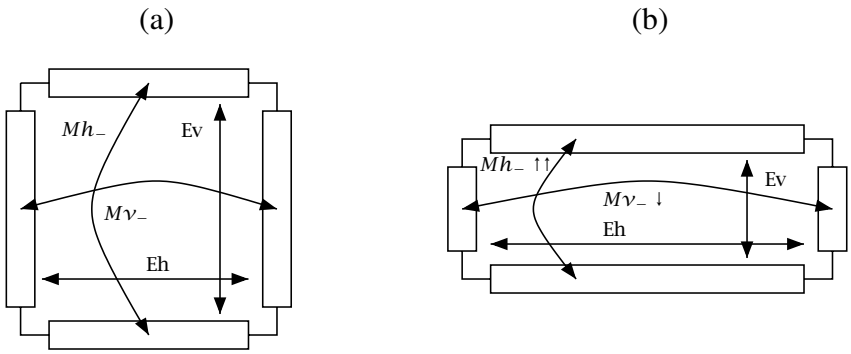


Figure 5.27: Shape influence of the inner hole of the inductance.

negative mutual inductance must be lowered by imposing a sufficiently large the inner hole, and the inductor resistance must be small. Then the total length of the inductor must be kept as small as possible. Also, the total area of the inductor must be reasonable in order to achieve a high circuits density on the die. LONG *et al.* give in [26] a minimal value for the inner hole of the inductor. This value must be greater than five line widths. This last assumption must be respected, because the negative coupling between the strips increases rapidly if the inner hole reduces too much, as shown in Figure 5.28.

The value of five line widths is probably not the optimal value, but it is a good estimation of the limit below which the performances of an inductor decrease. Some simulations have been done for different inductance values. After defining

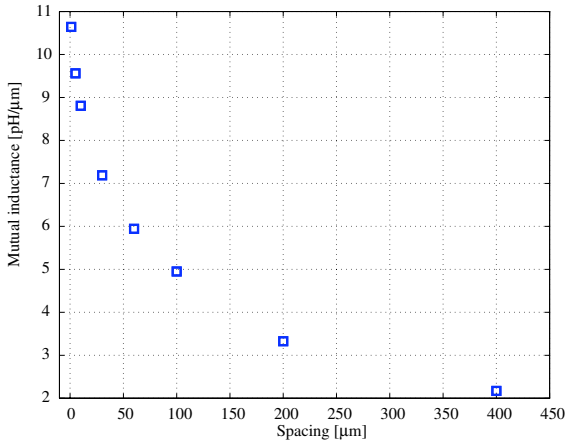


Figure 5.28: Mutual inductance of two microstrip lines with a width of $10\mu m$, simulated at 10GHz with the variational principle, as function of the spacing between the strips.

an inductance, the number of turns is changed and the dimension of the inner hole is modified in order to keep the same inductance value. Then the Q-factor is evaluated at 1GHz. Figure 5.29 shows the results of these simulation for 3 inductances of 1.25, 1.7, $2.3nH$ having a strip width of 5, 10, $15\mu m$ respectively. The optimal value for the dimension of the hole ranges between five and height line widths for all the simulated components.

Strips width The dimension of the strips influences also the different properties of the inductor. First, the width of the strips is directly related to the Q-factor by the ohmic losses. Second, the capacitance between the strips and the underpass is a linear function of the strip width. Then enlarging the strip will produce a reduction of the resonant frequency, and a reduction of the serial resistance at low frequency. At higher frequencies, as the skin depth is reducing, the improvement of the use of a wide strip becomes unimportant [36][37]. The better solution for reducing the ohmic losses is to use several metal layers connected together by vias to form the spiral [27], thicker metallization, or metal with a lower resistivity. Also the inductance can be drawn with varying the width of the strip to take into account the current distribution inside the strip. This last method, proposed by LOPEZ-VILLEGAS [36], increases the complexity of the layout, and makes difficult the optimization of the structure. For

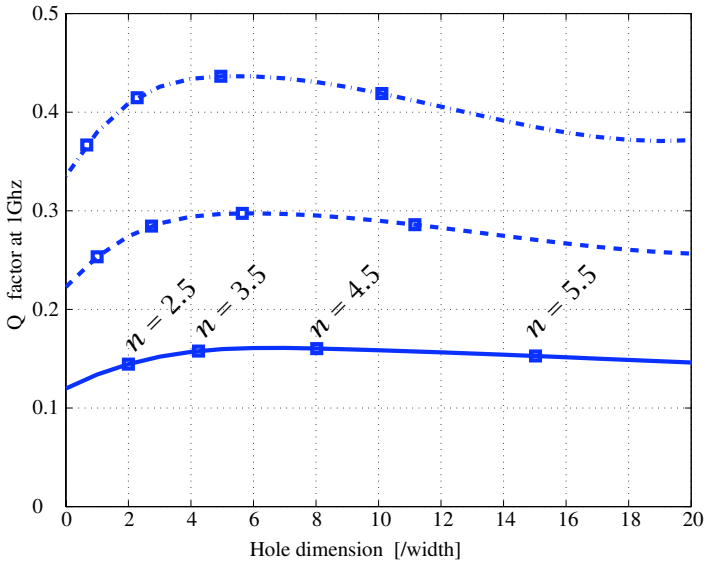


Figure 5.29: Q-factor of inductors of $1.25nH$ (—), $1.7nH$ (−−), and $2.3nH$ (−·−) for various dimensions of the inner hole.

the technology used, the better range for the conductors width is between 10 and $20\mu m$.

Spacing In order to maximize the quality factor, the positive mutual inductance between all the strip must be increased to its maximal value. The maximum is obtain when the distance between the strips is minimal, as shown previously (Figure (5.28)) [26].

Increasing the spacing increases the total length of the inductance. Then the lineic inductance of the spiral will increase, but the mutual inductance will be reduced. In such a case, it is not straightforward to determine the layout which maximizes the Q-factor. Numerous simulations have shown that the optimal design, in terms of Q-factor, is obtained when the spacing is set to the minimum available. Figure (5.30) presents some of the simulated results. For a given inductance value, the narrow spaced ($s = 1\mu m$) design requests a shorter inductance than the other ($s = 10\mu m$). Consequently, as the ohmic losses will be lower for the first inductance, its Q-factor will be higher.

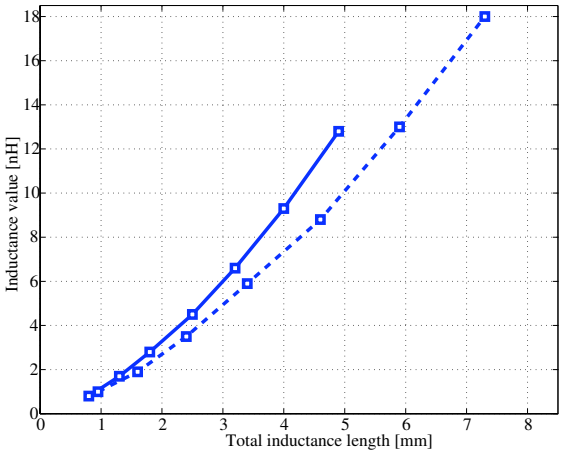


Figure 5.30: Inductance of inductors width a strip's width of 10μ and spacing of 1 and $10\mu m$ for various number of turns.

5.3.4.3 Prospecting new technologies

New technological solutions have been proposed to increase the performances of integrated inductors. Some authors describe the use of ground shield or heavily doped layer under the inductance to cancel the effect of the semiconductor substrate. Also some etching techniques are used to remove the silicon substrate under the inductor. All these solutions try to increase the quality factor of the inductor by lowering the losses. Another solution will be to increase the inductance value by introducing a layer of magnetic material in the substrate.

All this configuration can be studied with the developed model.

Ground shield and heavily doped layer These structures proposed by YUE in [11], are shown in Figure (5.31a,b). Their property is to present a ground plane below the inductance. The fields don't go through this ground plane, then the behavior of the inductor is not affected by the substrate. In that case, current loops appear in the ground plane and produce a negative mirror inductance which makes the classical formulae unusable. Introducing the structure into our model (Figure (5.31c)), the behavior of the simulated inductance is similar to the inductance measured by YUE. The difference between the two curves can be explained by the fact that the cross-section of the structure is not known in

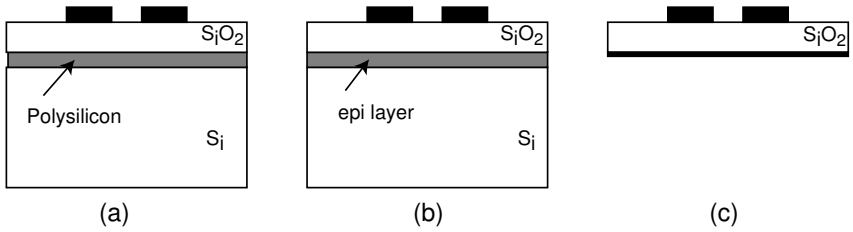


Figure 5.31: Cross section of alternative structure of integrated inductor using a polysilicon ground plane(a), or a heavily doped layer (b). And cross section used for simulation (c)

details (Figure 5.32).

Using magnetic layer Using high permeability materials can increase the inductance value of the inductor. Some simulation have been done, as a prospective study, about the influence of a magnetic layer situated under the spiral. Figure 5.33 shows the simulated results for a square spiral inductor composed of 3.5 turns with W=10 μm, S=10 μm and E_v=E_h=50 μm. This planar inductor is considered on a high resistivity silicon substrate with and without a magnetic layer with a relative permeability of 50 and a thickness of 50 μm. Results show the increase of the inductance value of more than 300 % and a quality factor at 5 GHz of 24 instead of 8.1 for the same spiral inductor by using a high-μ layer. Due to the increase of the inductance by turns with the use of high-μ layers, we can also see interests for decreasing the occupied area of integrated inductors for a given inductance value and then for contributing to the integration of passive elements on chips.

5.4 Conclusion

Along this chapter, a study of passive elements made on modern SOI technologies has been presented. First, topology of transmission lines has been investigated. The interest of thin film microstrip lines has been highlighted. Since TFMS avoids coupling from the signal to the silicon substrate, we think this kind of lines will be the most useful transmission line in the future generation

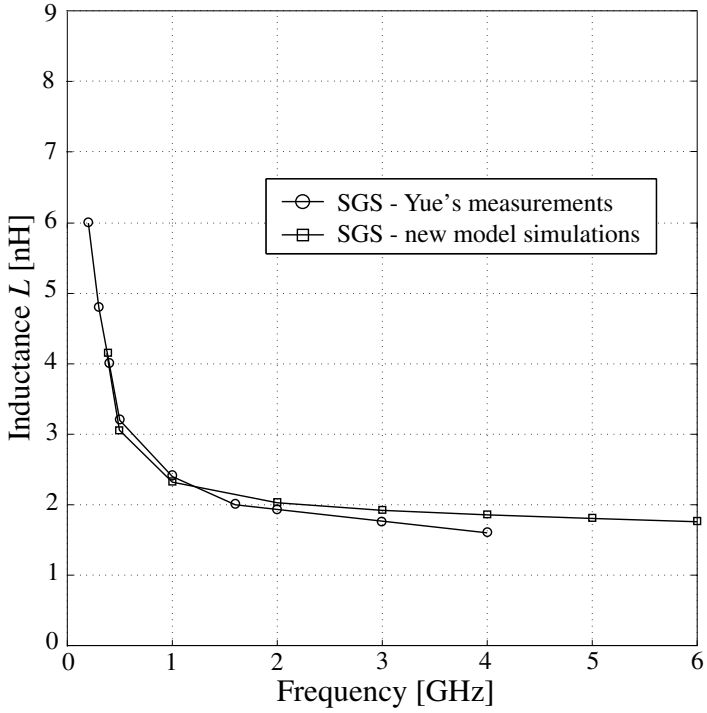


Figure 5.32: Simulated and measured inductance [11] of an inductor with a ground shield.

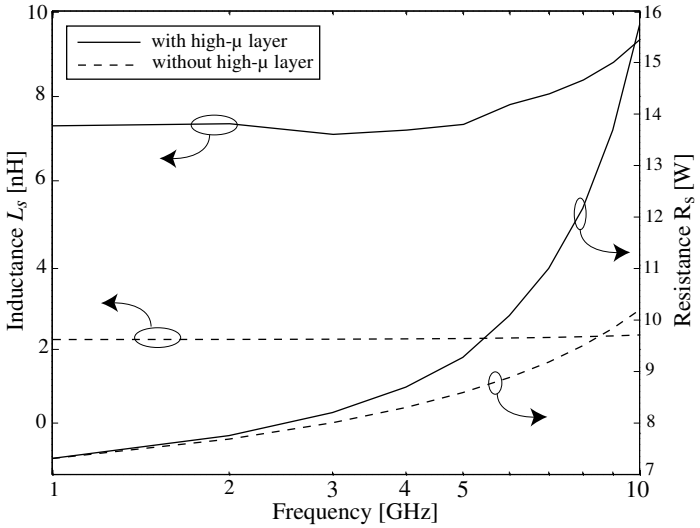


Figure 5.33: Simulated equivalent inductance L_s and series resistance R_s for a square spiral inductor built on a high-resistivity silicon wafer with and without a high permeability layer

of microwaves circuit on silicon-based technologies. Also, properties of TFMS lines do not depend on the under-laying substrate. Thus cheap, standard SOI wafers can be used. Second, analysis of square spiral inductor has been made. A model, based on a transmission line approach has been developed and validated. The study of the coupling between strips has lead to useful guidelines for the design of integrated inductor.

References

[1] B.M.Frank, A.P.Freundorfer, and Y.M.M.Antar, "Performance of 1-10ghz traveling wave amplifiers in 0.18 μm cmos," *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 9, pp. 327–329, Sept. 2002.

[2] Zeeland Software, *IE3D manual*, 2003.

[3] P.Arcioni, R.Castello, L.Perregrini, E.Sacchi, and F.Svelto, "An innovative modelization of loss mechanism in silicon integrated inductors," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 12, pp. 1453–1460, Dec. 1999.

[4] C.P.Yue, C.Ryu, J.Lau, T.H.Lee, and S.S.Wong, "A physical model for planar spiral inductors on silicon," in *Proc. IEDM 1996*, Dec. 1996, pp. 155–158.

[5] S.F.Mahmoud and E.Beyne, "Inductance and quality-factor evaluation of planar lumped inductors in a multilayer configuration," *IEEE Trans. on Microwave Thory and Techniques*, vol. 45, no. 6, pp. 918–923, June 1997.

[6] J-P.Raskin, *Modeling, characterization and optimization of MOSFET's and Passive Elements fot the synthesis of SOI MMIC's*, Ph.D. thesis, Université catholique de Louvain, 1997.

[7] D.Kajfez and E.J.Hwan, "Q-factor measurement with network analyzer," *IEEE Trans. on Microwave Thory and Techniques*, vol. 32, no. 7, pp. 666–670, Jul. 1984.

[8] J.N.Burghartz, D.C.Edelstein, K.A.Jenkiin, and Y.H.Kwark, "Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low-loss substrates," *IEEE trans. on microwave theory and techniques*, vol. 45, no. 10, pp. 1961–1968, Oct. 1997.

[9] A.M.Nikjejad, R.Gharpurey, and R.G.Meyer, "Analysis, design, and optimization of spiral inductors and transformers for si rf ics," *IEEE Journal of solid-state circuits*, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.

[10] K.K.O., "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies," *IEEE Journal of Solid State Circuits*, vol. 33, pp. 1249–1252, Aug 1998.

[11] C.P.Yue and S.S.Wong, "On-chip spiral inductors with patterned ground shields for si-based rf ics," *IEEE Journal of Solid-state circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[12] B.Razavi, *RF microelectronics*, Prentice Hall Communications Engineering and energing technologies series, 1998.

[13] M.Danesh, J.R.Long, R.A.Hadaway, and D.L.Harame, "A q-factor enhancement technique for mmic inductors," *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, no. 1, pp. 183–186, 1998.

[14] M.Goffioul, D.Vanhoenacker, and J-P.Raskin, "Direct extraction techniques of microwave small-signal model and technological parameters for sub-quarter micron soi mosfet's," *5th Symposium Diagnostics and Yield, SOI - materials, devices and characterization*, July 2000.

[15] B.Parvais and J-P.Raskin, "Oscillateurs rf intégrés en technologie cmos/soi," in *Journées Nationales Micro-ondes JNM2001*, May 2001, pp. 4D–18.

[16] D.G.Swanson, "A novel method for modeling coupling between several microstrip lines in mic's and mmic's," *IEEE Trans. on Microwave Theory and Techniques*, vol. 39, no. 6, pp. 917–923, June 1991.

[17] D.Lovelace, N.Camilleri, and G.Kannell, "Silicon mmic inductor modeling for high volume, low cost applications," *Microwave Journal*, pp. 60–71, Aug. 1994.

[18] S.S.Mohan, M.del Mar Hershenson, S.P.Boyd, and T.H.Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid state Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[19] R.Ronkainen, H.Kattelus, E.Tarviken, T.Tiihisaari, M.Anderson, and P.Kuivalen, "Ic compatible planar inductors on silicon," in *IEE Proceedings Circuits Devices Systems*, 1997.

[20] J.Lau, T.H.Lee, S.S.Wong, C.P.Yue, and C.Ryu, "A physical model for planar spiral inductors on silicon," in *IEEE 1996 IEDM technical digest*, 1996.

[21] H.M.Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE transactions on parts, hybrids and packaging*, 1974.

[22] J.Crols, P.Kinget, J.Craninckx, and M.Steyeart, "An analytical model of planar inductors on lowly doped silicon substrates for analog design up to 3ghz," in *Symp VLSI Circuits - Digest Tech papers*, 1996.

[23] M.Park, S.Lee, H.K.Yu, and J.G.Koo, "High q cmos-compatible microwave inductors using double-metal interconnection silicon technology," *IEEE Microwave and guided wave letters*, vol. 7, no. 2, pp. 44–47, Feb. 1997.

[24] A.J.BadenFuller and A.M.Parker, "Equivalent-circuit of microstrip spiral inductor circuit generation by computer," *Electronics Letters*, vol. 21, no. 7, pp. 279–280, Mar. 1985.

[25] B-K.Kim, B-K.Ko, K.Lee, and S-C.Kim, "Monolithic planar rf inductor and waveguide structures on silicon with performance comparable to those in gaas mmic," in *1995 IEEE IEDM Technical Digest*, Dec. 1995, pp. 29.4.1–29.4.4.

[26] J.R.Long and M.A.Copeland, "The modeling, characterization, and design of monolithic inductors for silicon rf ic's," *IEEE journal of Solid-State Circuits*, vol. 32, no. 3, pp. 357–368, Mar. 1997.

[27] J.N.Burghartz, M.Soyuer, and K.A.Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. on Microwave Theory and Techniques*, vol. 44, no. 1, pp. 100–104, Jan. 1996.

[28] R.A.Johnson, C.E.Chang, P.M.Asbeck, M.E.Wood, G.A.Garcia, and I.Lagnado, "High q cmos compatible microwave inductors using double-metal interconnection silicon technology," *IEEE Microwave and guided wave letters*, vol. 7, no. 9, pp. 323–325, Sept. 1996.

[29] I.Huynen, "Novel fast multiline analysis of parasitic effects in cpw inductors for mmic's," *IEEE microwave and guided wave letters*, vol. 8, no. 2, pp. 72–74, Feb. 1998.

[30] J.Malherbe, *Microwave transmission line filters*, Artech House, 1979.

[31] Silvaco International Software, *Atlas manual*, 2000.

[32] P.R.Sheperd, "Analysis of square-spiral inductors for mmic's," *IEEE Trans. on microwave theory and techniques*, vol. 32, no. 4, pp. 467–472, Apr. 1984.

[33] J.A.Dobrowolski, *Introduction to computer methods for microwave circuit analysis and design*, Artech House, 1991.

[34] I.Huynen, "Integrated microwave inductors on silicon-on-insulator substrate," in *Proceeding of the EuMC*, 1997, pp. 1008–1013.

[35] W.J.Getsinger, "End-effects in quasi-tem transmission lines," *IEEE trans. on Microwave theory and techniques*, vol. 41, no. 4, pp. 666–672, Apr. 1993.

[36] J.M.Lopez-Villegas, J.Samitier, C.Cane, P.Losantos, and J.Baussels, "Improvement of quality factor of rf integrated inductors by layout optimization," *IEEE Trans. on Microwave and Techniques*, vol. 48, no. 1, pp. 76–83, Jan. 2000.

[37] J.Craninckx and M.S.Steyaert, "A 1.8ghz low phase noise vco using optimized hollow spiral inductors," *IEEE journal of Solid State Electronics*, vol. 32, no. 5, pp. 736–744, May 1997.