Fast and accurate modelling of large TSV arrays in 3D-ICs using a 3D circuit model validated against full-wave FEM simulations and RF measurements

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***Abstract*—This paper presents a 3D circuit model capable of rapidly and accurately evaluating substrate noise coupling in the context of 3D integration. Since TSVs are large and noisy structures, the evaluation of electromagnetic coupling to and from TSVs has become crucial to the design of three-dimensional integrated circuits. In this work, we present a fast and accurate 3D circuit model to this end. The model is verified against full-wave simulations and wideband S-parameter measurements of three different TSV structures, including guard rings and up to four TSVs. The model maintains the accuracy of full-wave simulations while presenting a speed increase of 2 to 3 orders of magnitude. This features enables the model to investigate the coupling parameters and crosstalk voltages in very large and complex 3D volumes. Our powerful model provides new opportunities in large scale analysis, and as an example an 11x11 TSV array is simulated in both frequency- and time-domain over a wide frequency band including 121 TSVs and circuit nodes.**

TSV; substrate noise; crosstalk; 3D-IC; noise coupling; 3D circuit model ; shielding ; guard ring

I. INTRODUCTION

Planar scaling of ICs following Moore's law is nearing its limits. Alternatively, 3D integration follows a more-than-Moore strategy in which circuit layers are stacked vertically. The enabling technology for connections in the third dimension is the through silicon via (TSV). TSV-based 3D integration has the potential to significantly boost the performance and capabilities of state-of-art ICs, while supporting the integration of heterogeneous technologies [1]. TSVs are however large and noisy structures capable of interfering significantly with the operation of neighboring devices and circuits. For this reason the evaluation of electromagnetic (EM) coupling to and from TSVs has become crucial to the design of three-dimensional integrated circuits (3D-ICs). Therefore a fast and accurate model, that can take into account substrate effects (such as crosstalk and losses), capable of simulating large 3D structures with multiple nodes and ports is essential for reliable 3D-IC design. In this work, we present our "3D circuit model" that fulfills all of the above requirements towards 3D-IC modelling. The model is verified against wideband S-parameter measurements of three different TSV structures, including guard rings and up to four TSVs. The model is also in agreement with the commercially available full-wave simulation software Ansys HFSS, and outperforms it in terms of simulation time while maintaining accuracy. This allows the newly developed model to simulate large 3D structures that are inaccessible to HFSS, simply due to their size and/or number of ports of interest, and to explore TSV coupling and signal integrity over a wide range of parameters. Using the newly developed model, an 11x11 TSV array was simulated, including 121 TSVs and 242 RF ports (top and bottom of each TSV) to generate a 242x242 S-matrix over a wide frequency band (10 MHz to 100 GHz) in under 15 minutes, demonstrating the power of the model and its potential for CAD applications. We then further extrapolate the model to investigate the influence of TSV driver and load impedances on the substrate noise injection, and highlight the behavior or coupling alleviation and shielding techniques under these realistic conditions.

II. THE 3D CIRCUIT MODEL

A fast and accurate model capable of simulating substrate volumes with multiple nodes and ports is required in the context of 3D-IC design. Employing full-wave numerical simulators, such as HFSS, provides the needed accuracy, however such solutions are slow and memory intensive [2, 3] and as such are not suitable for large-scale analysis and design optimization. On the other hand, compact lumped element equivalent circuit simulations [4, 5] are very often limited to a single TSV pair, are difficult to extend and apply to different contexts, and cannot capture the complex field distributions that arise in the silicon substrate in the presence of additional TSVs or circuit nodes (such as transistors or guard rings) [6].

A. Modelling approach

The proposed 3D circuit model is based on a very large distributed network of discrete lumped elements that make up unit cells, up to 20,000, all connected together to represent the 3D volume and its properties and simulated to yield an S-parameter matrix over a wide frequency band. The entire volume is discretized into many of these unit cell elements, depicted in Fig. 1, that are then electrically connected together. The dimensions of the cell are described by the three parameter h_{unit}, l_{unit} and w_{wnit}, the height, length and width of the unit cell respectively.

The TSV unit cell, shown in Fig. 1 (a), is constructed using series self-resistance and self-inductance elements as

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well as shunt capacitance elements. The TSV unit cell elements are given by (1) – (7).

The TSV resistance is mainly frequency dependent due to the skin effect that occurs at high frequencies, and the total TSV resistance per unit cell is calculated by the root-squared value of the AC and DC resistance terms [7, 8].

$$R_{TSV} = \sqrt{\left(R_{TSV-DC}\right)^2 + \left(R_{TSV-AC}\right)^2} \tag{1}$$

$$R_{TSV-DC} = \frac{\rho_{TSV} h_{unit} / 2}{\pi r_{TSV}^2} \tag{2}$$

$$R_{TSV-AC} = \frac{\rho_{TSV} h_{unit} / 2}{\pi\left(2 r_{TSV}\delta - \delta^2\right)} \tag{3}$$

$$\delta = \sqrt{\frac{\rho_{TSV}}{\pi \mu f}} \tag{4}$$

Where r_{TSV} is the TSV's metal radius, ρ_{TSV} and μ are the TSV's metal resistivity and magnetic permeability, and δ is the skin depth inside the conductor at frequency f.

The self-inductance terms of a single TSV cell are modelled according to (5) [8, 9].

$$L_{TSV} = \frac{\mu h_{unit} / 2}{2\pi}\left[\ln\left(\frac{h_{TSV}}{r_{TSV}} + \sqrt{\left(\frac{h_{TSV}}{r_{TSV}}\right)^2 + 1}\right)\right.$$

$$\left. + \frac{r_{TSV}}{h_{TSV}} - \sqrt{\frac{r_{TSV}}{h_{TSV}} + 1}\right] \tag{5}$$

The capacitive elements of a TSV unit cell are modelled as cylindrical capacitors by (6) and (7). The TSV oxide liner defines the capacitance terms C_{ox}. The TSV's interface with the silicon bulk may be in a state of depletion, which is modelled by the capacitance terms C_{dep}.

$$C_{ox} = \frac{1}{4} \cdot \frac{2\pi\varepsilon_{ox} h_{unit}}{\ln\left(\frac{r_{TSV} + t_{ox}}{r_{TSV}}\right)} \tag{6}$$

$$C_{dep} = \frac{1}{4} \cdot \frac{2\pi\varepsilon_{Si} h_{unit}}{\ln\left(\frac{r_{TSV} + t_{ox} + t_{dep}}{r_{TSV} + t_{ox}}\right)} \tag{7}$$

It is common for the TSV/Si interface to be in depletion or inversion due to the presence of fixed positive oxide charges in the TSV liner [10, 11] for standard resistivity p-type substrates (10 Ωcm). For this reason, all depletion widths considered in this text will be considered as maximal. They can either be estimated by solving Poisson's equation in cylindrical coordinates [2] or through the use of a semiconductor simulation tool such as ATLAS TCAD Silvaco software [12] for a known nominal substrate resistivity.

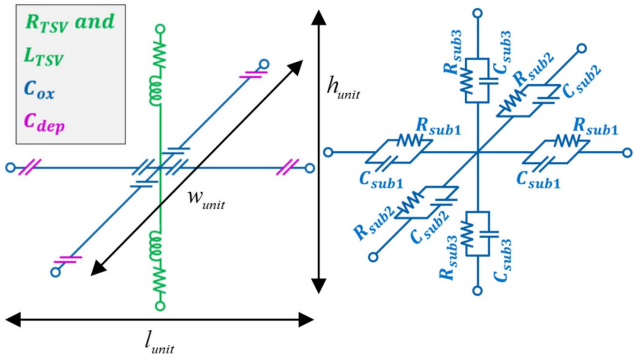

Figure 1. Equivalent circuit model for the 3D unit cells. (a) TSV unit cell. (b) Silicon substrate unit cell.

The substrate unit cell, shown in Fig. 1 (b), is modelled using parallel resistances and capacitances whose expressions are given by (8) – (13).

$$R_{sub1} = \rho_{Si} \frac{l_{unit} / 2}{w_{unit} h_{unit}} \tag{8}$$

$$C_{sub1} = \varepsilon_{Si} \frac{w_{unit} h_{unit}}{l_{unit} / 2} \tag{9}$$

$$R_{sub2} = \rho_{Si} \frac{w_{unit} / 2}{l_{unit} h_{unit}} \tag{10}$$

$$C_{sub2} = \varepsilon_{Si} \frac{l_{unit} h_{unit}}{w_{unit} / 2} \tag{11}$$

$$R_{sub3} = \rho_{Si} \frac{h_{unit} / 2}{w_{unit} l_{unit}} \tag{12}$$

$$C_{sub3} = \varepsilon_{Si} \frac{w_{unit} l_{unit}}{h_{unit} / 2} \tag{13}$$

B. *Model validation*

In order to verify the proposed model, it is compared to full-wave HFSS simulations as well as to on-wafer measurement structures. The three TSV coupling test structures that were fabricated and measured are depicted in Fig. 2.

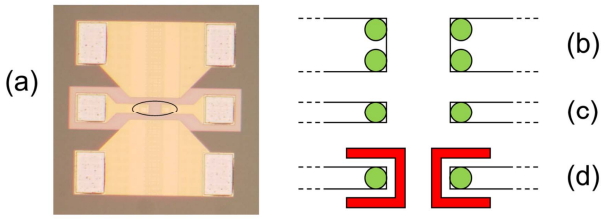

Figure 2. The fabricated TSV coupling test strucutres. (a) Photograph of the two port device including the feed CPW lines and the GSG probe landing pads. (b) Two-TSV to two-TSV coupling structure. (c) One-TSV to one-TSV coupling structure. (d) Guard-ring-TSV to guard-ring-TSV coupling structure.

All measurements were performed using GSG on-wafer probes and a vector network analyzer with a wideband frequency sweep from 10 MHz to 67 GHz. The TSV coupling structures are all accessed through 50 Ω CPW lines isolated from the silicon bulk by a 400 nm oxide. Fig. 2 (a) shows these CPW access lines as well as the GSG pads fabricated for the RF probes to land on during measurements. The coupling structures defined at the center of Fig. 2 (a) (encircled region), where the two CPW lines come together, are one of three configurations. The first is the coupling between two parallel connected TSV to two neighboring parallel connected TSVs. This set-up is schematically represented in Fig. 2 (b). The second type of structure is the single TSV to single TSV coupling set-up depicted schematically in Fig. 2 (c). The third coupling structure is that between a single TSV shielded by a grounded substrate contact or guard-ring at the surface (p^+ doped region that defines an Ohmic contact to the bulk), to an adjacent single TSV also shielded by such a guard-ring. This structure is schematically depicted in Fig. 2 (d) in which the red regions that define the guard rings are connected to the ground lines of the CPW (this connection is not shown). All three coupling structures were fabricated using the TSV technology parameters recapped in table 1. The fabricated structures were measured, and simulated using both HFFS and our own newly developed 3D circuit model. The agreement of the model with HFSS full-wave simulations and the S-parameter measurements is shown in Fig. 3 for all three test structures. The complex RF field distributions that arise in the bulk Si volume between the vias is accurately represented by our model, and the excellent agreement with all measured data permits its validation, in the case of multiple TSVs and also in the presence of grounded substrate nodes or guard rings.

TABLE I. TSV TECHNOLOGICAL PARAMETERS

Symbol	*Description*	*Value*	*Units*
r_{TSV}	TSV metal conductor radius	2.3	µm
h_{TSV}	TSV height	50	µm
t_{ox}	Oxide liner thickness	200	nm
p	Center to center TSV pitch	35	µm
ρ_{Si}	Silicon substrate nominal resistivity (measured)	5	Ωcm
t_{dep}	Depletion layer thickness (extracted)	460	nm

Furthermore, the model also shows excellent agreement with the full-wave EM simulator HFSS while being approximately 200 times faster. This is because a lumped modelling approach simplifies Maxwell's equations into linear Kirchhoff relations, which are much easier to solve. Such a modelling approach is valid in evaluating the coupling in 3D-IC structures between two nodes distant by up to 200 µm for frequencies up to 50 GHz (indeed, at these frequencies the wavelength of the RF waves in the materials considered are more than 20 times larger than the largest distance in the considered volume).

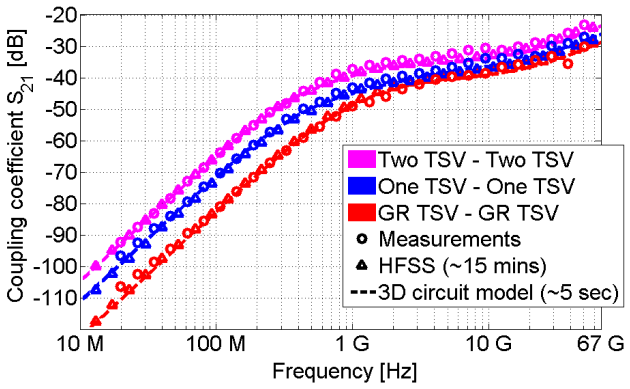

Figure 3. Simulated and measured coupling curves relative to the three different test strucures depicted in Fig. 2.

III. MODEL EXTRAPOLATION

In the following sections of the paper, the validated model will be used to simulate and investigate the electrical behavior of 3D-IC structures including large TSV arrays. Both frequency- and time-domain analysis will be run in order to demonstrate the versatility of the model. Then, special investigation into the effect of TSV load impedances will be presented.

A. *Large TSV arrays*

The drastic increase in simulation power brought to substrate coupling modelling by our validate model in the context of 3D integration allows for the first time the investigation of the full-coupling matrix in very large TSV arrays. To demonstrate this power, a square array of 11 by 11 TSVs was simulated. Fig. 4 depicts one quarter of the 121 simulated TSVs and introduces the port letterings that were used on the top side of the wafer. All of the same technological parameters as those given in table I were used, except for the TSV to TSV pitch which was modified to 15 µm.

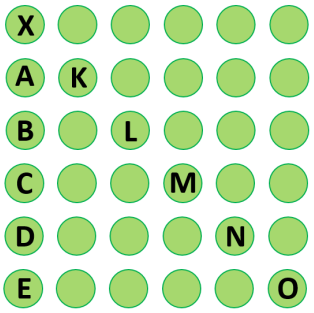

Figure 4. TSV top port lettering in the 11x11 TSV array simulation. Only one quarter of the array is depicted.

The RF port denoted as X is connected to the central TSV of the 11x11 array, on the top side. The entire 242x242 S-matrix of the 11x11 TSV array (two 50 Ω ports per TSV, top and bottom) was simulated, and a few of the coupling results are presented in Fig. 5 (referring to Fig. 4 for the port naming). Many of these coupling curves $S_{iX}(f)$ present a negative slope just after the point where the frequency is high enough for the electric fields to start to penetrate into the silicon bulk. Indeed, at low frequency, all of the coupling curves become almost equal. This is because the oxide capacitances are dominating the impedance paths between the nodes. Between any two TSVs of the array the impedance path is made up of two times the oxide capacitance in series with the silicon bulk resistance. Below a few hundred megahertz this second term is negligible compared to the first making the impedance paths between any two TSVs essentially equal, which is the reason why all the curves intersect at low frequency. At these frequencies the bulk is essentially acting as an equipotential volume. At higher frequencies however the electric fields start to penetrate into the silicon bulk and are captured predominantly by the surrounding TSVs. The noise power is no longer divided evenly between all the victim ports of the array. This is because the bulk impedance becomes the dominant term in the coupling paths, meaning that the noise power predominantly couples to the neighboring TSVs (TSVs A and K). This has the effect of drastically reducing the power coupled to the TSVs that are further away (D, E, N and O for example), to such an extent that the slopes of the coupling coefficients as a function of frequency become negative for these nodes. Although the impedance path to these far away TSVs reduces as a function of frequency, the impedance paths to the neighboring TSVs, which are competing impedance paths, reduces much faster. For this reason such coupling curves experience a negative slope once the potential starts to distribute itself inside the bulk. Curves of such shapes have been presented in [5, 13, 14] although no comments were given about the negative slope regions. In the work of [5] the introduction of a shielding TSV between two signal TSVs had the effect of alleviating coupling and introduced a negative slope region in the crosstalk curve at a few GHz. In [14] a 5x5 array of TSVs was simulated and negative slope regions in the coupling curves were obtained.

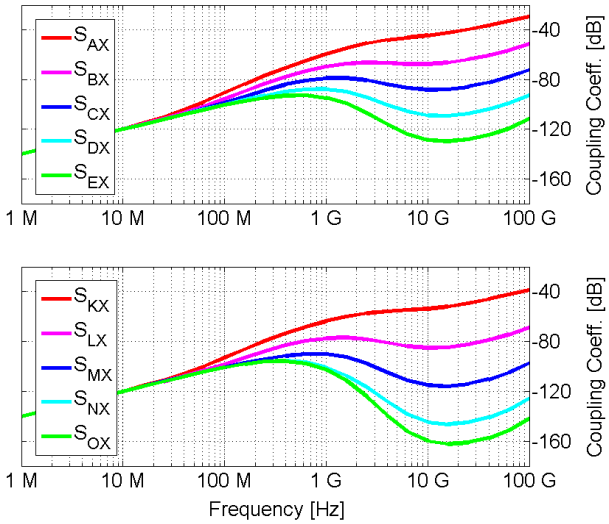

Figure 5. Couplig results of the 11x11 TSV array simulation.

B. *TSV driver and load impedances*

The coupling towards a victim node, as expressed in S-parameters, is dependent on the load impedance to ground at that node. Many studies represent the coupling S-parameters with reference to standard 50 Ω terminations and/or evaluate the crosstalk voltage between an aggressor TSV and a victim TSV loaded with 50 Ω [15-17]. Such low loading conditions, that are the standard for measurement equipment, are not realistic in the context of 3D integration as device input impedances are closer to the kilohm range at RF frequencies.

Fig. 6 plots the coupling coefficient between two TSVs of the 11x11 array for different loading conditions. The coupling is evaluated between the two TSVs shown in blue in the inset of Fig. 6. The one denoted as 'A' is considered as the aggressor TSV, and the one denoted as 'V' as the victim TSV. All other TSVs of the array are loaded with impedance values of Z_{Ref}, which was varied between 50 Ω, 1 kΩ and 10 kΩ. Several coupling alleviation configurations were investigated by grounding TSVs in the vicinity of the victim TSV. First, a single grounded shielding TSV between the two signal TSVs of interest was considered, and then the eight TSVs immediately surrounding the victim were grounded.

The results show that the coupling coefficient is shifted higher as the reference impedance value in increased. This is due to the fact that the signal TSVs that are excited from RF ports at the top of the wafer are loaded by impedances Z_{Ref} at the bottom side of the wafer. The insertion loss through the via (not shown) is degraded and the coupling into the bulk becomes higher. It is indeed these two coupling paths that are in competition to sink the RF current: through the via then into the load Z_{Ref}, or into the bulk and then towards other loaded TSV nodes.

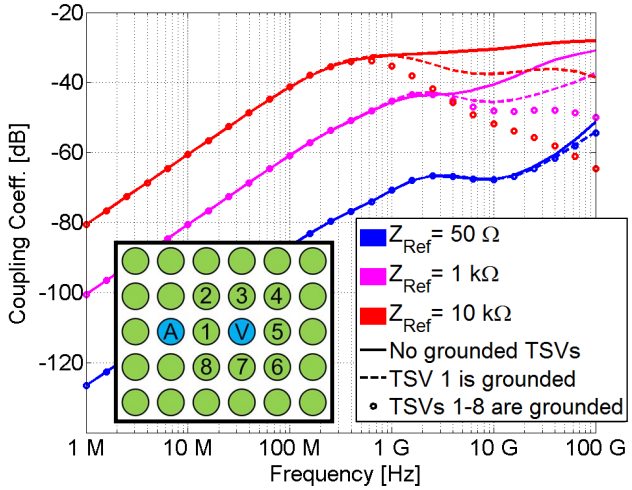

Figure 6. Coupling coefficient simulation results of the 11x11 TSV array simulation under three general loading conditions: 50 Ω, 1 kΩ and 10 kΩ, with different levels of EM shielding using grounded TSVs. Inset: depiction of the aggressor (A) and victim (V) TSVs in the array.

The results of Fig. 6 also show that in the case of 50 Ω reference impedances, substituting the 50 Ω loads of TSVs 1-8 for ground nodes (zero impedance loads) does not impact much at all on the coupling coefficient curve. This is because the impedance path between two neighboring TSVs is above 700 Ω in our simulations all the way up to 20 GHz, meaning that 50 Ω loaded TSVs are basically already acting as virtually grounded, and so shielding using a 50 Ω signal-TSV has the same effect as shielding using a grounded TSV. However, as the TSV load impedances are increased, an appreciable difference can be seen when substituting a signal TSV for a grounded TSV in the overall coupling coefficient, as can be seen from the purple and red curves of Fig. 6. The effect of the coupling alleviation of the shielding TSVs kicks in at the frequency at which the impedance path between TSVs becomes equal to the loading impedances. Before this frequency is reached, the TSV sidewall capacitance terms or bulk resistance terms dominate the impedance paths between TSVs. However, once the aforementioned frequency is reached, the electric fields between TSVs couple preferentially to the grounded vias that now have an appreciably lower path to ground than the loaded signal-TSVs. The shift in this frequency point can be observed for the different loading conditions, and is indeed seen to be inversely proportional to the load's value.

Fig. 7 shows the results of the time-domain voltage crosstalk simulations performed in the same context as the previous frequency domain results of Figs. 6. In these simulations, a 1 V amplitude voltage step with 20 ps of ramp-time was applied to the aggressor TSV of the array and the crosstalk voltage coupled to the victim TSV was obtained and plotted for the same set of loading and shielding configurations. The voltage driver's impedance was set to 200 Ω in all simulations.

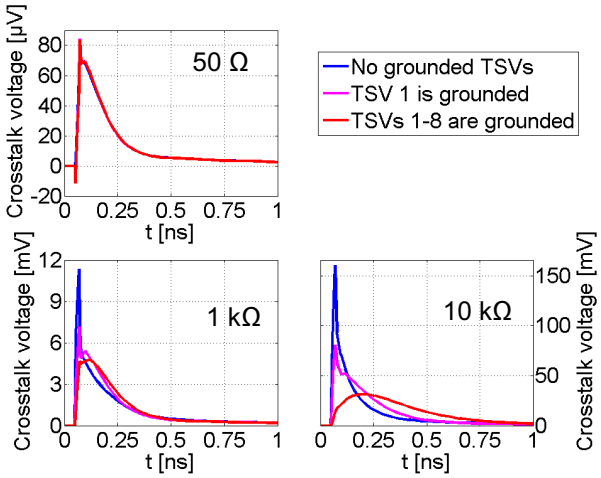

Figure 7. Voltage crosstalk results of the 11x11 TSV array simulation under three general loading conditions: 50 Ω, 1 kΩ and 10 kΩ, with different levels of EM shielding using grounded TSVs.

First, we notice again the increase in the coupling for higher loading conditions: the crosstalk voltage amplitude shows strong dependence on the TSV load's value.

Once again, as expected, the 50 Ω loaded TSVs act as being virtually grounded, and no improvement in the crosstalk voltage is to be found by replacing signal TSVs with shielding TSVs. However when the loading conditions are increased, improvements are observed when introducing the shielding TSVs. This improvement in diminishing the peak crosstalk voltage is around a factor of 2 for the 1 kΩ load case, and around a factor of 4 for the 10 kΩ loading case.

Fig. 8 plots the crosstalk voltage levels on a victim TSV in the case where one of its directly neighboring TSVs is acting as an aggressor (blue plots; TSV A1 shown in the inset is the only aggressor), and also in the case where its eight closest neighbors are all acting as aggressors (red plots; TSVs A1-A8 are all acting as aggressors). In this second case all voltage steps on the eight aggressing TSV nodes are synchronized in-phase. This enables us to extract the worst-case crosstalk voltage. It is also the most realistic switching scenario in a digital IC system because flip-flops will have a high chance of toggling together on the rising edge of the clock. Fig. 8 shows that higher impedance loads are more sensitive to voltage crosstalk. This crosstalk is however more easily alleviated for higher loaded TSVs, as we saw through the results of Fig. 7. For the 50 Ω terminated TSVs, the total electrical crosstalk obtained on the victim TSV through the

contributions of all eight aggressor TSVs amounts to a peak value of 6 mV. This results is coherent as the victim TSV is highly tied to ground through its 50 Ω load, which is far inferior to the other impedances of the TSV system. Once again, by increasing the TSV load values, the crosstalk voltage is raised. We can see from the 1 kΩ and 10 kΩ multi-aggressor results of Fig. 8 that a total voltage crosstalk can easily reach a significant fraction of a volt in practical systems, and that the voltage crosstalk results obtained from 50 Ω load simulations can be highly misleading.

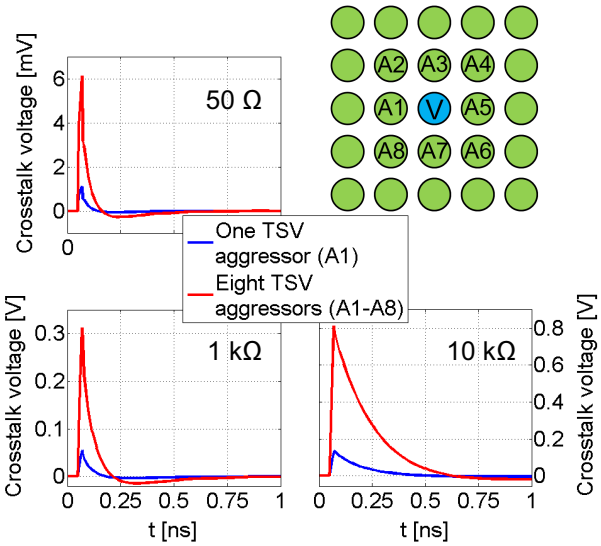

Figure 8. Voltage crosstalk results of the 11x11 TSV array simulation under three general loading conditions: 50 Ω, 1 kΩ and 10 kΩ, with different amounts of in-phase aggressos TSVs. Inset: depiction of the aggressor TSVs (A1-A8) and victim (V) TSVs in the array.

IV. Conclusion

A fast and accurate model capable of simulating substrate volumes with a very large number of nodes was established and validated against full-wave simulation and wideband on-wafer measurements. The model proves to be very powerful, allowing for large-scale analysis and design optimization in both frequency- and time-domain. A large 11x11 TSV array was fully simulated in a short time frame (15 minutes). Negative slope coupling curves were explained to be typical to large TSV arrays. The influence of TSV loading conditions was investigated, showing that conclusions based on the standard 50 Ω terminations can lead to seriously misleading results for the noise coupling coefficient and for the voltage crosstalk, which is anticipated to be as high as a fraction of a volt for worst case in-phase switching scenarios from multiple aggressor TSVs for practical TSV loading conditions.

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