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Extrinsic gate capacitance compact model for UTBB MOSFETs

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Abstract

Ultra-thin body and buried oxide transistors have gained attention as candidates for near future CMOS technology nodes. Recent studies have pointed out that the total parasitic gate capacitance becomes an important concern for very-high frequency performance. In this paper a semi-analytical model to describe the total extrinsic gate capacitance for ultrathin silicon body and buried oxide transistors is presented. The developed model considers the main technological parameters and has been verified by finite-element numerical simulations as well as by comparison with experimental measurements. The relative weight of the main parasitic components is addressed as well as their impact over the current gain cut-off frequency. Finally, the possibility to improve the cut-off frequency by about 35% due to the reduction of the parasitic gate capacitance is highlighted.

Keywords: UTBB, parasitic gate capacitance, modeling, cut-off frequency

(Some figures may appear in colour only in the online journal)

1. Introduction

The microelectronics industry is looking to maintain transistor scaling-down procedures toward the nanometric range. However, the presence of so-called Short-Channel-Effects (SCE) produces several challenges in order to keep device performance as the channel is shrunk. Several technologies have appeared as promising candidates to overcome those limitations [1], including among others, Fully-Depleted SOI (FDSOI) [2, 3], Multiple-Gate (MuGFETs) [3, 4], nanowire [5] and Gate-all-Around transistors (GAA-FETs) [6].

Under this scenario, FDSOI transistors with ultrathin silicon body and buried oxide (UTBB) become an attractive candidate to pursue the CMOS technology towards more Moore nodes [7–11]. UTBB transistors have some technological advantages compared with other solutions for nanometric nodes, such as their planar nature which avoids process complexity associated with the three-dimensional technologies as well as guaranteed CMOS compatibility [2, 11] and negligible threshold voltage and subthreshold slope variability [2, 12–14].

Regarding dc behavior, UTBBs have demonstrated their superior control over the SCE [15–17], the implementation of the ground-plane (GP) beneath the buried oxide (BOX) allows the possibility to tune the transistor threshold voltage [18] and boost the device performance [19].

Furthermore, UTBBs demonstrate outstanding potential for very high frequency analog applications [20–24] and to continue to improve the transistor analog/RF performance [25]. Moreover, it has been shown that analog figure-of-Merit (FoMs) can be affected by self-heating effects [26].

However, very recent results indicate that the parasitic gate capacitance becomes greater than the intrinsic counterpart for devices shorter than ~70 nm [21, 27–29] which degrades the device behavior for analog and RF applications. Therefore, proper modeling of the total gate parasitic capacitance (C_{gge}) becomes of first importance for Technology Computer-Aided Design (TCAD) tools.

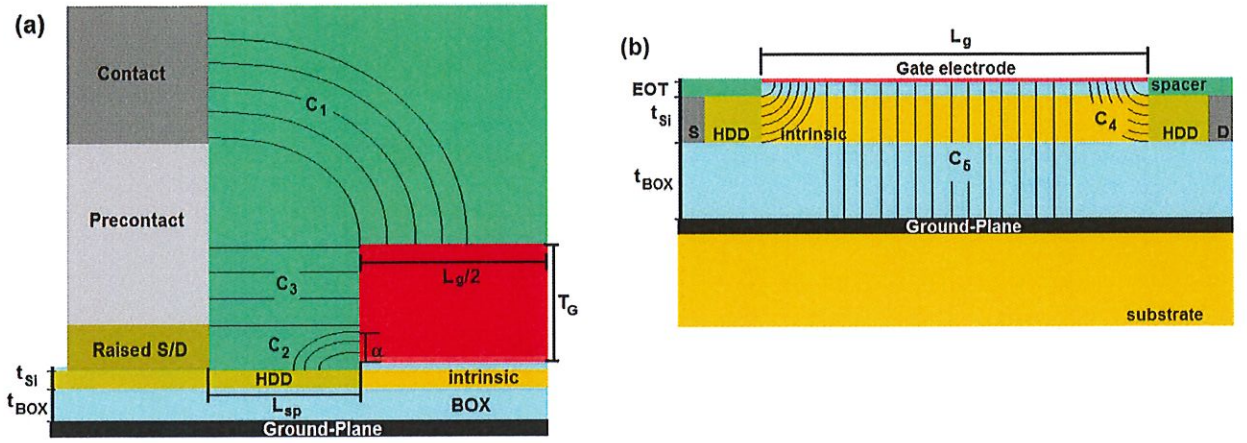


Figure 1. Structures used for extrinsic gate capacitances simulation; (a) external and (b) internal components. The main dimensions are the channel and spacer lengths (L_g and L_{sp}) and the silicon, BOX, gate electrode and equivalent oxide thicknesses (t_{si}, t_{BOX}, T_G and EOT).

Several models have been developed [30–34] with the aim to describe the parasitic gate capacitances for different types of transistor. Some of them model the main parasitic components [35], others describe a number of components in order to develop a general model which can be adapted for a specific device [36, 37]. However, dedicated models for UTBB transistors which describe the effect of the ground-plane, as well as validation with experimental data, are still missing.

In this paper, the impact of the parasitic gate capacitance over the current gain cut-off frequency (f_T) and a semi-analytical C_{gge} model are presented. The model has been validated by comparison with finite-element numerical simulations as well as experimental results.

2. Devices description

Experimental data used for model validation as well as UTBB transistors' description can be found in [29]. Two sets of transistors were used for model validation [29]. The first set consists of devices with different channel lengths and 40 gate fingers of 2 μm width each. The second set consists of transistors with 30 nm length and different finger widths. *S*-parameter measurements at different bias conditions as well as the full small-signal equivalent circuit parameters extraction were previously performed, as explained in [29].

3. Numerical simulations

Two dimensional (2D) ATLAS finite element simulations have been used in order to validate the developed model. Two different structures were considered with the aim to determine both internal and external parasitic capacitance components. Figure 1(a) shows the structure used for external components simulation. It is worth noting that due to the transistor symmetry only half of the device structure is considered. The silicon and silicon oxide beneath the gate electrode were modified with a dielectric constant of 0.001, in order to eliminate the internal capacitance components. As described in [38], the Source/Drain (S/D) electrode is divided in four regions: (i) the heavily drain-doped (HDD) region, (ii) the raised S/D, (iii) the metal precontact and (iv) the metal contact. The gate electrode includes a mid-gap metal electrode and a capping layer of polysilicon or silicide to reduce the gate resistance.

Figure 1(b) shows the structure used for internal components simulation. In this structure, the gate electrode is considered as a plane to avoid the external fringing components. Also, a small spacer region next to the EOT was considered with a dielectric constant of 0.001 with the aim to avoid external fringing components formed between the gate electrode plane and the silicon HDD regions. The schematic of the different capacitance components is also included.

Several sets of simulations considering different values of L_g, L_{sp} and different dielectric constants for the spacers were performed, in order to validate the model for a wide range of geometrical dimensions.

4. Impact on the cut-off frequency

Analog/RF characterization of UTBB transistors is based on the small-signal equivalent circuit model as shown in figure 2 [39]. Based on this model, the current gain cut-off frequency including all parasitic elements is defined as [40]:

$$f_{Te} = \frac{g_{mi}}{2\pi C_{gs}} \cdot \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right) + R_{sd}\left[\frac{C_{gd}}{C_{gs}}(g_{mi} + g_{di}) + g_{di}\right]} \quad (1)$$

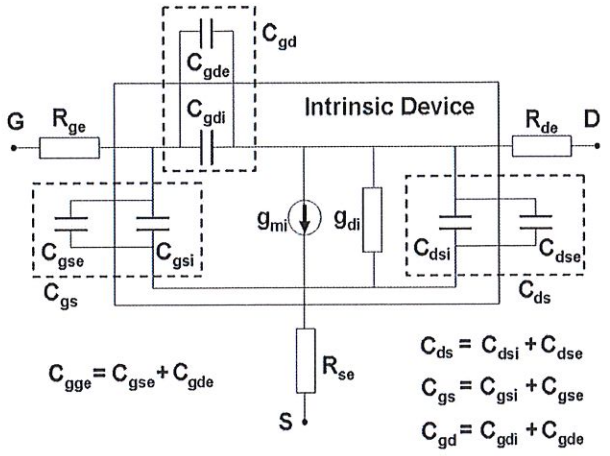


Figure 2. Small-signal equivalent circuit model for UTBB transistors [39].

If the series resistances are removed, the cut-off frequency can be rewritten as:

$$f_{TR} = \frac{g_{mi}}{2\pi C_{gs}} \cdot \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)} \tag{2}$$

Finally, the intrinsic cut-off frequency is obtained after removing both the series resistances and the extrinsic capacitances as:

$$f_{Ti} = \frac{g_{mi}}{2\pi C_{gsi}} \cdot \frac{1}{\left(1 + \frac{C_{gdi}}{C_{gsi}}\right)} \tag{3}$$

Previously in [29], the full equivalent circuit parameters were extracted. Based on those results, the cut-off frequencies, for different channel lengths, were calculated using (1)–(3), as figure 3 shows. In the inset, the comparison between the extracted intrinsic and extrinsic gate capacitances is presented.

As can be observed, the intrinsic cut-off frequency is close to 900 GHz for a 25 nm UTBB transistor. However, for very short channel length devices, C_{gge} becomes greater than C_{ggi}, which leads to strong degradation of the cut-off frequency down to values of approximately 320 GHz. An additional small degradation is attributed to the series resistances, finally giving an achievable cut-off frequency of around 275 GHz.

5. Extrinsic gate capacitance model

As was described in [41–43], it is possible to define four basic capacitance structures: (i) parallel-plates, (ii) perpendicular-plates or (iii) flat-plates non-parallel capacitor and (iv) fringing field capacitive component, as table 1 shows.

Those structures can be used in order to model the total gate capacitance for UTBB transistors, using the components represented in figure 1.

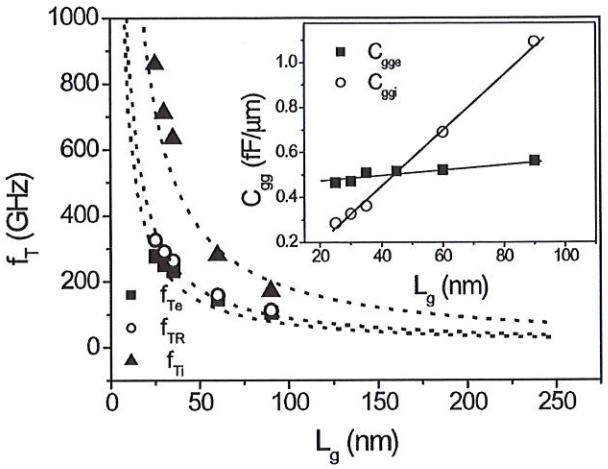


Figure 3. Comparison of the experimentally calculated cut-off frequencies with and without extrinsic parameters. In the inset the comparison between the experimentally extracted intrinsic and extrinsic gate capacitances is shown.

5.1. External components

There are three main parasitic capacitance components as described hereafter (figure 1).

C_1 models the electric field coupling between the top surface of the gate electrode and the lateral side of the S/D electrode and thus corresponds to a perpendicular-plates capacitor. Additionally, C_1 includes the electric field coupling between the top corner of the gate electrode and the lateral side of the S/D electrode like a fringing capacitance. Thus, the width normalized capacitance can be expressed as:

$$C_{1a} = \frac{2k_{sp}\varepsilon_0}{\pi} \ln\left(1 + \frac{\frac{L_g}{2} - \beta_1}{L_{sp}}\right) + \frac{k_{sp}\varepsilon_0}{2\pi} \ln\left(\frac{\pi W}{\sqrt{2}L_{sp}}\right), \tag{4}$$

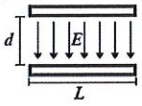
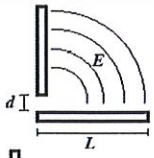
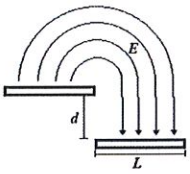
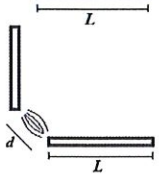
where k_{sp} is the dielectric constant of the spacer material, β_1 is a fitting parameter, and W is the finger width. A constant value of 10^{-4} cm is considered in order to maintain dimensional balance for a width normalized capacitance.

This component exhibits a weak channel length dependence. For very short devices, the perpendicular-plates component increases with L_g until a certain length where its increment becomes negligible and C_1 saturates. On the other hand, the fringing part is channel length independent. Therefore, width normalized C_1 can be expressed as:

$$C_1 = \frac{C_{1a}}{2}\left[1 - \tanh\left(\frac{\frac{L_g}{2} - \gamma_1}{\gamma_2}\right)\right] + \frac{C_{1b}}{2}\left[1 + \tanh\left(\frac{\frac{L_g}{2} - \gamma_1}{\gamma_2}\right)\right], \tag{5}$$

where, γ_1 and C_{1b} are, respectively, the turning point and the corresponding capacitance where C_{1a} becomes almost constant, as figure 4 shows. The hyperbolic tangent function is

Table 1. Basic capacitive structures considered in the model [41–43].

Structure	Equation[a]	Structure	Equation[a]
	(i) $C = k\varepsilon_0 \frac{L}{d}$		(ii) $C = \frac{2k\varepsilon_0}{\pi} \ln\left(1 + \frac{L}{d}\right)$
	(iii) $C = \frac{k\varepsilon_0}{\pi} \ln\left(1 + \frac{L}{d}\right)$		(iv) $C = \frac{k\varepsilon_0}{2\pi} \ln\left(\frac{\pi W}{d}\right)$

[a] L represents the metal length, d represents the distance between metal plates, W represents the metal width and k is the dielectric constant.

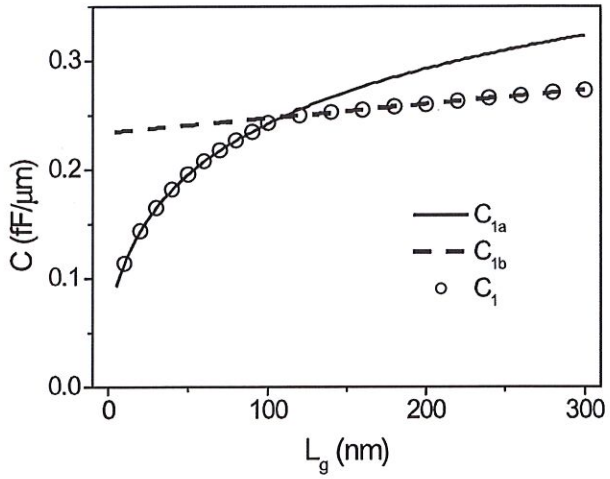


Figure 4. Modeling of the C_1 component. C_{1a} is valid for very short devices, while C_{1b} must be considered for long devices.

Table 2. Summary of the model fitting parameters.

Parameter	Value	Units
γ_1	55×10^{-7}	cm
γ_2	1×10^{-10}	cm
γ_3	17.5×10^{-7}	cm
β_1	$2 \times 10^{-7} + 0.2\ L_{sp}$	cm
α	$-1 \times 10^{-7} + 0.23 L_{sp}$ @ $k_{sp} = 7$ 0 @ $k_{sp} < 7$	cm
C_{1b}	$\frac{k_{sp}}{7}\left[0.12 + 0.25 \exp\left(-\frac{L_{sp}}{1.8 \times 10^{-6}}\right)\right]$ $(4.54 \times 10^{-12} + 25 \times 10^{-9} L_g)$	F
β_2	$\frac{4k_{si}\varepsilon_0}{\pi} \ln\left[1 + \frac{5.1 \times 10^{-7} + 0.3T_{BOX}}{EOT} \sin\left(\frac{\pi k_{ox}}{2k_{si}}\right)\right]$	F

used, in order to fit both dependencies, with γ_2 as a constant value. Table 2 summarizes the fitting parameters.

C_2 corresponds to the electric field coupling between the lateral side of the gate electrode and the top of the S/D HDD region. This component can also be considered as a perpendicular-plates capacitance. The coupling of the bottom corner of the gate electrode and the top of the S/D HDD is included. Thus, the width normalized capacitance can be determined as:

$$C_2 = \frac{2k_{sp}\varepsilon_0}{\pi} \ln\left(1 + \frac{\alpha}{EOT}\right) + \frac{k_{sp}\varepsilon_0}{2\pi} \ln\left(\frac{\pi W}{\sqrt{2} \cdot EOT}\right), \quad (6)$$

where α is the turning point which defines the change from the C_2 and C_3 components as figure 1(a) shows.

C_3 corresponds to the direct coupling between both the gate and S/D electrodes. This component corresponds to a parallel-plates capacitor and its width normalized value can be expressed as:

$$C_3 = k_{sp}\varepsilon_0 \frac{T_G - \alpha}{L_{sp}} \quad (7)$$

Consequently, considering the full transistor structure, the total external capacitance is defined as:

$$C_{ext} = 2 \cdot (C_1 + C_2 + C_3) \quad (8)$$

5.2. Internal components

Under depletion conditions, the channel is not formed and there will be an electric coupling between the bottom of the gate electrode and the S/D HDD region, and along the silicon body. Hence, a two-capacitance component appears, as figure 1(b) shows.

C_4 represents the electric field coupling between the bottom of the gate electrode and the lateral side of the HDD S/D region. This corresponds to a perpendicular-plates capacitance and due to the symmetry observed in figure 1(b) this component is presented twofold. The width normalized component is expressed as:

$$C_4 = 2\frac{2k_{si}\varepsilon_0}{\pi} \ln\left(1 + \frac{\frac{L_g}{2}}{EOT} \sin\left(\frac{\pi k_{ox}}{2k_{si}}\right)\right) \quad (9)$$