High Voltage Gain WSe_2 Complementary Compact Inverter With Buried Gate for Local Doping

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***Abstract*— Two-dimensional (2D) materials such as WSe_2 are potential for advanced electronics because of their ultra-thin geometry and unique electrical properties. Herein, a simplified high-performance WSe_2 complementary inverter based on a buried gate is demonstrated on an individual ambipolar WSe_2 flake, in which both n- and p-type WSe_2 transistors are achieved by local doping. The n-type doping is induced by the donors of benzyl viologen, showing an electron mobility of 28.1 $cm^2/V{\cdot}s$. In contrast, the p-type one is realized by Ozone exposure with a high mobility of 36.8 $cm^2/V{\cdot}s$. The buried gate enables enhanced electrostatic coupling, with a supply voltage (V_{dd}) of 5 V, and the complementary inverter demonstrates a voltage gain beyond 32, almost ideal noise margin approaching 0.5 V_{dd} and low static power consumption. This work paves the way to achieve high-performance 2D material complementary inverters with simplified fabrication process.**

***Index Terms*— Complementary inverter, buried gate, noise margin, voltage gain.**

I. Introduction

With the increase of integration density of integrated circuits, traditional transistors have shrunk continuously and are reaching their physical limit [1]. Owing to their excellent properties [2]–[4], two-dimensional (2D) materials-based semiconductor devices have attracted extensive attention for post-silicon electronics and become promising candidates to extend Moore's law towards large-scale integrated circuit [5]. Among these, some kinds of complementary inverters have been achieved with the development of 2D material transistors research and preparation process, while several crucial challenges still remain. First of all, it is quite difficult to obtain both n- and p-type semiconductor field-effect transistors (FETs) with single 2D material [6]. Meanwhile, the performances of 2D material complementary inverter need to be enhanced, such as the low noise margins, large static power consumption, and low voltage gain below 20 [7]. Furthermore, the complicated fabrication process of 2D material complementary inverters needs to be simplified as well [8].

Complementary inverter fabricated on an individual WSe_2 flake was firstly realized by gas-phase doping with overlapped top-gate device structure via easing the control of the conduction type in WSe_2 [9]. However, the resulting complementary inverter showed relatively low voltage gain because of the absence of rail-to-rail performance. Next, an organic charge transfer molecule doped WSe_2 complementary technology with voltage gain beyond 30 was reported, with multiple electrode depositions of Ag and Pt, which significantly increases the fabrication complexity [8], [10]. More recently, a chemically-doped WSe_2 complementary inverter was demonstrated by large-area chemical vapor deposition (CVD) grown WSe_2 monolayers, the voltage gain property must still be further improved [11]. Hence, it is essential to develop a complementary inverter on an individual WSe_2 flake, which not only offers excellent electrical characteristics, but also uncovers a simple fabrication process.

Herein, a WSe_2-based complementary inverter is demonstrated on an individual flake with a buried gated architecture. Briefly, benzyl viologen (BV) is employed as the surface electron transfer donor and renders n-type doping of the WSe_2 transistors. The hole conductivity is enhanced by exposing the WSe_2 flake in Ozone, which acts as efficient electron acceptor owing to its large redox potential [12]. Moreover, a buried gate with high-k dielectric is employed to improved electrostatic control of the gate [13], also convenient for the surface modulation of WSe_2 channel layer. Through the use of BV and buried gated

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architecture in complementary inverter technology, a simple fabrication process without a multiple electrode deposition or a top gate is developed. The obtained complementary inverters present a high voltage gain beyond 32 with excellent voltage transfer characteristic, full logic swing, and excellent noise margin approaching 0.5 supply voltage (V_{dd}) at a V_{dd} of 5 V. The strategy presented here is desired for the realization of large-scale 2D material electronics circuits.

II. Experimental

The fabrication process of WSe_2 complementary inverters is depicted in Fig. 1(a)-(b). In order to obtain a buried gate structure, two-step photolithography is used to deposit and pattern the gate buried electrode (10 nm/45 nm Cr/Au) and high-k gate dielectric (10 nm HfO_2), on a 300 nm SiO_2 coated p^+-Si substrate by thermal evaporation and atomic layer deposition, respectively. Subsequently, the exfoliated WSe_2 flake was transferred onto the buried structure. WSe_2 transistors are formed by electron beam lithography (EBL), Cr/Au electrodes deposition, and lift-off processes. Then, EBL is used to define the region for local doping of n-type WSe_2 transistor. The WSe_2 transistor was immersed into BV solution [14], followed by 10 nm HfO_2 deposition, as shown in Fig. 1(a). Finally, the WSe_2 transistor was exposed to Ozone for p-type doping (Fig. 1(b)). Note that the HfO_2 coating layer protects the n-type transistor region from Ozone exposure. Consequently, a WSe_2 complementary inverter on an individual WSe_2 flake with a buried gate structure was finalized.

III. Results and Disussion

Fig. 1(c) shows the cross-sectional schematic of the device structure and its top layout view using scanning electron microscope. The n-type transistor is connected to the p-type one on an individual WSe_2 flake with a buried gate structure, in series between the supply and ground voltage rails. Since monolayer WSe_2-based transistors exhibited low channel current and low carrier mobility usually, multi-layered WSe_2 flakes with a thickness of 3 nm were selected as the device channel. The channel length (L) and width (W) of both transistors are 5 μm and 6 μm, respectively. The flake integration with single contact between the n- and p-FETs, gate and symmetrical dimensions makes the inverter design highly compact. The influence of BV treatment time on the transfer characteristics (drain-to-source current (I_{ds}) varies with gate voltage (V_{gs})) of WSe_2 transistors are plotted in Fig. 1(d). Due to the high reduction potential of BV [14], the hole current decreases with immersion time, and the threshold voltage (V_{th}) shifts from -0.75 V to -1.33 V, while the current of the electron-dominated region is slightly enhanced. After immersing into the BV solution for 60 seconds, the current of the electron-dominated region is three orders of magnitude larger than that of the hole-dominated region, leading to a quasi-n-type transistor. Afterwards, the WSe_2 transistors were exposed in Ozone condition for p-type doping, as shown in Fig. 1(e). In contrary to the n-type doping of BV, the ambipolar characteristic has evolved to quasi-p-type with the increase of exposure time, and the V_{th} shifts from -1.62 V to 0.52 V. Meanwhile, Fig. 1(f) presents the output characteristics (I_{ds} varies with drain-to-source voltage (V_{ds})) of WSe_2 FETs with 60 s BV and 20 min Ozone treatment.

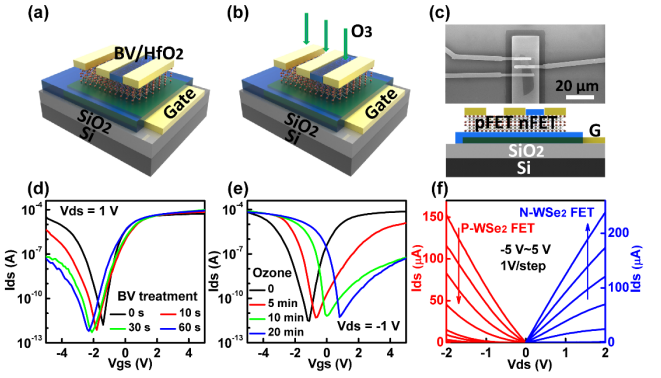

Fig. 1. (a)-(b) The fabrication process of WSe_2 complementary inverters. (c) Scanning electron microscope image and cross-sectional schematic of the WSe_2 complementary inverter (blue parts are HfO_2 and yellow parts are electrodes). (d)-(e) Transfer characteristics of WSe_2 FET with different BV and Ozone treatment times. (f) Output characteristics of WSe_2 FETs with 60 s BV and 20 min Ozone treatment.

The detailed evolutions of the field-effect mobility (μ_{FE}) of the WSe_2 transistors with the treatment time are plotted in Fig. 2(a) and 2(b), μ_{FE} is estimated by the usual equation [15]:

$$\mu_{FE} = \frac{L}{W} \cdot \frac{g_m}{C_i \cdot V_{ds}}$$

where $g_m = dI_{ds}/dV_{gs}$ is the transconductance, C_i is the capacitance per unit area of the 10 nm HfO_2. As a result, the electron-dominated field-effect mobility (μ_n) of the WSe_2 transistors shows no significant change with BV modification, while the hole-dominated one (μ_p) decreases with time. On the other hand, the devices with Ozone exposure present low μ_n as the treatment time increases, as shown in Fig. 2(b) [12]. The electron concentration of the WSe_2 FETs with 0, 10, 30, and 60 s BV treatment are calculated to be 3.8×10^{19}, 4.6×10^{19}, 6.2×10^{19}, and 5.9×10^{19} cm^{-3}, respectively [16]. The hole concentration of the WSe_2 FETs with 0, 5, 10, and 20 min Ozone treatment are 2.9×10^{19}, 3.3×10^{19}, 3.9×10^{19}, 3.7×10^{19} cm^{-3}. Besides, large on-off ratio of 10^8 is achieved, which is excellent compared with the traditional back gate structure and may originate from the enhanced gate coupling of the buried gate [13], [17]. Moreover, the electrical properties of WSe_2 transistors could be stable for at least one week after BV and Ozone treatment. All the results indicate the potential application of WSe_2 for high-performance complementary inventers.

Typical electrical performances of the integrated complementary inverter with different V_{dd} are presented in Fig. 2(c). The inset in Fig. 2(c) is the circuit diagram of the complementary inverter. The voltage transfer characteristics of WSe_2 complementary inverter exhibits excellent inverting performance under V_{dd} value is 3, 4, and 5 V, including full logic swing, sharp switching close to the middle of the voltage range, and symmetrical shape. An important note is that thanks to the balance of the n- and p-transistor I-V behaviors, the input voltage (V_{in}) and output voltage (V_{out}) ranges are identical, and limited from 3 V to 5 V, as required in practical complementary metal-oxide-semiconductor transistor (CMOS) inverters, differently to other publications [6], [7]. The slope of the sharp transition between two logic states yields the voltage gain of the inverter (dV_{out}/dV_{in}) [6]. Fig. 2(d) indicates that

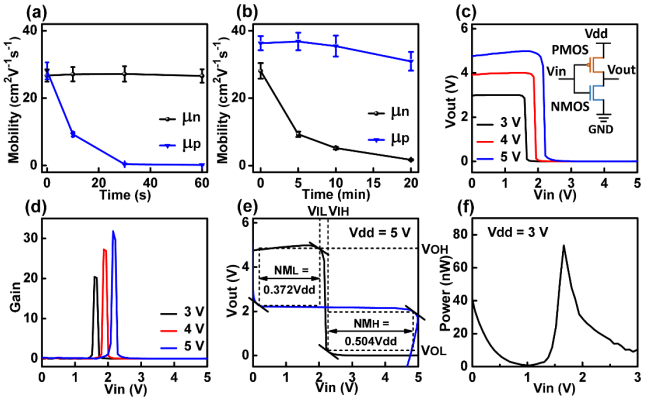

Fig. 2. (a)-(b) Mobility μ_{FE} of n- and p-type WSe_2 FETs with different BV and Ozone treatment time. (c) Voltage transfer characteristic curves of the complementary inverter for supply voltage V_{dd} = 3, 4, and 5 V, respectively. (d) Corresponding voltage gain. (e) Butterfly voltage transfer characteristics highlighting the N_{ML} and N_{MH} for V_{dd} = 5 V. (f) Static power consumption with steps of 60 mV and zero hold/delay times (V_{dd} = 3 V).

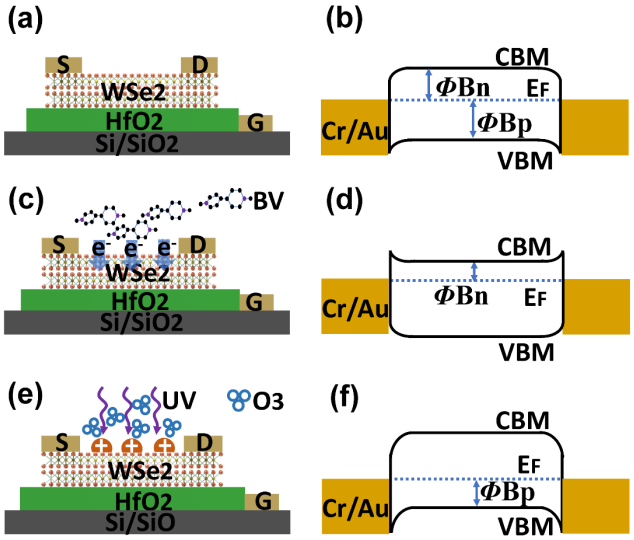

Fig. 3. Schematic image of the WSe_2 FETs and the corresponding equilibrium energy band diagrams: (a)-(b) pristine, (c)-(d) after BV treatment, and (e)-(f) after Ozone exposure, respectively.

the voltage gain increases with increasing V_{dd} as usually expected in CMOS and a voltage gain beyond 32 is achieved when V_{dd} is 5 V.

The noise margins condition the stability of the output voltage logic level against signal interference on the input voltage. The high input voltage (V_{IH}), high output voltage (V_{OH}), low input voltage (V_{IL}), and low output voltage (V_{OL}) are obtained from the slope of voltage transfer curve is -1 [18], and are respectively depicted in Fig. 2(e) with dash lines. The high noise margin N_{MH} and low noise margin N_{ML} are then calculated from $N_{MH} = V_{OH} - V_{IH}$ and $N_{ML} = V_{IL} - V_{OL}$ [6]. By mirroring the voltage transfer characteristics in the so-called butterfly chart, the N_{MH} and N_{ML} are extracted with their values depicted in the Fig. 2(e). The corresponding values are found to be $N_{ML} = 0.372V_{dd}$ and $N_{MH} = 0.504V_{dd}$. An almost ideal noise margin of $0.5V_{dd}$ is hence obtained at a V_{dd} = 5 V. The switching power consumption is another significant figure of merit of the inverter, which is the multiplication by V_{dd} of the current supplied by V_{dd} when measuring the voltage transfer characteristic, here with zero hold and delay times between the V_{in} steps. The power consumption increases with V_{dd} changes from 3 V to 5 V and get a minimum value 73 nW when V_{dd} is 3 V, as shown in Fig. 2(f). The low static power consumption is attributed to the low off-state current and leakage current of both n- and p-type WSe_2 transistors, allowing to low current flow through the complementary inverter.

To further understand the doping effect of BV and Ozone on WSe_2, the energy band qualitative analysis of WSe_2 transistors is performed before and after doping. Schematics of the transistors and equilibrium energy band diagrams of the pristine, BV treated, and Ozone exposed devices are presented in Fig. 3(a)-(b), Fig. 3(c)-(d), and Fig. 3(e)-(f), respectively. In general, the Fermi level (E_F) of the pristine WSe_2 is close to the middle of the band gap and near the work function value of Cr [19]. Since the transfer characteristic of pristine WSe_2 FETs show an n-type tendency, the E_F is rather close to the conduction-band minimum (CBM). Fig. 3(b) shows the schematic image of the band structure between WSe_2 and the Cr contact metal. After coating the WSe_2 FET with BV, which acts as surface charge transfer dopant, the electrons will transfer from BV molecules to WSe_2 and consequently lead to high E_F of WSe_2, as revealed in Fig. 3(d). When E_F rises, the electron injection barrier (ΦB_n) reduces, while the hole injection barrier (ΦB_p) increases. Subsequently, the p-type property of WSe_2 FET is effectively suppressed and the n-type doping is completed.

In the case of p-type doping, Ozone is a strong oxidizing agent and has a higher redox potential (E_{redox}) than the E_F of WSe_2 [13]. Ozone exposure induces a redox reaction on WSe_2 flake: O_3 (aq) + $2H^+$ + $2e^-$ (WSe_2) = O_2 + H_2O, where electrons transfer from WSe_2 to a redox system driven by the difference in E_F and E_{redox}. Thus, electrons are withdrawn from WSe_2 which results in the increase of hole density. Therefore, the E_F of WSe_2 will move close to the valence-band maximum (VBM) and the ΦB_p decreases, which is shown in Fig. 3(f). Opposite to BV doping, Ozone exposure leads to p-type doping and suppresses the n-type property of WSe_2 FET effectively. These band structure analyses strongly suggest that BV and Ozone can be used as an effective strategy to dope WSe_2 FET.

IV. Conclusion

In conclusion, we report a strategy to fabricate high-performance complementary inverter with an individual WSe_2 flake. In order to achieve desirable control over device, a buried gate structure is constructed with high-k dielectric. Then, the complementary doping effect of BV and Ozone on the performance of WSe_2 FETs is systematically studied. Thus, we obtained matched current levels in n-FET and p-FET with high on-off ratio and suitable V_{th}. Finally, compact complementary inverter is assembled on an individual WSe_2 flake. The WSe_2 complementary inverter exhibits large voltage gain beyond 32, almost ideal noise margin approaching $0.5V_{dd}$, and low power consumption. The performance of the simplified 2D material complementary inverter fabrication technology explored in this work could be applied to logic circuit in future.

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