High-Resistivity Substrates in 22-nm FD-SOI—Part I: Wideband Modeling and Impact on RF Losses

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***Abstract*— This article examines how the bulk and interface resistivity of silicon substrates influence the RF performance of devices fabricated in 22-nm fully depleted silicon-on-insulator (FD-SOI) technology. To investigate this, coplanar waveguides (CPWs) were designed and manufactured using GlobalFoundries' 22FDX (Registered trademark) process on a range of substrates, from standard 10-Ωcm silicon wafers to high-resistivity (HR) 620-Ωcm wafers. In addition, various silicon-interface conditions were explored, introducing process variations in interface resistivity alongside changes in bulk resistivity. To achieve high interfacial resistivity, a series of p-n junctions were implemented at the interface, and these are proven to drastically reduce RF losses. From the CPW line measurement data, interface and bulk resistivity values were extracted for all six considered substrate variations. The extraction of these properties enables modeling of the materials present in all substrate stacks and permits electromagnetic (EM) simulations of various RF layouts of various shapes, functions and characteristic dimensions, such as spiral inductors and mm-wave single-pole double-throw (SPDT) switches. Such simulations are shown to correlate well to the measured data using the calibrated material stack description. This work demonstrates the impact of the substrate's bulk and interface properties on the losses and quality of these devices and highlights the necessity for an effective interface passivation technique and appropriate modeling.**

***Index Terms*— Coplanar waveguides (CPWs), fully depleted silicon-on-insulator (FD-SOI) technology, implants, insertion loss (IL), low-loss RF substrate, p-n junctions, RF, RF modeling, RF simulations, substrate engineering, substrate modeling.**

I. Introduction

MODERN advanced CMOS nodes are well-suited for RF and mm-wave applications. In particular, fully depleted (FD) silicon-on-insulator (SOI) devices achieve f_t and f_{max} values between 300 and 400 GHz [1] while offering extensive back-end-of-line (BEOL) integration, including up to 11 metal layers with several thick copper interconnects that enable high-Q RF/mm-wave passives.

The silicon substrate is a key component of the electromagnetic (EM) environment for these passives and devices, but it can introduce significant losses, coupling effects, and nonlinear signal distortion [2], especially when its resistivity is low.

Using high-resistivity (HR) silicon substrates ($\rho_{nom} > 500$ Ωcm) instead of standard-doped silicon ($\rho_{nom} \approx 10$ Ωcm) helps mitigate these effects. However, the benefits are often limited by parasitic surface conduction (PSC), a phenomenon where fixed positive charges at the Si/SiO_2 interface attract free electrons, forming a highly conductive, channel-like layer [3], [4]. This PSC layer reduces the effective resistivity (ρ_{eff}) perceived by coplanar circuitry above the substrate stack, typically lowering it to 30–150 Ωcm [2], [5].

To counteract PSC, various interface passivation techniques have been developed, with the trap-rich approach being the most widely used. This method introduces a defect-rich polysilicon layer between SiO_2 and Si, which traps free carriers and increases interface resistivity [4], [5]. Trap-rich SOI has been highly successful in partially depleted (PD)-SOI nodes, where it is placed between the buried oxide (BOX) and the silicon substrate. However, in fully depleted silicon-on-insulator (FD-SOI), below-BOX features such as back-gate contacts, isolation wells, and diodes pose integration challenges with defect-rich polysilicon, which are envisaged to present significantly increased leakage currents into the substrate when reverse-biased, facilitated by the many recombination centers present when implemented in a trap-rich layer instead of in monocrystalline silicon. These compatibility constraints drive the need for alternative interface passivation techniques.

This article explores a novel p-n-interface passivation approach applied to commercial FD-SOI technology on HR substrates.

Over the past decades, substrate material properties have been widely recognized as being strongly impactful on the quality of RF devices, showcasing improvements brought to passive devices through substrate optimization and engineer-

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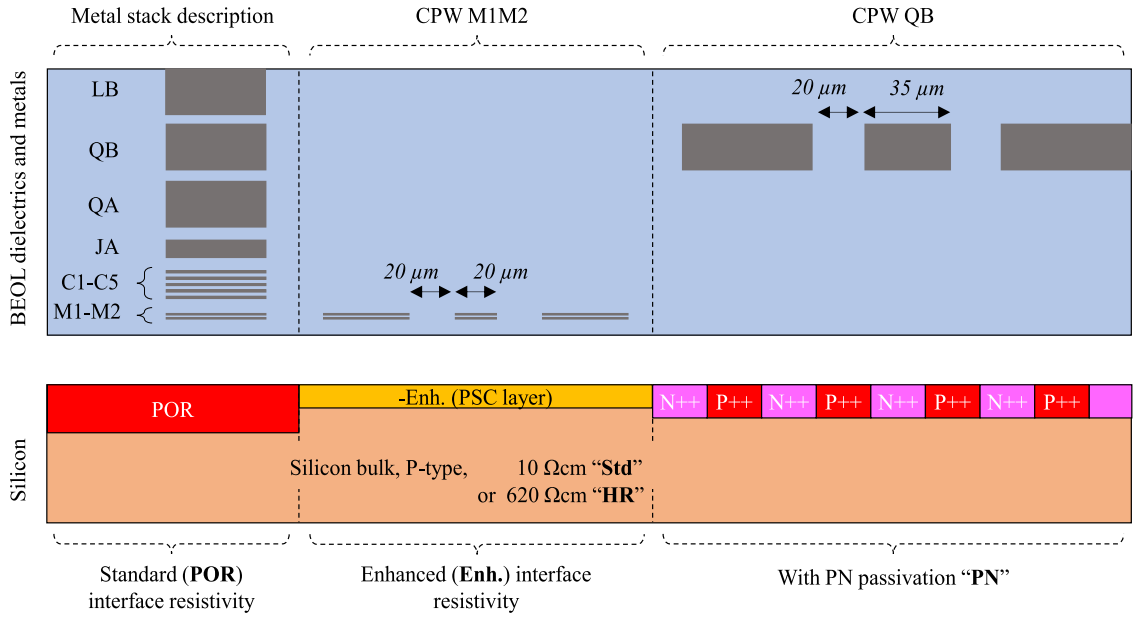

Fig. 1. Depiction of different substrate options (in the bulk and at the interface) and the overlying BEOL metal stack.

ing, such as transmission lines and spiral inductors [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23].

In this study, GlobalFoundries' 22FDX[1] technology was implemented on multiple FD-SOI wafers (p-type) with varying bulk silicon resistivity levels. In addition, three different interface configurations were evaluated: 1) the standard process-of-record (POR) interface, 2) an "enhanced" interface, and 3) a p-n-interface passivation technique.

The concept of the p-n-junction substrate, originally introduced in [20], involves alternating p- and n-type doping regions to disrupt the otherwise conductive interface caused by the PSC effect. These induced depletion junctions form a chain-like series, significantly increasing the overall substrate impedance (ρ_{eff}) perceived by overlying coplanar circuits (see Fig. 1). Since depletion regions are inherently highly resistive, they effectively break the conductive sheet at the Si/SiO_2 interface, thereby enhancing the interface's effective sheet resistivity.

The physical dimensions of the alternating P- and N-implanted regions impact on the RF substrate performance, and in [20] this was studied through prototypes in a research cleanroom with lithography capabilities down to 1 μm. Building on that, the p-n passivation technique was run on 300-mm wafers for the first time with lithography down to 300 nm in [21]. The p-n passivation was first applied to a full CMOS industrial process as part of this work, and the impact on passive components' losses and quality factors has already been reported in [22] and [23].

Beyond that, this article focuses deeply on *accuratemodeling and simulation* of the electrical properties of different layers in the considered substrates.

This article is organized as follows.

First, Section II describes the different substrate variations that were considered and fabricated for this work.

Next, in Section III, the substrate's effective material properties are extracted close to the Si/SiO_2 interface using coplanar waveguide (CPW) lines implemented in the lowest level metals (stacked M1 and M2). These lines enable us to extract ρ_{eff} values that are sensed by low-level interconnects close to the FETs for different substrate options. The effective substrate parameters sensed by higher level passives are also extracted, using CPWs designed in one of the last metal layers (QB). The measurements from these CPW devices enable us to extract a calibrated material-stack build-up of the substrate that can then be used for accurate EM simulations of various structures on different wafers.

Finally, in Section IV, this article uses those calibrated material stack model descriptions to study the loss and coupling effects observed in other RF devices, namely, 1) spiral inductors and 2) mm-wave single-pole double-throw (SPDT) switches. These devices serve to validate the accuracy of the extracted material stack electrical descriptions, as the simulated data using these models fit well to the measured data, accounting for the full layout of the RF test structures (inductors and SPDT designs).

II. 22FDX Substrate Variations

Fig. 1 illustrates the six substrate variations used for fabricating the CPW lines and other RF devices in this study.

Three different configurations were explored at the Si/SiO_2 interface.

1) *Process of Record ("POR"):* This is the standard interface option in the 22FDX process, where the interface resistivity is defined by specific implant steps in the reference manufacturing process. In the 22FDX technology, this interface is achieved using the "BFMOAT" mask layer. The interface resistivity is determined by implanted impurities rather than by parasitic oxide charges.

[1]Registered trademark.

2) *Enhanced ("Enh."):* This variant involves process optimizations to reduce interface conductivity compared with the POR case by omitting those specific implant steps. In that case, PSC induced by parasitic oxide charge determines the interface resistivity.

3) *p-n Passivation ("p-n" and "PN3V"):* In this approach, the enhanced process steps are applied instead of the POR, and additional p++ and n++ doped regions are introduced in an alternating pattern beneath the RF devices. These regions are created through implantation steps, and on-chip interconnects to each p and n region are included to allow dc biasing of the p-n junctions. This configuration is labeled "p-n" when no dc bias is applied and "PN3V" when a reverse bias of 3 V is applied to the p-n junctions.

Each p and n region is dc biased in practice through high-value polysilicon resistors integrated on-chip. Applying a reverse bias to the p-n junctions expands the depletion regions, which play a key role in determining the sheet impedance. As a result, increasing the depletion width effectively raises the sheet resistivity at the interface [23].

All three interface configurations described above were implemented and fabricated on two types of base wafers within the 22FDX process.

1) *Standard Resistivity ("Std"):* bulk silicon with a resistivity of approximately 10 Ωcm, currently part of the standard 22FDX process.

2) *High Resistivity*: using this option, the bulk silicon has a resistivity in the range of 620 Ωcm. This substrate will be labeled as "HR" from here on. These wafers are experimental in the 22FDX line.

III. Characterization and Extraction Using CPW Lines

A. CPW Line Variations

Fig. 1 illustrates the metallic layers in the BEOL of the fabricated chip used in this study. The stack consists of seven thin copper layers (M1, M2, and C1–C5) with thicknesses around 100 nm. Above these, a 1-μm-thick copper JA layer is followed by two thicker copper layers, QA and QB, each 3-μm-thick. The stack is completed with a 2.9-μm-thick aluminum LB layer.

A set of CPW lines were fabricated in the thick high-level metal QB to demonstrate the typical low-loss performance achievable across different substrates in this technology. To achieve a characteristic impedance (Z_c) of 50 Ω, the central signal linewidth (W_c) was set to 35 μm, with a 20-μm spacing (S) to the outer ground lines.

A second set of CPW lines was designed in a stacked combination of M1 and M2. To achieve Z_c of 50 Ω, W_c was set to 20 μm, and S to 20 μm. These CPW lines are quite lossy due to the thin metals used; however, by being closer to the silicon substrate, they have inherently higher sensitivity to various substrate options considered and will serve to extract accurate effective substrate properties close to the Si/SiO_2 interface. Those metrics will be analyzed and will also be of further use in Section IV-A to demonstrate the accurate modeling of the substrate's impact on the performance of the mm-wave SPDT switches.

B. On-Wafer Measurements and Extractions of CPWs

On-chip measurements were carried out on the fabricated CPW lines up to 67 GHz using 100-μm-pitch GSG probes from FormFactor, along with a Keysight PNA-X analyzer.

For both sets of CPWs (in QB and in M1M2), lines of two different lengths were measured (760 and 2000 μm) along with dedicated thru (290 μm of total length) and open structures.

Following the extraction procedure described in [24], the pad parasitics are deembedded and an mTRL approach is applied to extract the properties of the uniform line, such as the real and imaginary parts of both the propagation constant and the characteristic impedance, ultimately leading to the evaluation of the equivalent lineic RLGC parameters.

Following that extraction, the CPW lines on various substrates are compared in terms of lineic losses (α) and substrate effective resistivity (ρ_{eff}). The latter is computed from the lineic G parameter, thanks to a conformal mapping technique of CPW geometry [25], as detailed in [24].

C. Substrate Impact on CPW Lines in QB

Fig. 2(a) shows plots of the extracted results obtained from the measurements of the QB CPW lines. The substrate impact on the overall performance of the CPW line is highlighted.

A loss of 1.00 dB/mm at 30 GHz is observed on the Std-POR substrate.

It is demonstrated that this loss can already be substantially reduced by including the enhancement process of the interface resistivity compared with the POR reference process, with the same CPW on the Std-Enh wafer exhibiting 0.75 dB/mm of loss at 30 GHz. This reduction is explained by higher effective resistivity sensed by the line (i.e., lower lineic G parameter), which is increased from 35 to 47 Ωcm due to less conductive interface.

The same lines implemented on the HR-POR substrate present losses of 0.54 dB/mm at 30 GHz. Compared with the reference Std-POR sample, a 0.46-dB/mm improvement in loss is achieved by solely modifying the base resistivity of the wafer, which translates into an effective resistivity increase from 35 to 78 Ωcm at 30 GHz. This loss is reduced furtherusing the enhanced-interface process option, with the lines on the HR-Enh substrate exhibiting lineic losses of 0.25 dB/mm for a ρ_{eff} value of 196 Ωcm at 30 GHz.

Then, in that case, a PSC effect present at the Si/SiO_2 interface becomes the dominating effect determining the interface resistivity and the overall value of the lineic G term of the line.

This interface resistivity can be increased further and rendered significantly higher valued through the addition of p-n junction interface passivation. This is demonstrated through the measured results of the HR-PN substrate, which presents further reduced line loss of only 0.18 dB/mm at 30 GHz.

Note that a frequency dependence is present in the measured G and ρ_{eff} data. This tendency is anticipated due to the series combination of conductive doped regions (n or p) with capacitive depletion regions [20], which results in an effective interface impedance that decreases as frequency increases.

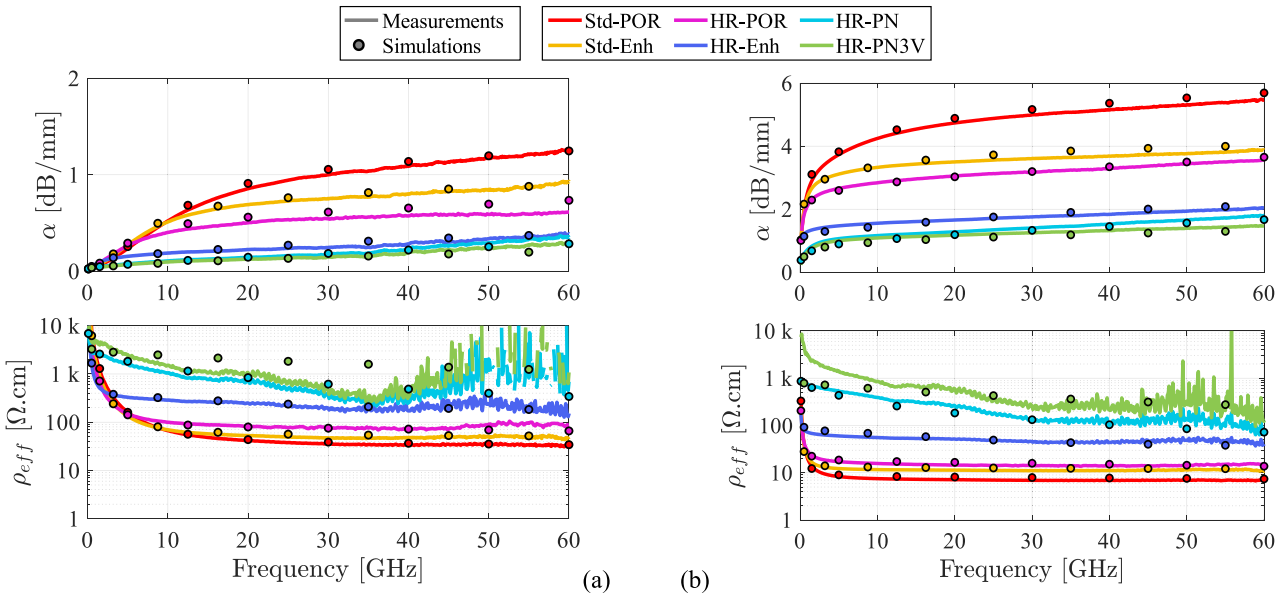

Fig. 2. Line losses (α) and effective resistivity (ρ_{eff}) from the measured CPW lines on different considered substrate options for (a) QB lines and (b) M1M2 lines.

TABLE I
MEASURED EFFECTIVE RESISTIVITY AND LINE LOSS AT 30 GHZ

At 30 GHz	CPW M1M2		CPW QB	
	ρ_{eff} [Ωcm]	α [dB/mm]	ρ_{eff} [Ωcm]	α [dB/mm]
Std-POR	6.9	5.01	35	1.00
Std-Enh	11.1	3.62	47	0.75
HR-POR	14.2	3.18	78	0.54
HR-Enh	45.9	1.76	196	0.25
HR-PN	124	1.40	360	0.18
HR-PN3V	266	1.25	457	0.15
Lossless sub sim: $\rho_{\text{intf}} = \rho_{\text{bulk}} = \infty$	∞	1.06	∞	0.13

By applying a reverse bias to the p-n junctions, the depletion regions can be expanded in space. This leads to an increase in interface impedance and to a further reduction in the line loss, as is demonstrated by the measured data pertaining to the HR-PN3V substrate option. The measured lines in that case are identical to the HR-pn lines, with the addition of a reverse 3-V biasing being applied to the p-n junction patterns.

Overall, the QB CPW lines on the HR-PN and HR-PN3V samples achieve effective resistivity values of around 360 and 457 Ωcm at 30 GHz and associated line losses of 0.18 and 0.15 dB/mm, respectively. Simulated data results are in good agreement with the observed measurements (modeling is discussed in detail further on) and serve to reveal that 0.13 dB/mm of the line losses at 30 GHz are due to finite metal conductivity of the QB layer (see the lossless substrate simulation data in Table I). This, in turn, indicates that the substrate-loss contribution to the total line loss for the HR-PN3V sample is very low, at only approximately 0.02 dB/mm, confirming that overall excellent substrate passivation is achieved.

D. Substrate Impact on CPW Lines in M1M2

Similar observations are observed when comparing the measurement data pertaining to the M1M2 CPW lines, which are plotted in Fig. 2(b).

At 30 GHz, the lines on the Std-POR substrate present lineic losses of 5.01 dB/mm. This high value is due to a low effective resistivity of 6.9 Ωcm (due to the close vertical proximity of the CPW to the silicon substrate), which is determined by a combination low interface resistivity (ρ_{intf}) and low bulk resistivity (ρ_{bulk}).

Solely increasing ρ_{intf} only improves the sensed ρ_{eff} to 11.1 Ωcm, as demonstrated by the Std-Enh data, and the lineic line losses at 30 GHz retain a high value (3.62 dB/mm at 30 GHz).

Similarly, only increasing ρ_{bulk} weakly improves the sensed ρ_{eff} to 14.2 Ωcm, as demonstrated by the HR-POR data, and the lineic losses retain a high value 3.18 dB/mm at 30 GHz.

Those observations are recapped in Table I at 30 GHz.

The effective resistivity is increased to 45.9 Ωcm on the HR-Enh sample at 30 GHz. In that case, the bulk loss is very low, and the interface loss is improved, though is still the dominating factor in the substrate loss on that sample (due to a PSC effect in that case).

By passivating that interface further using the p-n junction technique, the M1M2 CPW lines on the HR-PN and HR-PN3V samples achieve ρ_{eff} values of 124 and 266 Ωcm at 30 GHz for line losses of 1.40 and 1.25 dB/mm, respectively (and 1.06 dB/mm of that is associated with metallic losses in the M1M2 stacked lines).

We note that the bump in $\rho_{\text{eff}}(f)$ around 50 GHz (that occurs for the low-loss substrates, both in the QB and M1M2 lines) is nonphysical and is caused by a mispartitioning of total losses α among metallic resistive (R) and substrate-related losses (G) [23]. This effect becomes prominent for the low-loss substrates, as the measured G term becomes low in absolute value. Because of that, small errors in the extraction

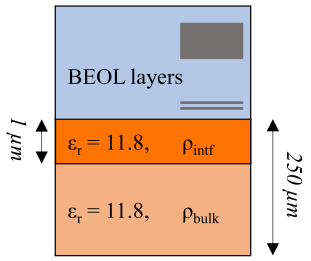

Fig. 3. Material stack description of EM simulation fitting.

procedure have a large relative impact on such low G (and hence high ρ_{eff}) values. This bump in the measurements is attributed to some probe coupling to the chip environment and is only partially corrected by the applied deembedding and mTRL extraction procedure [24].

E. Extraction of the Material Parameters of the Substrate Stacks Through Simulation Fitting

The simulation results are superimposed on the measurement data of Fig. 2(a) and (b). These were obtained from EM simulations of CPW lines in the 22FDX BEOL, run on several material stacks representing different silicon substrate options. The different stacks considered all model the silicon volume as being made up of two uniform layers, the first being defined as 1 μm in thickness with a resistivity ρ_{intf}, and the second being 250-μm-thick with a resistivity ρ_{bulk}. This is schematically depicted in Fig. 3. From the measured data of both the sets of CPW lines on different samples, excellent fitting was achieved by considering bulk resistivities ρ_{bulk} of 14 and 620 Ωcm for the Std and HR wafers, respectively, along with interface resistivities ρ_{intf} of 0.9 and 4.5 Ωcm for the -POR and -Enh (PSC) interface processes, respectively.

For the p-n-types of interfaces, excellent fitting was achieved by modeling ρ_{intf} as inversely proportional to frequency, having a value of 20 Ωcm at 30 GHz when unbiased, and of 150 Ωcm at 30 GHz when reverse-biased to 3 V. This is equivalent to modeling those layers as lossy dielectrics, with $\tan\delta$ values of $2.54{\cdot}10^{-1}$ and $3.39{\cdot}10^{-2}$ for the p-n and PN3V interfaces, respectively.

Since the p-n interface is made up of a series combination of capacitive (the depletion regions) and resistive (the p and n regions) elements, the overall interface impedance is frequency-dependent. At low frequency, the effective interface impedance is very high; however, as frequency increases, the capacitors become more and more transparent, and the interface impedance decreases to effective values of 20 and 150 Ωcm at 30 GHz, respectively, for the p-n and PN3V cases. These values are still one to two orders of magnitude higher than for the unpassivated Enh. or POR interfaces and present a significant enhancement still at 30 GHz.

Each substrate shows excellent model to hardware correlation for CPW lines designed in different metal layers, as demonstrated by the fitting in Fig. 2(a) for the QB lines, and by the fitting in Fig. 2(b) for the M1M2 lines.

Note that the fitting of bulk and interface parameters was not performed independently for each measurement trace. Instead, the four interface resistivity parameters and two bulk resistivity parameters are determined by the best overall fit for the 12 measurement curves of Fig. 2. Overall, the quality of the achieved fitting over two sets of CPW devices and bulk and interface conditions gives strong confidence in the equivalent substrate stacks extracted from these data, whose properties have been recapped in Table II. These equivalent and fit substrate models will be of use in the next section, helping to analyze substrate impact on the significantly different devices and layouts.

TABLE II
ELECTRICAL PROPERTIES OF THE SIMULATION MATERIAL STACKS

	ρ_{bulk} [Ωcm]	ρ_{intf} [Ωcm]
Std-POR	14	0.9
Std-Enh	14	4.5
HR-POR	620	0.9
HR-Enh	620	4.5
HR-PN	620	20·(30 GHz)/f
HR-PN3V	620	150·(30 GHz)/f

Where f is the frequency.

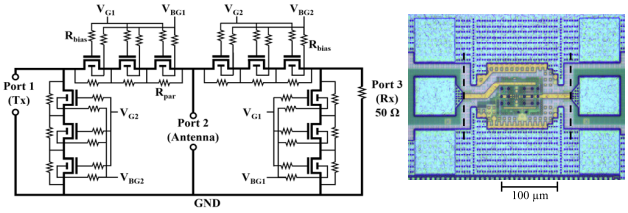

Fig. 4. Schematic and layout photograph of the fabricated mm-wave SPDT.

IV. VALIDATION USING OTHER RF DEVICES

In this section, we showcase the impact of the substrate on the performance of other RF devices, such as a spiral inductor and an mm-wave SPDT switch. These demonstrate that the equivalent material substrate stacks extracted in the previous section are capable of accurately modeling the substrate impact on devices and layouts of significantly different characteristic dimensions and shapes than the CPW lines used to calibrate and develop those model stacks.

Detailed analysis of the substrate's coupling and loss mechanisms in the SPDT switch layout is provided in the second paper of this series [26], though the main high-level takeaways are summarized in this section to highlight the use of the substrate stack models.

A. SPDT Switches

An mm-wave SPDT switch was designed and fabricated on the same wafer variations as the CPW lines in 22FDX. A conventional series-shunt topology is implemented to achieve wideband dc 40-GHz performance. Fig. 4 depicts the switch layout and circuit diagram, and each series branch and shunt branch of the switch are implemented using three stacked FETs to achieve a $P_{1\text{dB}}$ close to 20 dBm. The FETs are sized targeting the lowest possible insertion loss (IL) under the condition of maintaining better than 20-dB ISO over the considered dc to the 40-GHz band. The full SPDT design and all chosen parameters are detailed in Part-II [26].

The SPDT switch implemented on each of the substrates is both measured and simulated fully with the reference planes

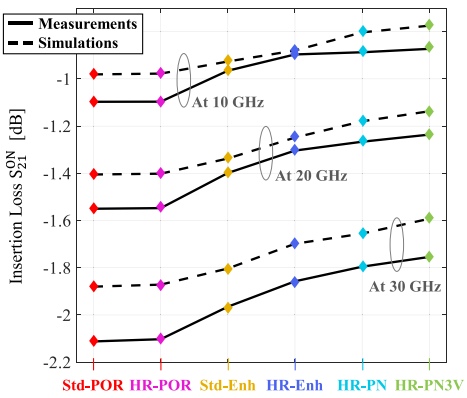

Fig. 5. Measured and simulated SPDT ILs (open deembedded) on different substrate options.

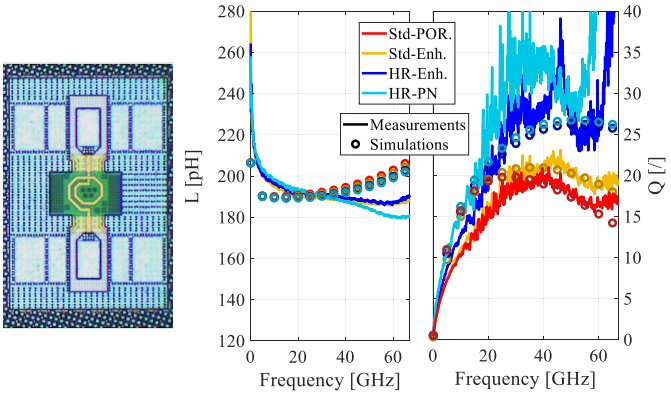

Fig. 6. Photograph and extracted parameters of a standalone two-port inductor.

set on the GSG probe pads. Ports 1 and 2 can be contacted with GSG probes while Port 3 is implemented on-wafer using an integrated precision 50-Ω load. An open-pad deembedding procedure is applied to both the measurements and simulations of the full SPDTs, by which the Y-matrix of a measured (simulated) open-pad structure is subtracted from the Y-matrix of the measured (simulated) full SPDT.

The switch IL performance results after open deembedding are plotted in Fig. 5 on various substrate options.

Fig. 5 demonstrates the substrate's impact on the overall loss of the switch module. By simultaneously enhancing the interface properties and increasing the bulk resistivity, the IL at 30 GHz is improved by around 0.35 dB from 2.11 dB (reference Std-POR substrate) to 1.76 dB (HR-PN3V sample).

The trends of the simulation data fit well to the measured results, as demonstrated in Fig. 5 over frequency. Quantitatively, the simulations have around 0.07/0.10/0.20 dB lower IL than the measured data at 10/20/30 GHz. This remains an accurate model to hardware correlation, and in particular the substrate's impact on the IL is well-captured. That is demonstrated in Fig. 5 which highlights that that impact—which is around 0.20/0.26/0.35 dB at 10/20/30 GHz—is well-modeled by the simulation approach (using the material stacks developed and calibrated in Section III-C) and can then be explored further based on the EM simulation files. Such analysis is performed in the second part of this work in [26], which presents the full simulation methodology for the SPDT switch on different substrate options, along with an in-depth analysis of the parasitic substrate impedances at each node to determine the main substrate paths contributing to the change in switch IL performance.

B. Spiral Inductors

A standalone two-port inductor device was also fabricated and measured on the same HR substrate variant and is depicted in Fig. 6. It is a 1.5-turn spiral inductor (190 pH) implemented in the topmost copper metal layer QB of the technology.

The inductor's measurements were performed on all wafers and deembedded using dedicated open and short structures. The self-inductance and overall quality factor values were extracted from the two-port data from the Y_{11} parameter, and the results are plotted in Fig. 6. The data demonstrate an appreciable increase in the inductor quality factor on the high-resistivity substrate option with interface passivation HR-pn, achieving a peak Q value above 30, compared with a peak Q value of around 19.5 on the reference Std-POR sample, with little impact on the self-inductor value.

Such improvement in inductor Q value is associated with reduced loss and coupling through the semiconductor substrate, provided by the enhancements of both the bulk and interface resistive properties. The modeling data of Fig. 6 fit well to the two sets of measured results and are obtained through full EM simulations of the inductor layout run on the extracted and calibrated substrate stacks from Section III (Fig. 3 and Table II). The good agreement for these significantly different layouts to the CPW lines that served to calibrate the substrate stacks provides additional validation to those extracted material descriptions.

V. Conclusion

In this work, GlobalFoundries's 22FDX process was run on several types of p-type FD-SOI wafers, from the conventional 10-Ωcm wafer to 620-Ωcm HR wafers. Beyond that, several silicon-interface conditions were explored, with specialized interface engineering efforts being made to ensure a highly resistive interface region to complement the introduction of resistive silicon wafers. This was achieved by implementing chain series of p-n junctions at the BOX–Si substrate interface, and these were proven through on-wafer RF measurements of CPW lines to dramatically reduce the loss. This passivation technique provides a significant increase in effective sheet impedance at that interface, when compared with unpassivated interface suffering from a PSC effect. The loss of a CPW line implemented in the topmost copper layer (QB) was demonstrated to decrease from 1.0 to 0.15 dB/mm at 30 GHz by simultaneously enhancing the substrate and interface resistive properties when compared with the materials available in the reference POR process of 22FDX.

Beyond demonstrating such improved RF performance results, this article proposes an extraction of effective material parameters of a model-substrate stack allowing for accurate simulations of various layouts of different geometries, sizes, and characteristic dimensions. This extraction was achieved by fitting a multilayered substrate description model to dedicated measurements from several geome-

tries of CPW line structures through EM simulations. This enabled the quantitative evaluation of the interfacial resistivity in all considered silicon substrates, which include several novel interface enhancing options, such as p-n junction passivation.

EM simulations were performed based on significantly different geometries of RF structures based on those material model descriptions of different fabricated substrate variants to validate the approach, including a spiral inductor and a full layout of a mm-wave SPDT switch. Overall, the model simulations (extracted and calibrated using several sets of CPW data) provide good correlation to measured devices.

It is shown through measurement data of fabricated switch devices on these substrate variants that the IL is improved by 0.35 dB at 30 GHz when using an optimized HR silicon with an effective interface passivation scheme compared with the reference POR process.

Having those models then provides the opportunity to extensively and quantitatively analyze (via EM simulations of portions of the layout or carefully selected variations in the material stack parameters) that impact on the switch layout's loss and coupling mechanisms. That study is continued in the second paper of this series [26] that extracts and analyzes equivalent impedance substrate paths in the switch layout, shedding light on the critical regions affecting switch RF performance metrics.

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