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Electrical characterization of true Silicon-On-Nothing MOSFETs fabricated by Si layer transfer over a pre-etched cavity

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Abstract

In this paper, “true” Silicon-On-Nothing (SON) MOSFETs fabricated by a new technique, consisting in Si layer transfer over a pre-etched cavity, are investigated. The process has no potential limitation with regards to the device dimensions as well as to the thicknesses of Si film and so-called “nothing” layers. Comparing to single-gate (SG) fully-depleted (FD) SOI MOSFETs fabricated on the same wafer, improved electrical characteristics of SON MOSFETs are demonstrated. Self-heating effect, which can be considered as the main drawback of SON devices, is experimentally addressed for the first time. Finally, the source-to-drain coupling through the substrate is demonstrated to be practically suppressed in such device architecture.

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1. Introduction

Silicon-On-Nothing (SON) MOSFETs are widely discussed as a possible alternative scalable solution to satisfy the ITRS Roadmap requirements [1–7]. Among the advantages of SON architecture, comparing to fully-depleted (FD) SOI, the major is the reduced source-to-drain coupling through the buried oxide (BOX), which becomes pre-occupant when Si film thinning is considered to suppress short-channel effects. Reduced coupling through the BOX allows in turn to reduce the minimal channel length of transistors or to relax the requirements on Si film thickness [6]. Moreover, since the so-called “nothing” (or air) layer embedded below the Si active film has lower dielectric permittivity than oxide, the parasitic capacitances between source/drain and substrate are reduced and therefore

higher circuit speed can be expected with SON devices. Furthermore, SON approach is imagined to be very promising to improve the total-dose radiation hardness. Thick buried oxide is indeed widely considered as a main drawback of SOI MOSFETs for the rad-hard applications, due to large positive charge accumulated in the thick BOX, while in the case of SON MOSFETs, no charge will accumulate in the air-gap. Finally, the SON architecture appears compatible with perspectives for 3D wafer-level integration.

Different technological solutions to fabricate SON MOSFETs have been invented. The first and more developed nowadays is the Silicon-On-Nothing process from ST-Microelectronics [2], for which, however, the name is related to the process and not to the final device structure itself. This creates a number of confusions, since the advantages and disadvantages of this process are then erroneously attributed to the SON structure in general. In the “ST-SON” process, the thin tunnel is formed under channel only (and not under source and drain regions) and is

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further filled by oxide [2] or oxide–nitride–oxide combination [3,5]. Therefore, numbers of SOI advantages related to the full dielectric isolation are lost, which is not the case of our true SON structure. From another side, the thin BOX under Si film explains the reduced self-heating effect (SHE) in “ST-SON” [2], which can be wrongly attributed to SON structure in general, contrarily to reality, as we will show. Another process, ESS (Empty Space in Si) based on Si surface atoms rearrangement under hydrogen annealing was introduced by Toshiba [4,8]. Good crystalline quality of SON layer comparable to the bulk one and no detectable stress in these devices have been reported [4]. However, limitations of this process with regards to eligible device dimensions and layers thicknesses were not discussed. Lastly, SON created by Silicon-On-Void (SOV) process, in which a layer of voids is formed by H^+/He^+ co-implantation, followed by nitrogen annealing, was proposed by Chinese Institute of Microelectronics [7]. While the functionality of 50 nm SON MOSFET fabricated using this process has been demonstrated, the regularity and uniformity of “voids” layer, have not been addressed yet. Moreover, similarly to ESS process, Silicon-On-Void approach seems to be limited in achievable device dimensions and thicknesses of Si and “nothing” layers.

In this paper, we present Silicon-On-Nothing devices fabricated by a new, alternative approach based on the wafer bonding of a thin Si layer over a pre-etched cavity. This approach thus appears simpler than above-cited ESS and SOV-based processes, more flexible with regards to the feasibility of a large range of layers thicknesses and finally more controllable or reproducible. This method was previously exploited to fabricate planar double-gate (DG) MOSFETs [9]. Using this approach for the fabrication of true SON MOSFETs appears to be more relaxed with regards to device dimensions and process requirements (alignments, polySi doping, W/L ratio, etc.) than when it is applied for DG MOSFETs. The resulting SON MOSFETs demonstrate to over-perform single-gate (SG) FD SOI MOSFETs created on the same wafer and approach the counterpart DG MOSFETs. The enhanced

self-heating effect, which can be considered as a main drawback of true SON devices, due to their poorer heat evacuation comparing to SG FD SOI, is experimentally evidenced, for the first time. On another side, the output conductance degradation caused by the source-to-drain coupling through the substrate [10,11] is demonstrated to be almost ruled out in SON devices.

2. Device fabrication

The principle of the present process lies in the transfer of a high quality thin silicon film (e.g., from a SOI wafer), by direct wafer bonding, over an array of cavities pre-etched into an oxidized silicon bulk wafer. The cavities are defined by a special mask designed to coincide with the final device channel region. The process flow is schematically presented in Fig. 1 and more details can be found in [9]. The device fabrication is initiated with two wafers: (1) a standard SOI UNIBOND wafer and (2) an oxidized Si-bulk handle wafer with predefined cavities (using SF_6 RIE etch). A flipped SOI wafer is bonded to the handle wafer. Then, Si substrate and BOX (of the flipped SOI) are removed by grinding and subsequent etch in TMAH and HF. The obtained structure with Si film over the BOX with cavities can proceed with a standard FD SOI CMOS process [12] in which active area and gate definitions are to be aligned with alignment marks realized as cavities in the initial handle wafer. It is to note that considering the thickness of the transferred Si layer (~ 100 nm here) the marks can be imaged through this film.

It is worth to point out here, that the alignment issue, which is very important when this process is used to fabricate DG MOSFETs, is not a major one in the case of SON MOSFET. Indeed, the SON MOSFET cavity can be extended under source and drain regions and even further, which rules out the misalignment problem between gate, channel and cavity and, moreover, eases the application of this approach to sub-micron devices.

The final structure is schematically presented in Fig. 2. A specific issue is that for SON MOSFET fabrication, the

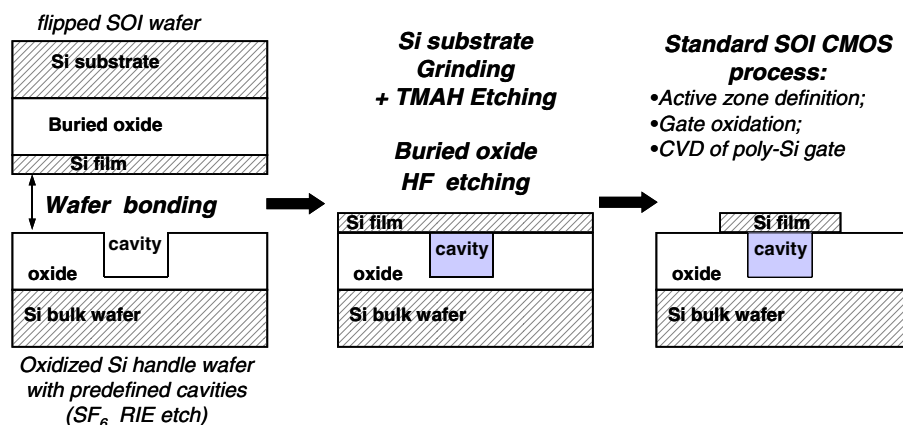


Fig. 1. Schematic illustration of the process flow.

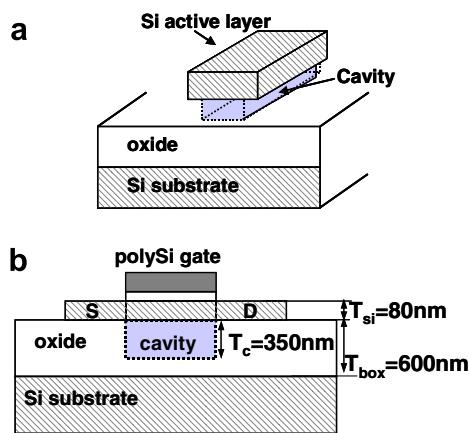


Fig. 2. (a) 3-D view of the SON structure and (b) longitudinal cross-section of the final SON MOSFET.

cavity must be slightly narrower than the transistor width to keep it closed during processing. Gate oxide, Si film and BOX thicknesses are 30, 80 and 600 nm, respectively. The cavity depth in our SON devices is 350 nm, i.e., not corresponding to whole buried dielectric thickness. However, it is worth to mention that this process is principally rather flexible with regards to the thicknesses of Si film and “nothing” layer as well as to device dimensions and relaxed to alignment issues. Moreover, it is compatible with 3D integration (of e.g., special buried dielectrics or interconnects) contrarily to other above-mentioned SON processes.

SG FD SOI MOSFETs were designed on the same wafer for sake of comparison. MOSFETs with different W/L ratios and different doping levels have been fabricated.

3. Electrical characterization and simulations

3.1. DC characteristics

Fig. 3 shows typical I_D-V_G characteristics of 2 μm long SON and SG FD SOI MOSFETs in linear ($V_D = 50\text{ mV}$)

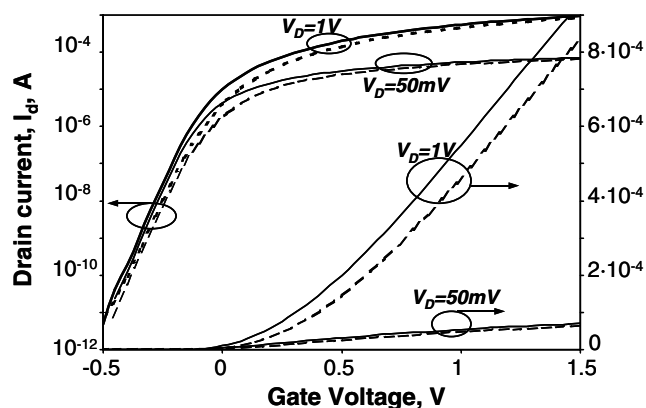


Fig. 3. I_D-V_G characteristics of SON (solid lines) and SG FD SOI (dashed lines) MOSFETs in linear ($V_D = 50\text{ mV}$) and saturation ($V_D = 1\text{ V}$) regimes plotted in semi-logarithmic and linear scales. $L = 2\text{ }\mu\text{m}$. $W = 10\text{ }\mu\text{m}$.

Table 1

Main extracted parameters of experimental SON and SG FD SOI MOSFETs with $L = 2\text{ }\mu\text{m}$ and $W = 10\text{ }\mu\text{m}$

	SON MOSFET	SG FD SOI MOSFET
V_T , V	−0.08	0.02
DIBL, mV/V	68	102
S , mV/dec		
Linear ($V_D = 50\text{ mV}$)	67.5	71.3
Saturation ($V_D = 1\text{ V}$)	67.3	72.9
G_m/I_D , V^{-1}		
Linear ($V_D = 50\text{ mV}$)	34.1	32.3
Saturation ($V_D = 1\text{ V}$)	34.2	31.6
$I_D/(W/L)$, A		
At $G_m/I_D = 10\text{ V}^{-1}$	3.6×10^{-6}	3.3×10^{-6}
At $G_m/I_D = 5\text{ V}^{-1}$	1.7×10^{-5}	1.5×10^{-5}

and saturation ($V_D = 1\text{ V}$) regimes. Well-behaving SON MOSFETs characteristics are obtained, proving the feasibility of proposed process for SON MOSFETs fabrication. Table 1 compares main parameters of SON MOSFETs with those of SG FD SOI counterparts. Threshold voltage, V_T , of SON MOSFETs is slightly lower than in SG counterparts, which is also confirmed by Atlas simulations. Indeed, the interfaces coupling in SON devices is attenuated and the control from the front gate is enhanced, which can result in lower threshold voltage and improved subthreshold characteristics. Smaller drain-induced barrier lowering (DIBL) effect in SON MOSFETs was expected [13] and may be related to the lower fringing fields, i.e., reduced drain-to-channel coupling through the buried dielectric. In addition, SON MOSFETs exhibit lower subthreshold slope, S , both in linear and saturation regimes, which directly results in higher achievable maximum transconductance-over-drain current ratio, i.e., $(G_m/I_D)_{\text{max}} = \ln(10)/S$ [14]. These are related, first, to the lower body factor in SON devices comparing to SG FD SOI counterpart (due to lower dielectric permittivity of air than of oxide and hence higher effective thickness) and, second, to the above-mentioned lower DIBL in SON devices, which is especially important in saturation regime. This explains the enhanced improvement in SON devices against SG counterpart in saturation: we can see degradation of both S and $(G_m/I_D)_{\text{max}}$ in saturation comparing to the “linear-regime” values for SG devices, while almost no change for SON ones. Finally, about 10% higher drive current is achievable in SON MOSFETs at fixed G_m/I_D which is normally related to [14,15] the lower body factor in these devices comparing to the SG counterparts, and possibly higher mobility in SON devices (due to lower electric fields), which, however, needs to be further confirmed by additional studies.

To validate and discuss the approach for decananometer dimensions, 2D Atlas simulations have been performed for 100 nm-long device with 2 nm gate oxide, 30 nm Si film and 150 nm “air” buried dielectric. In addition to confirming the interest of the air cavity to improve SCE control [6], our simulations have shown that extending the cavity

beyond the gate edges under source and drain regions still allows slightly improved DIBL and subthreshold slope by 3% and 1%, respectively. This extension is also very important for the misalignment issues already mentioned above. Simulations for the 100 nm-long device show that in the case of identical “air”-cavity and gate lengths, a 30 nm-misalignment of the cavity results in DIBL degradation by 11% and 4% whether “air”-cavity is shifted to the source or to the drain side, respectively, and S degradation of 3% and 2%, respectively. Contrarily, if the “air” cavity is extended under the source and drain regions, the 30 nm-misalignment on either source or drain side has no influence on DIBL and S .

Fig. 4 compares the I_D – V_D characteristics of 2 μm -long SON and SG FD SOI MOSFETs measured at different gate voltages. Higher drain currents are observed for SON MOSFETs at fixed V_G . This is partially related to the lower threshold voltage in addition to the above-mentioned lower body factor and possible mobility improvement. Another important feature is that the I_D – V_D characteristics of SON MOSFETs in saturation are much flatter than those of the SG FD SOI counterpart. Such decreased output conductance, G_D , in turn translates in a higher achievable Early voltages, $V_{EA} = I_D/G_D$ in SON MOSFETs, which is beneficial for further applications. Fig. 5 evidences the 20–150%, depending on the regime, higher V_{EA} in SON MOSFETs comparing to the SG FD SOI counterpart. There are two reasons for such high Early voltages in SON transistors. The first one is the improved control of the short-channel effects in SON transistors thanks to the strongly reduced coupling between drain bias and body potential (i.e., much lower lateral fringing electric fields), and hence lower DIBL as was already mentioned above. However, reduced DIBL alone can hardly explain the improvement of 150%. The second reason, especially important for higher gate biases, is related to the self-heating effect. In that case the G_D (and V_{EA}) improvements

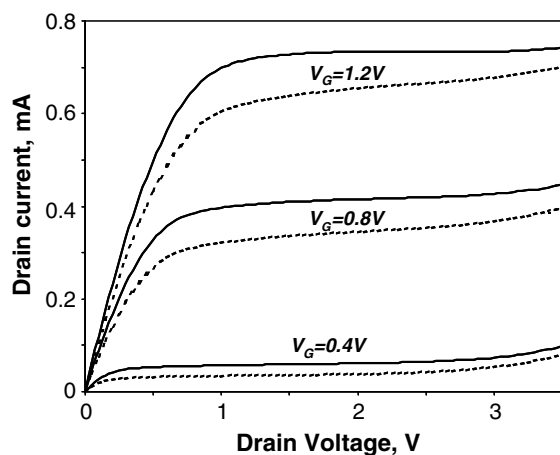


Fig. 4. I_D – V_D characteristics of SON (solid lines) and SG FD SOI (dashed lines) MOSFETs at different gate biases. $L = 2 \mu\text{m}$. $W = 10 \mu\text{m}$.

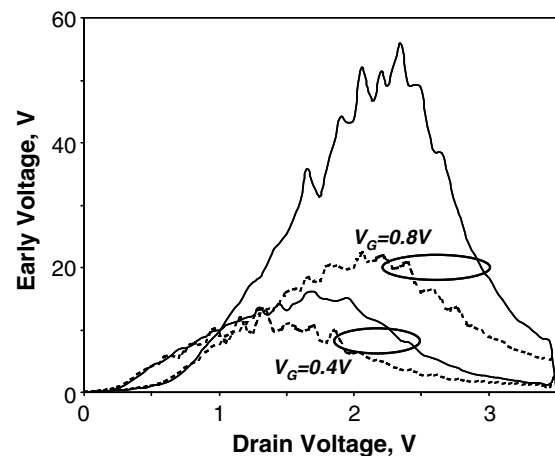


Fig. 5. Early voltages in SON (solid lines) and SG FD SOI (dashed lines) MOSFETs as a function of drain voltage at different gate biases. $L = 2 \mu\text{m}$. $W = 10 \mu\text{m}$.

achieved in SON MOSFETs at DC will be attenuated at high frequencies.

3.2. Self-heating effect

Enhanced self-heating effect is expected to be the main potential drawback of “true” SON MOSFETs even comparing to SG SOI MOSFETs [13]. The thermal conductivity of air is indeed much lower than that of oxide, generally used as the buried insulator in SOI structures ($2.6 \times 10^{-2} \text{ W/m/K}$ for air against 1.4 W/m/K for SiO_2) and bulk Si, which results in a stronger SON MOSFET overheat comparing to the bulk MOSFET and to SOI MOSFET with the same BOX thickness [13]. Note that we focus here on “true” SON, contrarily to “ST-SON” for which strongly attenuated SHE was demonstrated [2], since in “ST-SON” architecture thin BOX, not air-gap, is formed under channel, which eases heat evacuation.

2D Atlas simulations of SON and SG FD SOI MOSFETs with dimensions and thicknesses corresponding to our experimental devices were performed. Not only channel temperature but also the frequency variation of the output conductance were used to characterize the self-heating. At high frequency (typically 1–100 MHz) the self-heating effect is ruled out, and hence the difference between DC and high-frequency output conductance is often used as a measure of SHE [16,17].

Fig. 6a compares the channel temperature in 3 μm -long SON transistor and SG FD SOI counterpart, giving 5–7 $^\circ\text{C}$ more in the case of SON device at the maximum current. Such rather small difference in the channel temperature (about 5%), however, results in about two times stronger degradation of the output conductance in SON MOSFETs than in SG counterpart at $V_G = V_D = 2 \text{ V}$ (Fig. 6b).

The first experimental results confirm the tendencies predicted by 2D Atlas simulations. The output conductance vs. frequency measurements in a range from 1 kHz to 5 MHz were performed with Agilent B1500 for SON and SG

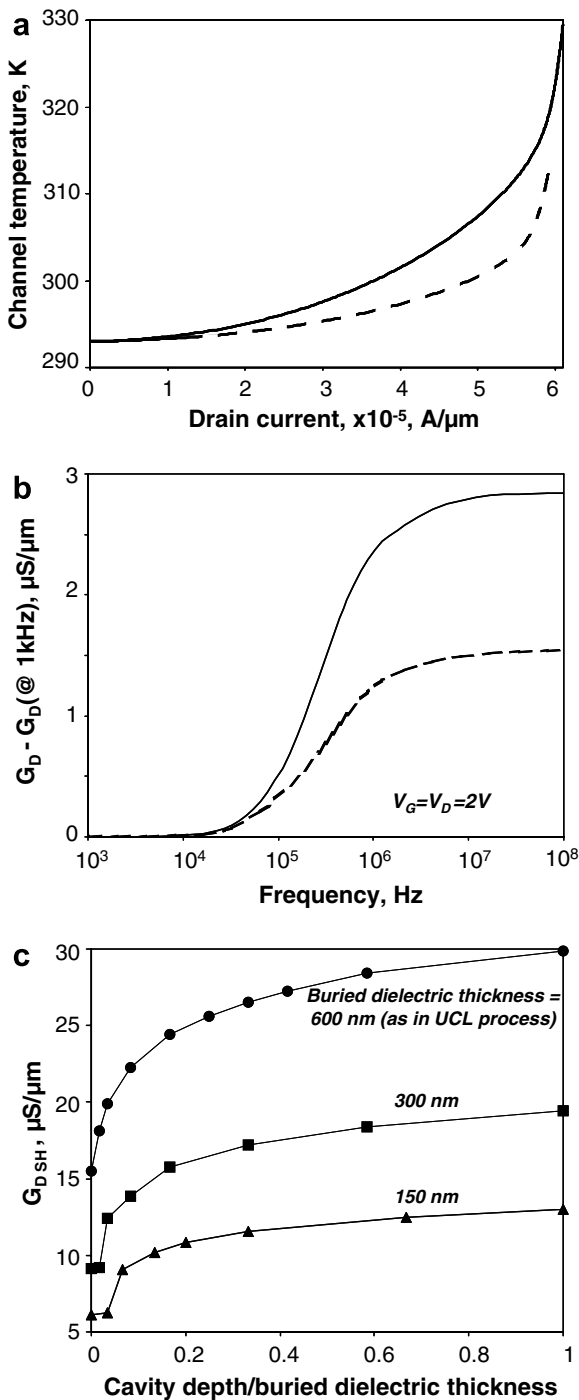


Fig. 6. 2D Atlas simulations. (a) Average channel temperature as a function of the drain current. (b) Output conductance variation with frequency in SON (solid lines) and SG FD SOI (dashed lines) MOSFETs. Device parameters are the same as used in our process: $T_{\text{gox}} = 30 \text{ nm}$, $T_{\text{Si}} = 80 \text{ nm}$, $T_{\text{BOX}} = 600 \text{ nm}$, $T_{\text{cavity}} = 350 \text{ nm}$ and $L = 3 \mu\text{m}$. (c) Amplitude of SHE-related output conductance degradation, $G_{DSH} = G_D(10^8 \text{ Hz}) - G_D(10^3 \text{ Hz})$ as a function of cavity depth to the total buried dielectric thickness ratio for different total buried dielectric thicknesses (600 nm – circles, 300 nm – squares, 150 nm – triangles).

MOSFETs. Fig. 7 demonstrates the SHE-related frequency variation of the output conductance in SON and SG MOSFETs at different biases. Similarly to the simulated results, SON MOSFET exhibit 2–3 times stronger output conduc-

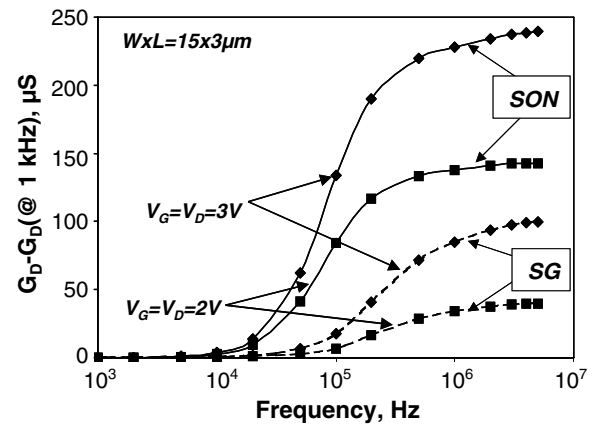


Fig. 7. Experimental output conductance vs. frequency variation measured on SON (solid lines) and SG FD SOI (dashed lines) MOSFETs with the same dimensions and the same biases. $L = 3 \mu\text{m}$. $W = 15 \mu\text{m}$.

tance degradation than SG counterpart, confirming that enhanced SHE is indeed a serious disadvantage of SON architecture and hence modifications and improvements are required in order to minimize this effect. Among such solutions we can imagine: reduction of the cavity depth and/or general thinning of the buried dielectric. Fig. 6c shows the variation of the SHE-related output conductance amplitude, i.e., $G_{DSH} = G_D(10^8 \text{ Hz}) - G_D(10^3 \text{ Hz})$, with cavity narrowing, keeping the total buried dielectric thickness the same. It is seen that for 600 nm-thick buried dielectric (as in UCL process) the reduction of cavity depth to less than 50 nm allows for strongly attenuating conductance degradation caused by SHE. However, we have to keep in mind that the price for this will be reduced channel control, resulting in degraded subthreshold slope (e.g., improvement in S comparing to SG is only 1% for 50 nm cavity, against 4–5% improvement in the case of 350 nm cavity), DIBL and other short-channel related effects as, e.g., source-to-drain coupling through the substrate discussed in the next section. Another approach to solve the problem of device overheat is to scale not only the cavity depth, but the buried dielectric thickness in general. Fig. 6c compares the SHE-related conductance degradation for different buried dielectric thicknesses (from 600 to 150 nm) as a function of the ratio of the cavity depth to total buried dielectric thickness. It is evident that buried dielectric thinning allows for strongly decreased SHE-related conductance degradation. Furthermore, this strategy does not lead to degradation, but on the contrary, improvement of the short channel effects, except for the source-to-drain coupling through the substrate (as discussed in the next section). The drawback of this approach is, however, that the related parasitic capacitances increase and hence the device speed reduces with buried dielectric thinning. Additionally, new/advanced engineering solutions for the heat sink/exhaust, as for example microfluidics or cavity filling with high thermal conductivity gas could be combined with our SON process on the contrary to other above-mentioned SON fabrication techniques.

3.3. Source-to-drain coupling through the substrate

It is well known that good control of short-channel effects requires FD SOI with ultra-thin Si film. On another hand, drain-to-channel coupling through the BOX, i.e., fringing fields, which acts as an additional short-channel effect, motivates the needs of BOX thinning to control these effects [2,18]. Furthermore, thin BOX is advantageous for attenuation of SHE. However, with BOX thinning and channel length scaling, the role of source-to-drain fringing coupling through the substrate (or variation of the potential at the substrate/BOX interface) becomes more important, which results in stronger output conductance degradation with frequency [11]. Fig. 8 shows variations of the output conductance with frequency for FD SOI MOSFETs with different BOX thicknesses simulated without taking SHE into account. Atlas simulations revealed that the degradation of the output conductance with frequency, caused by the variation of substrate capacitance [10] increases with BOX thickness decrease. Being only about 1% for FD SOI MOSFET with 400 nm-thick BOX, it can reach 150–250% (depending on frequency, bias conditions, etc.) for the devices with 20 nm BOX thickness as in “ST-SON” process. We hence believe that the coupling through the substrate can be a drawback of such approach. While the influence of coupling through the substrate in “ST-SON” devices was shown to be negligibly small on static characteristics [19], it will strongly degrade their dynamic behavior as evidenced in Fig. 8.

With this regards, true SON architecture appears as very promising solution since allowing to effectively suppress not only source-to-drain coupling through the buried dielectric, but also through the substrate. Fig. 9 presents output conductance frequency response simulated for the SON and SG FD SOI MOSFETs with dimensions corresponding to our experimental devices. The degradation of the output conductance is about six times smaller even in

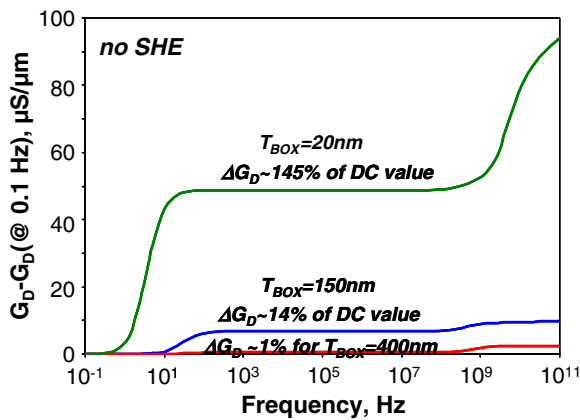


Fig. 8. Simulated output conductance variations with frequency in FD SOI MOSFETs with different BOX thicknesses. In order to avoid confusion, self-heating effect was not included in the simulations. $L = 0.17 \mu\text{m}$. $V_G = 0.7 \text{ V}$. $V_D = 1.5 \text{ V}$. $N_{\text{Asub}} = 6.5 \times 10^{14} \text{ cm}^{-3}$. $T_{\text{BOX}} = 2 \text{ nm}$. $T_{\text{Si}} = 60 \text{ nm}$.

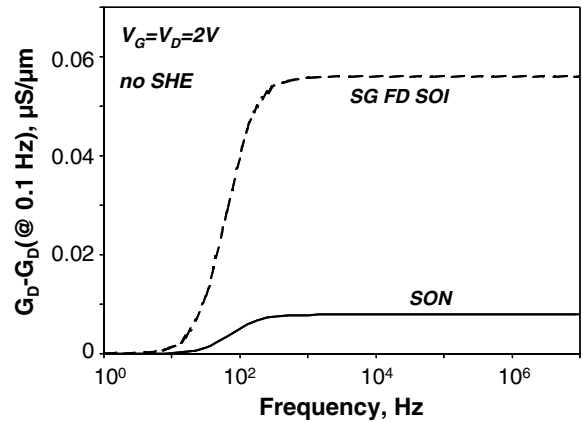


Fig. 9. Simulated output conductance vs. frequency variation in SON (solid line) and SG FD SOI (dashed line) MOSFETs. Device parameters are the same as used in our process: $L = 3 \mu\text{m}$. $T_{\text{gox}} = 30 \text{ nm}$. $T_{\text{Si}} = 80 \text{ nm}$. $T_{\text{BOX}} = 600 \text{ nm}$. $T_{\text{cavity}} = 350 \text{ nm}$. $N_{\text{Asub}} = 6.5 \times 10^{14} \text{ cm}^{-3}$. In order to avoid confusion, self-heating effect was not included in the simulations.

our case of 600 nm-thick BOX in SG FD SOI. This suppression can be further enhanced if the cavity length is extended under source and drain regions as well as if the cavity is deepened to the whole buried dielectric thickness reaching the substrate interface.

4. Conclusions

In this paper, the “Si layer transfer by wafer bonding over the pre-etched cavity” process has been demonstrated to be suitable for the fabrication of true SON MOSFETs. This process is rather flexible to device dimensions as well as to thicknesses of Si film and “nothing” layer. It is compatible with standard SOI CMOS process (after Si layer transfer is performed). In addition, application of this process for SON MOSFETs fabrication appears to be more relaxed with regards to the process requirements, such as device dimensions, alignments, polySi doping, comparing to the DG MOSFETs fabrication. Moreover, this approach for SON fabrication is consistent with 3D integration of special buried interconnects, dielectrics or heat exhaust solutions, contrarily to other techniques of SON realization.

Comparative electrical characterization revealed that fabricated SON MOSFETs over-perform SG FD SOI counterparts in terms of drive current, DIBL, subthreshold slope, transconductance-over-drain current ratio and even approach the DG MOSFETs fabricated with the same process [9]. Furthermore, the “substrate-related” variation of the output conductance with frequency has been demonstrated to be practically suppressed in SON MOSFETs.

The main disadvantage of “true” SON MOSFETs, i.e., the enhanced self-heating, has been confirmed experimentally for the first time. Experiments and simulations have shown 2–3 times stronger degradation of the output conduction variation with frequency due to SHE in SON MOSFETs compared to SG FD SOI counterparts.

Subsequent process/design modifications can be expected to result in a further improvement of the SON MOSFET performance. Extending of cavity length under source and drain regions can even stronger decrease the parasitic source-to-drain coupling through buried dielectric and Si substrate, resulting in reduced DIBL, improved sub-threshold slope, completely suppressed substrate-related output conductance degradation with frequency, etc. Moreover, such extension will further rule out the influence of charges at Si film–buried dielectric interface (i.e., bonded interface in our case) on the transistor parameters. Extended cavity under source/drain regions should also facilitate the practical realization of short-channel devices, solving misalignment issue. While proposed approach does not introduce special (specific or additional) limitations or restrictions to the channel length and thickness of the Si film (which can be thinned down after bonding step), further studies are, however, necessary to demonstrate the feasibility of proposed approach for the fabrication of thin-film short-channel SON MOSFETs. Then, the deepening of the cavity, down to the whole BOX thickness, may also allow to decrease the coupling due to the substrate, while it will increase the device overheat. In order to reduce self-heating effect, the general buried dielectric thickness should be reduced. Otherwise, new advanced engineering inventions enabling an improved heat exhaust could be integrated.

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