Temperature dependence of RF losses in HR SOI substrates

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Introduction: High Resistivity (HR) Si substrates with resistivity values higher than 3 kΩ.cm have been demonstrated to be suitable for High Frequency applications due to their negligible ohmic losses [1, 2]. However, oxide-passivated HR Si substrates usually suffer from resistivity degradation near the SiO_2/Si interface due to the presence of fixed charges (Q_{ox}) in the oxide. These charges attract free carriers near the substrate surface, forming a low conductivity accumulation or inversion layer [3]. Coplanar structures made on such substrates are very sensitive to the presence of this layer, which can lead to substantial RF loss increases [4]. As shown in [4] and [5], an efficient way to (partially or entirely) remove this conductive layer is to introduce a large density of traps (D_{it}) at the SiO_2/Si interface. In this work we investigate for the first time the suitability of HR SOI substrates for high temperature RF applications. The proposed analysis combines the effects of high temperature (T) and interface traps on resistivity degradation in HR SOI substrates. The temperature range of interest is selected from 20 to 200°C. It is shown that substrates without traps exhibit poorer high temperature performance.

Structure and Model: The simulations presented in this work were performed on a 2-dimensional device corresponding to the cross-section of a 50-Ω CPW line. The geometry of the device is presented in Fig. 1. As can be seen, the chosen substrate is a p-type wafer with N_a = 5x10^{12} /cm^3, corresponding to a nominal value of substrate resistivity (r_{DC}) close to 3 kΩ.cm. The mobility model used for the simulations is the *Lombardi cvt* model implemented in Atlas. It is a complete model that includes transverse field, doping and temperature dependent parts of the mobility as well as mobility degradation effects due to increased scattering in inversion layers [6]. For all simulations the backside of the substrate was grounded. For the simulations performed with interface traps, a constant trap distribution was considered throughout the Si bandgap (as in [4]). In all cases, the value of Q_{ox} was set to 1x10^{10} /cm². The AC simulations were performed from 0 to 40 GHz with 1 GHz step at 20, 70, 100, 150 and 200°C. The total simulated high frequency conductance (resp. capacitance) between the central electrode and the lateral electrode is noted G_{eff} (resp. C_{eff}).
The quality factor considered in this work to characterize the substrates is the value of their *effective resistivity* (r_{eff}), which is the resistivity actually 'seen' by the coplanar structures at RF and which accounts for surface variation of Si resistivity created by accumulation, inversion and/or depletion. It is related to G_{eff} by:

$$G_{eff} = \frac{K}{2\,r_{eff}} \qquad (1) \qquad\qquad C_{eff} = K e_{eff} \qquad (2)$$

where K [m] is a geometry factor that can be evaluated from C_{eff}. In the latter equation, e_{eff} is the RF effective permittivity of the structure. Its value (6.22.ε_0) was extracted from experimental measurements of propagation constant at 20°C on the CPW line presented in Fig. 1. It is expected from data presented in [7] that the temperature dependence of this parameter is rather small and has therefore not been included in the analysis. r_{eff} is then directly computed from (1) and (2).

Results and Discussion: At RF the total losses (a) in a CPW transmission line can be approximated by: $a \approx 0.5\,(R\,(C/L)^{0.5} + G\,(L/C)^{0.5})$ where R,G, C and L are the elements of the line distributed circuit. The first and the second terms in the sum represent conductor and substrate ohmic losses, respectively. As R is a linear function of T, it is expected that conductor losses should vary accordingly. However this dependence will not be considered in this paper. Figure 2 shows simulated data of a vs f for different values of r_{eff} at 20 °C and including both conductor *and* ohmic losses [2]. The data clearly indicate that the HR Si substrates behave as quasi-lossless when r_{eff} > 3 kΩ.cm; their ohmic losses are minor (< 0.5 dB/cm) when 1 kΩ.cm < r_{eff} < 3 kΩ.cm but they suffer from significant ohmic losses (> 0.5 dB/cm) and are thus inadequate for RF applications when r_{eff} < 1 kΩ.cm.
Figure 3 presents the extracted value of r_{eff} with respect to f for a HR (N_a = 5x10^{12} /cm³, r_{DC} = 3 kΩ.cm) and a standard resistivity (N_a = 6.5x10^{14} /cm³, r_{DC} = 20 Ω.cm) substrate without traps. It is interesting to notice that for all temperature points the value of r_{eff} is much smaller than 3 kΩ.cm for the HR substrate. This is related to the inversion layer formed at the substrate surface and induced by Q_{ox}, reducing r_{eff} by more than one order of magnitude and making the HR substrate unsuitable for RF applications. For temperatures below 100 °C the data indicate that r_{eff} is a slightly increasing function of T. A possible explanation for this observation is a temperature-related mobility reduction inside the inversion layer. However, above 100 °C r_{eff} drastically decreases and drops down to 80 Ω.cm at 200 °C. This is a direct consequence of the intrinsic carrier concentration (n_i)increase in the substrate. The figure also shows that the standard resistivity substrate exhibits an increase of r_{eff} with T, which could also be explained by substrate mobility reduction at higher temperatures.

Figure 4 indicates that r_{eff} is largely improved up to 150 °C when interface traps are present in the structure. The improvement is the most obvious in the lower temperature range and reaches a saturation value close to 4 kΩ.cm for D_{it} values of $3x10^{10}$ /cm²/eV and higher. This increase is directly related to the absorption of free carriers from the SiO_2/Si interface and the subsequent creation of a highly resistive depletion layer underneath the oxide. The data show that the substrate remains quasi-lossless up to 90 °C when $D_{it} \geq 3x10^{10}$ /cm²/eV, with an acceptable level of RF losses up to 70°C for $D_{it} = 1x10^{10}$ /cm²/eV and up to 120 °C for $D_{it} \geq 3x10^{10}$ /cm²/eV. For temperature points higher than 120°C the HR substrates exhibit high losses and become therefore inappropriate for RF applications, regardless of interface trap density. At 200°C, the value of r_{eff} becomes as low as ~60 Ω.cm, a value comparable to that of lower quality standard resistivity wafers. This last observation suggests that no RF substrate loss reduction is obtained when using HR instead of standard Si substrates at temperature points higher than 200°C. This shall be supported by experimental data in a near future.

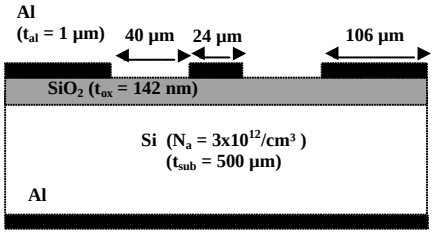

Figure 1: Simulated structure.

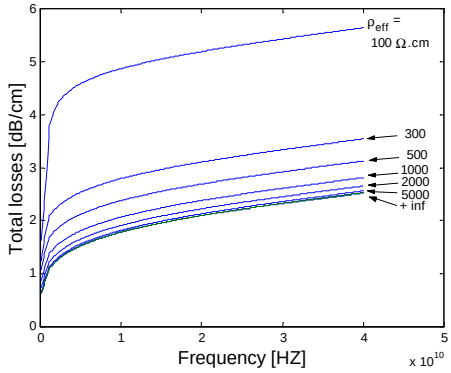

Figure 2: Total losses vs f for varying r_{eff} values.

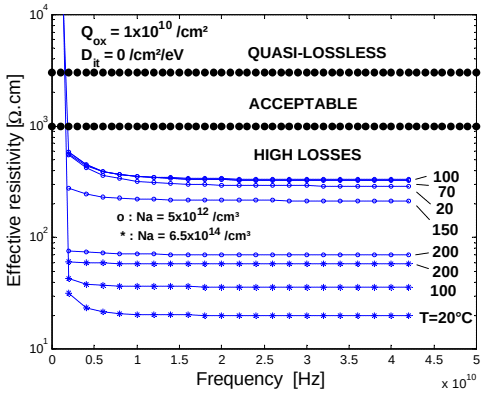

Figure 3: r_{eff} vs f for different T and N_a values.

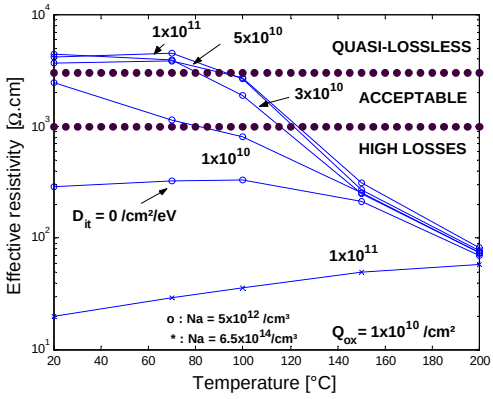

Figure 4: r_{eff} vs T at RF for varying D_{it} and N_a values.

Conclusion: Atlas simulations have shown that HR SOI substrates with an initial resistivity of 3 kΩ.cm are unsuitable for RF applications, even at ambient temperature (T), if fixed charges as low as $1x10^{10}$ /cm² are present in the buried oxide. This is consistent with data presented in [2]. However, when trap densities equal to $3x10^{10}$/cm²/eV or higher are introduced at the SiO_2/Si interface, the substrates become and remain quasi-lossless up to 90 °C. They still remain acceptable for RF applications (a_{sub} < 0.5dB/cm) up to 120°C, above which point they start suffering from significant RF losses and become therefore inadequate for RF applications. At 200°C, the simulations show that the quality of HR wafers is comparable to that of low cost standard resistivity wafers. These findings shall be supported in a near future by experimental data.

References

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