Nano Express

INCLUSIVE PUBLISHING TRUSTED SCIENCE
PURPOSE-LED PUBLISHING™

PAPER • OPEN ACCESS

Mechanisms of forward current transport in vertical nanoscale devices: insights and applications

To cite this article: Long Chen *et al* 2025 *Nano Ex.* **6** 015022

View the article online for updates and enhancements.

You may also like

- Photocatalysis and adsorption coupling in S-scheme K and P doped g-C_3N_4/GO/$MgFe_2O_4$ photocatalyst for enhanced degradation of Congo red dye
Rohit Kumar, Aftab Aslam Parwaz Khan, Anita Sudhaik et al.
- Microstructural, morphological, and optical properties of Fe_2O_3 nanoparticles obtained from Fe-MIM MOF
Olalekan C Olatunde, Murendeni P Ravele, Tunde L Yusuf et al.
- Investigation of solution-processed tungsten disulfide as switching layer in flexible resistive memory devices for performance and stability
Shalu Saini and Shree Prakash Tiwari

The Electrochemical Society
Advancing solid state & electrochemical science & technology

249th
ECS Meeting
May 24-28, 2026
Seattle, WA, US
Washington State Convention Center

Spotlight Your Science

Submission deadline: December 5, 2025

SUBMIT YOUR ABSTRACT

This content was downloaded from IP address 130.104.45.220 on 28/10/2025 at 10:44

NANO EXPRESS

OPEN ACCESS

RECEIVED
3 September 2024

REVISED
11 November 2024

ACCEPTED FOR PUBLICATION
28 November 2024

PUBLISHED
24 March 2025

Original content from this work may be used under the terms of the Creative Commons Attribution 4.0 licence.

Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.

PAPER

Mechanisms of forward current transport in vertical nanoscale devices: insights and applications

Long Chen[1,2], Liting Liu[1], Hongfu Li[1], Xingqiang Liu[3], Yuan Liu[1], Jean-Pierre Raskin[4], Denis Flandre[4] and Guoli Li[1,3]

[1] Key Laboratory for Micro/Nano-Optoelectronic Devices of Ministry of Education, and International Science and Technology Innovation Cooperation Base for Advanced Display Technologies of Hunan Province, School of Physics and Electronics, Hunan University, Changsha 410082, People's Republic of China

[2] Research Institute of Hunan University in Chongqing, Chongqing 401135, People's Republic of China

[3] College of Semiconductors (College of Integrated Circuits), Hunan University, Changsha 410082, People's Republic of China

[4] Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université Catholique de Louvain, Louvain-la-Neuve 1348, Belgium

E-mail: liguoli_lily@hnu.edu.cn

Keywords: 2D material, current transport, vertical device, simulation

Abstract

Current transport at metal/semiconductor interface becomes critical to determining ultimate limit in performance of two-dimensional (2D) electronic devices. In this work, we study output characteristics as well as carrier transport of the vertical Schottky-contact 2D transistors and diodes, by experimental measurements and detailed TCAD simulations. Device output current under the forward bias is primarily attributed to thermionic emission (TE) mechanism, then tunneling occurs and becomes the dominant interfacial charge transport in the few-layered MoS_2 transistors. While shrinking the vertical channel length from 20 nm to 3.6 and increasing the applied voltage, tunneling ratio rises above 90% for the sub-5 nm scale, indicating the dominated tunneling mechanism. Simultaneously, the Schottky diode loses its rectification ability. Noticeably, Fowler–Nordheim tunneling (FNT) mechanism cannot be accurately identified through the linear slope of $\ln(I/V^2)$ *versus* $1/V$ (FN-relation) of output current under high electric field, due to the co-existing thermionic current that displays a linear-like feature in the FN-relation plots. The transition from TE to FNT and direct tunneling (DT) regimes can be identified by analyzing the output current components and FN-relation of tunneling current. These results can be employed to understand physical insights and transport limitations of the nanoscale electronics, and to optimize the device design and performance for their ultra-scaled, low-power applications.

1. Introduction

Two-dimensional (2D) materials commonly feature controllable atomic-layer thickness [1–4], uniform flat surface [5–7], superior carrier mobility and effective mass [8–10], *etc*, over the conventional silicon technology in the post-Moore era [11–13]. Among them, transition metal dichalcogenides (TMDs) have been widely explored as alternative channel materials for electronic devices at the sub-10 nm scale [14–22]. For instance, the TMD-based pn junction, diode and field-effect transistor (FET) have been intensively realized in a vertically stacked configuration with the channel length scaled to few-atomic-layer thickness [23–27], and simultaneously featuring their decent rectifier behavior, high-frequency operation, and increased integration density.

Scaling down the channel length below depletion width of the Schottky barrier, current transport through the transistors becomes complex, in which the device output can be attributed by a combined effect of thermionic emission (TE) and field-emission tunneling [28, 29]. Previous works have discussed current and carrier transport inside the vertically-stacked elements. For instance, Li Hua-Min *et al* constructed the sub-5 nm vertical MoS_2-based p-n junctions, where the tunneling mechanisms like direct tunneling (DT) and Fowler–

© 2025 The Author(s). Published by IOP Publishing Ltd

Nordheim tunneling (FNT) dominated carrier transport [23]. Similar transport mechanisms were observed in other 2D materials-based heterostructure or p-i-n heterojunction [24, 30]. And the vertical transport model at the metal/TMDs interface has also been developed, with FNT mediated under high electric fields and TE dominated under low fields [31]. Among them, the $\ln(I/V^2)$ *versus* $1/V$ plot of the device current–voltage (I-V) was employed to clarify the transition from TE to DT and FNT. However, while continuously shrinking the vertical device geometry from bulk to the sub-10 nm scale, several questions are raised: (i) can the tunneling mechanism always be straightforwardly identified as the linear dependence featured in the $\ln(I/V^2)$ *versus* $1/V$ plots? (ii) how to adequately clarify the components of over-barrier thermionic current and under-barrier tunneling current across the metal/TMD contacts and their impact on device output thereafter, from theoretical and experimental aspects? These understandings are required for further exploring the physical limitation of 2D transistors, and critical for their ultra-scaled, high-performance design, and high-efficiency application in the next-generation nano-electronics.

In this work, we investigate the current characteristics and carrier transport mechanisms inside the vertical Schottky-barrier MoS_2-based FET and diode. The van der Waals (vdW) integration approach is implemented for the device fabrication, and TCAD simulation is carrier out to interpret the current transport and physical insights of vertical nanoscale device. Specifically, we notice that the linear feature of $\ln(I/V^2)$ *versus* $1/V$ plot of the output current under high electric fields cannot determine the FNT mechanism since the co-existing thermionic current also displays a linear-like feature. However, this method is available for sub-5 nm cases since the tunneling current is major contributor to output current. Furthermore, the output components like thermionic and tunneling current, of these devices with varying vertical channel length are quantified to explore size limit of MoS_2-based Schottky diodes. Our findings can be used for adequately understanding the current transport at the metal/TMDs contact interface of the vertical devices.

2. Results and discussion

2.1. Experimental measurements

To realize the atomically clean and high-quality metal/semiconductor interface, the 2D vdW integration and electrode lamination process are employed to fabricate the vertical MoS_2 transistors, with the experimental details described in our previous report [25]. In figure 1(a), the metal/MoS_2/graphene are stacked in a vertical direction. The graphene layer is grounded as the source, the top-metal (Ag/Au, 30/20 nm thick) is biased as the drain (V), and the back-gate voltage (V_B) is applied on the heavily doped silicon substrate. Sweeping V_B from negative to positive, the Fermi level in graphene rises from below to above the Dirac point and aligns to the conduction bottom in MoS_2 [32], thus modulating barrier height at the interface. Figure 1(b) shows the charge transport mechanisms through the Schottky contact interface, the tunneling is more likely to occur while scaling the vertical channel length. At low V, the field-induced band bending is not serious and the tunneling current is generated by DT mechanisms. Under high electric field (high V), the tunneling distance is reduced, then the tunneling current is mainly originated from FNT.

The output drain current (I) as a function of drain bias (V) are illustrated in figures 1(c) and (d), for the vertical eight- (~5 nm-thick) and five-layered (~3.6 nm-thick) MoS_2 transistors, respectively. The output characteristic features a linear relationship when a very positive V_B (e.g. 60 V) brings the lowered Schottky barrier. On the other hand, the output current I gets suppressed under a negative V_B (e.g. -60 V), and the I-V curve displays the nonlinear characteristics indicating the increased barrier height. Under the high electric field, a higher output current is observed in the 3.6 nm-thick device with a more negative V_B, which could be attributed to the decreased channel length and the enhanced tunneling effect at contact interface. Correspondingly, $\ln(I/V^2)$ *versus* $1/V$ (i.e. FN-relation, as discussed next) plots of the device output currents are depicted in insets of figures 1(c) and (d) for the eight- and five-layered MoS_2 transistors, respectively. The linear slope of the FN-relation plots under high bias voltage (low $1/V$) is referred as the criterion of FNT dominance [23, 24], whereas the logarithmic growth at low bias voltage indicates the transport mechanisms of direct tunneling (DT) and thermionic emission (TE). However, as illustrated in figure 1(b), charge transport mechanisms at the Schottky junction are denoted with direct tunneling (DT), Fowler–Nordheim tunneling (FNT), and thermionic emission (TE), which are specifically dependent on the electrical condition (contact barrier Φ_B, bias V) and device geometry (channel length d) [33, 34].

2.2. TCAD simulation analyses

In order to elucidate the current transport and conduction mechanisms inside the vertical nanoscale device, an equivalent two-terminal structure of the vertical Schottky diode is constructed in the TCAD platform (Atlas/SILVACO) [35]. Herein, MoS_2 is an intrinsically n-type semiconductor with varying thickness from 3.6 nm to 20 nm, the affinity and intrinsic bulk defect density are 4.2 eV and 1×10^{18} cm^{-2}/eV [36], respectively. The

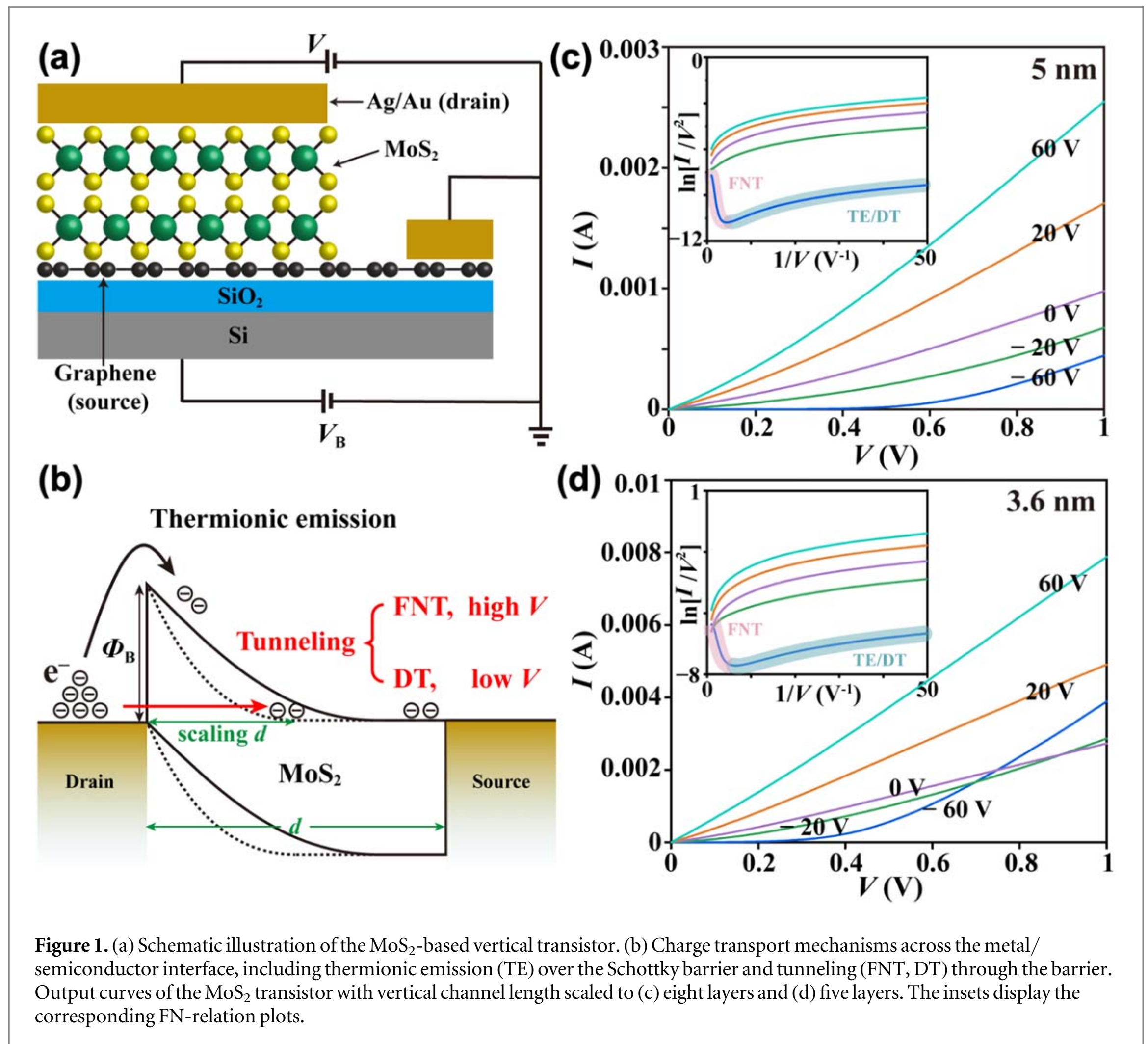

Figure 1. (a) Schematic illustration of the MoS_2-based vertical transistor. (b) Charge transport mechanisms across the metal/semiconductor interface, including thermionic emission (TE) over the Schottky barrier and tunneling (FNT, DT) through the barrier. Output curves of the MoS_2 transistor with vertical channel length scaled to (c) eight layers and (d) five layers. The insets display the corresponding FN-relation plots.

indirect band gap can be set to 1.3 eV for MoS_2 layer numbers exceeding four [23, 37]. Herein, the thermionic emission and Tsu-Esaki model are employed to simulate the current transport at Schottky contact interface. The boundary conditions are defined as a Schottky contact for the anode and an ohmic contact for the cathode. Then the external bias V is applied on anode and the Schottky barrier height Φ_B is set to 0.37 eV. Further, there are at least ten mesh cells in each nanometer along the carrier transport direction to guarantee the precision of numerical simulations. Both effective contact areas between the metal and semiconductor are 1 μm × 1 μm.

The thermionic current (I_{TE}) and tunneling current (I_{TN}) *versus* the applied bias V are plotted logarithmically in figure 2(a), while shrinking the vertical channel length (i.e. the film thickness d) from 20 nm to 3.6 nm. I_{TN} increases as d is scaled down, and starts to dominate the total current under large bias for $d = 3.6$ nm, implying a non-negligible role in carrier transport at the nanoscale device. In contrast, the over-barrier thermionic current I_{TE} grows exponentially with V before showing the sign of saturation in figure 2(a), and remains a constant regardless of the vertical channel length, proving that thermionic emission mechanism is independent of device geometry. Tunneling ratio (TR), we define it as $TR = I_{TN}/I_{TA}$, here, $I_{TA} = I_{TN} + I_{TE}$ is the device output total current. TR is employed to evaluate the dominant mechanism in the forward current transport. When TR exceeds 50%, it can be considered that tunneling is the main transport mechanism. Conversely, the thermal emission current is the main contributor to the output current. At $V = 1$ V, TR gets enhanced and reaches up to 66.5% while scaling d from 20 down to 3.6 nm. That means, carrier transport inside the vertical Schottky diode has switched from mainly thermionic emission to mainly tunneling response for the shortened vertical channel length and increased applied bias. These explain well the electrical behavior of ultra-scaled vertical devices, observed in other reports and our experimental characterizations [24, 25, 27].

To further clarify the thermionic emission and tunneling mechanisms inside the vertical diodes, each current component contributing to output characteristics is discussed separately as follows. Generally, thermionic emission currents over the Schottky barrier is given by [33, 35]:

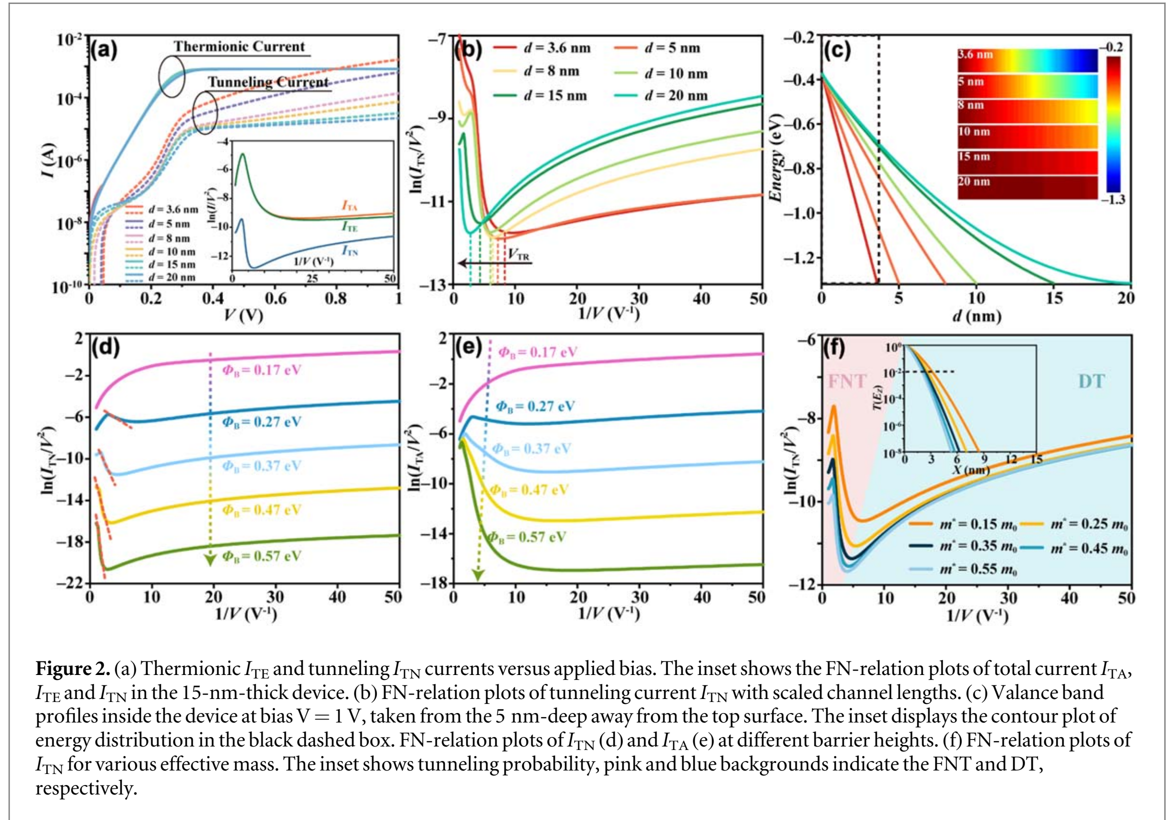

Figure 2. (a) Thermionic I_{TE} and tunneling I_{TN} currents versus applied bias. The inset shows the FN-relation plots of total current I_{TA}, I_{TE} and I_{TN} in the 15-nm-thick device. (b) FN-relation plots of tunneling current I_{TN} with scaled channel lengths. (c) Valance band profiles inside the device at bias V = 1 V, taken from the 5 nm-deep away from the top surface. The inset displays the contour plot of energy distribution in the black dashed box. FN-relation plots of I_{TN} (d) and I_{TA} (e) at different barrier heights. (f) FN-relation plots of I_{TN} for various effective mass. The inset shows tunneling probability, pink and blue backgrounds indicate the FNT and DT, respectively.

$$I_{TE} = A_{eff} A^* T^2 \exp\left(-\frac{\Phi_B}{kT}\right)\exp\left(-\frac{qV}{kT}\right), \tag{1}$$

where A_{eff} is effective contact area and normalized to be 1 μm^2 in our analyzation. T and Φ_B are temperature and barrier height, respectively. $A^* = 4\pi m^* qk^2/h^3$ is effective Richardson constant, and here m^* (= 0.47 m_0, m_0 is the free electron mass) is the effective electron mass of MoS_2 [38], q is elementary charge, k and h are Boltzmann's and Planck's constant, respectively. With respect to tunneling effect, FNT occurs at high bias. In such case, the FNT current (I_{FNT}) can be expressed as [29, 39]:

$$I_{FNT}(V) = \frac{A_{eff} q^3 m_0 V^2}{8\pi h \Phi_B d^2 m^*} \exp\left[-\frac{8\pi\sqrt{2m^*}\Phi_B^{\frac{3}{2}} d}{3hqV}\right], \tag{2}$$

where d is depletion width, i.e. the channel length in our cases. For further identify the FNT response in numerical results, the current–voltage characteristics are analyzed by plotting FN-relation. Therefore, the equation (2) can be rewritten as [23, 29]:

$$\ln\left[\frac{I_{FNT}(V)}{V^2}\right] = \ln\left[\frac{A_{eff} q^3 m_0}{8\pi h \Phi_B d^2 m^*}\right] - \frac{8\pi\sqrt{2m^*}\Phi_B^{\frac{3}{2}} d}{3hqV}, \tag{3}$$

indicating that the FNT response can be identified by a linear dependence in the FN-relation of $I_{FNT}(V)$. This signature has often been used by many researchers to verify the dominant FNT transport from experiments [23, 24, 30, 31].

Herein, we replot the FN-relation regarding I_{TA}, I_{TE} and I_{TN} of the vertical Schottky diode, as depicted in the inset of figure 2(a). In the high-voltage region, the FN-relation plot of I_{TN} clearly exhibits the linear dependence. Similar trends are also observed in figure 2(b), where the tunneling transport gets enhanced with reduced device geometry. Note that the I_{TE} achieves high current density, and also exhibits a linear-like feature in the FN-relation plot at low $1/V$. This implies that the linear-like feature in FN-relation plot of I_{TA} under high field (large bias, V) cannot ascertain the FNT mechanism in the nanoscale device. In such case, without adequately specifying the current components or verifying the dominant mechanism, it could be hazardous to conclude the FNT existence from the experimental results merely. At low bias, the barrier is not strongly deformed by the applied electric field. The current ascribed to direct tunneling (DT, I_{DT}) follows a linear relation to the bias V according to [29, 39]:

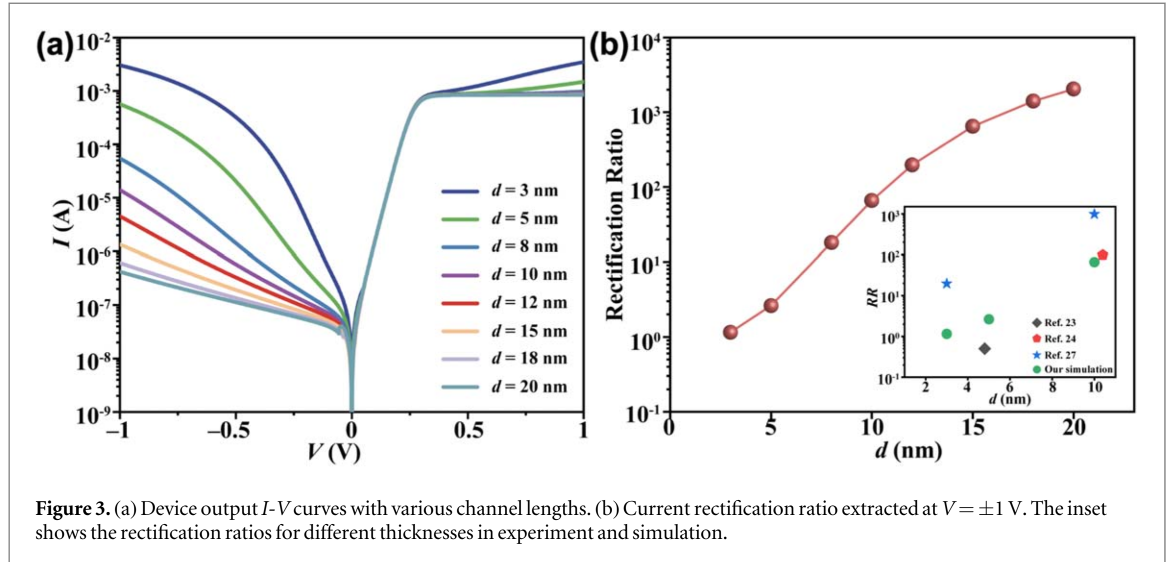

Figure 3. (a) Device output *I-V* curves with various channel lengths. (b) Current rectification ratio extracted at $V = \pm 1$ V. The inset shows the rectification ratios for different thicknesses in experiment and simulation.

$$I_{DT}(V) = \frac{A_{eff} q^2 \sqrt{m_0 \Phi_B} V}{h^2 d} \exp\left[-\frac{4\pi\sqrt{m_0 \Phi_B} d}{h}\right]. \tag{4}$$

Thus, a 'tick' shape is completely displayed in the plot of FN relation, regarding the tunneling current $I_{TN}(V)$ for the whole bias range. The strong linear dependence under a high bias suggests that FNT transport is dominant, whereas the logarithmic growth at a low bias represents DT mechanism.

For such that, the transition voltage (V_{TR}) is defined as the voltage at the transition of linear (FNT) to logarithmic region (DT). When the vertical channel length d decreases from 20 to 3.6 nm, the transition voltage V_{TR} gets reduced from 0.37 to 0.11 V (figure 2(b)). We point out that here, scaling d enables carriers yielding sufficient energy for tunneling due to the field-effect band bending [27], which leads to FNT occurring at lower bias. This session of analytical simulation interprets and agrees well with the experimental observations in [23, 30], where the absolute value of V_{TR} also decreased with the reduced thickness of the MoS_2-based pn junction. Figure 2(c) depicts the band diagram (at $V = 1$ V) of the Schottky diodes. As shown, the tunneling distance around the anode Schottky contact gets reduced, with d is scaling down. Correspondingly, the slope extracted from the FN-relation plot of I_{TN} under the high electric field gets steeper (figure 2(b)), which is consistent with the derivation from equation (3).

Furthermore, the impacts of barrier height Φ_B and carrier effective mass m^* on output characteristics of the device are investigated in figures 2(d)–(f). Heightening Φ_B from 0.17 to 0.57 eV at the anode, both I_{TN} and I_{TA} are largely suppressed. The absolute value of linear slope in FN-relation plot for tunneling current increases with the barrier height, guided with the red dashed lines in figure 2(d), and being proportional to $\Phi_B^{3/2}$ as analytically described in equation (3). Noticeably, weakening the barrier height, the FN-relation plots of I_{TN} and I_{TA} feature similar trends at $\Phi_B = 0.17$ eV, in which the tunneling current dominates. These simulated results explain how the Schottky barrier impacts the device output current and are consistent with our observations in figure 1(d), where Φ_B is modulated by the external bias V_B and the Ohmic-like contact is achieved at $V_B = 60$ V. In another aspect, reducing the effective mass m^* from 0.55 to 0.15 m_0, I_{TN} in figure 2(f) gets increased obviously. As shown in the inset, the tunneling probability $T(E_z)$ under the WKB approximation gets enhanced as m^* decreases, i.e. $T(E_z) \propto \exp(-\sqrt{2m^*})$ [34]. At a fixed $T(E_z)$, the distance for carriers travel through the barrier becomes shorter as the effective mass m^* increases, which agrees with the description in [28, 34], where tunneling distance d_T scales as $1/\sqrt{m^*}$.

Scanning the applied bias V from the forward to reverse conditions, full output curves of the vertical diodes with varying channel lengths are plotted in figure 3(a). Overall, favorable rectification characteristics are displayed for the channel length d exceeding 5 nm, where the output current under the forward bias maintains saturation and the reverse current gets notably suppressed. However, scaling d down to 5 and 3 nm, the reverse current level gets enhanced by orders of magnitude, which can be attributed to the reduction in tunneling distance caused by field-induced band bending. Rectification ratios (RR), defined as the ratio between the forward current I_F and the reverse current I_R, i.e. $RR = I_F/I_R$, are then calculated at $|V| = 1$ V for the various diode lengths in figure 3(b). The asymmetric nonlinear *I-V* characteristic for forward (I_F, $V > 0$ V) and reverse (I_R, $V < 0$ V) biases guarantees a reasonably high RR of $\sim 10^3$ for $d = 20$ nm. Also, the vertical diode with a 10 nm-thick film reveals a reasonable RR value of 66. These are close to the RR values reported previously in the 2D TMDs-based diodes, e.g. $RR = 20$ for a 10.4 nm-thick vertical WSe_2 diode and $RR = 1$ for the 8 nm-thick MoS_2 pn junction [23, 24, 27]. Further shrinking the diode length down to 3 nm, the device approximately loses

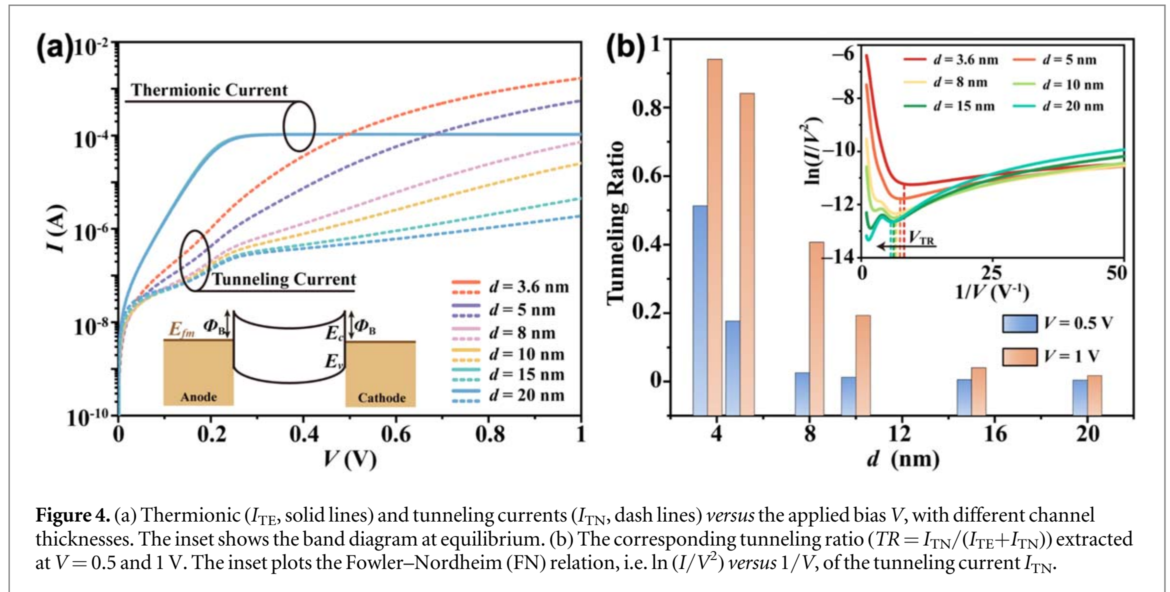

Figure 4. (a) Thermionic (I_{TE}, solid lines) and tunneling currents (I_{TN}, dash lines) *versus* the applied bias V, with different channel thicknesses. The inset shows the band diagram at equilibrium. (b) The corresponding tunneling ratio ($TR = I_{TN}/(I_{TE}+I_{TN})$) extracted at $V = 0.5$ and 1 V. The inset plots the Fowler–Nordheim (FN) relation, i.e. ln (I/V^2) *versus* $1/V$, of the tunneling current I_{TN}.

its rectification ability ($RR = 1.16$), as shown in figure 3(b). In other words, the tunneling effect becomes dominant in vertical Schottky device whatever in forward or reverse transport for such scale limit. For example, the $RR < 1$ has been experimentally measured for an 8 nm-thick vertical MoS_2 pn junction [23], demonstrating the ultimate limit in the vertical nanoscale diode before switching from the operation of thermionic emission to the dominant tunneling mechanism.

In the 2D vertical transistor or diode fabrication, the symmetrical metal contacts are often utilized [40, 41]. Therefore, in the device modeling, we specify that both anode and cathode are Schottky contacts with the same barrier height Φ_B of 0.37 eV. Figure 4(a) describes the numerically analyzed thermionic emission currents (I_{TE}, solid line) and tunneling currents (I_{TN}, dashed line) as a function of the applied voltage V for the symmetrical-Schottky-contact diodes, with 3.6, 5, 8, 10, 15 and 20 nm-thick vertical channels. While comparing with the asymmetrical-contact cases (figure 2(a)), the I_{TE} (regardless of the thickness d) of the symmetrical-contact Schottky diode gets reduced by an order of magnitude and the I_{TN} also gets suppressed, which can be attributed to the heightened potential barrier at the other contact. However, while scaling the device down to 5 nm, the diode length becomes shorter than the semiconductor depletion width. For this case, the tunneling distance is shortened, then the tunneling current occurs regardless of the barrier height. The tunneling ratio TRs (at $V = 1$ V) for the symmetrically contacted vertical diode with different channel lengths are illustrated in the bar graph of figure 4(b). The high value of TR (94.1% for the 3.6 nm-thick) demonstrates the dominance of tunneling transport, due to the additional Schottky barrier height significantly suppresses the thermal emission current but has a relatively weak effect on tunneling at such a scale. Specifically, we point out that here, as the channel thickness scales down to sub-5 nm, the tunneling mechanism becomes the dominant interfacial charge transport for these 2D vertical devices under a forward bias. The inset of figure 4(b) shows the FN-relation plot of tunneling currents, in which some bumps occur for low $1/V$ (voltage ranging from 0.17 to 0.24 V) and large d, due to the non-negligible effect of bulk defect density on tunneling current.

The numerical results show that the symmetric contact can be employed to maximize the tunneling current in forward bias, thus proven its priority for the design of low-voltage, ultra-scaled tunneling transistor or diode. In addition, contact engineering with large Schottky barrier height, as an effective method for suppressing reverse leakage current [42], can be helpful in maintaining the rectification behavior of sub-5 nm-thick Schottky diode.

3. Conclusion

In summary, we present a systematic framework of investigating current transport inside the vertical ultra-scaled 2D Schottky devices. Tunneling has occurred in the MoS_2-based vertical transistors, with the reduced channel layer number. By shrinking the channel length d (*e.g.* ranging from 20 to 3.6 nm) and increasing the applied bias V (electric field), tunneling effect becomes dominant over thermionic emission across the Schottky contact interface, exhibiting a tunneling ratio of 94.1% (at $V = 1$ V) for the sub-5 nm symmetric-contacted diode. Then, FNT mechanism can be clarified from TE and DT by the linear slope of the FN-relation plots: i.e. $\ln(I/V^2)$ *versus* $1/V$. Otherwise, it can be inaccurate to identify FNT by directly plotting the FN-relation of output characteristics, where the thermionic current also displays a linear-like relationship under high electric

field. These results establish the scaling limit (sub-5 nm) for the 2D nanoscale device, and provide strong theoretical support and analytical guidance for low-power, high-performance device design and further applications.

Acknowledgments

This work was financially supported by the National Key Research and Development Program of Ministry of Science and Technology (2022YFE041500), National Natural Science Foundation of China (62004065, 62274059), and Natural Science Foundation of Chongqing (cstc2021jcyj-msxmX0905).

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

ORCID iDs

Guoli Li https://orcid.org/0000-0001-7440-5295

References

[1] Lin Y C *et al* 2023 Recent advances in 2D material theory, synthesis, properties, and applications *ACS Nano* **17** 9694–747
[2] Xu Y *et al* 2023 Scalable integration of hybrid high-κ dielectric materials on two-dimensional semiconductors *Nat. Mater.* **22** 1078–84
[3] Chen W Y, Li L, Huang T, Yang Z X, Zhang T, Huang G F, Hu W and Huang W Q 2023 Extending Schottky-Mott rule to van der Waals heterostructures of 2D Janus materials: influence of intrinsic dipoles *Appl. Phys. Lett.* **123** 171601
[4] Liao L, Kovalska E, Regner J, Song Q and Sofer Z 2024 Two-dimensional van der waals thin film and device *Small* **20** 2303638
[5] Zhao T *et al* 2023 Substrate engineering for wafer-scale two-dimensional material growth: strategies, mechanisms, and perspectives *Chem. Soc. Rev.* **52** 1650–71
[6] Ali I, Dulal M, Karim N and Afroj S 2024 2D material-based wearable energy harvesting textiles: a review *Small Struct.* **5** 2300282
[7] Dong W, Dai Z, Liu L and Zhang Z 2024 Toward clean 2D materials and devices: recent progress in transfer and cleaning methods *Adv. Mater.* **36** 2303014
[8] Mondal A, Yadav P V K and Ashok Kumar Reddy Y 2023 A review on device architecture engineering on various 2D materials toward high-performance photodetectors *Mater. Today Commun.* **34** 105094
[9] Qin L, Tian H, Li C, Xie Z, Wei Y, Li Y, He J, Yue Y and Ren T L 2024 Steep slope field effect transistors based on 2D materials *Adv. Electron. Mater.* **10** 2300625
[10] Dutta T *et al* 2024 Electronic properties of 2D materials and their junctions *Nano Mater. Sci.* **6** 1–23
[11] Wang X, Liu C, Wei Y, Feng S, Sun D and Cheng H 2023 Three-dimensional transistors and integration based on low-dimensional materials for the post-Moore's law era *Mater. Today* **63** 170–87
[12] Liu A *et al* 2024 The Roadmap of 2D materials and devices toward chips *Nano-Micro Lett.* **16** 119
[13] Kim K S *et al* 2024 The future of two-dimensional semiconductors beyond Moore's law *Nat. Nanotechnol.* **19** 895–906
[14] Xu K *et al* 2017 Sub-10 nm Nanopattern architecture for 2D material field-effect transistors *Nano Lett.* **17** 1065–70
[15] Xiao X, Chen M, Zhang J, Zhang T, Zhang L, Jin Y, Wang J, Jiang K, Fan S and Li Q 2019 Sub-10 nm monolayer MoS_2 transistors using single-walled carbon nanotubes as an evaporating mask *ACS Appl. Mater. Interfaces* **11** 11612–7
[16] Guo S, Wang Y, Hu X, Zhang S, Qu H, Zhou W, Wu Z, Liu X and Zeng H 2020 Ultrascaled double-gate monolayer SnS_2 MOSFETs for high-performance and low-power applications *Phys. Rev. Appl.* **14** 044031
[17] Namgung S, Koester S J and Oh S-H 2021 Ultraflat sub-10 nanometer gap electrodes for two-dimensional optoelectronic devices *ACS Nano* **15** 5276–83
[18] Quhe R *et al* 2021 Sub-10 nm two-dimensional transistors: theory and experiment *Phys. Rep.* **938** 1–72
[19] Ma L, Tao Q, Chen Y, Lu Z, Liu L, Li Z, Lu D, Wang Y, Liao L and Liu Y 2023 Realizing On/Off ratios over 10^4 for sub-2 nm vertical transistors *nano Lett.* **23** 8303–9
[20] Tian J *et al* 2023 Scaling of MoS_2 transistors and inverters to sub-10 nm channel length with high performance *Nano Lett.* **23** 2764–70
[21] Liu L *et al* 2024 Ultrashort vertical-channel MoS_2 transistor using a self-aligned contact *Nat. Commun.* **15** 165
[22] Hu X, Huang Y, Qu H, Ye Y and Zhang S 2024 Two-dimensional ZrS_2 and HfS_2 for making sub-10 nm high-performance p-type transistors *J. Phys. Chem. Lett.* **15** 11035–41
[23] Li H-M, Lee D, Qu D, Liu X, Ryu J, Seabaugh A and Yoo W J 2015 Ultimate thin vertical p–n junction composed of two-dimensional layered molybdenum disulfide *Nat. Commun.* **6** 6564
[24] Nazir G *et al* 2018 Ultimate limit in size and performance of WSe_2 vertical diodes *Nat. Commun.* **9** 5371
[25] Liu L *et al* 2021 Transferred van der Waals metal electrodes for sub-1-nm MoS_2 vertical transistors *Nat. Electron.* **4** 342–7
[26] Wu F, Tian H, Shen Y, Hou Z, Ren J, Gou G, Sun Y, Yang Y and Ren T-L 2022 Vertical MoS_2 transistors with sub-1-nm gate lengths *Nature* **603** 259–64
[27] Li W *et al* 2022 Realization of ultra-scaled MoS_2 vertical diodes via double-side electrodes lamination *Nano Lett.* **22** 4429–36
[28] Knoch J and Appenzeller J 2008 Tunneling phenomena in carbon nanotube field-effect transistors *Phys. Status Solidi Appl. Mater. Sci.* **205** 679–94
[29] Lee G-H, Yu Y-J, Lee C, Dean C, Shepard K L, Kim P and Hone J 2011 Electron tunneling through atomically flat and ultrathin hexagonal boron nitride *Appl. Phys. Lett.* **99** 243114
[30] Bai Z, Xiao Y, Luo Q, Li M, Peng G, Zhu Z, Luo F, Zhu M, Qin S and Novoselov K 2022 Highly tunable carrier tunneling in vertical graphene-WS_2-graphene van der waals heterostructures *ACS Nano* **16** 7880–9

[31] Zhu Y, Zhou R, Zhang F and Appenzeller J 2017 Vertical charge transport through transition metal dichalcogenides—a quantitative analysis *Nanoscale* **9** 19108–13

[32] Kang J, Jariwala D, Ryder C R, Wells S A, Choi Y, Hwang E, Cho J H, Marks T J and Hersam M C 2016 Probing out-of-plane charge transport in black phosphorus with graphene-contacted vertical field-effect transistors *Nano Lett.* **16** 2580–5

[33] Sze S M and Ng K K 2008 *Physics of Semiconductor Devices* (Wiley Interscience)

[34] Appenzeller J, Knoch J, Björk M T, Riel H, Schmid H and Riess W 2008 Toward nanowire electronics *IEEE Trans. Electron Devices* **55** 2827–45

[35] 2020 *Atlas User's Manual: Device Simulation Software* (Silvaco Inc.)

[36] Chen Q, Li G, Liu Y, André N, Liu X, Xia Z, Flandre D and Liao L 2021 Origin of low-temperature negative transconductance in multilayer MoS_2 transistors *Appl. Phys. Lett.* **119** 043502

[37] Kuc A, Zibouche N and Heine T 2011 Influence of quantum confinement on the electronic structure of the transition metal sulfide TS_2 *Phys. Rev. B - Condens. Matter Mater. Phys.* **83** 245213

[38] Peelaers H and Van de Walle C G 2012 Effects of strain on band structure and effective masses in MoS_2 *Phys. Rev.* B **86** 241401

[39] Ikuno T, Okamoto H, Sugiyama Y, Nakano H, Yamada F and Kamiya I 2011 Electron transport properties of Si nanosheets: transition from direct tunneling to fowler-nordheim tunneling *Appl. Phys. Lett.* **99** 023107

[40] Wu H, Yan Z, Xie Z and Zhu S 2021 WSe_2/Pd Schottky diode combining van der waals integrated and evaporated metal contacts *Appl. Phys. Lett.* **119** 213102

[41] Xie H Q, Cui K Y, Cai X Y, Fan Z Q and Wu D 2022 Two-dimensional SiC Schottky junctions with symmetrical and asymmetrical metal electrode contacts *Appl. Surf. Sci.* **605** 154699

[42] Zhang X *et al* 2021 Near-ideal van der Waals rectifiers based on all-two-dimensional Schottky junctions *Nat. Commun.* **12** 1522