On-membrane PD SOI MOSFET with micro-heater for TID in-situ annealing: experiments versus Eldo and Atlas simulations.

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> Abstract

Silicon On Insulator (SOI) technology has improved immunity to Single Event Effects (SEE) thanks to the presence of the Buried Oxide (BOX). However, this technology remain very sensitive to the Total Ionizing Dose (TID) [1]. In recent works, we have integrated micro-heaters in the close vicinity of Partially-Depleted (PD) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), in order to study the possibility of in-situ thermal annealing to recover from TID-induced degradations [2]. A complete recovery by in-situ thermal annealing was demonstrated, after the exposure to high doses of gamma and proton radiations[1, 3]. The bulk etching technique used to perform the membrane, possibly alters the typical MOSFET's behaviour. In this paper, we use 2D Atlas simulations as well as Mentor Graphics ELDO simulations of the xfab XI10 1µm technology in order to confirm the experimentally observed trends. The simulated I-V characteristics were compared to the experimental measurements of the suspended PD SOI n-MOSFET.

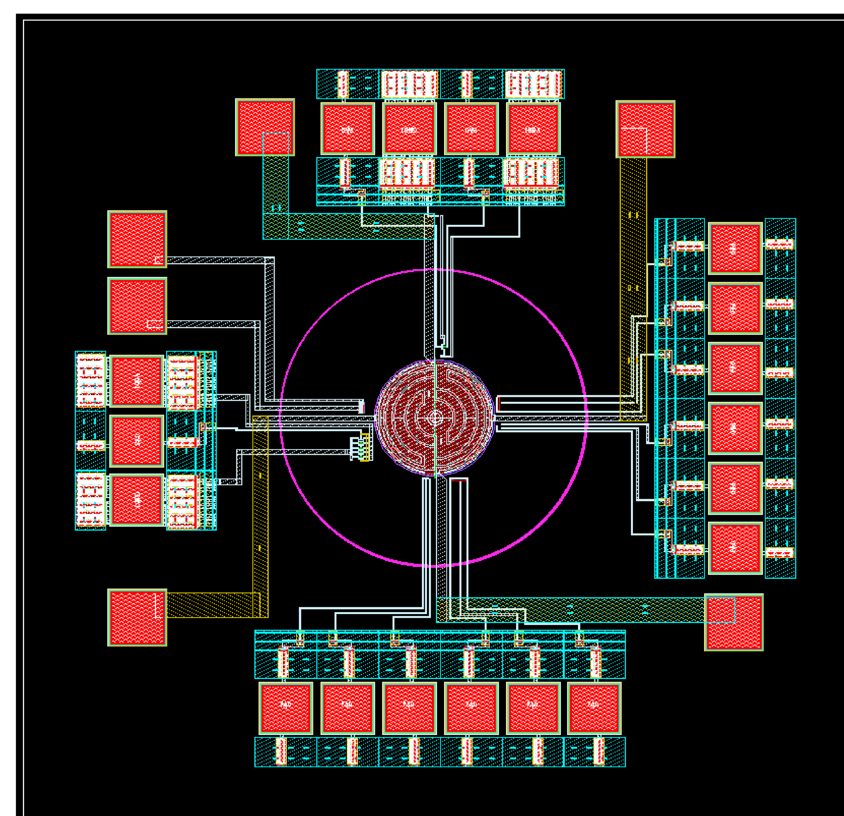
> Device description

1.0 µm PD SOI technology (XI.10 from X-fab)

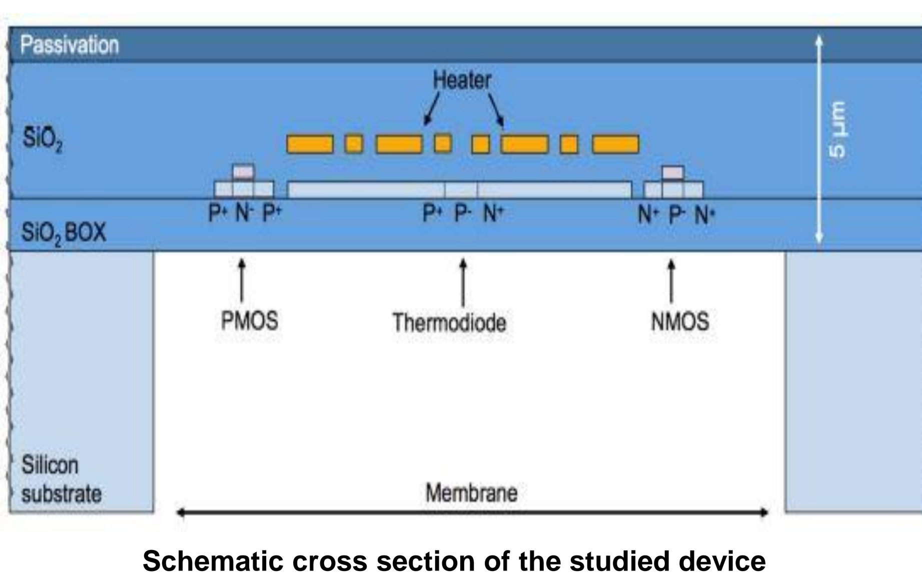
• Deep Reactive Ion Etching (DRIE) of the 400 µm thick substrate forming a 600 µm diameter membrane of 5 µm thick, where the BOX act as a back etch-stop layer.

• Circular-shaped Tungsten Joule heater with 200 µm diameter, placed in the center of membrane.

• Four n- and p-type PD MOSFETs, one inverter and lateral SOI diodes placed around the micro-heater. All the studied transistors have 1 µm channel lengths L = 1 µm and different widths of W = 6 µm and W = 24 µm for each type. The MOSFETs have a body tied to the source in order to reduce the floating body effect.



Layout overview of the device



Schematic cross section of the studied device

• The lateral PIN diode has a 20 x 10 µm footprint with an intrinsic length of 1 µm. The central PIN diode occupies all the area under the micro-heater. These two diodes are used as temperature sensors under a constant forward current bias [2-4].

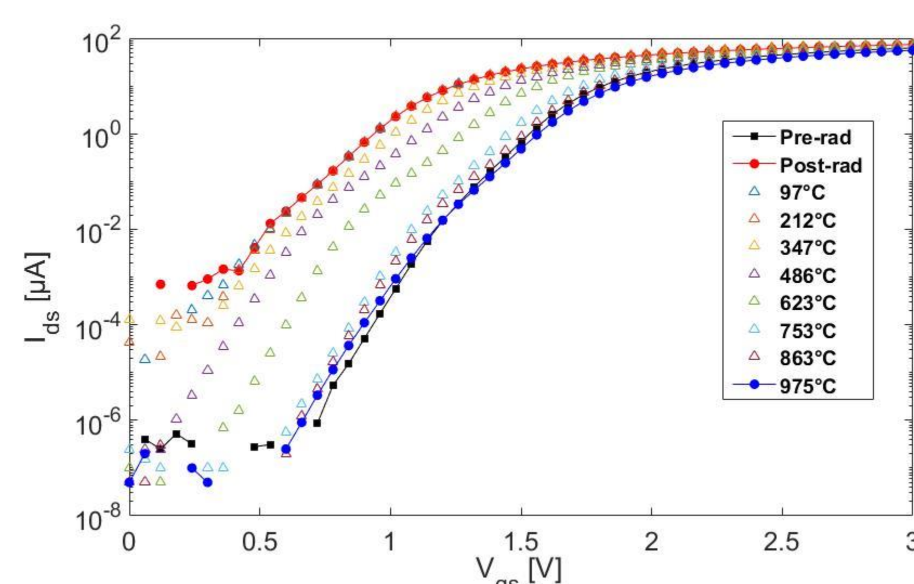
• The device was packaged in a DIL-24 ceramic package by wire-bonding, after that inserted in the Zero-Insertion-Force (ZIF) of the test fixture box and connected to a HP4145 Semiconductor Parameter Analyser by tri-axial cables for characterization.

> In-situ Thermal annealing of TID effects

• The described device, established an in-situ thermal annealing of the on-membrane MOSFETs after a **total ionizing dose of 3.5 kGy of gamma radiation**, provided by the cyclotron at UCLouvain, LLN, Belgium.

• A high temperature annealing was performed by the SOI-MEMS micro-hotplate reaching 975˚C with a maximum power consumption of 112 mW for a total annealing duration of 8.5 min.

• A partial or total recovery have been obtained, depending on the annealing temperature of the micro-heater.



The evolution of subthreshold I-V curves for the 24 µm wide mosfet after increasing temperature of the in-situ annealing steps [1]

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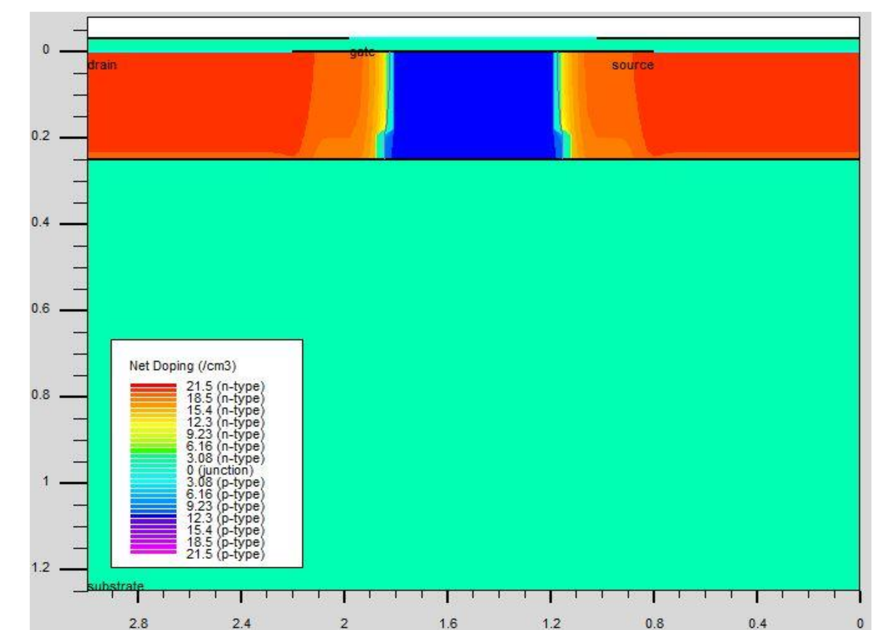
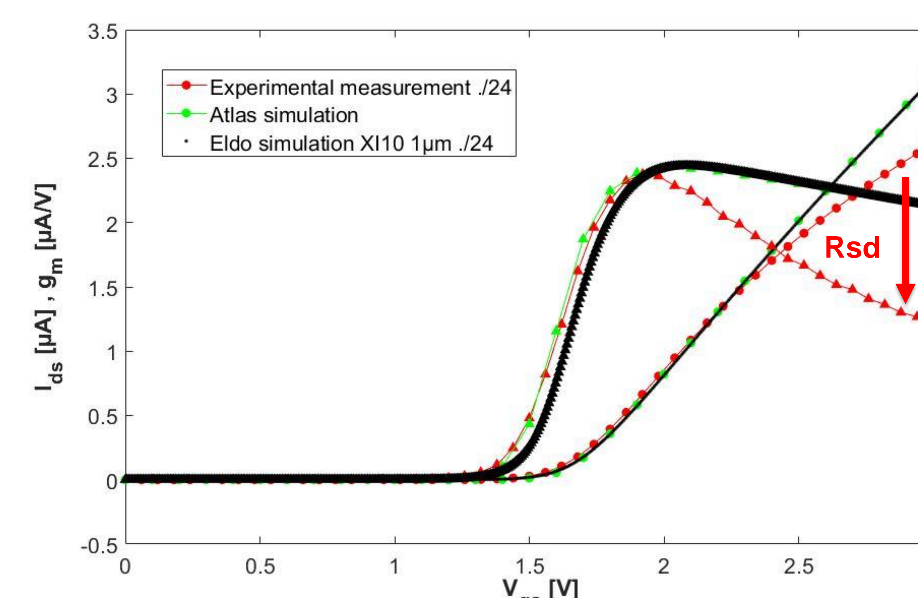
> Simulations and results

In order to simulate the on-membrane SOI n-MOSFET, 2D Atlas structure have been created with respect to the Xfab XI.10 1µm technology. Silicon substrate is etched down, BOX is 1 µm thick. As shown in the cross view, 250 nm active silicon layer is considered with a 25 nm thick gate oxide layer. A Low-Doped diffusions (LDD) extensions have been implemented between the high doped (N^{++}) Source/Drain and the p-type channel.

Parallel and perpendicular electric field, concentration and temperature mobility dependencies and carrier lifetimes effects are included in Atlas simulation.



Atlas Cross view of the Simulated 1µm technology n-MOSFET structure

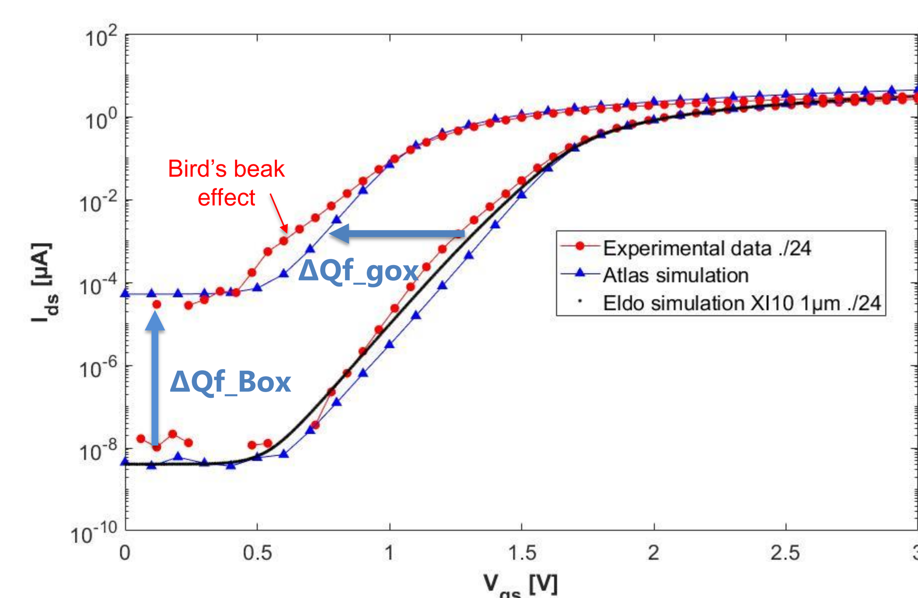


Normalized I-V characteristics of the Atlas and Eldo simulations versus experimental measurements in linear regime. Vds=60 mV.

An Eldo simulation is performed as well with the Xfab XI.10 design Kit library. Where Ids-Vds curves showed a close behavior to the Atlas simulation in linear regime. However an external series resistances (Rsd) are present in the experimental curves, caused by the different electrical cabling during the characterisation.

Threshold voltage and transconductance values of the Eldo and Atlas simulations followed by experimental measurements

	Pre-radiation		Post-radiation	
	Vth[V]	Gm[A,V⁻¹]	Vth[V]	Gm[A,V⁻¹]
Eldo simulation	1,63	2,4	--	--
Atlas Simulation	1,63	2,4	1,03	2,4
Experimental Results	1.63	2,3	1,04	2,1



Unitary subthreshold I-V curves of Atlas and Eldo simulations versus experimental measurements before and after ionizing radiation.

To simulate the TID effect and reproduce experimental results, we introduced additional fixed positive charges in the BOX and in the gate oxide. Additional charge in the BOX, Qf_box = $1,1.10^{12}$ cm^{-2} allows to reproduce the increase in the Off state leakage current. Introduction of additional charges in the gate oxide, Qf_gox=5.10^{11} cm^{-2} , in turn, allows for a good agreement with experimentally observed negative Vth shift.

After irradiation, some increase in the «edge-effect» (probably due to so-called «Bird's Beack») was observed in the experiments. This effect, being a 3D effect was not reproduced in our 2D Atlas simulations.

> Conclusions

- Atlas and Eldo simulations in linear regime confirmed the normal behaviour of the on-membrane PD SOI nMOSFET, where identical Vth and gm values are obtained. The Subthreshold slopes are quite close to the experimental measurements.
- Series Drain/Source resistances are present in the experimental measurements, but no serious effect on the Vth, max gm or subthreshold slopes.
- In-situ thermal annealing, using incorporated micro-heater, allows for partial or total recovery of the device behaviour from the TID-induced degradations.
- Experimentally observed trends can be reproduced in Atlas simulations by means of the net positive charge introduction in the gate oxide and in the BOX under radiation.

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