Reliability Analyses of Ultra-Low Voltage Analog Spiking Neurons

Grégoire Brandsteert, Léopold Van Brandt and Denis Flandre
ICTEAM Institute, UCLouvain, Louvain-la-Neuve, Belgium
Email: {gregoire.brandsteert, leopold.vanbrandt, denis.flandre}@uclouvain.be

***Abstract*—We investigate the behaviour of a bio-inspired artificial neuron, implementing a simplified Morris-Lecar model under downscaled supply voltages in the subthreshold regime towards ultra-low-power performance. The neuron spike characteristics, including amplitude, period, and typical shape, are analysed as the supply voltage is reduced. We observe a dramatic loss of the typical linear-exponential behaviour in the rising edge of the spike related to a drastic reduction in spike amplitude and an increase in spike period. These are used to define figures-of-merit of spiking operation for ad hoc neuromorphic computations. Subsequently, through Monte Carlo variability analyses, we highlight that ultra-low-voltage neurons are highly sensitive to process variations and prone to statistically likely failures. Our study evidences the challenges of maintaining stability and performance in low-power neuromorphic circuits and the importance of reliability assessments.**

***Keywords*—neuromorphic; spiking neural network (SNN); analog neuron; subthreshold , reliability; VLSI; ultra-low voltage**

I. INTRODUCTION

Computing technologies based on traditional CMOS technology and Von Neumann architecture are currently experiencing significant bottlenecks and approaching fundamental physical limits [1]. Limitations, related to processing speed, power consumption, and scalability, are prompting researchers to explore new design paradigms to overcome these challenges for information processing systems. One promising approach that receives considerable attention lies in spiking neural networks (SNNs) that are inspired by the operation of biological brains [2]. Specifically, SNNs use time-based signals, known as spikes, to process and transmit information, mimicking the temporal nature of neural communication in biological organisms.

Spiking neurons are key building blocks of SNNs that, similarly to their biological counterparts, integrate incoming spikes from other neurons over time. When the neuron internal potential reaches a critical threshold, it emits a spike, thereby transmitting information to other connected neurons through synapses [3]. This process, also known as spike-based communication, is substantially different from the continuous activation schemes used in conventional artificial neural networks (ANNs). The design and operation of these spiking neurons can be based on a variety of mathematical models, each with their own strengths and trade-offs [4].

In the context of hardware implementation, one of the main challenges is to ensure the scalability of the neurons in SNNs. As the number of neurons increases, it becomes essential to maintain a balance between computational capacity and power consumption. This is critical when neurons are to be integrated at a very large scale (VLSI) [5], similarly to the scale of biological neural networks, or for applications with strict power requirements. As a result, considerable attention has been paid to optimizing the energy efficiency of the hardware that supports these neural networks. Purely analog designs seem capable of much lower power operation compared to existing digital [6] or mixed-signal [7] circuits investigated for small scale bio-inspired SNNs.

A particularly noteworthy analog neuron architecture, presented in Fig. 1, approximating the Morris-Lecar (ML) neuronal model has been implemented in 65 nm CMOS technology in [8]. This design combines biophysical plausibility with high energy efficiency, operating in the order of a few femtojoules (fJ) per spike reported from measurements on a 65 nm CMOS prototype [8]. The architecture is highly compact, using only two capacitors in the femtofarad range and six MOS transistors, making it a promising candidate for efficient hardware implementations.

While other neuron designs have achieved even lower power consumption, down to tens of attojoules (aJ) per spike [9], these designs are often based on simpler mathematical equations such as the Leaky Integrate-and-Fire (LIF) model. Such artificial LIF neurons are unable to emulate the wide variety of dynamic behavioral characteristics of more complex

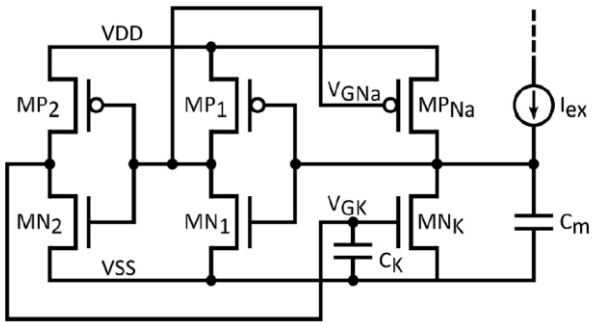

Fig. 1. Compact analog neuron design based on the Morris-Lecar model, from [8].

biological neurons [10]. This trade-off between energy efficiency and behavioral complexity is a major challenge regarding the hardware implementation of bio-inspired neural models.

The massive deployment of IoT sensor is an important motivation regarding energy efficiency. While reducing the energy consumption per spike is an important goal [11], it only represents a fraction of the total energy budget, and the quiescent energy consumption during periods of inactivity has to be accounted for. To address this issue, the present work proposes an extensive analysis of the effects of supply voltage reduction on neuron behaviour, defined by several figures of merit that we present in Fig. 2: amplitude, period and shape. In addition, the study includes process variability analysis using the Monte Carlo simulation technique to assess the circuit robustness under ultra-low supply voltage, as it operates deeper in subthreshold regime. This approach aims to explore whether further power reductions can be achieved without threatening the reliable functionality of the neuron.

II. The Simplified Morris-Lecar Artificial Neuron

The artificial analog neuron design under study is based on an approximation and simplification of the ML mathematical model appropriate in describing the dynamics of biological neurons at a relatively low computational cost [12]. In this approach, the typical response of the neuron is emulated by incorporating the exponential behaviour usually observed in biological neurons, while optimizing the design for energy efficiency. Both these goals are achieved through the subthreshold operation of MOS transistors, with gate voltages way below the transistor threshold voltages. This regime yields an exponential relationship between gate voltage and drain current, as well as low energy dissipation due to the low current and voltage values.

A brief overview of the neuron's circuit behaviour is as follows: the membrane voltage, denoted V_m, is initially set at a resting potential, typically pulled down close to the negative supply V_{SS} (set at 0 V). When a postsynaptic excitation current pulse (I_{ex}) is applied, the membrane capacitance begins to charge, causing the membrane voltage to rise linearly. When the first inverter switching voltage ($V_{switch,1}$) has been reached, the MP_{Na} transistor is activated, initiating a positive feedback loop that further increases the membrane voltage thanks to the exponential control of the drain current by the gate. This is shortly followed by negative feedback via the MN_K transistor when the C_K capacitance is fully charged. This alternance of positive and negative feedbacks creates a characteristic linear/exponential voltage increase followed by a rapid exponential discharge (Fig. 2) that mimics the action potential (or "spike") in biological neurons.

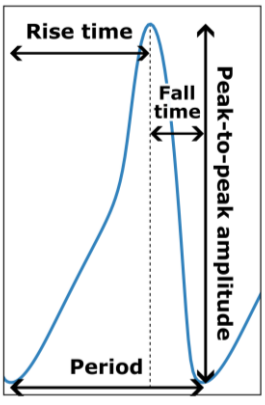

Fig. 2. Illustration of a voltage spike and definition of various the figures of merit used to characterise it.

This process of voltage rise and fall is repeated continuously as long as a sufficient excitation current (superior to 20 pA) remains present. In this architecture, the total energy consumption of the neuron is primarily determined by the supply voltage (V_{DD}) and the membrane capacitance (C_m). Hence, parameters with very low values are chosen (V_{DD} = 200 mV ; C_m = 4 fF) in order to minimize the energy requirement [8]. While both V_{DD} and C_m affect the active power consumption, the supply voltage is the major controllable parameter contributing to the static power consumption. Since the energy efficiency of a SNN is estimated to be dependent on a high spike sparsity [13], one can expect that its artificial neurons will operate with low duty cycles. The reduction of V_{DD} is therefore essential in improving the general energy efficiency of analog neurons.

III. Stability under Ultra-Low Supply Voltage

The main focus of this work is to further reduce the supply voltage below the value of 200 mV used in [8] and observe the behaviour of the circuit operating in the deep subthreshold regime. The effects of ultra-low supply voltages on the membrane voltage (V_m) are presented in Fig. 3. Three main phenomena are observable: a reduction in peak-to-peak amplitude, an increase in spike period, and a loss of definition of the typical ML spike shape, particularly the linear-exponential rise of V_m. While these observations are

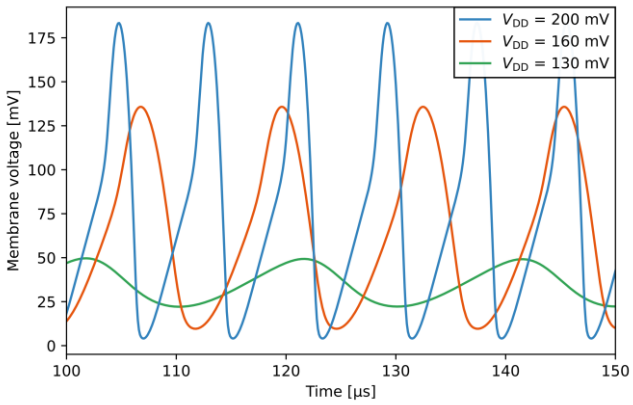

Fig. 3. Membrane voltage Vm under various supply voltages (I_{ex} = 150 pA). Illustrated case : SPICE simulation of Fig. 1, implemented in 65 nm CMOS technology with design parameters from [8].

somewhat expected, a question arises regarding the definition and quantification of a spike.

In the literature, an *action potential* or *spike* is described qualitatively as "an abrupt and transient change in membrane voltage that propagates to other neurons…" [14]. However, as the supply voltage decreases, the transient change becomes progressively less abrupt, as seen in Fig. 3. This is mainly due to the degradation of the inverters DC (lower gain, reduced noise margins [15]) and transient (longer delays [16]) characteristics for deep subthreshold regime operation. At very low supply voltages, the membrane voltage transition increasingly resembles a sinusoidal-like curve. These effects also increase the spike duration, diminishing the energetic advantages related to the potential low duty-cycle operation. As a result, it is crucial in this work to establish quantitative metrics to define the shape of the generated spike.

The first metric measures the peak-to-peak voltage of the spikes relatively to V_{DD}. This metric is particularly relevant for highly interconnected neurons subject to significant fan-out issues [17]. The second metric is the spike period, defined as the time between two local minima, which quantifies the relative deviation of the spike shape from an ideal time-localised pulse. The third metric focuses on the rising and falling times of the spike, measured as the time difference between the highest and lowest voltage points, and vice versa. The results are presented in Fig. 4-6 for three different excitation currents in the range used in [8].

Regarding the membrane peak-to-peak voltage (Fig. 4), we observe a rapid degradation in the generated spike amplitude for ultra-low supply voltages, which becomes critical if the neuron is highly interconnected, making it unable to drive the next components of the SNN. The DC switching voltage (defined as the voltage such that the inverter DC transfer curve satisfies $V_{in} = V_{out}$) of the first and second inverters ($V_{switch1,2}$) are presented by the dashed and dotted lines, respectively. It is expected that the inverters become unable to operate correctly under these limits. Therefore, minimum values of supply

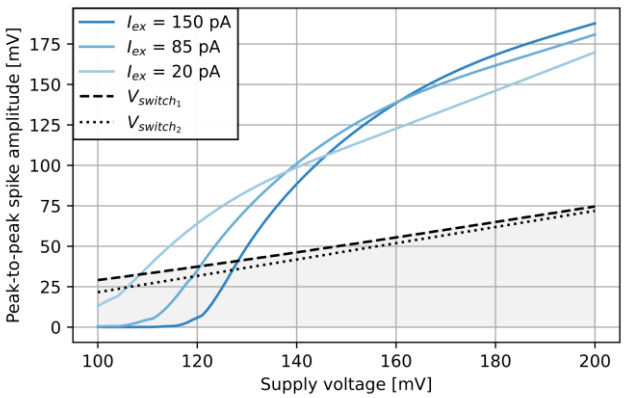

Fig. 4. Evolution of peak-to-peak spike amplitude with supply voltage for different excitation currents. The switching voltage of the two inverters are respectively shown by the dashed and dotted lines.

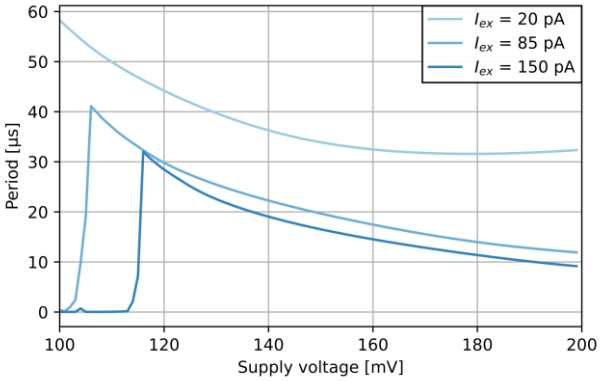

Fig. 5. Evolution of spike period with supply voltage for different excitation currents.

voltage ($V_{DD,min}$) are defined by the more restrictive dashed line for the different excitation currents, and the parts of the curves located in the greyed-out area are marked as unexploitable. The deviation from the theoretical value of $V_{DD}/2$ of the simulated switching voltages can be explained by the design parameters of the first inverter (i.e. the relative MN_1/MP_1 transistor strength) [15].

The increasing propagation delays of the inverters can be observed in Fig. 5. The spike period increases for lower supply voltages at each observed I_{ex}. The main cause seems to be the increased propagation delays of the subthreshold CMOS inverters. Note that for very low supply voltages (even below $V_{DD,min}$), the absence of spikes prevents the extraction of the period.

The rise and fall times of the membrane voltage are presented in Fig. 6. To qualitatively reproduce the biological dynamics of ion transport through the membrane, the rise time is expected to remain more important than the fall time due to the combination of linear and exponential behaviours. At voltages lower than $V_{DD,min}$, it can be observed that both times begin to merge, indicating a gradual degradation of the spike asymmetry and a loss of the biophysical plausibility of the model.

These different metrics are valuable in quantitatively comparing the generated spikes in ultra-low voltage conditions. As the spike peak-to-peak amplitude appears at this stage as the more stringent metric and has been shown to relate to the timing metrics, it will be retained in the next section where we will observe that the aggressive supply voltage reduction leads to several critical variability issues for practical neuromorphic circuit applications.

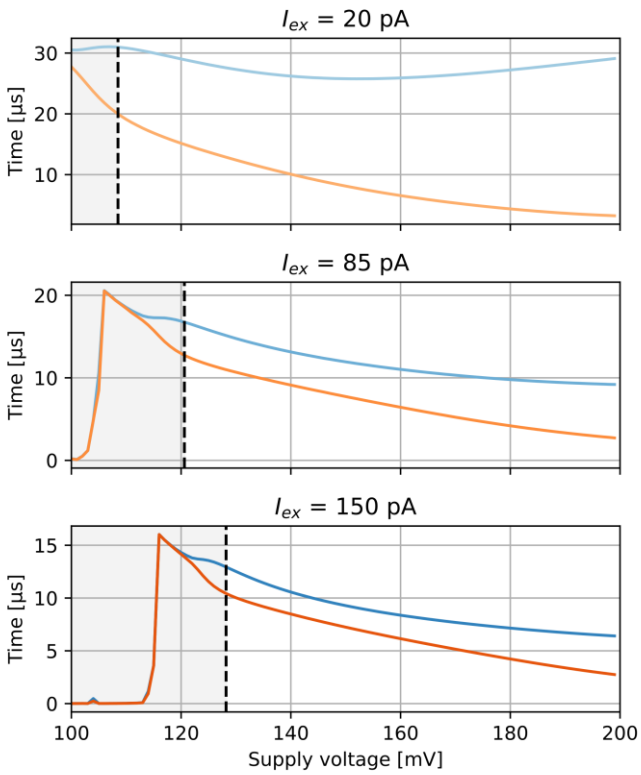

Fig. 6. Evolution of spike rise (blue lines) and fall (orange lines) times with supply voltage for different excitation currents. Respective limit supply voltages ($V_{DD,min}$) from Fig. 4 are shown by the black dashed lines.

IV. Variability Analysis

The functionality of a prospective ultra-low voltage SNN is endangered by process variations. This motivates reliability analyses at the analog neuron level. We conducted Monte Carlo simulations on the same design to examine the effects of process variability in ML-based neurons operating in the deep subthreshold regime. In Fig. 7, simulations were performed using three distinctive supply voltages (130, 160 and 200 mV) and an intermediate excitation current (I_{ex} = 85 pA). The peak-to-peak voltage amplitude, introduced in Section III, was normalized by the corresponding supply voltage to ease comparisons. This normalized metric was analysed over 10000 trials for each case, which constitutes a statistically sufficient data set moreover consistent with the number of neurons in the brains of some small insects [18] and SNNs [19]. For each Monte-Carlo experiment, random values of transistor parameters (including threshold voltage, transistor dimensions, oxide thickness and other key factors influencing circuit performance) are drawn based on the industrial compact model to faithfully simulate the effect of process variations. The normalized spike amplitude becomes a random variable taking different realisations.

These extracted realisations, plotted in histograms (Fig. 7) highlight significant shifts from the nominal values for the

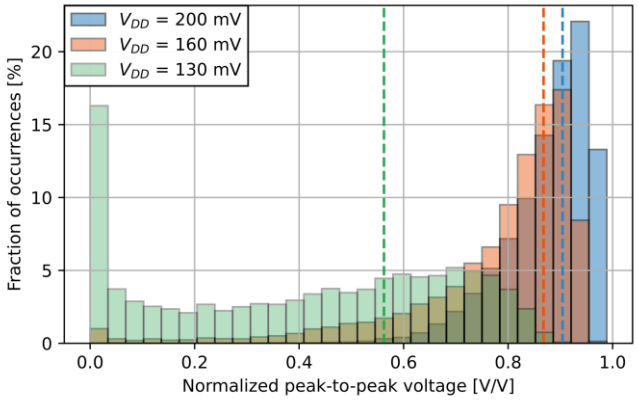

Fig. 7. Normalized spike amplitudes occurrences under various supply voltages over 10000 MC simulations. Nominal values are shown by the colored dashed lines.

three supply voltages. The general trend is that a larger fraction of spikes with lower normalized amplitudes are observed for lower supply voltages. This representation is also useful to observe the broader distribution of the spike metric, demonstrating the high variability and instability of the circuit under ultra-low voltage.

As specified in section III, we consider artificial neurons presenting peak-to-peak membrane voltages of less than $V_{DD,min}$ to be defective and establish this hard limit as criterion of functionality. Therefore, we observe in Fig. 8 the average neuron failure probability under ultra-low supply voltages for different excitation currents. The neuron variability is here analysed over 1000 Monte Carlo trials for each supply voltage, and each tested neuron whose peak-to-peak voltage is lower than $V_{switch1}$ is classified as a failure.

We observe a rapid increase of neuron failure probability with the supply voltage reduction. Note that while neurons with low excitation current are more robust under ultra-low supply voltage, they are less reliable at higher supply voltage. These results are of high importance, since it has been shown in [20] that there is a rapid deterioration of SNNs classifying accuracy proportionally to the increasing percentage of non-functioning neurons. Moreover, the effects of intrinsic transistor noise could inflate the failure probability [21] and hence require more attention.

These findings underscore the importance of carrying out thorough stability and robustness analyses for analog neurons operating in subthreshold regimes, extending our analyses to complete process, voltage and temperature variations. It also suggests that these observations could be extended to other types of energy-efficient artificial neurons, such as capacitance-less circuits [22], where the absence of traditional capacitances may further reinforce variability and noise impact.

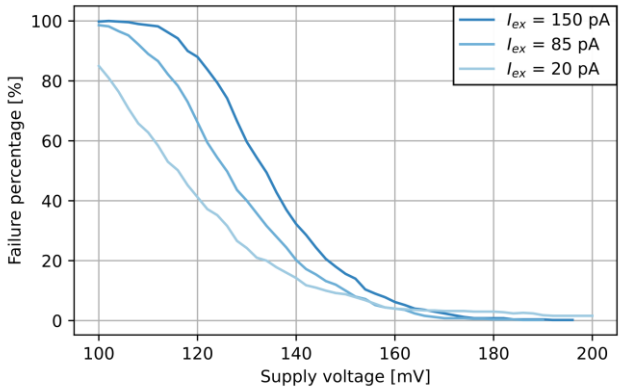

Fig. 8. Evolution of neuron failures with supply voltage for different excitation currents.

V. Conclusion and Perspectives

This work explores the behaviour of an energy-efficient artificial analog neuron based on a simplified Morris-Lecar model, to assess its performances under ultra-low supply voltage. We observed significant degradations in spike characteristics, such as reduced amplitude, increased period, and a loss of the typical biophysically plausible spike shape, as we reduce the supply voltage. The Monte Carlo variability analysis revealed that the subthreshold regime results in a high variability and instability in the neuron operation leading to high failure probabilities at low voltages. These findings highlight the importance of considering the effects of random phenomena inherent to ultra-low-voltage devices and circuits. Reducing quiescent energy efficiency while maintaining robustness and biological plausibility of spiking neurons remains a major challenge. This work emphasises the need for further investigation of the reliability of bio-inspired neurons operating at extremely low voltages.

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